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***Abstract*— This paper proposes a passive switched-capacitor single-ended-to-differential-converter (SDC) as a front-end of a differential SAR ADC, such that it can convert single-ended input signals. As the SDC is passive, the overall solution is power-efficient compared to active SDC solutions, and is especially suitable for lower/medium resolutions. As opposed to active SDC solutions with a static bias current, the proposed switched-capacitor network only consumes dynamic power, such that its consumption scales linearly with the sampling frequency. This paper discusses the basic concept of the proposed scheme, and analyzes the impact of noise and other imperfections, describes the trade-offs for power and area, and discusses the consequences for the input driver. A prototype implementation in 65nm CMOS achieves a figure-of-merit of 6.1fJ/conversion-step at 20MS/s, while reaching an SNDR of 54.7dB up to Nyquist and occupying a chip area of only 60μm × 36μm.**

***Index Terms*— Single-ended-to-differential converter, SAR ADC, switched-capacitor network, passive, low-power.**

I. Introduction

SUCCESSIVE Approximation Register (SAR) ADCs have become the architecture of choice for many low-power digitizing systems [1], for instance in the field of environmental sensing, medical wearables or implants, as well as wireline and wireless communication front-ends. Typically, such SAR ADCs have a differential input signal and use a (pseudo-) differential switched-capacitor DAC to both sample the incoming signal, and to perform the binary search algorithm to obtain the final output code [2]. A differential ADC implementation is beneficial as it improves resilience against common-mode disturbances and it results in a simple as well as symmetrical DAC implementation. However, many signal sources (like sensors, antennas, or ultrasound transducers) are originally single-ended. As a result, either a SAR ADC with a single-ended input is required, or a single-ended-to-differential-converter (SDC) is needed between the signal source and the SAR ADC, or an SDC function could be embedded inside the SAR ADC.

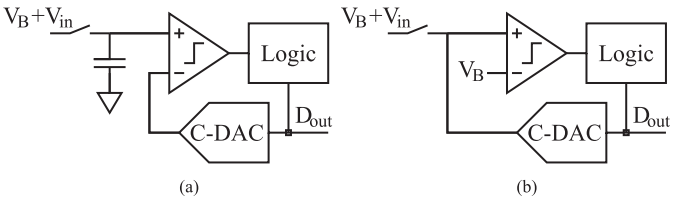

Fig. 1. Typical implementations of a single-ended SAR ADC: with a separate sampling capacitor (a), and sampling directly on the C-DAC (b).

Figure 1 shows two common options to implement a single-ended SAR ADC. In the first case (Fig. 1(a)), the input V_{in} (superimposed on a bias voltage V_B) is sampled on a capacitor, and its voltage is compared against the output of a capacitive DAC (C-DAC), which is tuned towards V_{in} using successive approximation. A disadvantage of this scheme is that it requires a dedicated sampling capacitor, and a comparator with rail-to-rail common-mode input range (assuming that V_{in} is rail-to-rail). These disadvantages are prevented with the implementation of Fig. 1(b), where V_{in} is directly sampled on the C-DAC, as for instance done in [3]. However, this requires an extra reference V_B. Also, if the comparator has a dynamic-biased input stage, impedance mismatch between the V_B node and the C-DAC may cause dynamic offset or distortion due to the charge flowing into or out of the comparator gates. The implementation in [4] mitigates impedance mismatch by connecting a C-DAC to each input of the comparator, even though V_{in} is only sampled on one side. Furthermore, a DAC switching scheme is proposed in [4] that reduces the common-mode variations, thereby reducing dynamic offset problems and relaxing the required common-mode range for the comparator.

As an alternative to a single-ended SAR ADC, an active SDC can also be placed in front of a differential ADC, e.g. as in [5]. While this can result in high SNDR, the active approach also results in an increase of power consumption, and it adds additional noise sources to the system. Moreover, since the SDC is build around an opamp, the power consumption of this approach is static, and does not scale with the actual sampling frequency.

As a third alternative, SAR ADCs with a differential C-DAC can be used, if the switching scheme of the DAC is adapted

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in such a way that a single-ended input can be sampled and converted to a differential representation prior to the actual AD conversion, as done for instance in [6] and [7]. The main advantage of this approach is that the signal is differential by the time the SAR conversion starts, and thus the common-mode level provided to the comparator is constant, thereby minimizing dynamic offset and distortion problems caused by the comparator. However, the integration of this SDC process inside the DAC results in a higher complexity in terms of the number of switches (and thus it also impacts the required interconnect and control signals). For instance, the 10-bit ADC in [6] requires 53 switches in the DAC, of which 20 are connected to ground, 20 to the supply, and 13 to an intermediate voltage level (between ground and supply). Similarly, the 8-bit ADC in [7] requires 80 switches, of which 30 are connected to ground, 34 to the supply, and 16 to an intermediate voltage level. The switches to ground and supply can often be implemented easily using NMOS and PMOS transistors, respectively. However, the other switches (13 or 16 switches in the above examples, respectively) may be more difficult to implement in advanced CMOS nodes where the V_{DD}/V_{th} ratio is limited. Clock boosting [8] or bootstrapping techniques [9] may be required to achieve sufficient linearity and bandwidth, which causes a penalty in power and area.

This paper, which is an extension of [10], proposes to use a passive switched-capacitor SDC to convert an incoming single-ended signal to a differential version before it is subsequently sampled and converted by a differential SAR ADC. Compared to the previously mentioned ADCs with an integrated SDC, the separation of the SDC and DAC capacitors results in a simplified switching scheme, requiring in total 47 switches for a 10-bit ADC, of which 21 are connected to ground, 21 to the supply, and only 5 to an intermediate voltage level. Since both the SDC operation and the signal transfer from the SDC to the ADC are fully passive, a low power consumption is possible. Moreover, the power consumption scales with the actual sampling rate as all circuits consume dynamic power only. Overall, the proposed solution achieves a small total capacitance, a low chip area, and a low power consumption. However, due to the passive charge sharing operation, this topology is mostly suitable for medium and low resolution applications, whereas higher resolutions will benefit from an active SDC or integrated SDC/ADC operation which avoids charge sharing losses.

The paper is organized as follows: in Section II, the principle of the passive SDC combined with a differential SAR ADC is introduced, and an analysis is made of the signal transfer function and the noise behavior, and the trade-offs are discussed in terms of input range, chip area, power consumption, and driver requirements. Section III describes the circuit-level implementation in a prototype chip, implemented in 65nm CMOS. Section IV shows the measurement results and evaluation, and conclusions are drawn in Section V.

II. Proposed Passive SDC Architecture Combined With a Differential SAR ADC

A. Architecture of the Passive SDC

Figure 2(a) shows the architecture of the proposed SDC, combined with a differential SAR ADC. Since the input signal

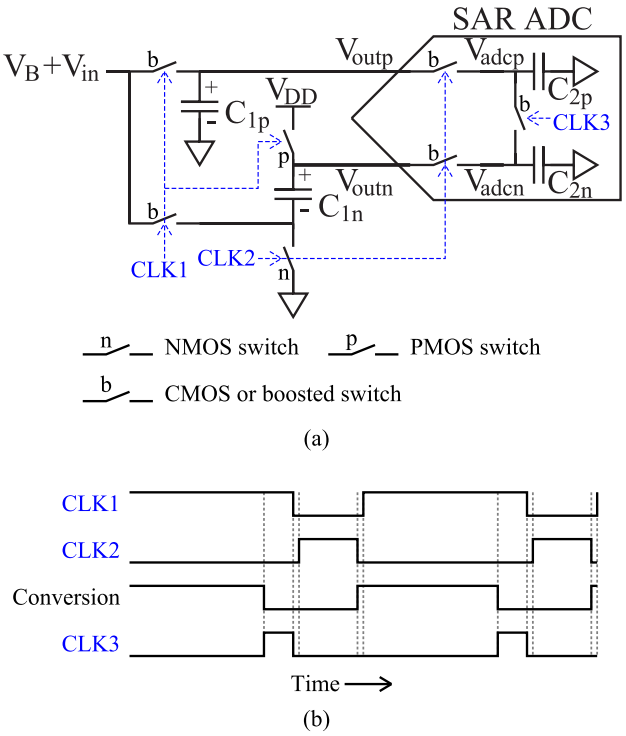


Fig. 2. Proposed passive SDC combined with a SAR ADC (a), and timing diagram (b). Modified from [10].

V_{in} is single-ended, it is superimposed on a bias voltage V_B, which is set to $\frac{1}{2}V_{DD}$. The maximum signal swing of V_{in} is thus $\pm\frac{1}{2}V_{DD}$ in case of a rail-to-rail input, but a smaller swing could also be chosen. The passive SDC is composed of two capacitors C_{1p}, C_{1n} and a number of switches to produce a differential output $V_{outp} - V_{outn}$. In Fig. 2(a), the differential SAR ADC is modeled by the input network, where the sampling switches are shown, as well as the aggregated capacitance of the differential C-DAC of the SAR ADC C_{2p}, C_{2n}, on which the output of the SDC will be sampled. The switches connected to ground and V_{DD} can be implemented with an NMOS or PMOS transistor, respectively, while the other switches require a transmission gate or boosted switch, dependent on the technology and required performance.

B. Operation of the Passive SDC

The timing diagram in Fig. 2(b) shows that $CLK1$ is high in the first phase of operation, and the SDC tracks the analog input signal on both capacitors C_{1p} and C_{1n}. However, C_{1p} is referred to ground, while C_{1n} is referred to V_{DD}. As a result of that, on the falling edge of $CLK1$, the voltages sampled on C_{1p} and C_{1n} are given by:

$$\begin{aligned} V_{C_{1p}} &= V_B + V_{in} \\ V_{C_{1n}} &= V_{DD} - (V_B + V_{in}) \end{aligned} \tag{1}$$

From these voltages, it follows that the common-mode and differential components on these capacitors are given by:

$$\begin{aligned} V_{CM} &= \frac{1}{2}(V_{C_{1p}} + V_{C_{1n}}) = \frac{1}{2}V_{DD} \\ V_{diff} &= V_{C_{1p}} - V_{C_{1n}} = 2\ V_{in} + 2\ V_B - V_{DD} \end{aligned} \tag{2}$$

Note that V_{CM} is independent of V_B and V_{in}. V_{diff} can be simplified to $2V_{in}$ if V_B is set to $\frac{1}{2}V_{DD}$. The driving circuit should set V_B rather accurately, otherwise it will lead to an offset at the output of the SDC, which reduces the dynamic range of the ADC. Next to that, interference or noise in V_B, V_{DD} or in the ground level will induce interference or noise in the differential output signal V_{diff}, which is a typical issue in single-ended systems. In theory, these disturbances can be compensated if V_B in the preceding circuit is defined as the average voltage of V_{DD} and ground (e.g. by means of a resistive divider), as this will cancel the $2V_B - V_{DD}$ term in equation (2). However, this suppression will only be effective in the bandwidth where V_B tracks V_{DD} and ground, which depends on the preceding circuit design. Alternatively, the V_B, V_{DD} and ground nodes could be designed to be relatively clean, e.g. by adding sufficient decoupling capacitors. Note that even though the SDC is passive, the signal magnitude of V_{in} is effectively doubled in V_{diff} because the input voltage V_{in} is sampled twice.

In the next phase (non-overlapping with $CLK1$), $CLK2$ will be enabled. In this phase, the ADC will track the output of the SDC, and will take a sample at the falling edge of $CLK2$. Since this process is passive, due to charge sharing, the amplitude of the signal will be affected according to the ratio of C_{1p} and C_{1n} versus C_{2p} and C_{2n}. Assuming that capacitors C_{2p} and C_{2n} were charged to V_{CM} prior to turning on $CLK2$, and assuming that $C_{1p} = C_{1n} = C_1$ and $C_{2p} = C_{2n} = C_2$, the voltages V_{adcp} and V_{adcn} after the falling edge of $CLK2$ will become:

$$V_{adcp} = V_{CM} + V_{in}\frac{C_1}{C_1 + C_2}$$
$$V_{adcn} = V_{CM} - V_{in}\frac{C_1}{C_1 + C_2} \tag{3}$$

As a result, the differential voltage V_{adc} equals:

$$V_{adc} = V_{adcp} - V_{adcn} = 2\ V_{in}\frac{C_1}{C_1 + C_2} \tag{4}$$

After the $CLK2$ phase, the actual AD conversion can be performed, as indicated by the $Conversion$ phase. In parallel, $CLK1$ can be enabled again to track the next input sample. After the conversion, before $CLK2$ will be engaged again, capacitors C_{2p} and C_{2n} should be reset to V_{CM} to ensure the condition required to obtain equation (3). To do so, capacitors C_{2p} and C_{2n} are shorted in phase $CLK3$. First of all, this removes the differential component on C_{2p} and C_{2n} so that it won't affect the next sample when charge sharing again with C_{1p} and C_{1n}, while it maintains the common-mode level. Because the common-mode voltage of the SDC is set to $V_{CM} = \frac{1}{2}V_{DD}$ in each cycle (equation (2)), and C_{2p} and C_{2n} are replenished from the SDC, the common-mode level at V_{adcp} and V_{adcn} will inherently stabilize to $\frac{1}{2}V_{DD}$ as well.

C. Noise Analysis

To analyze the amount of noise that will be ultimately sampled by the ADC due to the passive operation of the SDC, a half-circuit is drawn in Fig. 3(a). In this circuit, the input is shorted to ground as only the noise contributions from the switches need to be analyzed. In total there are four contributing steps to the final output noise at node V_{adcp}: sampling the input signal on C_1 by $CLK1$, resetting C_2 by $CLK3$, charge-sharing between C_1 and C_2 during phase $CLK2$, and final sampling on C_2 by $CLK2$. The first and second noise contributions are simply equal to kT/C terms due to sampling, but these noise quantities are sampled on C_1 and C_2, respectively:

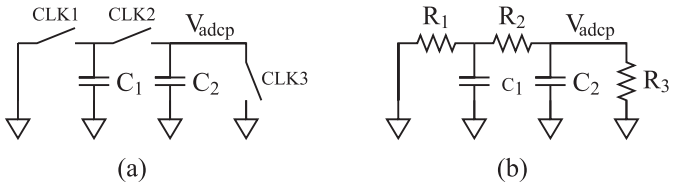


Fig. 3. Single-ended model for noise analysis (a) and equivalent model with switches replaced by resistors (b). Re-used from [10].

$$P_{n1} = \frac{kT}{C_1} \qquad P_{n2} = \frac{kT}{C_2} \tag{5}$$

During phase $CLK2$, by means of charge sharing, a fraction of P_{n1} will appear at V_{adcp}, but at the same time a fraction of P_{n2} will be removed from V_{adcp} as it is shared towards C_1. The noise power at the output can be calculated as follows:

$$P_{nout1} = \left(\frac{C_1}{C_1 + C_2}\right)^2 P_{n1} + \left(\frac{C_2}{C_1 + C_2}\right)^2 P_{n2} \tag{6}$$

Note that the capacitor ratios are squared in this equation since the calculation is in the power domain.

Furthermore, the noise of the switch controlled by $CLK2$ will add an additional kT/C term to the output at the falling edge of $CLK2$. Since C_1 and C_2 are effectively in a series loop when we sample with $CLK2$, this noise term is kT/C_{eq} where C_{eq} is the series of C_1 and C_2, thus equal to $C_1C_2/(C_1 + C_2)$. However, only a *voltage* fraction $C_1/(C_1 + C_2)$ of this term will appear on V_{adcp}, as the remaining fraction of $C_2/(C_1 + C_2)$ will appear on C_1. Thus, the noise power at the output due to sampling with $CLK2$ can be expressed as follows, where the capacitor ratio is again squared as the equation is in the power domain:

$$P_{nout2} = \frac{kT(C_1 + C_2)}{C_1C_2} \cdot \left(\frac{C_1}{C_1 + C_2}\right)^2 \tag{7}$$

By combining the contributions from P_{nout1} and P_{nout2}, the total noise at V_{adcp} can be determined and simplifies to exactly:

$$P_{nout,se} = P_{nout1} + P_{nout2} = \frac{kT}{C_2} \tag{8}$$

Finally, because the ADC is differential, the total noise power at the differential output V_{adc} will be twice larger:

$$P_{nout} = 2\ P_{nout,se} = 2\frac{kT}{C_2} \tag{9}$$

Therefore, regardless of the choice of components in the SDC, the final output noise that is sampled on the ADC's capacitors is simply given by C_2 only, and thus the noise

of the SDC plus ADC is the same as the noise that would be sampled if the ADC was used without SDC. Intuitively, this can be understood by the fact that charge sharing between the SDC and ADC adds new noise sources, but it also shares those, resulting in the same final quantity. Also note that for the continuous-time system in Fig. 3(b), where the switches of Fig. 3(a) are replaced by resistors, the total integrated noise at node V_{adcp} is also given by equation (8), regardless of the values of the resistors and capacitors.

While the above analysis shows that the noise of the SDC plus ADC equals that of the stand-alone ADC, the same is not necessarily true for the Signal-to-Noise Ratio (SNR). As shown in equation (4), the signal experiences a factor 2 passive gain thanks to sampling V_{in} on two capacitors, while it experiences attenuation due to passive charge sharing between C_1 and C_2. In practice, the ratio between C_1 and C_2 should be chosen such that for the desired input swing V_{in}, the ADC reaches its full-scale range at V_{adc}. If that is done, the SNR of the entire system will be equal to the SNR of the stand-alone ADC. Typically, $C_1 \ll C_2$ is not a practical choice, as this will produce substantial signal loss in the SDC and either implies a very large V_{in} to reach the ADC full-scale range, resulting in distortion at the input, or it implies a reduction of SNR due to not reaching the ADC full-scale range. Therefore, the situation where $C_1 \geq C_2$ is more useful, as it gives a practical input range while maintaining maximum SNR. However, a larger C_1 also comes at the cost of chip area and driver power, as will be analyzed further in Section II-E.

D. Circuit Imperfections

This section includes a brief discussion of the impact on the overall performance of various imperfections, namely: capacitor mismatch, parasitic capacitances, and non-idealities of the switches.

Mismatch between the capacitors C_{1p}, C_{1n}, C_{2p}, and C_{2n} would imply that equations (3) and (4) need to be adjusted to account for that. It can be deducted that mismatch between C_1 and C_2 results in a gain error of the entire converter, which implies the usable signal range would change, but this type of mismatch does not result in distortion. Fortunately, even with a mismatch between C_1 and C_2 of 10%, the resulting gain error would remain below 0.5dB if $C_1 \geq C_2$. If a precise gain of the system is critical, C_1 and C_2 are best implemented with the same type of capacitors. However, if precise gain is not required, different implementations could be chosen. This is relevant, because C_1 is a single capacitor in the layout, while C_2 is in practice implemented as a binary-scaled capacitor array, as it represents the C-DAC of the SAR ADC. Therefore, using different capacitor implementations can be beneficial to minimize overall chip area, at the cost of a minor gain error of the system.

A second type of mismatch is between C_{1p} and C_{1n} or between C_{2p} and C_{2n}. This may also cause a gain error, but more importantly, it creates unbalance in the differential output, which gives rise to signal-to-common-mode leakage.

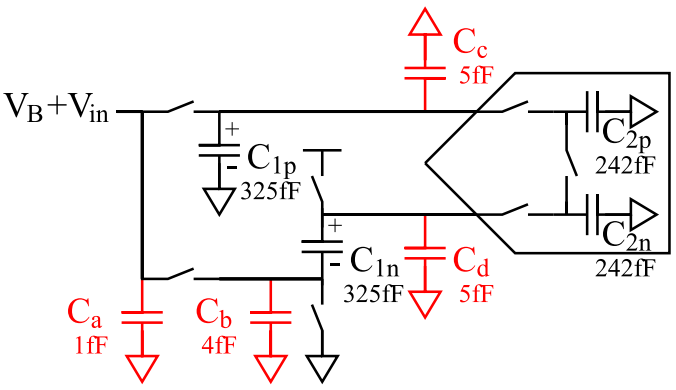


Fig. 4. Parasitic capacitors ($C_{a,b,c,d}$) in the SDC/ADC combination.

However, since C_{1p} and C_{1n} can be implemented with identical capacitor layouts (and the same applies to C_{2p} versus C_{2n}), and their values tend to be beyond 100fF for practical ADC designs, this mismatch should be rather small (e.g.: 0.1%). As a result, the impact on the common-mode should be small. Moreover, (pseudo-)differential ADC architectures are insensitive to small common-mode variations.

Similar to mismatch errors, parasitic capacitances present at the internal SDC nodes may result in various linear errors. Figure 4 shows the various parasitics (C_a up to C_d) that could be present in the SDC. Note that the specific values that are indicated can be ignored for the moment, but they match to the actual implementation that is discussed later in Section III. Parasitics C_a and C_b are initially charged from the input node. When the charge sharing towards the ADC takes place, C_a is disconnected from the rest of the network and C_b is shorted to ground, and thus these capacitors do not impact the output signals. Capacitances C_c and C_d are typically equal (or at least very similar), since they represent the parasitics of the top-plates of C_{1p} and C_{1n} and their interconnect, which can be laid out symmetrically. Since C_c is continuously in parallel to C_{1p}, it essentially just changes its value, and it can be accounted for in the design phase. On the other hand, C_d is only in parallel to C_{1n} during the charge sharing phase, but not during the phase where the input is sampled. Because of that discrepancy, C_d causes various errors in the system, including offset, a gain error, and signal-to-common-mode leakage. These errors can be modeled as follows:

$$\begin{aligned} V_{CM,adc} &= \frac{1}{2}V_{DD} + V_{CM,off} + A_{CM}V_{in} \\ V_{diff,adc} &= V_{diff,off} + A_{diff}(1+g_e)V_{in} \end{aligned} \tag{10}$$

where $V_{CM,adc}$ and $V_{diff,adc}$ describe the common-mode and differential signal components at V_{adcp} and V_{adcn}, respectively. $\frac{1}{2}V_{DD}$ represents the ideal output common-mode, and A_{diff} describes the ideal signal gain of the system (as in equation (4)). $V_{CM,off}$ and $V_{diff,off}$ describe the common-mode and differential offset, A_{CM} describes the input-to-common-mode leakage, and g_e describes the gain error, all due to C_d. From Fig. 4, these various errors can be calculated. After simplification, and assuming that $V_B = \frac{1}{2}V_{DD}$ and that

$C_d \ll C_1$, these errors can be estimated as:

$$\begin{aligned} V_{CM,off} &= \frac{1}{2} V_{DD} \frac{C_d}{2C_1} \\ V_{diff,off} &= -\frac{1}{2} V_{DD} \frac{C_d}{C_1 + C_2} \\ A_{CM} &= \frac{1}{2} \frac{C_d}{C_1} \\ g_e &= -\frac{1}{2} \frac{C_d}{C_1} \end{aligned} \tag{11}$$

In Section III, simulations on the actual circuit will be performed to verify the estimations given here. As a numerical example, if C_d is in the order of 1% of C_1, the above offsets will be in the order of a few mV, and the common-mode leakage and gain error in the order of 0.5%.

Lastly, charge injection from the various switches can also cause a gain error and offset in the system. Moreover, the switches could produce distortion. In this respect, the PMOS switch to V_{DD} and the NMOS switch to ground (in Fig. 2(a)) are not that critical since they connect to a DC level. Similarly, the reset switch in the ADC (driven by $CLK3$) is also less critical, as it always settles around V_{CM}. Distortion due to the differential sampling switches in the SAR ADC could occur, but at least the even-order distortion is suppressed here thanks to the differential operation. The most challenging switches are the two SDC input switches (driven by $CLK1$), as they need to deal with the largest signal amplitude. Moreover, since the signal is single-ended at this point, the even-order distortion of these input switches is not canceled out.

E. Design Trade-Offs

The main design choice for the proposed SDC (Fig. 2(a)) lies in the ratio of the SDC capacitance C_1 versus the ADC capacitance C_2. While C_2 determines the ultimate noise performance of the system (as determined in equation (9)), the C_1/C_2 ratio determines the input signal range, as well as the overhead in terms of chip area and power consumption. These three trade-offs are discussed in this section.

Figure 5 illustrates the overall gain of the SDC from the single-ended input V_{in} to the differential output V_{adc}, according to equation (4). For very large C_1, this gain approximates 2, which implies that a rail-to-rail differential output ($2V_{DD}$ peak-peak) can be generated from a rail-to-rail single-ended input (V_{DD} peak-peak). When $C_1 = C_2$, the overall gain is still equal to 1, but this implies that a single-ended rail-to-rail input will only generate a differential output which is 50% of rail-to-rail. For optimal use of the ADC's dynamic range, this implies that the full-scale range of the ADC should be designed at 50% as well (which will be done in the implementation that is discussed later). Alternatively, it is also possible to operate the ADC from a lower reference voltage as compared to the SDC, such that both circuits can operate rail-to-rail without requiring an excessively large C_1. However, this comes at the cost of added complexity by requiring two supplies, and level shifters for the various control signals.

The required area for the SDC is dominated by the two C_1 capacitors, while for most ADCs, the DAC capacitance

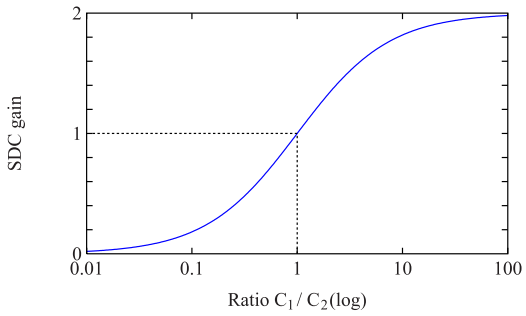


Fig. 5. SDC gain versus C_1/C_2 ratio.

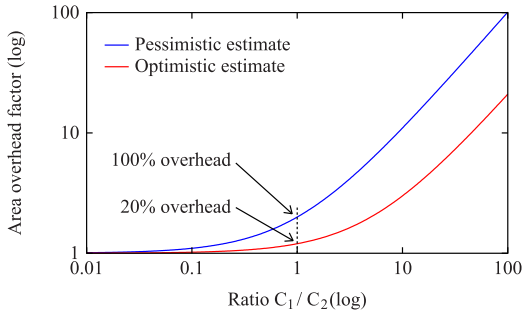
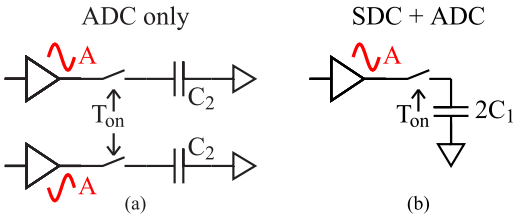


Fig. 6. SDC area overhead factor versus C_1/C_2 ratio.

is the largest contributor to the area. With these assumptions, an area overhead factor can be defined as $(A_{C_1} + A_{C_2})/A_{C_2}$, where A_{C_1} is the area of C_1 and A_{C_2} the area of C_2. This factor estimates how much larger the SDC + ADC combination is as compared to the stand-alone ADC. The area of each capacitor depends on the capacitor value, but also on the effective capacitor density. Since C_1 is a single capacitor, but C_2 is actually composed of a binary-scaled capacitor array with additional interconnect, the effective capacitor density for C_2 tends to be lower than that of C_1. Figure 6 shows the area overhead as function of the capacitor ratio, where the pessimistic estimate assumes that the capacitor density is the same for C_1 and C_2, while the optimistic estimate assumes that the capacitor density for C_1 is 5× higher than the density for C_2. As a result, the area overhead of the SDC is estimated between 20% to 100% when C_1 and C_2 are equal.

The second form of overhead from the SDC is in the form of added power consumption, which has several components: first, the SDC + ADC combination requires in total 3 clock signals (Fig. 2), and thus some additional logic is needed. $CLK1$ and $CLK2$ can be generated easily from a single clock using a conventional non-overlapping clock generator [11], which requires few gates and will cause negligible overhead. $CLK3$ can be derived from $CLK1$ and the end-of-conversion signal, which is usually already present in asynchronously clocked SAR ADCs [2]. Therefore, the clock generation is expected to cause negligible overhead in power consumption. A second contribution to the power consumption is due to the extra switch drivers. In particular, the switches driven by $CLK1$ and $CLK3$ may require voltage boosting, and this will cause an overhead in power consumption. Besides the increase in power consumption inside the SDC, it is also relevant to analyze the impact of the passive SDC on the power



	A (relative)	C	b	T_{on}
ADC	$C_1 / (C_1 + C_2)$	C_2	2	< 50%
SDC + ADC	1	$2C_1$	1	> 50%

(c)

Fig. 7. Driver scenarios in case of differential ADC (a) or SDC + ADC (b), and comparison of typical driving parameters (c).

consumption of the input driver. For instance, a large value of C_1 will result in a higher peak current of the input driver to charge the capacitor quick enough, resulting in a higher power consumption. While the design of the input driver is beyond the scope of this work, a simplified analysis is performed to compare two scenarios: in the first case (Fig. 7(a)), the differential ADC without SDC is driven by input buffers directly (either 2 single-ended drivers, or a differential driver, or an active SDC). In the second case (Fig. 7(b)), the SDC is driven by a single-ended input buffer, while the ADC is passively driven by the SDC. By comparing these two scenarios, it can be estimated how the power consumption of an input driver compares if the differential ADC is driven directly, or if it is driven via the proposed SDC.

In general, the power consumption of a driver for a switched-capacitor ADC is determined by the required peak current, which depends on: the amplitude (A) of the signal, the size of the capacitive load (C), the number of current branches (b), and the on-time of the switch (T_{on}), according to the following trend:

$$P_{driver} \propto \frac{A \cdot C \cdot b}{T_{on}} \tag{12}$$

Figure 7(c) indicates the (relative) values of these parameters for both scenarios. The relative amplitude for both scenarios is given by the signal gain (equation (4)), where the factor of 2 is omitted now as that is already accounted for in the differential structure (Fig. 7(a)). The capacitive load (per side) is C_2 for the ADC, while the SDC effectively sees two capacitors of C_1 in parallel. The number of current branches b is 1 for a single-ended driver and 2 for a differential structure (as it requires two single-ended drivers, or a differential driver which has two current paths as well). The last parameter, T_{on}, depends on the sampling period T_s of the ADC and how this is divided in a tracking time T_{track} and a conversion time T_{conv}. For the scenario in Fig. 7(a), T_{on} is equal to T_{track}. Dependent on the ADC, T_{track} may be 50% of T_s, but often T_{conv} is set well beyond 50% of T_s to allocate more time for the conversion process. This unavoidably reduces T_{track} and thus T_{on} to <50%. As opposed to this first scenario, for the scenario in Fig. 7(b), the on-time overlaps with the conversion time of the ADC ($T_{on} \approx T_{conv}$), as can be seen in Fig. 2(c)

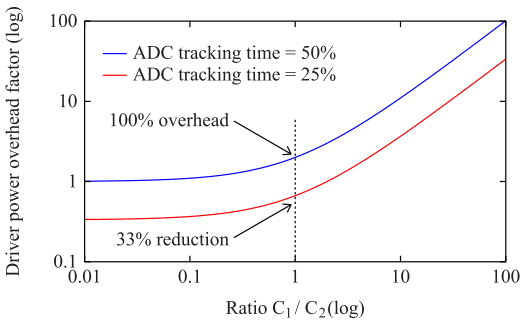


Fig. 8. Overhead factor of the input driver power consumption versus C_1/C_2 ratio.

where $CLK1$ overlaps with $Conversion$. As a result, T_{on} for this scenario tends to be >50%.

When substituting the values from Fig. 7(c) in equation (12), the power of the driver for the SDC, relative to the power of the driver for the ADC, can be determined:

$$\frac{P_{driver,SDC}}{P_{driver,ADC}} = \frac{(C_1 + C_2)}{C_2} \frac{T_{track}}{T_{conv}} \tag{13}$$

Based on this equation, Fig. 8 shows the estimated power consumption of the driver in case of the SDC, relative to the case without the SDC. For illustration, tracking times of 50% and 25% are shown, leading to on-times of 50% and 25% for the ADC driver and on-times of 50% and 75% for the SDC driver. Logically, the power overhead for the SDC increases with larger C_1. However, when $C_1 = C_2$, there might be either an overhead or a reduction of power, dependent on the ADC's tracking time. Since it is usually easier to design a SAR ADC with a relatively short tracking time rather than a short conversion time, and the passive charge sharing between C_1 and C_2 can be fast because it is not limited by driver bias current, this effect is advantageous for the proposed SDC in view of the overall system power consumption.

F. Discussion

In the previous section, the signal gain, and the overhead in terms of area and power consumption for the SDC were analyzed. It can be concluded that a large C_1/C_2 ratio ($\gg 1$) is not attractive, as this would result both in a large area penalty and excessive power consumption in the input driver. On the other hand, a small C_1/C_2 ratio ($\ll 1$) is also not attractive due to signal attenuation, which likely results in a sub-optimal ADC range. Therefore, the most practical choice would be to select a capacitor ratio around 1, where the area overhead can be reasonable, and the driver power may even be reduced. The impact of this choice though is that the signal range at the ADC will be far less than rail-to-rail. This would be an inefficient choice for high-resolution converters, as they tend to be thermal noise limited, and thus they benefit from a maximum possible signal range. On the other hand, for medium-to-low resolution converters, the noise level plays a less prominent role, and therefore the reduced signal swing can be acceptable.

In terms of sampling rate and signal bandwidth, it is expected that the proposed SDC can cover a wide range

of frequencies. Moreover, since the power consumption is dynamic, the efficiency will scale with the sampling rate inherently. For very high-speed operation, two main limitations are expected. First, the sampling networks for C_{1p} and C_{1n} are non-symmetric, which may lead to different high-frequency characteristics. Secondly, the switches have a $\frac{W}{L}$-sizing trade-off between charge-injection and on-resistance. As a result, high-speed design might come at the cost of linearity.

III. Passive SDC and SAR ADC Implementation

A prototype design of the passive SDC and a differential SAR ADC was made in 65nm technology. A resolution of 10bit and a sample rate of 20MS/s were chosen for the ADC, to enable a wide variety of sensor applications. Thanks to the dynamic and passive nature of the circuitry, it could be applied equally well to other sample rates.

A. Capacitor Implementation

Since power-efficiency and chip area of both the ADC and the SDC will be degraded when using large capacitors, a key optimization strategy is to minimize C_2 of the ADC, which will subsequently also minimize C_1. For that reason, the ADC presented in [12] is reused in this work. This is a 10bit switched-capacitor SAR ADC, using asynchronous timing as published in [13], and a comparator as in [14]. The most important feature is the implementation of the DAC capacitors. To minimize the value of the LSB capacitors towards the noise limit, these are implemented with delta-length capacitors. Essentially two large capacitors with a slightly different value are switched in an opposite direction to effectively create a very small (delta) value. In this way, as shown in Fig. 9(a) and explained in more detail in [12], very small capacitors can be made. Moreover, an accurate binary scale of capacitors can be made by scaling the length difference, rather than using multiple identical elements in parallel, thereby reducing chip area. An equivalent single-ended model of the ADC is shown in Fig. 9(b), showing the input sampling switch, the DAC, and the comparator. The indicated capacitor values are based on post-layout extraction. Thanks to the delta-length approach, the effective LSB capacitance is only 125aF, the effective DAC capacitance ($1024C_\Delta$) is 128fF, and the subtracted capacitance and parasitics yield a C_p of 114fF. Thus, the total input capacitance C_2 equals 242fF. As shown in Fig. 9(b), only the input signal needs an analog switch, while the bottom plates are switched between ground and V_{DD}, which can be done by digital inverters. Due to the presence of C_p, the differential full-scale range of the ADC is given by:

$$V_{adcrange} = 2\frac{1024C_\Delta}{1024C_\Delta + C_p}V_{DD} \approx 1.06 \cdot V_{DD} \qquad (14)$$

Combining equations (4) and (14), the value of C_1 was set to 330fF (based on post-layout extractions) to reach a single-ended input range of about $0.9V_{DD}$. Note that the use of delta-length capacitors suits well in this work for two reasons: first, it results in a small effective capacitance C_2, and secondly, it results in a reduced full-scale range of the ADC (due to parasitics and subtracted capacitance), which

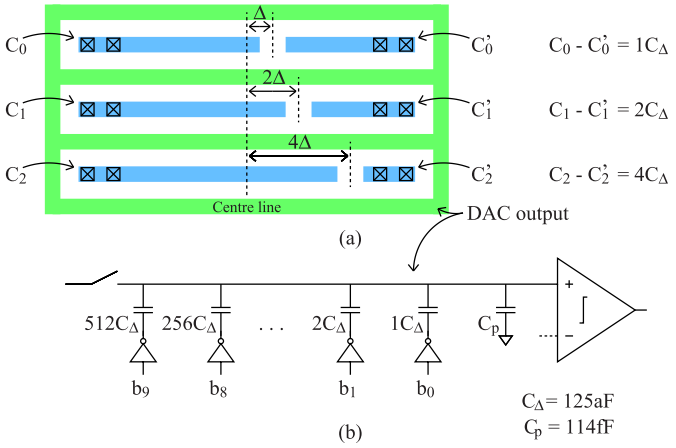


Fig. 9. DAC layout sketch (a) and equivalent single-ended model (b). Re-used from [10].

matches the signal reduction due to the passive SDC operation. Note that despite the small value of C_2 and the reduced signal swing, the kT/C-related SNR of the ADC (equation (9)) is still above 66dB (with $V_{DD} = 1$V). A conventional switching scheme is used in the DAC [2]; even though this is not very power-efficient by itself, thanks to the small value of C_2, the DAC's power consumption will still be small compared to the overall ADC consumption.

With the above values, the signal and noise levels of the stand-alone ADC and the SDC/ADC combination can be determined. An overview is given in Table I. First of all, the signal and noise levels of the differential ADC are referred to $V_{adc} = V_{adcp} - V_{adcn}$ in Fig. 2, while those of the SDC/ADC combination are referred to V_{in}. Both circuits use the same supply of 1V, which is also re-used as the reference voltage in the ADC. Based on the chosen value of C_1 (330fF) and the given value of C_2 (242fF, from the ADC in [12]), the gain factor of the SDC can be calculated as 1.15, based on equation (4). The full-scale peak-to-peak range of the ADC follows from equation (14). Then, the rms value can be determined by dividing this by $2\sqrt{2}$. Also, the LSB step size of the ADC follows from the peak-to-peak range divided by 1024 (the number of levels of a 10-bit ADC). Hence, the quantization noise (which is per definition equal to 0.289 LSB) can be calculated as well. The two dominant thermal noise sources are the comparator noise and sampling noise. The comparator, using the architecture in [14], was sized such that it achieves a noise level equal to the quantization noise, based on transient noise simulations. The sampling noise is calculated according to equation (9). The overall ADC input-referred noise can be determined by combining the 3 noise sources (in the power domain). Relative to the signal power, this results in an estimated SNR of 58dB for the ADC. For the SDC/ADC combination, the values are simply scaled back with the gain factor to refer them to V_{in}. As a result, the estimated SNR is identical in this case. It should be noted that the SNR estimate is optimistic, as for instance the noise contributions from the reference voltage, the supply, and the DAC drivers are ignored.

A parasitic extraction was performed on the top-level layout to determine the parasitic capacitances in the SDC network.

TABLE I

ESTIMATED SIGNAL AND NOISE LEVELS FOR THE ADC AND COMBINED SDC PLUS ADC

	ADC only	SDC + ADC
Referred to signal node (Fig. 2)	V_{adc}	V_{in}
$V_{DD} = V_{REF}$ [V]	1	1
Gain factor (eqn. (4))	N/A	1.15
Full-scale range [V_{pp}]	1.06	0.9
Full-scale signal [V_{rms}]	0.37	0.32
LSB step [mV]	1.04	0.90
Quantization noise [mV_{rms}]	0.30	0.26
Comparator noise [mV_{rms}]	0.30	0.26
Sampling noise (eqn. (9)) [mV_{rms}]	0.18	0.16
Total noise [mV_{rms}]	0.46	0.40
SNR [dB]	58	58

TABLE II

SIMULATED AND ESTIMATED ERRORS DUE TO PARASITICS

	Simulated	Estimated, eqn. (11)
$V_{CM,off}$	+3.8mV	+3.8mV
$V_{diff,off}$	-4.4mV	-4.4mV
A_{CM}	+0.75%	+0.77%
g_e	-0.76%	-0.77%

The values are summarized in Fig. 4, which includes all parasitics with a value of ≥1fF. Smaller parasitics were ignored due to their negligible impact. Table II summarizes the various simulated imperfections due to capacitive parasitics. These simulated results match very well to the estimated impact based on equation (11).

B. Switch Implementation

To implement the switches in the SDC and ADC (Fig. 2(a)), the switches towards V_{DD} are implemented with a single PMOS transistor while the switches towards ground are implemented with a single NMOS transistor. For all other switches, clock boosting is applied [8], since transmission-gate switches in this technology do not have a sufficiently low on-resistance to enable high-speed operation. In total, three independent clock boosting circuits are needed: one for each of the clock domains $CLK1$, $CLK2$, and $CLK3$. All switches (NMOS, PMOS, boosted switches) have an identical size for simplicity of design. The switch dimensions were optimized for the SDC input switches, as these are the most critical ones (see Section II-D). The linearity of a single clock-boosted NMOS switch followed by a 330fF sampling capacitor was simulated at a sampling rate of 20MS/s and input amplitude of 0.9V, mimicking one of the input switches of the SDC. Figure 10 shows the simulated results as function of the input signal frequency for different switch dimensions. As can be seen, a larger $\frac{W}{L}$ degrades the low frequency performance, which is due to an increase of HD2 caused by charge injection. However, for smaller $\frac{W}{L}$ values, the linear bandwidth is reduced due to an increase of on-resistance. As a compromise, a size of $\frac{W}{L} = \frac{4.8\mu m}{60nm}$ was selected, as it maintains similar performance in the entire bandwidth, and can achieve 10-bit linearity.

C. Logic Implementation

A simplified overview of the asynchronous logic in the ADC, together with a simplified state machine, is given in Fig. 11. This system implements the behavior as sketched

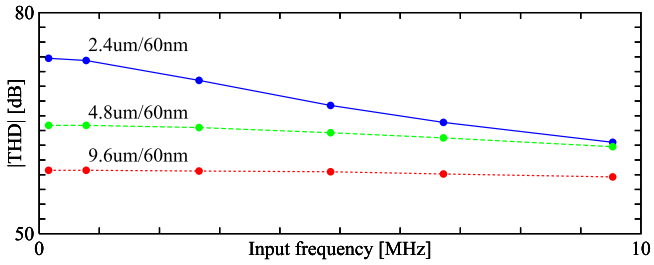


Fig. 10. Simulated THD for the SDC input sampler for different switch sizes.

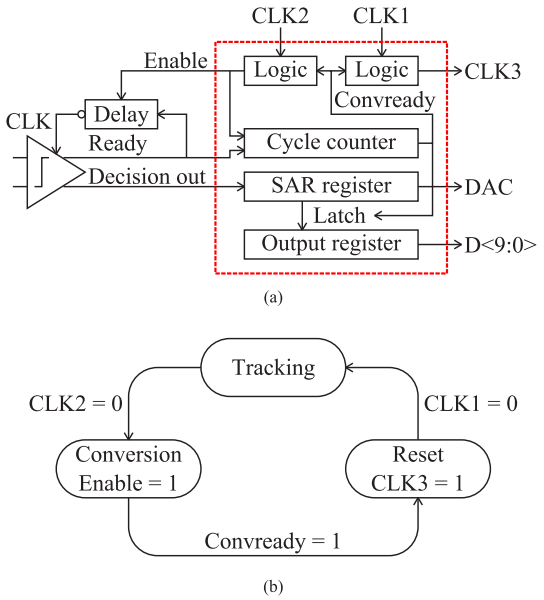


Fig. 11. Overview of the asynchronous ADC logic (a) and simplified state machine (b).

in Fig. 2(b). To save active power and leakage in the logic design, the circuitry is partially based on asynchronous dynamic logic [2]. For flexibility, the clock signals $CLK1$ and $CLK2$ are provided externally with a duty-cycle of 72% and 25%, respectively. This sets the tracking time of the SDC to 72% of the sampling period, while the conversion process and reset phase can take up to 75%. As explained earlier, these clocks could also be derived from a single external clock source using a basic non-overlapping clock generator [11]. As shown in the state machine, a falling edge of $CLK2$ will move the ADC from the *Tracking* state to the *Conversion* state. The *Enable* signal will enable a self-oscillation loop around the comparator as described in [13] and [15]. A cycle counter is incremented each cycle to keep track of the active bit cycle, while the consecutive comparator results are stored in a temporary SAR register that controls the DAC. Once the cycle counter reaches the final state, a *Convready* indication will disengage the *Enable* signal, it will copy the temporary SAR register to the output register by creating a *Latch* pulse, and shift the ADC to the *Reset* state. In this state, the cycle counter and SAR register are reset, and $CLK3$ is enabled to reset the DAC capacitors (Fig. 2(a)). Finally, a falling edge on $CLK1$ will return the ADC to the *Tracking* state.

D. Layout Implementation

The overall layout of the design is shown in Fig. 12, where the SDC occupies $24\mu m \times 36\mu m$ and the ADC occupies

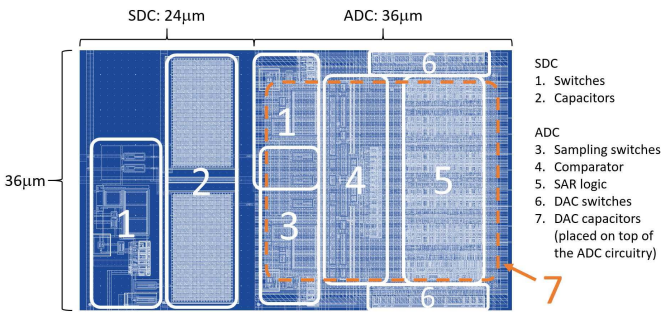


Fig. 12. Overall layout of the SDC and ADC. Re-used from [10].

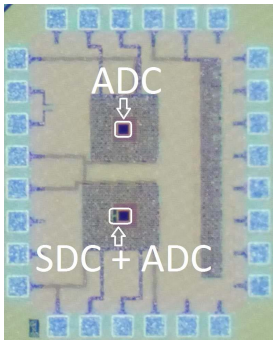


Fig. 13. Die photo with separate instances of a stand-alone ADC and a combined SDC + ADC. Areas are 36μm$\times 36\mu$m and 60μm$\times 36\mu$m, respectively. Re-used from [10].

$36\mu\text{m} \times 36\mu\text{m}$. Both C_1 and C_2 capacitors are implemented with MOM capacitors. However, the DAC capacitors (C_2) are implemented on two metal layers (6 and 7) only, such that the ADC's active circuitry can be placed underneath (using up to metal layer 3 for interconnect), while metal layers 4 and 5 are used to shield the circuitry from the DAC capacitors. An advantage of doing this is that the interconnect between the DAC switches and the DAC capacitors is mostly vertical, which shortens the connections and saves area otherwise needed to route the interconnect. On the other hand, the C_1 capacitors require far less interconnect, and are thus implemented as MOM capacitors with metal layers from 3 to 7, resulting in a much higher capacitor density. Effectively, the area for C_1 is approximately $4\times$ smaller than that for C_2, even though the capacitance of C_1 is larger than that of C_2. As a result, the SDC area overhead is relatively modest, as also estimated in Section II-E. In Fig. 12, it can also be noted that the 5 boosted switches (indicated by #1 and #3) occupy a relatively large area due to the required charge pumps. On the other hand, the area for the 40 PMOS / NMOS switches in the DAC (indicated by #6) and the PMOS and NMOS switches in the SDC (included in #1) is far smaller, as these switches are small. This result confirms the validity of the approach to minimize the number of rail-to-rail switches as motivated in Section I. The die photo in Fig. 13 shows the implemented test chip, where a stand-alone differential ADC is placed besides the combined SDC with ADC for benchmarking purposes.

E. Power Breakdown

Lastly, the power consumption of the stand-alone ADC is compared against that of the SDC + ADC combination.

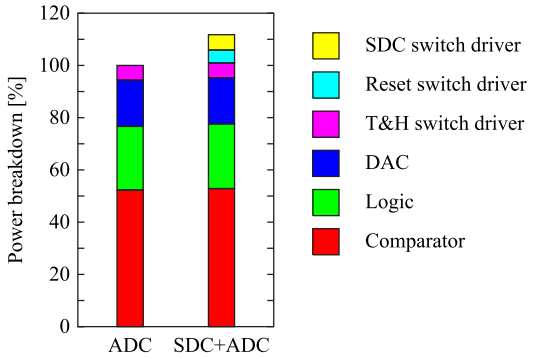


Fig. 14. Power breakdown based on post-layout simulations.

Figure 14 shows the simulated power breakdown using post-layout simulations, where the numbers are normalized to 100% for the stand-alone ADC. It can be seen that the SDC adds an overhead of 12%, which is almost entirely due to the two extra charge pumps (one for the SDC input switches driven by $CLK1$, and one for the ADC reset switch driven by $CLK3$). One can further note that the DAC consumption is relatively modest (18%) thanks to the small delta-length capacitors, despite using a conventional switching scheme. Lastly, based on the selected capacitor values and selected clock duty cycles, it is estimated based on equation (13) that the SDC + ADC combination would save up to 18% of power in the input driver as compared to the stand-alone ADC.

IV. Measurement Results

The implemented prototype was measured at 1V supply and 20MS/s sample rate. In the measurements, V_B was manually set to the mid-code of the ADC, which indirectly also compensates the offset of the entire system. Other than that, all results are obtained without any calibration. A near-Nyquist spectrum is shown in Fig. 15 for both the stand-alone ADC and the SDC + ADC combination. It can be observed that the SDC + ADC has a 1.6dB lower SNDR due to increased HD2, but also due to other spurious components that are visible in the spectrum. Later analysis revealed that part of this is due to the measurement setup, as a system with a single-ended input is more sensitive to disturbances injected into the input signal as compared to a differential system, which rejects at least the common-mode disturbances. After improving the cables for the input signals, new results (for the same chip) were obtained as shown in Fig. 16. Now, the SNDR loss is reduced to 0.8dB. Figure 17 shows the SNDR and SFDR for both designs as function of the input frequency. Note that this measurement was done prior to the improvement of the input signal cabling, and thus it could be on the pessimistic side. However, in this case, the SDC + ADC combination has an average SNDR loss of 1.6dB compared to the stand-alone ADC.

The INL and DNL using a $5 \cdot 10^6$-sample histogram test are shown in Fig. 18. This measurement is done after improvement of the input signal cabling. Note that the stand-alone ADC and the ADC in the SDC/ADC combination use a physically separate copy of the ADC in the same chip. As a result, random capacitor mismatches are different for the two instances, resulting in different INL/DNL patterns for

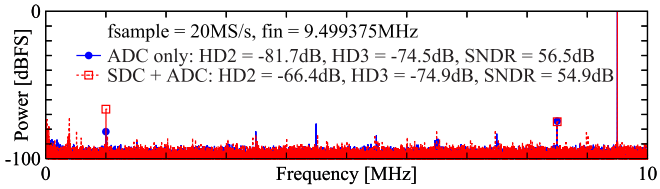


Fig. 15. Measured frequency spectrum for the ADC and for the SDC + ADC. Modified from [10].

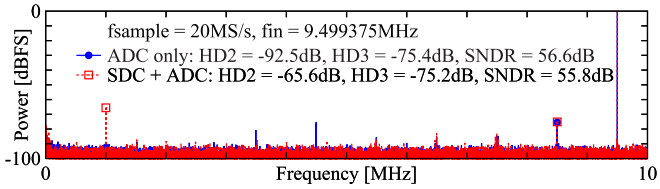


Fig. 16. Measured frequency spectrum for the ADC and for the SDC + ADC with improved input signal cabling.

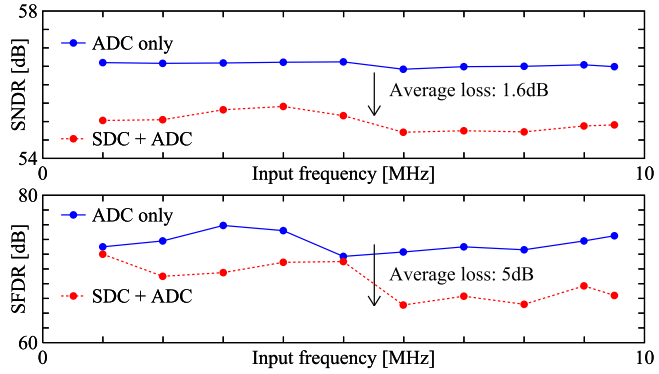


Fig. 17. Measured SNDR and SFDR for the ADC and for the SDC + ADC. Re-used from [10].

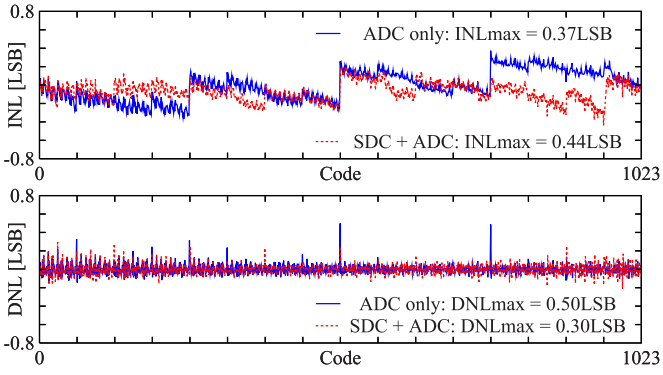


Fig. 18. Measured INL and DNL for the ADC and for the SDC + ADC.

both designs. As a further test, Fig. 19 shows the maximum INL and DNL for 5 measured samples. The average results are nearly identical (within 0.08LSB) for the SDC + ADC combination versus the stand-alone ADC, making it plausible that the static linearity is limited by ADC mismatch rather than distortion caused by the SDC.

Figure 20 shows the measured SNDR and SFDR for the same 5 samples. Here, the average SFDR and SNDR losses of the SDC + ADC combination relative to the stand-alone ADC are 9dB and 0.6dB, respectively. Note that the measured SNDR values (all between 55.7dB and 56.6dB) are relatively close to the estimated SNR of 58dB (Section III), even though

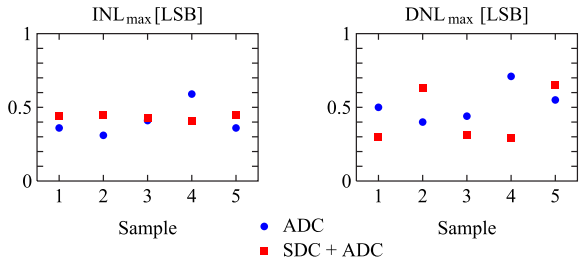


Fig. 19. Measured maximum INL and DNL for 5 samples.

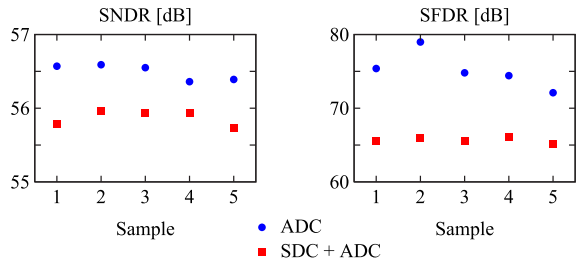


Fig. 20. Measured SNDR and SFDR for 5 samples.

TABLE III
MEASURED PERFORMANCE SUMMARY AND COMPARISON IN ADC MODE

	[5]	[4]	[3]	[6]	[7]	This work
Topology	Active SDC + SAR ADC	SAR ADCs with single-ended input				Passive SDC + SAR ADC
Technology [nm]	180	180	180	180	40	65
Resolution [bit]	12	8	12	10	8	10
F_{sample} [MS/s]	0.2	0.01	0.1	0.1	1	20
Total cap [pF]	5.4 *	7	15	18	2.8	1.1
Input range [V]	2.6	1.2	0.8	1.0	1.8	0.92
Supply [V]	2.8	1.1	1.0	1.0	0.9	1.0
Power [µW]	1160	0.127	3.8	1.72	29.7	54
INL [LSB]	0.76	0.81	0.8 #	0.45	0.40	0.60
DNL [LSB]	0.48	0.28	0.6 #	0.50	0.48	0.38
SFDR [dB]	80.4	61.9	64.2	63.6	65.8	65.1
SNDR [dB]	64.2	46.3	58.4	58.8	45.9	54.7
FoM [fJ/c.step]	4376	63.4	56	24.1	189.6	6.1
Area [mm²]	0.25	0.06	0.24	0.118	0.00986	0.0022

* ADC capacitors only, excluding SDC capacitors
# Estimated from provided graph, measured at 10bit resolution

the SNR estimate was optimistic, and the measured SNDR also includes distortion due to e.g. mismatch and switches.

The measured power consumption of the ADC (49μW) increases to 54μW when adding the SDC, which is mostly caused by the extra clock boosting circuits as also estimated in Fig. 14. Thanks to the dynamic power consumption, it can scale down with the sampling frequency down to a leakage level below 100nW (Fig. 21).

Table III summarizes the results of this work and compares it against prior SAR ADCs with a single-ended input. It should be noted that, due to the differences in technology, one cannot fairly compare the achieved power efficiencies. However, the capacitor size is a dominant parameter deciding power consumption and chip area. The proposed design has the smallest total capacitance (accounting for both the capacitors in the DAC and the SDC), which effectively results in the smallest area, a low power consumption, and an easier load for the input buffer. Next to that, as explained in Section I, this design has a relatively small number of rail-to-rail switches, which is also beneficial for chip area and power consumption. In terms of

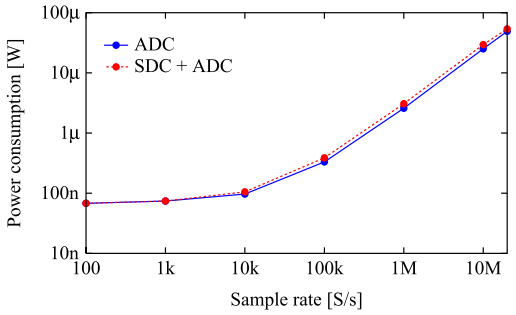


Fig. 21. Measured power consumption vs sampling frequency.

input swing and linearity, this work is similar to, but does not outperform prior-art.

V. Conclusion

A passive switched-capacitor single-ended-to-differential-converter (SDC) as a front-end of a differential SAR ADC was presented. Compared to active SDC solutions or single-ended SAR ADCs, the proposed solution offers the smallest total capacitance and a relatively low number of switches, which is advantageous for both the power efficiency and the chip area. A noise analysis showed that the passive SDC does not result in a noise penalty of the overall system. An analysis of the design trade-offs revealed that the SDC overhead in terms of area can be kept small, while it may even have benefits in terms of input driving requirements. The trade-offs also reveal that the proposed concept is mostly suitable for medium/low resolution converters due to the reduced ADC input signal range. A prototype implementation in 65nm CMOS achieves a figure-of-merit of 6.1fJ/conversion-step at 20MS/s, while reaching an SNDR of 54.7dB up to Nyquist and occupying a chip area of only 60μm $\times$ 36μm.

References

[1] B. Murmann. (Jun. 2021). *ADC Performance Survey 1997–2021*. [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

[2] P. Harpe *et al.*, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[3] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1V 3.8μW 100kS/s SAR ADC with time-domain comparator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 246–247.

[4] W. W. Hu, Y.-T. Liu, T. Nguyen, D. Y. C. Lie, and B. P. Ginsburg, "An 8-bit single-ended ultra-low-power SAR ADC with a novel DAC switching method and a counter-based digital control circuitry," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 7, pp. 1726–1739, Jul. 2013.

[5] M.-R. Kim, Y.-O. Kim, Y.-S. Kwak, and G.-C. Ahn, "A 12-bit 200-kS/s SAR ADC with hybrid RC DAC," in *Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS)*, Nov. 2014, pp. 185–188.

[6] C. Yuan, K. A. Ng, Y. P. Xu, S.-C. Yen, and N. V. Thakor, "A 1-V 9.8-ENOB 100-kS/s single-ended SAR ADC with symmetrical DAC switching technique for neural signal acquisition," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2015, pp. 1–4.

[7] S. Chaput, D. Brooks, and G.-Y. Wei, "An area-efficient 8-bit single-ended ADC with extended input voltage range," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1549–1553, Nov. 2018.

[8] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[9] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[10] M. van der Struijk, K. Pelzers, and P. Harpe, "A passive single-ended-to-differential-converter with SAR ADC achieving 6.1fJ/conversion-step," in *Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2021, pp. 288–291.

[11] B. Nowacki, N. Paulino, and J. Goes, "A simple 1 GHz non-overlapping two-phase clock generators for SC circuits," in *Proc. 20th Int. Conf. Mixed Design Integr. Circuits Syst. (MIXDES)*, 2013, pp. 174–178.

[12] P. Harpe, "A compact 10-b SAR ADC with unit-length capacitors and a passive FIR filter," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 636–645, Mar. 2019.

[13] P. Harpe, E. Cantatore, and A. van Roermund, "A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/conversion-step," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3011–3018, Dec. 2013.

[14] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9μW 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 244–245.

[15] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.

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