60 GHz Transceiver Circuits in SiGe-HBT and CMOS Technologies

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Zusammenfassung

Die Erhöhung der Übertragungsrate von Kommunikationssystemen ist von hohem wissenschaftlichem und wirtschaftlichem Interesse. Die stetige Fortentwicklung dieser Systeme, sowohl unter Aspekten der Hard- als auch der Software, hat ein neues Technologiezeitalter eingeläutet. Verschiedene Szenarien, auf optischen, drahtgebundenen und drahtlosen Technologien basierend, wurden für diese Anwendungen entwickelt. Im 60 GHz ISM-Band (57 GHz bis 65 GHz) ist wegen der hohen Absorptionsverluste bei dieser Frequenz eine Kurzstrecken-Kommunikation mit hoher Datenrate von besonders hohem Interesse. Die Realisierung solcher Systeme erfolgt aufgrund von Kosten- und Massenproduktions-aspekten auf Basis von SiGe-HBT und CMOS Technologien.

Schlüsselparameter eines 60 GHz-Transceivers sind eine hohe Ausgangsleistung, niedrige Rauschzahl, geringer Stromverbrauch und niedrige Herstellungskosten. Um den gesamten Frequenzbereich des 60 GHz ISM-Bandes abdecken zu können, wurden zahlreiche Transceivertopologien weltweit diskutiert. Die verfügbare Technologie mit ihren Schlüsselparametern f_t, f_{max} stellt hierbei eine wichtige Randbedingung dar.

In dieser Arbeit werden Aspekte des 60 GHz-Transceiver-Designs unter Verwendung einer 0,25 µm SiGe-HBT- und einer 90 nm CMOS-Technologie untersucht. Zunächst wird die Modellierung von passiven und aktiven Komponenten diskutiert. Verschiedene Techniken zur Modellextraktion basierend auf Messungen und elektromagnetischen Simulationen werden gezeigt. Für die wichtigsten passiven Bauelemente werden skalierbare Modelle entwickelt, um das Entwurfsverfahren zu präzisieren. Im nächsten Schritt werden 60 GHz CMOS- und SiGe-HBT-Leistungsverstärker untersucht. Basierend auf diesen Studien wurden zwei HBT und zwei CMOS-Endstufen konzipiert, realisiert und gemessen. Infolge der Verfügbarkeit einer hochgenauen Bauelemente-Bibliothek, ausgereifter Entwurfstechniken und der Verifikation auf Basis von EM-Simulationen konnte an den gemessenen Leistungsverstärkern eine hohe Ausgangsleistung mit guter Effizienz nachgewiesen werden. Die Ergebnisse zeigen weiterhin eine gute Übereinstimmung von Simulationen mit Messungen. Weiterhin wurden auf Basis einer 90 nm CMOS Technologie ein Heterodyne und ein OOK Transceiver entwickelt. Der Heterodyne-Transceiver mit einer Zwischenfrequenz von 20 GHz genügt dabei dem IEEE 802.15.3c Standard und erreicht eine Performance auf Höhe des internationalen Standes von Wissenschaft und Technik. Für den OOK Sender wurde eine neue Topologie entwickelt. Bei diesem Konzept bilden Modulator und Leistungsverstärker eine Einheit, woraus Vorteile hinsichtlich Ausgangsleistung, Effizienz und Chipgröße resultieren. Mit dieser Schaltung wurde in einem Systemtest eine Übertragungsrate von 6 Gbps über eine Entfernung von 4 m erfolgreich nachgewiesen.

Summary

The rise of high-data-rate hungry applications has brought a new dawn to telecommunication technologies in both hardware and software development aspects. Different scenarios, mainly based on optical, coaxial and wireless systems, have been developed for these multi-gigabit communication systems. In these scenarios, the wireless system is utilized for indoor and short-range communication, which can ease the requirements on RF power and noise figure of the transceivers. However, the demand for multi-gigabit communication imposes a broadband performance requirement upon these wireless transceivers. This broadband performance requirement can be within the range of 2 GHz to 10 GHz. In order to cover such a broad frequency range, different transceiver circuit topologies have been suggested by many circuit designers. Due to the high oxygen loss in the 60 GHz range this 57 GHz to 65 GHz ISM band has attracted attention for high speed short-range communication. Moreover, the newly emerged low cost technologies (like, CMOS and SiGe HBT) have further attracted the industry to explore this communication band.

The main requirements for a 60 GHz transceiver are high output power, low noise figure, low power consumption and broadband performance. To cover the whole 57 GHz to 65 GHz frequency band, numerous transceiver topologies are under discussion. The key parameter f_t, f_{max} of the available technology define the achievable system performance.

In this thesis, multiple aspects of the 60 GHz transceiver design based on the 90 nm CMOS and 0.25 µm SiGe HBT designs have been investigated. First, the modeling of passive and active components is presented. These components include capacitors, inductors, transformers, transmission lines, transistors, matching networks and RF pads. Different techniques for model extraction based on measurements and electromagnetic simulations have been examined. For inductors, transformers and capacitors scalable models have been developed. Further, the design techniques of 60 GHz CMOS and SiGe HBT power amplifiers have been studied. Based on these studies, two HBT and two CMOS power amplifiers have been designed, realized and measured. Due to accurate modeling and design techniques, high performance and good agreement with simulation has been achieved. Finally, two different types of transmitters (Heterodyne and OOK) based on the CMOS technology have been developed. The heterodyne transceiver, with an IF frequency of around 20 GHz, has been designed based on the IEEE 802.15.3c standard. This transmitter has achieved state of the art results with respect to output power, conversion gain and efficiency with a small chip size and low power consumption. For the OOK transmitter, a novel topology has been developed. In this topology, the modulator and the power amplifier have been integrated into one circuit. Due to many advantages of this new topology, this transmitter achieves higher output power and efficiency compared with state-of-the-art results. Furthermore, the realized circuit has been utilized within a wireless system where more than 6 Gbps has been successfully transmitted over a 4 m distance.

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List of Abbreviations

3D	Three dimensional
AC	Alternating Current
CAD	Computer aided design
CG	Conversion gain
CMOS	Complementary metal-oxide semiconductor
DC	Direct current
DUT	Device under test
EM	Electro-magnetic
f_t	Transient frequency
f_{max}	Maximum oscillation frequency
G_{MAX}	Maximum stable gain
HBT	Heterojunction bipolar transistor
HF	High frequency
HFSS	High frequency structural simulator
IC	Integrated Circuit
IF	Intermediate frequency
IP3	Third-order intercept point
K	Stability factor
LNA	Low noise figure
NF	Noise figure
NoF	Number of fingers
OP_{1dB} (P_{1dB})	Output power at 1dB compression point
PA	Power Amplifier
P_{sat}	Saturated output power
P_{1dB} (OP_{1dB})	Output power at 1dB compression point
PAE	Power added efficiency
P_{OUT}	Output power
PLL	Phase locked loop
RF	Radio frequency
Rx	Receiver
Si	Silicon
SiGe	Silicon-Germanium

Tx	Transmitter
TRx	Transceiver
VCO	Voltage controlled oscillator
W	The width of the single finger of the CMOS transistor
W_{tot}	Total width of the CMOS transistor

1 Introduction

High data-rate, wireless communication is demanded by many applications, such as for the Internet, video streaming for high definition TV and short-range data transfers (Fig. 1). Most of these applications are foreseen for short-range and indoor purposes with multi-user access. Due to the high data-rate, short-range and multi-user requirements, a large frequency bandwidth for operation is required by these applications.

Within the microwave frequency band (300 MHz to 30 GHz), the only available band which can offer the required large bandwidth for these purposes, is the 3.1 GHz to 10.6 GHz unlicensed band, which can be used for ultra-wideband (UWB) applications. The main problems with this frequency band are the difficulties in developing such broadband circuits at such a low frequency (as center frequency to bandwidth division is quite low) as well as the very low equivalent-isotropic-radiated-power (EIRP) restriction defined by the FCC [31] (-41 dBm for indoor applications), which further limits the data communication in both data-rate and communication distance aspects. Fig. 2 presents the overall mask requirement by the UWB application defined by the FCC [31].

Fig. 1 Indoor wireless communication scenario.

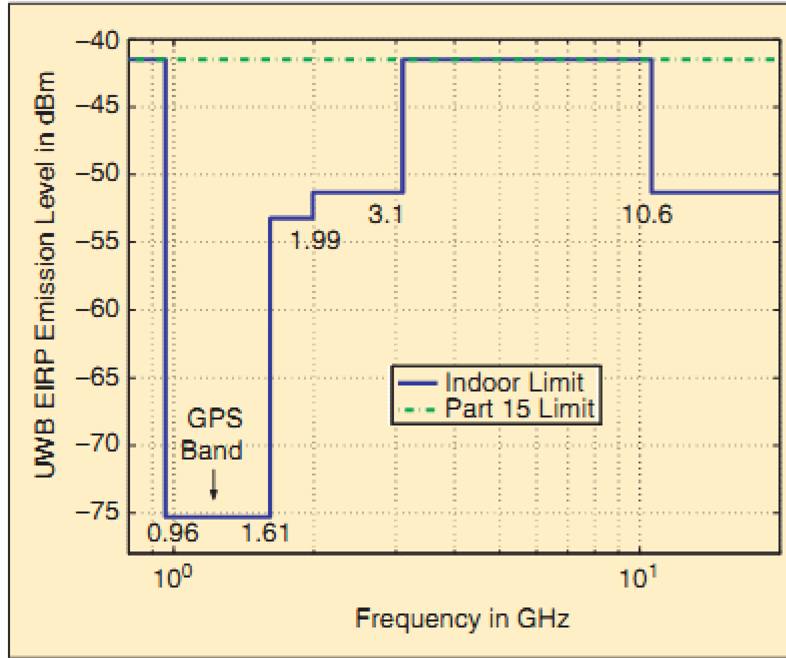


Fig. 2 FCC requirement for indoor EIRP of the UWB system [31].

Unlike the microwave band, the millimeter wave band offers an attractive opportunity for these scenarios. The unlicensed 60 GHz ISM band, with an 8 GHz bandwidth (57 GHz to 66 GHz), offers an opportunity to circuit designers to develop circuits for the above mentioned applications. Due to the high center frequency in comparison with the bandwidth, designing broadband circuitries is much easier for this frequency band. In addition, based on the IEEE 802.15.3c standardization [32], a much higher EIRP can be used within this frequency band (Table. 1) in comparison with the UWB, which further facilitates a high data-rate communication system design.

Table. 1 Maximum transmitted power levels in different regions

Region	**Max. output power**	**Max. EIRP**	**Regulatory document**
USA	□	indoor: 27 dBi outdoor: 40 dBi	47 CFR 15.255
Japan	10 dBm Max. bandwidth: 2.5 GHz	57 dBi	ARIB STD-T69, ARIB STD-T74
Australia	10 dBm	51.8 dBi	Radio communicat. Class License 2000

Besides the above mentioned advantages of the mm-wave band, the recent developments in the CMOS and Bipolar technologies have further facilitated the mass production and low cost development of mm-wave chips. According to the ITRS roadmap [33], CMOS technologies with more than 400 GHz f_t and f_{max} are expected to be commercially available in the market (Fig. 3), while the HBT technologies with more than 400 GHz f_t and f_{max} are already accessible [34].

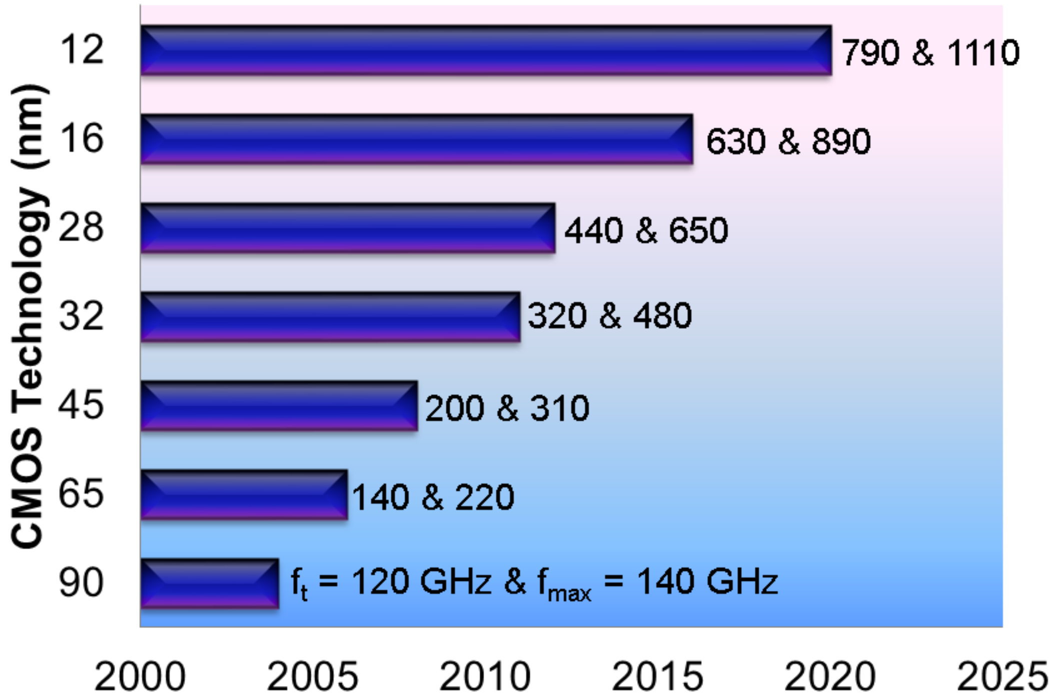


Fig. 3 ITRS CMOS downscaling roadmap [33].

Despite many advantages and progresses, designing for the mm-wave frequency faces many obstacles. Mainly lying in the passive and active components models and process variations, these problems are hard to solve. As to the issue of modeling, these challenges mainly include the extraction of the parasitic and coupling elements of passive components and the Q-factor maximization of inductors or tank circuits. Since λ/4 is in the same order as the length of the on-chip transmission lines (T.L.), the coupling elements along with parasitic elements play an important role in determining the behavior of the circuit. Moreover, the substrate conductance in some of these technologies is an obstacle for circuit design. For example, the resistivity of the substrate can vary from 50 Ohm cm in the 0.25 µm HBT BiCMOS technology to 2 Ohm cm in the 90 nm CMOS technology. Such a low ohmic substrate resistance in the CMOS technology can deteriorate the Q-factor of the passive components and, therefore, requires the employment of shielding techniques.

Even by including all of the parasitic and coupling elements at the simulation level, many discrepancies can be seen during measurement. These are mainly due to technological variations. In this case, all the designs must pass the worst-typical-best case scenarios for the models. These model conditions are more important for the active components and are usually provided by the foundries.

All these problems result in discrepancies between the simulated and measured performances. Consequently, these deviations in each of the RF front-end components (PA, LNA, Mixer, PLL, etc.) lead to the performance degradation of the total system. In this context, the main challenges for circuit designers are to minimize all these discrepancies, particularly at the mm-wave band, by using different EM simulators (2D, 2.5D, 3D) to extract all the parasitic and coupling elements, applying different techniques for highly tolerant designs (e.g., broadband designs) and checking process variation effects on circuit performances (e.g., Monte Carlo simulation).

Regardless of all these efforts in modeling, characterization and simulation, meeting all the system requirements is quite a big challenge in these technologies. Mainly due to limitations in the transistor performance, achieving high output power in the PAs and a low noise figure in the LNAs is quite challenging. In the PAs, many considerations, like PA core optimizations and high Q-factor matching network design must be included in the design procedure. Moreover, many power combining techniques - like Wilkinson, transformer and current-combining - must be utilized to improve the output power performance of the PA.

All the above-mentioned problems and considerations make the mm-wave circuit design quite challenging and require the extensive study of all aspects of the circuit development. In this work, the 60 GHz front-end design is studied. Different circuits, based on the SiGe HBT and Si CMOS technologies, have been designed, realized and measured. In these designs, different techniques to minimize discrepancies between the simulated and measured results, to increase the tolerances of the circuit and, finally, to improve their performance, have been investigated.

This work is organized as follows:

Chapter 1 is the introduction.

Chapter 2 describes all the modeling techniques that have been used in this work. These modeling techniques include the EM simulation techniques for the extraction of all the parasitic and coupling elements from the passive structures in both the 0.25 μm HBT and 90 nm LP CMOS technologies. Further, the model extraction of the active and passive components through measurements in the 90 nm LP CMOS technology has been investigated. Finally, scalable models have been developed for some of the passive components to facilitate the circuit design procedure. All the models have been extracted up to 100 GHz.

Chapter 3 presents the design procedures for different HBT PAs. The main required considerations for these designs are investigated. Based on these design procedures and considerations, two different types of amplifier have been developed. In the first amplifier, broadband performance with medium output power has been targeted, while in the second PA a transistor core extension based on the current-combining technique for high output power achievement has been investigated. Further, all the designed PAs have been realized and measured. Due to accurate modeling and design techniques the measured results showed good agreement with the simulation. In the low power PA, the broadband gain and input-matching covers the whole V-band (50 GHz up to 70 GHz) with 20 dB gain. Moreover, the large signal performance of the PA shows 15 dBm output power and 15% PAE. In the high power PA, owing to the optimized transistor core, 3 dB higher output power (18 dBm) has been achieved with almost the same PAE (14%) and 15 dB small signal gain at 60 GHz.

Chapter 4 continues with the PA design investigation in the 90 nm Si CMOS technology. In this part, the PA design procedure and considerations for the CMOS technology are investigated. As the CMOS transistor shows quite poor output power performance, different power combining techniques have been studied for output power improvement. Based on these power combining techniques, two PAs with a Wilkinson power combiner and transformer have been designed. Although the transformer-based PA consumes almost 2 times more DC power, the designs show the much smaller chip size and higher performance of this PA in comparison with the Wilkinson power combined PA. The Wilkinson power combined PA shows 11 dBm output power, 8 dB gain and 6% PAE with 100 mW DC power consumption and 0.45 mm^2 active chip size, while the transformer-based PA achieves 14 dBm output

power, 20 dB gain and 10% PAE with 200 mW DC power consumption and 0.065 mm^2 active chip size.

Chapter 5, investigates the design of two different types of transmitters (heterodyne and OOK) based on the CMOS technology. The heterodyne transceiver with an IF frequency at around 20 GHz was designed based on the IEEE 802.15.3c standard. In comparison with the other state-of-the-art results, these transmitters - with a small chip size and low power consumption – have achieved during the measurement a high P_{OUT} (13 dBm to 15.5 dBm), efficiency and conversion gains (Table. 25). These advantages are mainly due to the transformer-based PA that was used. Moreover, thanks to the accurate design of the Gilbert cell mixer, much higher isolations were achieved in this work in comparison with the other state-of-the-art PAs.

Further in this chapter, the design and measurement of a 60 GHz OOK transmitter has been investigated. In this transmitter, a new technique has been utilized to simultaneously increase the transmitted bitrate and minimize the power consumption and chip size. In this case, a new topology has been developed. In this topology, the OOK modulator and the PA are integrated into one circuit. Further, the modulator is designed for the maximum bitrate, no DC power consumption and a small chip size. Moreover, by utilizing accurate models and designing appropriate matching networks, a high performance PA has been realized. With this topology and optimization techniques, more than 8 dBm output power and 9 dB gain have been achieved in the measurement. In comparison with the state-of-the-art OOK results, this transmitter has achieved much higher output power and efficiency (Table. 26). Finally, by using this Tx in a complete wireless system, more than 6 Gbps over a 4 m distance with less than 36 mW DC power consumption has been transmitted which to the author's best knowledge is the highest data-rate over a 1 m distance ever measured with a CMOS transmitter at 60 GHz.

Chapter 6 concludes this work and discusses the possible future works and prospects for this application.

2 Modeling of Passive and Active Structures

The silicon-based high f_t and f_{max} CMOS and bipolar transistors give the chip designer the opportunity to use the mm-wave band for low cost wireless applications. These applications cover a wide range, from high data-rate short-range communications to radar systems. The operational frequencies of these applications are increasing as the new technologies provide higher f_t and f_{max}. For example, the 60 GHz band has been utilized for high data-rate, short-range applications [35], and the 77 GHz for radar systems [36]. The recent developments show the feasibility of transceiver design at 160 GHz [82]. Designing at such high frequencies requires the precise modeling of all the passive and active components and devices.

The main utilized passive structures in a mm-wave circuit consist of inductors, capacitors, transmission lines, transformers, junctions and transistor cores. Having a scalable model for these passive structures would considerably ease all the design problems and lead to a much simpler design and optimization techniques. However, including all the parasitic and coupling elements in a scalable model, especially at the mm-wave frequency range, is quite difficult and in some cases, not possible (for example, coupling elements between the input and output-matching networks); hence, different modeling techniques must be utilized during the design procedure.

In this section, the two main modeling techniques - based on the EM simulation - and mathematically scalable models for passive structures are investigated. The scalable models, although difficult to extract, have many advantages during design and optimization over the EM-simulated ones, as their parameters can be changed much more readily and quicker than EM-simulated models. Therefore, it is important to develop a design procedure that can utilize both modeling techniques to minimize the design time.

Fig. 4a presents a design procedure utilizing only the EM simulation. This procedure can be implemented for a complete chip design [16] and extended up to mm-wave frequencies. The main problem with this design technique are the complications and time consumption of the EM simulation. In order to simulate the complete circuit in an EM simulator, depending on the size of the circuit, a couple of hours to a couple of days might be required. Such a time consuming process makes the redesign quite difficult. However, the redesign process could be accelerated if the EM simulation could be drawn out of the main design loop.

Fig. 4b presents the second design procedure. With this design technique, the scalable model of the critical components (like capacitors, inductors and etc.) is utilized in the design process and the EM simulator is only used for a specific area of the circuit layout (like the transistor’s core and junctions). Through this, the EM simulation time can be reduced significantly. Moreover, by utilizing intelligent layout design techniques, the on-chip coupling can be reduced and the EM extraction

loop can be omitted. All together, these make modeling an important parameter in high frequency circuit designs.

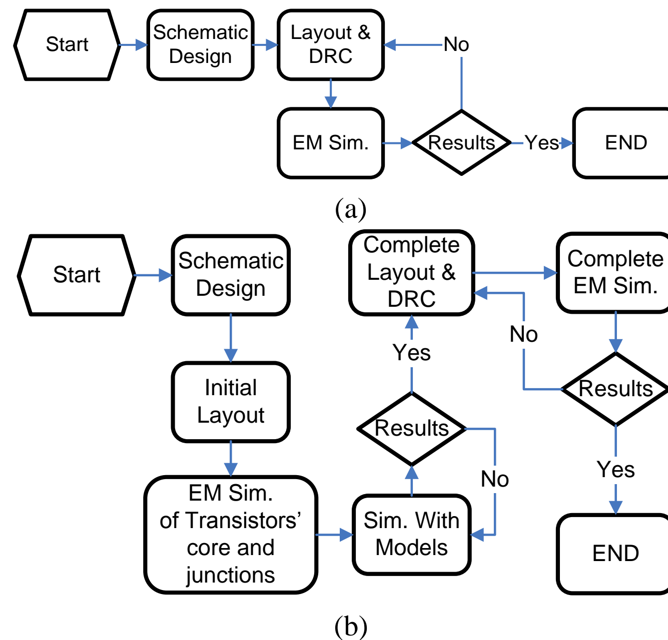


Fig. 4 Circuit design procedure (a) with EM simulation (b) with component modeling and EM simulation combined.

The accurate modeling of the passive elements would not be helpful unless the active components had an accurate model as well. Any slight inaccuracy in the transistor model can result in a large mismatch between the simulated and measured results as the frequency is increased. Finally, by cascading different circuits, these mismatches can utterly change the performance of the complete system.

Unlike the passive structures, the modeling of the active components can be quite challenging. Some active components - like varactors - can be modeled easily by using lumped components [25], while the transistor model includes frequency- and temperature-dependent small and large signal parameters. In this case, the accurate modeling of the transistors by the circuit designers is quite difficult and, hence, the foundry-provided model has to be utilized, which in turn has to be validated by comparing the simulated and measured results of the test transistors.

This chapter is divided into four sections. In the first section, the EM simulation technique for both the 0.25 µm HBT and 90 nm LP CMOS technologies is explained. In the second and third sections, the modeling of different passive and active components for the 0.25 µm HBT and 90 nm LP CMOS technologies is investigated. Finally, the fourth section concludes this chapter.

2.1 EM Simulation

Different EM simulators are commercially available (HFSS, Momentum, CST…). These simulators use different solution techniques to solve and characterize passive structures, with good accuracy up to 100 GHz and above.

In this work, HFSS has been utilized for the model extraction. Employing a 3D simulation, this simulator is appropriate for multilayer chip design up to 100 GHz. All the necessary passive structures can be drawn in the Cadence and imported into the HFSS using Tech-file mapping. All the necessary information regarding the port definition and boundaries can be found in the HFSS manual provided by Ansys Co. [45]. An example of the HFSS simulation setup is shown in Fig. 5, where a folded Wilkinson combiner has been simulated completely on the SiGe HBT substrate.

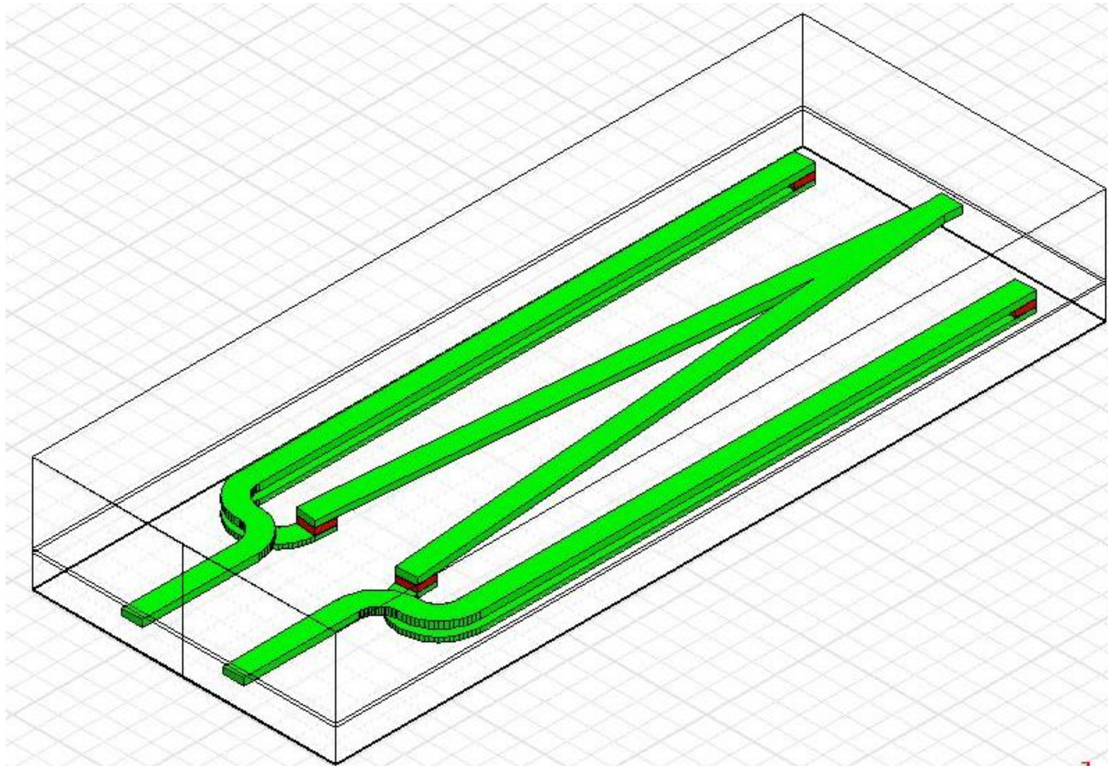


Fig. 5 An example of complete HFSS simulation.

2.2 Passive Structures Modeling for HBT Technology

Each matching network consists of parallel and series transmission lines and capacitors. In this section, the modeling of these passive structures is presented. All the models are verified by comparison with measured results up to 110 GHz.

2.2.1 Capacitors

Although in this technology the provided on-chip capacitors at the V-band show a high Q-factor, the inclusion of its parasitic elements within the design is still necessary. In this section, a complete scalable lumped component model up to 140 GHz for this capacitor has been developed. The developed model has been compared with measurements for validation [14].

The capacitor parasitic elements (Fig. 6) can be divided in two categories:

- Parasitic elements of the capacitor core
- The coupling elements to the surrounding structures

The parasitic elements of the capacitor core are the sheet resistance, the inductance of the capacitor plates and the resistance of the insulator. The coupling elements between the capacitor and the surrounding passive structures are difficult to extract. This is due to the layout variations of the neighboring structures. In this work, all these elements are extracted with the EM simulator for a square-shaped capacitor with a fixed surrounding ground plane. The technology provides five metal layers. The capacitor is formed between metals two and three with the help of an extra layer (metal C). Fig. 6 shows the capacitor and all the parasitic and coupling elements.

In order to simplify the modeling and split the above mentioned parasitic effects in the MIM capacitors, it is important to remove the ground layer below the capacitor and choose an ideal substrate. The plates and the insulator of the capacitor have different parasitic elements. The conductance of the insulator is negligible for the mm-wave band. Furthermore, by selecting square capacitors the ratio of area-to-perimeter could be minimized, which minimizes the fringe effect of the capacitor.

As mentioned before, the EM simulation has been performed to extract the parasitic elements. For this simulation, the capacitor is fed with an EM signal from one side while the other sides are open. For capacitor sizes of less than λ/10, the capacitor can be modeled with a series of resistors, inductors and capacitors. This model agrees well with the measured results up to 140 GHz for all the capacitors smaller than 4 pF for this technology.

As the value of the MIM capacitor (C_{MIM}) is less dependent on the fringing effect and frequency, in the modeling process it can be set as a constant. The values of the inductor and resistor can be formulated through curve-fitting techniques from the S-parameter results. This is presented as follows:

$$R = C_1 f^n + C_2 \; [\Omega] \tag{1}$$

$$L = C_3 e^{Z(C_{MIM}, f)} \; [\mathrm{H}] \tag{2}$$

In the above formula, C_1, C_2 and C_3 are constant values and Z is a function of the C_{MIM} and frequency (f). Also, due to the square shape of the capacitors, the series resistance of the plates does not depend on the capacitor values.

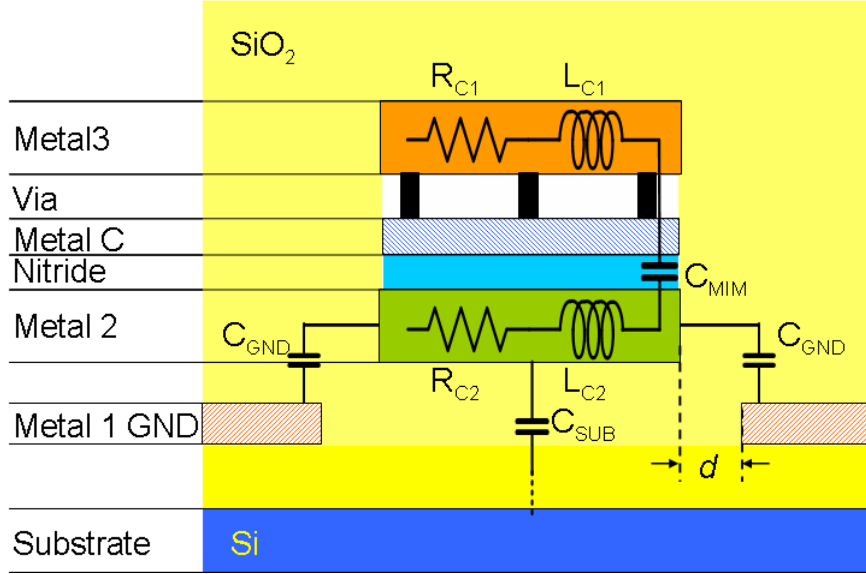


Fig. 6 Cross-section of the capacitor with main parasitic and coupling components.

The grounding of the capacitor is one of the most important parts of circuit design within the mm-wave band. The ground plate cannot be omitted as most of the structures need a DC or RF ground. However, any ground plane under or around the capacitor can increase the coupling capacitances considerably and so change the performance of the capacitor severely. Due to these problems, the ground plate must be drawn in such a way that the coupling elements are minimized while the grounding of the other passive parts is less affected.

In order to minimize the effect of the ground coupling on the capacitor performance, there must be no ground plate (Metal 1 in Fig. 6) under the capacitor. By eliminating the ground under the capacitor, the remaining coupling elements are the fringing capacitance from the edge of the capacitor to the edge of the ground plate (C_{GND}) and from the coupling capacitor to the substrate (C_{SUB}). The fringing capacitance is a function of the distance (d) between the edges of the ground and the capacitor. Fig. 7 shows the total coupling capacitance to ground and the substrate for the capacitors up to 4900 fF.

As seen from the simulated results presented in Fig. 7, the fringe capacitance is negligible when d is more than 8 µm. The total coupling capacitance ($C_{Ctot} = C_{SUB} + C_{GND}$) can be formulated as a function of d and the capacitor size (C_{MIM}):

$$C_{SUB} = K_1 + K_2 C_{MIM}\ [F] \quad (3)$$

$$C_{GND} = K_3 e^{k_4 d}\left(e^{k_5 C_{MIM}} - e^{k_0 C_{MIM}}\right)\ [\mathrm{F}] \quad (4)$$

In the above formula, K_1 to K_6 are constant values. As is evident from the presented EM simulated results, for ground metallization far from capacitor plates ($d > 8$ µm) the C_{GND} contribution to C_{tot} is much less and C_{SUB} dominates.

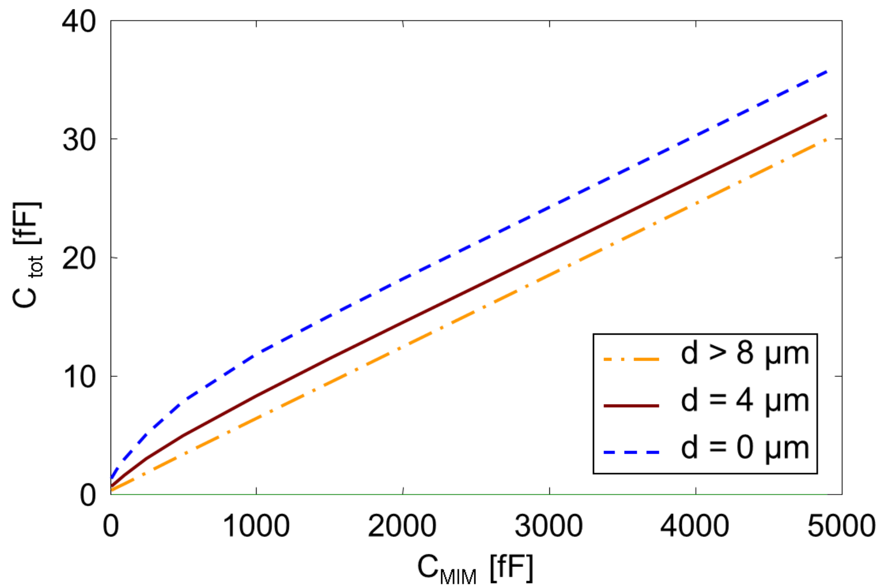


Fig. 7 Simulated total coupling capacitance (C_{tot}) as a function of *d*

The verification of the proposed model has been carried out with the help of the basic model provided by the foundry, EM simulation and measurement for various structures. In this part, the capacitor model can be validated in two different conditions. In the first case, the modeled capacitor core is compared with a very basic and an EM-simulated capacitor model to determine the discrepancy between them up to 140 GHz. In the second verification process, the developed model has been simulated together with other modeled passive structures, like transmission lines, via and pads, and compared with the measured results up to 110 GHz. Fig. 8a-c shows the schematic, the 3D view from the EM simulator and the chip micrograph of a realized MIM test structure in the ground-signal-ground (GSG) configuration.

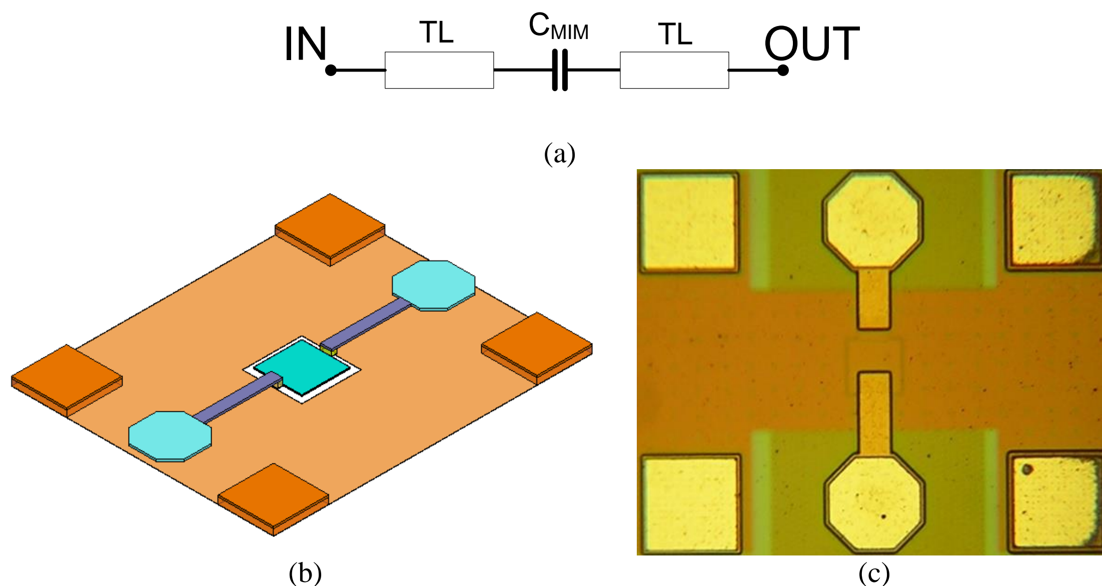
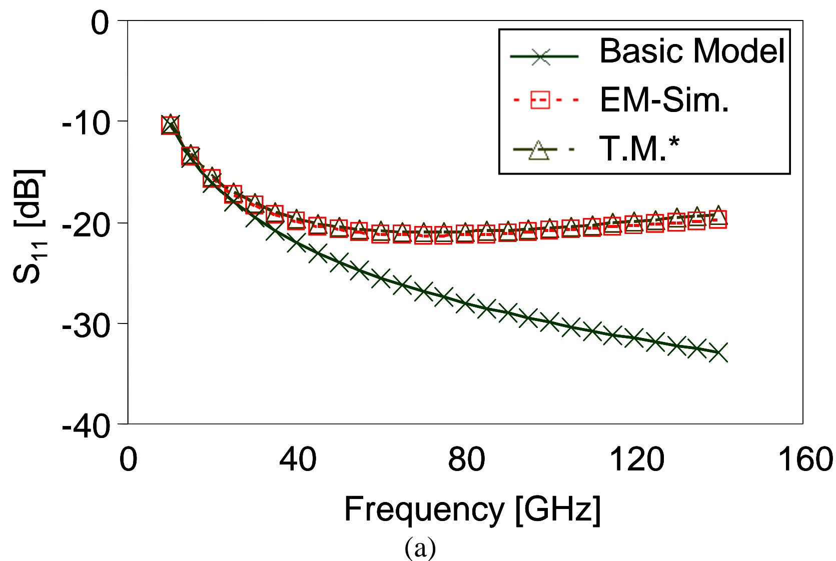


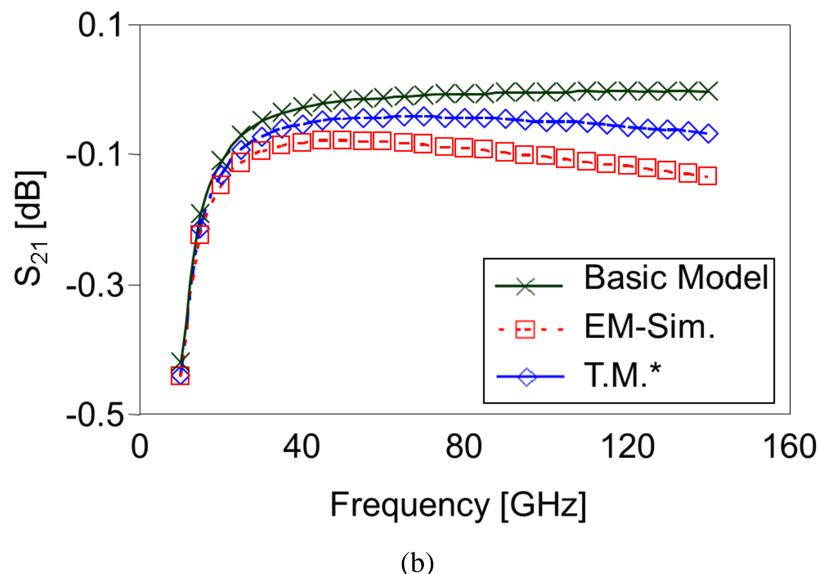
Fig. 8 Capacitor with TL, via and pad (a) Schematic of test structure (b) HFSS layout (c) Chip micrograph

In the first simulation, the modeled capacitor is compared with an EM-simulated model and the basic capacitor model provided by the foundry up to 140 GHz. Fig. 9 presents the S-parameter results for a 250 fF capacitor (with d = 4 µm). As seen, the modeled capacitor shows very good agreement with the EM simulation. From Fig. 9a, it is clear that the input reflection of the capacitor diverges from the basic model at higher frequencies and that the deviation increases with frequency.

The modeled capacitor is also compared with the measured results up to 110 GHz. The comparison results are presented in Fig. 10 for a 500 fF capacitor (22.25 µm x 22.25 µm). The S-parameter measurements have been performed on-wafer with a vector network analyzer. In order to reduce the coupling between the input, output pads and probes, the capacitor has been extended with transmission lines by 70 µm from each side (Fig. 8a). The pads, transmission lines ([44] and section 2.2.2) and vias are modeled accurately and included in the simulation. As seen from these figures the model shows good agreement with the measured results and EM simulation over the whole frequency band.

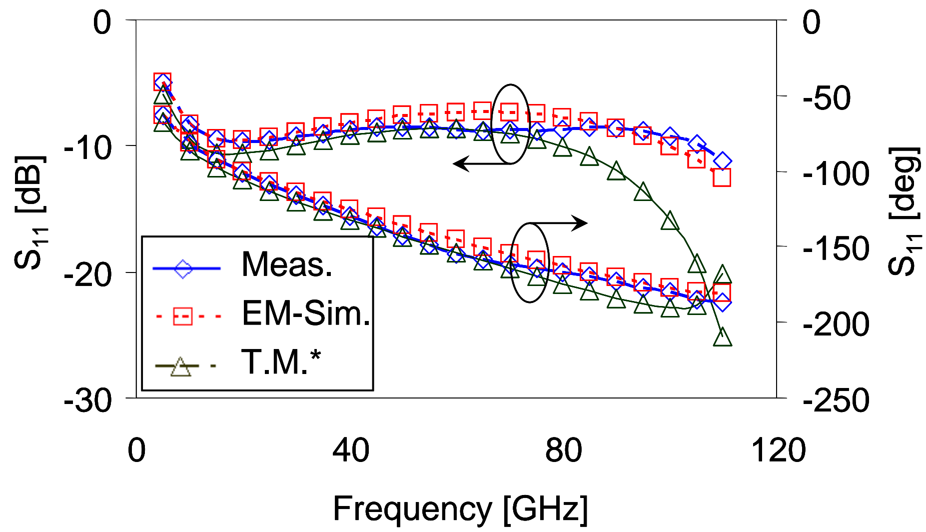


(a)

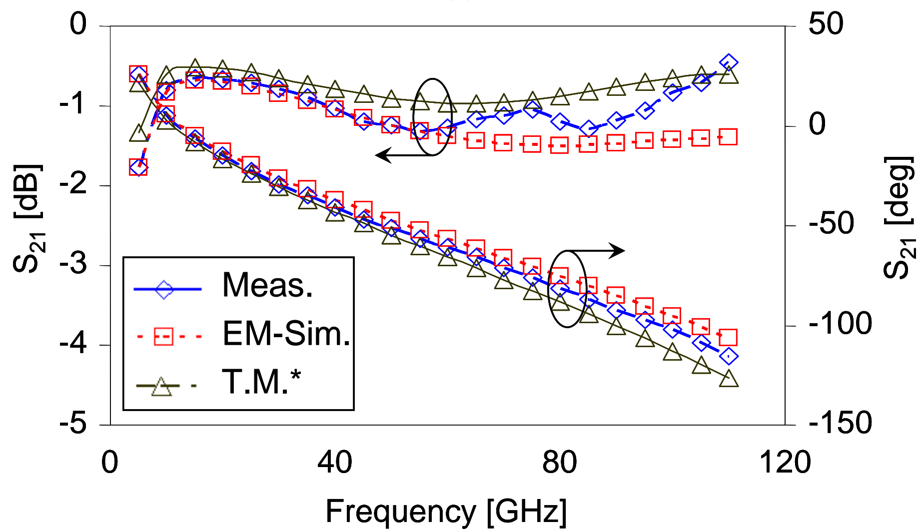


(b)

Fig. 9 The S-parameter comparison of a 250 fF (a) Input reflection(b) Transmission
* This Model



(a)



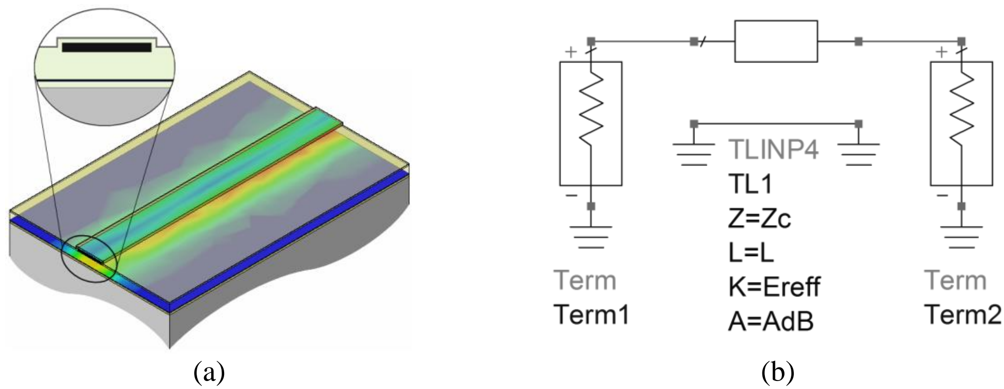
(b)

Fig. 10 The S-parameter comparison of a 500 fF: a) Input reflection b) Transmission
* This Model.

2.2.2 Transmission Line

In this work, and with the help of a systematic methodology and by extracting the propagation coefficient and characteristic impedance of the transmission lines, a scalable model for integrated microstrip lines is developed [44]. The extraction has been performed with the help of EM simulations up to 140 GHz. Finally, the extracted model has been verified by comparison with the measured results of the various transmission line sizes up to 110 GHz. The detail of this work is presented in [44]. Here, only the final results are presented.

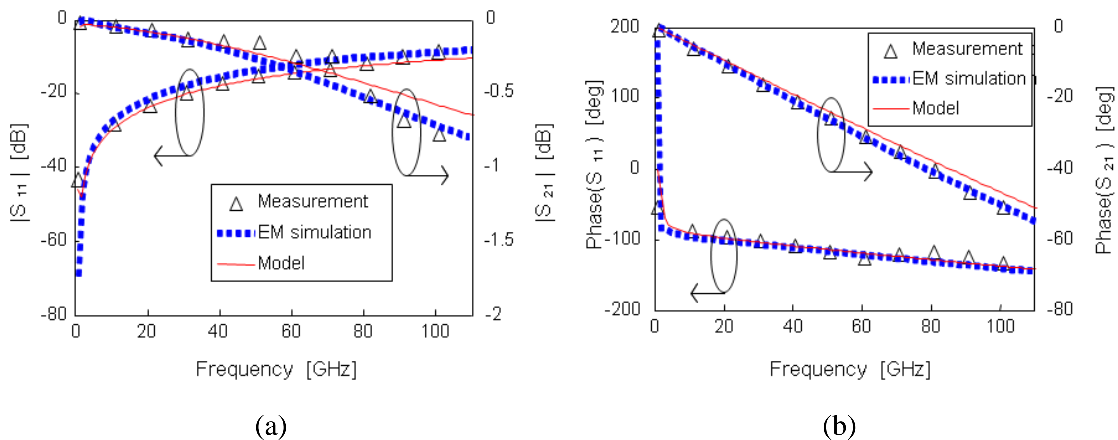
Fig. 11a presents the 3D view of EM-simulated transmission line with accurately drawn substrate and passivation layers. The extracted model has been imported into the ADS TLINP4 model (Fig. 11b) for design and optimization purposes.



(a) (b)

Fig. 11 a) Example of a microstrip line in HFSS. b) The extracted scalable model in ADS. [44]

As mentioned earlier, the model has been verified by EM simulation and measurement. Fig. 12 shows the comparison of the model, the EM-simulated and measured results of a transmission line up to 110 GHz. The good agreement of the results validates the extracted model for the transmission line.



(a) (b)

Fig. 12 Measured and simulated S-parameter results of a transmission line with *W*=30 um, *L*=200 um. a) Magnitude. b) Phase.

2.3 Passive and Active Structure Modeling for CMOS Technology

Unlike bipolar technologies, CMOS circuit performance is more sensitive to any deviations of the components models. This is mainly due to the much lower impedances and gain of the transistors in these technologies. Further, these problems can get aggravated, as much higher metal densities are required in CMOS technology in comparison with bipolar technologies for the same f_t and f_{max}. For example, the 250 nm HBT [34] has the same f_t as the 45 nm CMOS technology [33], but the much smaller metallization in the 45 nm CMOS - in comparison with 250 nm HBT - results in a much higher metal density requirement during the CMOS process. In order to satisfy the density requirements of the CMOS circuits, most of the circuit must be filled with floating metal fillers. The metal fillers can affect the RF performance of the circuit by changing the RF characteristics of the matching networks by introducing new parasitic elements and deteriorating the quality factor of the passive structures by increasing the coupling losses.

The above mentioned problems make the CMOS modeling and passive structure design more complicated than for bipolar technologies. These difficulties mainly lie in the sensitive CMOS transistor performance and unreliable passive structure model and quality factor. In order to solve these problems, two main tactics have been considered during the circuit design:

- Filler effect minimization on the RF path.
- Model extraction form measurement and comparison with EM simulation.

In this chapter, firstly, a model extraction technique from the measurements is investigated. In order to be able to extract the model of the test structures directly from the measurements, the RF feeding structure - comprising RF probing pads, pad to the transmission line transition, and short 50 Ω transmission lines both at the input and output - must be modeled first. In the first section, a technique for the extraction of such feeding structures from the measurements has been introduced [10].

Further, in the second section, to improve the matching networks quality factor and filler effect minimization, two types of transmission lines based on a coplanar structure have been studied. Based on the introduced extraction technique, different transmission line sizes are extracted from the measurements and compared with the EM simulation [7].

In the third section, on-chip transformers for mm-wave applications have been studied. A model extraction technique based on EM simulation has been investigated and verified by the measured results. Moreover, to be able to facilitate the transformer-based PA design, a scalable model has been developed [1].

Finally, in order to verify the transistor model for 60 GHz application, different transistor sizes have been realized and their models have been extracted from the measurements based on the introduced technique. The extracted model also includes the transistor core (the passive structure connecting the transistor to the matching networks), which makes this model appropriate for amplifier design since the reference points of these models and the matching networks are all on the same level (on the top-metal layer) [9].

2.3.1 RF Feeding Structure

This section presents the extraction techniques of the RF feeding structures for accurate modeling of on-chip passive and active components. The presented techniques have been applied for a group of test structures realized in a 90 nm CMOS process and validated through measurements up to 100 GHz. Feeding structures comprising RF probing pads, pad to the transmission line transition and short 50 Ω transmission lines, have been modeled with the help of measurements and EM simulations. The modeled structures have been utilized in the extraction of the test components - like MIM capacitors, transistors, etc. - from the measurements. The comparisons between the foundry-based models and the extracted results of the components show good accuracy, which further validates the applied techniques up to 100 GHz operating frequencies.

2.3.1.1 Topology

Feeding structures (i.e., pads plus interconnections) are necessary for the measurement of the on-chip circuits. In this technology, in order to facilitate the model extraction of the passive and active components from the measurements, a fixed feeding structure has been selected for the measurement of all passive and active test structures.

Fig. 13 presents the selected structure showing the probing pads in a GSG configuration. The GSG configuration is designed with 100 µm pitch and an 82 µm by 47 µm pad size to minimize the chip size of the feeding structure. The input and output ports of the test structures are placed at a distance of more than 200 µm from each other in order to minimize the high frequency coupling effects between them. Also, all the passive components are connected to the pads through a 50 Ω transmission line. Finally, the pad and the transmission line are connected with a tapered transition structure to minimize the parasitic junction capacitances.

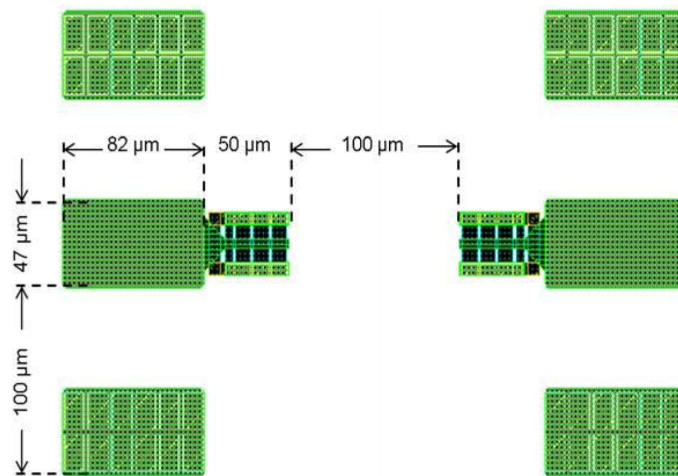


Fig. 13 Feeding structure utilized for the entire device under tests.

2.3.1.2 Extraction Techniques and Results

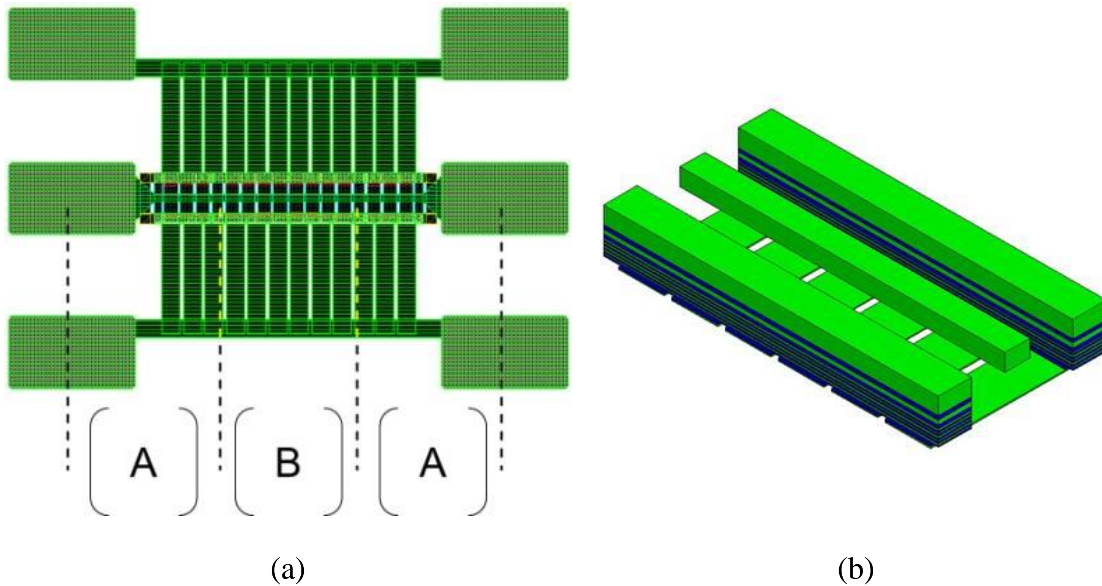
In order to extract the pad structure, a test circuit has been designed and measured (Fig. 14a). In this test circuit, the two feeding structures are simply connected with a transmission line. The ABCD matrix of the total test structure can be described as follows:

$$[T] = [A] * [B] * [A] \tag{5}$$

In this formula, [A] and [B] are the ABCD matrixes of the feeding structure and the transmission line, [T] is the ABCD matrix of the total test structure and "*" denotes the matrix multiplication. It should be noted that in the above formula the output feeding structure is in the opposite direction to the input feeding structure and, hence, its matrix is inserted as $[A]^{-1}$. However, in the extraction code, since the feeding structure is passive and both the input and output-matching are almost 50 Ω, the matrixes [A] and $[A]^{-1}$ can be, with a good estimation considered to be the same.

The model of the transmission line is extracted with HFSS simulation (Fig. 14b). In addition, the ABCD matrix of the total structure is calculated from the measured S-parameters. In this case, the only unknown in the above formula is matrix [A]. In order to extract matrix [A] from the above formula, the following equation must be solved:

$$[A] = [B]^{-1} * [A]^{-1} * [T] \tag{6}$$



(a) (b)

Fig. 14 a) Test structure utilized for the extraction of the model of the feeding structure. b) The EM simulated transmission line for matrix [B] calculation.

The above equation is solved with the help of MATLAB programming. In this solution, $[A]^{-1}$ is considered as an error function with an initial value equal to the unit matrix. An error matrix [E] is calculated each time and is used to calculate the new [A] matrix. This calculation continues until the error magnitude drops below 1%. The total algorithm for the MATLAB coding is presented in Fig. 15. This algorithm is only for a single frequency point and must be repeated for the whole frequency range.

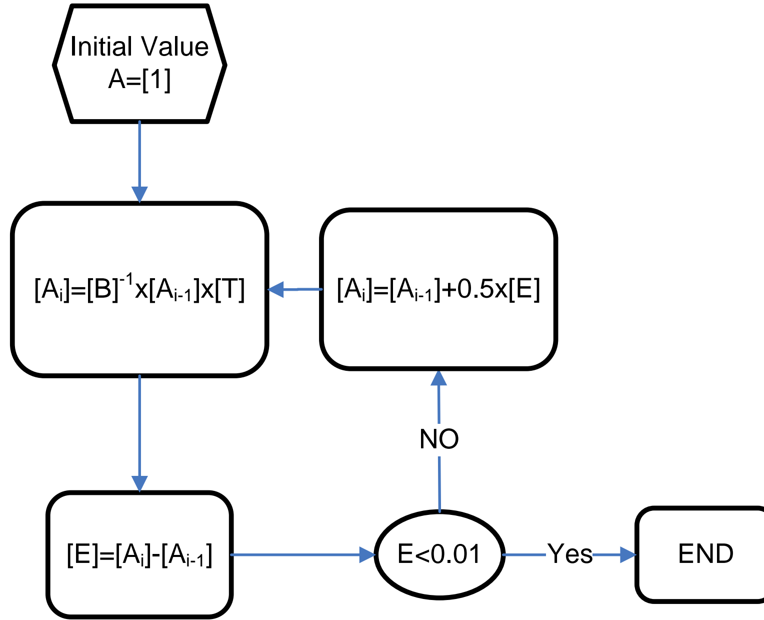


Fig. 15 Algorithm for the extraction of the feeding structure based on Matlab coding.

The extracted S-parameter model of the feeding structure is calculated from matrix A and presented in Fig. 16. As expected, the input and output reflection coefficients are lower than -20 dB (Fig. 16a). This is due to the 50 Ω transmission line and the utilized tapered connection between the transmission line and the pad.

Fig. 16b presents the insertion loss (as the reflection coefficients are negligible the S_{21} can be considered as the insertion loss) of the feeding structure. The extracted model exhibits a 0.5 dB to 0.7 dB insertion loss at the V-band.

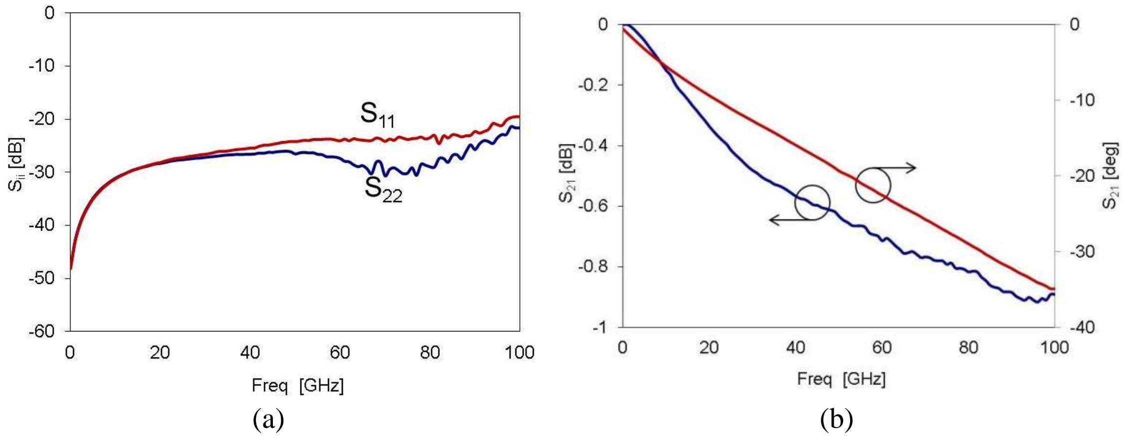
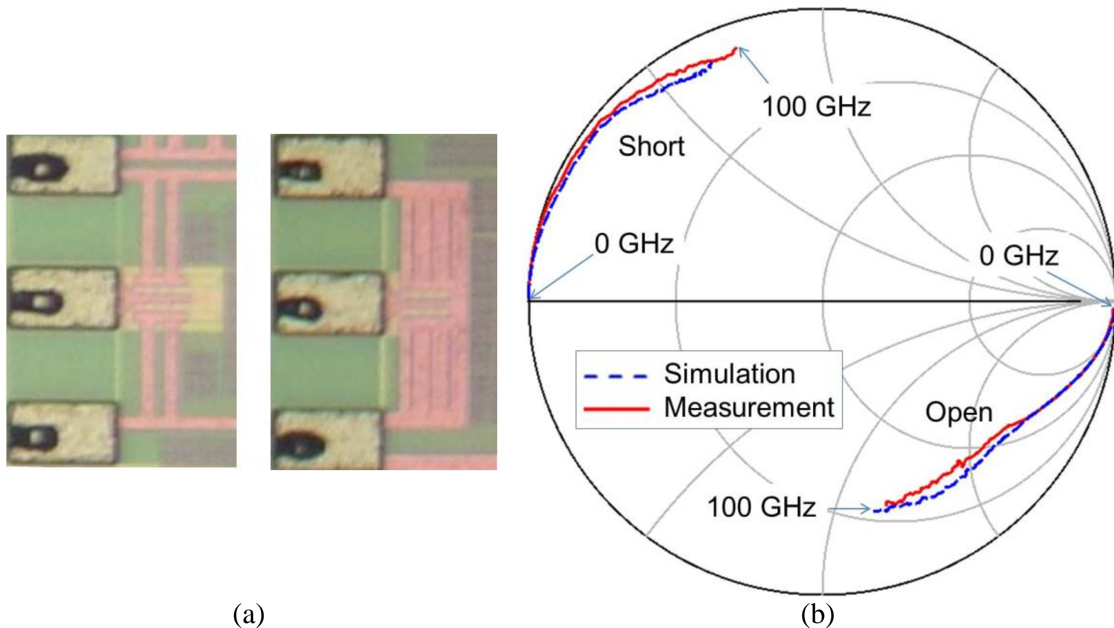


Fig. 16 The S-parameter of the extracted feeding structure:
a) Input and output return loss. b) Transmission

In order to validate the modeled feeding structure, two test circuits have been realized. Fig. 17a presents the realized open and short circuits. In Fig. 17b, the S-parameter (S_{11}) measured results and simulations are compared. The comparisons show the accurate model of the feeding structure up to 100 GHz. The simulated and measured S_{11} results slightly diverge from each other at frequencies above 70 GHz. This is mainly, as expected due to the switching in the measurement set-up from coaxial to waveguide operations at around 65 GHz.



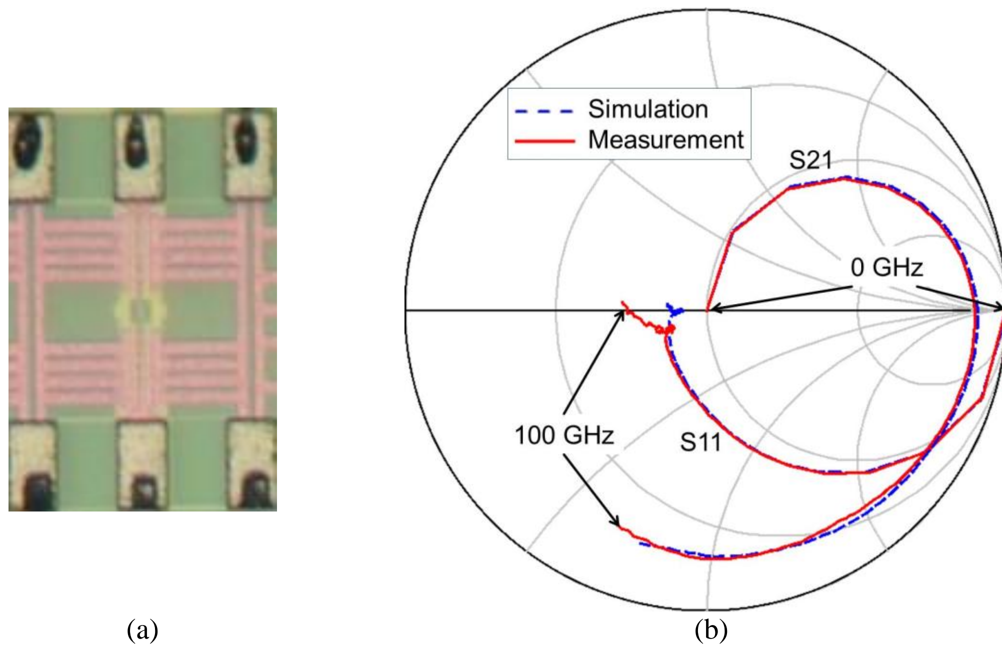
(a) (b)

Fig. 17 a) Left: Chip-micrograph of the open. Right: Chip-micrograph of the short.
b) S-parameter comparison between simulation and measurement.

2.3.1.3 Extraction Example

To design mm-wave circuits in this technology, different passive and active components (including different transmission lines, inductors, and varactors) have been realized and measured, and their models have been extracted with the help of the model of the feeding structure. In this part, a capacitor (Fig. 18a) is studied by comparing its measured and simulated results. The simulations are performed with the help of foundry-based models and the feeding structure.

Capacitors of different sizes have been realized and measured. The foundry provides an optional shielding structure for the capacitors. Due to the very low substrate resistance and the high sensitivity of the circuit performance to the parasitic elements at mm-waves, the shielding structure has been utilized to minimize the effect of the substrate on the performance of the capacitors. Fig. 18b compares the S-parameter measurement and simulation of a 470 fF capacitor with the feeding structure. A good agreement (especially in S_{21}) has been achieved up to 90 GHz. The discrepancies between the simulation and measured results increase as the frequency goes beyond 90 GHz. Part of these discrepancies might also be due to the junction capacitances between the capacitor and the transmission line which can be reduced by using wider transmission lines, a tapered connection between capacitor and transmission lines, or else smaller capacitor sizes.



(a) (b)

Fig. 18 a) Chip-micrograph of a 470 fF capacitor. b) The S-parameter comparison between simulation and measurement.

2.3.2 Transmission Lines

This work investigates the design of two different coplanar transmission lines (TL) and their application at millimeter wave frequencies up to 100 GHz. The coplanar structure has been selected to improve the grounding and to remove the effect of the fillers on the transmission lines. The two transmission lines differ by their bottom metal layer patterns. In the first transmission line, the bottom metal is solid ground while in the second transmission line the bottom metal layer is simply used as a shield. The transmission lines are optimized for different parameters, such as insertion loss, inductance per unit length and size. In addition, to justify the simulated electromagnetic models of the transmission lines, different transmission lines have been realized and measured. The characteristics of the transmission lines are extracted from the measured results. The comparison of the model's simulated results and the measured results shows good agreement up to 100 GHz. Finally, two 60 GHz amplifiers in the 90 nm CMOS technology were designed based on these transmission lines so as to further verify their functionality for 60 GHz circuit design.

2.3.2.1 Designed Transmission Lines

Two coplanar TLs with different bottom ground patterns are designed. The 3D views of the designed TLs are presented in Fig. 19. In the first design (Grounded Coplanar Transmission Line - GCTL), the bottom metal layer is selected to be as wide as possible (Fig. 19a-b). The ground width (W_1) is limited by the manufacturing density rules. A wide bottom grounded metal minimizes the coupling to the substrate and also requires less TL width (W) for 50 Ω and lower impedances. Although this kind of transmission line is quite compact, it suffers from both eddy current loss and a low self-resonant frequency due to higher capacitance to ground, and it also faces many difficulties in the design of higher ohmic TLs (> 50 Ω). To compensate such losses and the low self-resonant frequency, and to increase the TL impedance, a shielded structure has been used in the second TL (Shielded Coplanar Transmission

Line - SCTL) instead of the ground plane (Fig. 19c-d). This kind of structure results in higher impedance and lower eddy current losses, but to have the desired impedance a much wider TL is required. Fig. 20 and Fig. 21 present the simulated results of both TLs versus the width and the spacing values. The spacing value in the GCTL is selected to be smaller than the SCTL. In the GCTL, this would help in gaining 50 Ω impedance for smaller TL widths. However, in the SCTL having a higher spacing would help in increasing the inductance value per unit length for the transmission line. As result, the spacing values are selected at around 7.5 µm for the GCTL and 9 µm for the SCTL. In the SCTL, increasing the spacing value would increase the impedance and, consequently, the inductance value, but it is limited by the density requirement of the foundry.

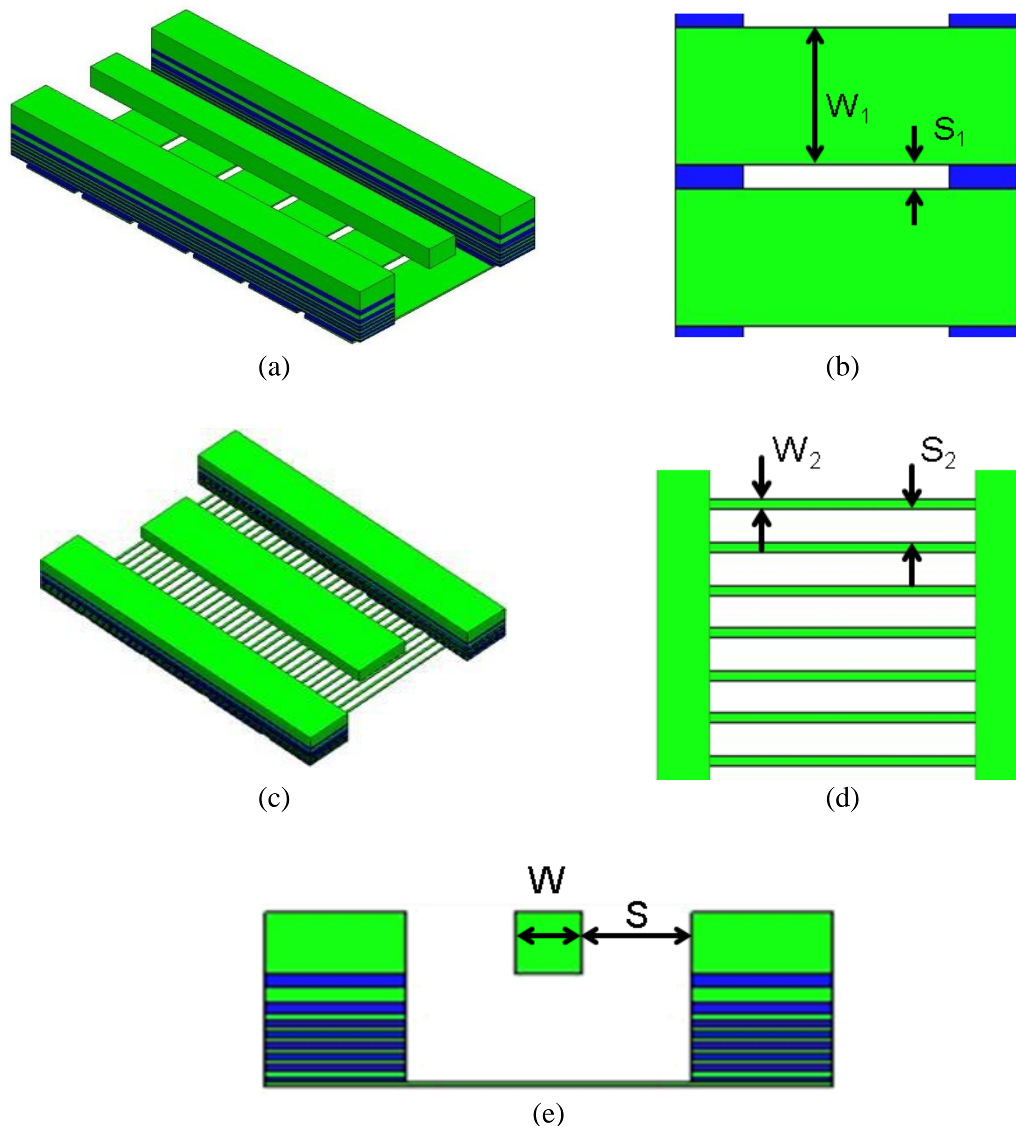


Fig. 19 a) GCTL. b) GCTL bottom view. c) SCTL. d) SCTL bottom view. e) Both TLs front view.

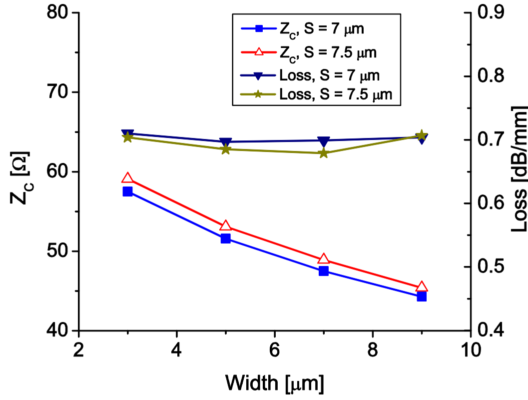


Fig. 20 Impedance and insertion loss of the GCTL for various widths and spacing.

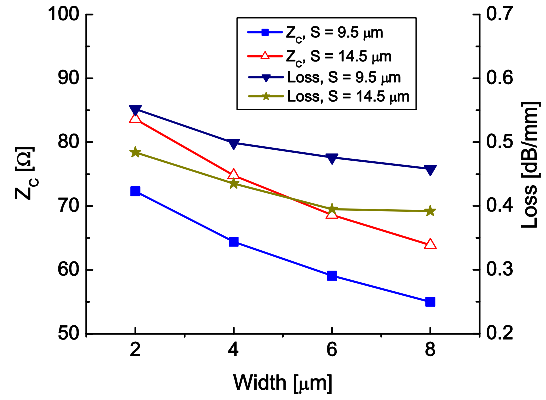


Fig. 21 Impedance and insertion loss of the SCTL for various widths and spacing.

In order to verify the introduced TLs, two different GCTLs (lengths equal to 100 µm and 600 µm) and one SCTL (length equals to 100 µm) have been manufactured and measured. The measurements are performed completely on the chip with GSG probes and a network analyzer from 100 MHz up to 100 GHz. The general shape of the test structure is presented in Fig. 22. As mentioned in the RF feeding structure section (Section 2.3.1), in order to extract the TLs performance all the pad structures are modeled. By using the following equation, the ABCD matrix of the TL can be extracted from the total test structure:

$$[ABCD]_{TL} = [ABCD]_{Pad}^{-1} \times [ABCD]_{ALL} \times [DBCA]_{Pad}^{-1} \quad (7)$$

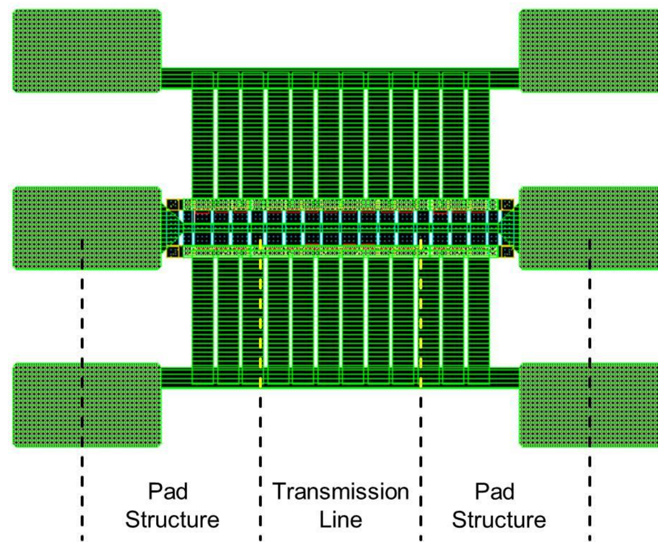


Fig. 22 Test structure view including the transmission line and the pas structures.

Fig. 23 presents the comparison between the S-parameter measured results and the simulated results of the 100 µm GCTL. The pad structure has been subtracted from the measurements, as explained above. Due to the good calibration during the measurements and the accurate EM simulation of the transmission line, a good agreement between simulated and measured results has been achieved. The measured results show around a 0.8 dB/mm insertion loss.

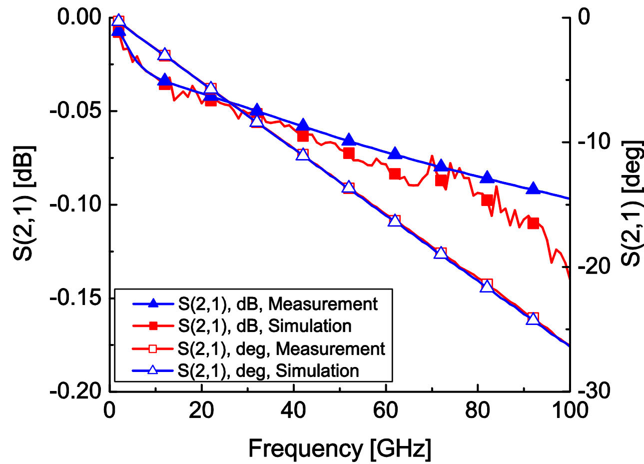


Fig. 23 Comparison between the simulated and measured results of 100 μm GCTL with 5 μm width and 7.5 μm spacing.

Fig. 24 and Fig. 25 present the comparison between the simulated and measured characteristics of both transmission lines. In the GCTL, the simulated results of both the impedance and inductance of the 100 μm GCTL are compared with the measured results. The comparison shows good agreement up to 60 GHz. The simulation and measured results diverge slightly from each other at frequencies above 60 GHz. This might be mainly due to the calibration as well as to the slight differences in the substrate characteristics at higher frequencies between simulation and measurement.

In the SCTL, only the inductance value could be compared with the simulation. Due to certain calibration problems at frequencies above 65 GHz, the impedance value cannot be extracted accurately.

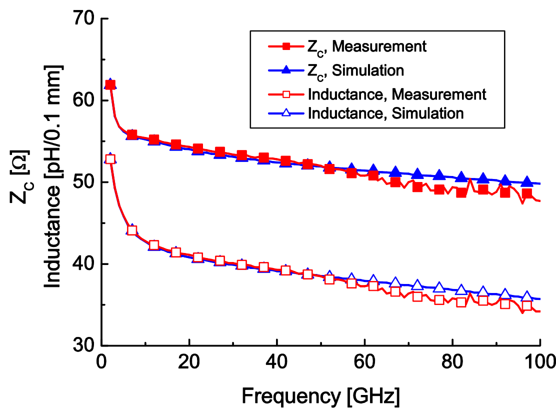


Fig. 24 Comparison between the simulated and measured results of 100 μm GCTL with 5 μm width and 7.5 μm spacing.

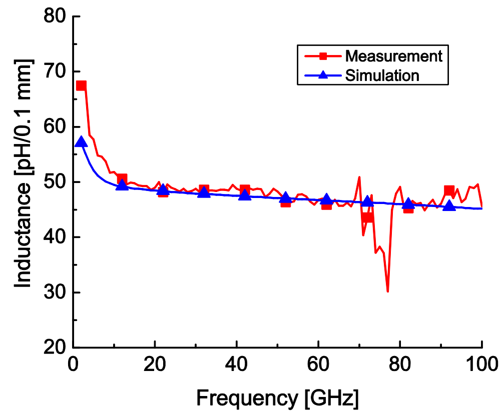


Fig. 25 Comparison between the simulated and measured results of 100 μm SCTL with 8 μm width and 9.5 μm spacing.

2.3.2.2 Test Circuits Implementation

In order to justify the transmission line model and its functionality in circuit design, two different amplifiers have been realized and measured (Fig. 26 and Fig. 27). The matching network of the first amplifier has been designed with the help of the GCTL while the second amplifier utilizes the SCTL.

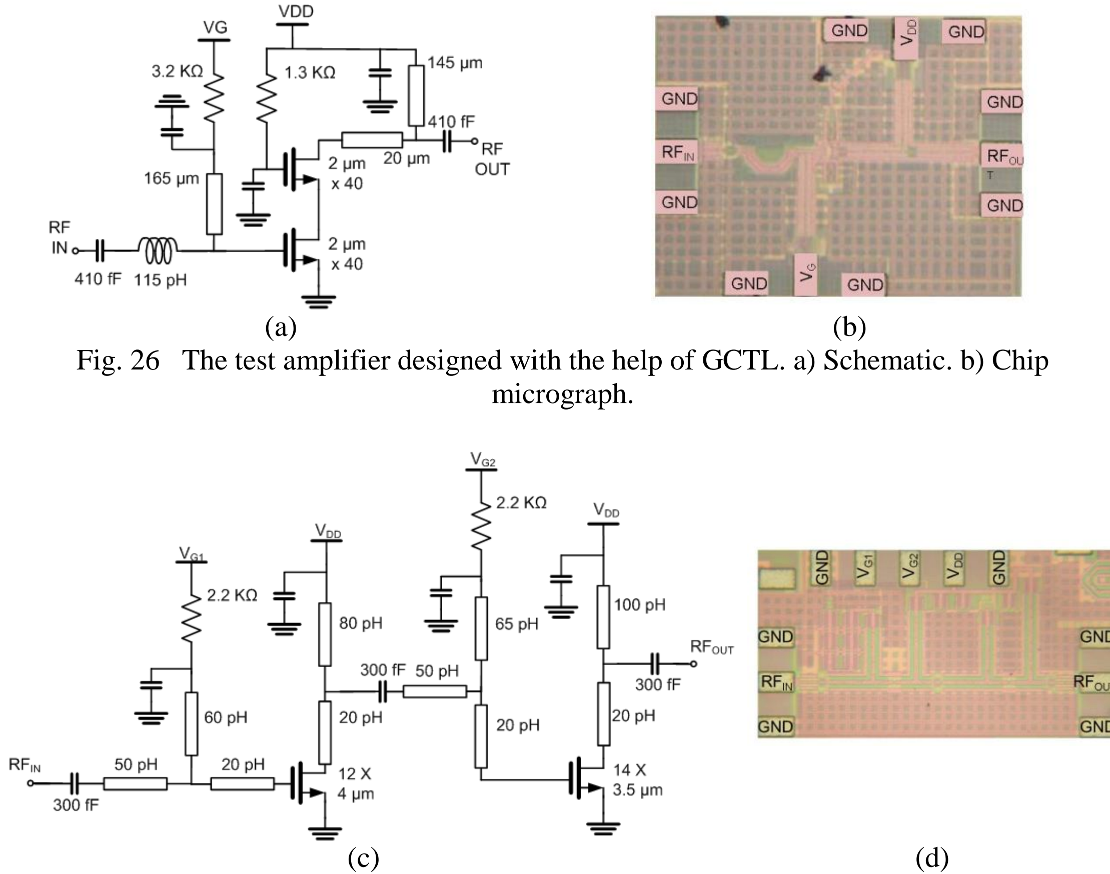


Fig. 26 The test amplifier designed with the help of GCTL. a) Schematic. b) Chip micrograph.

Fig. 27 The test amplifier designed with the help of SCTL. a) Schematic. b) Chip micrograph.

The first amplifier has been designed with a cascode topology. The one-stage cascode topology provides good output-to-input isolation and, therefore, good stability. Although the cascode topology in the CMOS technology shows less output power than common source (C.S.) topology [8], it is widely used in the low noise amplifier design [75]. As a high inductance value is needed for the input-matching, an inductor has been used instead of a long transmission line in order to minimize the chip size.

Unlike the first amplifier, in the second amplifier a C.S. topology has been utilized. The C.S. topology provides a much better output power in comparison with the cascode [8], making this topology more interesting for power amplifier design; however, its lower isolation between output and input ports, in comparison with the cascode topology, can cause instability.

The measurements have been performed under 1 V gate voltages and 1.2 V drain voltages for both amplifiers. Fig. 28 and Fig. 29 show the good agreement between the simulated and measured results for both amplifiers up to 100 GHz. The first amplifier shows around 5 dB gain while the second amplifier shows more than

10 dB gain around 60 GHz. On the other hand, and as expected, the one-stage cascode amplifier provides better isolation (S_{12}) than the two-stage C.S.

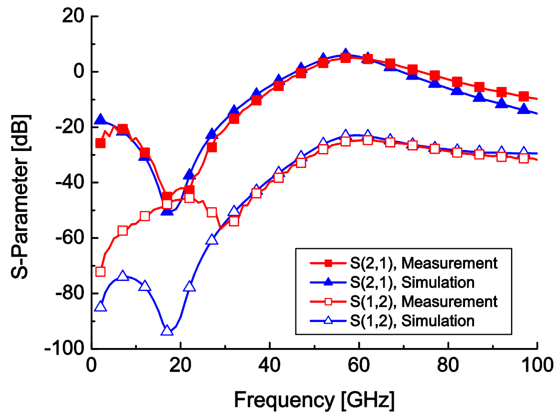


Fig. 28 Comparison between the simulated and measured results of the Cascode amplifier.

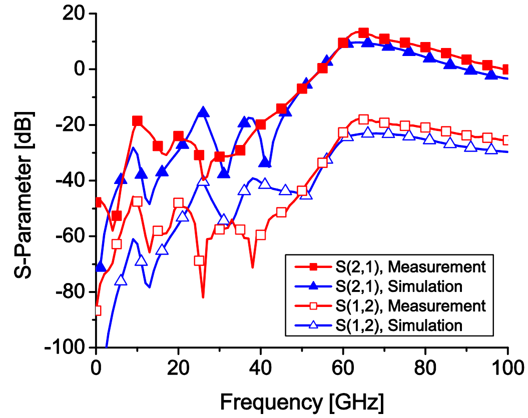


Fig. 29 Comparison between the simulated and measured results of the common source amplifier.

2.3.3 Transformer Design

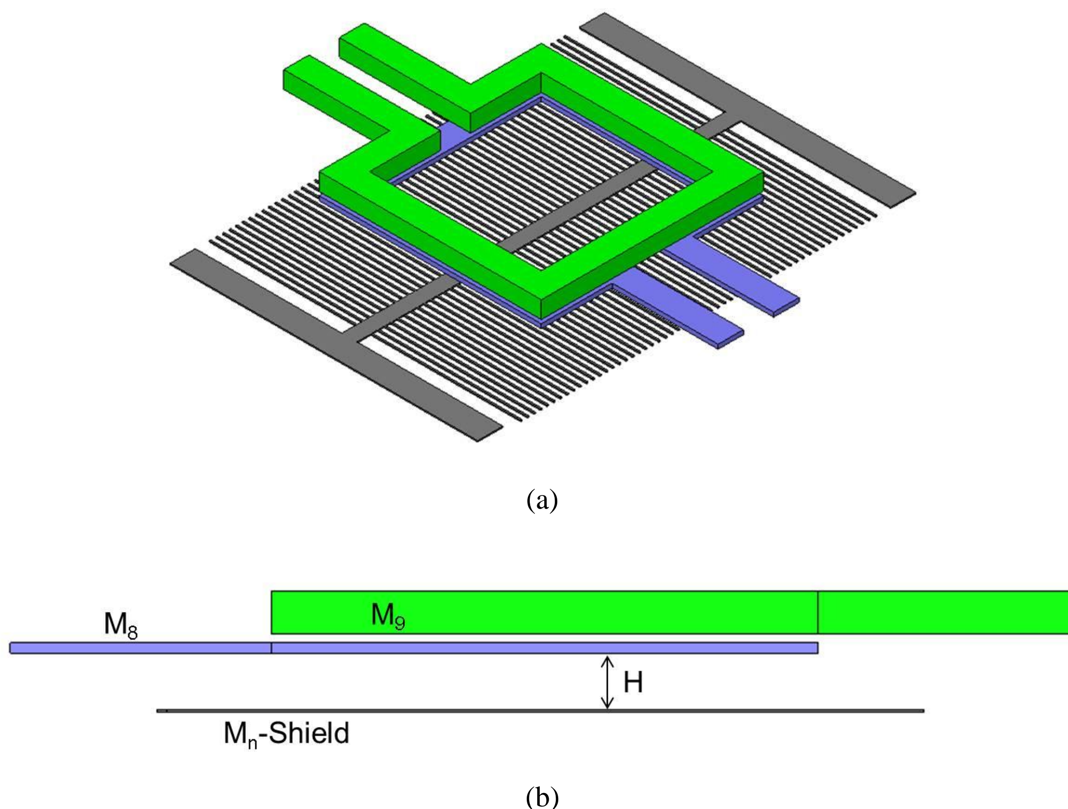
In recent years, developments in transformer-based CMOS PA design have demonstrated the capability of chip size minimizations without noticeable P_{OUT} degradation [77]. To ease the use of transformers in mm-wave circuit design, scalable models for transformers have been developed by different circuit designers [76]-[77]. The model presented in [76], although for complex transformer structures, shows less accuracy for higher frequencies. To increase the accuracy up to the mm-wave, a transmission line-based model is proposed in [77]. Although this model shows a good tendency with the measurement results, due to higher filler density requirements in these technologies, determining even and odd impedances and the propagation constant is quite challenging.

In this work, different types of transformers have been investigated. Depending upon the balanced or unbalanced state, number of turns and shielding position, different transformers for different purposes (mainly including the up-converter and the 60 GHz PA design) have been characterized. In the first step, different transformers have been realized and, by extracting from the measured results, their performances have been compared with the EM-simulated results. Although EM simulation shows excellent agreement with the measured results, this technique can be time consuming in relation to the design process (Fig. 4). Every time that the width or the length of the transformer has to be changed, the new transformer must be simulated again with an EM simulator. This process can become even more complicated, as the complex nature of the transformer does not allow the designer to guess either the correct initial value or the required size change.

Further, in order to ease the design procedure by decreasing the number of iterations of the EM simulation, a scalable model for the transformer has been developed. The developed model is based on a lumped component and includes all the parasitic and coupling elements, which make it appropriate for mm-wave application. Moreover, to be able to use this model in optimization techniques, a mathematical formula for the equivalent model of the transformer has been developed.

The 3D structure of the transformer is presented in Fig. 30a. The shielding structure has been selected in parallel with the transformer terminals to minimize signal coupling to the shielding ground plane. In almost all the designs, the transformers are realized on the two thick uppermost metal layers (and on the three uppermost metals for more winding turns) to minimize the conductor losses and to maintain the maximum distance from the low ohmic substrate. On the other hand, the shielding structure has been realized in different layers. Placing the shielding structure on the lowermost layer would result in minimum parasitic capacitance to ground at the expense of the filler effects of all the other layers on the transformer performance. By decreasing H (Fig. 30b), the filler from lower metal layers would be shielded but the parasitic capacitance would increase.

In this section, first the EM-simulated and measured results of different transformers are compared to validate the EM modeling technique. Further, to ease the design of transformer-based mm-wave circuits, a lumped component-based scalable model for this transformer is introduced. The modeling has been performed for the shielding on the lowermost metal layer. By using the developed model, a mathematical formula based on the transformer width and the length of the winding and input impedance has been derived. Finally, the simulated results of the derived model are compared with the measured results for validation.



(a)

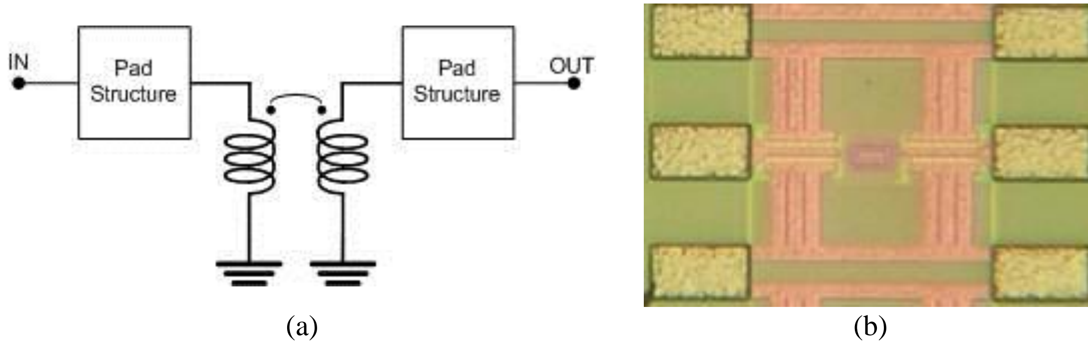
(b)

Fig. 30 Investigated transformers. a) 3D view. b) Side view.

2.3.3.1 Transformer Modeling with EM Simulation

For a successful development of the transformer scalable model, the measured results of different transformer sizes are required. The realization of different transformer sizes is not a particularly cost-effective procedure. To decrease the number of required transformer samples, the EM simulation has been utilized. By inserting the exact details of the technology substrate and boundary requirements, the extraction of the exact transformer model with the help of EM simulation has been attempted. Further, to justify the accuracy of the model different transformers have been realized and their extracted measured results have been compared with those of the simulation.

Fig. 31a shows the general schematic of the realized transformers. Due to measurement difficulties associated with differential structures, all the realized transformers have been connected as single-to-single baluns. The chip micrograph of a realized transformer with the pad structures is presented in Fig. 31b. The results of the realized transformers have been extracted from the measurements based on the technique introduced in previous section (Section 2.3.1) and in [10].



(a) (b)

Fig. 31 Realized transformer. a) Schematic. b) Chip micrograph.

To justify the accuracy of the EM simulation for different transformer architectures, three different transformers have been realized (Fig. 32). The transformers differ in the number of turns, winding and the shielding layers.

The first transformer is designed on M9 and M7 with the shielding on M6. The total length of the transformer is around 400 µm with a 4 µm metal width. To minimize the total length of the transformer, a multi-turn structure has been selected. This transformer has been designed for the LO-path in a test up-converter mixer to convert the single input into two balanced signals. As in this test up-converter, the LO power has been fed externally so that the losses of the transformer could be neglected, which allows us to have the transformer winding metals further apart from each other on M7 and M9. Unlike the losses, the signal balance is quite important for the up-converter's performance. In this case, by placing a symmetrical shielding structure directly below the transformer, the filler effect on the RF path has been minimized and, hence, any effect on the LO signal balance has been avoided.

In the second transformer, the winding metals are located on the M8 and M9 layers with a one turn architecture. In this design, and like the first design, the shielding is located as near as possible to the transformer lower winding metal (M7) to avoid any filler effects on the RF signal. This transformer has a total length of 300 µm and a width of 8 µm for both winding metals

The third studied transformer has also been designed on M8 and M9 with one turn winding and a length of 200 µm and a width of 4 µm. Unlike the two other

transformers, in this design the shielding is located on the lowermost metal layer (M1), to minimize the common mode capacitance to ground. Minimizing the common mode capacitance results in the higher self-resonant frequency of the transformer, which makes this type of metal shielding quite desirable for the PA design.

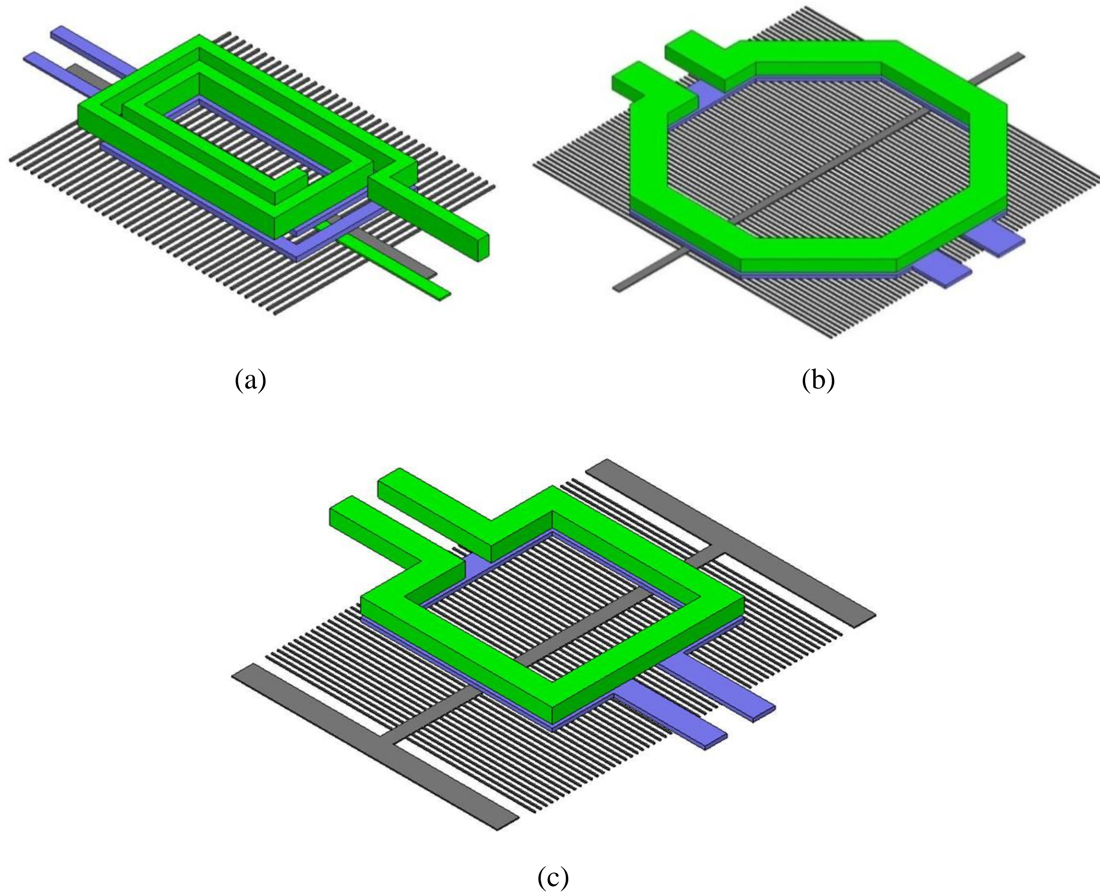
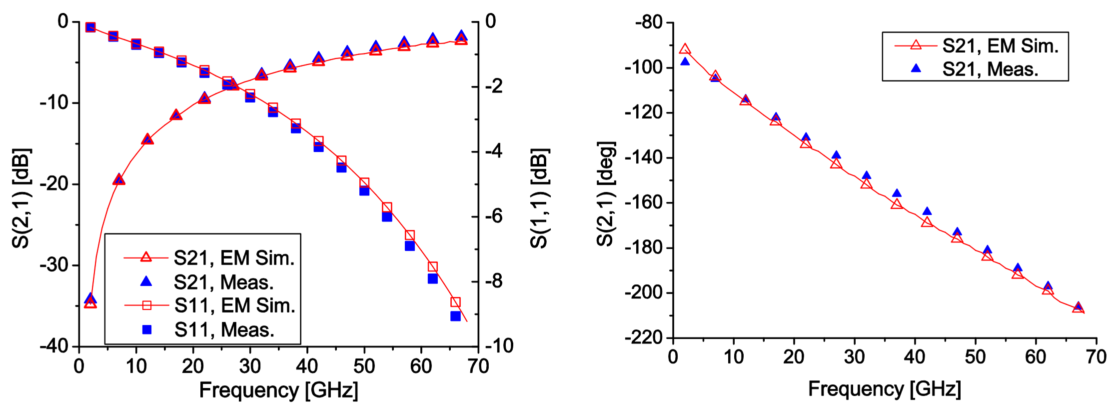


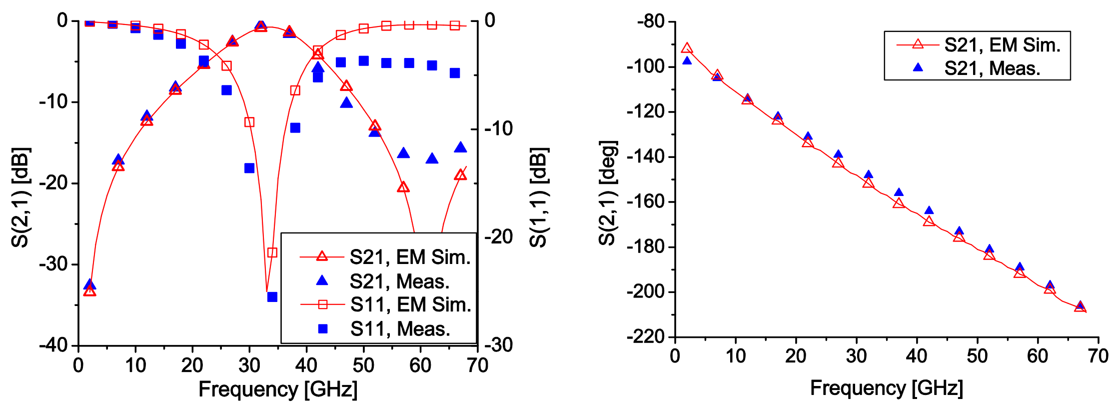
Fig. 32 3D view of the realized transformers. a) Two turns on M9 and M7 with shielding on M6. b) One turn on M9 and M8 with shielding on M7. c) One turn on M9 and M8 with shielding on M1.

The measured versus EM-simulated results of the realized transformers up to 67 GHz are presented in Fig. 33. The good agreement between the EM-simulated and measured results (especially in the first and third transformers) validates the EM simulation modeling technique and setup. Moreover, this accuracy validates the extraction technique introduced in the previous section (Section 2.3.1) and in [10].

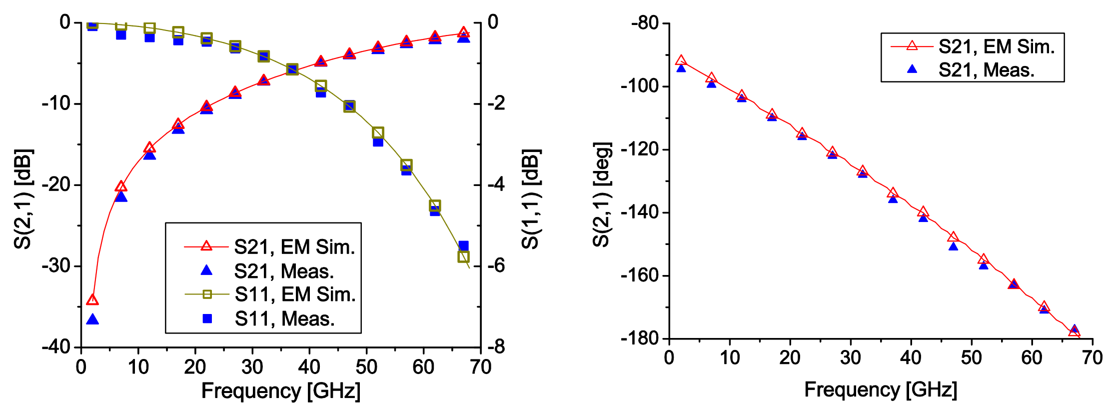
The deviation of the measured and simulated results at higher frequencies in the second transformer is due to the low self-resonant frequency of this transformer. This is mainly due to the minimum distance between the lower transformer winding and the shielding structure, and the long and wide size of windings, which resulted in higher common mode capacitance to ground.



(a)



(b)



(c)

Fig. 33 Measurement vs. EM simulation. S-parameter of: a) the first, b) the second and c) the third transformer.

2.3.3.2 Scalable Transformer Model

As the transformer modeling is targeted for the PA design, the third transformer (Fig. 32c) type introduced in the previous section has been selected. As explained earlier, due to the maximum distance between the winding and the shielding layers, common mode capacitance is minimized and, hence, this transformer has the highest self-resonant frequency in comparison with the other types.

To facilitate modeling, the transformer is divided into three parts (Fig. 34a), which include two coupled lines (coupled lines A and B) and the inductive (high impedance) lines (L_S) to the terminals. By separately modeling each part, the complete transformer model can be developed (Fig. 34b).

As the couple lines A and B are completely symmetrical, the same model can be utilized for both of them. In this model, the parasitic junction capacitances have been neglected and the model has been developed for straight coupled lines (Fig. 35a). The detailed model of this structure is presented in Fig. 36, where C_o and C_e are odd and even mode capacitances, R_s is the metallic resistance of the windings and L_p and L_{leak} are the winding and leakage inductances. Furthermore, as the substrate is shielded its parasitic elements are neglected.

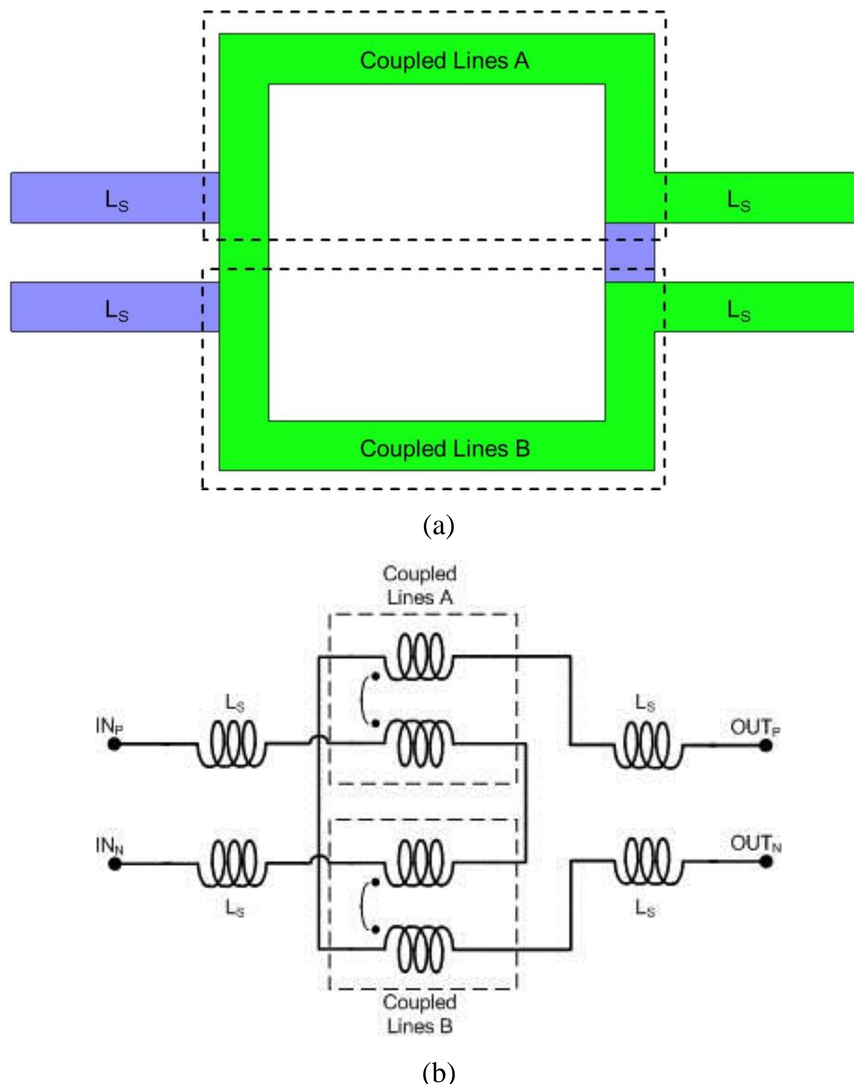


Fig. 34 Trans_M1. a) Cross section. b) Model.

Based on the dimensional parameter introduced in Fig. 35a (d, t, w and l) and the frequency (freq), all the model parameters and components, including coupling factor (K), inductance per µm (L_{pum}), L_P, L_{leak}, C_o, C_e and R_S, have been parameterized. The detailed model of the coupled line is presented in Fig. 36.

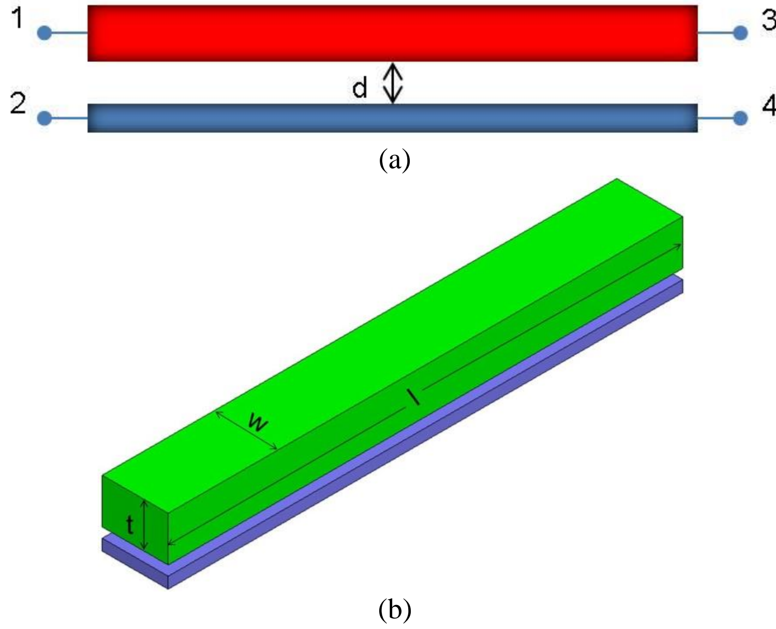


Fig. 35 Coupled lines. a) Cross section. b) 3D view.

Except for K and L_{pum}, the other parameters can be directly calculated from the physical dimensions of the transformer. To extract the constant and coefficient values, various optimization algorithms (e.g., genetic and radiant) have been utilized:

$$K = 0.71 + \frac{w - 5\mu m}{100\mu m} + 5 \times \frac{2 \times l - 140\mu m}{16mm} \quad (8)$$

$$L_{pum} = 0.35 + \frac{10\mu m - w}{50\mu m} + \frac{2 \times l - 140\mu m}{16mm} \quad [\frac{pH}{\mu m}] \quad (9)$$

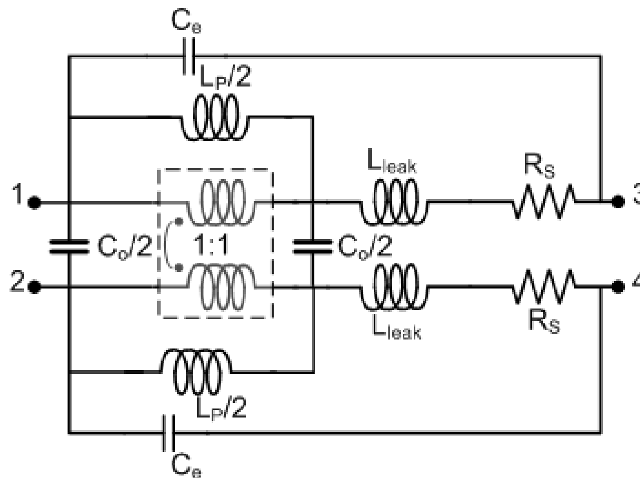


Fig. 36 Coupled lines model.

In the above equations, l and w are in millimeters. In the EM simulation, it has been observed that K is a strong function of the spacing between the two windings (d). By increasing d, K drops rapidly, which makes the power coupling less efficient and, hence, less desirable for the PA design. K in (8) has been calculated for the two upper thick metal layers of the technology (M8 and UTM).

With the help of K, L_{pum} and the physical dimensions of the transformer, L_p, L_{leak} and C_o can be calculated:

$$L_P = K \times L_{pum} \times l \quad [pH] \tag{10}$$

$$C_o = \varepsilon_0 \times \varepsilon_r \times \frac{(w+t) \times l}{d} \quad [fF] \tag{11}$$

$$L_{leak} = L_p \times \left(\frac{1-K}{2 \times K}\right) \quad [pH] \tag{12}$$

In (11), C_o is calculated as a lumped component while the dimensions of the transformer is in the same order of magnitude as λ/10. In order to minimize this effect on the accuracy of the transformer model, C_o is distributed between the input and output ports (Fig. 36).

R_s and C_e relations with the physical structure of the transformer are quite complex. In the same way as K and L_{pum} calculation, optimization techniques have been utilized to extract the constants and coefficient values:

$$R_S = 2 \times \left(1 - e^{-\frac{freq}{100G}}\right) \ [\Omega] \tag{13}$$

$$C_e = \frac{C_o}{20} \quad [fF] \tag{14}$$

In (13), frequency (freq) is in GHz. The value of L_S depends upon the length of the connecting line at the terminal of the transformer. In this design, all the connecting lines are around 20 µm, which results in:

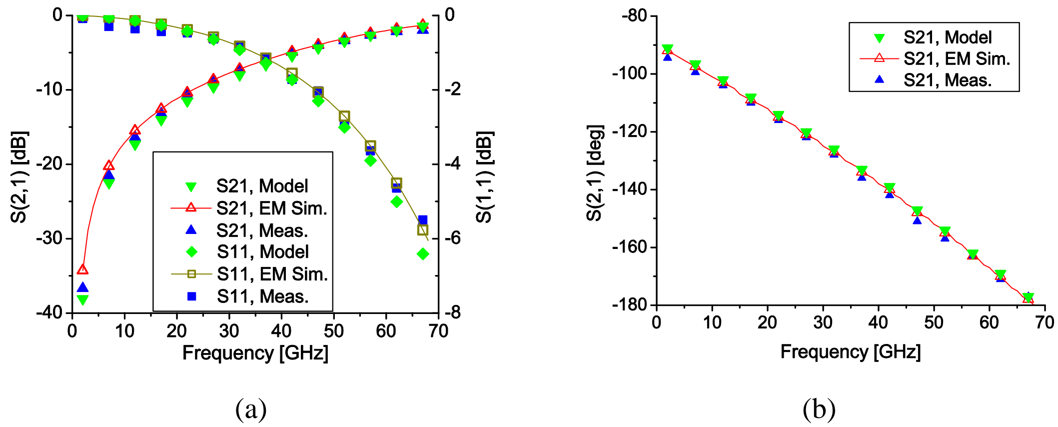
$$L_S = 7\ pH$$

By simplifying the total transformer model, a mathematical formula can be derived, where Z_i and Z_o are the terminal impedances of the transformer:

$$S = j\omega$$

$$Z_o = L_sS + \frac{2\left[\frac{\left(\frac{2(\frac{Z_i}{2}+L_sS)}{2+(\frac{Z_i}{2}+L_sS)(4C_o+C_e)} + L_{leak}S + R_s\right)L_pS}{\frac{2(\frac{Z_i}{2}+L_sS)}{2+(\frac{Z_i}{2}+L_sS)(4C_o+C_e)} + L_{leak}S + R_s + L_p\,S} + \frac{L_{leak}S+R_s}{1+2C_eS(L_{leak}S+R_s)}\right]}{2+\left[\frac{\left(\frac{2(\frac{Z_i}{2}+L_sS)}{2+(\frac{Z_i}{2}+L_sS)(4C_o+C_e)} + L_{leak}S + R_s\right)L_pS}{\frac{2(\frac{Z_i}{2}+L_sS)}{2+(\frac{Z_i}{2}+L_sS)(4C_o+C_e)} + L_{leak}S + R_s + L_p\,S} + \frac{L_{leak}S+R_s}{1+2C_eS(L_{leak}S+R_s)}\right]C_oS} \tag{15}$$

This model has been verified using HFSS simulation for various transformer sizes. Further, the model has been verified for the third transformer introduced in Fig. 32c up to 67 GHz. The comparison of the results (Fig. 37) shows the accuracy of the model.



(a) (b)

Fig. 37 Comparison between model, EM simulated and measured results of the transformer

2.3.3.3 Center Tap

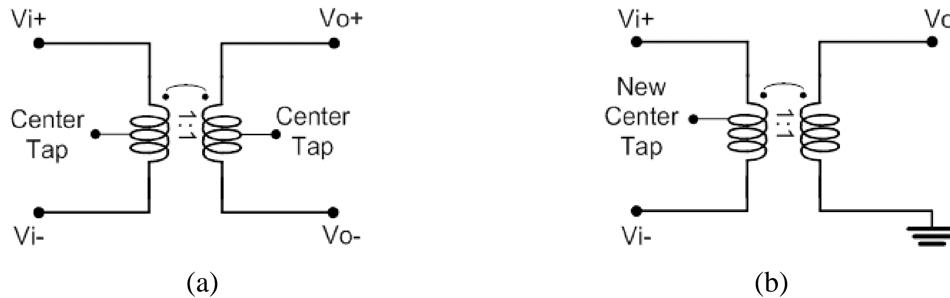
In the active circuit design, the center tap of the transformers plays an important role in the DC feeding. In an ideal balanced transformer, the center taps of the primary and secondary windings are located exactly in the middle. However, in the unbalanced transformer design, the center tap can affect the transformer performance. In the case of one unbalanced terminal, the center tap of the balanced side would be shifted away from the middle of the winding (Fig. 38).

By shifting the center tap to the new point, the middle point of the transformer winding is no longer an RF ground. Because of this problem, the parasitic elements of the DC feeding network at the center tap point must be considered in the simulations. To include this structure in the simulation, the DC feeding network has been modeled.

Fig. 39 shows a transformer designed in 90 nm CMOS technology with feeding structures at the center tap points. Since, regardless of the transformer sizes, the size and structure of the DC feeds are always the same, L_{CT} and C_{CT} (in Fig. 40) are selected as constant values. By performing a tuning simulation in ADS, L_{CT} and C_{CT} can be extracted from the HFSS-simulated transformer with center tap connections:

$$L_{CT} = 15\ pH$$

$$C_{CT} = 20\ pF$$



(a) (b)

Fig. 38 a) Balanced structure. b) Unbalanced structure with unsymmetrical center tap.

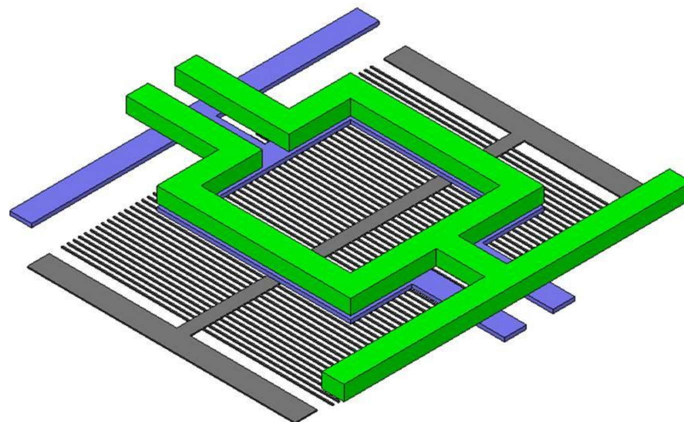


Fig. 39 3D view of the transformer with DC feeding connections at the center tap points of both primary and secondary windings.

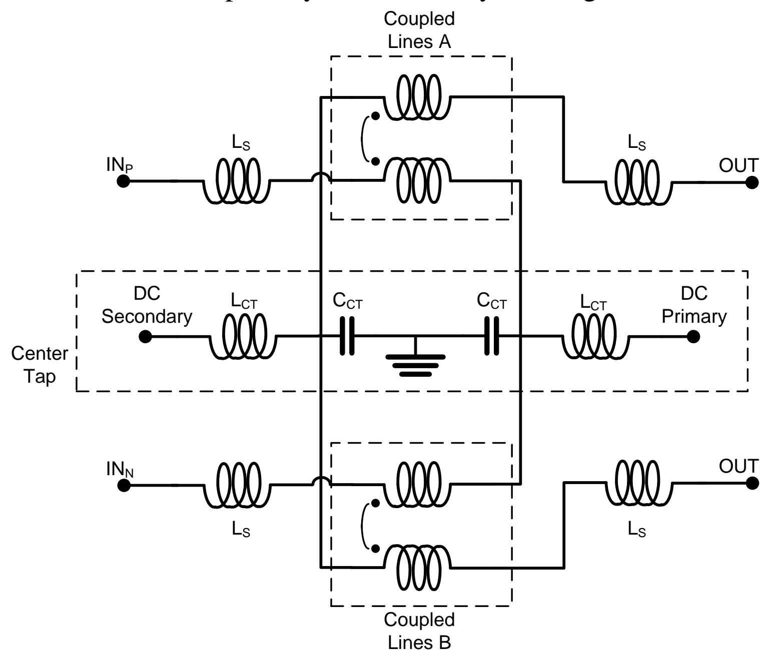


Fig. 40 The complete model of the transformer with center tap.

2.3.4 Transistors

In this section the small signal characterization of nMOS transistors in 90 nm CMOS technology is presented. Two different transistor widths, based on the measured results up to 110 GHz are characterized. The widths of the transistors are optimized for two different cases of low noise and power applications at 60 GHz. For the characterization purpose, the on-chip feeding structures (pads, transmission lines and vias) are extracted from the measured results based on the discussion in RF feeding structure section (Section 2.3.1).

2.3.4.1 Realization and Extraction Techniques

Fig. 41 shows the schematic and the layout of the realized transistor test structures. The transistors are in common-source configuration, with grounded bulk and source terminals. The layout shown in Fig. 42 also includes the details of all the on-chip feeding structures. This includes the RF pad structures in the GSG configuration and the optimized low loss 50 Ω transmission lines (GCTL – Section 2.3.2) up to the device input/output plane (Fig. 42 plane B). A very careful layout design and EM modeling have been carried out to facilitate the accurate device characterization. In order to decrease the coupling between the input and output probe tips, the distance between the two pads is fixed to 200 µm.

The realized devices have been characterized on-wafer. The measurement set-up includes a 110 GHz network analyzer, 110 GHz W-Band probes and external bias tees for gate and drain biasing.

As explained in the pad RF feeding structure section (Section 2.3.1), to accurately extract the transistor's small signal performance, the pad, transmission line and parasitic effects of the transistor core layout have been modeled and de-embedded accurately. Through this technique, we were able to move our reference plane of measurements (Fig. 42 plane A) to the input and output of the transistor (Fig. 42 plane B). Finally, EM models of the transistor layout interconnects (transistor core) were utilized to characterize the transistor with the electromagnetic effects of the layout.

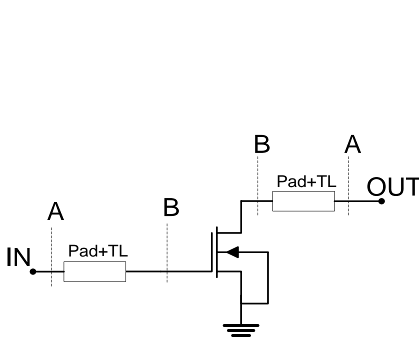


Fig. 41 Schematic of the transistor test structure.

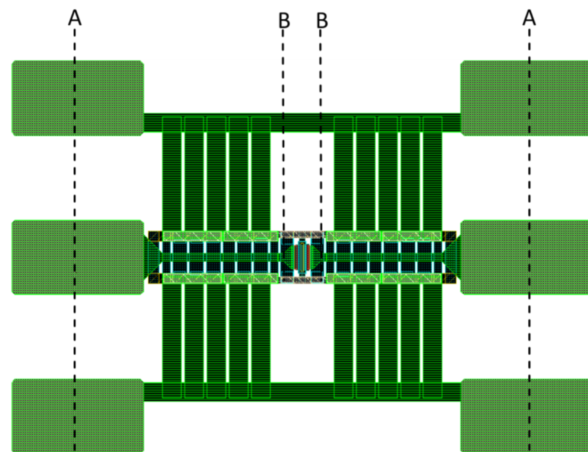


Fig. 42 Layout of the transistor test structure.

Fig. 43 and Fig. 44 compare the simulated and measured S-parameter results on plane A of the 25 µm and 80 µm transistors under the same biasing condition (Vg=0.8 V, Vdd = 1.2V). As is shown in these figures, good agreement between the

measured and simulated results - particularly up to 60 GHz - has been achieved. This confirms the various critical aspects, including the pad model de-embedding method from the measurement, the EM modeling of the transmission lines, the utilized RF transistor models, and the measurement techniques.

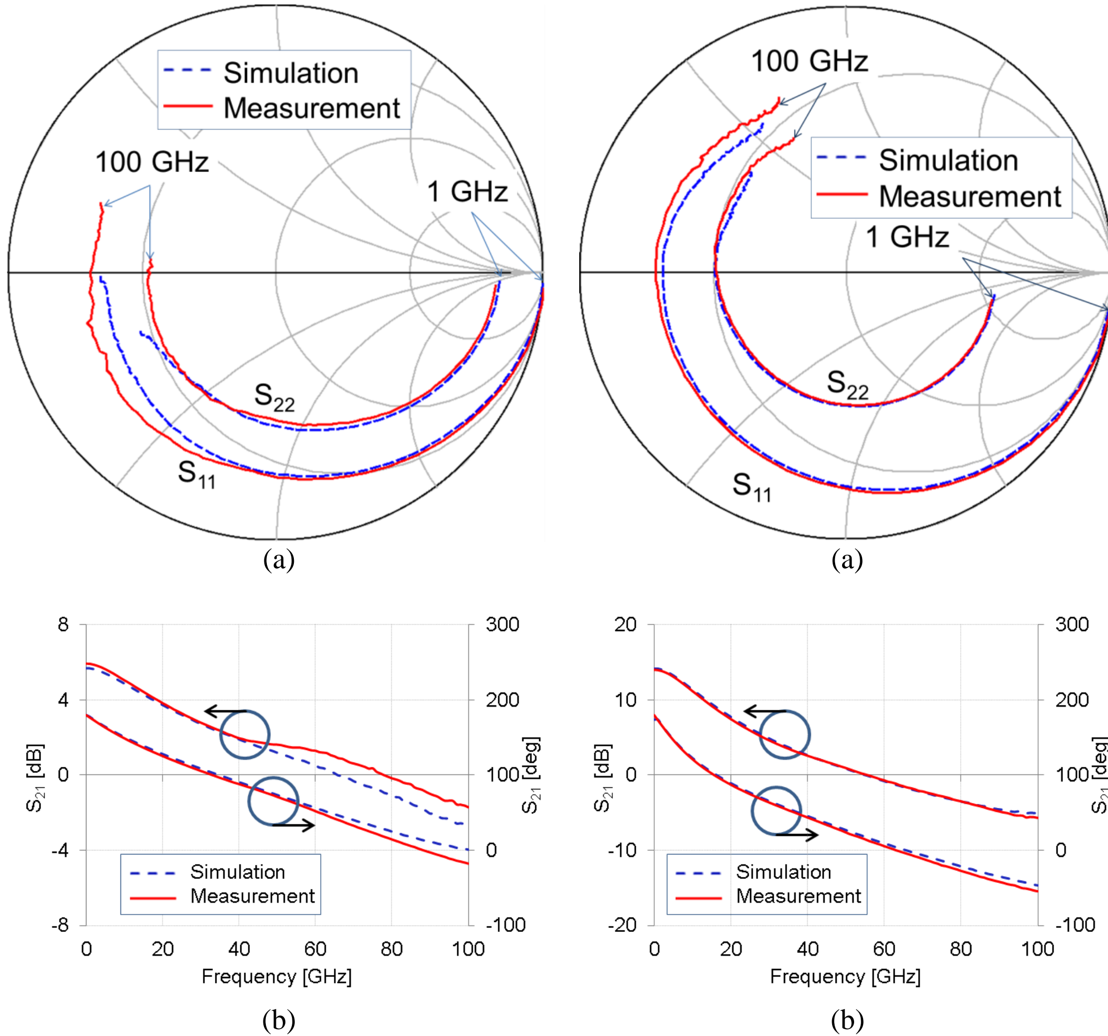
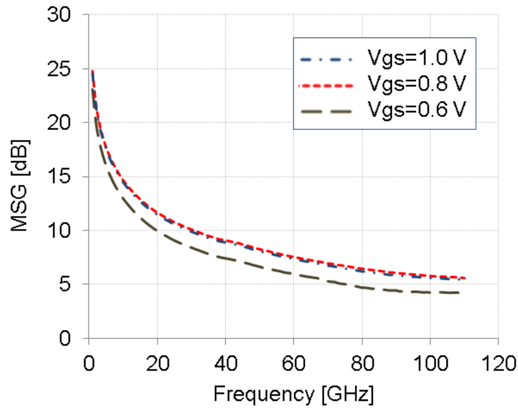


Fig. 43 The S-parameter comparison of a 25 µm CMOS (Vdd=1.2 V and Vg=0.8) before de-embedding (at plane A): a) Input and output reflections. b) Transmission.

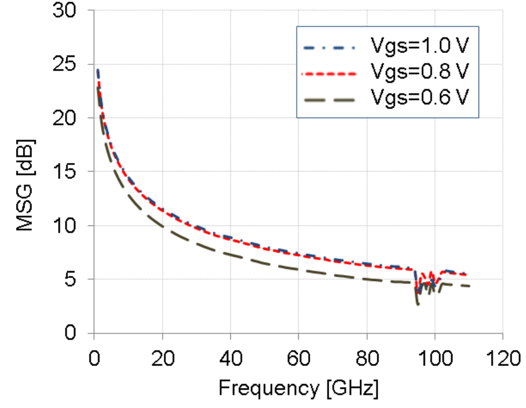
Fig. 44 The S-parameter comparison of a 80 µm CMOS (Vdd=1.2 V and Vg=0.8) before de-embedding (at plane A): a) Input and output reflections. b) Transmission.

Further, through the methods mentioned above, we extracted the fundamental and critical parameters of the transistors alone, such as the maximum stable gain (MSG), the transit frequency (f_t) and the maximum oscillation frequency (f_{max}). The extracted results are presented in Fig. 45 and Fig. 46. The MSG for both transistor sizes and for different bias points is shown in Fig. 45a and Fig. 46a.

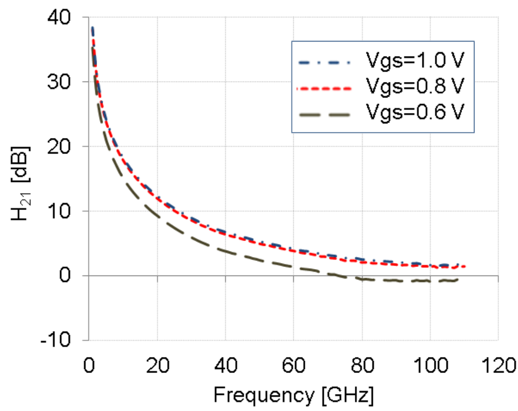
The extracted current gain (H_{21}) results are presented in Fig. 45b and Fig. 46b. From these results, it should be noted that the 80 µm transistor optimized for power amplifier applications has f_t and f_{max} values above 120 GHz for all the bias points. A high f_t and f_{max} are needed in the higher biasing levels in the power amplifier design.



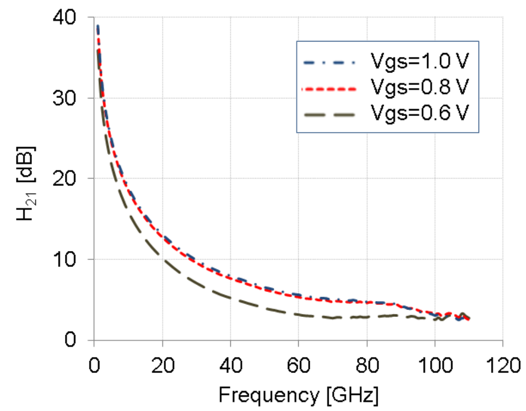
(a)



(a)



(b)



(b)

Fig. 45 The S-parameter comparison of a 25 µm CMOS (Vdd=1.2 V and Vg=0.8) before de-embedding (at plane A) (a) Input and output reflections (b) Transmission

Fig. 46 The S-parameter comparison of a 80 µm CMOS (Vdd=1.2 V and Vg=0.8) before de-embedding (at plane A) (a) Input and output reflections (b) Transmission

2.4 Conclusion

Throughout this chapter, different passive structure models for HBT and CMOS technologies are introduced. The introduced procedures are based on EM simulation modeling and model extraction from measurement. A 3D EM simulation setup based on ANSYS HFSS software was introduced in the first section.

In the second, the modeling of two types of commonly-used passive structures for the HBT PA design (capacitors and transmission lines) was investigated. Based on these investigations, scalable models for both the transmission line and the capacitor were developed. The model was further compared with the EM-simulated and measured results. The good agreement between the simulated and measured results up to 100 GHz has validated the models and EM simulations.

In the third section, firstly, a technique for the extraction of on-chip RF feeding structures up to 100 GHz was presented. The extracted feeding structure can be utilized to extract the accurate model of the passive and active components from the measurements. To justify the accuracy of the technique, two different passive components (a feeding structure with open and short terminations) were realized and

measured. The comparisons showed a very good trend between the S-parameter measurements and the simulations up to 100 GHz. Furthermore, the feeding structure model was utilized to validate the foundry-based models of capacitors for mm-wave applications. Various capacitor sizes were realized and characterized. The comparisons between the measurements and simulations showed the accuracy between the models while the extracted results confirmed the applied techniques up to 100 GHz.

Further, the performances of two different TLs for mm-wave circuit design were investigated. The main difference lies in the bottom metal layer. In the GCTL, the bottom metal layer is used as a ground plane while in the SCTL it is used as a shield. Moreover, the SCTL is wider than the GCTL, but it has less insertion loss and provides a bigger inductance per unit length. The TLs were realized and measured. The EM-simulated and measured results show good agreement up to 100 GHz. With the help of these two TLs, two different amplifiers were designed on 90 nm CMOS technology for 60 GHz band. The matching network of the cascode amplifier was realized using the GCTL while the C.S. amplifier utilizes the SCTL. The one-stage cascode amplifier showed a power gain higher than 5 dB at 60 GHz, while the power gain of the two-stage C.S. amplifier reached 13 dB at around 62 GHz. The simulated and measured results showed good agreement up to 100 GHz, which indicates the functionality of these TL types for the mm-wave band circuit design.

In the third step, and to satisfy the need for a transformer model in up-converter and PA designs, a scalable transformer model based on lumped elements was developed. By comparing the simulated results of the model and the EM simulation with the extracted results from the measurements, good agreement with relatively high precision was shown and, hence, validated the transformer model and the modeling technique.

Finally, the design, realization, de-embedding and characterization of the nMOS transistors up to 110 GHz were studied. Transistors with different sizes optimized for low noise and high power applications were realized and tested under different biasing conditions. The measurements were compared with the simulations including all the passive feeding structures. Very good agreement was shown between the measured and simulated results up to 110 GHz. Moreover, by using the extracted and modeled passive structures, the critical high frequency parameters of the transistors were extracted for various biasing conditions.

Based on the investigations done on this section, all the passive and active components have been modeled with high accuracy. Furthermore, all the components have been optimized for maximum performance, which makes these components appropriate for mm-wave circuit design.

3 HBT PAs

In this chapter, the design, realization and measurement of different PAs on the 0.25 µm SiGe HBT technology are studied. For this purpose, and in order to select the optimum transistor size, biasing circuits and voltages, topology and, finally, the matching networks, many PA design considerations are investigated. In the first section of this chapter, these design considerations are introduced. In the second section, the designed and realized PAs are demonstrated, with a comparison of their simulated and measured results. Finally, the third section concludes the chapter.

3.1 HBT PA Design and Considerations

As shown in Fig. 47, any PA is made up of three main blocks of a PA core, matching networks and biasing networks. In order to achieve the maximum performance of the PA, each block must be designed and optimized separately. In this case, the impact of each part on the PA performance must be considered. These considerations can be categorized as follows [11]-[12]:

- Optimization of the PA transistor core
- Optimization of the biasing networks
- Optimization of the collector DC current
- Increasing the breakdown voltage [53]
- Topology selection
- Broadband design

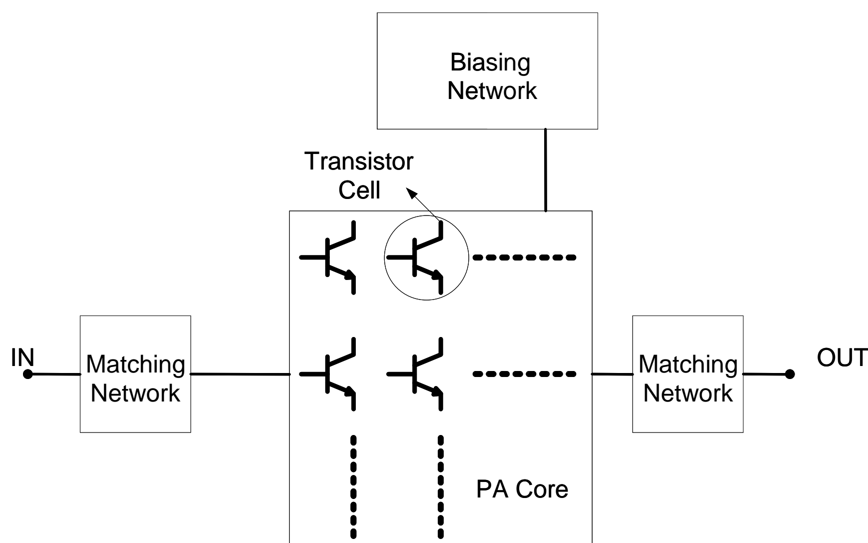


Fig. 47 PA with an array of transistors

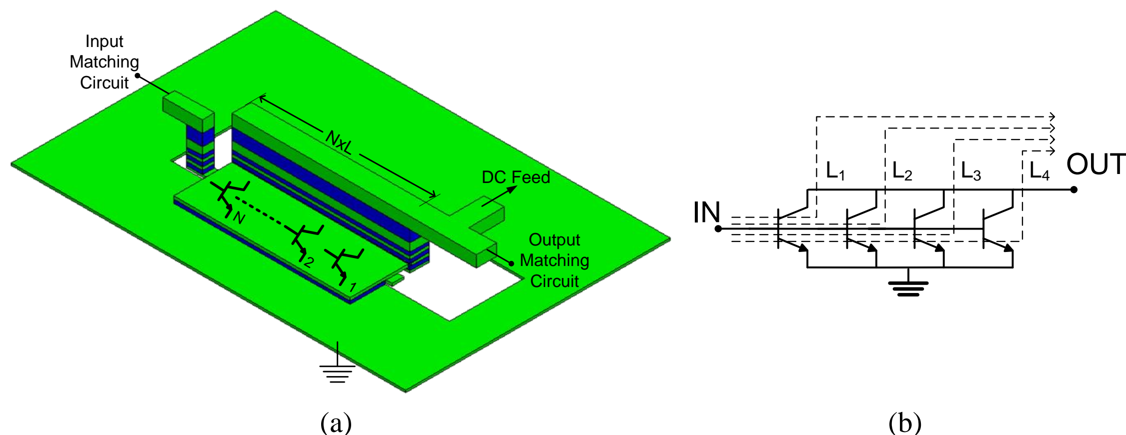
In this section, all the above-mentioned considerations are investigated in detail. The relations between the PA performance and the transistor sizes and the number of parallel transistors are shown. The effects of the power-dependent biasing circuits, the transistors' base impedance and the transistors' DC current density on the large and small signal performance of the PA are studied. The optimum topology for the maximum output power, gain and stability has been selected. Finally, some techniques for broadband PA design are introduced.

3.1.1 PA Transistor Core

All the transistors contributing to the output power of a PA and the interconnections between them are considered as the PA core (Fig. 48a). The schematic of the transistors in the PA core is presented in Fig. 48b. By carefully distributing the transistor cells and designing the corresponding interconnections, the size of the PA core and, hence, the output power can be maximized **[30]**. One of the main considerations for the PA core design is the input-to-output electrical length of each transistor (L_1 to L_4 in Fig. 48b). Any difference between these lengths results in an out-of-phase current-combining at the output of the PA core and, thus, output power degradation. In this case:

$$L_1 = L_2 = L_3 = L_4$$

Even by ensuring a careful design of the PA core, the output power of the PA cannot be increased linearly for the larger transistor sizes and is limited by the operating frequency and the parasitic elements of the passive structure of the PA core. Fig. 48a shows a PA core simulated in HFSS. In this core, the common emitter (C.E.) transistors are placed in a row. As the PA core size increases, the electrical length between two transistors at two opposite corners of the core becomes more significant. This increases the difference between the impedances seen by these two transistor cells. This means that many transistor cells will be terminated with impedances different from the required optimum impedance. Consequently, these cells will make a poor contribution to the output power of the PA.



(a) (b)

Fig. 48 a) 3D layout view of PA core. b) Schematic of the PA core. L_1 to L_4 are equal to electrical length of the signal path through each transistor from input to output.

The effect of increasing the number of transistor fingers has been investigated at 60 GHz for various transistor sizes. The simulated results of a C.E. transistor with an ideal core show a constant gain and increasing OP_{1dB} as the transistor size

increases (Fig. 49a). By including the EM-simulated results of the interconnections (PA core) it can be seen that, by increasing the number of fingers (NoF), the gain decreases constantly (Fig. 49b). However, even a further decrease in gain does not help increasing the output power performance after a 100 μm core length and, hence, OP_{1dB} remains almost constant for any core size above 100 μm (Fig. 49a). The N*L in Fig. 49 plots are explained in Fig. 48a, which is the number (N) of the parallel transistors multiplied by the length (L) of each transistor cell (the outer dimension of each transistor including the trench).

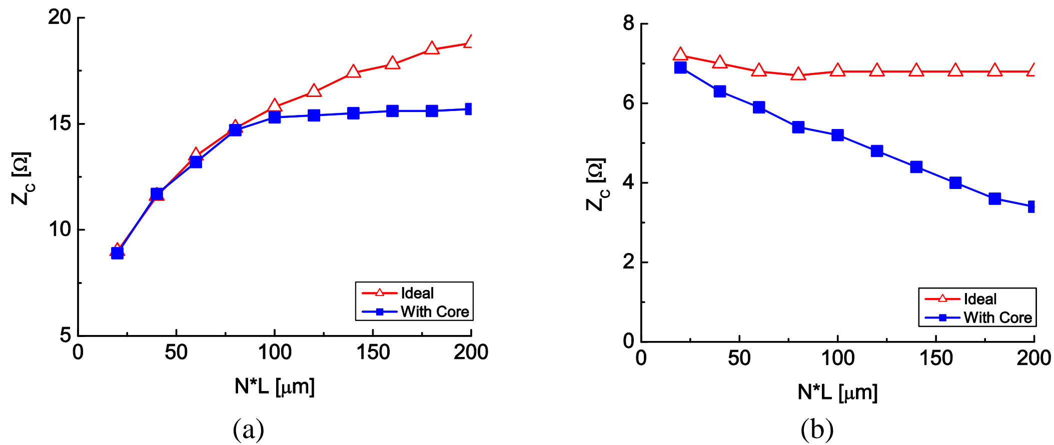


Fig. 49 PA characteristics vs. transistors core size at 60 GHz. a) OP_{1dB} b) Transducer gain.

Furthermore, complicated output-matching networks - due to the high losses of the passive components in the mm-wave band - can usually provide poor quality factors and as such must be avoided. One way to simplify these matching networks is to select the correct transistor size. A larger PA core has lower load reactance, which can make the design of the output-matching network more complicated and result in a lower quality factor of the matching network (Fig. 50). In addition, the larger transistor sizes have more parasitic elements, which can affect the accuracy of the small and large signal models of the transistors. On the other hand, the smaller transistor sizes can provide lower output power. In this case, based on Fig. 50 and Fig. 49, a N*L equal to 80 μm (four parallel transistors with 6 NoF) is quite appropriate for high power and simple matching network PA design.

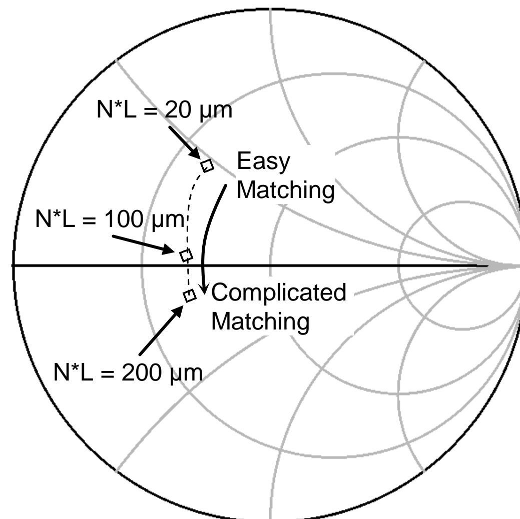


Fig. 50 Optimum load impedance for maximum OP_{1dB}.

3.1.2 Pre-Amplifier Transistor Core

In PA design, utilizing an appropriate pre-amplifier is necessary to improve the gain, PAE and bandwidth (Section 3.1.6) of the PA. However, any pre-amplifier increases the total power consumption. A large pre-amplifier transistor size with high power consumption can deteriorate the total PAE of the PA. Moreover, by selecting very small transistor sizes for the pre-amplifier, the OP_{1dB} of the PA can be affected by the linearity of the pre-amplifier. Due to these problems, the size of the pre-amplifier core must be selected appropriately. A formula can be derived for the minimum pre-amplifier transistor size:

$$NOF_{Pre} > \frac{NoF_{PA}}{10^{\frac{(Gain_{PA,dB}-1)}{10}}} \tag{16}$$

In the above formula, NoF_{PA} is the number of the finger of the power stage transistor and $Gain_{PA,dB}$ is the gain of the power stage in dB. In addition, in this formula it is assumed that both the PA and pre-amplifier transistors have the same base- and collector-biasing voltages.

As the pre-amplifier is usually biased at lower collector current density levels than the PA, the rule of thumb requires a core size at least 3 to 4 times larger than the minimum value. As an example, for the PA with 11 dB gain and 20 fingers, the minimum size of the pre-amplifier core must be larger than 2 fingers, and by applying the rule of thumb this size must be around 6 to 8 fingers so as to avoid any linearity distortion of the PA.

3.1.3 Biasing Networks

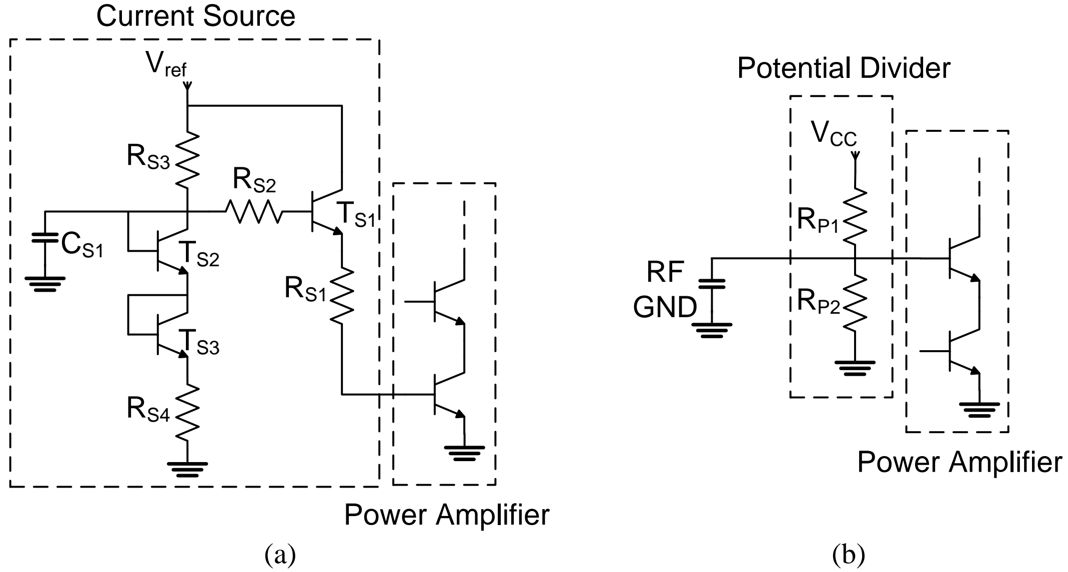
The C.E. transistors in the cascode topology are biased with the help of a current source (Fig. 51a) while the C.B. (Common Base) transistors are biased with a potential divider and RF ground at their base (Fig. 51b). The main advantage of the current source is its sensitivity to the input power, which helps to increase the linearity of the PA [55].

Fig. 52a compares the base voltage (V_{BB}) of the C.E. transistor in Fig. 51a and its collector current for different base-biasing networks (the introduced current source and resistive potential divider). V_{BB} falls much faster in the case of a resistive biasing network than the current source at higher input powers (Fig. 52a). This results in a much smaller collector current increase (Fig. 52a) in the resistive-biasing network and, consequently, lower output power.

Fig. 52b presents the change in the PA load line on the IV curve. With the lower input powers, the load line is at the lower DC current, which thus results in a lower DC consumption. As the input power increases, the load line moves towards the higher DC currents, which would subsequently increase the load line amplitude and the output power.

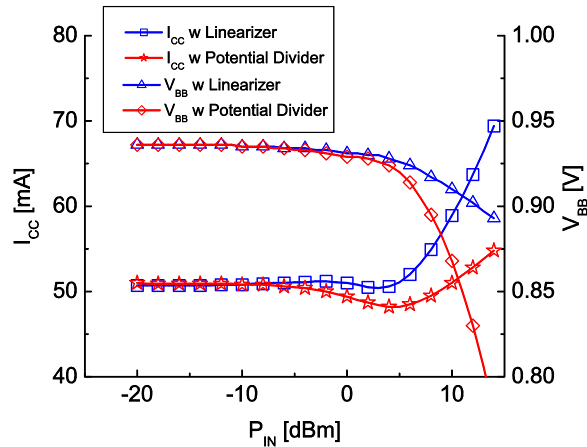
Finally, as explained in [53] in the HBT technology, the breakdown voltage of the transistors are a function of their base impedances. The lower base impedance can result in a larger breakdown voltage (Fig. 53) and, hence, improve the output power. It can be observed from Fig. 53 that at the DC level the breakdown voltage of the C.E. amplifier can be increased from 2 V to around 2.8 V by decreasing the base termination from open to 100 Ω. This can still be improved to 3.5 V by further

decreasing the base impedance. In the cascode topology, the breakdown voltage of the C.B. transistor can be significantly enhanced (Fig. 57b) by connecting its base to the RF ground ([16] and [38]).

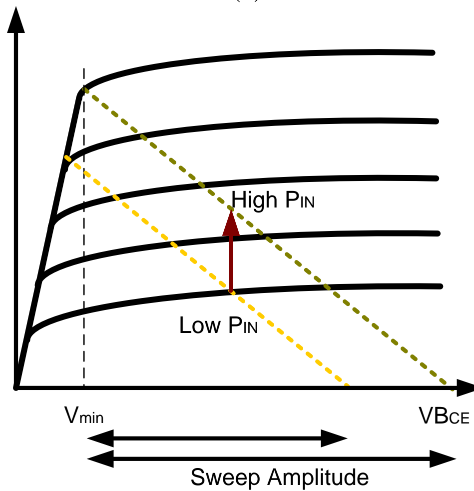


(a) (b)

Fig. 51 a) Biasing network of the C.E. transistor. b) Biasing network of the C.B. transistors.



(a)



(b)

Fig. 52 a) Comparison between the introduced current source and resistive potential divider. b) Load line variation of the PA by input power (P_{in}) with the introduced current source.

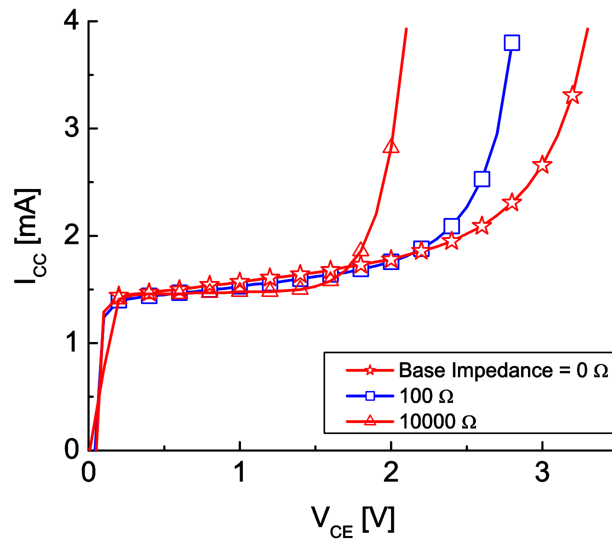


Fig. 53 BVCE for different base terminations.

3.1.4 Collector Current

Two important factors in the biasing current selection are the f_t and f_{max} of the transistor. In order to achieve the maximum performance of the PA, the collector current must be selected within the range where f_t and f_{max} are maximized. Fig. 54 shows that by selecting collector current between 2.2 mA to 2.5 mA per transistor finger maximum f_t and f_{max} is achievable. However, higher current densities can result in a higher output power, due to model validity degradation, and this is not recommended by the foundry. Fig. 54 also shows a decrease in f_t and f_{max} by increasing the NoF. This appears as the parasitics increase by increasing the NoF.

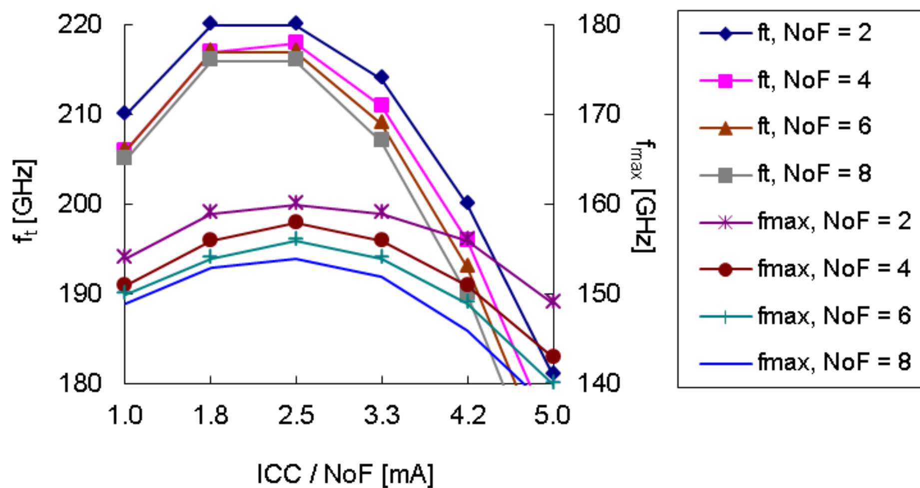


Fig. 54 F_t and F_{max} vs. collector current.

3.1.5 Topology Selection

C.E. and cascode topologies are commonly used in PA design. The main advantages of each topology are:

- Cascode topology:
  - ✓ Higher isolation (Fig. 55) and, hence, better stability
  - ✓ Higher gain (Fig. 56)
  - ✓ Larger output voltage swing (Fig. 57) and, hence, more output power (Fig. 56)
- C.E. topology:
  - ✓ Less parasitic elements and a less complicated design procedure
  - ✓ Better f_t due to less parasitic elements (Fig. 58)

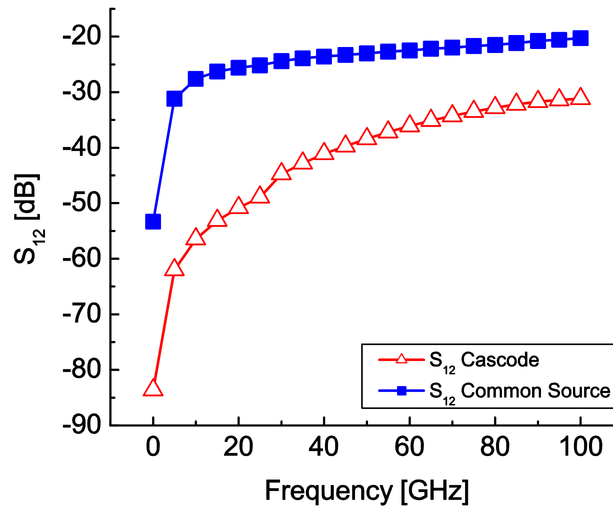


Fig. 55 Isolation (S_{12}) vs. topology.

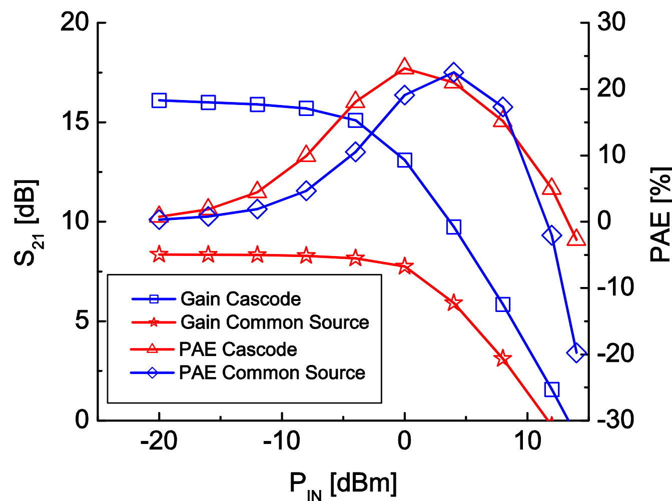


Fig. 56 Large signal performance. C.E. vs. Cascode.

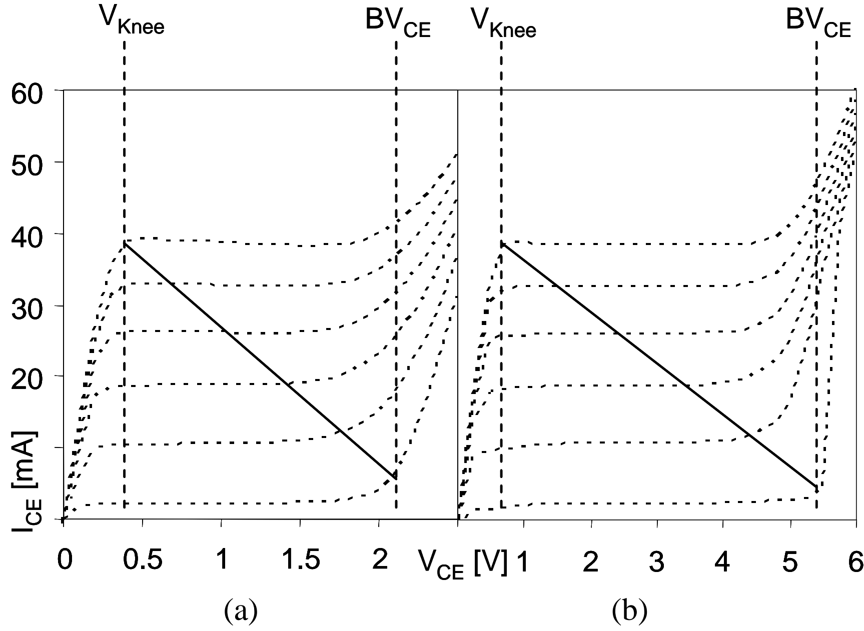


Fig. 57 The IV-curves of the SiGe HBT: a) Common emitter b) Cascode

As the parasitic elements of the C.E. transistor core are significantly less than for the cascode topology, its design procedure is easier. Furthermore, and for the same reason, the f_t of the C.E. is much higher than the cascode topology (Fig. 58). As shown in Fig. 58, the f_t of the C.E. is around 200 GHz while the cascode has a f_t of 120 GHz. This is critical for those applications with a frequency of operation near f_t. On the other hand, the cascode topology shows better performance in stability (due to higher isolation), gain and output power (Fig. 55 and Fig. 56). Fig. 57 shows the IV-curves of these two topologies. In the cascode topology (with stacked configuration [89]), the breakdown is around 5.5 V but, in the C.E. topology, it only reaches 2.2 V. This means that almost a 4.5 V voltage swing is possible using the cascode topology. In comparison with the C.E. configuration, this voltage swing is almost two and a half times higher ($BV_{CE} - V_{Knee} = 1.7$ V).

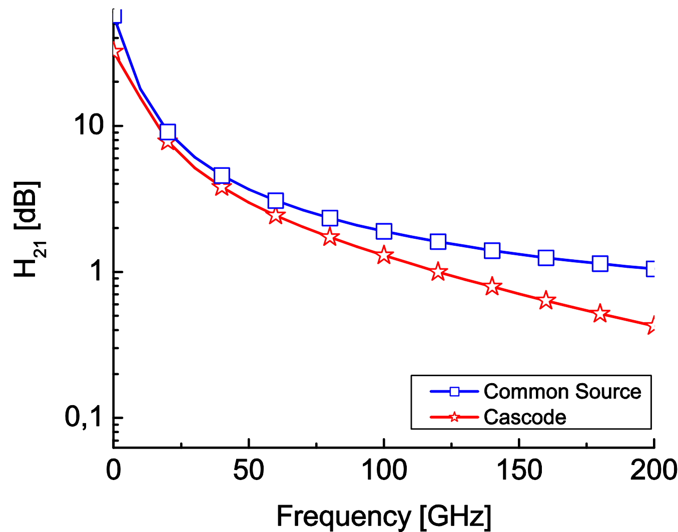


Fig. 58 f_t vs. topology.

3.1.6 Broadband Design

Designing broadband PAs for a mm-wave band requires the accurate modeling of the passive components and the fine-tuning of matching networks. Some V-band broadband PAs have already been reported using CMOS and HBT technologies ([11], [51] and [85]). The broadband design techniques are required for both the large and small signal performances of the PAs. Simultaneous maximum bandwidth and high output power and efficiency are the main objectives to achieve. In order to achieve these goals, one PA must have simultaneous broadband gain, broadband small signal input-matching and broadband large signal output-matching. To overcome these problems, different design procedures for broadband PA design are suggested.

Compared to the implementation of an amplifier with broadband gain, the design of a similar narrowband single-stage amplifier with high gain is much more straightforward. This is mainly due to the quality factor limitations of the complex broadband matching networks and their corresponding chip sizes. Instead of designing a single broadband amplifier, several narrow band amplifiers with different center frequencies can be cascaded (Fig. 59). By fine-tuning the center frequency of each amplifier, the bandwidth of the total amplifier can be enlarged. Fig. 59 illustrates this method using two narrow-band amplifiers (a pre-amplifier and a power stage) matched at two different frequencies. The cascaded connection of each amplifier results in the overall broadband performance of the multistage amplifier.

Although the above procedure sounds quite easy, it can face many difficulties during the design procedure. These difficulties lie mainly in the frequency dependency of the matching networks. In those cases where the above procedure faces a difficulty, some tuning and optimization techniques can be utilized instead in order to select the correct inter-stage matching network components for broadband gain performance. All these procedures have been explained and employed in [11], [51] and [85].

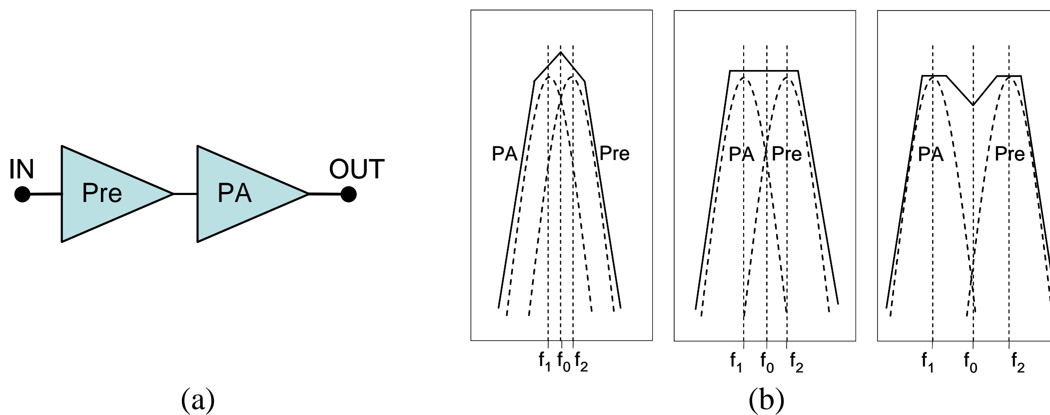


Fig. 59 a) Cascaded power stage and pre-amplifier. b) Total transducer gain for different frequency spacing between f_1 and f_2.

In the case of input-matching network design, since a lossy input-matching network does not affect the output power or linearity of the PA, a complicated network can be utilized to have as broadband as possible form of input-matching to cover the entire desired frequency bandwidth. However, complicated matching networks at mm-wave frequencies are quite lossy and, hence, they are not appropriate for output-matching networks. In this case, and unlike the input-matching network, the output-matching network has to be designed so as to be as simple as possible.

3.2 Realized V-band SiGe HBT Power Amplifiers

In this section, four PAs are designed and realized in the 0.25 µm HBT technology and the realizations have been thoroughly characterized. The PAs are designed for V-band (60 GHz) applications. As discussed previously (Section 3.1.5), in this technology the f_t of the cascode topology is above 120 GHz (two times higher than 60 GHz), which makes this technology and the cascode topology appropriate for the V-band PA design.

In these designs, two types of PAs are targeted. The main differences between these PAs lie in the P_{OUT} and the DC power consumption (P_{DC}). For each type, a primary version has been designed, realized and measured. Consequently, the primary versions have been extended and improved in the secondary versions. In this document, the second PA is the extension of the first PA and the fourth PA is the extension of the third PA. In the rest of this paper, the first and second PAs are referred as ‘low power PAs while the third and fourth PAs are referred as ‘high power PAs. The general criteria for both types of PAs are listed in Table. 2.

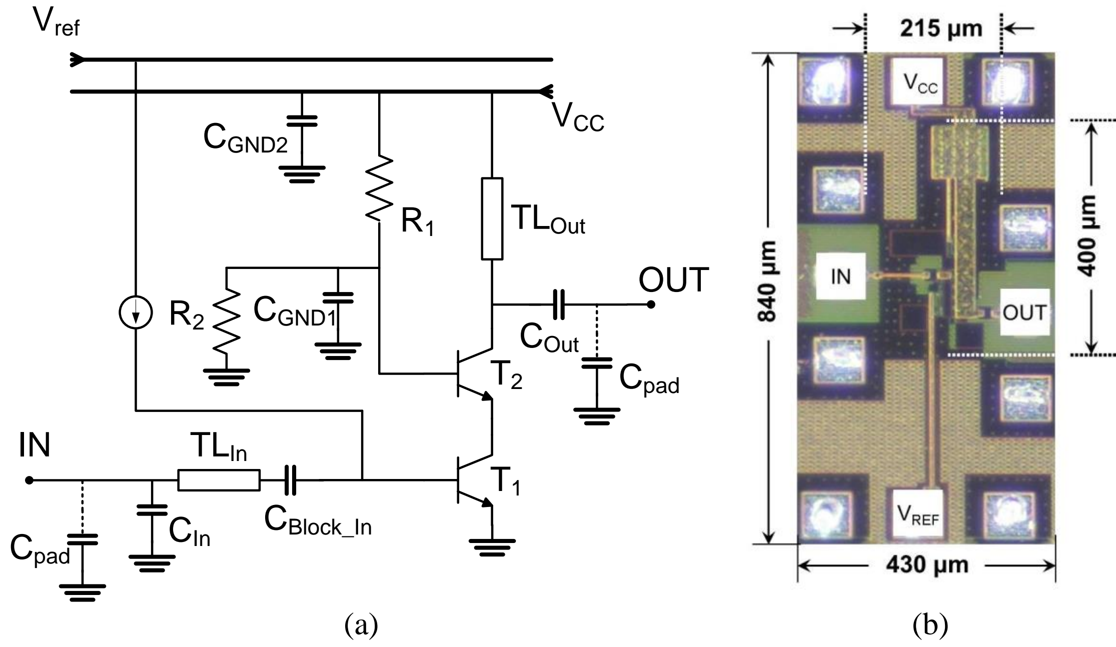
Table. 2 HBT PA design criteria

Properties	Low Power PAs	High Power PAs
Gain [dB]	20	20
P_{sat} [dBm]	15	18
OP_{1dB} [dBm]	14	15
PAE [%]	15	15
P_{DC} [mW]	200	400
Bandwidth [GHz]	50 – 70	50 – 70

As shown in Table. 2, most of the design criteria for both types of PAs are the same. The main difference lies in the P_{sat} of the PAs. In order to improve the output power by 3 dB, a current-combining technique has been investigated and utilized in the high power PAs. Besides, all the PAs are designed for high gain, high PAE and the maximum coverage of the V-band.

3.2.1 Low Power PA – 1st Version

In the first PA, a single-stage amplifier with the cascode topology is designed [15]. Fig. 60 shows the schematic and the chip micrograph of the PA. The values of all the PA components are also presented in Table. 3. The one-stage PA has been designed for maximum P_{OUT}, gain and PAE. Both the input and output-matching networks are designed at the P_{sat} level to achieve the maximum OP_{1dB} and PAE. In addition, the cascode topology has been selected for better P_{OUT}, gain and stability (Section 3.1.5). The PA achieved a 1dB gain bandwidth of more than 9 GHz, from 57 GHz to 66 GHz, and a 3dB gain bandwidth of more than 18 GHz, from 51 GHz to 69 GHz. Furthermore, the large signal matching at the output resulted in an OP_{1dB} higher than 11.5 dBm and a PAE of around 9%, from 57 GHz to 65 GHz, with more than 14 dBm P_{sat}. The total size of the PA is 0.36 mm^2 and the active size of the PA is 0.086 mm^2.



(a) (b)

Fig. 60 a) Schematic of the PA. b) Chip-Photo

Table. 3 The values of the PA components.

Parameter	Value	Parameter	Value
TL_{In} [µm] (W/L)	3/90	**C_{GND1} [pF]**	8
TL_{Out} [µm] (W/L)	30/250	**C_{GND2} [pF]**	6
C_{In} [fF]	130	**R_1 [kΩ]**	1.5
C_{Out} [fF]	500	**R_2 [kΩ]**	3
C_{Block_In} [fF]	500	**C_{pad} [fF]**	20
$T_1 = T_2$ (NoF)	4×6		

Table. 4 The current source elements (Fig. 51a).

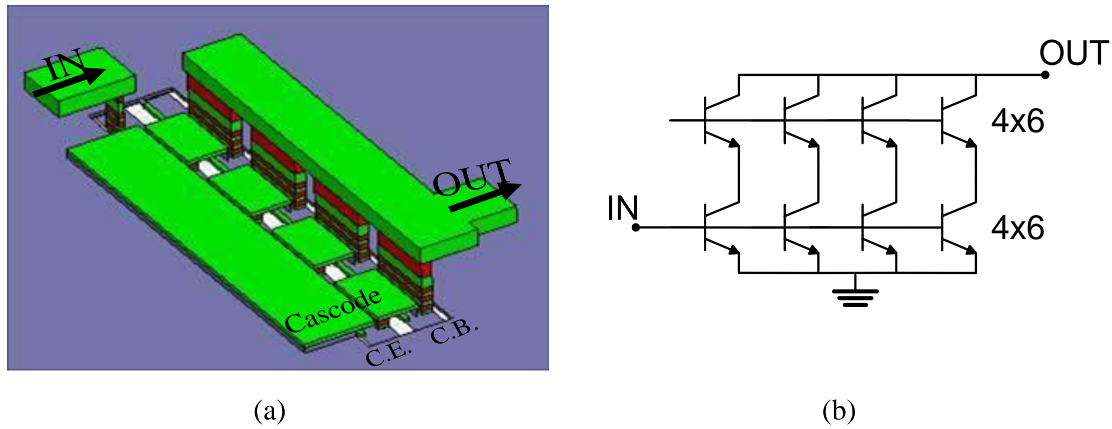
Parameter	Value
$T_{S1} = T_{S2} = T_{S3}$ (NoF)	1×1
R_{S1} [Ω]	30
R_{S2} [kΩ]	2
R_{S3} [kΩ]	3.2
R_{S4} [Ω]	500
C_{S1} [pF]	2

3.2.1.1 PA Design

The value of all the components utilized in the PA and the current source are given in Table. 3 and Table. 4. The schematic of the current source is also given in Fig. 51a. In this section, the detailed design of each part is explained.

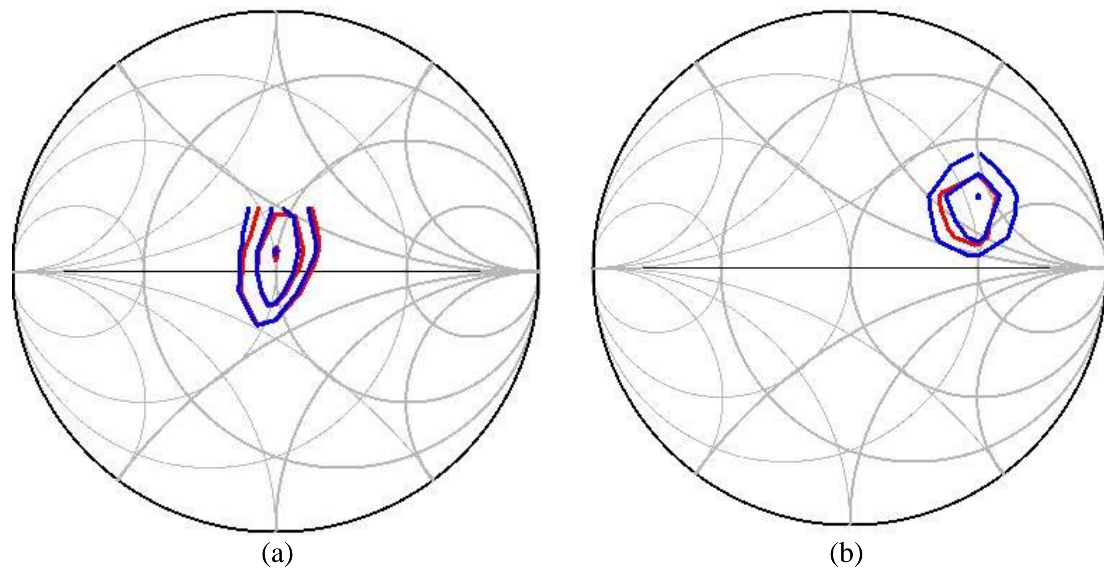
Fig. 61a-b presents the PA transistor core. The PA core is designed as four parallel cascode amplifiers with an equal electrical length from input-to-output for minimum signal distortion at the output (Section 3.1.1). Both the common base and the C.E. transistors in each cascode amplifier have 6 fingers.

The introduced current source (Section 3.1.3) has been utilized for the biasing of the C.E. transistors. Furthermore, a potential divider with a relatively low ohmic RF ground has been utilized for the biasing of the common base transistors. As mentioned earlier, the low ohmic RF grounds are necessary for both the gain and breakdown voltage (Section 3.1.3) improvement of the cascode topology. The biasing voltages are 3.3 V for the V_{CC} and 2.6 V for the current source (V_{ref}). The total current consumption of the PA is 46 mA.



(a) (b)

Fig. 61 a) 3D view of the PA transistor core for a four parallel Cascode.
b) PA core schematic.



(a) (b)

Fig. 62 The load-pull simulation of the PA after matching. a) At P_{sat}. b) At small signal.
Red: Power with 0.5 dB step. Blue: PAE with 2% steps.

As mentioned earlier, the output has been matched at the P_{sat} level. Fig. 62a shows the large signal matching of the PA output (including the matching network). The center of the load-pull circles point to the maximum power and efficiency. The red contours show the P_{OUT} with a step of 0.5 dBm, decreasing from the maximum power, while the blue circles show the PAE contours with a step of 2%, decreasing from the maximum efficiency. The simulated results show a maximum power of 15 dBm and a maximum efficiency of 15%, including all the matching networks and the RF pad structures.

The main consequence of large signal output matching of the PA is poor output-matching at the small signal level (Fig. 62b). This can result in output-matching as low as 5 dB (based on the simulated and measured results). Moreover, as in the single-stage amplifiers the OP_{1dB} and P_{sat} can be affected by input-matching (due to finite isolation between output and input terminals), the input of the PA has to be designed at the higher power levels with the help of source-pull simulation setup. Designing the input-matching at higher input power levels can further result in poor small signal input-matching.

Finally, with help of the EM simulation, input and the output-matching networks and the PA core have been characterized and optimized. In addition, in order to extract the coupling elements, the whole PA has been simulated in HFSS (Fig. 63).

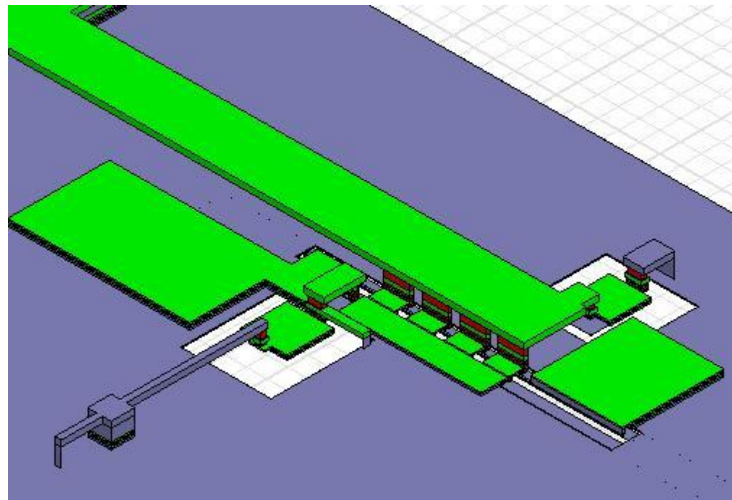


Fig. 63 3D view of the EM simulated PA.

3.2.1.2 Measurement vs. Simulation

Both large and small signal measurements are performed on the chip at room temperature. The small signal measured results show good agreement with the simulation up to 100 GHz. Fig. 64 shows the small signal gain and the isolation of the PA. Around 8.8 dB gain has been achieved at 62 GHz with 1dB gain bandwidth of more than 9 GHz, from 57 GHz to 66 GHz, and 3dB gain bandwidth from 51 GHz to 69 GHz. Also, and as expected, due to the employment of the cascode topology, an isolation better than 25 dB is achieved within the entire band.

As mentioned before, the small signal matching at both the input and output terminals is significantly affected by the large signal matching techniques utilized. Fig. 65 shows around 5 dB and 8 dB matching, respectively, for the output and input terminals.

Finally, the large signal measurement shows the good performance of the PA within the required frequency band from 57 GHz to 66 GHz (Fig. 66 and Fig. 67).

More than 11.5 dB OP_{1dB} with 9% PAE is achieved during measurement, from 57 GHz to 65 GHz. Table. 5 presents the large signal characteristics of the PA versus the frequency.

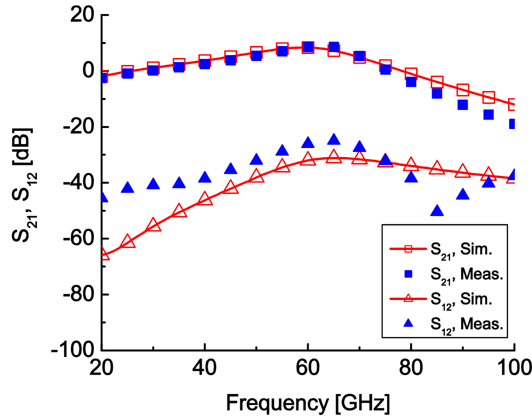


Fig. 64 Small signal gain and isolation. Sim. vs. Meas.

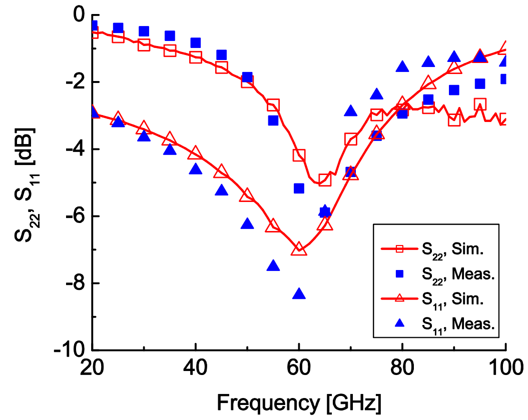


Fig. 65 Small signal matching. Sim. vs. Meas.

Table. 5 PA characteristics over the frequency.

Freq. [GHz]	58	60	62	64	66
Gain [dB]	8	8.6	8.8	8.8	7.8
OP_{1dB} [dBm]	13.3	12	12	11.8	10.8
P_{sat} [dBm]	>14	>14	>13	>13	>12
PAE [%]	9.8	9.2	9.6	9.2	7

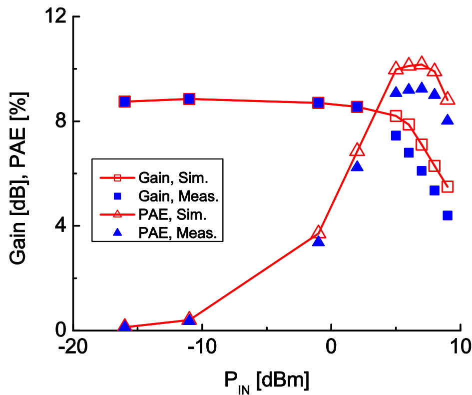


Fig. 66 Gain and PAE vs. input power at 60 GHz.

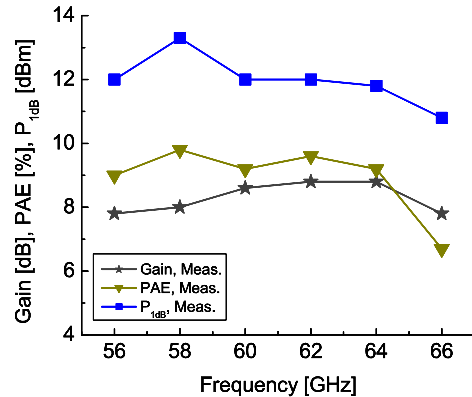
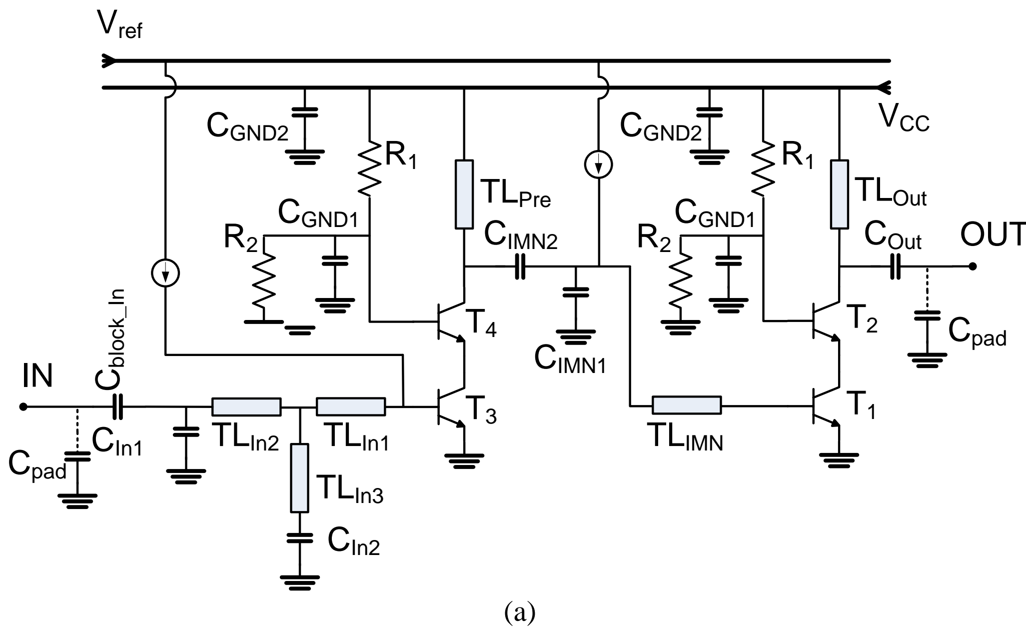


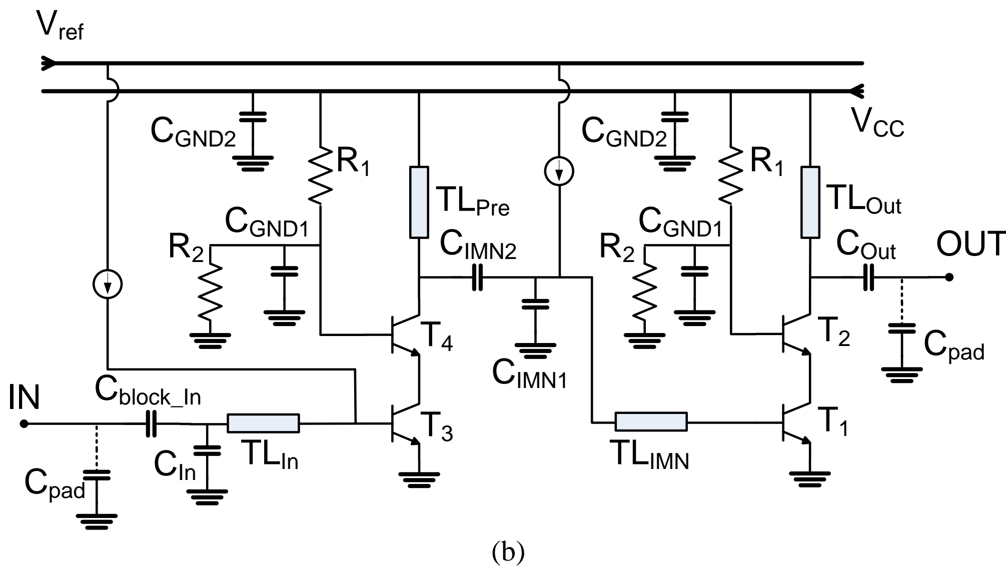
Fig. 67 PAE, OP_{1dB} and gain vs. frequency.

3.2.2 Low Power PA – 2nd Version

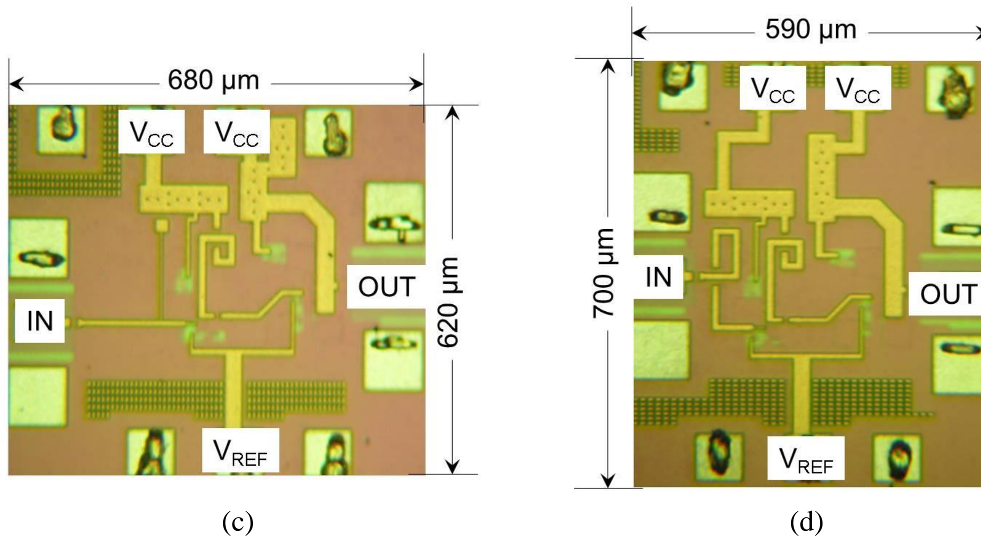
The first PA is extended and improved into two PAs (PA_1 and PA_2) with higher targeted PAE and OP_{1dB} [11]. A pre-amplifier has been utilized to increase the total gain of the PAs. The small signal gain (S_{21}) has been optimized to be almost flat over a wide frequency band, covering from 50 GHz to 70 GHz. The broadband gain performance of the PAs is achieved by tuning the inter-stage matching network in the cascaded structures (Section 3.1.6). The two-stage PAs utilize the cascode topology to boost the gain, power and output-to-input isolation (Section 3.1.5). A flat gain of around 20 dB with a 3 dB bandwidth covering almost the entire V-band (50 GHz to 70 GHz) is achieved. The maximum OP_{1dB} is 14 dBm, with a peak PAE of 15%. Good agreement is observed between the simulated and measured results, which further confirms the accuracy of the presented design methodology. The schematics and the chip micrographs of the PAs are presented in Fig. 68. The active chip sizes of the PAs are 0.2 mm^2 and 0.19 mm^2 and their total sizes are 0.42 µm^2 and 0.41 µm^2.



(a)



(b)



(c) (d)

Fig. 68 Schematics and chip micrographes of the: a)PA_1. b)PA_2. c) PA_1. d) PA_2.

Table. 6 The values of the PA_1 components.

Parameter	Value	Parameter	Value
$T_1 = T_2$ (NoF)	4×6	C_{In1} [fF]	45
$T_3 = T_4$ (NoF)	1×6	C_{In2} [fF]	91
TL_{In1} [µm] (W/L)	7/15	C_{IMN1} [fF]	100
TL_{In2} [µm] (W/L)	7/130	C_{IMN2} [fF]	50
TL_{In3} [µm] (W/L)	3/151	C_{Out} [fF]	500
TL_{IMN} [µm] (W/L)	7/150	C_{Block_In} [fF]	200
TL_{Out} [µm] (W/L)	30/250	C_{GND1} [pF]	8
R_1 [kΩ]	1.5	C_{GND2} [pF]	6
R_2 [kΩ]	3	C_{pad} [fF]	20

Table. 7 The values of the PA_2 components (The rest are the same as PA_1).

Parameter	Value
TL_{In} [µm] (W/L)	10/420
TL_{IMN} [µm] (W/L)	7/130
C_{In1} [fF]	200
C_{In2} [fF]	50
C_{IMN2} [fF]	35

Table. 8 Current source values (Fig. 51).

Parameter	Value			
	PA_1		PA_2	
	Power Stage	Pre-amp.	Power Stage	Pre-amp.
$T_{S1} = T_{S2} = T_{S3}$ (NoF)	1×1	1×1	1×1	1×1
R_{S1} [Ω]	30	50	30	50
R_{S2} [kΩ]	2	2	2	2
R_{S3} [kΩ]	5	13	3.2	11
R_{S4} [Ω]	500	500	500	500
C_{S1} [pF]	2	2	2	2

3.2.2.1 PA Design

The value of all components utilized in these PAs and the current sources are given in Table. 6, Table. 7 and Table. 8. The schematics of the current source are also given in Fig. 51a. In these designs, the current sources of PA_1 and PA_2 exhibit certain differences. These differences have helped in achieving different biasing conditions under the small and large signal power levels. In this section, the detailed design of each part of the power amplifiers is explained.

Based on the presented design procedure (Section 3.1.6), two broadband PAs are developed. Each PA includes two cascaded amplifiers, consisting of a cascode pre-amplifier followed by a cascode power stage. The PAs are designed to work through the V-band with approximately 20 dB small signal gain. The outputs of the PAs are matched at 60 GHz for the maximum linearity and PAE. In the following sections, the design of different parts of the PAs, including the amplifier cores (pre-amplifier and power stage), input, output and inter-stage matching networks, are explained.

a) PA Core and Output-matching: The PA core selection is introduced in section 3.1.1 and section 3.2.1. Based on the selected PA core, an output-matching network is designed. The output of the PA is matched at the large signal level to achieve the maximum power performance. The main problem in the design of the output-matching network of the power stage is the selection of the corresponding input power level. To find the optimum input power level for the maximum OP_{1dB} and P_{sat} performance, a cascode topology with an output-matching network is simulated for various input power levels (Fig. 69a). Fig. 69b shows the simulated results for various input power levels. At each power level, the optimum output-matching network is designed based on the load-pull simulation and modeled with the help of an EM simulator. With regard to Fig. 69b, the output-matching network of the power stage is designed for an input power level of 0 dBm. For this power level, the OP_{1dB} reaches a maximum of 15 dBm while maintaining satisfactory gain and output-matching. The 3D view of the power stage is presented in Fig. 69c.

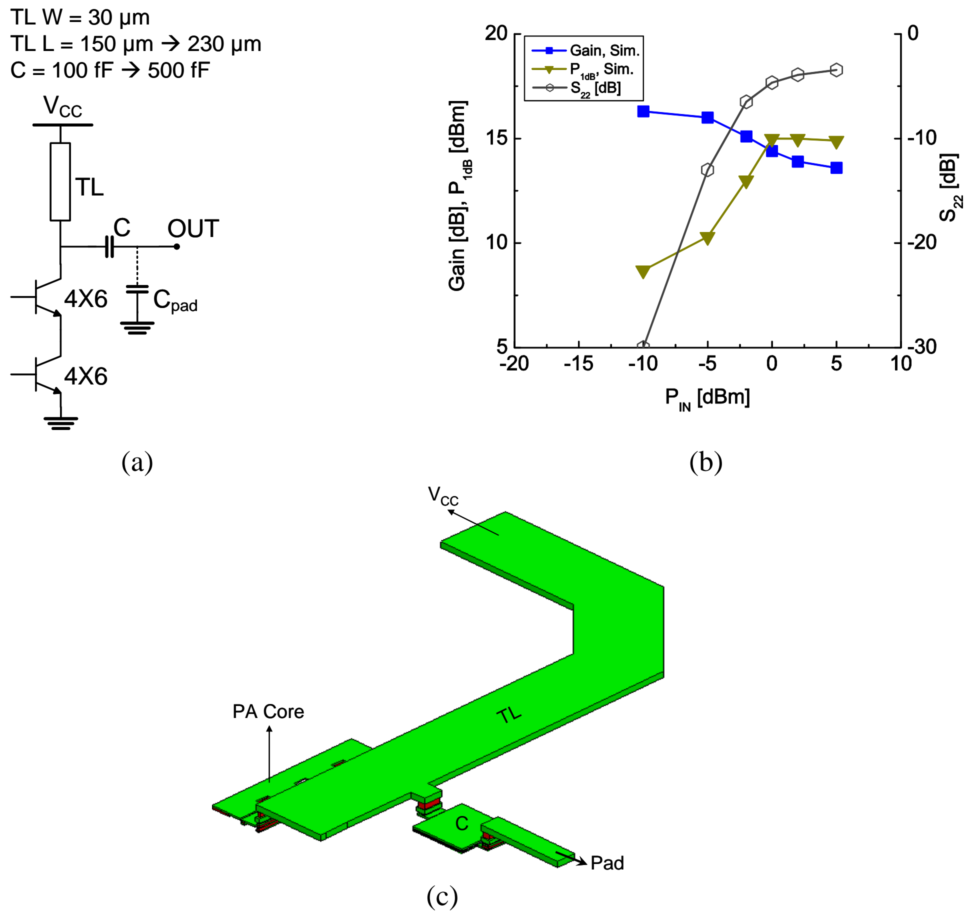


Fig. 69 PA core with output matching: a) Schematic. b) Performance vs. output matching network variation at 60 GHz. c) 3D layout view of the PA core and output matching.

The results of the large and small signal load-pull simulations are presented in Fig. 70. As expected, and due to the large signal matching, the small signal matching is quite poor (Section 3.2.1).

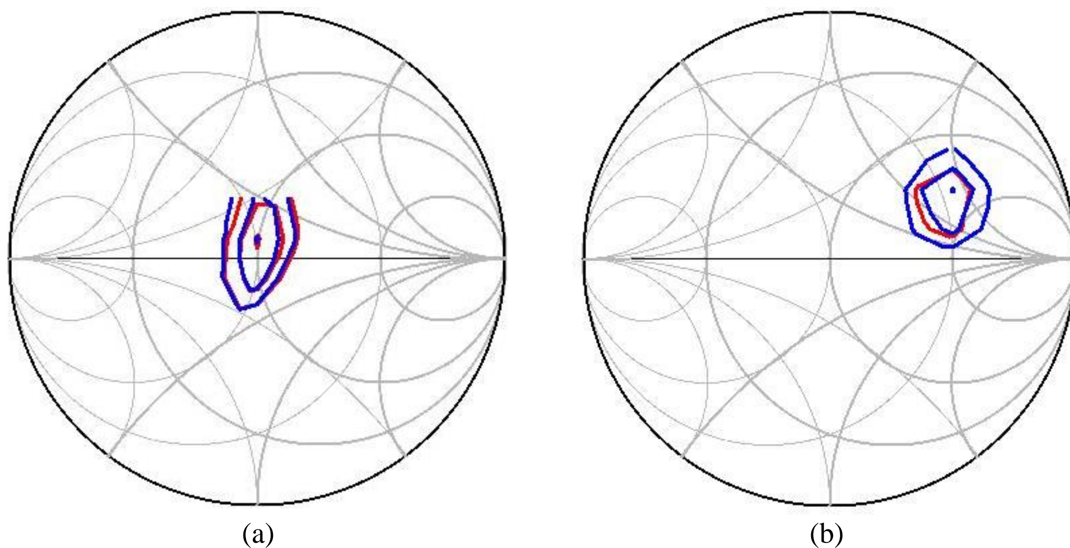


Fig. 70 The load pull simulations of the PA after matching. a) At P_{sat}. b) At small signal. Red: Power with 0.5 dB step. Blue: PAE with 2% steps.

b) Inter-stage Matching Network: The inter-stage matching network plays the most important role in the broadband design. The input-matching network of the power stage and the output-matching network of the pre-amplifier must be designed at two different frequencies (Section 3.1.6). The correct selection of these frequencies is important as they determine the bandwidth and the in-band gain variations. The intermediate matching must match the output of the pre-amplifier at f_1 to the input of the power stage at f_2. Fig. 71 presents the designed intermediate matching circuit. In both of the PAs designed in this work, f_1 is selected at 55 GHz but f_2 is selected at 65 GHz for PA_1 and 67 GHz for PA_2.

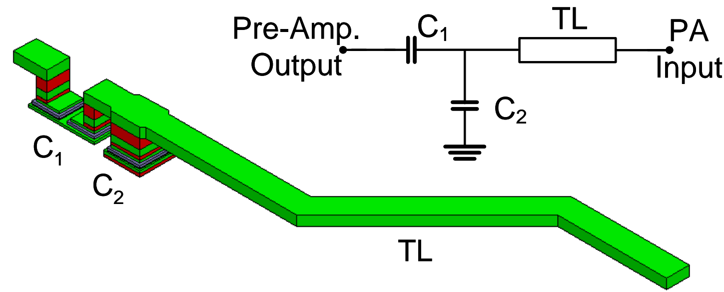
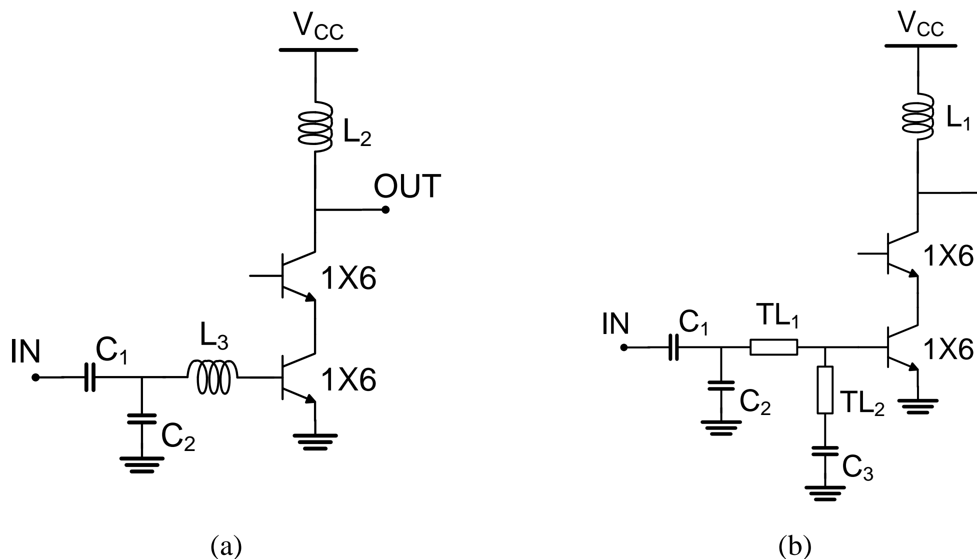


Fig. 71 Schematic and 3D view of the intermediate matching network.

c) Pre-Amplifier and Input-matching: Having designed the PA core, the pre-amplifier core must be designed. By using (16) introduced on section 3.1.2, the approximate core size can be calculated. By employing a tradeoff between the matching network loss and the minimum required pre-amplifier transistor size, a six finger transistor is selected for the pre-amplifier.

To improve the broadband characteristic of the total PA, a broadband input-matching network is designed for the pre-amplifier as well. The principle of the design is introduced in [12]. For each of these PAs, a different input-matching network is designed. The second matching network has a better Q-factor, but it occupies more space than the first one. The schematic and the 3D layout of the designed matching networks and pre-amplifier are presented in Fig. 72.



(a) (b)

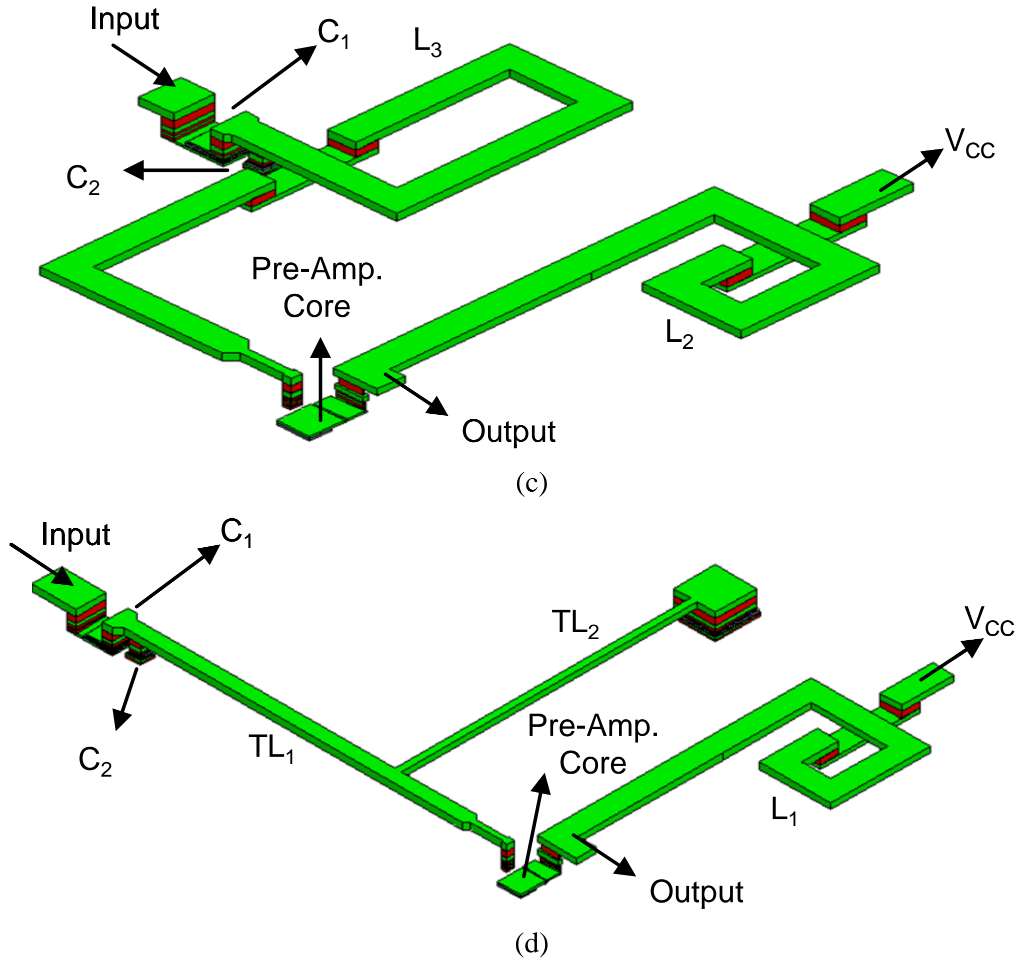
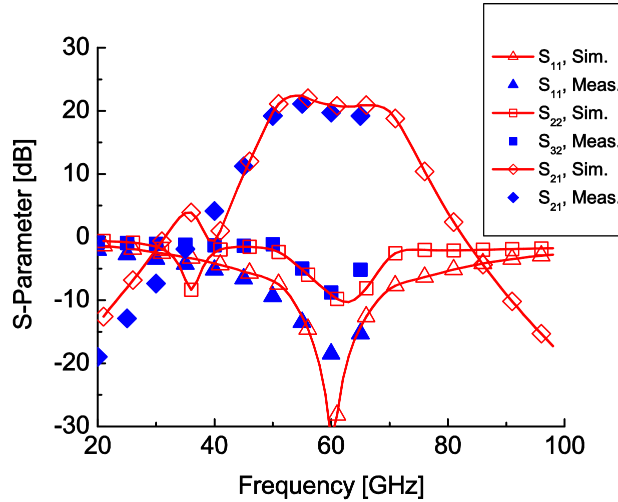


Fig. 72 Schematic and 3D view of: a&c) Pre-amplifier 1. b&d) Pre-amplifier 2.

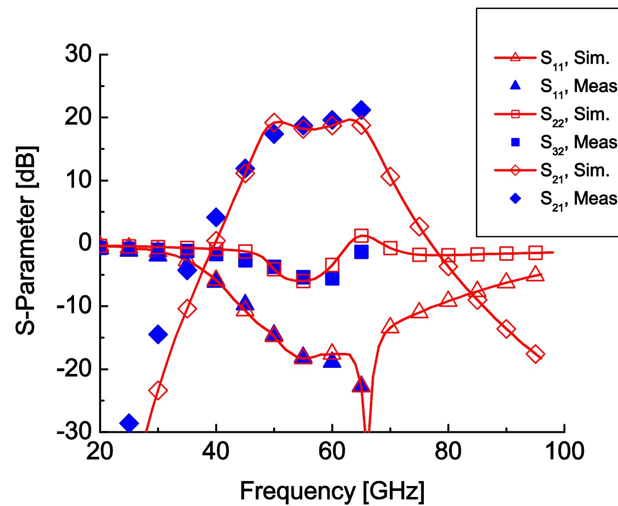
3.2.2.2 Measurement VS. Simulation

Fig. 73a-b present the simulated and measured small signal results of both realized PAs. The PAs have been biased at the 3.3 V collector voltage (V_{CC}) and the 2.6 V reference voltage (V_{ref}). Due to different biasing networks, the collector current (I_{CC}) of each PA is different. The total current consumption of PA_1 is 45 mA (Class AB), while the total current consumption of PA_2 is 55 mA (Class A). Thanks to the accurate small signal transistor model and the EM modeling of the whole chip, the measured and simulated results show a good agreement.

As shown in Fig. 73, broadband input-matching and transducer gain are achieved. An input-matching of better than 10 dB from 51 GHz to 70 GHz for PA_1 and from 47 GHz to above 70 GHz for PA_2 are measured. The peak gain values of both PAs are around 21 dB. Due to different input and inter-stage matching networks, the peak gain varies from 55 GHz in PA_1 to 65 GHz in PA_2. The 3 dB bandwidth is from 50 GHz to 68 GHz in PA_1 and from 52 GHz to 70 GHz in PA_2. More than 5 dB small signal output-matching has been achieved in both PAs, at around 60 GHz. As explained on section 3.2.1.2, this is mainly due to the large signal matching at the output for the maximum OP_{1dB} and PAE.



(a)

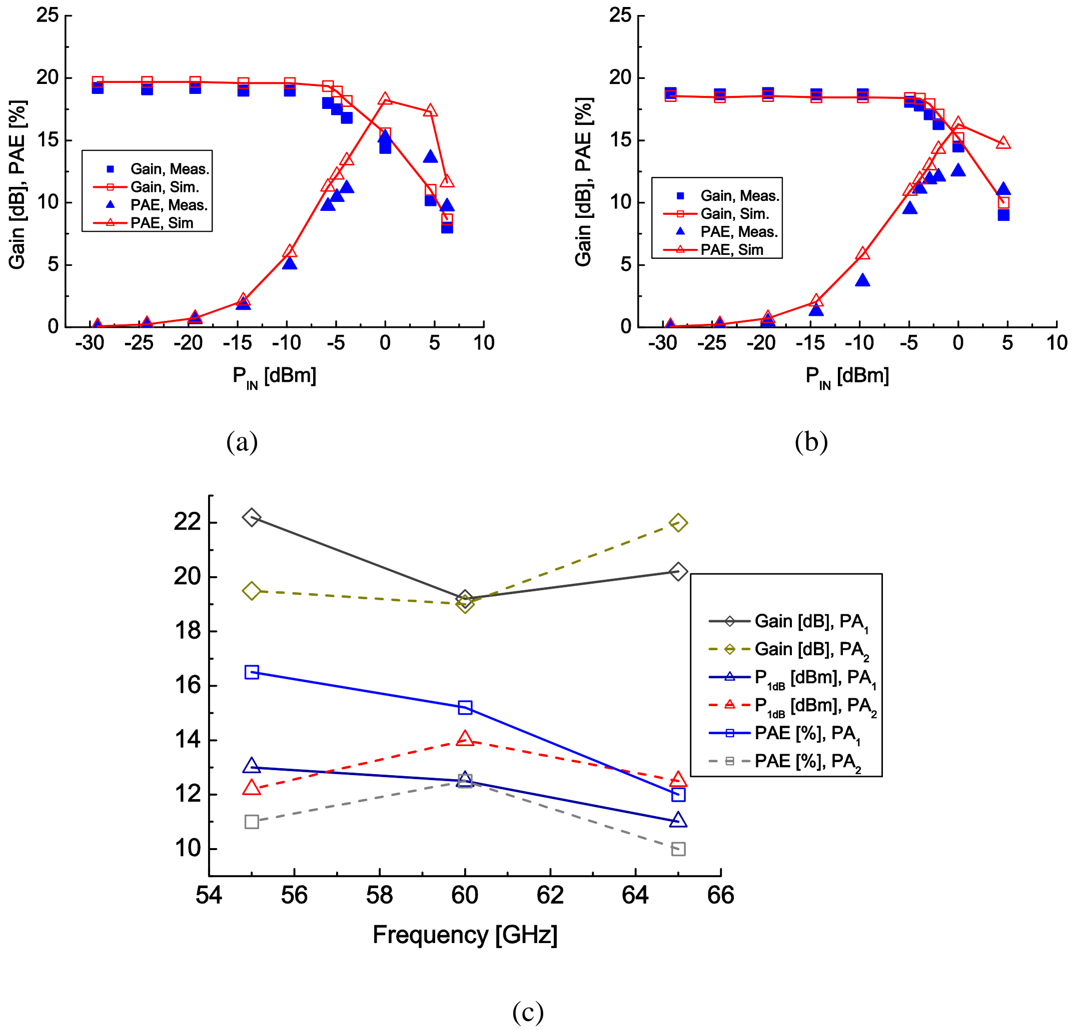


(b)

Fig. 73 S-parameter measurement vs. simulation. a) PA_1. b) PA_2

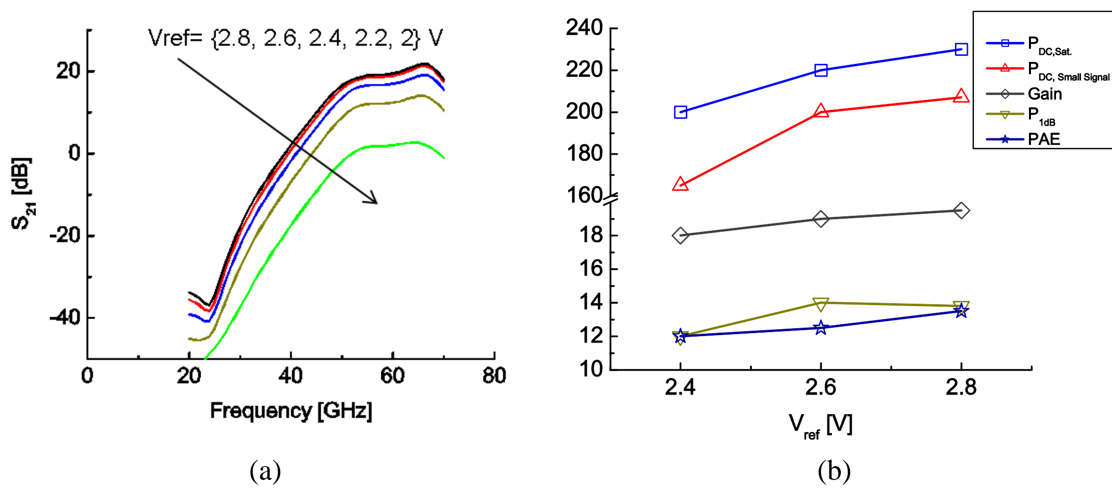
The large signal measurements are performed for both PAs under different biasing conditions and different frequencies. Fig. 74a-b presents the measured results of both PAs at 60 GHz under the same biasing conditions used for the small signal measurements (V_{CC}=3.3 V and V_{ref}=2.6 V). Both PAs have almost the same power gain at 60 GHz (around 20 dB) but, compared to PA_1, the OP_{1dB} of PA_2 is 1.5 dB more. This is mainly due to the higher collector current of PA_2, which on the other hand has resulted in 3% less peak PAE in PA_2 than in PA_1. Furthermore, and for the same reason, PA_1 has slightly better PAE at the back-off.

The large signal performances of both PAs versus frequency are presented in Fig. 74c. An almost constant OP_{1dB} is achieved for both PAs from 55 GHz to 65 GHz. As already mentioned, due to the different biasing conditions, PA_1 shows better PAE than the PA_2 over the targeted frequency band. Moreover, Fig. 75a-b present the small signal and large signal performances of PA_2 versus different bias points, which further proves that 2.6 V V_{ref} is the optimum selection for the current source-biasing voltage.



(c)

Fig. 74 Large signal measurement of both PA_1 and PA_2: a&b) vs. input power at 60 GHz. c) vs. frequency.

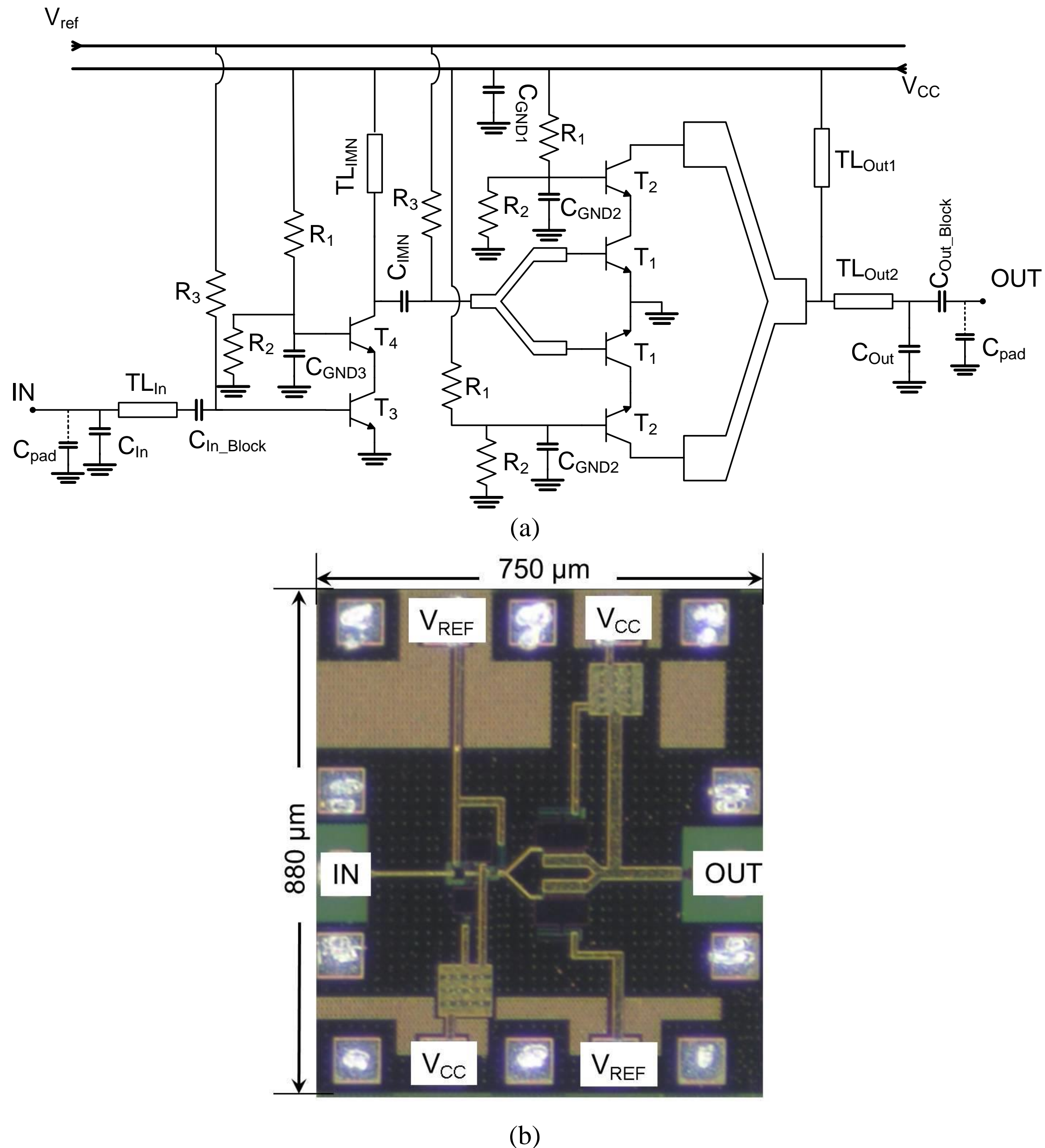


(a) (b)

Fig. 75 PA_2 measurement: a) small signal S_{21}. c) large signal performance.

3.2.3 High Power PA – 1st Version

The third PA is designed for a higher output power in comparison with the previous PAs [16]. In order to improve the output power of this PA, a current-combining technique is utilized [60]. Further, a two-stage amplifier with a cascode topology is selected for better gain, output power and stability (Section 3.1.5). The two-stage PA provides a gain of 17 dB at 64 GHz. The PA is also optimized for biasing circuit, PA Core and matching networks. Because there are certain process variations, narrow band matching designs and unpredicted parasitic and coupling elements, a frequency shift is observed that deteriorated the power performance of the PA. Due to these problems, the PA achieves a maximum OP_{1dB} of 13.8 dBm at around 64 GHz, but the OP_{1dB} nevertheless remains higher than 12 dBm within the entire range of the frequency. The total chip size of the PA is 0.67 mm^2 and the active size of the PA is around 0.3 mm^2.



(a)

(b)

Fig. 76 a) Schematic of the PA. b) Chip-Photo.

Table. 9 The values of the PA components.

Parameter	Value	Parameter	Value
T_1 = T_2 (NoF)	4×6	**C_{In} [fF]**	88
T_3 = T_4 (NoF)	1×6	**C_{In_Block} [fF]**	500
TL_{Out1} [µm] (W/L)	20/280	**C_{IMN} [fF]**	200
TL_{Out2} [µm] (W/L)	20/100	**C_{Out} [fF]**	200
TL_{IMN} [µm] (W/L)	10/180	**C_{Out_Block} [fF]**	500
TL_{In} [µm] (W/L)	3/130	**C_{GND1} [pF]**	16
R_1 [kΩ]	1.5	**C_{GND2} [pF]**	8
R_2 [kΩ]	3	**C_{GND3} [pF]**	4
R_3 [kΩ]	5	**C_{pad} [fF]**	20

3.2.3.1 PA Design

The values of all the components utilized in the PA and the biasing circuits are given in Table. 9. In this design, and unlike the other designs, no current source is utilized and instead the base of the C.E. transistors is directly biased through a resistor (R_3 in Fig. 76a). In this section, the detailed design of each part is explained.

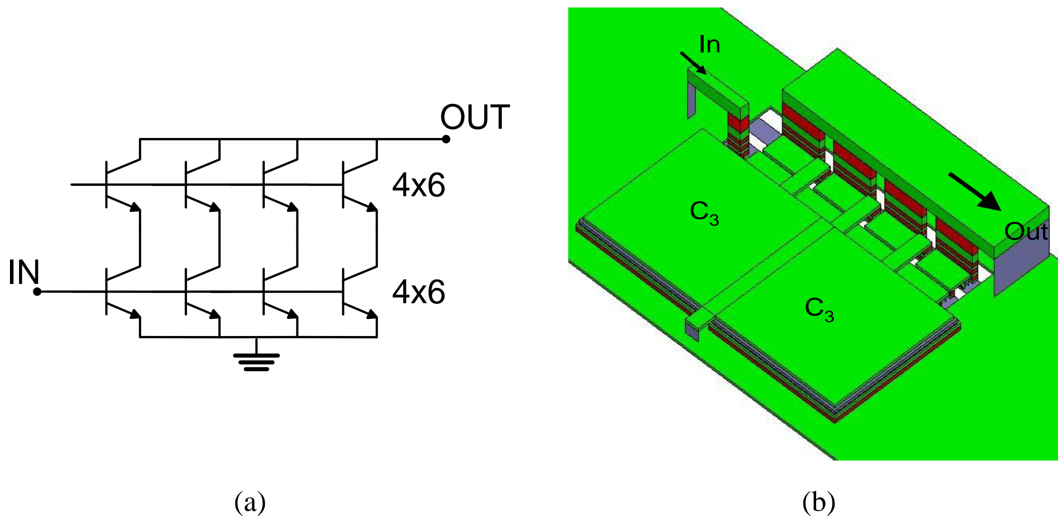
The design of the PA is divided into two parts. In the first part, the power stage and the pre-amplifier core design is investigated, while in the second part the matching network designs are introduced.

a) PA and pre-amplifier cores: In this design, the total PA core is divided into two smaller cores. The size of each core is selected based on the previous discussions (Section 3.1.1 and Section 3.1.2). These cores are current-combined at both their inputs and outputs. Current-combining is a simple technique that can be utilized in on-chip PA designs [60]. In this technique, two completely symmetrical PA cores can be connected to each other with a short but optimized line length. This only requires the same impedances at the terminals of the transistor cores [60]. With this technique, the number of parallel transistors in each PA core will be decreased by half (or even further by three-quarters [60]), which facilitates the power distribution and collection from each transistor.

Unlike the hybrid design, because in the chip design the transistors are all located on one substrate, they show the same characteristics and hence those of their PA cores with the same passive structures have the same output and input impedances. Having the same impedances at the PA core terminals is ideal for the current-combining technique since the isolation compensation (as with the Wilkinson power combiner) between the input ports of the current combiner no longer has an important role in the performance of the total PA. Despite this advantage, the PA cores still cannot be placed too close to one another; such a placement would result in high parasitic and coupling elements between the two and, hence, the deterioration of the output power. The optimum spacing between the two PA cores, in this design, is calculated with the help of EM simulation.

The pre-amplifier transistor size is selected based on the discussion on Section 3.1.2. In the power stage in this PA, two transistor cores are combined, which results in a core size two times larger than the low power PAs (Section 3.2.1.1). In this case, the pre-amplifier NoF must be two times larger. In this design, the NoF of the pre-amplifier core is selected as 12 (2 transistors with 6 NoF for each transistor).

Fig. 77 presents the schematic and the 3D view of each single core in the power stage. The C_3 capacitors in Fig. 77b are the RF ground placed as near as possible to the common base transistors so as to ensure the low ohmic RF ground at this point and, hence, improve the breakdown voltage of the transistors (Section 3.1.5). The complete 3D view of the PA core, including the input and output current combiners, is also presented in Fig. 78.



(a) (b)

Fig. 77 The single core of the PA: a) schematic. b) 3D view.

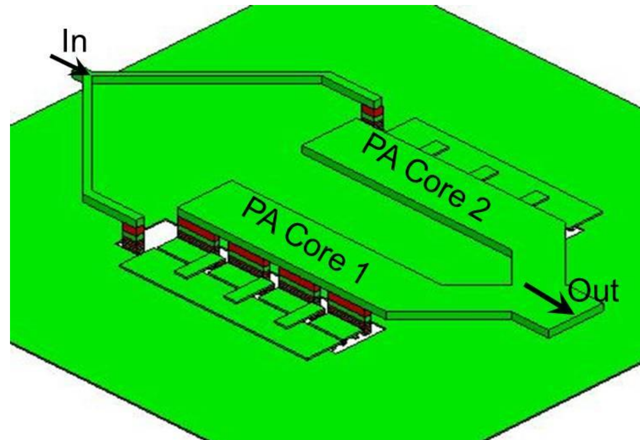


Fig. 78 The two parallel identical transistor cores combined with the current combiner.

b) Matching networks: After finishing the PA core design, the matching network must be added. In this case, the output-matching is designed at the P_{sat} level of the PA with the help of shunt and series inductors and capacitors. Fig. 79 presents the 3D view of the designed output-matching network. The small and large signal load-pull simulated results of the PA output-matching are presented in Fig. 80. As mentioned before (Section 3.2.1.2), matching at the P_{sat} level resulted in the poor small signal output-matching of the PAs. The step-by-step output-matching procedure of the power stage, after the DC feed, is explained in Fig. 81.

Narrow band matching techniques are utilized for the input and inter-stage matching networks. In this design, a series transmission line and a shunt capacitor are used to match the input of the pre-amplifier. The output of the pre-amplifier is directly matched to the input of the power stage with the help of a shunt inductor and a series capacitor.

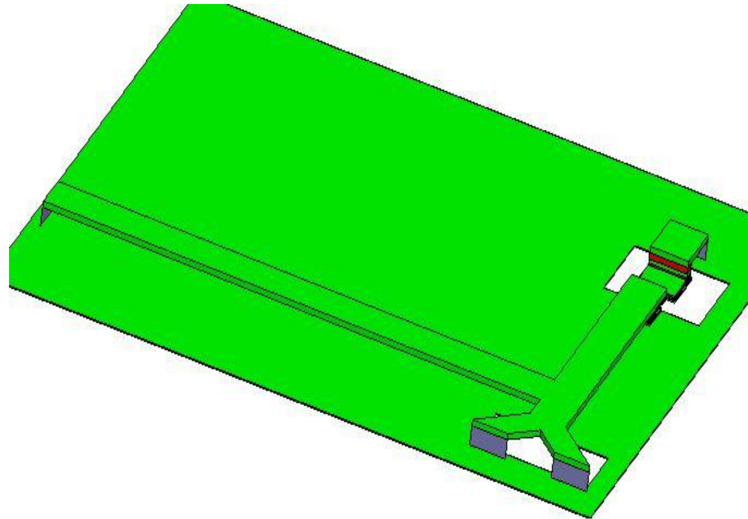


Fig. 79 3D view of the PA output matching network together with the output current combiner.

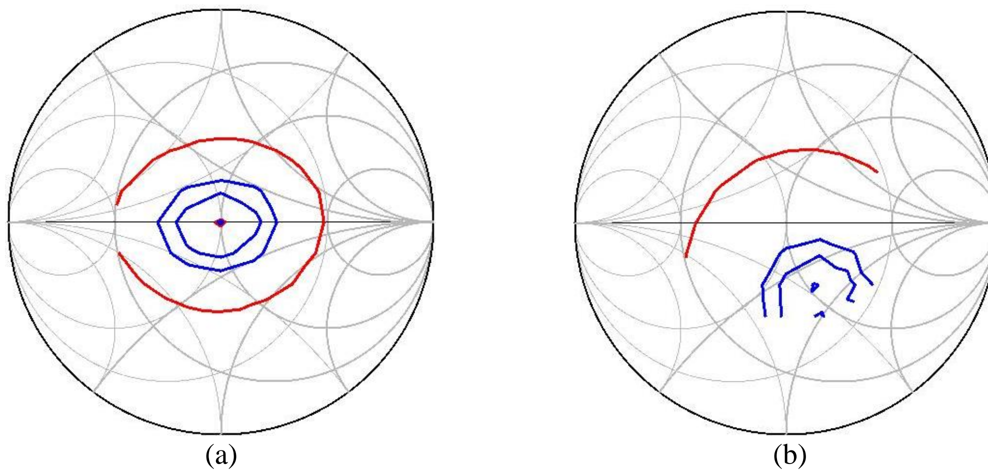


Fig. 80 The load-pull simulations of the PA after matching. a) At P_{sat}. b) At small signal.

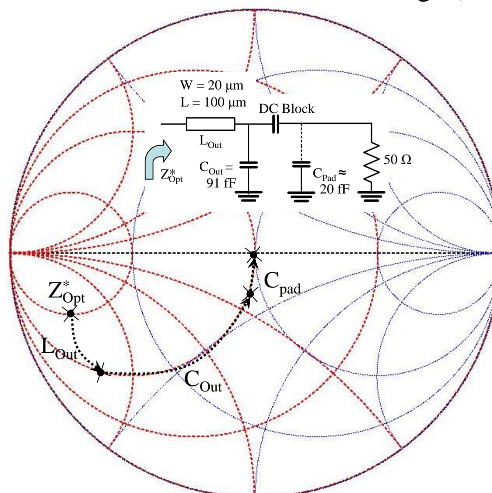


Fig. 81 Output matching steps of the output of PA core and DC feed to 50 Ω.

3.2.3.2 Measurement vs. Simulation

Fig. 82 presents the small signal simulated and measured results. Due to narrow band matching, process variations and unforeseen parasitic and coupling elements, the peak gain is shifted from 60 GHz to 64 GHz. The unforeseen parasitic and coupling elements can mainly be located in the power stage core itself. Further simulations have shown the high sensitivity of the PA performance to the coupling elements between the two PA cores. The measured results show 14 dB gain at 60 GHz and 17 dB gain at 64 GHz. Input-matching of more than 10 dB is achieved, but due to the large signal output-matching (Section 3.2.1.2) the output small signal matching is quite poor, at around 60 GHz.

However, due to the frequency shift, the performance of the PA is deteriorated, though the large signal measured results still show the good power performance of the PA within the frequency band from 60 GHz to 66 GHz (Fig. 83). In this frequency range, an OP_{1dB} higher than 12 dBm is achieved. The PA also achieves an OP_{1dB} of 13.8 dBm at 64 GHz and 13.2 dBm at 60 GHz, with a PAE higher than 6%. These results could be further improved by utilizing a current source instead of resistive biasing, as the measurement showed the collector current to drop at larger signal levels. The large signal performance of the PA at different frequencies is presented in Table. 10.

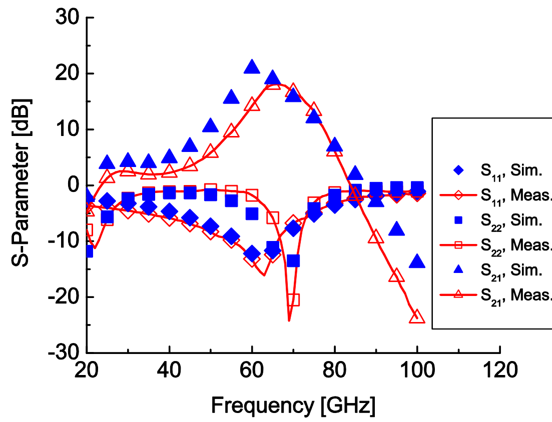


Fig. 82 PA Small signal S-Parameters. Simulation vs. Measurement.

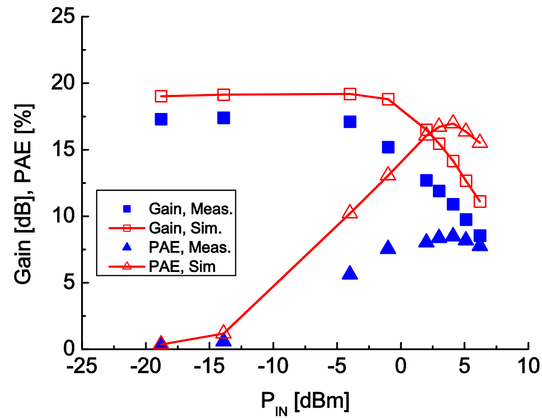


Fig. 83 Measured Gain and PAE vs. input power at 64 GHz.

Table. 10 Measured PA characteristics over the frequency.

Freq. [GHz]	Gain [dB]	OP_{1dB} [dBm]	P_{sat} [dBm]	PAE [%]
60	14.2	13.2	15	6.3
62	16.2	12.3	15	6
64	17	13.8	15	8.5
66	17.1	13.5	15	8

3.2.4 High Power PA – 2nd Version

The previous PA (High Power PA – 1st Version) was redesigned and optimized in this work for higher P_{OUT}, PAE and linearity. In the same way as with the previous PA, a current-combining technique is utilized for the P_{sat} improvement (Section 3.2.3.1). As observed with the previous PA, narrow band matching networks and unforeseen parasitic and coupling elements in the PA core result in a frequency shift in the PA's performance. In this case, extra precautions in the PA core, input and intermediate matching networks are considered for the broadband PA's performance and, hence, less sensitivity of the PA to the process variations.

At 60 GHz, this power amplifier achieves 18 dBm output power and 11 dB gain in saturation with a peak power added efficiency of 14%. The PA is completely integrated, including the matching networks and the biasing circuitry. The total chip area is 0.53 mm^2 and the active area is 0.19 mm^2. The simplified schematic and chip micrograph of the realized PA is shown in Fig. 84.

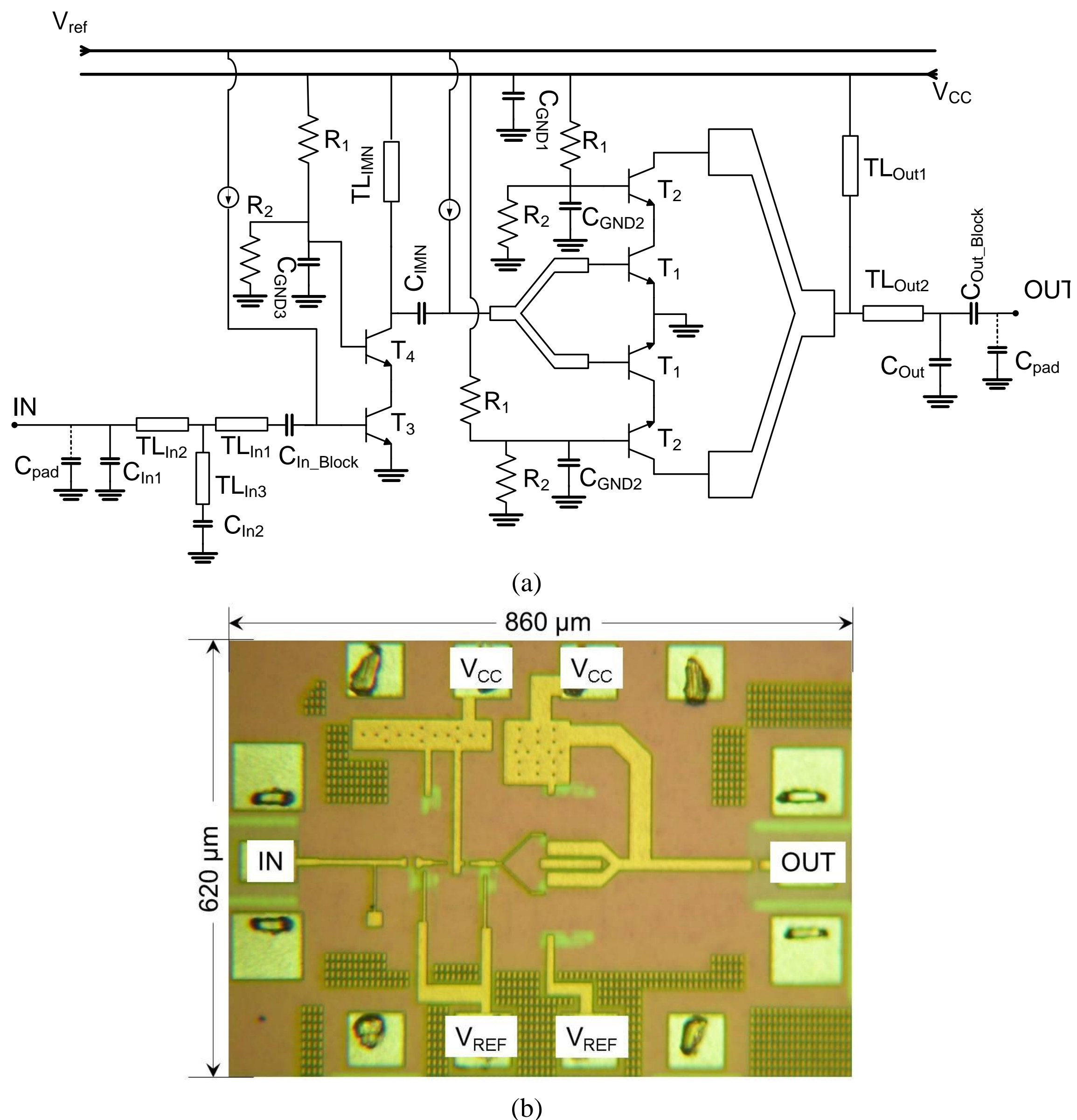


Fig. 84 a) Schematic of the 4th PA. b) Chip-Photo.

Table. 11 The values of the PA components.

Parameter	Value	Parameter	Value
$T_1 = T_2$ (NoF)	4×6	C_{In1} [fF]	70
$T_3 = T_4$ (NoF)	1×6	C_{In2} [fF]	200
TL_{Out1} [µm] (W/L)	20/250	C_{In_Block} [fF]	500
TL_{Out2} [µm] (W/L)	10/130	C_{IMN} [fF]	200
TL_{IMN} [µm] (W/L)	10/160	C_{Out} [fF]	100
TL_{In1} [µm] (W/L)	5/30	C_{Out_Block} [fF]	500
TL_{In2} [µm] (W/L)	5/100	C_{GND1} [pF]	16
TL_{In3} [µm] (W/L)	3/60	C_{GND2} [pF]	8
R_1 [kΩ]	1.5	C_{GND3} [pF]	4
R_2 [kΩ]	3	C_{pad} [fF]	20

Table. 12 The current source elements (Fig. 51a).

Parameter	Value
$T_{S1} = T_{S2} = T_{S3}$ (NoF)	1×1
R_{S1} [Ω]	30
R_{S2} [kΩ]	2
R_{S3} [kΩ]	3.2
R_{S4} [Ω]	500
C_{S1} [pF]	2

3.2.4.1 PA Design

Unlike the first version (High Power PA – 1st Version), in the second version a current source is utilized to improve the power performance of the PA at the large signal levels. The values of all the components utilized in this PA and the biasing circuitries are given in Table. 11 and Table. 12. The schematic of the current source is also given in Fig. 51a. In this section, the detail design of each part is explained.

a) PA and pre-amplifier cores: The PA core design is based on [16] (High Power PA – 1st Version). In the design presented in [16], the PA was matched at the output for maximum linearity. The expected OP_{1dB} of the PA was around 16 dBm. However, a high NoF and unwanted parasitic and coupling elements between the passive structures of the power stage transistor core resulted in less accurate simulated

results and, hence, caused the PA linearity's reduction by 2 dB. In this design, and in order to improve the PA tolerance, an extra shielding ground is placed between the PA cores (Fig. 85). Although this structure results in the lower impedance of the PA core, it improves the PA tolerances by avoiding the inter-core coupling elements.

Similar to the High Power PA – 1st Version, a cascode PA topology with 48 (8x6) fingers and a cascode pre-amplifier topology with 12 (2x6) fingers for both the C.E. and C.B. transistors is selected. The optimum PA core is obtained by the in-phase combining of the transistor fingers (Section 3.1.1) and the utilization of current-combining techniques [60].

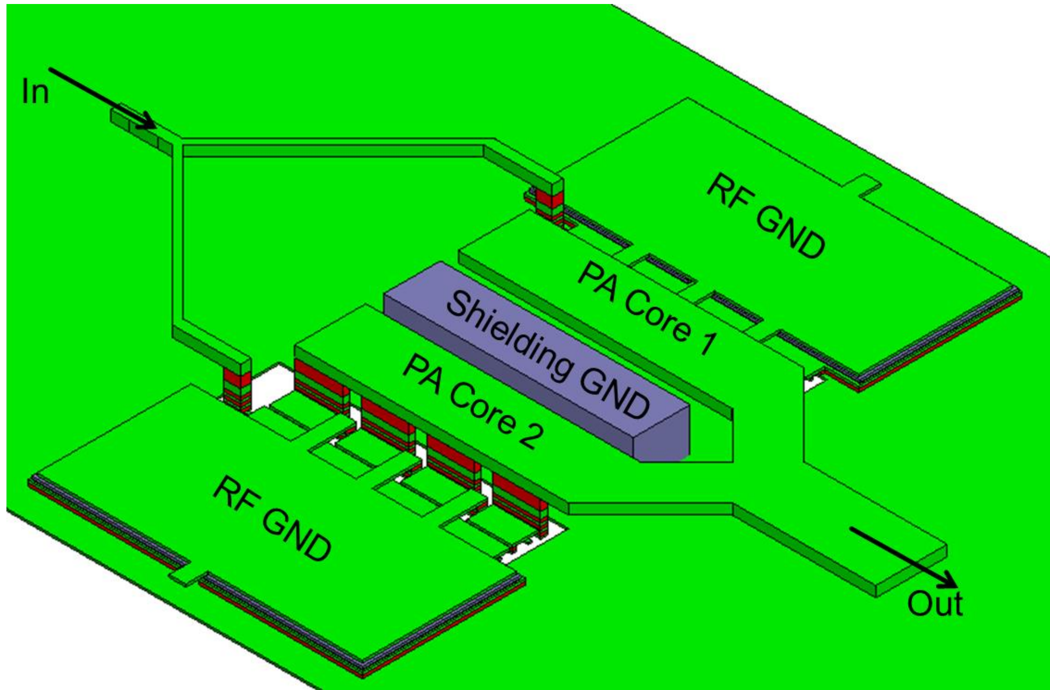


Fig. 85 The 3D view of the transistor Core of the power stage with shielding ground.

b) Matching networks: As mentioned earlier, one of the most important design parameters is the PA optimum output impedance. This impedance varies as a function of the input power. Fig. 86 presents one such variation in the output impedance of the PA. Due to this variation, the amplifier performance is a strong function of the output-matching. This includes the linearity (the OP_{1dB}), the P_{sat}, efficiency and PAE.

The maximum OP_{1dB} can be achieved only for specific impedance on the Smith chart. This impedance specifies an input power for which both gain and output power are high. Matching the output of the transistor for higher or lower input powers would result in the linearity's deterioration. Moreover, due to the small radius of the 1dB contour around the P_{1dB} optimum impedance (Fig. 86), any technology variation or modeling problems can result in the fast deterioration of the OP_{1dB}. Unlike the OP_{1dB}, the P_{sat} is less dependent on the output impedance or the power level at which the output is matched. Shown in Fig. 86 are the simulated gain contours of a PA core (the gain step is 1 dB) for different input power levels. It can be seen that as the input power increases the 1 dB contours become larger, which simplifies the matching tolerances for the P_{sat}.

Although an accurate model is important in designing a high gain and high PAE amplifier, due to the broad contour regions the P_{sat} becomes less dependent upon the transistor large signal model accuracy. A PA matched to the optimum P_{sat}

impedance can achieve a simultaneous high gain, P_{sat} and PAE. In this case, a good approximation of the optimum saturated impedance can be quite helpful in a high performance PA design.

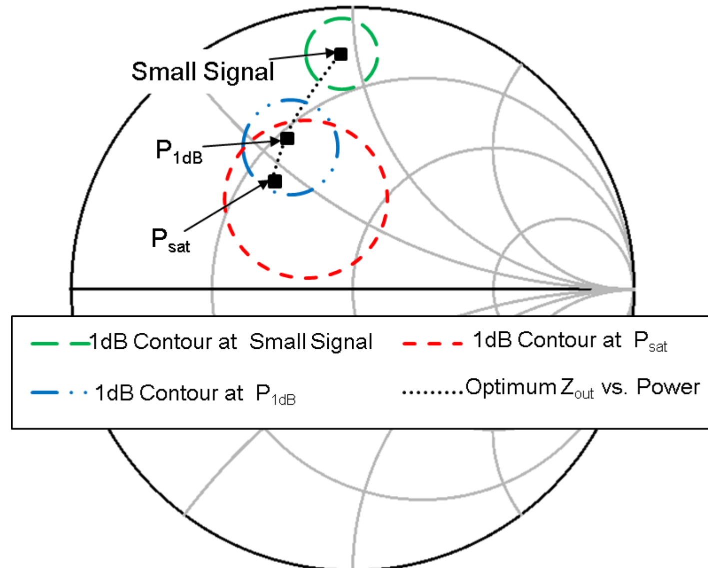


Fig. 86 Simulated optimum output impedance versus input power.

In this design, the approximate optimum P_{sat} impedance of the transistors is estimated. The matching network and all the interconnections are designed with help of EM simulation. As the power gain near P_{sat} is quite low, a pre-amplifier is added. In order to minimize the size of the inter-stage matching network, the output of the pre-amplifier is directly matched to the input of the PA. Further, to minimize the process variation effects on the PA performance, the inter-stage matching network is designed for the broadband performance of the transducer gain (Section 3.1.6).

Fig. 87 presents the methodology applied for the input-matching. A wideband input-matching is designed with the help of shunt-series transmission lines and MIM-capacitors. As shown in Fig. 87 using the presented network, the input reflection can be located within a 10 dB circle for the entire desired frequency band.

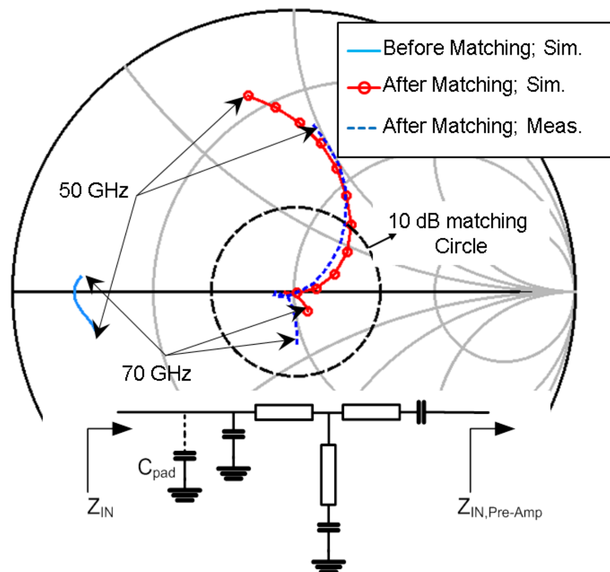


Fig. 87 The broadband input matching.

3.2.4.2 Measurement vs. Simulation

Fig. 88 shows the simulated and measured small signal results of the realized PA. The PA has been biased at 3.3 V with 60 mA of total current consumption. As seen in Fig. 88, although some frequency shift can be observed, due to broadband design and accurate EM modeling of the whole chip, the measured results show a good agreement with the simulation.

Due to the broadband input matching, the input reflection is better than 10 dB from 55 GHz to more than 70 GHz with a value better than 40 dB at 60 GHz. Under the above biasing conditions, the PA has a small signal gain of 16 dB at 60 GHz. The gain increases to 18 dB at 62 GHz. This is mainly due to the large signal matching at the output of the PA at 60 GHz, which helps us to have the highest P_{sat} at the 60 GHz.

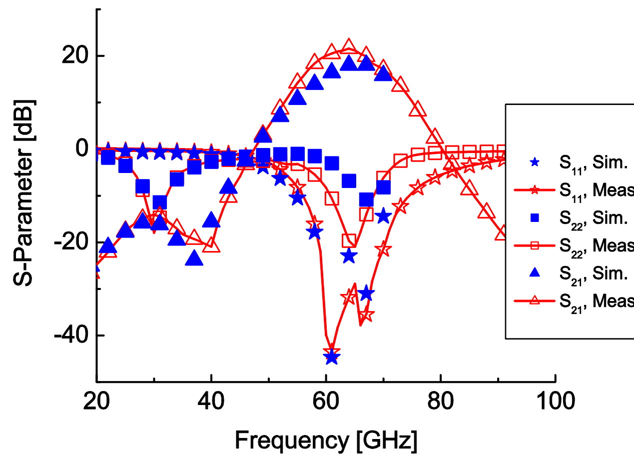


Fig. 88 Measured and simulated small signal performance of the PA biased for class AB.

Biasing points for operations close to class A, class AB and class B have been chosen for large signal measurements. Presented in Fig. 89 is the collector current variation of the PA for all these biasing conditions as a function of the input power. It can be seen that, due to the utilized current source topology, the total collector current increases with the input power. The small signal currents are 60 mA, 100 mA and 130 mA, respectively, for each bias point.

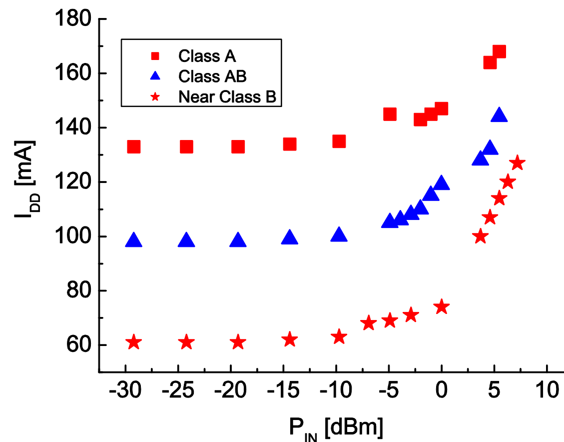


Fig. 89 Measured PA collector current vs. input power at 60 GHz.

Fig. 90a-b and Fig. 91 present the large signal measured results for three operating conditions. As seen in Fig. 91, in the class AB biasing condition the PA has a slightly higher small signal gain (16 dB) in comparison with 15 dB gain of the class B condition. The PA achieves 17.5 dBm output power with 12 dB power gain and 11% PAE under class AB biasing. However, the operation points near class B shows a better P_{sat} (18 dBm) and a higher PAE (14%) with 11 dB power gain.

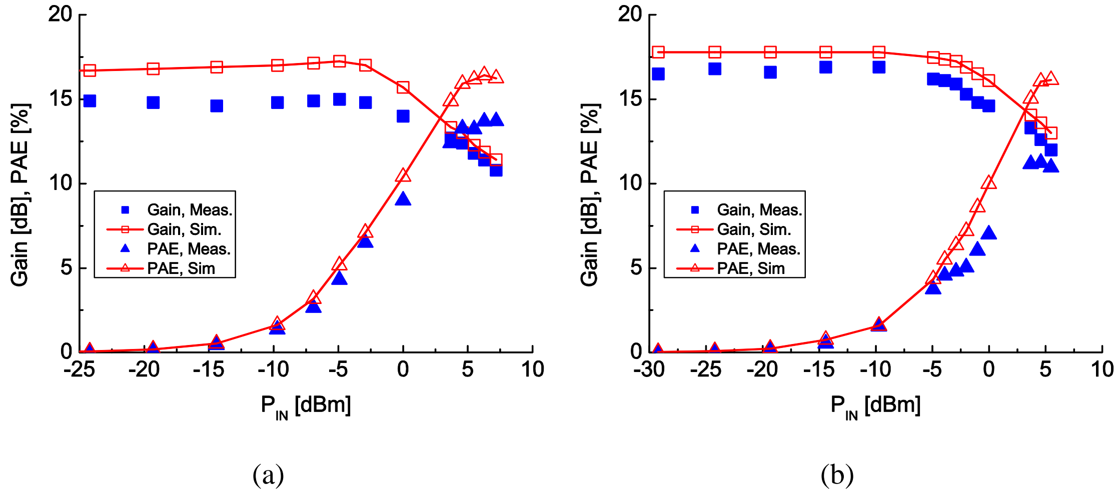


Fig. 90 Measured large signal performance of the PA at 60 GHz.
a) Near class B biasing. b) Class A.

As shown in Fig. 91, the P_{DC} and gain at small signal input power increase by 3 dB from class B to class A. Moreover, as the P_{sat} is constant for all the bias points, the resulted PAE values are lower at higher biasing conditions.

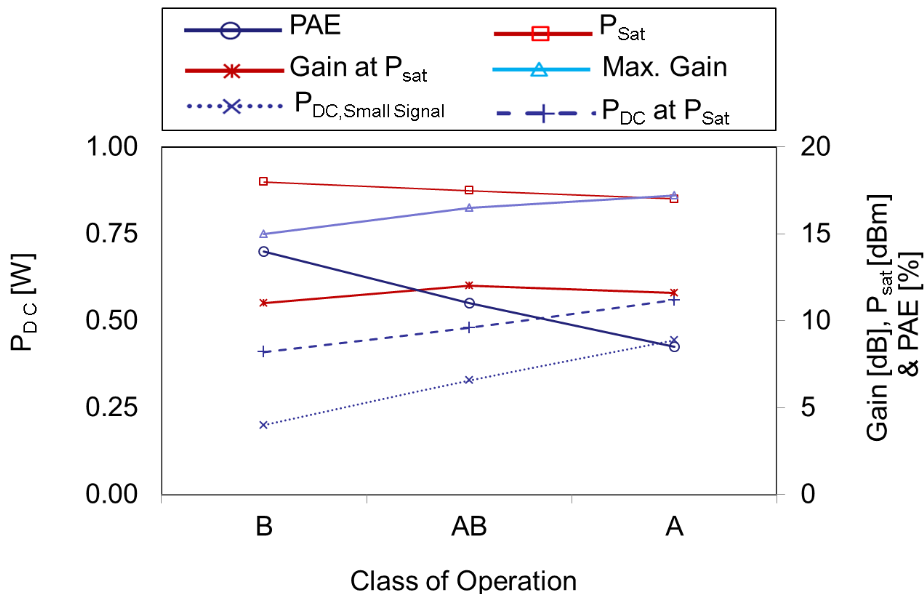


Fig. 91 The PA performance vs. class of operation at 60 GHz.

3.3 Conclusion

In this work, the design of different PAs, based on HBT technology, are studied. Different optimization techniques and design considerations are introduced. For the first PA type, (Low Power PA – 1st Version and 2nd Version) a single PA core without any power combining was utilized. These PAs were designed for simultaneous high OP_{1dB} and PAE. Due to the lower NoF used in the PA core, a better transistor small signal model was obtained at the simulation level and, hence, negligible discrepancies in the small signal level were observed between the simulated and measured results. Further, by performing small signal optimizations, a flat gain was achieved in the Low Power PA – 2nd Version.

At the large signal level, the expected P_{sat} from the simulation was achieved in the measurement, which further justified the utilization of the large signal load- and source-pull simulations and matching techniques. However, unlike the small signal level, and due to the poor large signal model of the transistors, the small 1dB gain contour around the OP_{1dB} (Fig. 86), and the process variations, the prediction of the correct impedance for simultaneous maximum OP_{1dB} and PAE faced certain difficulties. The inability of the correct impedance extraction from the simulation level for the maximum PAE resulted in the P_{sat} occurrence for higher P_{DC}s, which resulted in around 4% lower PAE in comparison with the state-of-the-art results for the same output power. Despite this problem, the designed PAs achieved more than 20 dB Gain, 14 dBm OP_{1dB}, 15 dBm P_{sat} and 14% PAE with broadband performance covering the entire V-band and a less than 0.2 mm^2 active chip size.

With the second design type (High Power PA – 1st Version and 2nd Version), simultaneous maximum P_{sat} and PAE were targeted. In addition, in these designs and in order to improve the output power of the PA, a current-combining technique was utilized [60]. With this technique, a 3 dB output power boost was targeted.

Unlike the previous version, the larger size of the PA core, the lower impedance and higher number of coupling elements between the transistors, resulted in a poorer small signal model of the PA core and, hence, a larger deviation was observed in the small signal level in comparison with the previous PAs. By utilizing broadband design techniques for the High Power PA – 2nd Version, the effect of the small signal deviations on the large signal performance of the PA was eased and, therefore, the discrepancies between the simulated and measured results were minimized.

Further, the use of the resistive biasing in the High Power PA – 1st Version has shown large signal performance deterioration. This is mainly due to the collector current decrease in the PA by the increase in input power. In the High Power PA – 2nd Version the presented current source (Section 3.1.3) was utilized. The observed measured results verified the functionality of this current source (Fig. 89).

At the large signal level, these PAs were matched at the saturation level for simultaneous maximum P_{sat} and PAE (in comparison with the OP_{1dB} in the previous PAs). This is mainly due to the much larger 1dB contour around the P_{sat} in comparison with the OP_{1dB}. With these techniques, the designed PAs achieved 18 dBm P_{sat}, 14% PAE and 16 dB gain with around 0.19 mm^2 active chip size.

Furthermore, a survey of the (currently) state-of-the-art publications (at 60 GHz and 77 GHz) shows an almost linear relationship between the P_{sat} and PAE of the PAs. It can also be seen that the PAE decreases as the P_{sat} increases (Fig. 92), and vice versa. For 60 GHz PAs, the PAE decreases from 20% at 15 dBm [35] to 6.3% at

23 dBm (differential) [39]. By placing this PA (High Power PA – 2nd Version) on this plot, the credibility of this design technique can be proven. Table. 13 compares these PAs with the other published PAs. In this table, the PAs are sorted based on their operating frequency and output power.

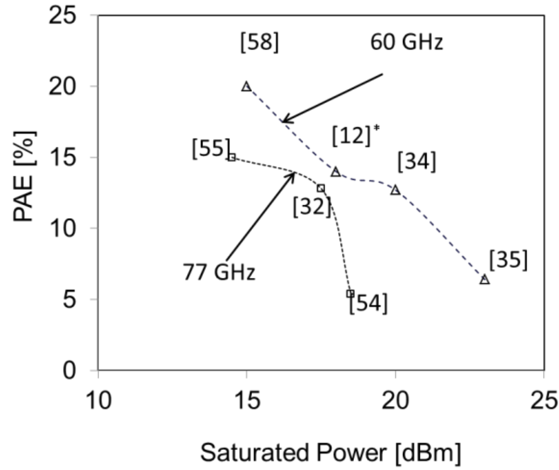


Fig. 92 PAE vs. P_{sat} for the state-of-the-art PAs and High Power PA – 2nd Version
* High Power PA – 2nd Version

Table. 13 Comparison of our work with previously published PAs

Ref.	Freq. [GHz]	Mode[2]	S_{21}[3] [dB]	3 dB BW[4] [GHz]	OP_{1dB} [dB]	P_{sat} [dBm]	PAE [%]	V_{CC} [V]	Total Size [mm^2]
[15]	60	Single	8.6	51 - 69	12	14	9.2	3.3	0.36
[11]	60	Single	20	50 – 68	12.5	15	15	3.3	0.41
[11]	60	Single	19.5	52 – 70	14	15	12	3.3	0.42
[16]	60	Single	14.2	58 - 70	13.2	15	6.3	3.3	0.67
[62]	60	Bal.	11.5	–	11.2	15.8	16.8	–	–
[61]	60	Diff.	31	–	12	17.4	9.2	4	0.5
[12]	60	Single	16.5	59 – 70	13.2	17.5	11	3.3	0.53
[61]	60	Diff.	31.7	–	13.6	17.9	7.5	4	0.5
[12]	60	Single	15	59 – 70	14	18	14	3.3	0.53
[38]	60	Diff.	18	58 – 65	13	20	12.7	4	0.98
[39]	60	Diff.	20	–	–	23	6.3	4	3.42
[35]	61	Single	18.8	–	14.5	15	20	3.3	0.8
[16]	64	Single	17	58 - 70	13.8	15	8.5	3.3	0.67
[38]	64	Diff.	19.5	58 – 65	10.5	18	8	4	0.98
[61]	66	Diff.	21.4	–	15.5	18.4	11.5	4	0.5
[59]	66	Diff.	22.8	–	17.1	19.1	10.2	4	0.5
[61]	77	Diff.	–	–	–	18.5	5.4	–	–
[58]	77	Single	–	–	14.5	14.5	15.7	–	0.15
[36]	77	Single	17	–	10.2	17.5	12.8	–	0.61

[1] Single ended, differential and balanced mode of operation
[2] The small-signal gain
[3] Bandwidth

4 CMOS PAs

In this chapter, the design, realization and measurement of different PAs on the low power bulk 90 nm CMOS technology are studied. In the same way as with the HBT PA design, firstly, to select the optimum transistor size, biasing voltages and topology, many PA design considerations are investigated. In the first section of this chapter, these design considerations are introduced. In the second section, the designed and realized PAs are demonstrated with a comparison of their simulated and measured results. Finally, the third sections conclude this chapter.

4.1 CMOS PA Design and Considerations

As explained in the previous chapter, many considerations must be taken into account for the mm-wave HBT PA's design. Some of these considerations are common between CMOS and HBT PA design procedures, including pre-amplifier transistor size selection, the broadband design and load- and source-pull simulation setups. Despite these similarities in the design procedure, due to intrinsic differences between the CMOS and HBT transistors, some considerations cannot be the same. Among these considerations, the power stage transistor size and the PA topology selection are the most prominent ones.

In this section, each of these two considerations is studied in detail and their results are used in the design of the desired PAs.

4.1.1 Transistor Size Selection

In order to design a power amplifier, it is important to select the correct transistor size, which requires the selection of the optimum values for their length, width and NoF. Usually, the length of the transistors can be selected as small as possible so as to achieve the maximum f_t and f_{max}. However, selection of the width and the NoF can depend upon many different factors, including:

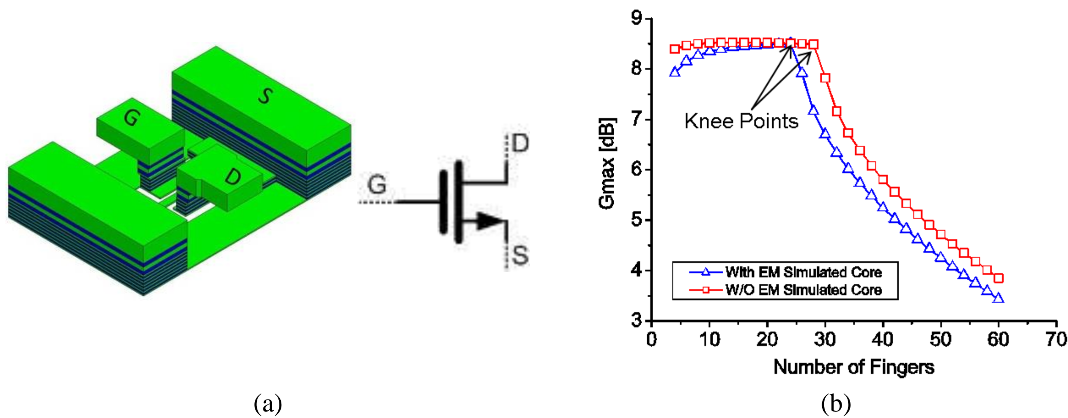
- Transistor core
- Output power
- PAE
- Gain
- Stability
- Input and output impedances

In this section, the effect of the parasitic elements of the PA core on the RF performance of the transistors is studied. Further, the relation between transistor size and the large and small signal performance of the transistor is investigated. Moreover, the optimum transistor size for a low loss matching network design is determined. Finally, an optimum range for the transistor width and the NoF is suggested.

4.1.1.1 Transistor Core

Although, the transistor core is among the smallest parts of the PA, the parasitic elements of its passive structure can have a massive effect on the performance of the PA. This is mainly due to the low impedance of large PA transistors (usually around 10 Ω or less in a 90 nm CMOS), which can be easily affected by the intrinsic parasitic elements of the PA core, especially at higher frequencies [15].

Adding the EM simulated core (Fig. 93a) to the simulation usually results in a higher stability factor, which means a lower knee frequency point (the point where the stability factor becomes more than 1) for G_{MAX}. Fig. 93 compares the MSG at 60 GHz with and without the EM simulated core for different transistor widths. Fig. 93b shows that by adding the EM simulated core, G_{MAX} sharply drops for transistor sizes above 75 µm while without the core G_{MAX} remains constant up to 90 µm.



(a) (b)

Fig. 93 a) HFSS 3D view of the transistor core. b) Simulated maximum stable gain with and without EM simulated core for 3 µm finger width (W) at 60 GHz and V_{DD} = 1.2 V.

4.1.1.2 RF Performances

The RF performance of the transistor can be divided into two main categories of large and small signal characteristics. These transistor performances are a function of different parameters, such as f_t, f_{max}, G_{MAX}, stability and breakdown voltage. These parameters can be modified by the intrinsic and extrinsic parameters of the transistors:

- Intrinsic:
  - Channel length
  - Substrate conductivity
  - Electron mobility
  - Transistor technology (e.g. CMOS, Bipolar, LDMOS, etc.)
- Extrinsic:
  - Transistor size
  - Biasing conditions

Although the intrinsic parameters have a more prominent effect on the transistor performance, the large and small signal performances can also be modified by extrinsic parameters. For example, f_t and f_{max} deteriorate with increasing the transistor size and they usually show the peak value for a specific biasing condition.

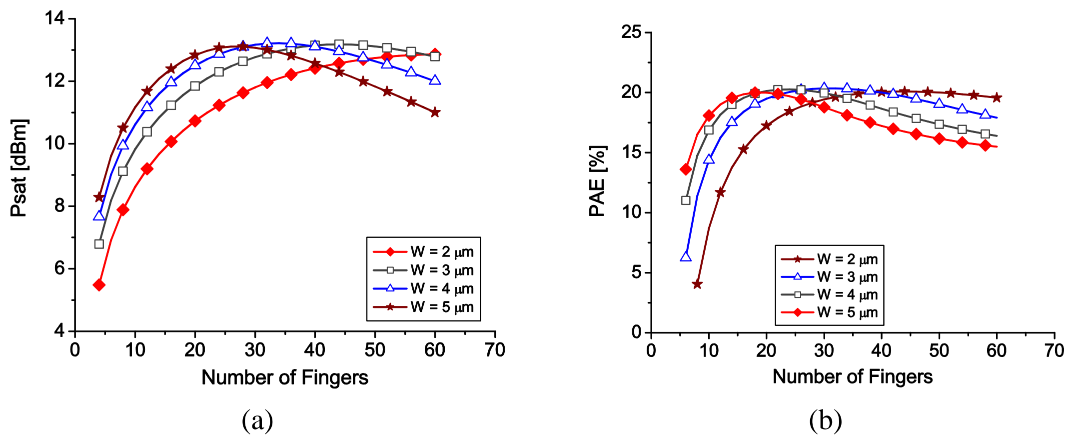
On the other hand, the power capability increases with increasing the transistor size and drain current density, which will also be limited by the parasitic elements of the larger transistors and their electron mobility. Finally, G_{MAX} is a function of f_t and f_{max}, the frequency of operation and the RF power level at which the transistor is operating.

In the PA design, and depending upon the required output power and gain, different combinations of the above mentioned parameters could serve as the optimum selection. For example, during power stage design, high P_{OUT} and average gain are the main requirements. Based on these requirements, larger transistor sizes and higher current densities can be selected. In contrast with the power stage, for the pre-amplifier stage a high gain and a medium or low P_{OUT} are required. In this case, smaller transistor sizes and lower current densities can be selected.

In this section, the detailed large and small signal characteristics of the 90 nm CMOS transistor (provided by TSMC foundry) are studied. Based on this study, a range of transistor sizes for high gain, P_{OUT}, and PAE are introduced.

4.1.1.2.1 Large Signal Performance

The most important characteristics of PA are P_{OUT} and PAE. In an ideal case, by increasing the transistor size the P_{OUT} increases linearly while the PAE remains constant. However, this is not the case in reality. Fig. 94 presents the P_{sat} and PAE of a single transistor with the EM-simulated core for different sizes (W and NoF). To calculate the maximum P_{sat} and PAE, the transistor is terminated in each case with its optimum input and output impedances (determined by load- and source-pull simulations). As shown, P_{sat} decreases for total transistor widths of more than 120 µm (Fig. 94a) while PAE decreases for a total transistor width of more than 100 µm (Fig. 94b). Table. 14 and Table. 15 present the different combinations of NoF and W with which the maximum P_{sat} and PAE can be achieved.



(a) (b)

Fig. 94 Large signal simulations for various W and NoF @ 60 GHz for V_g = 1 V and V_{DD} = 1.2 V. a) P_{sat}. b) PAE.

Table. 14 NoF and finger width (W) for maximum PAE (Simulation)

W	NoF	PAE max
2 µm	44	20.5%
3 µm	32	21.5%
4 µm	24	21%
5 µm	18	20

Table. 15 NoF and finger width (W) for maximum P_{sat} (Simulation)

W	NoF	P_{sat}
2 µm	60	13 dBm
3 µm	44	13 dBm
4 µm	34	13 dBm
5 µm	26	13 dBm

4.1.1.2.2 Small Signal Performance

As the P_{OUT} of the mixers and modulators are often quite low, high gain PAs are required to be able to drive the output of the PA into P_{sat} or up to the P_{1dB} level. The gain of the PA can be increased by increasing the number of the amplifier stages and optimizing the transistor size and current density. Increasing the number of stages can result in a larger PA chip size, but it eases the complexity of the PA design, which is mainly due to the lower gain requirement from the power stage. On the other hand, the optimum transistor size and current density selection can decrease the number of stages and minimize the chip size. It should be noticed that the transistor gain is limited by G_{MAX} (dependent upon the technology) and also that this optimization may result in poorer power performance. In this case, by enabling a tradeoff between the power stage performance and number of pre-amplifier stages, the transistors of the power stage can be selected for medium gain and high P_{OUT}, while the transistors of the pre-amplifiers can be optimized for maximum gain and moderate P_{OUT}.

To find the optimum condition, the G_{MAX} of the transistor at 60 GHz is plotted (Fig. 95) for various total widths and current densities. Within this plot, the single finger width of the transistor is 3 µm and the total width of the transistor is varied by changing the NoF. The blue dashed line indicates a stability factor less than or equal to one. All the points below the blue dashed line have a stability factor of more than one. Furthermore, by increasing the current density of the transistor, the stability factor increases. This can result in a knee-point condition (Fig. 95) in the G_{MAX} plot, where the gain drops rapidly. Based on the discussion in [74], the G_{MAX} value for stability factors higher or lower than one can be calculated as follows:

$$G_{MAX} = |S_{21}/S_{12}| \quad (17)$$

$$G_{MAX} = |S_{21}/S_{12}| \times \left(k - \sqrt{(K^2 - 1)}\right) \quad (18)$$

For stability factor of less than one, G_{MAX} can be calculated from (17). As the stability factor becomes more than one, a new pole appears (18), which results in a rapid decrease in the G_{MAX} value.

Based on Fig. 95, for a stability factor close to one (the blue dashed line) and for current densities of more than 100 µA/µm (where the transistor reaches the saturation), a flat G_{MAX} - around 8 dB for this technology - can be achieved at 60 GHz. In this case, and for the better power gain performance of the amplifier, the transistor size and current density can be selected for stability factors close to one. It should be considered that, due to low quality factor of the passive structures, by adding the matching network the stability factor will further increase. Finally, as

shown in Fig. 95 for G_{MAX} better than 7 dB and current densities higher than 100 µA/µm, a total transistor width of less than 90 µm should be selected.

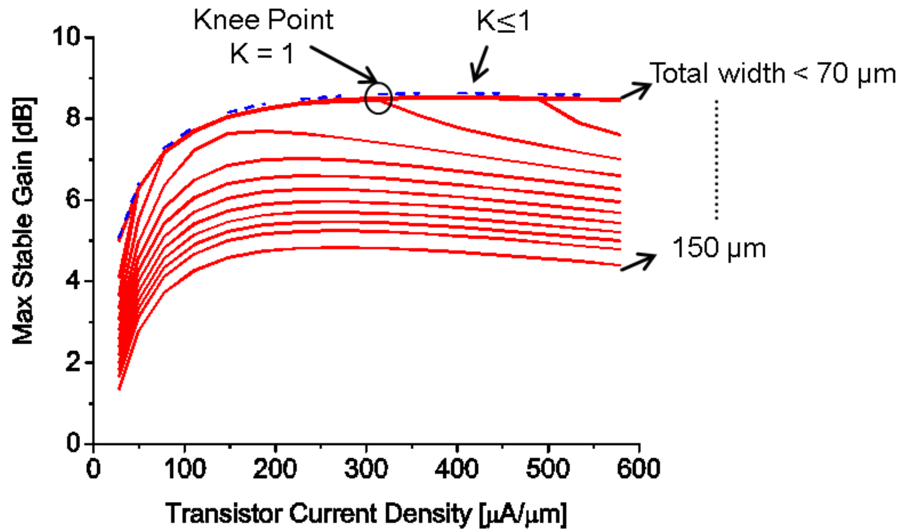
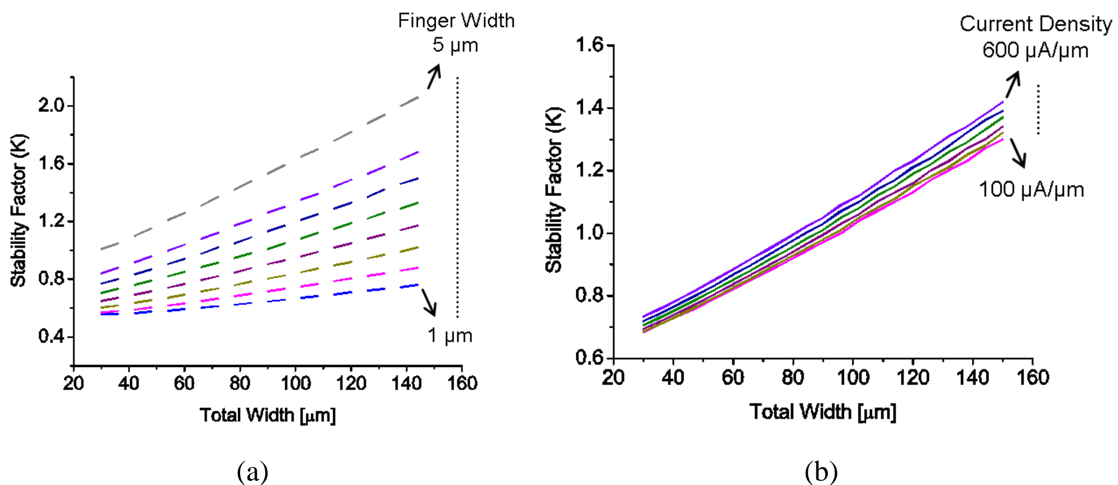


Fig. 95 Simulated G_{MAX} vs. transistor size and current density at 60 GHz for W= 3 µm for each transistor finger and V_{DD} = 1.2 V.

As is already known, the total width of the transistor is a function of finger width and the NoF, but the series gate resistance has a direct relation with the finger width and an indirect relation with the NoF. By increasing the finger width, the series resistance of each finger increases, which results in higher stability factors. Fig. 96a presents the stability factor versus the total width of the transistor for various finger widths. As can be seen, the stability factor is quite sensitive to the finger width.

Unlike the stability factor sensitivity to the NoF (Fig. 95) and finger width (Fig. 96a) of the transistor, the CMOS transistor shows less sensitivity in its stability to the current density. As shown in Fig. 96b, at a single total width, the stability factor varies by less than 10% from 100 µA/µm up to 600 µA/µm current densities.

Based on the discussion in this section and the previous section, and depending upon the required P_{OUT}, the correct transistor size and current density can be selected for the maximum PAE and gain.



(a) (b)

Fig. 96 Stability factor vs. the total transistor width, a) finger width for 200 µA/µm current density. b) Current density for 3 µm total width.

4.1.1.3 Transistor Size vs. Matching Network

The power performance of the PA is a function of the transistor size and the quality factor of the matching networks. In order to realize high quality factor-matching networks on-chip with low substrate resistivity, a precisely modeled passive component with shielding structures is required. However, this may not be enough for the matching of very low impedance transistors. Low impedance transistors (large width) require more than a one-stage matching network for high quality factor design [74]. The complexity of this matching network, especially of mm-wave frequencies, can result in further quality factor deterioration and also in discrepancies between simulation and measurement due to unseen parasitic and coupling elements in simulation. Fig. 97 presents the transistor input and output impedances for various transistor widths. For these terminal impedances, the transistor can deliver the maximum output power. With this technology, and in order to achieve a less complicated matching network, especially at the output of the PA the transistor sizes around 40 µm to 50 µm can be selected.

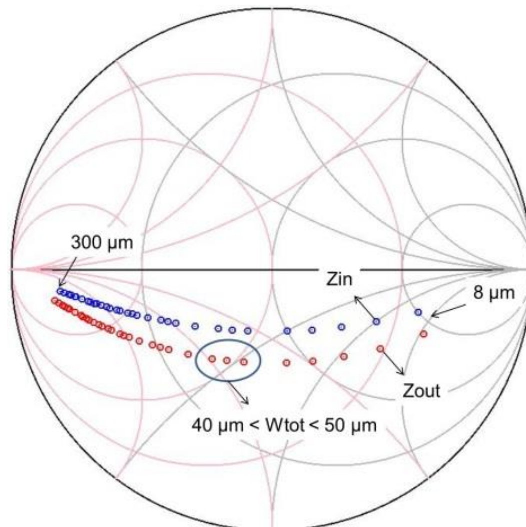


Fig. 97 Simulated optimum input and output impedance at 60 GHz and VDD = 1.2 V.

4.1.2 Topology

C.S. and cascode topologies are the two common topologies utilized in the PA design. The cascode topology provides a better isolation between output and input ports, which will improve the stability of the circuit and facilitate the matching network design. In addition, the cascode topology can have a higher power gain than the C.S. topology as, for the same current gain, the cascode topology provides a higher output impedance (dependent upon the technology) and, hence, a higher power gain. In HBT technology, the cascode topology can provide higher output power (two times or higher) as the base of the common base transistor is connected to a very low ohmic RF ground (Section 3.1.3). The increase in output power is mainly due to the nature of the breakdown voltage in bipolar transistors, which varies by the base impedance [53]. Unlike the HBTs, in the two-well CMOS technology the cascode topology does not help in improving the breakdown voltage and, hence, the output power. In this case, to increase the drain voltage (more than 1.2 V), the triple well CMOS transistors are necessary, though this introduces more parasitic elements and can deteriorate the transistor performance.

By having the drain voltage fixed at 1.2 V, the C.S. topology can deliver a higher voltage swing (Fig. 98) at the output and thus a higher output power than the cascode topology. Due to these issues, the C.S. topology has been selected for our designs.

(a) (b)

Fig. 98 The maximum voltage swing a) C.S. b) Cascade.

4.1.3 Conclusion

In this section, various considerations for the 90 nm Si CMOS PA design are investigated. These investigations have been divided into two parts, namely the transistor size and the topology of the PA selections. In the first part of these investigations, the importance of the transistor passive core in simulation was shown and the large and small signal behavior of the transistor and the matching network restrictions were studied. Based upon these studies, different transistor sizes were selected for optimum large and small performances and the optimum matching network design.

In this case, for optimum large signal performances, the optimum transistor size for the maximum PAE is around 95 µm (Table. 14), while for maximum P_{sat} transistor sizes of more than 115 µm (Table. 15) can be selected. In the small signal investigation, transistor sizes of less than 90 µm display G_{MAX} better than 7 dB. Finally, for the optimum matching network design (to 50 Ω terminal impedance), the transistor sizes between 40 µm and 50 µm are the most appropriate. In this case, and based upon the PA requirements, a tradeoff between the large and small signal performances and matching network complexity must be made.

Further, different topologies (C.S. and cascode) were investigated for this technology. It has been shown that, by using a two-well transistor technology, the maximum V_{DD} cannot be increased to more than 1.2 V in either of the topologies and, hence, the C.S. topology shows a better output power in comparison with the cascode topology.

4.2 Realized V-Band Si CMOS Power Amplifiers

In this section, two different V-band CMOS power amplifiers are presented. The two PAs are designed, realized and measured. The PAs are designed to satisfy the system requirements (defined in Section 5.1.1).

In order to achieve a higher output power, different power combining techniques must be applied. The most common techniques for the mm-wave CMOS technologies are Wilkinson power combining [78], transformer-based PAs [81] and distributed active transformers [84]. In this section, first, the two power combining techniques are studied and two PAs based on these techniques are realized.

4.2.1 Wilkinson CMOS Power Amplifier

In this work, a fully integrated 60 GHz two-stage power amplifier for high data-rate wireless communication is presented [8]. All the matching networks are designed on the top metal layers with SCTL structures [7]. The two-stage C.S. PA was optimized for high P_{OUT}, gain and PAE. These goals were achieved through source- and load-pull simulations and optimum transistor size selection.

The transistor sizes were selected based on the discussions in section 4.1.1 and section 5.1.1. Based on the discussion in section 5.1.1, around 10 dBm P_{OUT} is required. Moreover, as shown on section 4.1.1, this power is only 2 dB less than the maximum achievable P_{OUT} from the single transistor. This means that a large transistor size is required and, hence, that the PA-matching with this transistor size might result in poor gain performance and a complicated matching network. To ease the requirement on the PA design, a power combining technique is utilized to decrease the required P_{OUT} from each individual PA.

Moreover, in order to be able to use larger transistor sizes for higher P_{OUT} performance, the output and input impedances of the PA are matched to 16 Ω instead of 50 Ω. This technique allows the use of larger transistor sizes with simpler matching networks with higher quality factors. The 16 Ω impedance is later transformed to 50 Ω impedance at the output.

Further, the Wilkinson power combining technique is utilized in the design for P_{OUT} enhancement. Utilizing GCTL and SCTL structures (Section 2.3.2 and **[7]**) for the Wilkinson combiner's design resulted in low combining losses. Moreover, the Wilkinson power combiner was used as a part of input- and output-matching networks to match the 16 Ω at the terminals of the PA to 50 Ω at the input and the output. The simplified block diagram of the complete power amplifier is presented in Fig. 99.

Using a C.S. topology (Section 4.1.1) and power combining, the PA achieved 11 dBm P_{sat}, 9 dBm OP_{1dB} and more than 8 dB small signal gain with a peak PAE of 6%. The broadband performance of the gain was achieved utilizing the cascaded structure [11]. The detailed design procedure and the achieved measurement results are presented in this section.

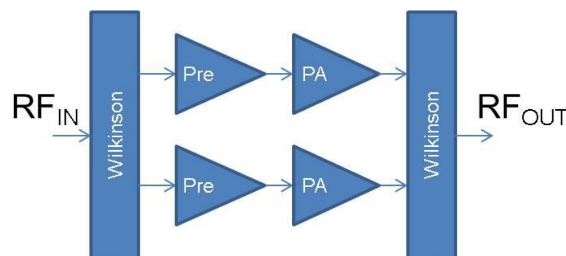


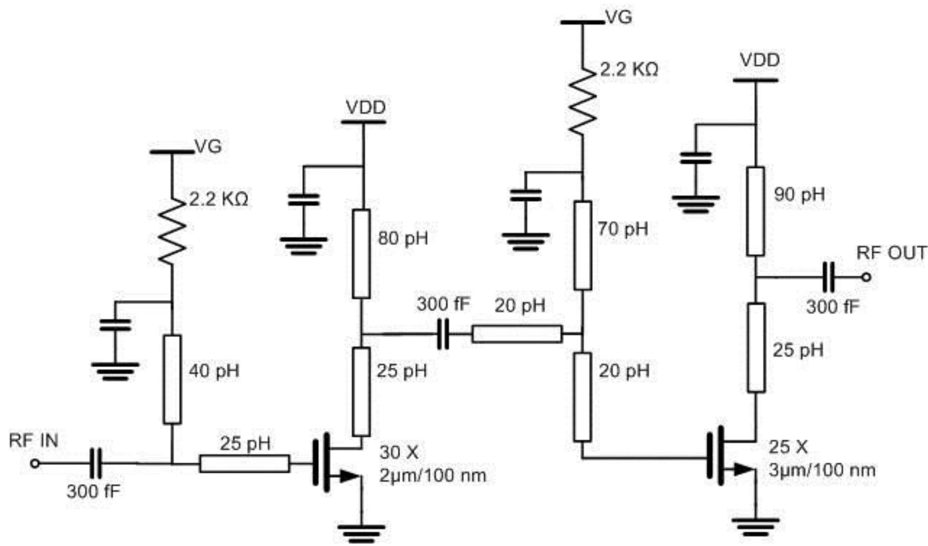
Fig. 99 The PA block diagram.

4.2.1.1 Power Amplifier Design

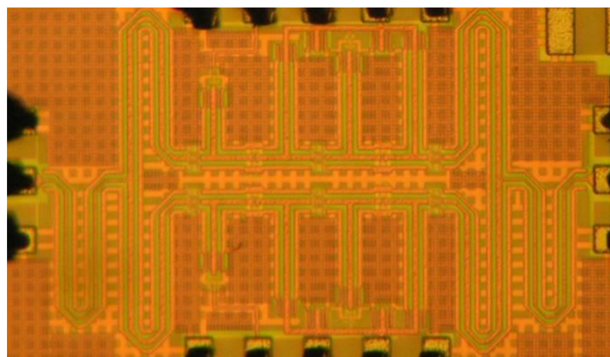
The schematic of the realized PA is shown in Fig. 100a. The designed PA is matched at the output for the maximum linearity to 16 Ω with the help of load-pull simulation. Moreover, the size of the PA transistors was selected based on the discussion in section 4.1.1.1 for the optimum matching to 16 Ω and maximum power performance. The input-matching network is designed for broadband performance in order to cover the entire required band around 60 GHz. In addition, the inter-stage matching network is designed, based on the idea introduced on section 3.1.6 ([11]), for broadband gain performance. The matching was designed utilizing the low loss SCTL (Section 2.3.2). To avoid the critical impact of the capacitor quality factor on the PA performance, the DC block capacitors are fixed at 300 fF.

The chip micrograph of the complete PA is presented in Fig. 100b. The total chip size, including all the RF and DC pad structures, is 0.76 mm^2. The active area of the total chip (without pads) is 0.45 mm^2.

In this section, the complete PA design procedure is presented. First, the design of the power stage and the pre-amplifier are explained. Finally, the design of the Wilkinson power combiner with the required terminal impedances is investigated.



(a)



(b)

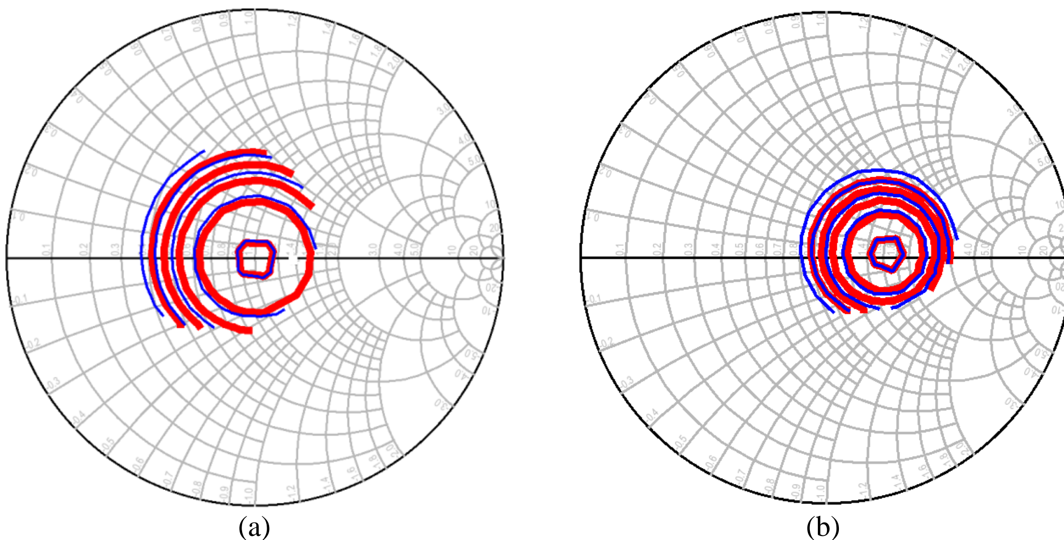
Fig. 100 a) Schematic of the single PA. b) Chip photo with total chip size of 0.76 mm^2.

a) Power Stage: As mentioned in section 5.1.1, around 10 dBm is the required P_{OUT} from the PA. Since the Wilkinson power combiner was utilized, the required P_{OUT} from each individual PA is lower. In this design, by considering less than 1 dB combining loss for the Wilkinson power combiner, each power stage can be designed for 8 dBm P_{OUT}. In this work, each PA is designed with 8 dBm P_{OUT} at around its OP_{1dB} point. Furthermore, the output of the power stage was matched near the saturation power level for the maximum OP_{1dB} while its input was matched to the output of the pre-amplifier for the maximum gain.

In the first step, the transistor size was selected based on the discussion on section 4.1.1. By assuming 3 dB differences between the OP_{1dB} and P_{sat} and a 1 dB loss of the matching network and interconnections, the transistor size can be selected for 12 dBm P_{sat}. As shown in Fig. 94a, by selecting a transistor width around 75 µm, the maximum P_{OUT} around 12 dBm can be achieved. However, this transistor size is much larger than the optimum transistor size for 50 Ω matching. As discussed earlier, to simplify the matching network design and improve its quality factor, the input and output of the PA are matched to 16 Ω. The 16 Ω impedance will later be transformed 50 Ω with the help of the Wilkinson power combiner.

The finger width, NoF and current density of the power stage can be selected from the discussion in the CMOS transistor size selection section (section 4.1.1). Based on Fig. 95 for the stability factor near to one current density around 400 µA/µm is required. In order to achieve the maximum P_{OUT} from the power stage, current densities above 400 µA/µm should be selected. Simulating the graph in Fig**.** 96a for this current density shows that 25 NoF and a 3 µm finger width is optimum.

Based on this transistor size and the current density, and with the help of the load- and source-pull simulation setup, the optimum load and source matching networks were designed. Fig. 101 presents both the large and small signal load-pull simulations at 60 GHz for a single power stage with a matching network. As motioned earlier, in order to select larger transistor sizes and keep the matching network simple, the output of each PA was matched to 16 Ω. As shown in Fig. 101a, the PA has a complete large signal matching at the saturation power level. Despite the large signal matching, the small signal matching stays inside the 10 dB matching circle (Fig. 101b).



(a) (b)

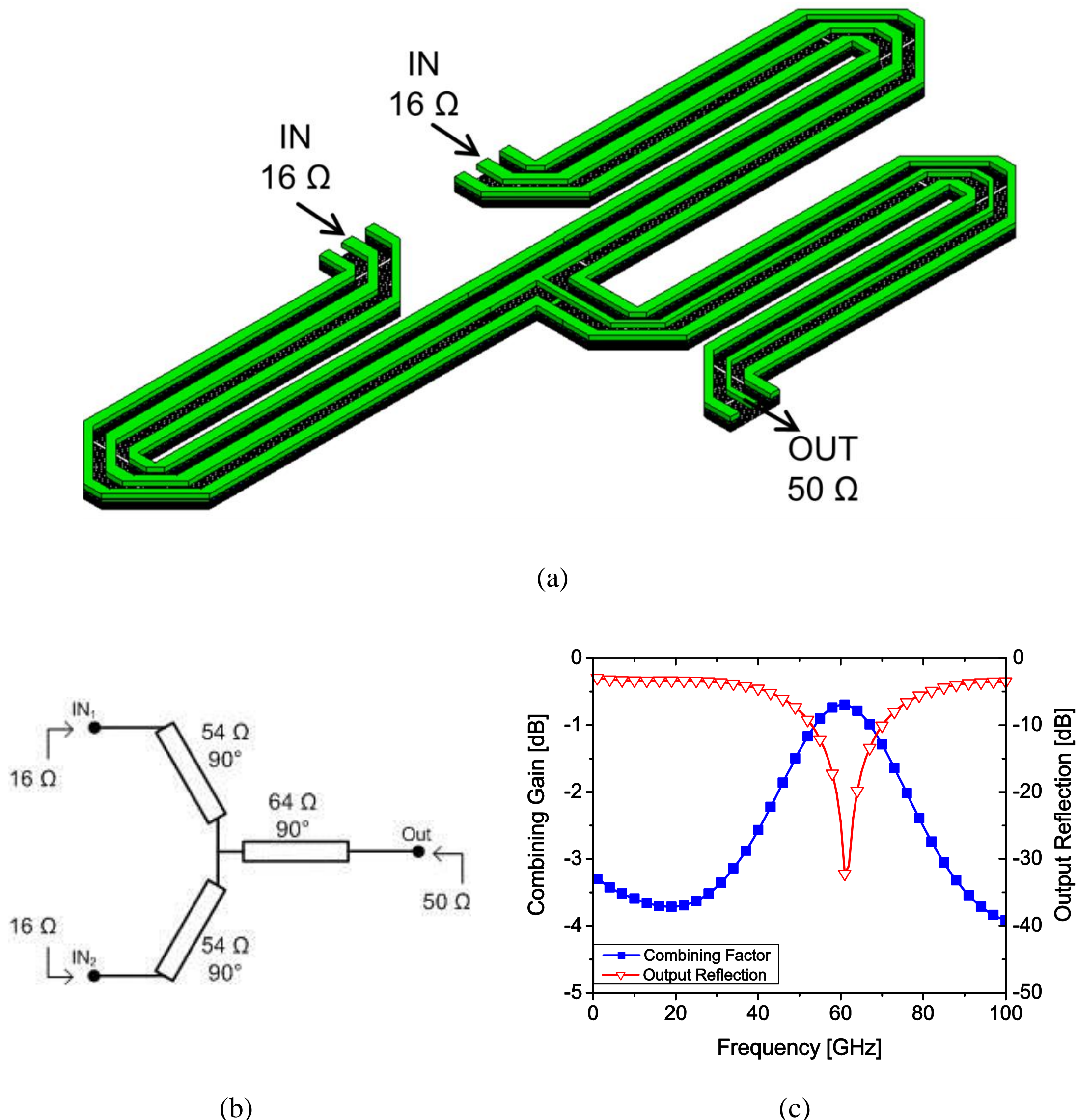
Fig. 101 Load-pull simulation of the PA after matching on the 16 Ω Smith chart and @ 60 GHz: a) At P_{sat}. b) At small signal.

Red: Power with 0.5 dB step. Blue: PAE with 2% steps @P_{sat} and 0.2% @ small signal.

b) Pre-amplifier: The size of the pre-amplifier transistors (60 µm) was selected slightly smaller than the power stage. Besides the transistor size scaling for the pre-amplifier, its current density has also been scaled. In this case, the current density of the pre-amplifier transistor was selected around 250 µA/µm, which is around one and a half times less than the current density of the power stage.

In order to increase the tolerances of the PA against the process variations, the inter-stage matching network was designed for the broadband performance of the PA gain (Section 3.1.6).

c) Wilkinson Power Combiner: The symmetrical input and output Wilkinson power combiner-divider (Fig. 102b) was designed with the introduced transmission lines (Section 2.3.2). The complete structure was simulated with the help of the 3D EM simulator Ansoft HFSS (Fig. 102a). The design shows a combiner loss of less than 1 dB and better than 10 dB output-matching from 55 GHz up to 65 GHz (Fig. 102c). The Wilkinson power combiner is designed to have 16 Ω impedance at the input ports and 50 Ω impedance at the output. As mentioned before, this facilitates the matching network design and improves the output power of the amplifier. The total on-chip size of the Wilkinson combiner is 0.15 mm^2.



(b) (c)

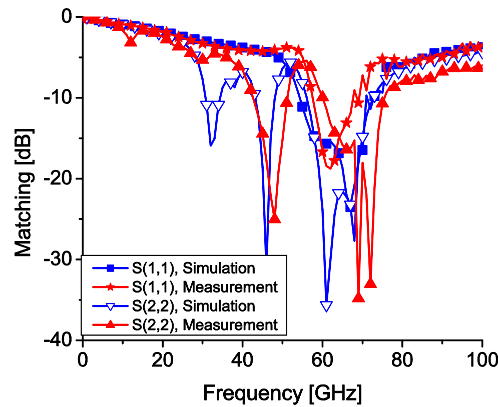
Fig. 102 a) Wilkinson combiner. b) Simulated results of the Wilkinson combiner.

4.2.1.2 Measurement vs. Simulation

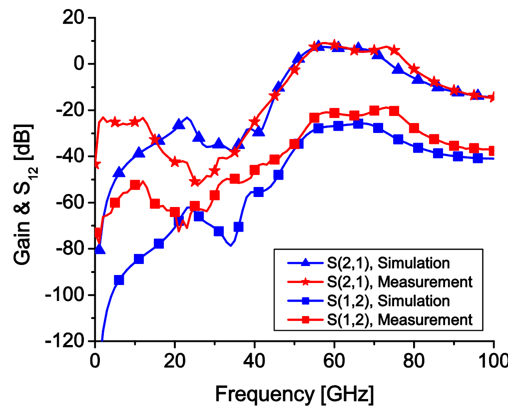
Both large and small signal measurements were performed on-wafer. The measurement setup is the same as that introduced in [12]. All the measurements were carried out at room temperature (23 C) for various bias points. The following sections describe the small and large signal measurement results and their comparison with the simulation.

a) Small Signal Results: Fig. 103 presents the simulated and measured small signal results of the realized PA. The power stage and the pre-amplifier were biased at 1.2 V with 1 V gate voltage for the power stage and 0.8 V for the pre-amplifier. Due to the good small signal modeling of the transistors [9] and the accurate modeling of the passive components [7],[10], the comparison between simulation and measurement shows good agreement.

As shown in Fig. 103a, input-matching values better than 15 dB were achieved for the whole band (57 GHz to 65 GHz). Moreover, output-matching values better than 10 dB were achieved at around 60 GHz. Due to the low isolation in the C.S. topology, and as expected, the PA exhibited only 20 dB isolation between output and input terminals (Fig. 103b). Finally, by utilizing the design technique introduced in [11], a broadband performance of the transducer gain was accomplished. As shown in Fig. 103b, the PA displays almost flat gain, from 57 GHz up to above 70 GHz, with a peak gain of 8.7 dB at around 59 GHz.



(a)



(b)

Fig. 103 Small signal simulation and measurement. a) Matching. b) Gain and S_{12}.

b) Large Signal Results: The large signal measurement was performed at three different operating frequencies (55 GHz, 60 GHz and 65 GHz). Fig. 104a-b present the large signal measurement results at 60 GHz with the same biasing condition as the small signal measurement. The large signal measurement results also show good agreement with the simulated results up to OP_{1dB} of the PA. From Fig. 104a it can be seen that the PA exhibits more than 8 dB gain with 9 dBm OP_{1dB} and more than 11 dBm P_{sat}.

Furthermore, under this biasing condition PA consumes around 100 mW DC power at the saturation level, resulting in more than 6% peak PAE and 10% drain efficiency (Fig. 104b). The detailed performance of the PA for each measured frequency is presented in Fig. 104c.

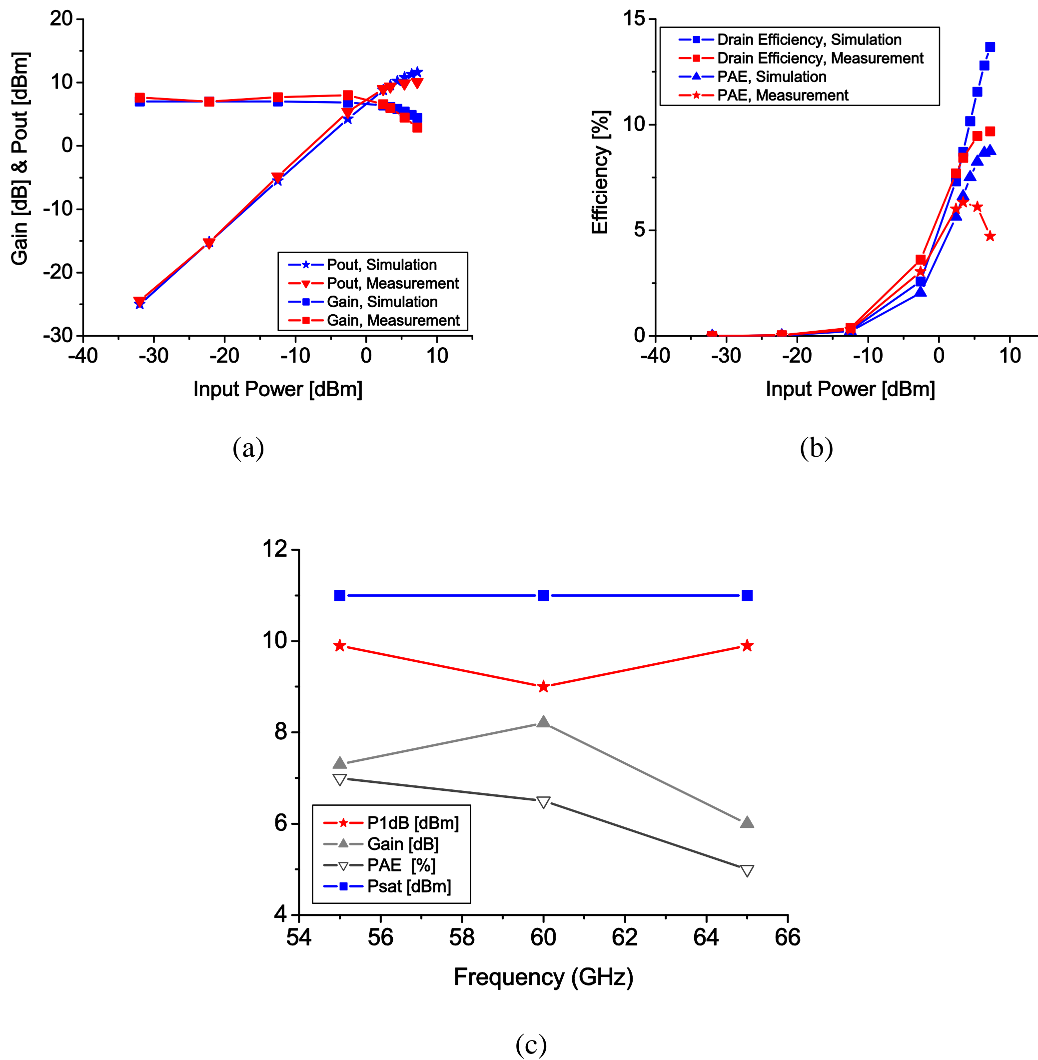


Fig. 104 Large signal simulation and measurement. a) Power. b) Efficiency. c) Large signal measured results at three different frequencies.

4.2.2 Transformer CMOS Power Amplifier

In this work, the design of transformer-based power amplifiers was investigated [1]. For this purpose, a new scalable model for on-chip transformers is introduced (Section 2.3.3). The modeling technique is also validated for 90 nm LP CMOS technology by comparing measured and simulated results. Due to the high accuracy and scalability of the model, a faster and more accurate design procedure for a high performance transformer-based power amplifier design is achieved. The measured results of the power amplifier show 22 dB gain, 14 dBm saturated output power, 12 dBm output power and a 1dB compression point at 60 GHz with 0.065 mm^2 active chip size.

The high P_{OUT} requirement for 60 GHz CMOS application required the utilization of power combining techniques or array structures. In each case, to minimize the total chip area, the size of each PA must be minimized. Fig. 105 compares the trend of P_{sat} and OP_{1dB} versus power-stage-chip-size (the active chip size divided by the number of stages) for published state-of-the-art CMOS PAs. Estimations show a faster P_{OUT} drop for power-stage-chip-sizes of less than 0.015 mm^2. Based on Fig. 105, 14 dBm P_{sat} and 12 dBm OP_{1dB} with 0.015 mm^2 are quite feasible. Although these results are 4 times less than the results published in [78], the active chip size of the power stage is 20 times smaller.

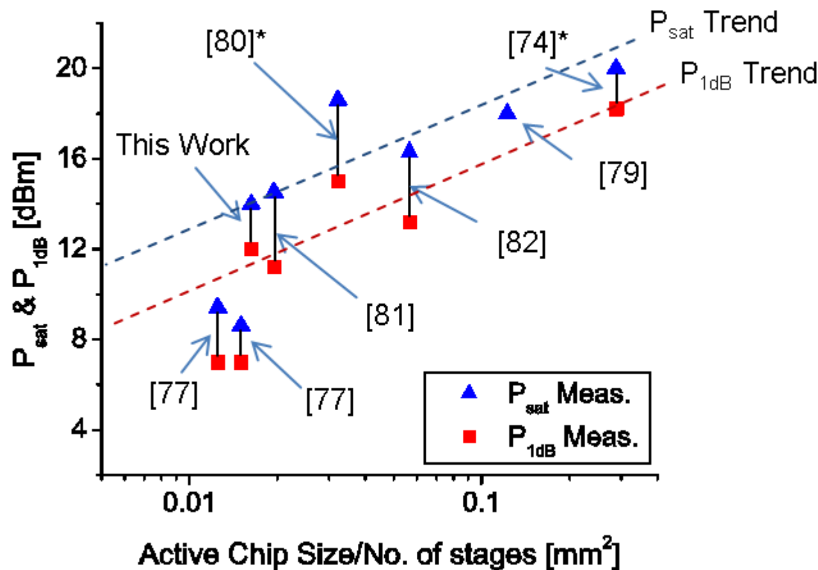


Fig. 105 The OP_{1dB} and P_{sat} of the state-of-the-art PAs vs. the power stage size (Active chip size divided by number of stages).

* Estimated chip size

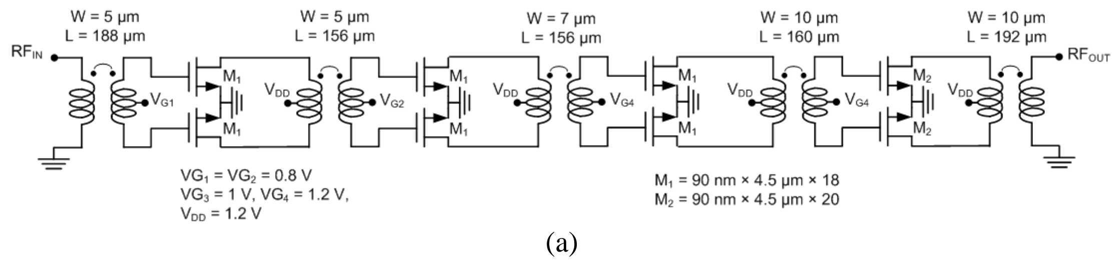
In recent years, developments in transformer-based CMOS PA designs have shown the capacity for chip size minimization without noticeable P_{OUT} degradation [77]. To ease the use of transformers in mm-wave circuit design, scalable models for transformers have been developed by different circuit designers [76]-[77]. In this work, the developed scalable model (Section 2.3.3) for on-chip transformers has been utilized in the design of a 60 GHz PA. In the first section, the design of this transformer-based 60 GHz PA - with the help of this model - is investigated. In the

second section, the measured and the simulated results of the realized PA are compared to validate the design procedure.

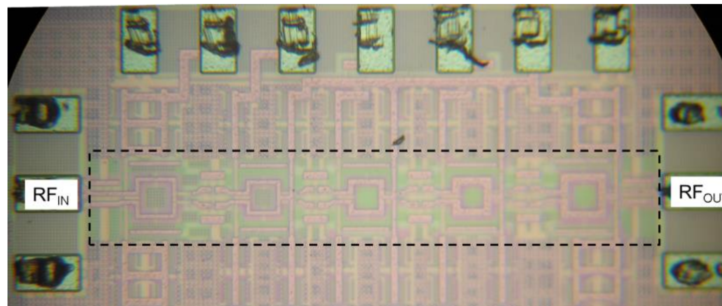
4.2.2.1 Power Amplifier Design

Based on the modeled transformer, a high performance 60 GHz PA has been designed. Four stages with a C.S. topology (Fig. 106a) were selected for better gain and P_{OUT} (Section 4.1.2). In order to avoid source degeneration caused by the parasitic elements of the ground plane, the sources of the differential transistor pairs in each stage are connected as closely as possible to each other.

All the pre-amplifiers are designed with the same transistor sizes but with different biasing. The first two-stages are biased with 200 µA/µm, the third stage with 300 µA/µm and the power stage with 450 µA/µm drain current densities. The chip micrograph of the PA is shown in Fig. 106b with 0.065 mm^2 active chip size.



(a)



(b)

Fig. 106 a) The schematic of the transformer-based PA. b) Chip micrograph of the realized PA with 0.065 mm^2 active chip size and 0.27 mm^2 total chip size.

The design procedure for the power stage (the last stage) is shown in Fig. 107. In this Smith chart, the optimum input and output impedances (Z_{IN} and Z_{OUT}) of the transistor with differential structure, including the transistor core versus the transistor size, are presented. In addition, by using (15), all those impedances that can be transformed to 50 Ω impedance using the introduced transformer model are calculated (the yellow circle in Fig. 107). Based on this calculation, any transistor sizes larger than 70 µm (for each transistor) can be matched at small and large signal levels to 50 Ω impedance using the introduced transformer. Although larger transistor sizes are required for higher P_{OUT}, due to intrinsic parasitic elements of the transistor and f_t and f_{max} drop, the maximum achievable P_{OUT} in this technology is limited and remains almost constant for transistor sizes above 120 µm (Section 4.1.1). In this design, by considering Fig. 107 and performing a tradeoff between the gain, P_{OUT}, PAE and the size of the transformer, the power stage transistor size is selected (Fig. 106a). By considering the size of the power stage transistors, the rest of the PA is designed with the same technique.

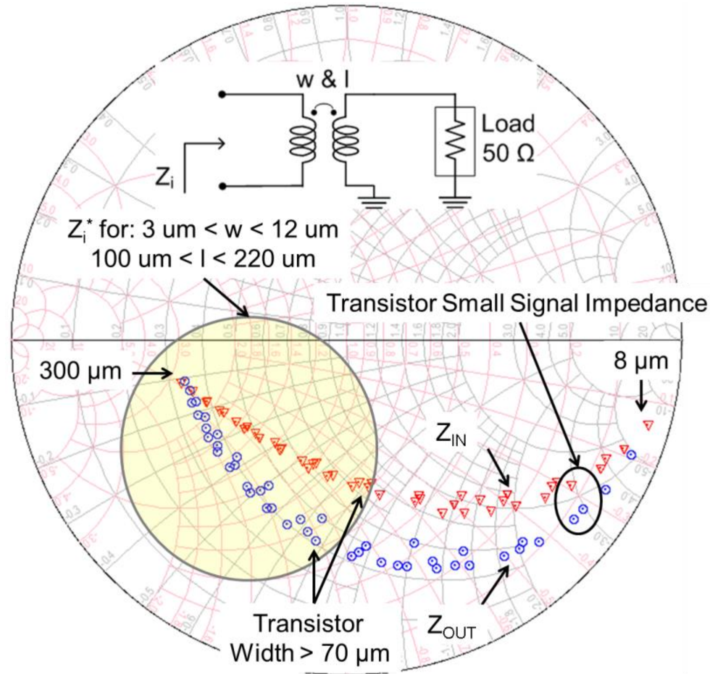
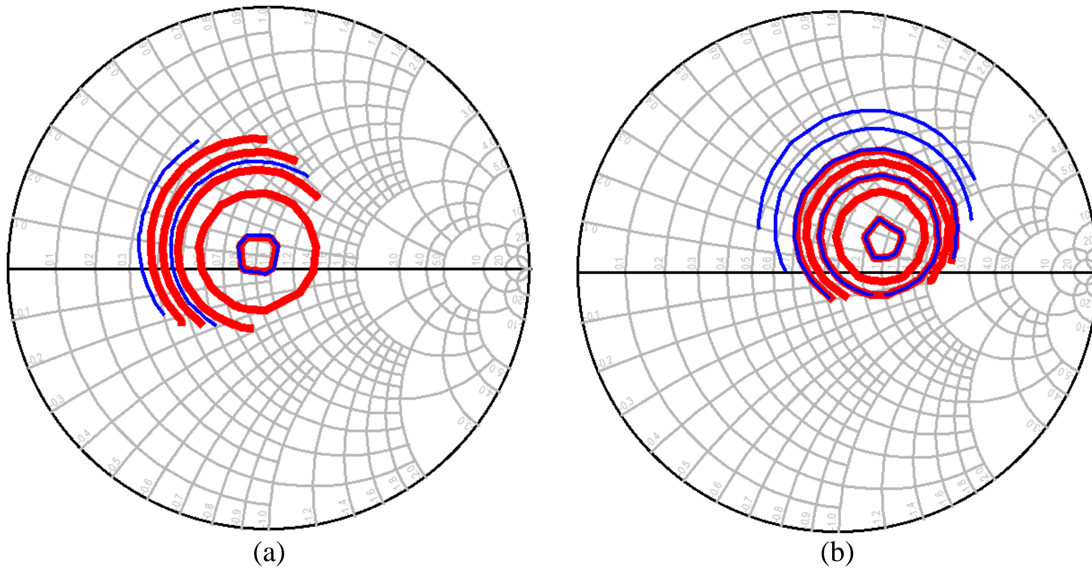


Fig. 107 Optimum power stage transistor sizes for transformer-based matching.

As the output of the power stage has been matched at the large signal level, a very good output-matching near the saturation level is achieved (Fig. 108a). Despite the large signal matching of the PA, the small signal matching stays inside the 10 dB matching circle (Fig. 108b).



(a) (b)

Fig. 108 Load-pull simulation of the PA after matching @ 60 GHz:
a) At P_{sat}. b) Small signal.
Red: Power with 0.5 dB step. Blue: PAE with 2% steps @P_{sat} and 0.2% @ small signal.

4.2.2.2 Measurement vs. Simulation

Small and large signal measurements are performed on-chip and at room temperature up to 67 GHz. The measurement setup is the same as that introduced in [12]. In all the measurements, the PA consumes 200 mA from a 1.2 V supply voltage. The small signal measured results show good agreement with the simulated results. A small signal gain of around 22 dB and with more than 10 dB matching at both input and output terminals was achieved at around 60 GHz (Fig. 109).

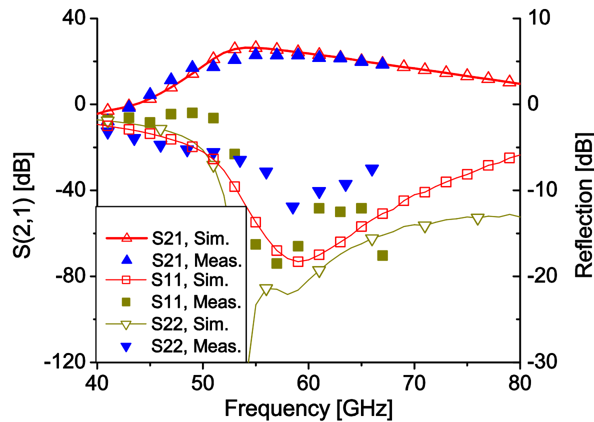


Fig. 109 Measured and simulated S-parameter results of the PA.

Fig. 110a presents the large signal measured and simulated results of the PA at 60 GHz with good agreement up to P_{sat}. The measured PA achieves around 12 dBm OP_{1dB} and 14 dBm P_{sat} with 10 % PAE.

The large signal performances of the PA are also measured for four IEEE 802.15.3c channels. The PA shows a relatively constant OP_{1dB} and P_{sat} for all four channels, which is appropriate for broadband application at 60 GHz (Fig. 110b).

The output third-order intercept point (OIP3) is also measured for both upper and lower harmonics at 10 MHz and 1 GHz frequency offsets. The measured results show around 18 dBm OIP3 for all four measured channels (Fig. 110b).

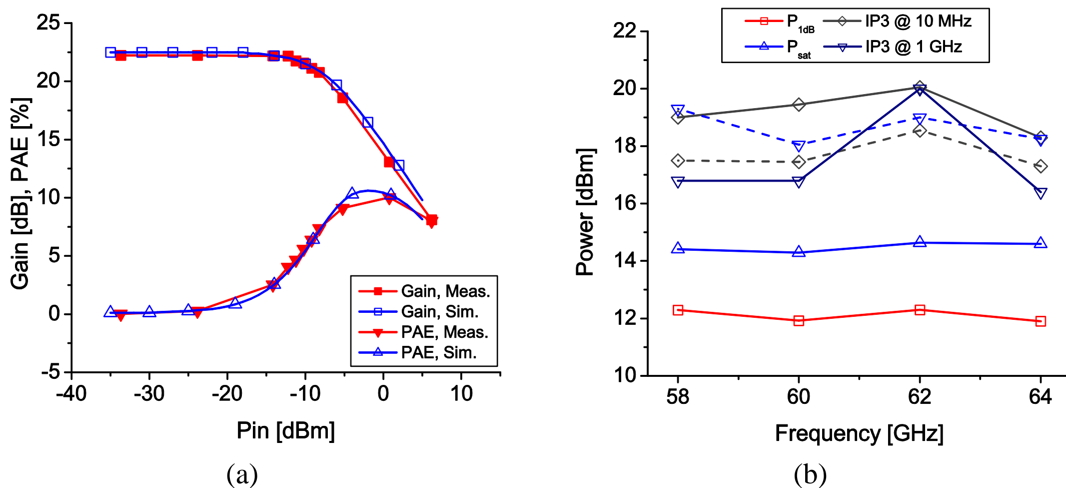


Fig. 110 a) Large signal measured and simulated results vs. power at 60 GHz. b) Measured linearity and large signal for four IEEE 802.15.3c channels. The dash line is the upper channel and the solid line is the lower one.

4.3 Conclusion

In this work, the design and optimizations of 60 GHz Si CMOS PAs on the 90 nm technology have been investigated. The investigations show the limitations of the transistor size and topology (Section 4.1) for high power applications. The limited output power of the transistors requires the usage of power combining techniques. Two different types of on-chip power combiners (Wilkinson and transformer) were studied in this work and, based on these power combiners, two different PAs were designed, realized and measured.

In the first PA, and to improve the output power, a Wilkinson combiner was designed and the outputs of two single PAs with a C.S. topology were combined. The designed Wilkinson combiner transfers the 16 Ω at the input ports to 50 Ω at the output, which facilitates the matching network design and improves the power performance of the PAs. All the matching networks and Wilkinson combiners were designed with the help of low loss shielded coplanar transmission lines (Section 2.3.2) for the further minimization of the combining losses. The utilization of a full chip EM simulation led to a good estimation of all the parasitic elements and resulted in good agreement between the simulated and measured results.

Although Wilkinson combining enhances the power performance of the PA, due to the large size of this structure the resulting chip size is quite large. In order to minimize the chip size and further improve the PA performance, a transformer-based PA design was investigated. Unlike the Wilkinson combiner, transformers can play the roles of DC feeding and matching besides power combining. This further facilitates the DC feed and matching network design and results in much smaller chip sizes. Further, due to the removal of the matching networks and DC feeds, the total losses at the output of the transistors are much lower in this PA in comparison with the Wilkinson PA. Also, as the source of the differential transistors in each stage is placed as near as possible to each other, the RF ground at these points is almost perfect and, hence, the source degeneration due to the parasitic elements of the ground plane is minimized in the transformer based PA. These all together have resulted in higher power performance of the transformer based PA in comparison with the Wilkinson PA.

As a result of the above discussion, in the second part of this work a new technique for transformer-based PA design is studied. For this purpose, a scalable transformer model has been developed (Section 2.3.3). Thanks to the transformer model accuracy and design procedure, a high performance PA was developed. The realized PA, with 14 dBm P_{sat} and 12 dBm OP_{1dB}, agrees well with the trend shown in Fig. 105. Moreover, the 0.065 mm^2 active chip size makes this PA quite appealing for on-chip power combining and array system design.

Table. 16 compares the designed PAs in this work with the currently published state-of-the-art results with the 90 nm CMOS technology. As mentioned earlier, due to lower combining losses and a less complicated matching network and DC feed in the transformer-based PA (in comparison with the Wilkinson PA), the achieved performance of the transformer-based PA is much better.

Further comparisons demonstrate the much smaller size of the designed transformer-based PA in comparison with the other PAs. In comparison with [78], the transformer-based PA has a more than 20 times smaller chip size with only 4 times less output power. Also, and in comparison with [83], this PA has a more than 6 times

smaller chip size with 3 times less output power. In addition, by comparing this work with the other state-of-the-art transformer-based PAs ([77] and [81]), it can be observed that with almost the same chip size, higher gain, P_{sat} and OP_{1dB} have been achieved. As this technology does not provide high quality capacitors, the usage of the neutralization network has been avoided and, hence, the achieved PAE in this work is slightly lower than the state-of-the-art results.

Table. 16 Comparison of our works with previously published PAs

REF	Gain [dB]	P_{sat} [dBm]	OP_{1dB} [dBm]	PAE [%]	V_{DD} [V]	Active Chip size [mm^2]
[78]	20.6	19.9	18.2	14.2	1.2	1.4
[83]	15.5	18.5	N.A.	10	1.2	0.4
[60]	4.2	14.2	12.1	5.8	1	0.85
[1]	22	14.5	12	10	1.2	0.065
[77]	5.5	12.3	9	8.8	1	0.24*
[87]	20	12	8.2	9	1.2	0.65*
[60]	8.2	11.6	10.1	11.5	1	1*
[88]	16.3	11.5	10.5	8.5	0.9	0.16
[77]	13.8	11	N.A.	14.6	1.2	0.22
[8]	8	11	9	6	1.2	0.45
[81]	20	9.4	7	19.5	1.2	0.05
[87]	17	8.4	5.1	5.8	1.2	0.99*
[67]	9.6	7.6	5	4.3	1.2	N.A.

* Approximated from chip photo.

5 Transmitters

Two types of transmitter, heterodyne and ON-OFF-shift-keying (OOK), have been investigated in this work. The transmitters are realized with 90 nm low power CMOS technology. The characterizations and measurements show the functionality of these circuits for different 60 GHz short-range data communication scenarios.

There are many advantages and disadvantages for each of these transmitter topologies. Based on these advantages and the system requirements, the optimum transmitter topology must be selected. In this case, a detailed study of each topology is necessary.

The main advantage of the heterodyne transmitter lies in its bandwidth efficiency. By utilizing complex modulation schemes, like 16QPSK, a much higher bitrate for the same bandwidth can be achieved. The relation between bandwidth and modulation scheme and bitrate can be formulated as follows:

$$BW = \alpha \times \frac{Bit\ Rate}{n} = \alpha \times Symbol\ Rate \tag{19}$$

In the above formula, α is the modulation factor (less than 2) and n is the number of the bits per symbol. For example, for 5 Gbps in the BPSK system, an 8 GHz bandwidth (α = 1.8) is required while in a QPSK system the required bandwidth is around 4 GHz (α = 1.6); in the 16QPSK system, for the same bitrate the bandwidth can be as low as 2 GHz. These calculations reveal the importance of the heterodyne topology for the scenarios where high data-rate communication in the narrow frequency band is required.

Although the OOK transmitter suffers from bandwidth inefficiency, it has less circuit complexity, lower DC power consumption and a smaller chip size in comparison with the heterodyne transmitter. All these advantages are mainly because of the lower number of components and the simpler system architecture of the OOK in comparison with the heterodyne transmitter. The main components of the OOK transmitter are an oscillator (without any PLL), a modulator (which can be as small as a switch) and a medium power PA. The medium power requirement in the OOK is mainly due to no back-off requirement in the modulation scheme.

In the first section, the design, realization and characterization of the heterodyne transmitter is presented. The realized transmitter achieves between 13 dBm to 15.5 dBm P_{OUT}, 11 dBm to 14 dBm P_{1dB}, 8% to 14% efficiency and 22 dB to 30 dB power gain for all four channels defined in the IEEE 802.15.3c [32].

In the second section, the design, realization, characterization and system measurements of the OOK transmitter are presented. This transmitter achieves 8 dBm P_{OUT}, 9 dB gain and 17% efficiency with less than 36 mW DC power consumption. The realized transmitter was further utilized in an OOK transceiver system setup, where more than 6 Gbps was transmitted over a 4 m distance.

Finally, the last section concludes these works.

5.1 Heterodyne Transmitter

The block diagram of the 60 GHz heterodyne Tx is presented in Fig. 111a. The IF is selected at around 20 GHz and the LO at around 40 GHz, both based on IEEE 802.15.3c [32]. The IF, LO, and RF frequencies are listed in Table. 17.

The first harmonics ($F_{LO} \pm F_{IF}$) at the output of the mixer are 20 GHz and 60 GHz. In this topology, the RF signal (60 GHz) is selected far away from the image signal (20 GHz), which can be damped down in the output using the transformer, matching network and the gain of the PA (Fig. 111b-c).

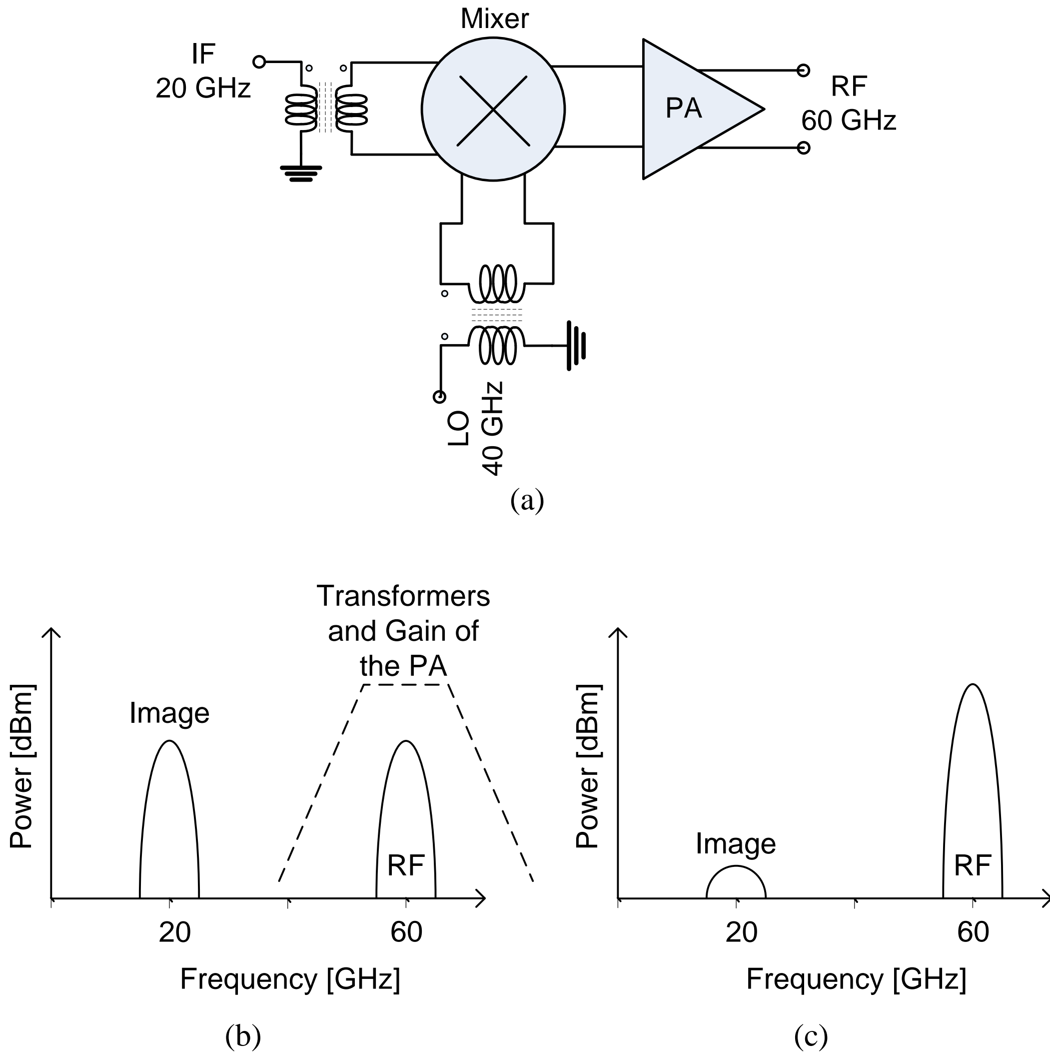


Fig. 111 a) The block diagram of the Heterodyne transmitter. b) Output power of the Mixer. c) Output power after the PA.

Table. 17 60 GHz frequency plan for IEEE802.15.3c standard.

Channel #	Center (GHz)	LO (GHz)	IF (GHz)
1	58.32	38.88	19.44
2	60.48	40.32	20.16
3	62.64	41.76	20.88
4	64.80	43.20	21.60

5.1.1 Link Budget

The link budget must be calculated for different modulation schemes. This is mainly due to the different SNR requirement for each modulation. The four IEEE channels and the system plan for short-range data communication based on this standard are presented in Fig. 112 and Fig. 113. By considering these values, the minimum required P_{OUT} from the PA for each modulation scheme can be calculated (Table. 18). Based on these calculations, in order to be able to transmit all these modulation schemes over a 4 m distance, a minimum P_{1dB} of around 10 dBm from the PA is required.

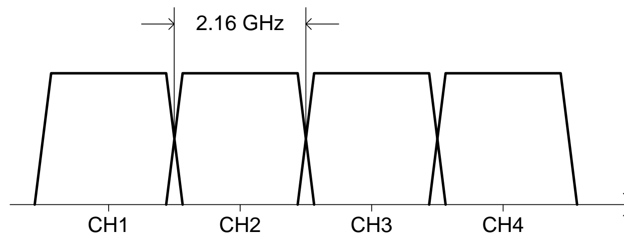


Fig. 112 The four IEEE802.15.3c channels.

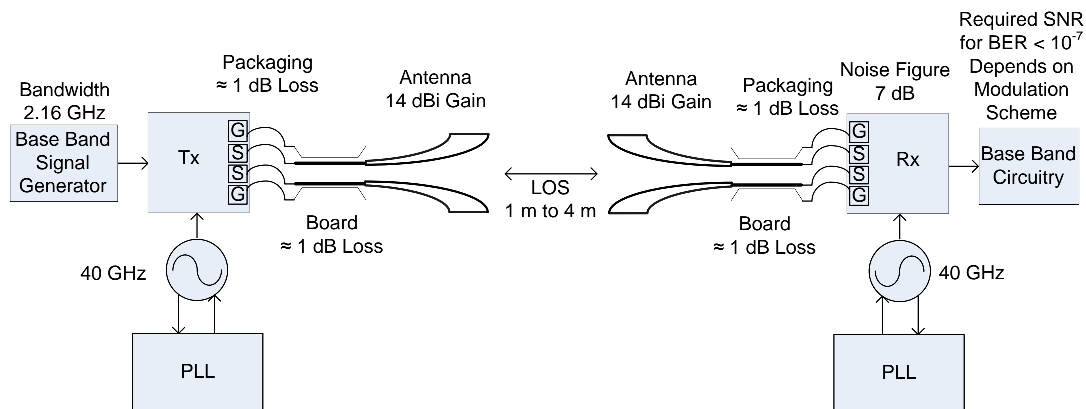


Fig. 113 System plan.

Table. 18 Link budget calculation.

Modulation Scheme	OFDM BPSK	OFDM QPSK	OFDM 16QPSK	OFDM 64QPSK	Units
Distance	4	4	4	4	m
Bandwidth	2.16	2.16	2.16	2.16	GHz
Antenna Gain Tx/Rx	14	14	14	14	dBi
RF packaging losses Tx/Rx	3	3	3	3	dB
BB packaging losses Rx*	2	2	2	2	dB
Receiver noise figure [91]	7	7	7	7	dB
Required SNR	2.5	5.5	12.1	16.7	dB
Required Tx Back-off*	10	10	10	10	dB
Min. Tx required P_{OUT}	-3.6	-0.6	6	10.8	dBm
Achieved bit rate*	0.756	1.512	3.024	3.402	-

* Defined in EASY-A project by the project partner IHP.

5.1.2 Circuit Design

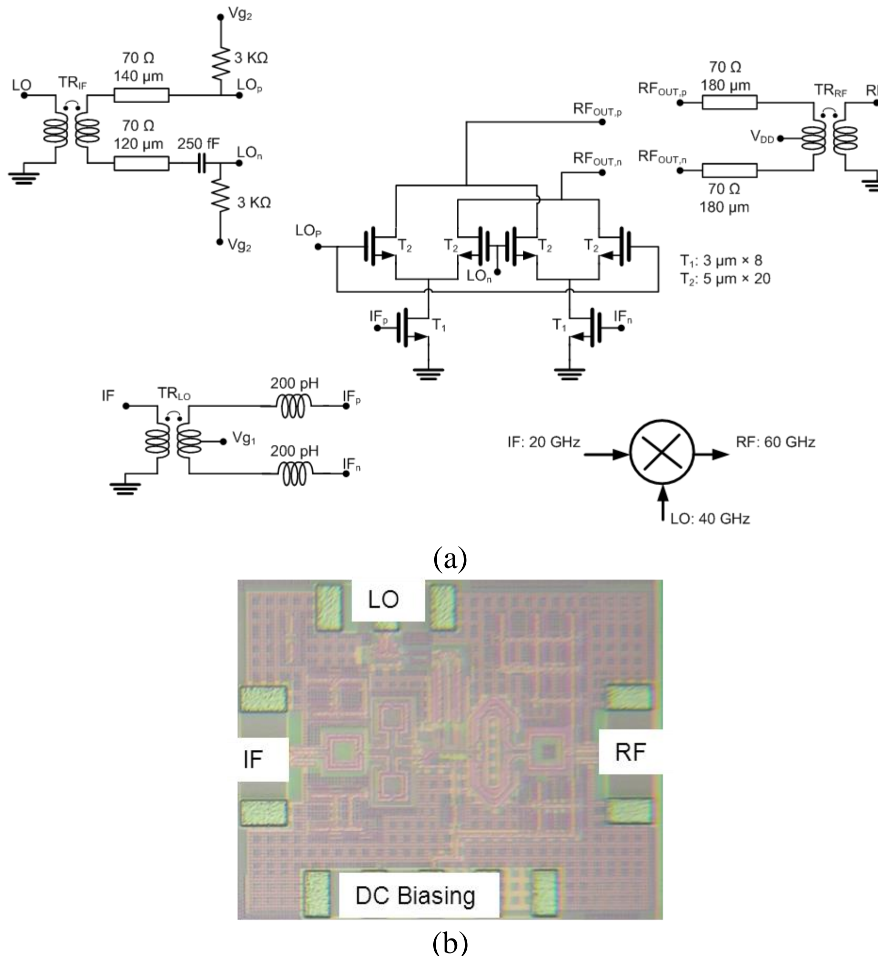
The transmitter consists of two main circuits, a PA and an up-converter. To minimize the LO leakage to the output, a Gilbert cell topology has been selected for the up-converter. In order to be able to characterize it completely, the mixer was realized and measured separately. In addition, the PA utilized in this work is the extension of the PA presented in the previous section (Transformer CMOS Power Amplifier).

Furthermore, in order to maximize the common mode rejection and the effect of the ground parasitic element on the circuit's performance, a fully differential topology was selected for both circuits. In this case, and for ground parasitic suppression, the emitters of each differential transistor pair are located as close as possible to one another.

In this section, the detail design procedure of each circuit is presented.

5.1.2.1 Up-Converter

Fig. 114a presents the schematic of the Gilbert cell mixer. Because of differential measurement limitations, differential-to-single-ended baluns are used at all ports. The detailed design procedure of the baluns is presented on section 2.3.3 (Transformer Design). The high quality factor SCTL (Section 2.3.2) is also utilized in the matching network circuits. Including the pads and baluns, the total size of the mixer is 0.41 mm^2 (Fig. 114b).



(a)

(b)

Fig. 114 a) Schematic of the mixer. b) Chip photo with 0.41 mm^2 total chip size.

The transistor sizes are optimized to meet the design requirements. In this circuit, the T_1 transistors are the IF amplifying transistors while the T_2 transistors are responsible for mixing the LO and IF signals. A co-design must be performed for the T_1 and T_2 transistor size selections, as their performance is closely related to their size. In this work, the size of the T_2 transistor has been selected as the first optimization point. Based on this selection, the optimum size for the T_1 transistors was calculated.

The LO switching transistors (T_2) are selected based on Fig. 115. Fig. 115a shows the simulation setup. In this setup, the V_{DD} is set to 0.6 V, since in the maximum V_{DS} of the switching transistors in the Gilbert cell cannot exceed this value. The gate was biased with 0 V for the off-case and 1.2 V for the on-case. By using this setup, the ON-OFF impedance of the switch was calculated at the IF frequency (around 20 GHz). A correct transistor size must have low impedance at the ON condition while showing high impedance at the OFF condition.

The ON-OFF impedances of the transistor are calculated for various transistor sizes. According to Fig. 115b-c, the transistor size with 3 μm width and 15 fingers (NoF=15) shows simultaneously low ON impedance and high OFF impedance. As each IF signal (drain of the T_1 in Fig. 114a) is connected to two T_2 transistors, a width of 3 μm and NoF=8 can be selected for each T_2 transistor.

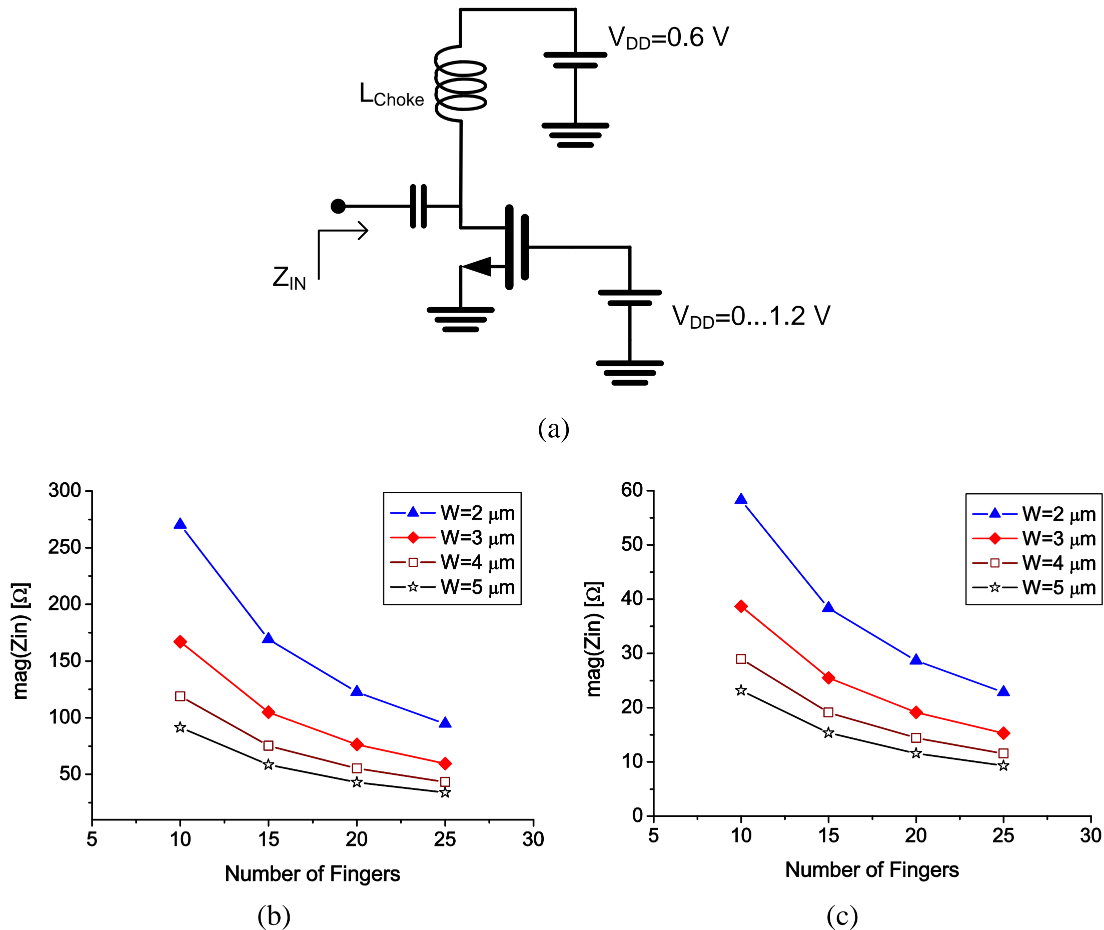
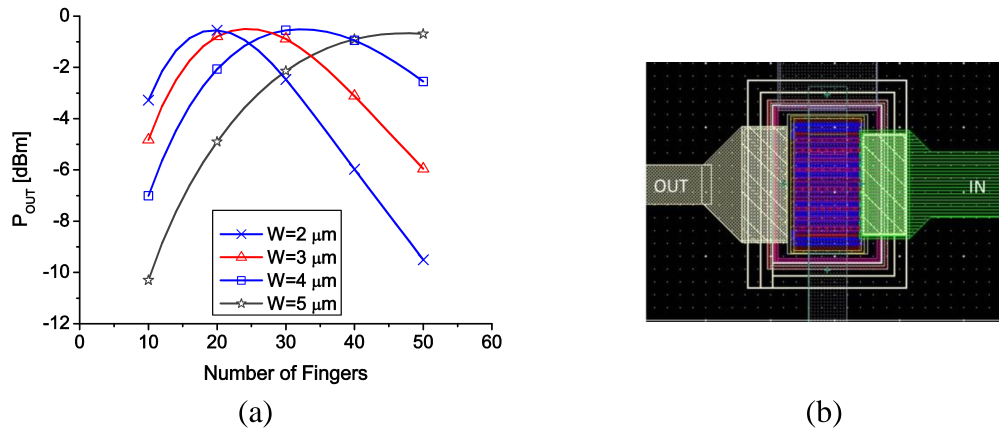


Fig. 115 The T_2 transistor output impedance vs. size. a) Schematic. b) Z_{IN} for OFF condition. c) Z_{IN} for ON condition.

Consequently, by selecting the T_2 transistor size, the T_1 transistor size can be selected. In this case, the T_1 transistors are optimized for the maximum output power performance of the mixer. Fig. 116 shows the simulated saturation output power performance of the mixer versus the transistor size while Table. 19 summarizes all the transistor sizes in which the P_{OUT} is at its maximum. Due to process and layout limitations, less transistor fingers are preferable. In this design, 20 fingers with 5 µm width were selected for the T_1 transistors. Finally, further optimization iterations show minimum T_1 and T_2 transistor size changes from these values.



(a) (b)

Fig. 116 a) Output power for various transistor sizes
(IF-power = 0 dBm & LO-power = 5 dBm). b) IF transistor layout.

Table. 19 The optimum transistor sizes for the maximum output power.

W (µm)	NF	Total Size	P_{OUT} (dBm)
2	48	96	-0.5
3	32	96	-0.5
4	24	96	-0.5
5	20	100	-0.5

As the next step, the mixer is matched at all the terminals to 50 Ω. The S-parameter simulation of the mixer is presented in Fig. 117. The RF-matching is designed as broadly as possible to avoid any frequency shift effect on the mixer performance. Therefore, in this design an output-matching of greater than 15 dB was the design goal over the entire V-band. In addition, the 10 dB IF and LO matching bandwidth covers the IF and LO frequencies of the four targeted IEEE channels.

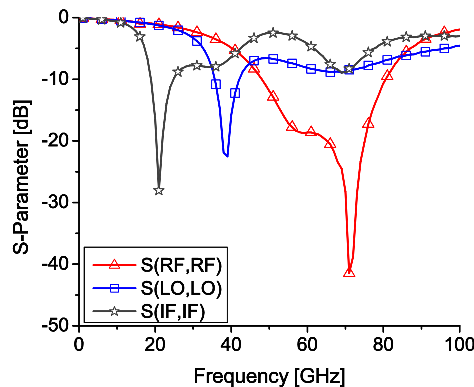
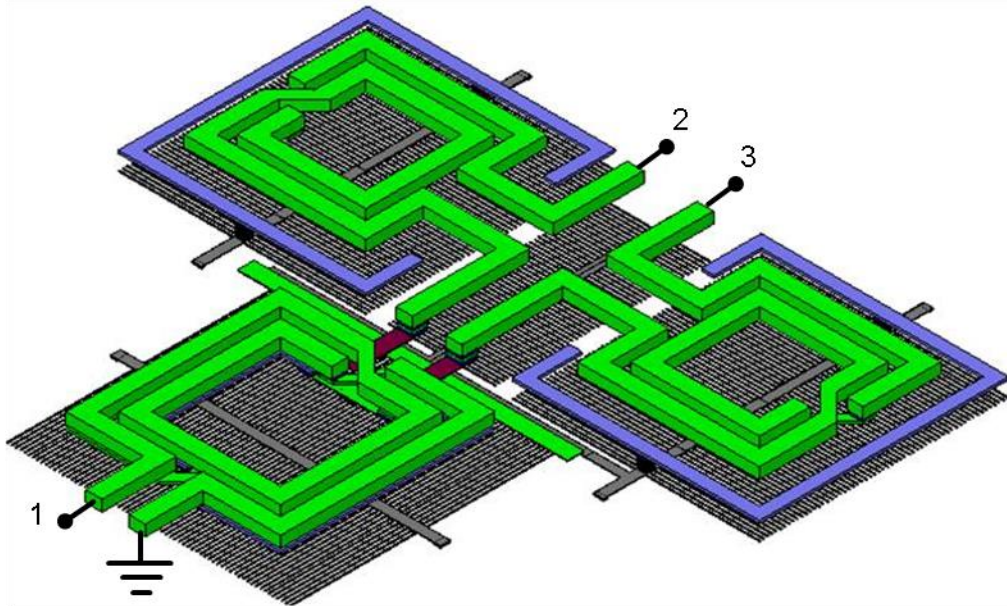
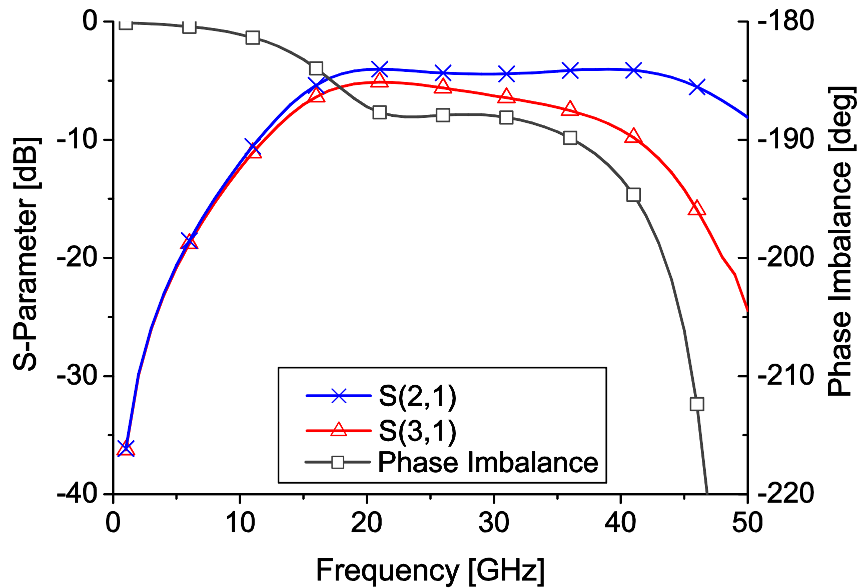


Fig. 117. Simulated S-parameter results.

The IF, LO and RF transformers were utilized as a balun and a matching network in this design. The 3D view and the S-parameter simulation of the IF-matching network and the balun are presented in Fig. 118a-b. The inductor was designed on M9 (UTM) for the maximum Q-factor. The size of the inductors was optimized to have a 200 pH inductance value at around 20 GHz. An amplitude imbalance of 1 dB and a phase imbalance of less than 10° was achieved at around 20 GHz.



(a)



(b)

Fig. 118 a) IF matching and transformer. b) S-parameter and phase imbalance simulation of the IF matching network.

5.1.2.2 Power Amplifier

The designed PA in this work is the same as the PA described on section 4.2.2, with an extra pre-amplifier stage and some stability circuitries. The complete schematic of this circuit is presented in Fig. 119. The parallel R-C network (R_1 and C_1) was added between the third and the fourth stages to damp down the low frequency oscillations. The network cut-off frequency can be calculated as follows:

$$f_{RC} = \frac{1}{2\pi R_1 C_1} = 6.6\,GHz$$

The 6.6 GHz cut-off frequency is much lower than the minimum frequency of the first channel (57.24 GHz) and still high enough to surpass all the low frequency oscillations (near DC oscillations). The in-band stabilization was performed by using source degeneration. This was done by adding small common mode inductors (L_1) to the source of the M_2 transistors. The value of this inductor is around 5 pH.

All the transistor sizes from the first up to the fourth stage were the same. Although the transistor width scaling for the pre-amplifier stages can improve the PAE of the PA, as mentioned in section 4.2.2.1, and due to the design complications of the scaled transistors, the drain current scaling was selected instead. In this case, the drain current densities of the first three stages are selected at a very low level (120 µA/µm). A medium drain current density was selected for the fourth stage (300 µA/µm) and a high drain current density for the last stage (450 µA/µm).

Finally, a matching network (L_2, L_3 and C_2) was added to match the output of the PA at the large signal level (near the P_{sat} of the PA). The load-pull simulations of the PA at different power levels are presented in Fig. 120.

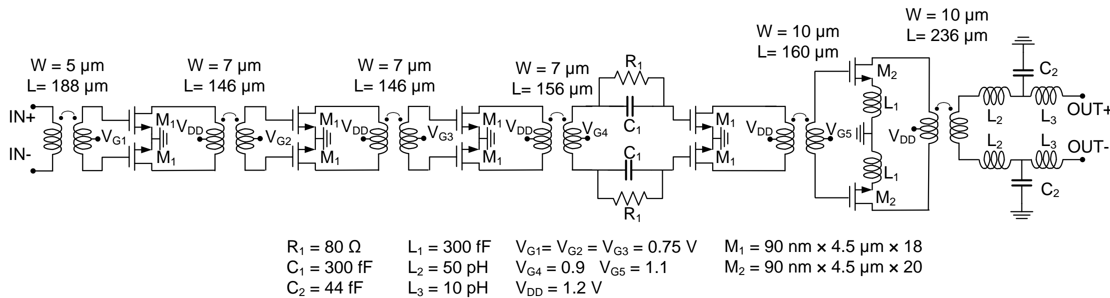
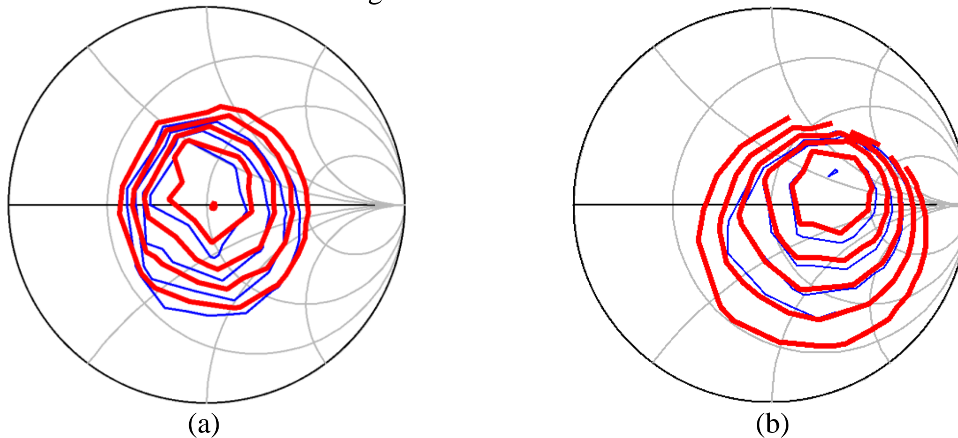


Fig. 119 PA schematic.



(a) (b)

Fig. 120 Load-pull simulation of the PA after matching @ 60 GHz:
a) At P_{sat}. b) Small signal.
Red: Power with 0.5 dB step. Blue: PAE with 2% steps @P_{sat} and 0.2% @ small signal.

5.1.3 Experimental Results

Both the mixer and the PA were realized and measured separately. The measured results of the PA (with three pre-amplifiers and a single output) have already been introduced on section 4.2.2. In this section, firstly, the measured versus the simulated results of the mixer are presented and compared. Finally, the results of the whole transmitter are shown. The chip micrograph of the complete transmitter are presented in Fig. 121.

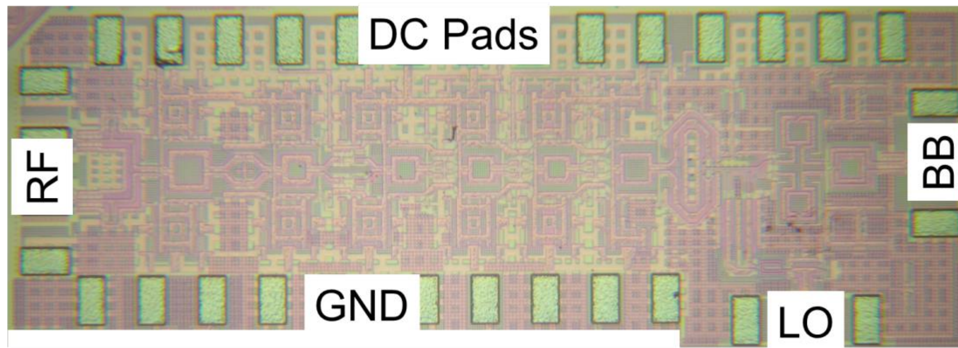


Fig. 121 Chip micrograph with 0.6 mm² (0.4×1.5mm²) chip size including pads.

5.1.3.1 Up-Converter

As mentioned earlier, the mixer was matched at all terminals to 50 Ω. The S-parameter measured versus the simulated results of the mixer are presented in Fig. 122. The RF-matching is designed as broadly as possible to avoid any frequency shift effects on the performance of the mixer. In this design, an output-matching better than 10 dB was achieved in the measurement for the entire required band. Moreover, a higher than 10 dB IF- and LO-matching has been measured for all the four IEEE channels.

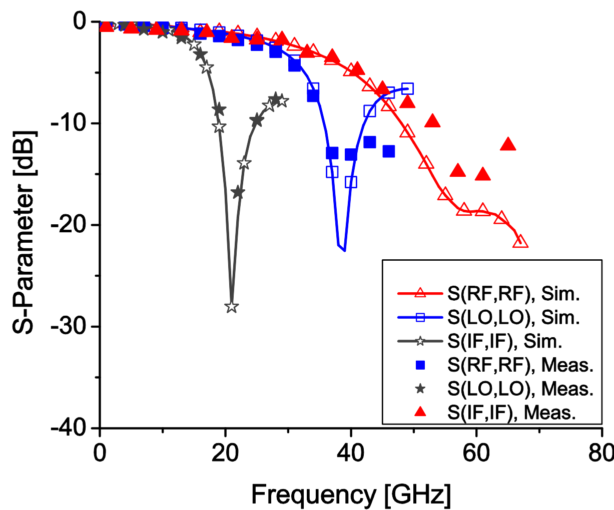


Fig. 122 Simulated S-parameter results.

The measurement setup includes two DC to 50 GHz HP 83650L signal generators for the IF and LO sources, a variable attenuator and a R&S FSU spectrum

analyzer for DC up to 67 GHz. Fig. 123 presents the measured CG of different channels and the P_{DC} for various LO powers. At 4 dBm LO power, the measured results show less than 1 dB CG variation from channel no.1 to no.4. The DC power was 17 mW.

In addition, the large signal measurements were performed for various IF power levels, at 14 mA (from 1.2 VDD) drain current and 4 dBm LO power. Fig. 124 compares the measured and simulated results of the up-converter for channel no.2. The OP_{1dB} around -9 dBm and the CG of -2 dB is achieved in the measurement. Due to the careful modeling of all passive and active components, good agreement between simulations and measurements was observed. Also, due to the carefully designed mixer core and the small size of the T_1 transistors, a very high LO-RF and IF-RF isolation was achieved. Fig. 125 presents the measured isolation at the center frequency of each channel. For all the channels, an isolation greater than 30 dB was measured.

Fig. 126 presents the complete large signal performance of the mixer for all four IEEE standard channels. The measurements were performed at the center frequency of each channel. Due to the problems explained earlier, the mixer has slightly less CG than the simulation in the entire band. A flat CG and OP_{1dB} were measured for all four channels, which makes this mixer appropriate for this application. The performance summary of the mixer for all four channels is presented in Table. 20.

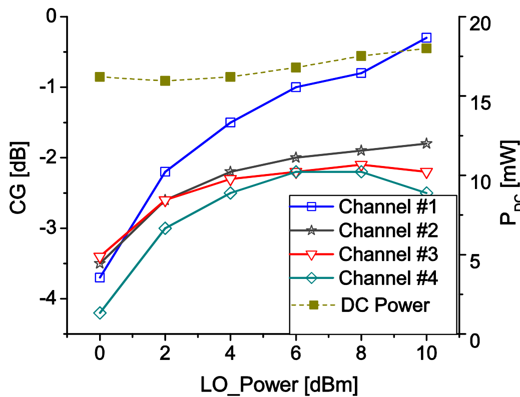


Fig. 123 Measured GC and PDC versus LO power and gate voltage.

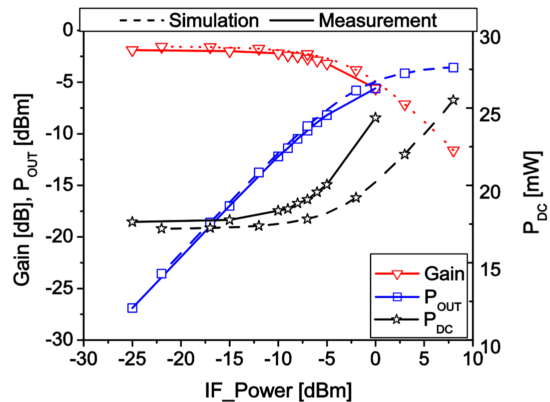


Fig. 124 Measured large signal performance at 60 GHz vs. IF power for channel No.2.

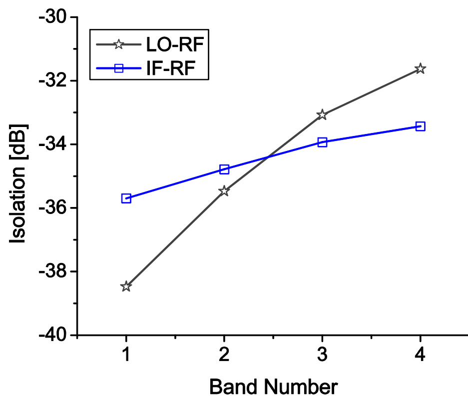


Fig. 125 Measured isolation for IEEE802.15.3c channels.

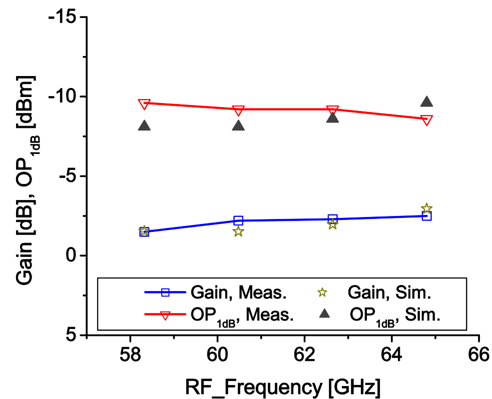


Fig. 126 Measured large signal performance for IEEE802.15.3c channels.

Table. 20 Performance Summary

Frequency band	57 GHz – 66 GHz
CG	-8 dB ± 1 dB
P_{sat}	-8 dBm ± 1 dB
P_{1dB}	-11 dBm ± 1 dB
PDC	11 mW (1.2 V)

5.1.3.2 Heterodyne Transmitter

The measured results of the complete transmitter show also a good agreement with the simulation. Fig. 127 and Fig. 128 show the small signal matching at the output terminal and the large signal performance of the second channel versus the simulated results. The complete transmitter consumes around 250 mW. For 1 dB less P_{OUT}, the power consumption can be decreased to less than 200 mW. Based on the mixer measurement, the LO power was selected at around 3 dBm. Fig. 129 presents the complete performance of the transmitter for all four channels. Furthermore, the transmitter results are summarized in Table. 21.

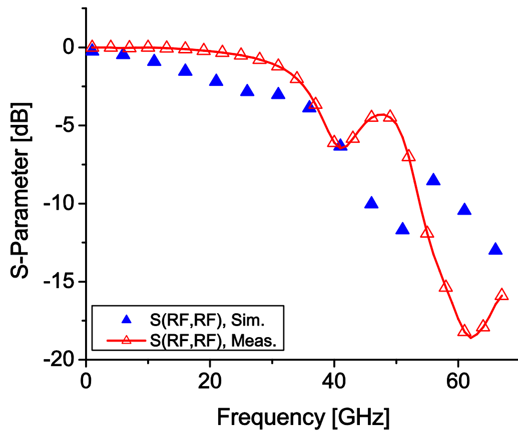


Fig. 127 S-parameter results.

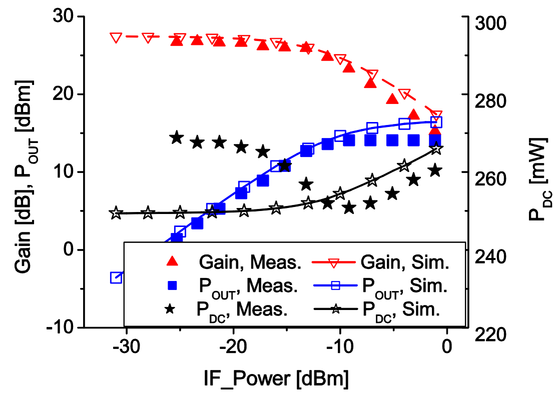


Fig. 128 Large signal performance at 60 GHz vs. IF power for channel No.2.

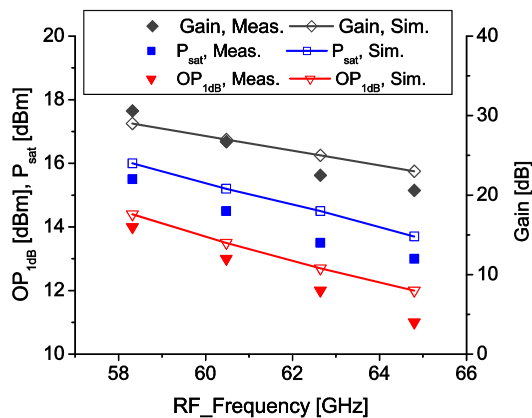


Fig. 129 Measured large signal performance for IEEE802.15.3c channels.

Table. 21 Performance Summary

Frequency band	57 GHz – 66 GHz
CG	31…21dB
P_{sat}	15.5…13 dBm
P_{1dB}	14…11 dBm
LO-RF Iso.	>45 dB
IF-RF+Image Iso	>45 dB
P_{DC}	250 mW (1.2 V)

5.2 OOK Transmitter

In recent years, different circuit topologies have been proposed for OOK transmitter front-ends. In these designs, either the modulator and the PA are separate components ([65] and [68]), or the modulator has been optimized for high output power performance ([66] and [67]). Fig. 130a presents the general schematic of the modulator designed in these works ([65]-[68]). Although these modulators have some differences in their topologies, they are all mainly based on the DC current (ID) switching of a single-ended or differential cascode amplifier. In [65] and [66], the gate voltage of the common gate transistor in the cascode amplifier was utilized to modulate the RF signal. Moreover, in [65], the cascode modulator was optimized as a PA. Although this technique reduces the chip size due to the gate impedance of the common gate transistor, it results in poor gain and power performance in the PA. In [66], the modulator was biased for minimum DC power consumption and was followed by a separate PA to improve the output power. This technique results in a better gain and output power (>0 dBm) but requirs a larger chip size. In order to improve the performance, a modulated current source and extra pMOS switch were also added to this circuit [66]. The pMOS switch in this design improved the ON-OFF transition by at least 80 ps in simulation. In [68]-[69], the modulator was designed to have high output power (1.5 dBm). In this design, the RF and DC paths are separated. The RF path includes two-stage C.S. amplifiers, while both amplifiers share the same DC current. This helps with the minimization of the DC current consumption but requires a higher drain voltage to improve the output power (1.8 V). Moreover, to separate the baseband circuitries from the RF circuitries, a quarter-wave length line at 60 GHz was utilized. Using these long lines in the matching circuits resulted in a larger chip size.

The other problem with these designs is the high frequency switching of the drain current (more than 3.3 Gbps in [67]). In these topologies (Fig. 130a), the BB signal switches the drain current (I_D) on and off at the bitrate frequency. Since the frequency of the BB signal (<10GHz) is much lower than the RF signal (60 GHz), much larger RF ground capacitors (Fig. 130a) are needed on-chip to isolate the biasing circuitry from the BB signal. If the RF GND cannot isolate the BB signal, the impedance seen from the biasing circuitry can affect the I_D waveform which can result in RF leakage to the output in the OFF state and a lower signal level in the ON state. This condition deteriorates as the transistor size increases, which limits the maximum achievable P_{OUT} of this topology (a maximum of 1.5 dBm in [68]).

In order to overcome the above mentioned problems, the topology of the OOK was modified. In the new topology, the modulator is completely integrated in the matching network of the PA (Fig. 130b). In this design, transistor T_2 is used as a passive shunt switch. For a BB equal to 1, the T_2 switch connects the RF path to ground. This stops the RF signal from reaching the PA (T_1 transistor) and vice versa for a BB equal to 0. It must be considered that, in this design, the T_2 transistor is part of the PA-matching network. This means that, in an ideal case, for a BB equal to 0 the input-matching of the PA must have a reflection coefficient near 0 and, for a BB equal to 1, a reflection coefficient near 1.

In this topology, the modulator consumes no DC power and the drain current (I_D) of the PA is only a weak function of the BB signal. This helps to increase the T_1 transistor size independently from the modulator performance, so as to improve the output power of the transmitter. Finally, in order to improve the gain and the isolation of the transmitter, a cascaded structure with two-stages was utilized (Fig. 130c).

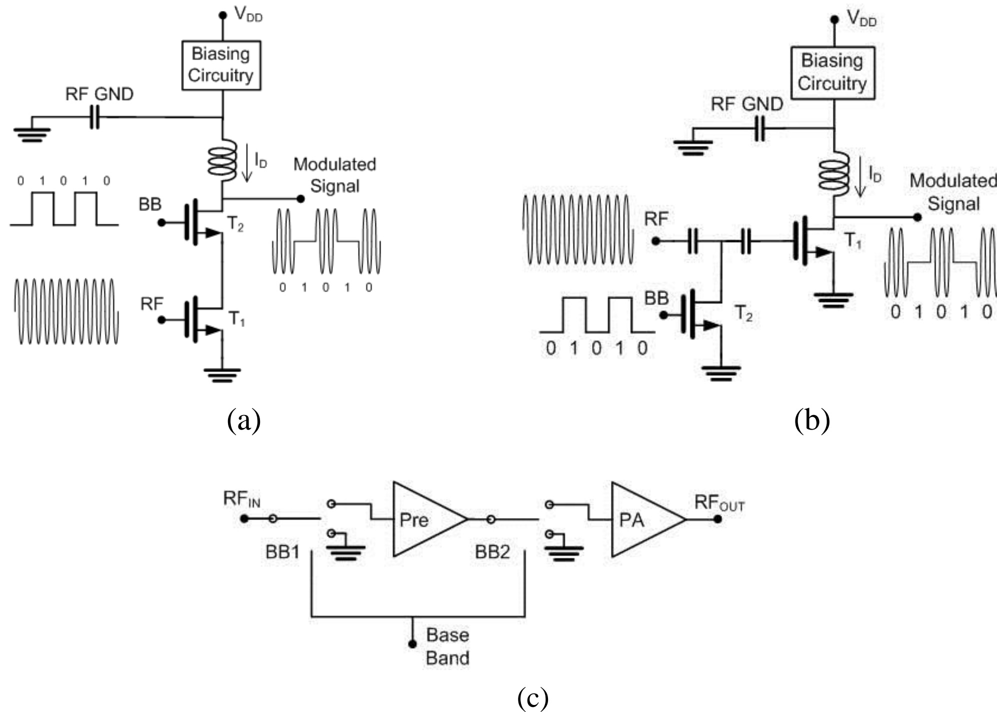


Fig. 130 a) Conventional OOK modulator. b) Proposed OOK Tx circuit. c) OOK transmitter.

In this work, an ON-OFF shift keying transmitter front-end for 60 GHz wireless communication is designed, realized and measured. The transmitter is realized in 90 nm LP CMOS technology with a small chip size of 0.38 mm^2 and DC power consumption of only 36 mW. In order to enhance the transmitter performance, a novel modulator topology is implemented. In this design, the modulator does not consume any DC power and is completely integrated into the matching network of the power amplifier. The power amplifier has been also designed for high gain and high output power. With this design, more than 9 dB gain and 8 dBm P_{sat} with 10% PAE was measured at 61 GHz. By using this transmitter in a wireless system with an external LO signal and horn antennas, data communication with bitrates higher than 6 Gbps over a 4 m distance were measured.

5.2.1 Link Budget

Due to the absence of a peak power-to-average ratio (PAPR) requirement in the OOK system, a very high power PA is not a requirement for the OOK system. The system plan of an OOK TRx is presented in Fig. 131. As mentioned before, based on current publications, the expected receiver noise figure is around 7 dB [91] and the minimum required SNR for the base band circuitry is around 15 dB [93] (for BER < 10^{-7}). Based on these results, and in considering the system plan details (Fig. 131), at 4 m distance the minimum required P_{OUT} from the PA is around 3 dBm.

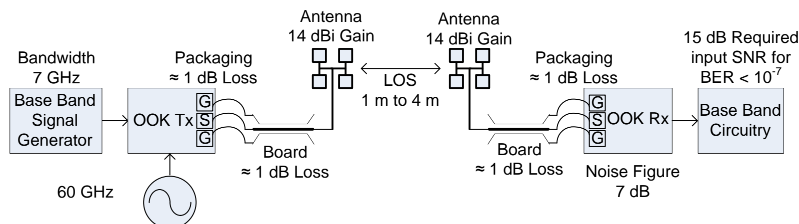


Fig. 131 Link-budget for the OOK system.

5.2.2 Circuit Design

As the modulator (T_2 in Fig. 130b) is part of the PA-matching networks, the design of the PA and modulator must be done together. In this part, first of all, the design of the optimum modulator based on this technology is introduced. Next, and based on these results, the optimum PA is designed. All the optimizations were performed based on the requirements calculated in the previous section.

5.2.2.1 OOK Modulator

The modulator schematics are shown in Fig. 132. The C_1 capacitors and L_1 inductors are used to avoid RF coupling between the two PA stages. The L_1 inductors have been designed based on a SCTL (Section 2.3.2) to connect the BB signal from the pad structure to the gate of the T_2 transistor with minimum insertion loss.

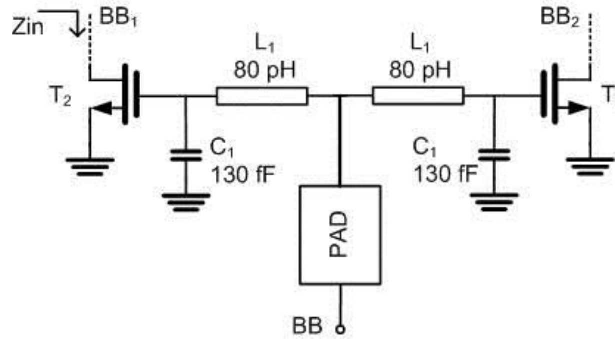


Fig. 132 Schematic of the OOK modulator.

To select the optimum size of the T_2 transistors, different characteristics must be studied. These characteristics include the rise and fall times and the impedances (Z_{IN} in Fig. 132) in ON and OFF conditions (BB equal to 1 and 0). Fig. 133 and Fig. 134 present the simulated results of Z_{IN} versus T_2 size at 60 GHz. If the NoF and the width increase, Z_{IN} decreases. This is desirable in the ON condition (BB equal to 1) as a very low impedance is required. However, in the OFF condition (BB equal to 0), this can complicate the input-matching network design. Based on these simulated results for the NoF between 15 to 20 and a width of 3 µm to 4 µm, an appropriate Z_{IN} can be achieved. In this transistor size range, the impedance Z_{IN} is between 10 Ω to 20 Ω in the ON state and 80 Ω to 100 Ω in the OFF state.

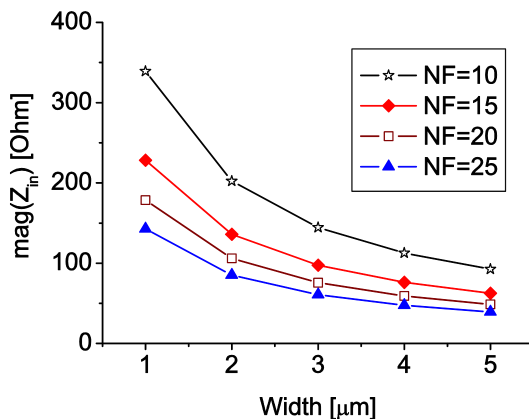


Fig. 133 Z_{in} vs. T_2 size for BB=0.

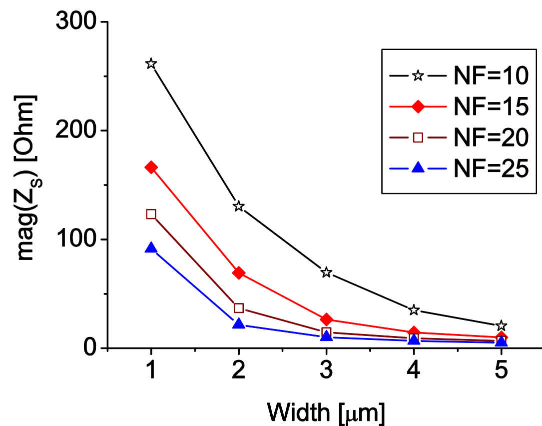
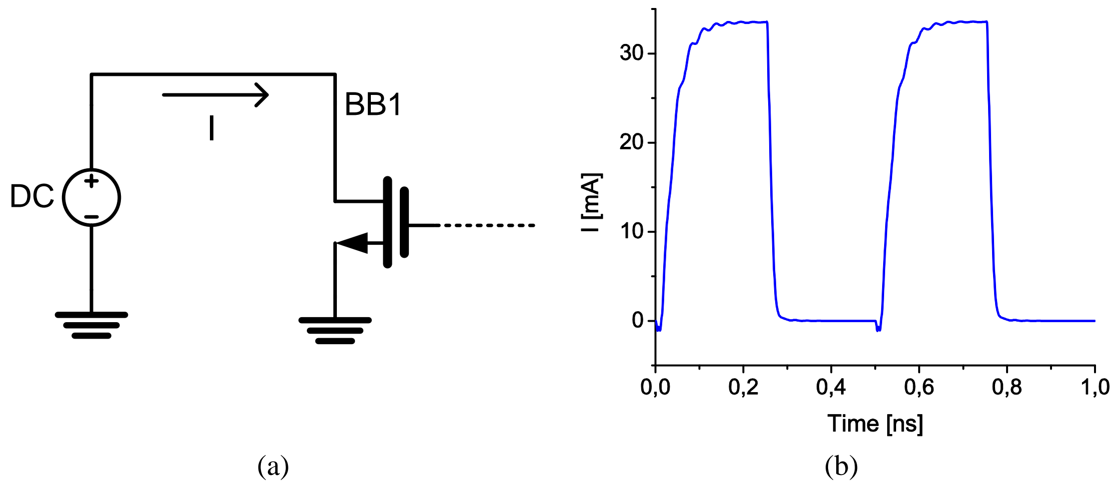


Fig. 134 Z_{in} vs. T_2 size for BB=1.

The ON and OFF transient times of the T_2 transistors define the maximum bitrate of the modulator. In this transmitter, the maximum targeted bitrate is 10 Gbps. This means that the summation of the rise and fall time must be less than 100 ps in order to avoid any vertical eye-diagram closing. In order to calculate the ON-OFF transient time of the switch, a transient simulation was performed (Fig. 135a) and the fall and rise times were calculated from Fig. 135b. It must be considered that the voltage swing at the gate of the transistors is a determining factor of the transistor speed. The swing amplitude is a function of the impedance seen at the gate of the transistor. In this case, to correctly simulate the transient switching time, the switch core, matching circuits (L_1 and C_1) and feeding structures are considered in the simulation.

Fig. 136 presents the simulated results of the rise and fall times versus the transistor sizes. The transistor size (total width) between 60 µm to 100 µm shows the minimum transient time of around 90 ps (Table. 22). Based on these results (Fig. 133 to Fig. 136), the NoF equal to 15 and a width equal to 4 µm were selected.



(a) (b)

Fig. 135 OOK switch transient simulation. a) Test bench. b) Drain current of the switch.

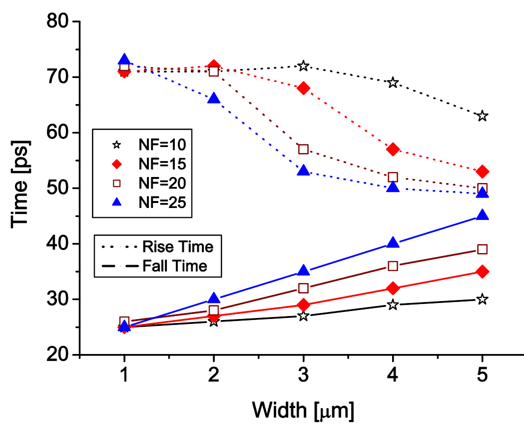


Fig. 136 Rise and fall time between BB=1 and BB=0 for various T2 sizes.

Table. 22 Total transient time (rise time + fall time) in pico-second for different W and NoF (Simulation)

W / *NoF*	**10**	**15**	**20**	**25**
1 µm	96	96	98	98
2 µm	97	99	99	96
3 µm	99	97	***89***	***88***
4 µm	98	***89***	***88***	***90***
5 µm	93	***88***	***89***	94

5.2.2.2 OOK Power Amplifier

The two-stage PA is designed for maximum P_{OUT} and high gain. As discussed in the previous section, the OOK modulation requires no back-off power and the linearity (OP_{1dB}) of the PA does not play a determining role in the performance of the transmitter. As such, the PA can be designed for high P_{sat} and gain [12]. For this purpose, the first stage is designed for high gain while the second stage is designed for high P_{sat}. The design of each stage includes transistor size and biasing condition selection and matching network design. In this design, all the matching circuits are designed with the help of SCTL (Section 2.3.2) [10].

5.2.2.2.1 Power Stage

Fig. 137 presents the power stage of the power amplifier. The output of the power stage was matched at the saturation level for the maximum P_{sat} while its input was matched to the output of the pre-amplifier. The transistor size was selected based on the discussion in the previous chapter (Section 4.1.1). Based on the discussion in the link budget section (Section 5.2.1), a P_{sat} at around 3 dBm is enough for indoor point-to-point communication. As shown on section 4.1.1, this power is much lower than the maximum power, which can be yielded (13 dBm) from a transistor with this technology. In this case, the transistor size can be optimized for other factors like PAE, G_{MAX} and a high quality factor-matching network.

As the matching network, the interconnections and antennae suffer from losses a higher transistor P_{OUT} is required to ensure the correct Tx performance. In this case, by selecting a transistor width of around 50 µm, the maximum P_{OUT} at around 9 dBm can be achieved. Meanwhile this transistor size is appropriate for matching-network design (Section 4.1.1.3). The finger width, NoF and current density of the power stage can be selected from Fig. 96. In order to achieve the maximum of P_{OUT} from the power stage, current densities more than 400 µA/µm should be selected. Simulating the graph in Fig. 96a for this current density shows 14 NoF and 3.5 µm finger width for a stability factor of around one.

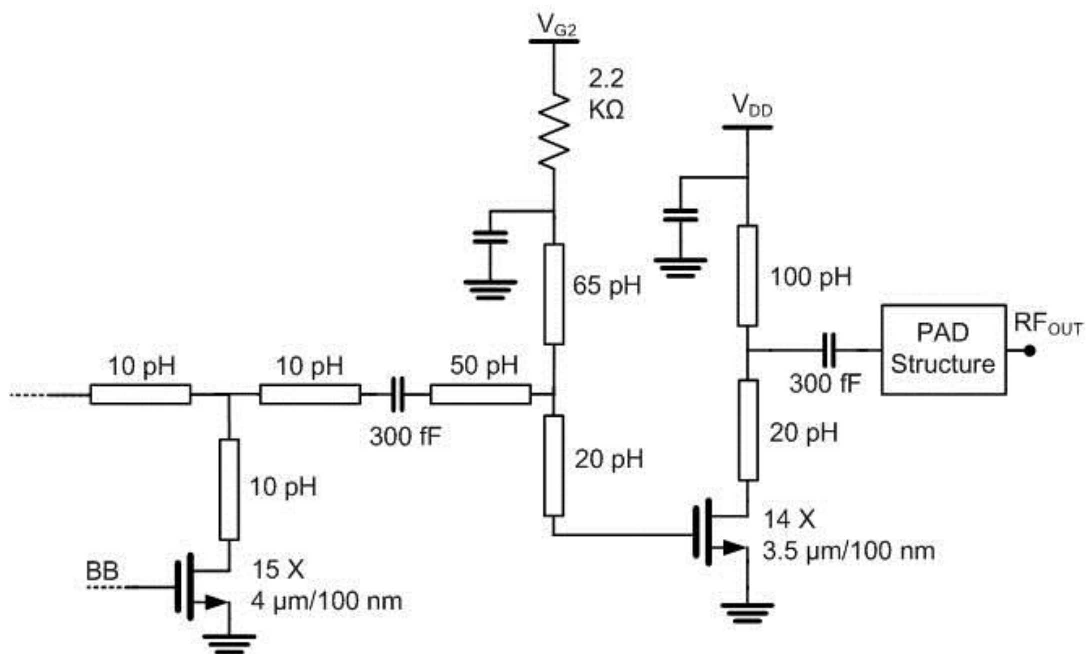


Fig. 137 Schematic of the PA.

Based on this transistor size and current density, the optimum load and source matching networks are designed. These designs are performed with the help of source and load-pull simulations. The parasitic elements of the OOK modulator have also been considered in this design. Fig. 138 presents the source- and load-pull simulations of the power stage with the matching networks at 60 GHz and at around P_{sat} level (with 3 dBm LO power).

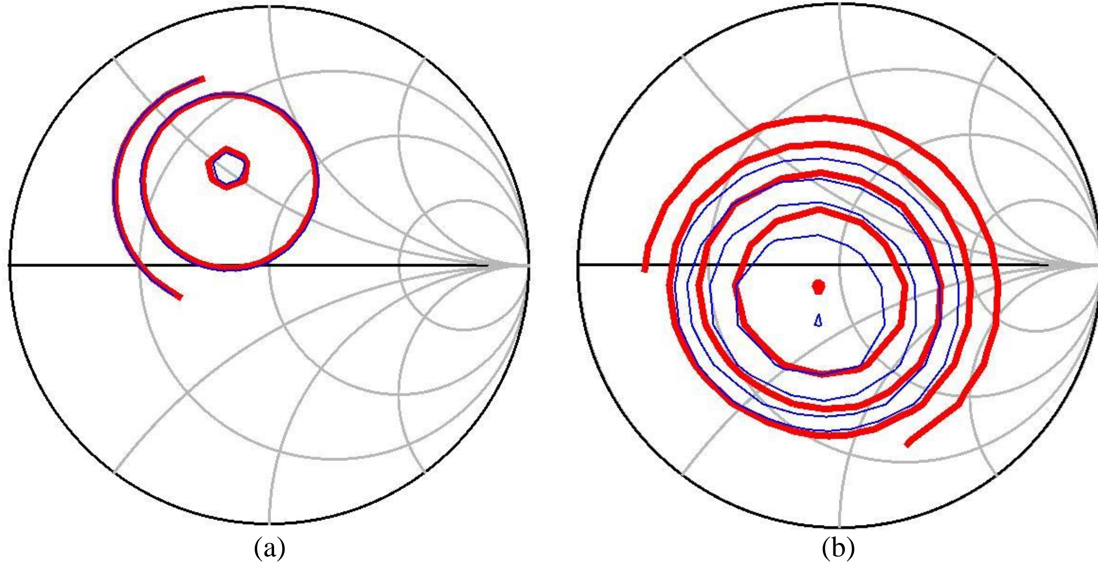


Fig. 138 a) Simulated source pull and b) load pull of the PA at 60 GHz and V_{DD}=1.2 V. Red: Power with 0.5 dB step. Blue: PAE with 2% steps @P_{sat} and 0.2% @ small signal.

Fig. 139 presents the simulated large signal performance of the power stage. Due to the losses of the output pad structure (around 1 dB [10]) and the matching network, and also because of the large signal matching of the amplifier, the gain of the power stage is around 2.5 dB less than the G_{MAX} of the transistor. Finally, by matching the output of the power stage at the saturation level, a high linearity and P_{sat} are achieved. Although linearity does not play any role in the OOK performance, high linearity means high gain near the saturation power. The detailed simulated performance of the PA is also presented in Table. 23.

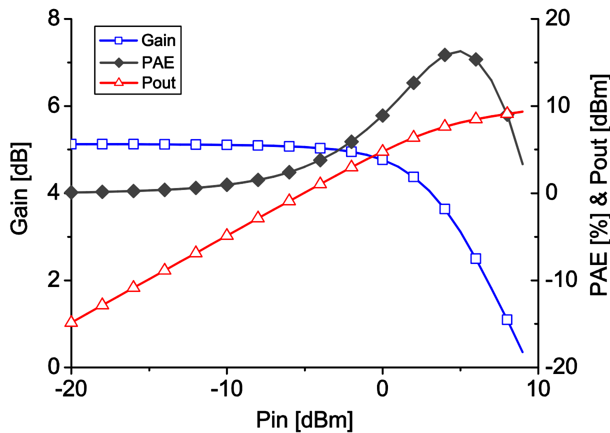


Fig. 139 Simulated large signal performance of the power stage.

Table. 23 Power stage large signal performance (Simulation)

V_{DD}	1.2 V
V_G	1 V
I_{DD}	20 mA
P_{sat}	9 dBm
OP_{1dB}	7 dBm
Gain	5 dB
PAE_{Max}	16%

5.2.2.2.2 Pre-Amplifier

To boost the PA small signal performance, the first stage of the transmitter is optimized for maximum gain. In this case, the current density and the transistor size are selected for maximum gain and the matching networks are designed at the small signal level.

The optimum current density and transistor size are also selected based on the discussion in the previous chapter (Section 4.1). Based on this discussion, with smaller transistor sizes and lower current densities, higher gain can be achieved. However, other factors like stability and P_{OUT} can be limited. As discussed before, smaller transistor sizes and lower current densities result in a lower stability factor and P_{OUT}. The lower stability factor (less than 1) can increase the chance of the PA oscillation. Although this can be tolerated to some extent due to the matching network losses, the mismatches between the pre-amplifier and the power stage and low stability factor can result in an internal oscillation, which can drive the pre-amplifier output into saturation and cause DC current instabilities. Further, the low P_{OUT} of the pre-amplifier can affect the large signal performance (gain at P_{sat}, linearity and PAE) of the power stage and the complete PA.

The power stage simulation shows around 5 dB small signal gain. This means that the input P_{1dB} of the power stage is 4 dB (as the gain in OP_{1dB} is 1 dB less than the small signal gain) lower than the OP_{1dB} of the power stage. In this case, the OP_{1dB} of the pre-amplifier can be 4 dB lower than the power stage. In this design, in order to have a margin, the pre-amplifier is optimized for 2 dB lower OP_{1dB}. As discussed on section 4.1.1.3, the optimum transistor size for 50 Ω-matching is around 40 µm to 50 µm. This is around the same transistor size as has been selected for the power stage. In this case, the current density can be down scaled instead of the transistor size for the desired power performance. In this design, the current density of the pre-amplifier was selected as around 1.7 times (around 2.3 dB) less than the power stage current density at around 230 µA/µm. The drain current of the transistor, biased at class AB, increases at around the saturation level. For this reason, the current density of the pre-amplifier is selected at a lower level than the design target (230 µA/µm instead of 250 µA/µm).

In order to select the correct width and NoF for the pre-amplifier transistor, the graph in Fig. 96a must be simulated again with the new current density. The lower current density means a lower stability factor for the same transistor size. In this case, the width of each transistor finger can be selected as being larger than the power stage in order to compensate the stability factor decrease. In this design, 4 µm for the finger width and 12 NoF were selected.

Moreover, in this design and in the design of the power stage, the optimization of the PA for the maximum PAE was neglected. As shown in Fig. 94b, by selecting 50 µm transistor width the maximum achievable PAE (just from a transistor without matching networks) is around 18%, which is around 3% less than the maximum PAE.

Finally, the input and output of the pre-amplifier were matched with the help of source- and load-pull simulations. To improve the small signal performance, the matching was performed at a lower power level than the power stage (5 dB lower, at -2 dBm). Fig. 140 presents the source-pull and load-pull simulations of the pre-amplifier at 60 GHz. As is shown in Fig. 140a and b, the input is matched at 50 Ω while the output is matched to the input of the power stage.

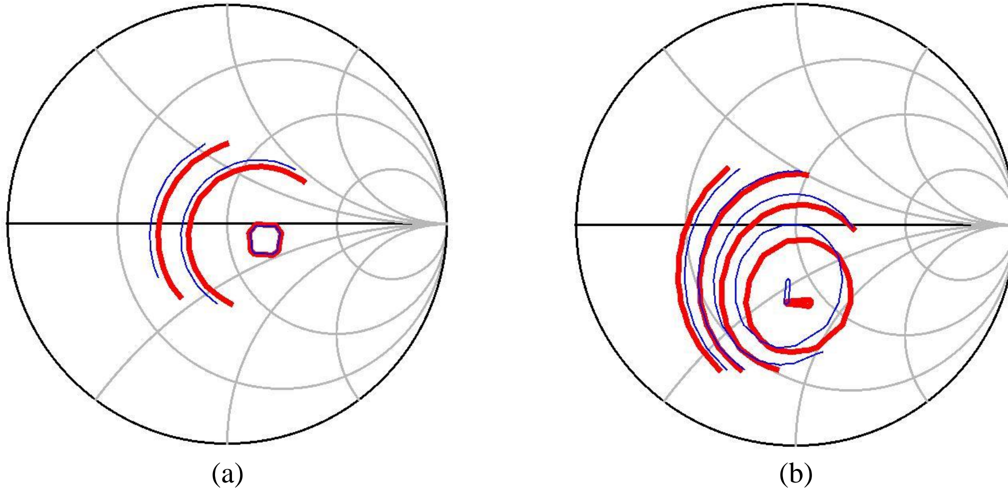


Fig. 140 a) Simulated source pull and b) load pull of the PA at 60 GHz and V_{DD}=1.2 V.

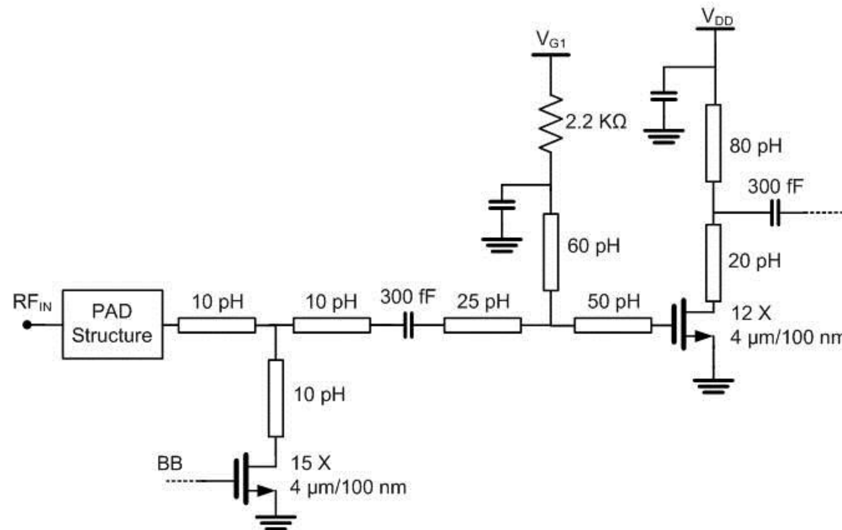


Fig. 141 Schematic of the pre-amplifier.

The complete schematic of the pre-amplifier is presented in Fig. 141. All the matching networks are realized with SCTL (Section 2.3.2) for minimum losses. In addition, the values of the matching network inductance are selected in such a way that the inductances can be easily realized on-chip with this kind of transmission line. The large signal performances of the pre-amplifier are presented in Fig. 142 and Table. 24. As mentioned above, by decreasing the gate voltage of the pre-amplifier from 1 V to 0.8 V, the drain current was decreased to 11 mA in order to increase the total PA efficiency. As mentioned earlier, due to current increase in class AB amplifiers, the OP_{1dB} of the pre-amplifier is only 1.5 dB less than the power stage. Furthermore, the saturation power of the pre-amplifier is the same as the power stage at around 8 dBm, but with less power gain (at the saturation level). The gain could only be improved by around 0.3 dB and, due to the small signal matching of the pre-amplifier, the PAE of the pre-amplifier is almost 2% less than for the power stage.

The simulated results of the power stage and pre-amplifier presented here are for the conjugate-matching condition, where the output of the pre-amplifier and the input of the power stage are connected to their conjugated matched impedance. As shown in the next section in Fig. 145, this PA in the simulation level achieves around 9 dB gain.

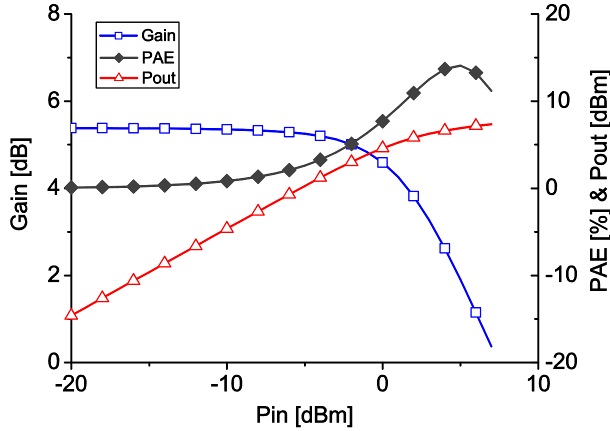


Fig. 142 Simulated large signal performance of the pre-amplifier at 60 GHz and V_{DD} = 1.2 V.

Table. 24 Pre-amplifier stage large signal performance (Simulation)

V_{DD}	1.2 V
V_G	0.8 V
I_{DD}	11 mA
P_{sat}	8 dBm
OP_{1dB}	5.5 dBm
Gain	5.3 dB
PAE_{Max}	14%

5.2.3 Experimental Results

After the design and optimization of each part, the final Tx was realized. Fig. 143 presents the chip micrograph of the realized Tx. The complete chip, including pads, occupies 0.38 mm^2. To completely characterize the Tx small signal, large signal and time domain (data modulation and transmission), simulations and measurements were performed. All the characterizations were done on-chip. In all the above simulations, the S-parameter models for passive structures (extracted with EM simulation) were utilized. The use of S-parameter models in time-domain simulations can result in longer simulation times and, sometimes, in simulation conversion problems. This can be a serious problem in complicated circuits like PLLs. However, as the circuit structure of the Tx designed in this work is quite simple and the size of the total chip is quite small, this problem does not have a significant effect on the time domain circuit simulation.

In this section, each simulation and measurement category is presented. By comparing the measured and simulated results in each section, the validity of the models and the design techniques are verified. All the simulations and measurements presented in this section are performed under 1.2 V drain voltage and 30 mA total current.

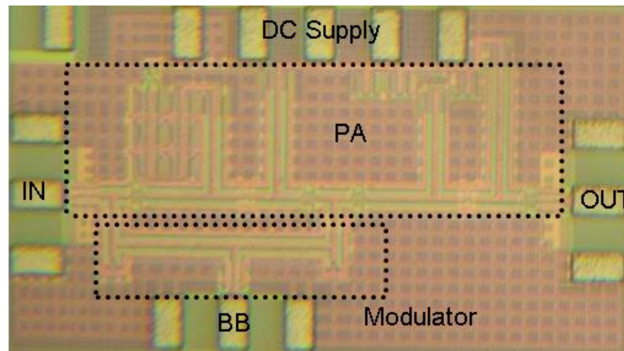


Fig. 143 Chip micrograph (0.38 mm^2 with pads)

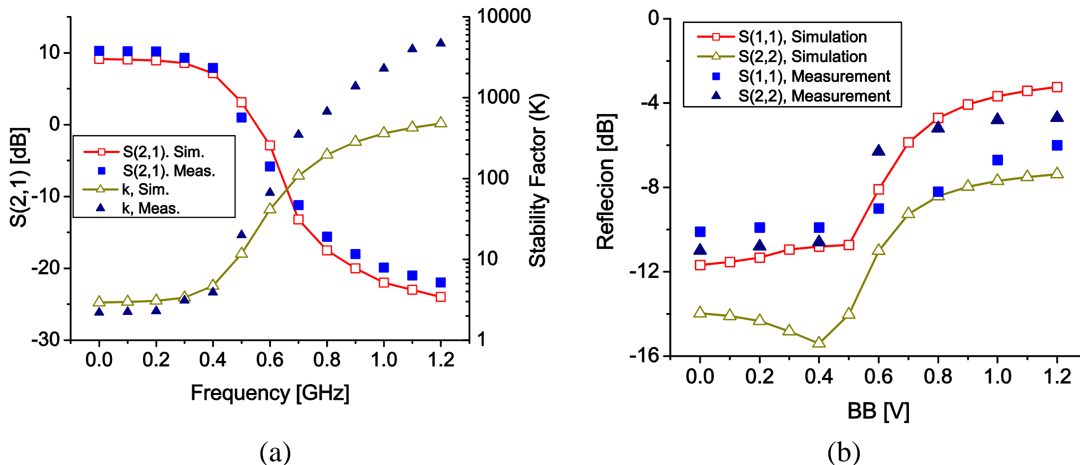
5.2.3.1 Small Signal

The main small signal performances are gain, stability and terminal matching. It should be considered that, as in the OOK Tx, the BB signal only switches the LO signal on and off, the gain of the OOK Tx is calculated between the LO and RF paths. In this case, for a BB equal to 0, the BB pad is connected to ground while, for a BB equal to 1, it is connected to 1.2 V. In addition, the measurements are performed in steady state conditions. Later, in section 5.2.3.4, the CG of the modulator with linear modulation techniques (QPSK, etc.) is calculated.

In this section, these small signal measurements are carried out for various LO frequencies and DC voltages at the BB path. Although the circuit has been designed for the desired performances at the BB equal to 0 and 1, the investigation of the conditions between these two cases can give us a better understanding of the circuit's performance. Fig. 144 presents the gain, stability and reflections at both the input and output ports versus the BB at 60 GHz. As can be seen (Fig. 144a-b), the PA performance is relatively constant for BB DC voltages of less than 0.4 V and more than 1 V. This demonstrates the good performance of the Tx for even smaller voltage swings at the switch inputs.

The gain versus BB (Fig. 144a) measurement shows good agreement with the simulation, although for some points a higher gain was achieved in measurement, which might be mainly due to frequency shifts due to process variations. Furthermore, Fig. 144a shows a stability increase by increasing the BB voltage. As expected, the minimum stability occurs for a BB equal to 0, whereby at 60 GHz a stability factor better than 2 is achieved. Finally, and as shown in Fig. 144b, the terminal matching deteriorates with an increase of the BB voltage. This is quite desirable, as higher mismatches at a BB equal to 1 mean less radiated power and, hence, a better dynamic range between the ON and OFF cases.

Based on the above measurements (Fig. 144), the OOK performance region can be divided into three regions. In the first region (a BB less than 0.4 V), the switch is completely off and the Tx transmits the 60 GHz signal with its maximum output power. In the second region (a BB between 0.4 V and 1 V), the Tx is between the ON and OFF conditions. In this region, the gain of the Tx (between the LO and RF paths) decreases almost linearly as the BB voltage increases. Finally, in the third region (a BB more than 1 V), the gain is relatively low and almost no power radiates from the Tx.



(a) (b)

Fig. 144 Measurement vs. simulation: a) and b) Small signal performance vs. BB voltage.

As a final step in the small signal measurement, the Tx was characterized versus frequency. Fig. 145 compares the simulated and measured small signal gain of the PA for both BB states (ON and OFF). Around 9 dB gain and 30 dB ON-OFF isolation at the small signal level was measured at around 60 GHz. As shown later, the isolation deteriorates slightly by driving the PA into deep saturation. The input (LO pad) and output (RF pad) reflections for a BB equal to 0 are shown in Fig. 146a, with better than 10 dB matching at around 60 GHz. Finally, the measured stability factor from 50 GHz to 70 GHz shows the unconditional stability of the circuit for both BB cases (Fig. 146b).

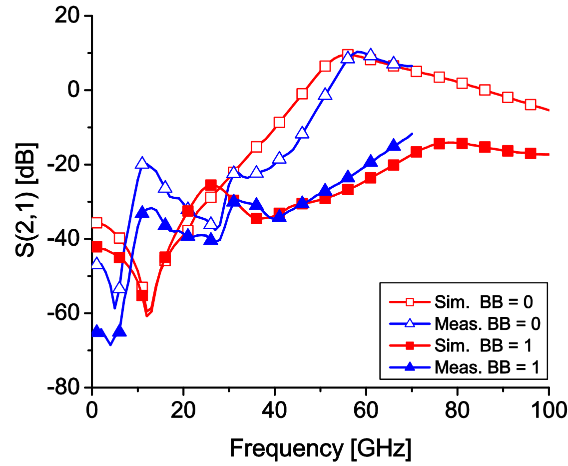
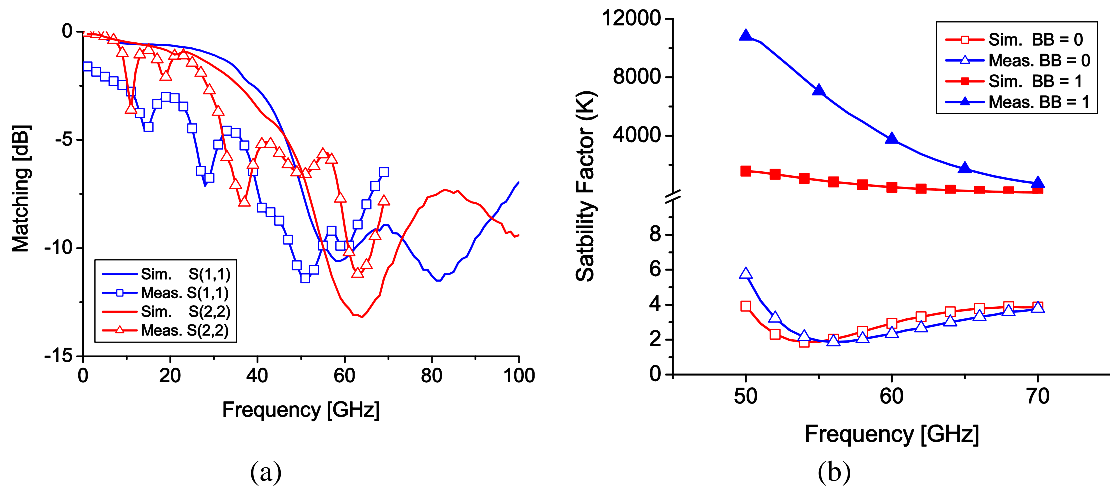


Fig. 145 Measured and simulated small signal gain.



(a) (b)

Fig. 146 Measured and simulated: a) matching. b) stability factor.

5.2.3.2 Large Signal

In order to justify the large signal design techniques, the performance of the complete Tx was measured for various input powers, LO frequencies and BB signals. In these measurements, the main large signal characteristics, including P_{OUT}, power gain, PAE and ON-OFF isolation, are characterized.

As mentioned in the previous section, the small and large signal performances of the PA are functions of the BB signal DC biasing. In this section, the behavior of the PA versus the BB biasing voltage is also investigated in order to find the optimal biasing for power performance. Fig. 147 presents the measured and simulated results of the P_{OUT} versus the BB biasing voltage. As expected, the large signal performance shows the same tendency as the small signal performance (Fig. 144a).

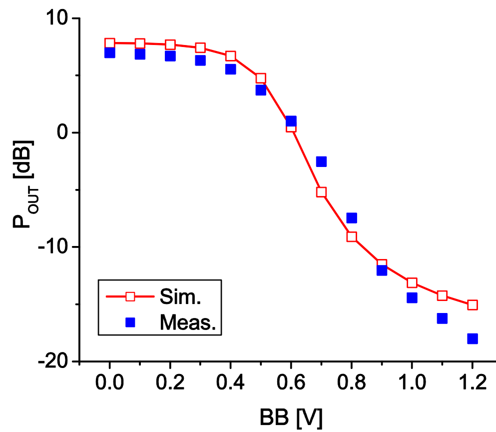


Fig. 147 Measured and simulated P_{OUT} vs. BB biasing voltage.

The power gain of the Tx at 60 GHz versus the input power for both BB states is shown in Fig. 148. The power gain measurement shows 1 dB less gain than the small signal measurements, which is mainly due to calibration errors. The Tx achieved 8 dBm P_{sat} and better than 8 dB power gain. In this design, the isolation shows around a 3 dB decrease near P_{sat} in comparison with the small signal level. With 8 dBm P_{OUT} from the PA, an ON-OFF isolation higher than 27 dB was measured. The detailed performance over the frequency is presented in Fig. 149.

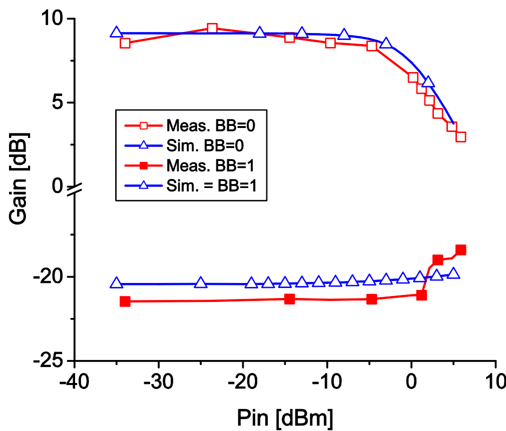


Fig. 148 Meas. vs. sim. gain of the PA for both BB states.

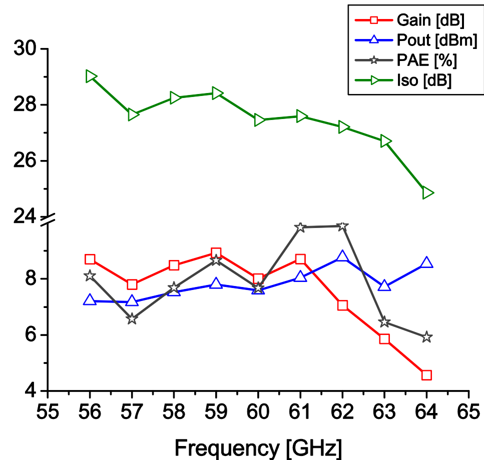


Fig. 149 Measured large signal performance of the PA over frequency.

5.2.3.3 Time Domain OOK Modulation

To further guarantee the modulator switches and PA design procedure, time domain simulations were performed. The Tx was simulated with different BB bitrates to identify the maximum Tx speed without EYE diagram closing. The EYE diagram closing happens as the bitrate exceeds the rise and fall times of the Tx. As a result, the P_{OUT} of the Tx decreases as the bitrate further exceeds the rise and fall times of the Tx. In this case, the rise and fall times must be calculated from the point where the BB signal change at the input to the point where the modulated signal reaches the steady state condition at the output of the Tx.

Fig. 150 presents the output of the Tx modulated with a 400 Mbps BB signal. By zooming to the transient conditions, the rise and fall times can be calculated (Fig. 150b-c). Based on this calculation, the total transient time is around 100 ps (50 ps rise time and 50 ps fall time). These values agree well with the simulated results of the modulator alone (Section 5.2.2.1). Furthermore, this simulation shows the minor effect of the PA on the rise and fall times of the signal. This is mainly due to the small transistor sizes of the power stage and pre-amplifier as well as the high f_t and f_{max} of the amplifying transistor under these biasing conditions.

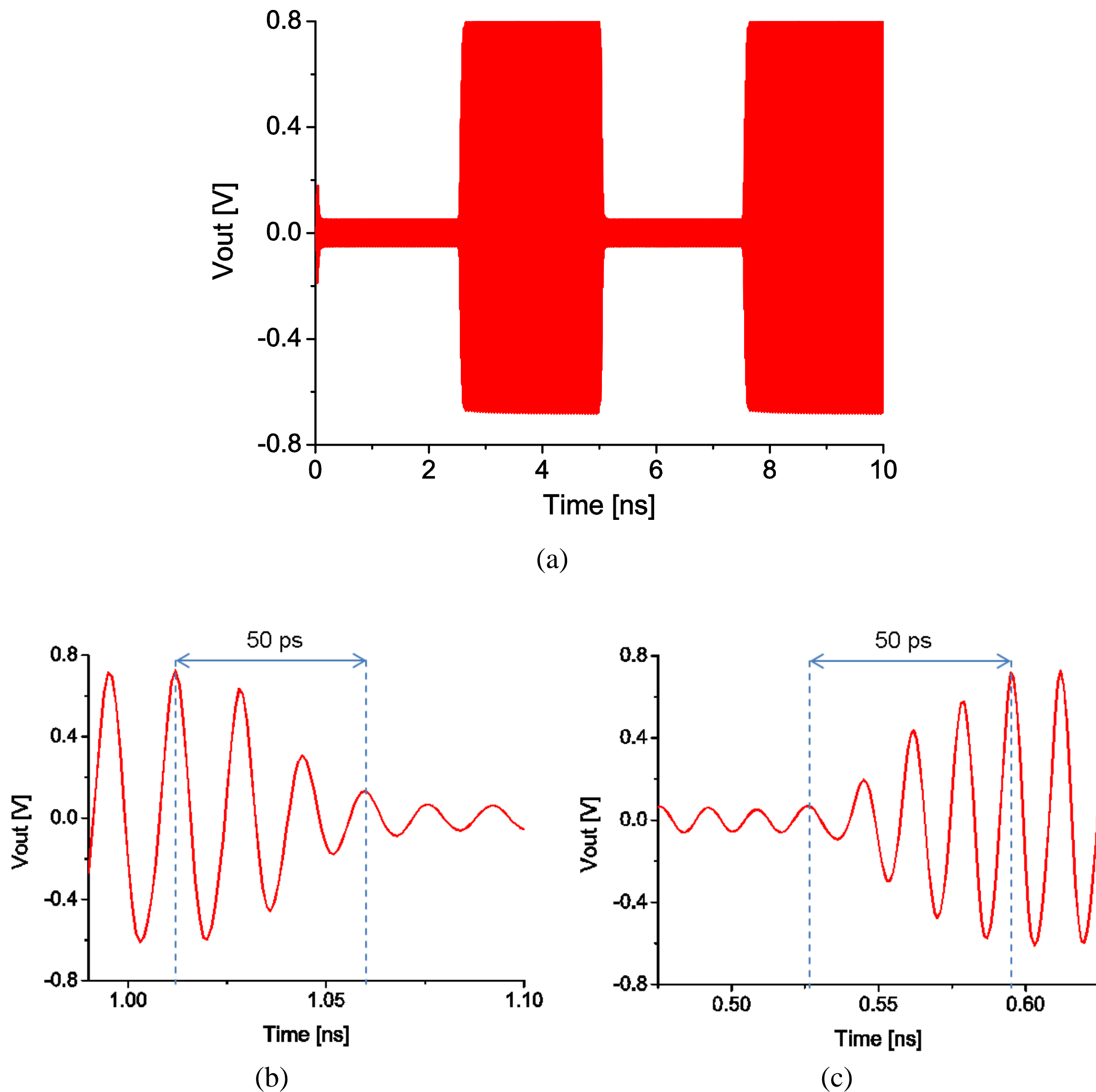
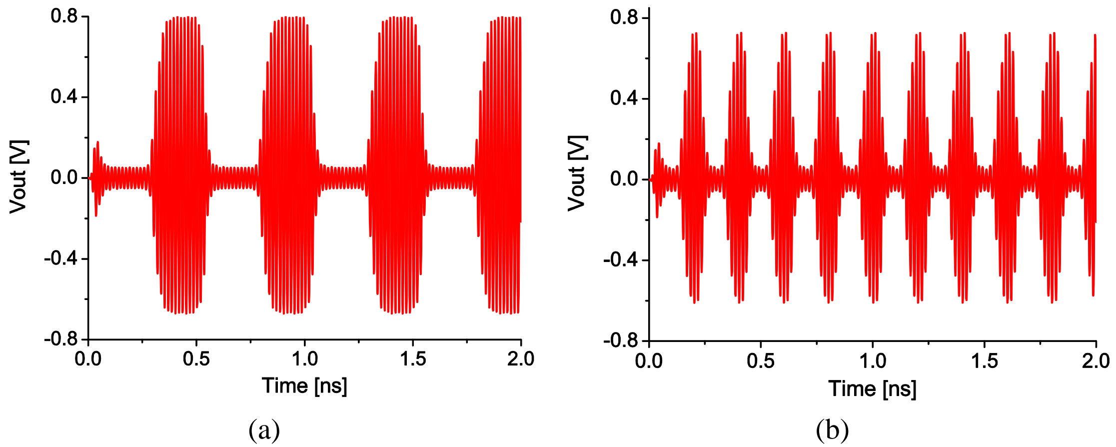


Fig. 150 a) The output of the Tx modulated with 400 Mbps. b) Rise time. c) Fall time.

An approximately 50 ps rise and fall time mean that the maximum bitrate, for which the P_{OUT} does not decline, is around 20 Gbps. This is higher than the required OOK bitrate considered in the link budget calculations (Section 5.2.1). Fig. 151 presents higher bitrate simulations with the designed OOK Tx. As can be seen, the amplitude of the Tx signal remains constant as the bitrate increases from 400 Mbps (Fig. 150a) to 4 Gbps (Fig. 151 a). Nevertheless, by further increasing the bitrates to 10 Gbps (Fig. 151b) the amplitude declines. This is mainly due to a low pass filter effect of the BB path matching network, which further delays the transistor switching.



(a) (b)

Fig. 151 The output of the Tx modulated with: a) 4 Gbps. b) 10 Gbps

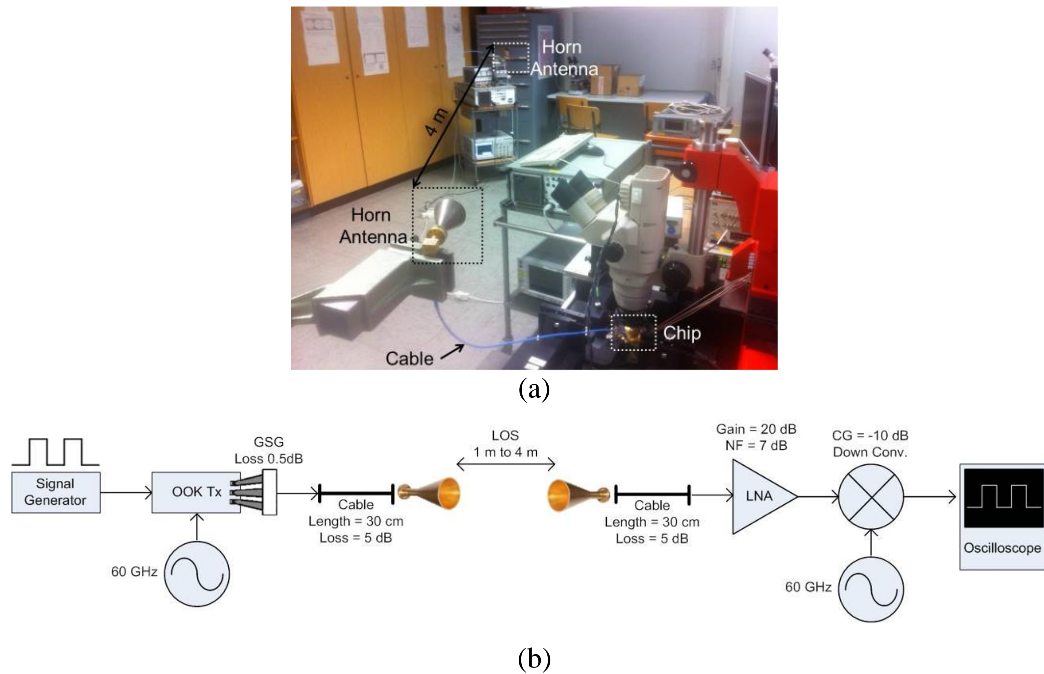
Although the above simulated results show the feasibility of high bitrate data transmission with the help of this OOK Tx, the maximum bitrate of the wireless communication can decline due to other problems during measurement. These problems can include the bandwidth limitations of the antenna and the TRx-antenna interconnections, and multipath and receiver limitations. As the OOK modulation suffers from bandwidth inefficiency, any bandwidth limitation of any component in the TRx path can cause bitrate decline. But the multi-path can be tolerated as long as the time differences between the paths are much smaller than the bit period.

To test this Tx in a wireless data communication system, a measurement setup was built (Fig. 152a). As shown in Fig. 152b, the setup includes local oscillators, horn antenna at both the transmission and reception paths with 25 dBi gain, a LNA with a 7 dB noise figure and 20 dB gain, a down-converter mixer with 10 dB conversion loss, and an oscilloscope with a 40 GS/s sampling rate. The output of the Tx and horn antennae is connected via a probe and a cable. This adds an extra 5.5 dB loss (probe 0.5 dB to 1 dB and cable 4.5 dB to 5 dB loss at 60 GHz) at the output of the Tx. By using a waveform generator, a periodic 0 and 1 bit sequence signal was generated.

The receive path was installed completely on a wheeled table so as to measure the transmitted signal at different path lengths from 1 m to 4 m (limited by the room size). In addition, and as mentioned earlier, one of the advantage of the OOK TRx in comparison with the normal TRx is the absence of a requirement for signal synchronization in the receiver path. This allows us to have two independent signal generators for Tx and Rx.

With the help of this measurement setup different bitrates at different distances were measured. Due to the lack of a high data-rate pseudo-random signal generator, a square wave signal generator was utilized to generate the sequence of 0 and 1 bits. The EYE-diagrams of the received signal for 4Gbps and 6 Gbps bitrates at 2 m and 4 m distances are presented in Fig. 153. As expected, the higher bitrates

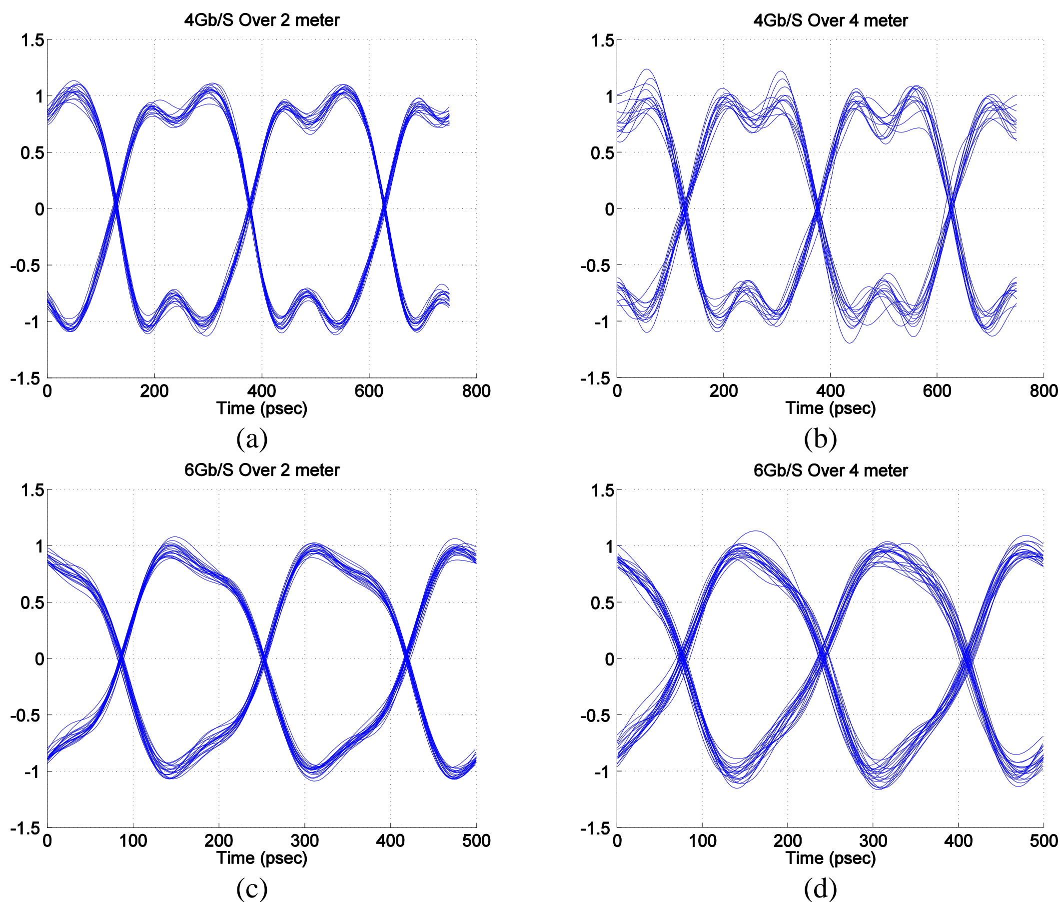
demonstrate a smaller EYE-diagram in the receiver due to the bandwidth limitations of the TRx components. Furthermore, increasing the Tx and Rx distance results in a lower SNR in the receiver and, hence, a less clear signal.



(a)

(b)

Fig. 152 Wireless communication set-up. a) Photo. b) Components.



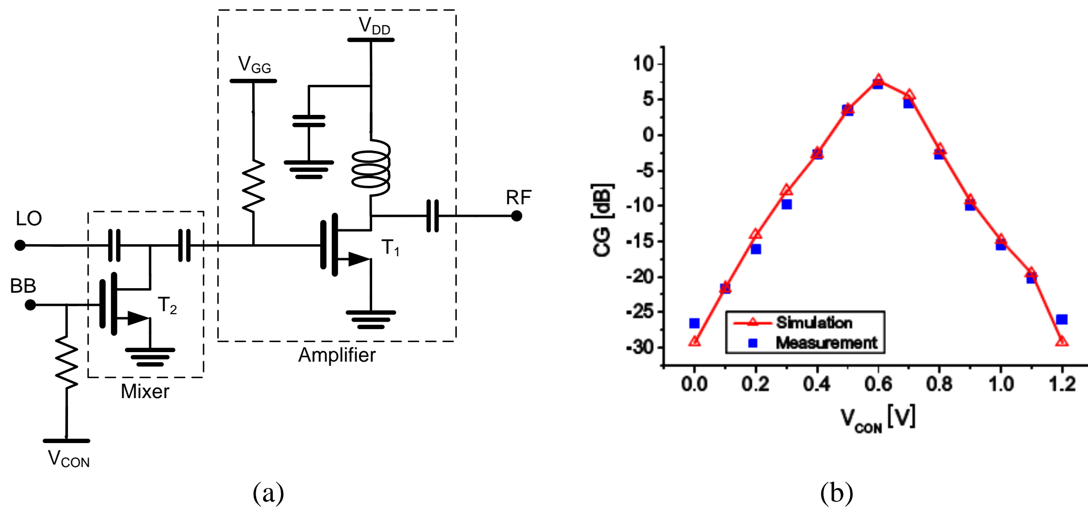
(a) (b)

(c) (d)

Fig. 153 Measured EYE-diagrams of wireless data communication over 2 m and 4 m distances. a&b) 4 Gbps. c&d) 6 Gbps.

5.2.3.4 Linear Modulation – Homodyne Tx

As shown in Fig. 144a and Fig. 147, the linear region between 0.4 V and 0.8 V shows the possibility of linear modulation (e.g., QAM, QPSK, etc.) with this structure. The simplified schematic of the direct conversion Tx (LO at 60 GHz) for linear modulation is presented in Fig. 154a. In this case, by applying a small signal BB, the switches can function as a passive mixer. The performance of this passive mixer can be controlled by changing the V_{CON}. Fig. 154b shows measured and simulated BB to RF (60 GHz) conversion gain of the Tx for the small signal BB at various bias points (V_{CON}). This graph can also be calculated by differentiating the S_{21} curve in Fig. 144a.



(a) (b)

Fig. 154 a) Schematic of the Tx for linear modulation. b) BB to RF conversion gain for linear modulations vs. V_{CON}.

The conversion gain in Fig. 154b shows the maximum for around a 0.6 V BB biasing voltage (V_{CON}). In addition, from Fig. 147 we know that by increasing the V_{CON}, the P_{OUT} of the PA decreases, which means less output power from the Tx. With a LO power of around 5 dBm, the mixer shows a constant gain for all four channels. Fig. 155 presents the large signal performance of the mixer for all four channels. With a 35 mW power consumption and 5 dBm LO power, the Gilbert cell mixer achieved around 5 dB CG and -4 dBm OP_{1dB}.

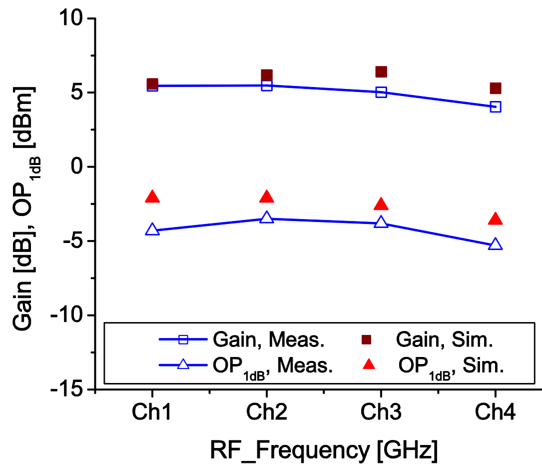
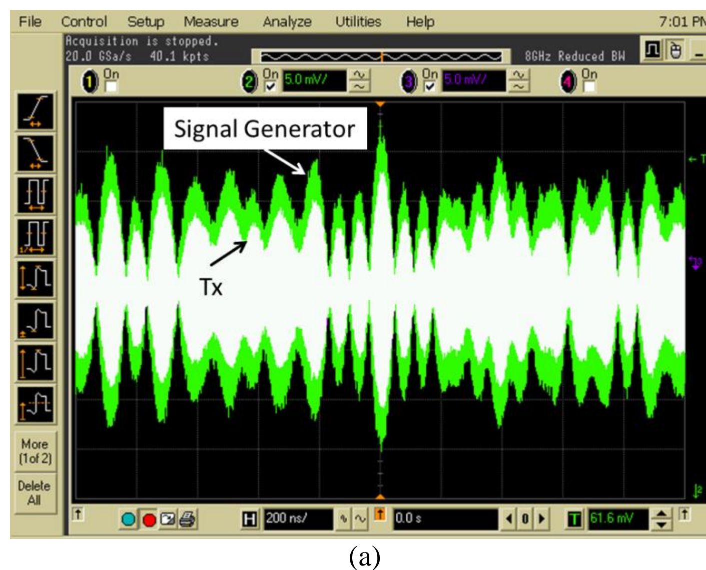


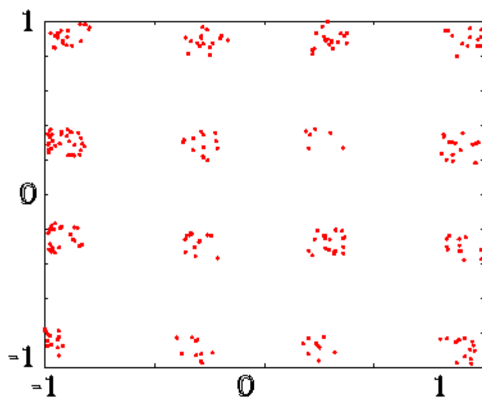
Fig. 155 Large signal measured vs. simulated results.

In order to justify the functionality of the circuit for a 60 GHz application, this circuit was tested in a 60 GHz wireless communication system as a homodyne Tx over 1 m distance. In this system, the output of the Tx was connected to the horn antenna via a probe and a cable. The modulated signal was generated with a SMU200A signal generator with a 25 MHz bandwidth. At the receiver side, the setup includes local oscillators, horn antennae, LNA with a 7 dB noise figure and 20 dB gain, a down-converter mixer with 10 dB conversion loss and 2 GHz IF frequency, and an oscilloscope with a 40 GS/s sampling rate.

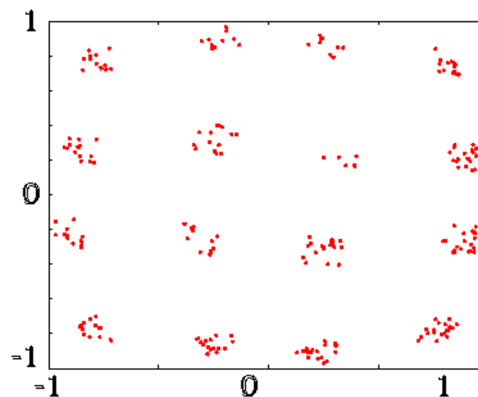
The 100 Mbps time domain signals at the output of the SMU200A and the receiver are presented in Fig. 156a. After sampling and data processing in MATLAB, the constellation of the 16 QPSK signal was drawn in Fig. 156b-c. Fig. 156b presents the constellation diagram directly at the output of the signal generator and Fig. 156c presents the constellation diagram of the received signal. The main source of EVM deterioration is due to the gain compression. As shown in Fig. 156c, the received signal amplitude drops at the corners of the constellation as the signal levels pass the 1dB compression point.



(a)



(b)



(c)

Fig. 156 a) Comparison of time domain signal from the Tx and the signal generator. b) Signal generator constellation. c) Constellation of the received signal.

5.3 Conclusion

In this work, two types of transmitters - heterodyne and OOK - are studied, designed, realized and measured. Both transmitters have shown state-of-the-art performance.

The heterodyne transmitter utilized the Gilbert cell topology for the up-conversion to gain better LO-RF and LO-IF isolations and image rejection ratios. The Gilbert cell mixer was followed by a five-stage transformer-based PA to boost the conversion gain and output power. Thanks to the transformer characteristics, no DC-block was used in this design, which, because of the low Q-factor of the capacitors in this technology, can deteriorate the output power. Furthermore, by placing the PA transistors as close as possible to one another at each stage, an almost perfect RF ground was introduced which further deterred any source degeneration. The realized transmitter achieves between 13 dBm to 16 dBm P_{OUT}, 11 dBm to 14 dBm P_{1dB}, 8% to 14% efficiency and 22 dB to 30 dB power gain for all four channels defined in the IEEE 802.15.3c [32]. In comparison with the state-of-the-art results (Table. 25) this transmitter achieves high CG, P_{OUT}, isolation and efficiency with small chip size.

Table. 25 Comparison of the heterodyne Tx with the state-of-the-art results.

Ref./Tech.	[92] 40 nm	[91] 65 nm	[90] 45 nm	Heterodyne Tx-90 nm
RF Freq. [GHz]	59.5-67	55-67	53-66	57-65
IF Freq [GHz]	0	0	0	18-22
Conv. Gain [dB]	26	18.3	15	22…30
P_{1dB} [dBm]	<13	9.5	N.A.	11…14
P_{sat} [dBm]	13.8…15.6	10.9	10	13…15.5
P_{DC} [mW]	220	186	360	250
EFF. (%)	11…16.5	5	3	8…14
LO-RF Iso. [dB]	N.A.	N.A.	>22	>45
IF-RF Iso +Image [dB]	>20	N.A.	>10	>45
Size [mm^2]	0.96	3.5*	0.23	0.6

In the second transmitter topology, a novel OOK Tx structure based on CMOS technology was introduced and the measured results were presented. The modulator is designed for maximum bitrate, no DC power consumption and small chip size. In addition, by utilizing accurate models and designing an appropriate matching network, a high performance PA for this purpose was realized. With these optimization techniques, more than 8 dBm output power, 9 dB gain and 17% efficiency were measured. As shown in Table. 26, in comparison with the other state-of-the-art results, the Tx presented in this work achieves much better performances. Finally, by using this Tx in a complete wireless system, more than 6 Gbps over a 4 m distance with less than 36 mW power consumption was achieved during

measurement. To the author best knowledge, this is the highest data-rate beyond 1 m distance ever measured with a CMOS transmitter at 60 GHz.

Table. 26 Comparison of the OOK Tx with the state-of-the-art results.

Ref.	[63]	[64]	[67]	OOK Tx
Modulation	QPSK	OOK	OOK	OOK
Distance [m]	1	0.3-0.5	0.6	4
Bit Rate [Gbps]	4	1.5	3.3	6
P_{sat} [dBm]	10	-10	7	8
P_{DC} [mW]	123*	31.2*	183*	36
EFF. (%)	8*	0.3*	3*	17.5
On/off Iso. [dB]	-	19.5	-	30
Antenna	25 dBi Horn	11.5 dBi Yagi-Uda	14 dBi Patch	25 dBi Horn
Size [mm^2]	6.875	1.08	0.43	0.38

*Including VCO

Further, this design (OOK Tx) has been utilized as direct conversion (homodyne) Tx with linear modulation scheme. This Tx is working more like an direct conversion up-converter as its output power is quite low. This topology demonstrate poor LO isolation (> 10 dB), but it shows higher OP_{1dB} and CG in comparison with so far published state-of-the-art up-conversion mixers (Table. 27).

Table. 27 Comparison of the homodyne Tx with the state-of-the-art results.

Ref.	[71]	[73]	[5]	Homodyne Tx
Process	CMOS 90 nm	CMOS 90 nm	CMOS 90 nm	CMOS 90 nm
Freq. [GHz]	40-51	25-75	58-66	58-66
IF [GHz]	11	N.A.	18-22	BB
LO Power [dBm]	0	6	4	5
CG [dB]	-11	1	-2	5
OP_{1dB} [dBm]	-10	-3.5	-9	-4
LO Iso. [dBm]	26.5	>30	>30	>10
V_{DD} [V]	1.2	3	1.2	1.2
P_{DC} [mW]	13.2	93	17	34
Size [mm^2]	0.63	0.3	0.41	0.38

6 Conclusion

The emerging new applications require must faster data communication. To satisfy these requirements, new systems and technologies are being developed. In line with this trend, the main focus of system designers - in respect of the physical layer - lies in the optical and wireless mediums. Higher data-rate requirements demand a higher bandwidth. The higher bandwidth requirement together with the recent technological developments in the CMOS and SiGe HBT technologies has attracted circuit designers towards the mm-wave frequency band for wireless applications. In this regard, the 60 GHz band (57 GHz to 65 GHz) has seen tremendous investigation in many different aspects, from transceiver topology selection (homodyne, heterodyne, OOK and regenerative) to detailed circuit design.

One of the most important research areas for any transceiver is the power amplifier design. A high P_{OUT} and efficiency are essential for high data-rate communication, coverage and battery lifetime. These problems become more prominent at higher frequencies, as many design and technology limitations are already limiting the performance of the power amplifier.

In this thesis, many aspects of 60 GHz transceiver modeling and design based on 90 nm CMOS and 0.25 µm SiGe HBT design have been investigated. Based on these investigations, different types of power amplifiers and transmitters were designed. The designed power amplifiers based on the HBT technology, although occupying a larger chip size, show higher output power and efficiency in comparison with the CMOS power amplifiers. The two different power amplifiers designed on the HBT technology show 15 dBm to 18 dBm P_{OUT} with around 15% PAE, while the CMOS PAs could only achieve 11 dBm to 14 dBm P_{OUT} and around 10% PAE. In both technologies, higher output power was achieved through different power combining techniques. In the HBT PA, current-combining was utilized for minimum power, combining loss and chip area occupation. Due to the higher output and input impedances of the HBT transistors in comparison with the CMOS technology, this power combining technique can be used without any low impedance problem during the matching network design.

On the other hand, the sensitive and low impedance CMOS transistors require more accurate power combining techniques. In this case, two types of power combining have been tested with this technology. With the first PA, a Wilkinson power combiner with different input and output impedances was utilized. The input impedance of this combiner was 16 Ω while its output is matched to 50 Ω. This allows to use larger transistor sizes for the PA design and, hence, increase the output power. Although this technique has resulted in output power enhancements, due to source degenerations and combining losses, this PA only achieved around 11 dBm P_{OUT}. In order to minimize the combining losses and cancel out source degenerations, a transformer was used in the second PA. This PA achieved 3 dB better P_{OUT} (14 dBm), with better PAE and a much smaller chip size. By comparing these two PAs, it can be concluded that the transformer would be a much better choice when compared with the other types of combiners (i.e., the current and Wilkinson combiners).

Finally, two different types of transmitters (heterodyne and OOK) based on the CMOS technology have been designed and realized. The heterodyne transceiver with an IF frequency at around 20 GHz was designed based on the IEEE 802.15.3c

standard. In comparison with state-of-the-art results, this transmitter - with a small chip size and low power consumption - achieved a high P_{OUT} (13 dBm to 15.5 dBm), efficiency and conversion gains (Table. 25), which is mainly due to the use of the transformer in this design. Moreover, thanks to the accurate design of the Gilbert cell mixer, much higher isolations were achieved in this work in comparison with state-of-the-art PAs.

For the OOK transmitter, a novel topology was developed. In this topology, the modulator and the PA were integrated into one circuit without affecting the P_{OUT} of the Tx. Thanks to this topology, this Tx achieved much higher P_{OUT} with much lower power consumption. This resulted in much higher efficiency of this transmitter in comparison with state-of-the-art OOK transmitters. Finally, the realized circuit was utilized in a wireless system where more than 6 Gbps was successfully transmitted over 4 m distance. To the author best knowledge, this is the highest data-rate beyond 1 m distance ever measured with a CMOS transmitter at 60 GHz.

Future works include the completion of both transceivers (heterodyne and OOK) and packaging. In this case, the antenna design and antenna-chip interface must be studied. In addition, and with regards to the PA design, some new techniques such as distributed active transformers and transistor neutralization could be used in the above designs to further increase the P_{OUT} and PAE.

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