

Integrated Optical Receivers for High-speed Indoor Optical Wireless Communication

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Integrated Optical Receivers for High-speed Indoor Optical Wireless Communication

THESIS

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus Prof.dr. S.K. Lenaerts, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op maandag 19 juni 2023 om 11:00 uur

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Summary

Over the past decades, wireless data traffic has significantly increased, particularly in indoor scenarios. As predicted by many telecommunication analysts, the demand for wireless communication will keep growing exponentially in the foreseeable future. Current wireless communication systems based on radio technologies struggle to keep this pace owing to limited available bandwidth. The research landscape is moving towards optical wireless communication (OWC), which has more bandwidth available and enables high-speed connectivity to offload heavy data traffic loads from radio networks through using optical beams. In a typical short-range (distance < 3m) indoor OWC system, the optical beam incident on the receiver is generated by the optical wireless access points. These access points are connected to a low-cost indoor fiber-optic network and are deploying beam-steering techniques. The maximum optical beam power from an access point is limited due to eye safety regulations. A receiver with a large aperture can efficiently collect enough optical power to allow high-speed transmission. Usually, a large-aperture receiver requires a large-aperture photodetector (PD). Top-illuminated PDs with a large aperture can collect sufficient light but suffer from a decreased electrical bandwidth due to their large capacitance. To break this optical-electrical trade-off, the cascaded aperture optical receiver (CAO-Rx) enabled by a surface grating coupler (SGC) and a high-speed waveguide uni-traveling-carrier photodetector (UTC-PD) has been proposed, and its first preliminary concept has been demonstrated on the InP-membrane-on-Silicon (IMOS) platform in our earlier work. It can optimize the electrical bandwidth and the light collection independently from each other, and it has the potential to achieve a large aperture. The IMOS platform, consisting of a thin membrane with high-refractive-index contrast and full photonic functionality, including light generation, light amplification, and light detection, is compatible for co-integration with CMOS electronics. In this thesis, advanced

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high-sensitivity CAO-Rx schemes are proposed. The concept of the CAO-Rx is comprehensively investigated, upgraded with novel functionalities, and implemented, yielding considerable performance improvements.

First of all, a complete CAO-Rx scheme with optical preamplification is proposed in this work. The proposed high-sensitivity CAO-Rx consists of five modules: the light collection module (a large-aperture SGC and a lens), the optical amplification module (an on-chip optical power monitor, and semiconductor optical amplifiers (SOAs)), a tunable optical bandpass filter (OBPF) module, the high-speed optical-to-electrical (O\E) (large-bandwidth UTC-PD) module, and an electronic transimpedance amplifier (TIA) module. The signal optical beam from free space is first coupled into the receiver via the light collection module. Then the power of the received weak signal light will be boosted by the on-chip optical amplification module. To provide an adaptive current-injection scheme in order to optimize the amplification for best performance, an on-chip optical power monitoring unit is needed to capture the incoming light and give feedback regarding the input power of the SOAs. The optical power monitor is a directional coupler cascaded with a low-dark-current UTC-PD. The tunable OBPF module mainly filters the out-of-band amplified spontaneous emission (ASE) noise from the SOAs. The high-speed UTC-PD inside the O\E module is for converting the modulated optical signal into a high-speed electrical signal. Finally, the high-speed electrical signal is amplified by the on-chip TIA. This on-chip system is able to address both high-speed signal detection and optical performance monitoring. This system is targeted to be validated on the IMOS platform, which in the future can realize the fully integrated CAO-Rx with optical and electronic amplifiers within a compact size.

To further increase the aperture of an on-chip OWC receiver, a receiver array architecture can be considered. To overcome the inherent trade-off between bandwidth and power coupling, a novel large-aperture receiver concept was proposed to improve light collection with minimal bandwidth degradation in our earlier work. This novel receiver concept has been demonstrated before based on a large-scale $M \times M$ top-illuminated PD array, requiring one TIA. The PD array is based on series and parallel interconnections. It is able to achieve a large aperture with square millimeters area and a large field of view (FoV) simultaneously. Since a single CAO-Rx has a trade-off between its aperture and its FoV, the proposed CAO-Rx array can break this trade-off by the inherent advantage of the CAO-Rx (i.e., separately optimizing light collection and electrical detection). Thus, a CAO-Rx array is able to enormously enhance the light collection and almost maintain an acceptable field of view, where its PD array also is with series and parallel interconnection for not sacrificing the bandwidth of PDs.

This thesis covers the following main topics:

Optical receiver with a metal-reflector-assisted SGC

To implement a more efficient SGC, a reflector is introduced under the grating area for reflecting more light and enhanced light coupling into a waveguide to maximize the receiver's output electrical signal-to-noise ratio. Considering the good fabrication compatibility with UTC-PDs (for monitoring and signal detection) and its excellent robustness to the bonding layer-thickness-variation causing coupling degradation, a metal reflector is selected. Here, the bonding layer is for bonding the InP membrane and the silicon carrier together, and the thickness of the bonding layer varies from run to run, which may reduce the coupling efficiency of the SGC. In this work, we not only developed a highcoupling efficiency linear SGC with a metal reflector but also we experimentally verified that the metal reflector-assisted linear SGC and the UTC-PD could be monolithically co-integrated in the IMOS platform. The demonstrated metal reflector-assisted linear SGC is polarization selective and has a size of 10 × 10 μ m². A polarization-independent SGC has been developed in other work, and puts special additional fabrication challenges (e.g., a decreased fabrication tolerance). Hence, an SGC design optimized for TE polarization (with polarization-dependent loss > 20 dB) is used in this work. The dry etching rates of the grating groove above the metal layer and the one above the dielectric layer are different. Hence, performance-optimized etching for those two-types of SGC in a single run could not be ensured. As a result, the comparison between the SGC with and without a metal reflector is made by using separate runs. The measured maximum beam-to-waveguide coupling loss is 4 dB, which is 1.5 dB smaller than the typical value of a linear SGC without a metal reflector on the IMOS platform. The optical back-to-back sensitivity of the CAO-Rx with a metal reflector without any amplifiers for a 10 Gb/s link is measured, which is 1.5 dB higher than that of a CAO-Rx without a metal reflector. This metal reflector can also be applied in an advanced polarization-independent large-aperture SGC design to further increase the SGC's coupling efficiency.

Optical receiver with multiple-stage SOAs

A novel noise-reduction optical amplification scheme by integrating cascaded SOAs is proposed to maximize the receiver's output electrical signal-to-noise ratio. Compared with utilizing a one-stage optical amplifier, using multiple independent SOAs with the same total length as a multi-stage optical amplifier offers the advantage of optimizing the noise figure of each optical amplifier independently by tuning their injection currents, which leads to the reduction of the total noise and an improvement of the receiver sensitivity. As the integration of SOAs with high-speed PD on the IMOS platform was under de-

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velopment at that time, we tested the high-sensitivity integrated OWC receiver scheme with multi-stage optical preamplifiers on the HHI InP-based platform with a low-refractive-index contrast instead as a first experimental step to validate our concept. Making a trade-off between the contribution of noise figure at each stage and the injection currents driving complexity, the tested receiver consists of a single waveguide PIN photodetector integrated with two cascaded SOAs. The sensitivity of the implemented two-stage optically amplified receiver (SOA-PIN) is 1.5 dB better than that with one-stage optical amplification, even 3dB better than the state-of-the-art electrically amplified receiver (PIN+TIA). By combining optical and electrical amplification (SOA-OBPF-PIN-TIA), where an OBPF is added to further reduce ASE noise, a higher sensitivity receiver is achieved.

Optical receiver with bias voltage-optimized PDs

The bias voltage of the low-dark-current PD within the optical amplification module and of the large-bandwidth UTC-PD inside the high-speed O\E module is optimized to be the same in order to reduce system-level complexity. By redesigning the layer stack of the UTC-PD and optimizing the fabrication process using the IMOS platform, the trade-off between PD's dark current and PD's -3dB bandwidth is optimized. The improvement details are: 1) redesigning the layer stack of the UTC-PD in order to decrease the bias dependence of the -3 dB bandwidth, and 2) developing passivation techniques, being compatible with the standard fabrication process of the CAO-Rx, in order to decrease the dark current of the waveguide UTC-PD at a certain bias voltage. The new UTC-PD layer stack on the IMOS platform, with an unintentionally doped InGaAsP quaternary layer between the InGaAs absorption layer and the InP carrier collection layer, is designed to suppress the electron accumulation at the InGaAs-InP heterojunction interface. A UTC-PD has been demonstrated, which is biased at -1V to achieve a -3dB bandwidth above 40 GHz and a responsivity around 0.7 A/W, while its dark current is below 1 nA. These results prove that the optimized UTC-PD can meet the requirements of the system design. Furthermore, we also experimentally verified that tuning the waveguide etching depth of a waveguide UTC-PD in order to be compatible with a deeply-etched SGC developed for reducing one lithography step did not noticeably degrade the performance of the UTC-PD. This result reduces the fabrication complexity of the CAO-Rx.

Passive receiver unit based on a zero-volt-bias UTC-PD

To relax the power supply stress of the CAO-Rx-array-based receiver for decreasing system complexity, a passive unit based on a zero-volt-bias CAO-Rx is introduced. The term "passive receiver unit" in this context refers to a sub-component inside the receiver that operates without relying on an external

power supply. The key component of a zero-volt-bias CAO-Rx is a zero-volt-bias UTC-PD, which needs to have a large -3 dB bandwidth to support a high-speed OWC link. In this work, we not only developed a zero-volt-bias CAO-Rx with an acceptable large bandwidth for the prototype of a 10-Gbaud OOK array-based receiver but also validated its transmission performance in a 10 Gb/s OWC link. A new layer stack of the UTC-PD on the IMOS platform is designed for maintaining large carrier drift velocity in order to achieve an acceptable bandwidth at zero-volt bias. And the size of the UTC-PD is optimized to improve PD's responsivity while maintaining an acceptable -3 dB bandwidth (for supporting a data rate > 10 Gb/s). The photocurrent of the zero-volt-bias waveguide UTC-PD shows good linearity when the input optical power of the UTC-PD stays below 0.75 dBm. Compared with the first-generation UTC-PD at zero-volt bias, the -3 dB bandwidth of this new-generation UTC-PD is largely enhanced from < 3 GHz to 13.3 GHz, and the responsivity at zero voltage is increased from < 0.2 A/W to 0.8 A/W. In terms of the system performance of a 10 Gb/s OOK signal OWC link with a zero-volt-bias CAO-Rx, it was found that there was only a minor receiver sensitivity penalty (<0.2 dB) when compared to the same CAO-Rx with -1V bias. These results suggest that the zero-volt-bias UTC-PD can be applied in a CAO-Rx array. Moreover, these results also suggest that this zero-volt-bias UTC-PD can be used inside the power monitor of the proposed CAO-Rx with optical amplification to reduce system complexity.

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Chapter 1

Introduction

1.1 Background

Wireless communication is a field with numerous pioneers, and it is challenging to identify a single individual who has made the most significant contribution. Michael Faraday, James Clerk Maxwell, Heinrich Hertz, Sir Oliver Lodge, Aleksandr Stepanovich, and Guglielmo Marconi are among the many who played critical roles in developing early wireless technology [1]. Some of these individuals developed the theoretical foundations of wireless communication, while others applied the theory to create innovative technological applications. Nevertheless, it is widely recognized that Marconi's successful transmission of wireless telegraphy, or radiotelegraphy, across the English Channel in 1899 was a groundbreaking event in the history of wireless communication. Marconi's success in transmitting wireless telegraphy messages paved the way for new social networking and communication forms. In 1906, De Forest developed the technology for radio broadcasting, which allowed audio and music to be transmitted over wireless systems, transforming the way we entertain ourselves [2]. In the decades that followed, wireless technologies underwent significant advances, leading to a dramatic increase in the capacity of wireless networks. According to Ref. [3], between 1955 and 2011, wireless networks increased their capacity by over a million times, largely following Cooper's Law. This law states that the data rate available to a wireless device doubles approximately every 30 months [4].

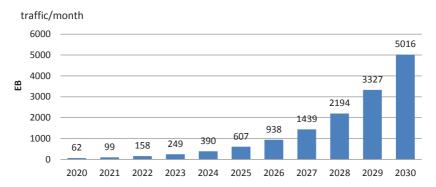


Figure 1.1: Prediction of mobile data traffic growth (M2M data traffic included) [6].

The future of wireless networks will see a significant increase in data traffic. The International Telecommunication Union (ITU) predicts that wireless traffic, including machine-to-machine (M2M) traffic, will grow at an annual rate of approximately 55% between 2020 and 2030, as shown in Figure 1.1. This growth is expected to result in total traffic of 5016 EB (exabyte) in 2030, more than 30 times the traffic in 2022. Furthermore, statistics from IEEE Future Networks suggest that almost 80% of wireless traffic is generated indoors [5].

The rapid growth in wireless data traffic in indoor environments has created the need for increased indoor network capacity to prevent severe congestion. According to the Shannon-Hartley theorem, the maximum attainable capacity of a communication link can be calculated as $C = B \cdot log_2(1 + SNR)$ in bits/second, where B denotes the bandwidth of the channel [7]. By using an increased signal-to-noise ratio (SNR) and wider bandwidth B, wireless links can achieve significantly higher capacity. Increasing the amount of available channel bandwidth is the most straightforward way to expand wireless network communication capacity, and it is directly dependent on the availability of spectrum for communication.

Currently, indoor data traffic is primarily served by mobile communication systems and IEEE 802.11 Wireless Fidelity (WiFi) systems, which deploy the radio frequency spectrum for information transmission. The radio frequency spectrum covers a frequency range from 30 kHz to 300 GHz, and its use is strictly regulated by local and international authorities [8]. For the latest commercial 5G mobile communication technology, the utilization of high-frequency bands at 39 GHz has been authorized. The protocol for the utilization of the 60-GHz

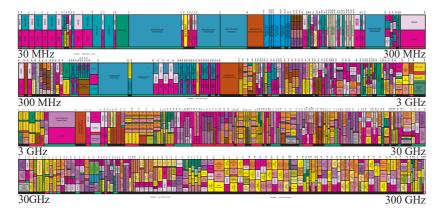


Figure 1.2: The allocation of radio spectrum from 30 MHz to 300 GHz [10].

band has been released [9]. New spectrum bands are being opened, such as sub-THz bands up to 300 GHz, as shown in Figure 1.2. Despite this expansion, the exponential growth in data traffic is quickly exceeding the capabilities of radio communications. Available radio frequency resources are becoming scarce, and the spectrum is becoming congested.

1.2 Indoor optical wireless communication

In recent years, there has been a growing interest in Optical Wireless Communication (OWC) technologies from academia and industry. OWC has the potential to alleviate congestion by providing vast additional unlicensed bandwidth that is low-cost and opens up a huge amount of bandwidth, much larger than available radio frequencies. The visible spectrum (400 nm-700 nm) offers an additional 320 THz, and the fiber infrared spectrum (1460 nm-1625 nm) offers an additional 20.9 THz of available bandwidth [11]. OWC technology is an attractive solution for offloading heavy traffic loads from congested wireless networks that rely on radio waves. In addition, OWC systems offer many other benefits, such as immunity to electromagnetic interference (EMI) and high levels of security. OWC can be used in environments where radio-based wireless communications are not feasible, such as aircraft cabins, underwater, and in areas where electromagnetic interference is a concern. The main OWC technologies may be divided into two groups: visible light communication (VLC) (using a

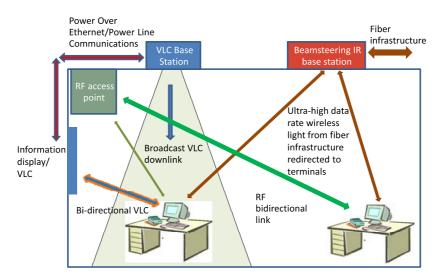


Figure 1.3: Basic indoor OWC scenarios, with the visible light communication (VLC) system and the beam-steered infrared light communication (BS-ILC) system [17] (© [2016] IEEE. Reprinted, with permission from Ref. [17]).

fixed beam) and beam-steered infrared light communication (BS-ILC) [11–15]. In addition to these two types, an OWC link can also be established using a fixed infrared beam [16]. However, this particular type of OWC link will not be discussed in this thesis due to its similarities with VLC.

OWC is designed to complement, rather than replace, existing radio-based wireless networks. Both the coherent optical detection technique and the direct detection technique can be used in OWC links. Although the coherent optical techniques provide ultimate sensitivity [18], the additional optical carrier recovery circuit is expensive and complex, making the coherent technique difficult to apply in short-reach OWC systems, which are cost-sensitive. Therefore, the intensity modulation direct detection (IM/DD) technique is generally preferred for an OWC system because it is a cost-effective solution [19]. The SNR of the direct detection technique depends on the square of the received optical power, which means that IM/DD links can only tolerate a limited amount of path loss [19]. Consequently, most OWC links are established using a clear line-of-sight path with low path loss. Radio techniques operating at frequencies

below 60 GHz can be used in conjunction with OWC to establish links that do not rely on a clear line of sight; at higher frequencies, they are also limited by line-of-sight requirements.

1.2.1 Visible light communication

White light-emitting diode (LED) bulbs were primarily developed as light sources for indoor lighting due to their high efficiency and long lifespan. In 2003, researchers experimentally demonstrated that electrical signals could be encoded into the visible light emitted from LED chips using high-frequency amplitude modulation [20]. As long as the frequency of the amplitude modulation is higher than 200 Hz, it is not perceived by the human eye and does not affect the primary lighting function [21]. This development led to the creation of VLC technology, which uses visible light as a medium to transmit data wirelessly. The optical spectrum available for VLC ranges from 400 nm to 700 nm, corresponding to a frequency range of 428.27 THz to 749.48 THz. This frequency range is 10^4 times larger than the entire radio frequency spectrum, providing sufficient space for data transmission. As a result, VLC has the potential to reduce congestion in the radio frequency spectrum by providing an alternative bandwidth solution.

The schematic of a typical VLC application scenario is shown in Fig. 1.3. This process involves converting an electrical signal into a fast-intensity modulated optical signal. Then the optical signal is transmitted through free space. Later it is received by an optical receiver for converting the optical signal back to the electrical signal that can be read by the desktop computer, laptop computer, tablet computer, smartphone or other wireless end-user devices.

One of the main factors limiting the transmission speed of VLC is the low modulation speed of the LED light source. Two types of white LED lamps have been developed for indoor lighting, which can be used in VLC. The first type, known as a phosphor-converted LED (pc-LED), uses a blue LED and a phosphor coating, while the second type, called RGB LED, uses a combination of red, green, and blue LEDs [14]. The pc-LED is more commonly used as an indoor lighting source due to its lower cost and higher efficiency. White LED bulbs typically use a blue LED with a phosphor coating to spread the blue light into white light. They have limited bandwidth, with the phosphor component typically having a -3dB bandwidth of around 2 MHz due to its long decay time [12]. In addition, the typical -3dB bandwidth of commercial large-area blue LED chips is around 10 MHz [12]. Researchers have found that the modulation bandwidth of white LED bulbs can be improved to match that of the blue LED chips if only

the blue wavelength is detected [22]. The use of a blue color filter at the receiver can effectively block the phosphor and increase the link bandwidth [23]. To overcome this limitation, researchers have explored the use of micro-LEDs, which have a higher bandwidth due to their smaller capacitance. A micro-LED chip has been demonstrated to achieve the highest modulation bandwidth of around 1 GHz [24].

VLC technology can provide gigabit speeds over short distances with additional signal processing technology. Using a commercial white LED bulb and the Orthogonal Frequency Division Multiplexing (OFDM) scheme, a transmission speed of 1 Gb/s can be achieved [25]. With a custom white LED chip, even higher speeds of up to 1.9 Gb/s have been demonstrated [26]. The use of an RGB LED chip in VLC allows for the use of Wavelength Division Multiplexing (WDM), enabling even faster speeds. In a demonstration, a VLC link using an RGB LED chip achieved a speed of over 10 Gb/s through the combination of WDM and OFDM [27].

VLC links are unidirectional, meaning data is only transmitted in one direction. Recently, Light-Fidelity (LiFi) has been developed based on VLC technology that supports bi-directional communication, multiple users, and mobility. The first commercial LiFi systems were introduced in 2013 [28].

1.2.2 Beam-steered infrared light communication

The infrared optical spectrum is the basis of fiber-optic communication networks that connect continents and serve as the backbone of modern communication systems. These networks provide high-speed data access to metropolitan areas, cities, towns, and homes. Extending the use of infrared beams used in the optical fiber to enable free-space connections for last-mile connectivity represents a logical and relatively straightforward progression. A new approach for OWC has been created, utilizing infrared light communication that utilizes steered narrow laser beams, known as BS-ILC [14, 29, 30]. In free space, the infrared beam can serve as a virtual optical fiber, which allows the use of well-established infrastructure and components of fiber-optic communication networks to enable maximum transmission speeds.

The BS-ILC system, which enables bi-directional communication, can be classified as "LiFi 2.0" [31]. A typical application scenario of the BS-ILC system is shown in Figure 1.3. In this system, data from the access network is processed and modulated at the central communication controller before being sent to the beam-steering IR base station. The base station then steers the infrared beams to the user terminals, while RF-based communication is used to support upstream communication.

The BS-ILC can achieve a maximum transmission speed of 112 Gb/s using pulse amplitude modulation 4-level (PAM-4) modulation with a single beam, as demonstrated in a previous study [32]. Furthermore, it has been demonstrated that the BS-ILC is capable of supporting a Terabit/s link with ten wavelengthdivision multiplexed PAM-4 signals [29]. The high-speed transmission capacity of BS-ILC can be attributed to several factors. Firstly, the use of infrared laser beams in BS-ILC is allowed at higher power levels compared to visible laser beams owing to eye safety regulations. Lasers are classified according to their level of risk, with Class 1 being the safest for all normal conditions of use, including direct viewing or use with magnifying devices such as telescopes or microscopes with limited aperture. Eve safety standards such as International Electrotechnical Commission (IEC) 60825 and American National Standards Institute (ANSI) Z136 typically limit the maximum continuous wave radiant power for the visible laser beam to 0.5 mW. In contrast, for an infrared laser beam above 1400 nm, the maximum continuous wave radiant power is limited to 10 mW [33]. Secondly, the use of beam steering technology improves the directionality of the beam. It is important to note that even the use of the collimated infrared beams in the BS-ILC system is compliant with eye safety regulations. Thirdly, the high-speed optical devices widely used in optical fiber systems, such as laser diodes, photodetectors (PDs), and optical modulators, can also be applied in the BS-ILC.

1.2.3 Visible light communication versus beam-steered infrared light communication

VLC technology tends to be more cost-effective, requiring minimal infrastructure or utilizing existing infrastructure, such as power-line communication or power-over-ethernet techniques, which can be reused for VLC [14]. And VLC systems use a wide beam to support wide coverage, making it easier to align the receiver with the light source. However, VLC systems do have several limitations. VLC systems often employ LEDs as the primary light source, which are designed primarily for illumination purposes. As such, the beam output from the LED typically has a widespread [12]. As the intensity of the wide beam scales with the squared inverse of the distance between the user and the LED source, the received optical power decreases rapidly as the distance increases, which ultimately limits both the reach and transmission speed of the system. Moreover, it is important to keep the LED bulb switched on continuously to maintain the VLC link. However, in certain situations (such as bright

daylight entering a room), the illumination that results from keeping the LED bulb switched on may not be feasible or desirable.

The BS-ILC technology allows for a decoupling of the illumination and communication functions as it utilizes an invisible infrared beam to the human eye. It can be deployed in scenarios where an always-on illumination is not desirable. Furthermore, the BS-ILC link is established on-demand, which leads to improved energy efficiency compared to VLC. Additionally, the BS-ILC can support each user with higher transmission speeds, making it a promising technology for high-speed data transmission. Indoor wireless communication networks are evolving towards higher transmission rates and better energy efficiency [6, 34]. This thesis expands the research which was done so far on BS-ILC systems.

1.3 Integrated optical receiver for beam-steered infrared light communication

An optical receiver, a key component for an OWC system, is used to collect and convert the optical signal into an electrical signal. Current research focuses on two versions: one is the coherent optical receiver, and the other is the direct detection receiver. The coherent optical receiver provides the ultimate sensitivity [18]. However, the additional optical carrier recovery circuit is expensive and complex, making the coherent receiver challenging to apply in indoor OWC since the OWC system is cost-sensitive. Thus, the IM/DD technique is preferred for an indoor OWC system. So the direct modulation receiver is exploited for OWC in this research.

Due to the eye safety regulation, the maximum transmitted power of the infrared laser beam in a BS-ILC link should be below 10 dBm for $\lambda > 1.4 \,\mu m$ [33]. An OWC receiver is usually required with high speed and high sensitivity to enable a high connectivity rate and large power budget communication link. Moreover, the ideal OWC receivers are expected to have a large aperture and a large field of view (FoV) to collect as much as possible optical power as well as to decrease the required alignment accuracy of the tracking unit at the transmitter and at the receiver in a BS-ILC system [35]. Usually, a large-aperture receiver requires a large-aperture PD. In practice, the aperture of a waveguide-fed PD is limited. A spot size converter (SSC) feeding a high-speed waveguide photodetector (WGPD) has a high coupling efficiency [36]. However, the aperture of the SSC is usually designed to match the single-mode fiber, and its aperture scalability is limited. A top-illuminated PD with a large active area can collect

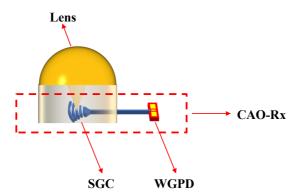


Figure 1.4: Schematic of the cascaded aperture optical receiver (CAO-Rx) enabled by a waveguide photodetector (WGPD) and a surface grating coupler (SGC) [40].

sufficient light but with decreased electrical bandwidth due to its large capacitance. External optics, such as compound parabolic concentrators, can be used to expand the aperture at the cost of a reduced FoV [37]. The étendue law limits the ability of optical components such as lenses or mirrors to simultaneously increase the aperture and the FoV of an optical system. The law of conservation of étendue in physics, also referred to as the $A-\Omega$ product, states that the product of the aperture A and the FoV Ω of an accepted beam remains constant in a concentrating optical system [38]. In other words, $A_i \times \Omega_i \leq A_o \times \Omega_o$, where A_i , A_o , Ω_i , and Ω_o represent the aperture and FoV at the input and output of the system, respectively [39].

Several approaches were proposed to improve the performance of an OWC receiver. An angle-diversity receiver (ADR) using multiple PDs to receive the optical power from different angles can achieve a large aperture as well as a large FoV. Each PD should be connected to a separate transimpedance amplifier (TIA), which increases complexity. The étendue law may be broken by a fluorescent concentrator-based receiver [41]. A slab transparent waveguide doped with fluorophore is used to capture the photons with short wavelengths and re-emit the photons with longer wavelengths to guide them to a PD [42]. This light may have a long decay time, which may limit the speed of this type of optical receiver. According to the étendue law, utilizing a large-aperture PD can effectively increase the input aperture of a concentrator while preserving the input FoV. The first preliminary concept of a cascaded aperture optical receiver (CAO-Rx) enabled by a WGPD and a surface grating coupler (SGC) was pro-

posed and demonstrated by Dr. Cao et al. [43], which can achieve large light collection aperture without degrading the electrical bandwidth. The schematic of this CAO-Rx is shown in Fig. 1.4. The receiving aperture can be increased to more than 10000 μ m² when the SGC has an apodized design, and the aperture can be further increased by an array of SGCs and a waveguide optical power combiner [40]. A single CAO-Rx still has limited aperture and low-cost external optics may be packaged with a single CAO-Rx to further increase its aperture [40]. However, it is important to note that the FoV of this receiver remains limited by the étendue law when employing external optics. In the future, a CAO-Rx array architecture can be considered to further increase the aperture of an OWC receiver. A novel large-aperture receiver concept requiring one TIA. with a PD array based on series and parallel interconnections, was proposed and demonstrated to improve light collection and Fov with minimal bandwidth degradation by professor Koonen et al. [35]. It should be mentioned that the proposed PD array, the CAO-Rx and the CAO-Rx array are compatible with the photonic integration circuits technologies.

The practical implementation of OWC systems by users will largely depend on three factors: scalable manufacturability, power efficiency (especially for battery-powered mobile devices), and cost-effectiveness [31]. Photonic integrated circuits are manufactured by a sequence of precise process steps carried out on batches of wafers. The ability to fabricate hundreds or thousands of circuits simultaneously leads to cost reductions, making mass production a compelling reason for integration. The 2018 Jeppix roadmap provides a preliminary cost estimate for a mature generic foundry process, with costs starting at 100 euro/mm² for 10,000 chips per year and dropping to the order of 10 euro/mm² for production levels of one million chips per year [44]. Extrapolating this further, laser and detector chips for high-volume smartphones, computer peripherals, and home broadband applications are expected to cost just some mere cents. Photonic integration is highly desirable for indoor OWC due to its compactness, high performance, and, most importantly, mass manufacturability and reduced cost. The generic foundry process allows production volumes to be aggregated across multiple product lines. In addition, the trend to increasing manufacturing throughput and power efficiency while reducing package cost and chip size has led to the adoption of a monolithic integration optical receiver for BS-ILC, with this research developing a monolithically integrated optical receiver [45].

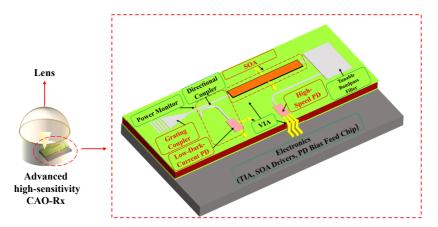


Figure 1.5: Schematic of the advanced high-sensitivity cascaded aperture optical receiver (CAO-Rx). SOA: semicondcutor optical amplifier; PD: photodetector; TIA: transimpedance amplifier.

1.4 Organization and contributions of this thesis

The CAO-Rx has a unique capability that enables separate optimization of light collection and electrical detection. Furthermore, it can be manufactured on a massive scale using photonic integration technology. These advantages make the CAO-Rx an excellent candidate for the BS-ILC receiver. The CAO-Rx enabled by an SGC and a high-speed waveguide uni-traveling-carrier photodetector (UTC-PD) has been proposed, and its first preliminary concept has been demonstrated on the InP-membrane-on-Silicon (IMOS) platform in our earlier work. [43]. In this thesis, advanced high-sensitivity CAO-Rx schemes are proposed. The concept of the CAO-Rx is comprehensively investigated, upgraded with novel functionalities, and implemented, yielding considerable performance improvements.

The optimal receiver architecture of the advanced high-sensitivity CAO-Rx scheme consists of five modules: the light collection module (a large-aperture SGC and a lens), the optical amplification module (an on-chip optical power monitor, and semiconductor optical amplifiers (SOAs)), a tunable optical bandpass filter (OBPF) module, the high-speed optical-to-electrical (O\E) (large-bandwidth UTC-PD) module, and an electronic TIA module. Figure 1.5 illustrates the schematic of the proposed CAO-Rx architecture, which is discussed

in detail in Chapter 2. The receiver system is targeted to be validated on the IMOS platform, which in the future can realize the fully integrated CAO-Rx with optical and electronic amplifiers within a compact size. The proposed high-sensitivity CAO-Rx in a power-limited OWC system has to maximize the receiver's output electrical SNR at a high-speed data rate while trying to minimize the complexity. The factors affecting the receiver's electrical SNR are mainly related to the optical power received by a CAO-Rx, and the gain and the amplified spontaneous emission (ASE) of the optical amplifiers. To increase the electrical SNR, a key challenge (Research Challenge 1) is how to improve the received signal power level in the optical domain. Research Challenge 1 mainly requires increasing the signal optical power received by the high-speed UTC-PD before the SOAs are saturated. Thus, two research goals have been set: Research Goal 1.1 (Chapter 4) is to decrease the optical signal loss by improving the optical beam-to-receiver coupling efficiency of the light collection module; **Research Goal 1.2** (Chapter 5) is to optimize the optical amplification module by developing a novel SOA-noise-reduction scheme to provide higher on-chip gain without degrading the signal quality. Here, as described in the introduction of the optical amplification module, an on-chip optical power monitor is introduced to inject a current into the SOAs, which is adapted for obtaining optimum performance. Therefore, a high-sensitivity monitor design is made to decrease the coupling loss from the received signal light into the waveguide. A low-dark-current UTC-PD (typically with a dark current < 10 nA) is achieved in order to meet the higher-sensitivity requirement. The low-dark-current UTC-PD (the monitoring PD) and the high-speed UTC-PD (the data-detecting PD), based on the first-generation UTC-PD device on the IMOS platform, are usually biased at different voltages. The opposite requirement of small-voltage biased PD for low dark current and large-voltage biased PD for high speed is caused by the heavy bias-voltage dependence of the -3 dB bandwidth of the first-generation UTC-PD device. Research Challenge 2 is about this inconsistent bias design which increases the complexity at the system level. Research challenge 2 is to bias the monitoring PD and the data detecting PD at the same reverse voltage and to minimize this voltage (in order to reduce the electronic circuit requirements). Research Goal 2 (Chapter 6) is about optimizing the UTC-PD fabrication in order to achieve PDs with large bandwidth, high responsivity, and low dark current at a certain low bias voltage, so only one bias feed chip is needed to drive the monitoring PD and the data detecting PD in the proposed receiver architecture shown in Figure 1.5.

To further increase the aperture of an on-chip OWC receiver, a receiver array architecture can be considered. To overcome the inherent trade-off between

bandwidth and aperture (so power coupling factor), a novel large-aperture receiver concept was proposed to improve light collection with minimal bandwidth degradation in our earlier work [35]. This novel receiver concept has been demonstrated before based on a large-scale $M \times M$ top-illuminated PD array, requiring one TIA. The PD array is based on series and parallel interconnections. It is able to achieve a large aperture with square millimeters area and a large FoV simultaneously. In this thesis, we explored a receiver architecture strongly building on the capabilities of integrated optics, namely the CAO-Rx array architecture. A single CAO-Rx has a trade-off between its aperture and FoV, which arises from the constraints imposed by the SGC component [46]. The aperture size in the proposed CAO-Rx array is equivalent to that of the SGC array, thus enabling the CAO-Rx array to break that trade-off by the inherent advantage of the CAO-Rx (i.e., separately optimizing light collection and electrical detection). Thus, a CAO-Rx array has the potential to enhance the light collection and maintain an acceptable FoV. Simultaneously, its PD array employs an identical interconnection configuration, consisting of series and parallel interconnections, as proposed in Ref. [35], ensuring that the bandwidth of PDs is not compromised. But no matter the top-illuminated PD array or the CAO-Rx array, the number of PDs will inevitably increase, and the bias voltage of a largescale PD array may exceed the system's capabilities. The voltage-bias design of a large-scale PD array (e.g., $M \times M$) (Research Challenge 3) will require an additional bias feed chip and increase system complexity. A zero-volt-bias PD with sufficient bandwidth would be a good solution for the array-based OWC receiver. Thus, Research Goal 3 (Chapter 7) is about developing a unit based on zero-volt-bias CAO-Rx for a potential large-scale array-based OWC receiver to relax the voltage-bias-supply stress.

The contributions of this thesis will be presented in each chapter, and the detailed research methods and results will be shown accordingly.

Chapter 2 presents a detailed analysis of the receiver architecture of the advanced CAO-Rx implemented in this thesis. The chapter begins by introducing the state-of-the-art high-sensitivity high-speed receiver schemes as published in recent publications. In addition, the system considerations of the optical receiver are thoroughly discussed. Considering the system requirements and the key findings outlined in those state-of-the-art works, the architecture of the advanced CAO-Rx is determined, consisting of five modules:

- 1) the light collection module (a large-aperture SGC and a lens),
- 2) the optical amplification module (an on-chip optical power monitor and SOAs),
 - 3) a tunable OBPF module to filter the out-of-band ASE noise from the SOA,

4) the high-speed optical-to-electrical (O\E) (large-bandwidth UTC-PD) module,

5) an electronic TIA module,

Then the research challenges are identified in these modules, which involve maximizing the receiver's electrical SNR to achieve a high-sensitiv-ity CAO-Rx and reducing the complexity of the integrated optical receiver. In order to overcome these challenges, specific research goals are outlined. This chapter serves as the foundation for the subsequent chapters, providing a clear framework for the advanced CAO-Rx.

In **Chapter 3**, two InP-based photonic integration platforms related to this work, namely the IMOS platform and the HHI platform, are introduced. The HHI platform serves as a temporary bridging solution to fill the gap in the IMOS platform. As the integration of SOAs with high-speed PD on the IMOS platform was under development at that time, we tested the high-sensitivity integrated OWC receiver scheme with optical preamplifiers on the HHI InP-based platform with a low-refractive-index contrast instead as a first experimental step to validate our concept. The fabrication process of CAO-Rx on the IMOS platform is also detailed, supporting subsequent discussions in the following chapters. Moreover, the introduction of the measurement setups for characterizing photonic chips from these platforms is given.

Chapter 4 describes the experimental demonstration of a metal-reflector-assisted SGC (MRSGC) in a CAO-Rx, and verifies its performance in a back-to-back optical link for the first time. To implement a more efficient SGC in the light collection module of an advanced CAO-Rx, a metal reflector is introduced under the grating area for reflecting more light and enhanced light coupling into a waveguide. Compared to the dielectric-based Distributed Bragg Reflector (DBR) that requires multiple deposition steps, the metal reflector only needs one metal deposition step and results in reduced device processing complexity. The validation of the CAO-Rx integrated with an MRSGC is described, beginning with simulation, design, and separate fabrication of the MRSGC component, followed by the cointegration of the CAO-Rx with an MRSGC, and ending with the verification of the CAO-Rx with an MRSGC in a back-to-back optical link. The chapter also addresses the fabrication challenges encountered during the processing.

In **chapter 5**, a novel noise-reduction optical amplification scheme by integrating cascaded SOAs is proposed to optimize the optical amplification module of the advanced CAO-Rx. Compared with utilizing just a one-stage optical amplifier, using multiple independent SOAs with the same total length as a multistage optical amplifier offers the advantage of optimizing the noise figure of

each optical amplifier independently by tuning their injection currents, which leads to the reduction of the total noise and an improvement of the receiver sensitivity. Making a trade-off between the contribution of noise figure at each stage and the injection currents driving complexity, the tested receiver consists of a single waveguide PIN PD integrated with two cascaded SOAs. The sensitivity of the implemented two-stage optically amplified receiver (SOA-PIN) is 1.5 dB better than that with one-stage optical amplification. Compared with two-stage SOAs, utilizing more than four cascaded SOAs is a feasible method to achieve a further reduction of the noise figure by 0.5 dB, as demonstrated in Ref. [47]. The noise figure is a ratio between the input signal-to-noise ratio and the output signal-to-noise ratio [48].

In **chapter 6**, the bias voltage of the low-dark-current PD within the optical amplification module and of the large-bandwidth UTC-PD inside the high-speed O\E module is optimized to be of the same in order to drive both PDs with a single bias feed to reduce system-level complexity. The opposite requirements of a low-voltage biased PD (the monitoring PD) for low dark current and a high-voltage biased PD (the data detecting PD) for high speed is caused by the heavy voltage-bias-dependence of the -3 dB bandwidth of the first-generation UTC-PD device. By redesigning the UTC-PD's layer stack and optimizing the fabrication process using the IMOS platform, which can make the CAO-Rx compatible with both shallowly-etched and deeply-etched SGCs, the trade-off between the PD's dark current and -3dB bandwidth is optimized. This enables the biasing of both the monitoring PD and the data-detecting PD at the same reverse voltage.

In chapter 7, a unit based on zero-volt-bias CAO-Rx was developed, designed for potential large-scale array-based OWC receivers. This aims to alleviate concerns related to voltage-bias-supply issues of the array-based OWC receiver. A novel large-aperture and large-FoV receiver concept was proposed to improve light collection with minimal bandwidth degradation in our earlier work. This novel receiver concept has been demonstrated before based on a large-scale $M \times M$ top-illuminated PD array, requiring only one TIA [49]. This PD-array-based receiver uses a combination of series and parallel interconnections. While a single CAO-Rx aperture is limited, an array of CAO-Rx can significantly increase light collection aperture without sacrificing bandwidth by using a similarly interconnected PD array. However, the use of a large PD array increases the number of PDs, resulting in a bias voltage that may exceed the capabilities of the system. In this work, we not only developed a zero-volt-bias CAO-Rx with an acceptable large bandwidth for the prototype of a 10-Gbaud OOK array-based receiver but also validated its transmission performance in a 10 Gb/s OWC link. In terms of the system performance of a 10 Gb/s on-off

keying (OOK) signal OWC link with a zero-volt-bias CAO-Rx, it was found that there was only a minor receiver sensitivity penalty (<0.2 dB) when compared to the same CAO-Rx with -1V bias. These results suggest that the zero-volt-bias UTC-PD can be applied in a CAO-Rx array.

Chapter 8 summarizes the contributions of this thesis and provides possible future routes based on the work described in this thesis.

Chapter 2

Receiver Architecture

Infrared optical wireless communication (OWC) was created to improve the "last-mile" wireless connectivity in fiber optical communication networks. The "last mile" is the final segment of the fiber optic network that connects the main infrastructure to the end user's devices, which are mostly in an indoor/short-reach environment. The infrared beam in a free-space OWC link may act as a virtual optical fiber; the maximum transmission speed demonstrated in an OWC channel achieved already speeds of up to 112 Gb/s with PAM-4 modulation [49].

The optical receiver is an essential part of the OWC system that converts free-space optical signals into electrical signals. As discussed in Chapter 1, this work focuses on studying the cascaded aperture optical receiver (CAO-Rx) for high-speed transmission. To ensure efficient and reliable data transmission, the detection scheme of CAO-Rx must meet specific criteria, as described below.

Firstly, the photodetector (PD) in the receiver must have a wide -3dB bandwidth to achieve high data rates and minimize intersymbol interference (ISI). This ISI occurs when the signal from one symbol affects the signal from a subsequent symbol, causing errors in the received data [50]. The required bandwidth is over 40 GHz, e.g., calculated by the symbol rate (112 Gb/s pulse amplitude modulation 4-level (PAM-4) signal) divided by the spectral efficiency (typically 2.8 bit/s/Hz) [51]. Equalization techniques can improve spectral efficiency and permit the use of PDs with lower bandwidth [52]. But they tend to increase complexity, cost, and power consumption and are not favored in OWC systems.

18 Receiver Architecture

Secondly, the receiver must also have sufficient sensitivity to maximize transmission speed over the required reach. This can be particularly important in a power-limited OWC link. Sensitivity refers to the minimum amount of optical power that the receiver can detect and accurately interpret as a valid signal at a given transmission speed. The maximum transmitted optical power in an infrared OWC link operating beyond 1400 nm is limited to 10 mW due to eye safety regulations [33]. The received optical power at the receiver may be low in indoor beam-steered infrared light communication (BS-ILC) systems due to the low optical coupling efficiency of the free-space beam to the receiver's PD [53]. Low efficiency can result from factors such as misalignment between the transmitter and the receiver and geometric loss caused by the mismatch of the beam to the PD's aperture and the loss of the intermediate optics (the light-collecting lenses or mirrors). The geometric loss represents the ratio between the total power in the beam spot and the power that enters into the receiver aperture [53].

2.1 State-of-The-Art of optical receivers with different detection schemes

As discussed in Chapter 1, the advanced CAO-Rx is investigated in this work. By reviewing the state-of-the-art approach, the final architecture of the targeted CAO-Rx is determined. The detection scheme used in an optical receiver plays a critical role in determining the receiver's maximum transmission speed and sensitivity and is therefore discussed first. Optical receivers with various detection schemes have been developed before, such as P-I-N PD with transimped-ance amplifier (PIN-TIA), avalanche PD with transimpedance amplifier (APD-TIA), Erbium-doped optical fiber amplifier with a P-I-N PD and transimpedance amplifier (EDFA-PIN+TIA) and semiconductor optical amplifier with a P-I-N PD and transimpedance amplifier (SOA-PIN+TIA). Key components used in these optical receiver schemes include the optical-to-electrical (O\E) conversion device (PIN PD, APD), optical amplifiers (SOA, EDFA), and the current-to-voltage converter (TIA). In Section 2.1.1, we will briefly introduce the unique properties of these components to determine which components will be used in the advanced CAO-Rx. Subsequently, we will review the state-of-the-art of optical receivers with different detection schemes in Section 2.1.2 regarding their transmission speed, sensitivity, and compactness.

2.1.1 Main components for optical receivers with different detection schemes

P-I-N photodetector

A PIN PD is a basic semiconductor device used for light detection. The device consists of a p-type layer, an intrinsic layer, and an n-type layer. The application of an external reverse bias to the contact pads generates an enhanced electric field, which depletes the intrinsic layer. When photons with energy equal to or larger than the bandgap of the intrinsic semiconductor are absorbed, electronhole pairs are generated [54]. These photogenerated carriers are then separated by the electric field and collected across the reverse-biased junction. The reverse bias voltage applied to a PIN PD can range from 0 to several tens of volts. By increasing the reverse bias voltage, the width of the depletion junction in the PIN PD is increased, which leads to a stronger electric field that can sweep out more photogenerated carriers [54]. This improves the PD's responsivity. Moreover, the wider depletion region reduces the PD's capacitance, thereby increasing its bandwidth [55]. However, a higher reverse bias voltage also results in an increased leakage current, which in turn leads to a higher dark current.

Avalanche photodetector

An APD is similar to a pin PD but has the added benefit of high internal gain. The device uses the avalanche phenomenon to amplify the photocurrent. When a photon is absorbed in the depletion region of an APD, an electron-hole pair is created. When a sufficiently high reverse bias voltage is applied, the electric field in the depletion region becomes strong enough to accelerate some of the electron-hole pairs to high velocity. This creates additional electron-hole pairs through collisions. This avalanche effect results in a higher current flow (higher output electrical signal), resulting in high sensitivity and making APDs useful in low-light applications. However, the gain and bandwidth of an APD are interrelated due to carrier impact ionization [56], which is inherently noisy and causes fluctuations not only in gain but also in time response. This interrelation is known as the gain-bandwidth limitation. As the reverse bias voltage increases, the electric field in the depletion region becomes stronger, resulting in a higher gain in the detector but lowering bandwidth. Recently, a record gain-bandwidth product value of 432 GHz was achieved by the Germanium/Silicon APD operating at 1510-nm wavelength [57]. III-V-based APDs operating at 1550-nm wavelength can achieve a gain-bandwidth product of 240 GHz [58].

Erbium-doped optical fiber amplifier

EDFAs amplify optical signals by using an erbium-doped fiber as the active medium. The input signal enters the EDFA and is directed through the erbium-doped fiber where it interacts with excited erbium ions. A pump laser excites the erbium ions in the fiber and brings them into a higher energy state which leads to the amplification of the incident signal through stimulated emission. The output is then sent through the output port. EDFAs have a gain bandwidth from 1525 to 1610 nm, covering a significant part of the low-loss window of standard single-mode fiber [59]. EDFAs usually are large and costly. The cost of an EDFA depends on its power and performance characteristics. For example, EDFAs that exhibit low dispersion, thereby minimizing signal broadening, and can deliver high output powers up to 20 dBm, often cost several thousand Euros [60].

Semiconductor optical amplifier

An SOA is a type of optical amplifier that amplifies an optical signal using quantum wells or bulk semiconductor material. The gain is created by applying an electrical current to the material to enable stimulated emission. This amplifies the incoming optical signal. The gain of an SOA depends on the semiconductor material, the length of the active region, and the current applied to this area. SOAs are typically fast, with high gain and low noise, making them suitable for use in high-speed optical communication systems. They are smaller in size than EDFAs and can be integrated with other photonic components to form photonic integrated circuits (PICs). SOAs with low polarization dependency also have been demonstrated [61]. It is important to note that the SOAs typically have a higher noise figure (NF) than the EDFAs, which can lead to more signal degradation [62]. Varying the composition of the active layer, the typical 3-dB-gain bandwidth of the SOA is 80 nm [59].

Electronic transimpedance amplifier

When light is incident on a PD, the PD generates a small current proportional to the light intensity. Directly converting the small photocurrent to a voltage swing using a small resistor load may result in a weak voltage signal that is difficult to detect in a receiver circuit [63]. However, using a large resistor load can impact the bandwidth of the PD. The electrical signal must be amplified and processed by electronic components before it can be sent to the next-stage circuit. To convert the current signal from the PD into a voltage signal

Receiver type	Sensitivity (dBm) OOK	Data rate Gb/s	Power consumption
APD+TIA [65]	-30	10	low medium
PIN+TIA [66]	-21	10	low
PIN+TIA [66]	-12.5	40	low
PIN+TIA [67]	-7.5	54	low
EDFA+PIN+TIA [68]	-27.8	40	high
SOA+PIN+TIA [69]	-20	25	medium
Discrete SOA+PIN +bandpass filter [69]+TIA	-22	25	medium
Integrated SOA+PIN+TIA [61]	-25.7	10	medium
Integrated SOA+PIN+TIA [61]	-21	40	medium

Table 2.1: Typical optical receivers with \geq 10 Gb/s data rate at BER of 10⁻⁹

with minimal impact on the -3dB bandwidth, a TIA is used when its -3dB bandwidth can satisfy the system requirements [64]. The transimpedance of the TIA, which is the ratio of output voltage to input current in the circuit and is measured in ohms, allows it to amplify the small current signals generated by the PD. A typical TIA consists of a resistor connected in the feedback loop across a junction-gate field-effect transistor (JFET) or a metal-oxide-semiconductor field-effect transistor (MOSFET), which serves as the input stage.

2.1.2 Evaluation of Different detection schemes of optical receivers

The state-of-the-art optical receivers enabled by different detection schemes are reviewed in the following. Table 2.1 shows the reported optical receivers enabled by different detection schemes. Several researchers have demonstrated a range of high-speed and high-sensitivity optical receivers, including APD-TIA [65], PIN-TIA [66], separated SOA-pin [69], EDFA-PIN-TIA [68] and monolithically integrated SOA-PIN+TIA [61]. The conventional PIN-TIA, which has a relatively low sensitivity, can support beyond 54 Gb/s [67]. The APD-TIA has the highest receiver sensitivity at a lower data rate, shown in Table 2.1. However, at 40 Gb/s, an APD faces difficulties in achieving a high sensitivity due to its limitation of the gain × bandwidth product [66]. A complex high-voltage driver, including a controller, is needed for the APD with a well-controlled high

gain to achieve high sensitivity [70]. Commercial APDs with a transmission speed above 10 Gb/s and sufficient gain are rare [71]. The detection scheme used in the CAO-Rx should support beyond 112 Gb/s transmission speed mentioned at the beginning of this chapter. Achieving this goal is a challenge with the use of an APD.

Another high-sensitivity detection scheme that supports high data rates is the EDFA-PIN-TIA scheme, in addition to the high-sensitivity APD+TIA scheme. Using an EDFA as the optical preamplifier in an optical receiver can increase the sensitivity of the receiver, allowing it to detect weaker optical signals [68]. This can be particularly useful in long-haul optical communication systems, where the optical signal is attenuated due to losses in the optical fiber. Additionally, an EDFA with a gain tuning option can increase the dynamic range of the receiver, allowing it to handle a larger range of signal levels without distortion. The EDFA-PIN-TIA comes with a large footprint and high receiver cost, which is not suitable for OWC.

A waveguide integrated PD is proven to exhibit high bandwidth and high responsivity [55]. An SOA is electrically pumped, and it is easy to make the driver for an SOA. Moreover, an SOA can amplify beyond 112 Gb/s PAM-4 signal [32]. So both components, the SOA and waveguide integrated PD, can meet the requirement of future development of a compact OWC receiver module. Due to SOA's suitability for integration, waveguide PDs can be integrated with SOAs based on photonic integrated circuit technology. Despite the typically higher noise figure (NF) of SOAs compared to EDFAs [62], it is very promising to integrate SOAs with the waveguide-integrated PIN and use this as a high-sensitivity high-speed optical receiver.

2.2 Architecture choice for the targeted CAO-Rx receiver

In this section, the minimum sensitivity of the optical receiver used in the targeted beam-steering system is determined through calculation. A receiver design is proposed based on an evaluation of existing detection methods and calculations. An analysis of the system considerations of the proposed optical receiver is carried out. Based on the analysis, research tasks have been identified and set for this work, with the goal of enhancing the receiver's performance.

2.2.1 Sensitivity requirement for high-speed optical receiver in beam-steered infrared light communication

The PIN-TIA and SOA-based-PIN-TIA detection schemes both support high-speed transmission at rates of 40 Gb/s or higher and have a compact size, as discussed in Section 2.1.2. These schemes can be adopted in the CAO-Rx. The latter has improved receiver sensitivity over the former, but the former has lower power consumption. The power consumption of the OWC receiver is also a key factor to consider. The suitability of the PIN-TIA detection scheme for high-speed optical receivers in the targeted BS-ILC system should be verified in terms of its sensitivity. We then calculate the relationship between BER performance and input optical power, taking into account various beam spot diameters at a transmission speed of 40 Gb/s.

In a narrow-beam OWC link, the diameter of the narrow beam is smaller than or equal to the aperture of the receiver. We assume that the narrow beam and the receiver have been accurately aligned, enabling the OWC receiver to capture the optical power in a narrow-beam OWC link fully. To ease alignment and improve tracking, a wider beam can be used. If the beam size exceeds the receiver aperture and the receiver cannot capture the full power of the beam, the received optical power can be calculated using Eq. 2.1 [72] under the assumption of a well-aligned beam with a uniform profile:

$$P_{rx_min} = P_{beam} \frac{D_{rx}^2}{D_{beam}^2} (1 + \frac{L^2}{2H^2})^{-1}$$
 (2.1)

where P_{rx_min} is the minimum received power level, P_{beam} is the total optical power in the beam, D_{rx} is the receiver aperture, D_{beam} is the beam diameter, the scanned area of the two-dimensional (2D) beam steering module is $L \times L$, and H is the height of the 2D beam steering module. The geometric loss, denoted as the L_{beam} , is the product of the right two terms. The diagram depicting the geometric relationship associated with the geometric loss L_{beam} , as described in Eq. 2.1, can be found in ref. [72]. The assumption in this analysis is that the power received by the receiver is not limited by the receiver's field of view (FoV). Such an assumption is valid when the beam is pointed at the active absorption area of the receiver.

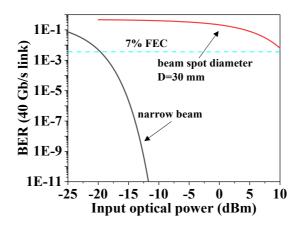


Figure 2.1: Theoretical BER performance versus input optical power by using the receiver with the 1-mm aperture at different beam spot diameters for a 40 Gb/s OOK signal. As the diameter of the narrow beam is less than 1 mm, the OWC receiver can fully capture the optical power of the narrow beam.

For the optical link with the on–off keying (OOK) modulated signal, the bit error ratio (BER) for a PIN-TIA optical receiver can be calculated by a simplified equation [73,74]:

$$BER = 0.5erfc(\sqrt{\frac{E_b}{N_0}})$$
 (2.2)

where E_b (= P_{rx_min}/R_b) is the bit energy, P_{rx_min} is the minimum received power, and R_b is the bit rate of the link; N_0 (= P_N/B_r) represents the optical noise power energy (in W/Hz), with P_N as the optical noise power and B_r as the receiver bandwidth. In the given simplified equation, only the signal power and the noise power from the optical domain are taken into account. The receiver efficiency, which includes both the coupling efficiency and the quantum efficiency of the PD, is not considered in this model. An OOK modulated signal and PAM-4 modulated signal are typically used in the OWC link. To attain the same symbol rate, a receiver for a PAM-4 signal requires 4.8 dB more received optical power than that receiving OOK signal [75].

The relation between the BER performance of an optical receiver for 40 Gb/s OOK signal as a function of the input optical power at different beam spot diameters is calculated based on Eq. 2.1 and Eq. 2.2, shown in Figure 2.1.

A prototype of a 2D beam-steering module with a 3-cm diameter beam was demonstrated in our previous work, and the optical receiver aperture, denoted as D_{rx} , is set as 1 mm [72]. Utilizing external optics, such as a parabolic concentrator or condenser lens, may increase D_{rx} but also limits the FoV due to the restrictions of the etendue law [11]. The other system parameters utilized in our previous work for designing the beam-steering demo, as outlined in [72], are used for the calculation. The length of the $L \times L$ scanned area is 1.5 m, and the ceiling height H=2.5 m. According to Eq. 2.1, the geometric loss L_{beam} is -30.3 dB. The receiver bandwidth is 40 GHz. The ambient optical noise power normally is in the order of several μ W [76], so we choose P_N = 3 μ W. For the wide spot beam, we use Eq. 2.1 for calculating the minimum received optical power.

Seen from Figure 2.1, the calculated minimum required receiver sensitivity for a narrow-beam link operating at 40 Gb/s with OOK signal is -12.6 dBm, corresponding to a BER of 10⁻⁹. This result matches the reported BER performance of the PIN-TIA optical receiver presented in Ref. [66]. In the reference, it achieved a receiver sensitivity of -12.5 dBm at a BER of 10^{-9} in 40 Gb/s link. Then the sensitivity of this pin-TIA optical receiver in the OWC link with a 30mm-diameter beam can be estimated by using the calculated results shown in Figure 2.1 under 7% FEC limit. In an OWC link, it can use forward error correction (FEC) to correct bit errors in the received data to improve the receiver sensitivity. As long as the pre-FEC BER is below the FEC limit, all bit errors are successfully identified and corrected, and, therefore, no packet loss occurs [77]. Therefore, a pin-TIA optical receiver may use in a wide-beam link. Due to the eye safety regulation, the maximum allowed optical power in the link is limited to 10 dBm. The optical receiver based on the pin-TIA detection scheme meets the system capacity requirements under 7% FEC when it is used in a wide-beam 40-Gb/s OWC link.

Besides, one approach to further extend the aperture of the CAO-Rx is by applying an array of surface grating couplers (SGC-s) followed by a waveguide light combiner. The inherent insertion loss of a $2^N \times 1$ MMI-based power combiner is equal to 3N dB, where 2^N is the number of input waveguides [78]. As a consequence, the UTC-PD, followed by the MMI-based power combiner, will receive less optical power. The first preliminary concept of the CAO-Rx in our previous work was based on the uni-traveling-carrier photodetector (UTC-PD) (a variant of PIN PD), which has no internal gain [40]. The sensitivity of this receiver should be comparable to that of the PIN-TIA optical receiver. The use of a beam-steered infrared light communication (BS-ILC) system with a 30-mm

beam spot diameter results in low optical power reception, shown in Figure 2.1, while the high insertion loss of the MMI-based power combiner can exacerbate the issue. The preliminary concept of the CAO-Rx may not satisfy the system requirement.

Therefore, it is important to investigate alternative solutions, such as an advanced and high-sensitivity CAO-Rx. In order to determine the appropriate configuration of the advanced CAO-Rx, an estimation of the power budget for the link is essential. The estimation can be achieved by considering two optical receiver schemes: the SOA-PIN+TIA scheme and the PIN-TIA scheme. These receiver schemes are frequently utilized in the design of high-speed OWC receivers that support transmission rates exceeding 10 Gb/s. In this estimation, a 7% FEC limit is taken into account. As shown in Table 2.1, the receiver sensitivity of the SOA-PIN+TIA scheme is roughly 10 dB higher compared to that of the PIN-TIA scheme within the same data rate link. Based on the calculated relation depicted in Figure 2.1, we can determine the power budget for the 40-Gb/s OWC system. The calculation is based on the following system parameters: a 30-mm beam spot and a receiver aperture diameter of 1 mm. Taking into account a reserved system margin of 3 dB [79], the power budgets for these schemes are 7 dB and -3 dB, respectively. A sufficient power budget for high-speed optical wireless transmission is required to maximize the transmission speed. An SOA used as an optical amplifier is crucial in enhancing the sensitivity of the OWC receiver for maximum-speed data transmission. The utilization of photonic integrated circuit technology enables the integration of SOAs and waveguide PDs with minimal assembly complexity [80]. And the trend in optical wireless communication is to pursue higher transmission speeds. Therefore, a new component, the SOA, will be integrated into the CAO-Rx to achieve higher sensitivity for maximizing the transmission speed. Hence, the high-sensitivity CAO-Rx with optical preamplifiers should be investigated.

2.2.2 Proposed CAO-Rx scheme with optical preamplifiers

The proposed high-sensitivity CAO-Rx consists of five modules: the light collection module (a large-aperture SGC and a lens), the optical amplification module (an on-chip optical power monitor, and SOAs), a tunable optical bandpass filter (OBPF) module, the high-speed optical-to-electrical (O\E) (large-bandwidth UTC-PD) module, and an electronic TIA module. Figure 2.2 shows the schematic of the CAO-Rx chip design without a lens. The signal optical beam from free space is first coupled into the receiver via the light collection module. The grating coupler within the light collection module is a crucial component

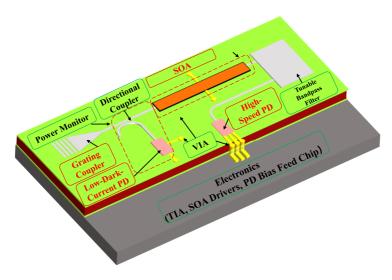


Figure 2.2: Diagram of a proposed high-sensitivity CAO-Rx. SOA: semiconductor optical amplifier; PD: photodetector; TIA: transimpedance amplifier.

of the CAO-Rx [43]. It enables the CAO-Rx to achieve a large light collection aperture while maintaining high electrical bandwidth. With an apodized design, the SGC can achieve receiving apertures larger than 10000 μ m² [40]. Then the power of the received weak signal light will be boosted by the on-chip optical amplification module. The optimal injection current for the SOA varies depending on the input optical power, as the gain and noise figure of the SOA are determined by both the injection current and input optical power [81]. To provide an adaptive current injection scheme in order to optimize the amplification for the best performance, an on-chip optical power monitoring unit is needed to capture the incoming light and give feedback regarding the input power of the SOAs. The optical power monitor contains a directional coupler cascaded with a low-dark-current UTC-PD. The use of a UTC-PD as an optical power monitor is due to the choice of the data detection PD. Both the PIN PD and UTC-PD can be used for power monitoring. However, the UTC-PD has been demonstrated to have higher bandwidth [82] and is therefore used as the data detection PD in this work. Since the layer stack of the PIN PD and UTC-PD differ from each other, using the UTC-PD as the power monitoring PD simplifies the wafer epitaxy process. The tunable OBPF module mainly filters the out-of-band

amplified spontaneous emission (ASE) noise from the SOAs. Unfiltered ASE can result in a high penalty due to ASE-ASE beat noise [61,69]. The high-speed UTC-PD inside the O\E module is for converting the modulated optical signal into a high-speed electrical signal. Finally, the high-speed electrical signal is amplified by the on-chip TIA. The close integration of the TIA and the high-speed PD can effectively mitigate signal degradation caused by bonding wire [83,84]. This on-chip system is able to address both high-speed signal detection and optical performance monitoring. This system is targeted to be validated on the InP-membrane-on-Silicon (IMOS) platform, which in the future can realize the fully integrated CAO-Rx, including the optical and electronic amplifiers, within a compact size.

2.2.3 System Considerations of the CAO-Rx with Optical Amplifiers

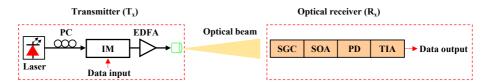


Figure 2.3: Block diagram of a LOS infrared light communication link with the advanced cascaded aperture optical receiver (CAO-Rx). The power monitor module of this CAO-Rx is not shown. PC: polarization controller; IM: intensity modulator; EDFA: Erbium-doped fiber amplifier; SGC: surface grating coupler; SOA: semiconductor optical amplifier; PD: photodetector; TIA: transimpedance amplifier.

A block diagram of a line-of-sight (LOS) infrared light communication link is presented in Figure 2.3. The transmitter modulates electrical data onto the instantaneous intensity of an optical beam via an intensity modulator (IM). The modulated optical signal is then amplified by an EDFA, and launched into the free space, whose optical power is represented by P_t . Here according to the human eye safety standard of International Electrotechnical Commission (IEC) 825-1 in infrared optical wireless system, the maximum value of P_t is limited to 10 mW. LOS systems typically use a narrow optical beam which maintains a high power flux density at the receiver. It is worth noting, however, that this approach requires careful beam alignment to reach the OWC receiver.

In a power-limited LOS OWC system, the proposed high-sensitivity CAO-Rx needs to optimize the output electrical signal-to-noise ratio (SNR) in order to maintain a high-speed data transfer rate. The electrical SNR represents a critical factor in determining the optical receiver's ability to accurately detect incoming optical signals [85]. Therefore, it is essential to identify and clarify the factors that influence the electrical SNR of the receiver. The output electrical SNR of the CAO-Rx with optical preamplifiers is defined as

$$SNR = \frac{i_s^2}{\sigma^2} = \frac{i_s^2}{\sigma_{sp-sp}^2 + \sigma_{sig-sp}^2 + \sigma_s^2 + \sigma_{n,TIA}^{RMS}}$$
(2.3)

where i_s is the total signal current, σ_{sp-sp} is the amplified spontaneous emission (ASE)-ASE beat noise, σ_{sig-sp} is the signal-ASE beat noise, σ_s is the shot noise, and $\sigma_{n,TIA}^{RMS}$ is the TIA noise.

By minimizing excess loss and selecting an appropriate splitting ratio, the insertion loss of the proposed CAO-Rx directional coupler (shown in Fig. 2.2) can be significantly reduced to a value typically below 1 dB [86]. Since the directional coupler is positioned before the SOA, the insertion loss associated with the directional coupler can be taken into account as a contributing factor to the overall coupling loss. For the proposed CAO-Rx with the optical amplifier, the total signal current can be expressed as

$$i_{s} = \overline{P}_{s}GR_{E} \tag{2.4}$$

where \overline{P}_s is the received average signal optical power, R_E is the external responsivity of the detector, and G is the gain of the SOA.

The received average signal optical power \overline{P}_s can be expressed as [87]:

$$\overline{P}_s = \overline{P}_r \times \frac{\alpha^2}{\alpha^2 + 1} \tag{2.5}$$

where \overline{P}_r is the received average optical power. α is the modulation depth at the transmitter. α is defined as V_s/V_c , where V_s and V_c are the amplitudes of the signal and carrier, respectively. Since the square of the amplitude of the light is equal to its optical power, the modulation depth α can also be denoted as $\sqrt{\frac{P_s}{P_c}}$, where P_s is the message optical signal and P_c is the carrier optical power. The \overline{P}_r is related to the receiver aperture when the transmitted optical power is given in a typical OWC link.

The PD's external responsivity R_E can be expressed as

$$R_F = R_{PD} \times 10^{\frac{\eta}{10}} \tag{2.6}$$

where R_{PD} is the PD's internal responsivity, and η is the coupling efficiency (unit: dB).

The total noise current variance σ^2 can be expressed as

$$\sigma^{2} = 4R^{2}S_{sp}^{2}B_{0}\Delta f + 4R^{2}G * 10^{\eta} * P_{r}S_{sp}\Delta f + 2q\left[R(G * 10^{\eta} * P_{r} + S_{sp}B_{0})\right]\Delta f + v_{n \ out}^{RMS}/R_{T}$$
(2.7)

where the four terms of the sum on the right-hand side of the equation describe, respectively, ASE-ASE beat noise, signal-ASE beat noise, shot noise, and TIA noise. The first two terms are related to the ASE noise. The values denoted by S_{sp} , B_0 , Δf , $v_{n,out}^{RMS}$, and R_T are, respectively, the ASE spectral density, optical bandpass filter bandwidth, receiver bandwidth, measured output noise voltage, and the transimpedance gain mid-band value. The dark current of the detector is small compared to the photocurrent and therefore is ignored. In a previous numerical analysis of various noise sources within the optical pre-amplified receiver, Angelini et al. demonstrated that the ASE noise plays a dominant role [88]. And the signal-ASE beat noise was found to be significantly larger than the ASE-ASE beat noise by a factor of several times in Ref. [88].

The relation between a PD's signal current i_s and the receiver sensitivity can be expressed [85]:

$$i_s = Q \times \left\langle \sigma^2 \right\rangle^{1/2} \tag{2.8}$$

where Q is the parameter related to the minimum SNR ratio required to obtain a specific BER. For example, at Q=6, the corresponding BER value is 10^{-9} .

2.2.4 Research tasks described in this thesis

To maximize the sensitivity of the proposed high-sensitivity CAO-Rx with optical preamplifiers (Figure 2.2), the analysis in Section 2.2.3 highlights the crucial objective of increasing the optical signal power received by the high-speed UTC-PD before SOA saturation. It is important to note that when the SOA becomes saturated, its noise figure increases, which can degrade the signal quality [89]. To achieve this objective, two research tasks have been established.

Research task 1.1 (Chapter 4) aims to improve the coupling efficiency η of the light collection module to reduce the optical signal loss. To achieve a specific BER value, the corresponding Q value in Eq. 2.8 is fixed. According to Eqs.

2.8 and 2.6, if the $\langle i_n^2 \rangle$ and WGPD's internal responsivity R_{PD} are optimized, improving the coupling efficiency of the SGC helps to obtain a high external responsivity of grating-assisted PD, resulting in a high receiver sensitivity (lower received optical power \overline{P}_r). $\langle i_n^2 \rangle$ is the mean square noise current referenced to the photocurrent.

Research task 1.2 (Chapter 5) focuses on optimizing the optical amplification module by developing a novel SOA-noise-reduction scheme to provide a higher on-chip gain without signal quality degradation. Previous research clarified that the ASE noise was the main contributor to the source of noise in the SOA-pin+TIA optical receiver [88]. Optimizing the injection current of the SOA is a possible way to enhance the SNR in the optical domain. This is because the gain and ASE noise of the SOA are linked to its injection current [89]. As described in Eqs. 2.3, 2.4, 2.7, and 2.8, this improvement, in turn, increases the receiver's electrical SNR, resulting in improved sensitivity.

The advanced CAO-Rx has more functionalities, which demands more complex circuits and driver circuits. As described in the introduction of the optical amplification module in Section 2.2.2, an on-chip optical power monitor is added to inject a current into the SOAs, which is adapted for obtaining optimum noise figure. Therefore, a high-sensitivity monitor design is made to decrease the coupling loss from the received signal light into the waveguide. A low-darkcurrent UTC-PD (typically with a dark current < 10 nA [90]) is achieved in order to meet the higher-sensitivity requirement. The low-dark-current UTC-PD (the monitoring PD) and the high-speed UTC-PD (the data-detecting PD), based on the first-generation UTC-PD device on the IMOS platform, are usually biased at different voltages. Note that the UTC-PD is also used as the monitoring PD to match the choice of high-speed PD, which is also the UTC-PD. Further details on this aspect are discussed in Section 2.2.2. The opposite requirement of a smallvoltage biased PD for low dark current and large-voltage biased PD for high speed is caused by the heavy voltage-bias-dependence of the -3 dB bandwidth of the first-generation UTC-PD device [55]. It is desired to bias the monitoring PD and the data detecting PD at the same reverse voltage to simplify the electronic circuitry to reduce the complexity at the system level.

In **research task 2** (Chapter 6), the goal is to optimize the fabrication process of UTC-PDs to achieve devices with high responsivity, large bandwidth, and low dark current at a specific bias voltage while minimizing this voltage to reduce the electronic circuit requirements. This allows for the use of only one bias feed chip. Furthermore, by optimizing the driving voltage of these PDs to be below the reverse bias voltage of 1.5 V, the low drive bias of this type of UTC-PD meets the requirements for heterointegration with a CMOS chip [82,91]. This allows

for full utilization of the benefits of the IMOS platform and facilitates the close integration of high-speed PDs and electronic amplifiers on CMOS chips, which improves the overall receive performance [39]. This approach effectively eliminates parasitic effects commonly associated with hybrid integration utilizing wire bonding, including the parasitic capacitance from bonding pads and parasitic inductance from bonding wires [92, 93]. Additionally, the heterogeneous integration reduces both assembly complexity and costs [94]. In comparison to hybrid integration, which involves connecting multiple dies with bonding wires, heterogeneous integration is particularly well-suited for high-volume applications [95]. This makes it an ideal choice for the large-scale implementation of OWC receivers in the future.

As indicated by Eq. 2.1, increasing the receiver aperture D_{rx} to 5 mm reduces the sensitivity required for the optical receiver as more power of the beam is captured. To support a 40 Gb/s OOK signal with a wide-beam link, the receiver sensitivity should be below -5 dBm. Then the pin-TIA detection scheme can be implemented, which reduces the additional power consumption of the SOAs. To further increase the aperture of an on-chip OWC receiver, a receiver array architecture can be considered. To overcome the inherent trade-off between bandwidth and aperture (so power coupling factor), a novel large-aperture receiver concept was proposed to improve light collection with minimal bandwidth degradation in our earlier work [35]. This novel receiver concept has been demonstrated before based on a large-scale $M \times M$ top-illuminated PD array, requiring one TIA. The PD array is based on series and parallel interconnections. It is able to achieve a large aperture with square millimeters area and a large FoV simultaneously.

Since a single CAO-Rx has a trade-off between its aperture and its FoV [46], the CAO-Rx array can break this trade-off by the inherent advantage of the CAO-Rx (i.e., separately optimizing light collection and electrical detection). Thus, a CAO-Rx array is able to enormously enhance the light collection and maintain an acceptable field of view, where its waveguide PD array is also with series and parallel interconnection. Whether it is a top-illuminated PD array or a CAO-Rx array (a waveguide PD array), the number of PDs will inevitably increase compared to an optical receiver with a single PD. This increase in PD number may require a bias voltage that exceeds the capabilities of the system. The voltage-bias design of a large-scale PD array (e.g., $M \times M$) will require an additional bias feed chip and increase system complexity. A non-biased PD (or zero-volt-bias PD) would be a good solution for the array-based OWC receiver. Thus, **research task 3** (Chapter 7) is about developing a unit based on zero-volt-bias CAO-Rx for a potential large-scale array-based OWC receiver to relax the voltage-bias-supply stress.

2.3 Chapter Summary

In this chapter, the receiver architecture has been discussed. Firstly, the optical receiver architectures with different detection schemes have been reviewed. Additionally, we calculate the required receiver sensitivity of the OWC receiver for the beam-steering system employing a 3-cm-diameter beam. Based on the calculation results and a review of high-sensitivity detection methods, a novel high-sensitivity CAO-Rx architecture with optical preamplifiers is proposed. Finally, the research tasks for improving the performance of the advanced CAO-Rx have been outlined.

Chapter 3

Photonic Integration Platforms for This Project

3.1 Introduction

In the previous chapter, the key components of the advanced cascaded aperture optical receiver (CAO-Rx) were discussed, with the semiconductor optical amplifier (SOA) being a particularly important component. Given that the InP platform offers the benefit of monolithic integration of SOAs and lasers, the advanced CAO-Rx was investigated based on an InP-based photonic integration platform. In our previous work, the first preliminary concept of CAO-Rx was demonstrated on the TU/e InP membrane-on-silicon (IMOS) platform, and ongoing research continues to investigate the advanced CAO-Rx on the IMOS platform. And the IMOS platform, as envisioned by its designers, is expected to enable the heterointegration of photonic and electronic circuits [96]. This has the potential to enable the full integration of a CAO-Rx system with optical amplifiers and electronics on the IMOS platform. Previously, achieving the integration of SOAs and high-speed PDs on the IMOS platform posed a significant challenge. However, considerable progress has been made in developing this integration. A promising approach to bridging the current gap in this rapidly evolving IMOS technology is to utilize the well-established Fraunhofer HHI InPbased photonic platform. Notably, the HHI platform has been optimized for receiver applications, making it a particularly suitable option for our research. However, the small refractive index contrast of the HHI platform hinders the successful realization of the surface grating coupler (SGC) on the HHI platform, which is a crucial component of the proposed CAO-Rx design [97]. As a result, the full functionality of the proposed CAO-Rx cannot be achieved on the HHI platform. As a preliminary validation step of our concept, we tested the SOA scheme on the HHI platform before implementing it on the IMOS platform, which will involve integrating SOAs into the CAO-Rx. This chapter provides a brief introduction to these two photonic integration platforms that are involved in our work.

3.2 Introduction to IMOS photonic integration platform

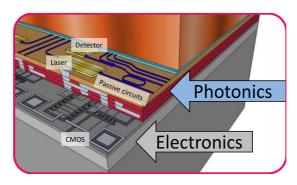


Figure 3.1: Schematic of the fully functional IMOS platform with active and passive photonic components in the thin InP membrane and active photonic devices connected to CMOS electronics (electronic amplifiers and drivers) [96] (© [2020] IEEE, Reprinted, with permission, from Ref. [96]).

Figure 3.1 presents a schematic of the fully functional Indium Phosphide membrane on Silicon (IMOS) platform. One envisioned concept of this platform is its ability to bond a thin InP membrane layer to the surface of a CMOS wafer, allowing for the integration of Complementary Metal-Oxide-Semiconductor (CMOS) electronics and optical elements with full photonic functionality. The high refractive index contrast of the IMOS platform is especially advantageous, as it can significantly reduce the size of the chip. The platform has the capability for double-sided processing, which allows for the integration of components with different layer stacks while minimizing the need for regrowth steps [98,99]. The

platform enables easy transmitter (Tx) and receiver (Rx) integration. In addition, using electrical vias through the bonding layer allows active photonic components to be connected to electronic circuits, effectively merging photonic and electronic functions. Shorter connections between detectors and electronic amplifiers lead to reduced parasitic loss [100], which is advantageous for achieving a high-speed optical receiver. The InP-based material system offers two major advantages: 1) the ability to integrate both active components (such as lasers, detectors, and modulators) and passive components (such as waveguides, filters, couplers, and demultiplexers) in a single layer and 2) the ability to leverage or adapt mature technologies developed in generic InP foundries for use on the InP membrane platform [101].

3.2.1 Performance of building blocks on the IMOS platform

A wide range of passive and active building blocks have been demonstrated on the IMOS platform. More recently, successful on-chip connections have been established between active photonic components on the InP membrane and electronic devices on the CMOS wafer [84]. A summary of the performance of basic building blocks on the IMOS platform is given in Table 3.1. The IMOS platform is ready to support open-access multi-project wafer run [102].

Table 3.1: Performance overview of the main IMOS platform building block

waveguide [102] Microring [106]	Q = 62000 (Scanner patterned)
Bending	$0.03 \text{ dB/90}^{\circ}$ at 5 μ m radius
Single-mode waveguide [106]	(Scanner patterned) dimension: 300×400 nm ²
	loss: 1.8±0.1 dB/cm
SGC with metal reflector [105]	loss: 2.4 dB~ 2.6 dB
SGC without metal reflector [103, 104]	loss: 5 dB∼12 dB
Basic device	Specification

Table 3.1 – continued from previous page

Specification	
loss: 3.5 dB; cross talk >20 dB	
(Scanner patterned)	
$110~\mathrm{cm^{-1}}$ net modal gain @4 kA cm $^{-2}$	
2.5 kA cm ⁻² threshold current	
13 mW in the waveguide	
-3 dB bandwidth: > 67 GHz	
responsivity: 0.7 A/W	
dark current: 146 nA@-4V	

The essential components required for the proposed CAO-Rx receiver, such as the SGC, microring, SOA, and high-speed PD, have been successfully developed on the IMOS platform. Therefore, it is important to assess the feasibility of directly utilizing these existing building blocks as sub-components within the proposed CAO-Rx. The SGC and the high-speed PD represent two of the most crucial sub-components of the proposed CAO-Rx. The subsequent discussions primarily focus on these two crucial components. Two types of SGCs have been developed: the metal-reflector-assisted SGC (MRSGC) and the ordinary SGC without a metal reflector. The coupling loss of the MRSGC is significantly reduced, as shown in Table 3.1, compared to that of the ordinary SGC. As discussed in Section 2.2.1, one approach to expanding the aperture of the CAO-Rx is by utilizing an array of the SGC followed by a waveguide light combiner. However, it should be noted that doubling the connected SGC results in an additional 3dB insertion loss. The additional loss resulting from the implementation of the SGC array can be expected to be partially compensated by utilizing the MRSGC with reduced coupling loss. Since the SGC with a metal reflector and the highspeed PD have never been integrated together before, a solution of utilizing the more efficient SGC and the WGPD in a CAO-Rx is desired. The first-generation high-speed PD (UTC-PD) demonstrated on the IMOS platform has been demonstrated with wide -3dB bandwidth, which can support beyond 112 Gb/s PAM-4 transmission speed. This PD can be used as the data-detecting PD in the proposed CAO-Rx. Additionally, as discussed in Chapter 2, the proposed CAO-Rx includes another PD for monitoring input optical power. To simplify the related bias feed circuits, it would be advantageous if both the monitoring PD and the data detecting PD could be driven by a single bias feed chip, biased under the same voltage. However, the low-dark-current UTC-PD (the monitoring PD) and the high-speed UTC-PD (the data-detecting PD), based on the first-generation UTC-PD device on the IMOS platform, are usually biased at different voltages. This opposite requirement arises from the heavy voltage-bias-dependence of the -3 dB bandwidth in the first-generation UTC-PD device. Consequently, the development of a new generation of UTC-PD becomes necessary.

3.2.2 Fabrication flow of the SGC-assisted waveguide UTC-PD on IMOS platform

The detailed fabrication process can be referred to Ref. [82]. In this section, the fabrication process is briefly outlined, along with the key adjustments implemented by the author. The IMOS chips mentioned in Chapters 4, 6, and 7 were fabricated by the author in the Nanolab at Eindhoven University of Technology.

Here is the general fabrication flow for the topside process. The whole processing starts from the epitaxy of the UTC-PD function layer on the semiinsulating InP substrate. The UTC-PD wafer in Figure 3.2 (a), which is with the redesigned layer stack, was grown epitaxy through Metal-Organic Chemical Vapor Deposition (MOCVD) tool. In Chapter 6, a comprehensive introduction of the redesigned layer stack will be provided, including detailed information and specifications. At first, we define p contact on p doped In_{0.53}Ga_{0.47}As layer by a lift-off process. Subsequently, a mesa of In_{0.53}Ga_{0.47}As is defined through selective etching, as shown in Figure 3.2 (b), utilizing an extremely dilute solution of H₂SO₄/H₂O₂/H₂O and ultraviolet (UV) lithography thick resist as the mask. The use of an extremely diluted solution results in a slower etching rate, which can precisely control the size of the In_{0.53}Ga_{0.47}As mesa. Alignment markers are transferred to the InP wafer using CH₄/H₂-based inductively coupled plasma (ICP) dry etching with a SiN_x hard mask. A thin SiO₂ layer is then deposited on both the Si and InP wafers, and a thin metal layer of Germanium (Ge)/ Silver (Ag)/ Gold (Au) is defined in a specific area, as shown in Figure 3.2 (c). This thin metal layer serves as the metal reflector for the metal reflector-assisted surface grating coupler, which will be introduced in Chapter 4. The InP wafer is then bonded to a SiO₂/Si carrier wafer using Benzocyclobutene polymer (BCB). Following the wafer bonding process, the InP substrate is removed by etching the wafer with a concentrated HCl/H₂O solution (Figure 3.2 (d)). The resulting samples have a functional UTC-PD membrane on silicon.

The general fabrication flow for the backside process is shown in Figure 3.3. The process starts with the removal of the $In_{0.53}Ga_{0.47}As$ sacrificial layer (Figure 3.3 (e)). Next, Nickel(Ni)GeAuGeAu ohmic contacts are defined on n-InP using a lift-off process, followed by rapid thermal annealing. A selective etch

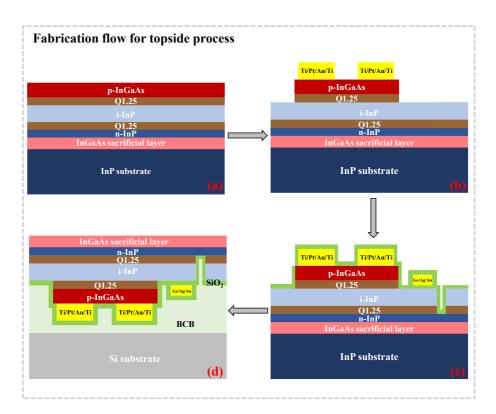


Figure 3.2: Topside fabrication flow of the membrane-based waveguide uni-traveling-carrier photodetector (UTC-PD). (a) InP wafer stack; (b) p contact definition and p-InGaAs mesa formation; (c) alignment marker etch and metal reflector definition; (d) bonding UTC-PD function layer to silicon and remove InP substrate.

solution of HCl/H_3PO_4 is then used to form the n-InP mesa, using the n-contact metal as a mask and Q1.25 quaternary material as an etch stop layer. The extremely dilute solution of $H_2SO_4/H_2O_2/H_2O$ is then used to remove the Q1.25 layer outside the n-InP mesa. The PD mesa and waveguide are then defined by ICP CH_4/H_2 dry etching in one step. In the next step, the surface grating coupler is formed by ICP CH_4/H_2 dry etching with SiN_x as a hard mask. The wafer is then wet-chemically cleaned using a combination of extremely dilute

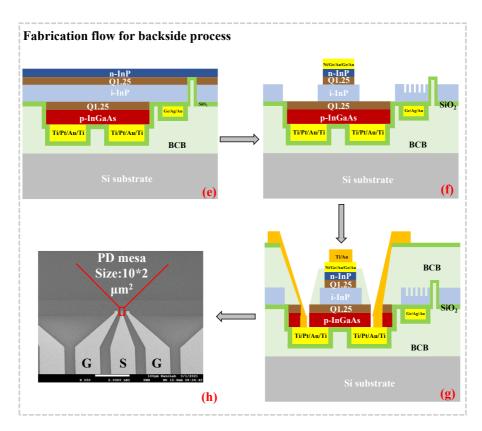


Figure 3.3: Backside fabrication Flow of the membrane-based waveguide UTC-PD. (e) remove InGaAs sacrificial layer; (f) n contact definition, PD mesa definition, waveguide, and surface grating etch; and (f) Benzocyclobutene (BCB) planarization, p contact open, and ground-signal-ground (GSG) transmission line and GSG pad formation; (h) scanning electron microscope (SEM) image of a waveguide uni-traveling carrier photodetector (UTC-PD) with a 10 ×2- μm^2 PD mesa size and a GSG pad.

 $\rm H_2SO_4/H_2O_2/H_2O$ and dilute HF to achieve a low dark current PD [110] (Figure 3.3 (f)). BCB is used as the planarization material for passivation and planarization [111]. In Chapter 6, the motivation behind the use of BCB planarization material and the combination wet-chemical treatment will be explained in de-

tail. The metal contact pad is opened, and a thick Titanium (Ti)Au metal layer is deposited to create the ground-signal-ground (GSG) transmission lines and probe pads for measurement (Figure 3.3 (g)).

3.2.3 Characterization setup for the IMOS chips

The setup used to characterize the IMOS vertical-coupling device is presented in Figure 3.4. The fabricated IMOS chip is placed on a holder, and vertically cleaved single-mode fibers are used as fiber probes, which are precisely positioned using 3-dimensional positioners to achieve optimal alignment. To facilitate alignment between the fiber probe and the surface grating coupler (SGC), a charge-coupled device (CCD) camera with a tilt angle is used. When characterizing the active device, the fiber probe on one side can be replaced by

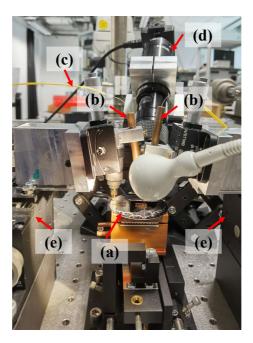


Figure 3.4: Picture of the characterization setup for the IMOS passive structure, comprising (a) a fabricated IMOS chip; (b) fiber probes; (c) single-mode optical fiber; (d) microscope camera; (e) 3-dimensional positioners.

metal probes, and the optical microscope should be used accordingly to see the metal probes clearly.

- (a) Fabricated IMOS chip The characterization setup is designed to measure chips smaller than 1 inch in diameter. Although a 2-inch wafer can be placed on the copper wafer holder, the movement range of the fiber probe is limited to less than 1 inch. Therefore, a quarter-sized chip from a 2-inch InP wafer is used in this work. To hold the chip securely during testing, a vacuum can be used to maintain its position on the wafer holder.
- **(b,c)** Fiber probes and the single-mode fiber The fiber probe is created by removing the coating layer from one end of a single-mode fiber and vertically cleaving the fiber end. The angle of the fiber probe can be adjusted from 2° to 12° with respect to the normal line to the chip surface. The other end of the single-mode fiber has a fiber connector, which can be connected to other equipment such as an external laser source or the optical power meter.
- **(d) CCD microscope camera** The camera is tilted and positioned to the right of the fiber probe. It can provide an unobstructed view and help locate the position of the fiber probe during alignment. In order to track real-time alignment, the CCD microscope camera is connected to a computer, which displays live images.
- (e) 3-dimensional positioner The high-precision Thorlabs stage is used to align the fiber probe with the surface grating coupler. The positioner has an accuracy of approximately 0.5 μ m [112], which meets the requirements for alignment of the surface grating coupler. Maintaining a misalignment between the surface grating coupler and the fiber probe within 1 μ m can ensure that the coupling efficiency penalty remains below 0.5 dB [113].

3.3 Introduction to HHI photonic integration platform

The HHI platform is an InP-based photonic integration platform initially developed with receiver-only capabilities, achieving a 40 Gb/s receiver [114]. The platform was later enhanced with optimized butt joint regrowth, enabling the integration of laser-related structures [114]. With these enhancements, the HHI platform is now capable of supporting Tx-Rx integration, enabling the integration of SOAs and high-speed PDs. The platform requires three growth steps, including epitaxy of the base wafer layer, Tx layer, and Rx layer [115]. The platform includes several building blocks such as (1) passive waveguides and

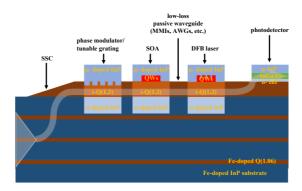


Figure 3.5: Schematic diagram of the HHI platform. The transmitter-type layer is utilized by the modulator, as well as the SOA and DFB layer, while the receiver-type layer is reserved exclusively for the photodetector. These active devices are connected by the low-loss passive waveguide layer, which enables high-efficiency signal transmission and integration [97].

spot size converters (SSCs), (2) phase modulators/tunable gratings, (3) SOAs, (4) DFB lasers, and (5) PDs. A schematic of the generic foundry platform implementation of the HHI platform is shown in Figure 3.5.

3.3.1 Performance of building blocks on the HHI platform

The performance of building blocks in HHI platform is listed in Table 3.2. The HHI InP-based platform has been well-developed and has provided MPW (Multi-Project Wafer) services for several years, making it a promising choice for InP-based photonic circuits. However, it has certain limitations that prevent the full functionality of the CAO-Rx from being realized on this platform. When building an on-chip optical integrated circuit on the HHI platform, the spot size converter (SSC) is used as the building block for coupling light from a single-mode fiber. An SSC-feeding high-speed waveguide photodetector (WGPD) is with high coupling efficiency [36]. However, the aperture of the SSC is usually designed to match the single-mode fiber, and the aperture is limited. Since the HHI platform is a generic InP-based photonic integration platform, it is with small refractive index contrast. The practical SGC cannot be realized on this platform [97]. Consequently, the HHI platform is utilized as a supplementary platform to the IMOS platform.

Basic device	Specification
Spot size converter [116]	loss: < 2 dB/cm coupling to the single mode fiber
Single-mode waveguide [116]	loss: 2 dB/cm; default width: 2 μm
Bending waveguide [117]	minimum radius: 150 μ m
1x2 MMI coupler [117]	loss:0.5 dB
SOA [115]	$3\sim4~\mathrm{dB}/100~\mu\mathrm{m}$ gain per length 3-dB spectral bandwidth of 40 nm around 1550 nm
DFB laser [97]	output power > 10 mW
PIN	-3dB bandwidth > 40 GHz
photodetector	responsivity 0.8 A/W
(PIN-PD) [114]	dark current 1 nA@-3V

Table 3.2: The performance of basic building blocks on HHI platform

3.3.2 Characterization setup for HHI chips

The experimental setup shown in Figure 3.6 is specifically designed for the horizontal-coupling chip. To begin the experiment, the chip is mounted onto a chip holder, and the DC probe and GSG probe are attached to the chip pad. Next, a fiber probe equipped with a vertically cleaved fiber is aligned to the SSC on the chip. The electrical and optical performance of the components of the photonic integrated chip are then evaluated and characterized. Finally, the bit error rate (BER) performance of the receiver is analyzed at various input optical power levels in both the optical back-to-back link and the optical wireless communication (OWC) link. The BER tester, tunable laser source, and optical power meter are not shown in this figure.

- (a) Fabricated HHI chip This experimental setup is designed to measure edge-coupling photonic integrated chips. The HHI chip used in this experiment is $2 \times 8 \text{ mm}^2$ and is mounted on an aluminum chip holder using adhesive resin.
- **(b) Copper holder** The aluminum chip holder is screwed to the copper holder. The copper holder is equipped with both vacuum and wafer cooling.

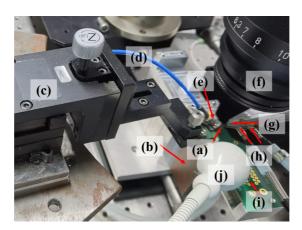


Figure 3.6: Picture of the characterization setup for the HHI chip, comprising (a) a fabricated HHI chip; (b) copper holder with water cooling; (c) Ground-signal-ground (GSG) probe positioner arm; (d) RF cable; (e) GSG probe; (f) optical microscope; (h) fiber probe; (h) DC probes; (i) printed circuit board (PCB) board; (j) light-emitting diode (LED) bulb.

- (c) GSG probe positioner arm The arm of the GSG probe positioner is used to adjust the position of the GSG probe for connection to the GSG pad on the chip. The arm of the Formfactor GSG positioner used in this experiment has a resolution of less than 1 μ m and a travel range of less than 12.5 mm.
- **(d) RF cable** The RF cable serves the purpose of transmitting the high-speed RF signal from the designated chip while minimizing signal loss, enabling transmission capabilities of up to 40 GHz.
- (e) GSG probe The GSG probe is used to extract the RF signal from the designed chip. The pitch of the GSG probe is 125 μ m, and it is an air coplanar probe (ACP) designed to extract the signal up to 40 GHz with minimal distortion.
- **(f) Optical microscope** The optical microscope is used to help connect the metal probe and metal pad and to align the cleaved optical fiber probe with the spot-size converter on the chip.
- **(g) Fiber probe** The fiber probe is made by removing the coating layer from one end of a single-mode fiber and vertically cleaving the exposed fiber end. The opposite end of the fiber probe is equipped with a fiber connector, enabling it to be easily connected to various equipment, including external laser sources or optical spectrum analyzers.

- **(h) DC probes** The DC probe serves the purpose of establishing a connection with the metal pad on the chip, thereby enabling an on-chip electrical connection to the current source or voltage meter.
- (i) PCB board This PCB is intended for use in the electronics assembly to be connected to the on-chip pad by wire bonding. During the measurement process, the wire bonding was not done, and the PCB was only used to fix the position of the aluminum holder.
- (i) LED bulb Due to a malfunction of the microscope's light source, an LED bulb is being used as the illumination source during the use of the optical microscope.

Other equipment, such as a tunable laser, electrical/optical power meter, and current source, are not visible in this picture. These components will be used in the system experiment.

3.4 Chapter Summary

In this chapter, the capabilities of the IMOS and HHI platforms are reviewed, including their extensive libraries of devices that can be used for Tx-Rx applications. The reasons for using the IMOS and HHI platforms are discussed. Both platforms are based on InP-based photonic integration. Since the SOA-PD monolithic integration was under development on the IMOS platform previously, the preliminary verification of the SOA-PD monolithic integration scheme was verified on the more mature HHI platform in this work. As the IMOS platform continues to evolve, it is expected that additional features will be incorporated to further enhance its capabilities. The ultimate goal is a fully functional CAO-Rx integrating on-chip optical and electronic amplifiers that can be realized on the IMOS platform in the future.

Chapter 4

Optical Receiver with A Metal-Reflector-Assisted SGC

4.1 Introduction

High-speed optical receivers with high-efficiency power collection capability are highly demanded in an optical wireless communication (OWC) system to achieve high sensitivity due to the power-limited eye safety regulation. As discussed in Chapter 2, a surface grating coupler (SGC) is a crucial component in the advanced cascaded aperture optical receiver (CAO-Rx). Its primary function is to collect optical power from the off-chip. One of the drawbacks of an SGC is its low coupling efficiency. To improve the coupling efficiency of an SGC, a metal reflector (MR) is introduced under the grating area for reflecting more light and enhanced light coupling into a waveguide. The MR-assisted SGC (MRSGC) is developed by several groups [105, 118–121]. In [105, 118–120], the coupling efficiency of the MRSGC either reaches minus sub-decibel or is improved by several decibels. In this chapter, the coupling efficiency is defined as the negative of the coupling loss. It is attractive to employ the MRSGC in the CAO-Rx to improve the coupling efficiency. This is possible thanks to the concept of the CAO-Rx. It enables individual optimization of the SGC and the PD. As a result, the coupling efficiency of the SGC can be significantly improved without any compromises. However, previous works mainly focus on a discrete MRSGC, and the experimental validation of the cointegration concept between MRSGC and the PD component remains unexplored. In [121], Li et al. theoretically proposed to use an MRSGC to realize the connection of a top illuminated photodetector (PD) in optoelectronic integrated circuits. And the MRSGC scheme is compatible with the SGC design with polarization independence mentioned in [122]. A solution of utilizing the more efficient MRSGC and the waveguide photodetector (WGPD) in a CAO-Rx is desired.

4.2 Passive run: a metal-reflector-assisted SGC

In this section, we focus on exploring the fabrication process of MRSGC during the passive run before integrating it with the high-speed waveguide unitraveling-carrier photodetector (UTC-PD). This approach is preferred since the passive run requires significantly less time to complete the design, fabrication, characterization, and optimization cycle.

4.2.1 Design and fabrication

An MRSGC is utilized to enhance the coupling efficiency of a WGPD and the position of the MR should be evaluated. In [118], Hoppe et al. proposed a scheme to deposit the MR beneath the SGC and in the cavities of the carrier substrate. The standing substrate with cavities is fragile, which poses a challenge for PD device fabrication. Chen et al. deposited the MR across the entire surface of the substrate located below the SGC [119]. It is not suggested to use this scheme since the low Ohmic buried property of the metal layer will add additional parasitic capacitance to lag the performance of the high-speed PD [123]. Rodriguez et al. developed a buried metal SGC with an MR, which consists of SiO₂ stripes covered by a metal layer [120]. The principle of this metal SGC is to couple light into the dielectric waveguide by exciting a surface plasmon polariton mode. Compared with dielectric SGCs, plasmonic devices usually suffer from higher absorption loss, resulting in lower coupling efficiency [124]. Kashi et al. demonstrated both deeply-etched and shallowly-etched focusing InP-based SGC with an MR [105]. A focusing SGC requires accurate alignment between its focal point and the position of the input of the waveguide. In my test runs aimed at integrating PD and SGC into one chip, the alignment markers for the e-beam lithography (EBL) exposure occasionally get damaged in the wet etching process. Then the manual alignment had to be performed for the successive EBL exposure. It is worth noting that the accuracy of manual alignment is constrained to several hundred nanometers. It is not recommended to utilize

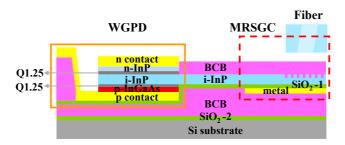
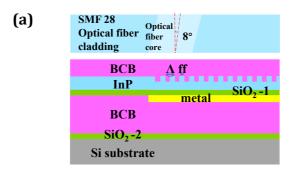


Figure 4.1: Cross section of the layer stack of the waveguide photodetector (WGPD) with a metal-reflector-assisted surface grating coupler (MRSGC).

the focusing SGC design if the manual alignment of EBL exposure is intended to be performed.

Here, we adopt a rectangular-shaped InP-based SGC combined with an MR to achieve a high-sensitivity optical receiver in this prototype, where the MR is selectively buried below the SGC. The rectangular-shaped SGC has better lithography alignment tolerance during fabrication compared with the focusing SGC. The WGPD with an MRSGC is fabricated on the Indium Phosphide membrane on Silicon (IMOS) platform. Before the bonding process, it is feasible to deposit the metal layer specifically in the desired region on top of the SiO $_2$ layer. Subsequently, after the bonding process, the SGC can be defined on the upper surface of the MR. This is facilitated by bonding the InP-based WGPD function layer with SiO $_2$ (referred to as SiO $_2$ -1 as depicted in Figure 4.1) to the silicon carrier wafer on this platform, using benzocyclobutene (BCB). The cross-section picture of the WGPD is shown in Figure 4.1.

In this prototype, in order to decrease the fabrication challenge, we used the matured standard design of the rectangular-shaped InP-based SGC with a grating period (Λ) of 660 nm and a filling factor (ff) of 0.5 on the IMOS platform. The SGC with such parameters is expected to be with a central wavelength of 1550 nm and a coupling efficiency of -5.5 dB [55]. The thickness of the InP layer used for defining the SGC and the waveguide is 300 nm, and the etching depth of the grating groove is 120 nm. The thickness of the BCB as the cladding layer and the bonding layer is 1 μ m and 2 μ m, respectively. A 1550 nm light source with the transverse electric mode is used and connected by a fiber probe with 8° angle. The angle of the fiber is determined relative to the normal surface of the chip, as depicted in Figure 4.2 (a). Due to the symmetry of the used uniform SGC, a simplified two-dimensional (2D) finite-difference time-domain



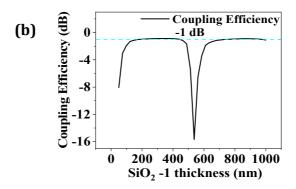


Figure 4.2: (a) Two-dimensional simulation structure of a metal-reflector-assisted surface grating coupler (MRSGC) at an input fiber angle of 8° , (b) Simulated coupling efficiency as a function of the thickness of SiO_2 -1 layer at the input wavelength of 1550 nm.

(FDTD) simulation method was adopted to find the optimal thickness of SiO_2 -1 layer to realize the constructive interference along the waveguide direction at the SGC. The simulation structure is shown in Figure 4.2 (a). The simulated coupling efficiency of the SGC as a function of SiO_2 -1 layer thickness is plotted in Figure 4.2 (b). The coupling efficiency behavior is periodic and is with a half-wavelength period. When analyzing the coupling efficiency of the SGC as a function of the thickness of SiO_2 -1 layer in the first cycle, it was found that the simulated coupling efficiency remained below -1 dB for SiO_2 -1 layer thicknesses larger than 180 nm. The thickness of SiO_2 -1 layer is chosen as 200 nm in our design.

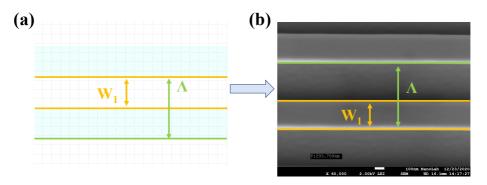


Figure 4.3: (a) The initial mask design for the surface grating coupler, with a grating tooth width W_1 of 330 nm and a grating period Λ of 660 nm; (b) An SEM image of a single period of the surface grating coupler is presented. The fabricated structure features a grating tooth width W_1 of 293 nm and a grating period Λ of 660 nm.

The fabrication flow for this passive run is very similar to that described in Section 3.2.2 but with fewer fabrication steps. It only requires four lithography steps. Prior to the wafer bonding process, a thin metal layer is deposited below the InP membrane in a specific area. The MR is defined as consisting of the Germanium (Ge)/Silver (Ag)/Gold (Au) layer stack. Since Ag exhibits poor adhesion to silicon dioxide [125], the thin Ge layer is added as an adhesion layer with a minor affecting on light reflection. The Ag layer is the reflection layer, which has been shown to be a highly effective reflector of infrared light [126]. To prevent the oxidation of the Ag layer during the successive wafer cleaning process with O_2 plasma, a thin Au layer is deposited. Following the bonding process, an SGC is defined above the metal layer.

Pattern offset

An issue during the fabrication was the need for an additional dimensional offset of the SGC pattern in the passive run.

Figure 4.3 (a) and (b) are the designed pattern and the scanning electron microscope (SEM) picture of one period of the fabricated SGC before dimension offset, respectively. In Figure 4.3 (a), the blue line is the position of the grating groove in a grating period in the EBL mask, which will be the exposure area during EBL exposure. The white line is the position of the grating tooth in a

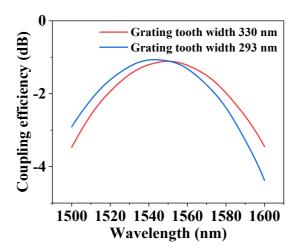


Figure 4.4: The simulated coupling efficiency of the grating coupler as a function of the wavelength with a grating period of 660 nm with different grating tooth widths is presented. The red line represents the simulation result with a grating tooth width W_1 of 330 nm; the blue line represents the simulation result with a grating tooth width W_1 of 293 nm.

grating period. The width of the grating tooth W_1 is designed to be 330 nm, and the grating period is 660 nm. After completing this passive run, pictures of the SGC are taken by the SEM to check the dimension of the SGC. Here only one grating period is shown in Figure 4.3 (b) due to the limited field size in the 60, 000x magnification. The width of the grating tooth W_1 and the grating period of fabricated SGC are 293 nm and 660 nm, respectively. The width of the fabricated grating tooth shrinks 12 % compared with the design parameter. It can be explained that since electron beam lithography (EBL) is used to define the pattern size, the pattern size will expand a certain ratio due to the proximity effect caused by the electron beam exposure. The proximity effect is a phenomenon that occurs during EBL exposure, whereby the exposure of the defined pattern also affects the surrounding area [127]. The recalibration of the relationship between exposure dose and structure dimension is necessary because this particular type of SGC has not been previously verified on the IMOS platform.

A simulation was conducted to assess the influence of different grating widths on the performance of the SGC. The results of this simulation are presented in Figure 4.4. Most of the simulation parameters remained the same as the previ-

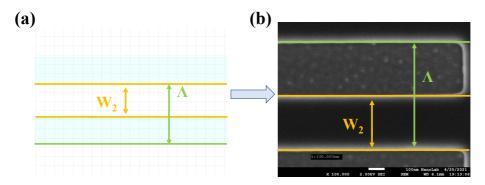


Figure 4.5: (a) The updated mask design for the surface grating coupler, with a grating tooth width W_2 of 370 nm and a grating period Λ of 660 nm; (b) An SEM image of a single period of the surface grating coupler is presented. The fabricated structure features a grating tooth width W_2 of 330 nm and a grating period Λ of 660 nm.

ous simulation, with the exception of the grating tooth width. It was observed that narrowing the width of the grating tooth (from 330 nm to 297 nm) resulted in a blue shift of approximately 7 nm in the central wavelength of the grating coupler.

Lowering the exposure dose during the EBL lithography process is one possible method for compensating for the dimension of the grating tooth. However, this approach may adversely affect the exposure quality of a large-area pattern. In the subsequent passive run, the width of the grating tooth was adjusted with a 12% dimension compensation, and the updated design mask specified a width of 370 nm, as shown in Figure 4.5. Subsequently, it was observed that the width of the grating tooth under the same exposure conditions was 330 nm, which perfectly matched the designed parameter of 330 nm.

4.2.2 Device performance

The coupling efficiency of the MRSGC is measured by coupling a laser beam with TE polarization into a passive device with an input MRSGC via an input fiber. We then measured the optical power of the laser beam that was coupled out with a fiber from an output MRSGC of the same device. This passive device consisted of two identical MRSGCs connected by a waveguide. The recorded fiber-to-fiber loss of this device includes the insertion loss of both the

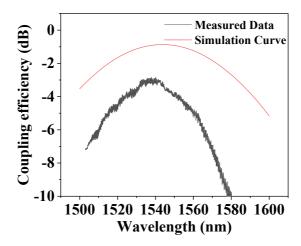


Figure 4.6: Coupling efficiency as a function of the wavelength; the red line and black line represent the simulation result and the measurement data, respectively.

MRSGC and the waveguide. To calculate the propagation loss of the waveguide, a set of passive structures was used, in which the waveguide varied in length in different devices. Subsequently, the coupling efficiency of an MRSGC was calculated. The measurement setup described in Section 3.2.3 was utilized. The red line and dark line, as shown in Figure 4.6, represent the simulated coupling efficiency of an MRSGC as a function of the wavelength and the measured coupling efficiency of an MRSGC at different wavelengths, respectively. The simulation parameters are identical to those parameters mentioned in the design section. Extracting from the measured curve with black color in Figure 4.6, the maximum coupling efficiency of this MRSGC is -3 dB, which obtains a 2.5 dB improvement compared with that of the typical InP-based SGC on the same platform [101]. The SGC with an MR is centered at 1540 nm with a 1 dB bandwidth of around 30 nm. The shifted central wavelength of the SGC is possibly caused by the overetched groove depth [128]. According to Ref. [128], the discrepancy in coupling efficiency between the simulation and experimental results can be partially attributed to the scattering loss caused by the imperfect fabrication, such as the non-perfect straight grating stripes affected by the proximity effect in e-beam lithography, the non-vertical groove, and roughness. The ripples in the measured data can be ascribed to reflections occurring at the SGC [120].

4.3 Active run: CAO-Rx with a metal reflector-assisted SGC

The previous section discussed the fabrication process of the metal reflector-assisted SGC during the passive run, which resulted in enhanced coupling efficiency. In this section, we demonstrate the integration of the CAO-Rx with the metal reflector-assisted SGC. The devices' performance is thoroughly characterized, and the CAO-Rx with the metal reflector-assisted SGC is verified in the back-to-back optical link.

4.3.1 Fabrication

This optical receiver is fabrication on the IMOS platform, which uses double-sided processing. The general double-sided processing flow can be referred to in Section 3.2.2.

Fabrication challenge

The wafer bonding process, depicted in Figure 3.2 (d), is a crucial step in the fabrication process. It involves depositing a SiO₂ layer with a specific thickness on both a quarter of a 2-inch InP wafer and the 2-inch silicon carrier wafer, followed by spinning adhesion and BCB layers. The InP wafer is placed episide down on the silicon wafer and bonded with a certain force from the top. The bonded wafer is kept at 280°C for 1 h to cure the BCB bonding layer and strengthen the bonding in the bonding machine before the InP substrate is removed by wet etching to obtain the InP membrane. On a quarter of a 2-inch InP wafer, pattern alignment is performed using only a single group of EBL markers. By employing only one group of EBL markers, the die size consumption of these markers is significantly reduced. However, if bubbles are introduced and subsequently damage the EBL maskers during the bonding process, it will result in the failure of the entire wafer. Although the InP wafer and the silicon carrier wafer were carefully processed using ultrasonic and acetone cleaning to reduce particles, we observed the presence of bubbles surrounding the markers or causing damage to the InP membrane in the early runs. One possible reason for the observed phenomena is that when spinning the BCB layer on a quarter of a 2-inch wafer, the thickness of the BCB layer at the edge is significantly thicker due to the edge bead effect [129, 130]. This increase in thickness may harm the overall bonding quality. Through several attempts and observation of these failures, the preparation of spinning the BCB layer onto the bonding wafer was found to significantly affect the success rate of the wafer bonding process. To improve the wafer bonding process, we tested various methods of spinning the BCB layer on the bonding wafers, including spinning it on either the InP or silicon wafer, spinning it on both wafers, curing it on one wafer, or spinning it directly on both wafers. After several unsuccessful runs, we found that the most effective approach to avoid manufacturing failures was to spin the BCB layer separately on the surfaces of both bonding wafers and bond them together with a high compression force of 28 N/cm². It should be noted that when using this bonding method, there is a potential risk of air bubbles being absorbed into the bonding layer. However, this problem was not observed during the experimental runs carried out for this study. To minimize the risk of such problems occurring, it is essential that the process is followed carefully. This study utilizes this selected method because of its notable fabrication tolerance, which results in fewer bubbles compared to other available approaches.

4.3.2 Device performance

This section presents and discusses the measurement results, which include the coupling efficiency of the MRSGC and the performance of the WGPD assisted by the MRSGC. The microscope picture of the WGPD assisted by the MRSGC is shown in Figure 4.7.

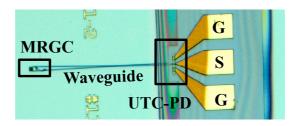


Figure 4.7: Picture of a waveguide uni-traveling-carrier photodetector (UTC-PD) with a size of $8\times2~\mu\text{m}^2$ and with a metal-reflector-assisted surface grating coupler (MRSGC).

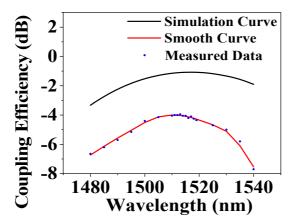


Figure 4.8: Coupling efficiency as a function of the wavelength; the black line, blue dot, and red line represent the simulation result, the measurement data and the smooth curve of the measurement data, respectively.

Characterization of the waveguide photodetector assisted by an SGC with a metal mirror

The reference waveguide arrays were fabricated to calculate the MRSGC's coupling efficiency and the waveguide loss. The measured waveguide loss is 10 dB/cm. The high propagation loss of the waveguide is caused by the roughness of the waveguide, which is introduced by the EBL exposure. The black line, blue dots, and red line, as shown in Figure 4.8, represent the simulated coupling efficiency of an MRSGC as a function of the wavelength, the measured coupling efficiency of an MRSGC at different wavelengths and the smooth curve for the measured data, respectively. The simulation parameters, such as the groove etching depth, the filling factor, and the thickness of the BCB cladding layer, are updated in the simulation according to the measured data during fabrication, and other simulation parameters are identical to those parameters mentioned in the design section. When measuring the coupling efficiency of the SGC, the waveguide of the input light is tuned manually, and the measured data is the discrete points. Extracting from the smooth curve with red color in Figure 4.8, the maximum coupling efficiency of this MRSGC is -4 dB, which obtains a 1.5 dB improvement compared with that of the typical InP-based SGC on the same platform [101]. The SGC with an MR is centered at 1513 nm with a 1 dB bandwidth of 33 nm. During the simulation, it was observed that a 1-degree

change in the angle of the incident light results in a 15 nm shift in the central wavelength of the MRSGC. Considering that the -1 dB bandwidth of this MRSGC is 33 nm, the calculation of its -1 dB field-of-view indicates a 2-degree range. According to Ref. [128], the discrepancy in coupling efficiency between the simulation and experimental results is partially attributed to the scattering loss caused by the imperfect fabrication, such as the non-perfect straight grating stripes affected by the proximity effect in e-beam lithography, the non-vertical

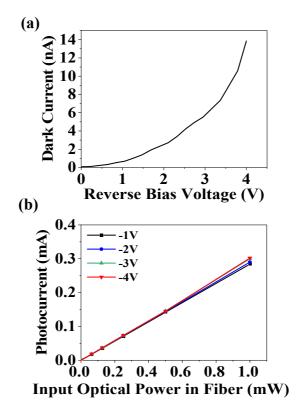


Figure 4.9: DC Performance of the photodetector with a size of $8\times2~\mu\text{m}^2$ inside the proposed optical receiver. (a) Dark current curve of this waveguide photodetector; (b) Photocurrent curve of this waveguide photodetector at 1515 nm at different bias; When the reverse voltage increases, the PD's responsivity increases slightly.

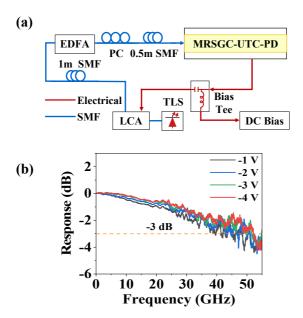


Figure 4.10: Measured frequency response of this waveguide photodetector with a size of $8\times2~\mu\text{m}^2$ inside the proposed optical receiver. (a) Experimental setup for 3-dB bandwidth measurement. TLS: tunable laser source; LCA: lightwave component analyzer; EDFA: erbium-doped fiber amplifier; PC: polarization controller; GC-UTC-PD: grating coupler-assisted uni-travelling-carrier photodetector; SMF: single-mode fiber. (b) Measured frequency response of the membrane-based waveguide UTC-PD with the PD size of $8\times2~\mu\text{m}^2$.

groove, and roughness. The surface reflection between the air and the cladding layer of the SGC could also deteriorate the measured maximum coupling efficiency [131]. In this section, the MRSGC (obtained through an active run) exhibits a coupling efficiency that is 1 dB lower than the MRSGC obtained from the passive run (as presented in the previous section). An active run refers to a fabrication run involving the fabrication of active devices, including PDs. One possible reason for this discrepancy is that during this active run, the waveguide layer undergoes multiple cycles of O₂ plasma cleaning and oxide cleaning. These cleaning processes result in the removal of approximately 1-2 nm of the waveguide layer during each cycle, leading to a reduced thickness of the SGC and consequently diminishing the coupling efficiency of the SGC [128].

The measured dark current of the WGPD as a function of the reverse bias voltage is shown in Figure 4.9 (a). The achieved value is 13.9 nA at -4 V and 0.7 nA at -1V. The external responsivity of the WGPD assisted by an MRSGC is calculated by measuring the output photocurrent as a function of input optical power in the fiber probe at different bias voltages. From Figure 4.9 (b), the calculated external responsivity of WGPD assisted by an MRSGC is 0.31 A/W at -4 V and 0.28 A/W at -1 V at 1515 nm.

An Agilent lightwave component analyzer with 67 GHz bandwidth is utilized to measure the -3 dB electrical bandwidth of this waveguide PD with $8\times2~\mu\text{m}^2$. The wavelength of the laser source is set at 1515 nm. The modulated optical signal is amplified by an erbium-doped fiber amplifier (EDFA). One polarization controller (PC) is inserted between EDFA and the fiber probe to control the polarization state of the light. The normalized frequency response (S21) measured at various voltages from -1 V to -4 V ranging from 0 GHz to 55 GHz are shown in Figure 4.10. The achieved -3 dB electrical bandwidth of the membrane-based waveguide UTC-PD is 52.2 GHz at -4 V and 41.3 GHz at -1 V, respectively.

4.3.3 Transmission experiment

This section evaluates the transmission performance of the CAO-Rx with a metal reflector-assisted SGC for a 10 Gb/s optical link in the back-to-back optical link. The verification of the CAO-Rx with an MRSGC in an OWC link is presented in chapter 7.

Experimental setup

A proof-of-concept experimental setup for a 10 Gb/s back-to-back link was built by utilizing the suggested optical receiver as shown in Figure 4.11. It is noticed that the transmitted data rate is restricted by the used bit-error-ratio tester (BERT). The -3 dB bandwidth of this waveguide PD is larger than 40 GHz, which can support beyond 56 GBaud/s signal. In the communication control center, an optical carrier is created by a tunable laser source with an output optical power of 10 dBm, which is subsequently modulated by a 40 GHz Mach-Zehnder modulator (MZM). The BERT generates the desired 10 Gb/s electrical OOK data to drive the MZM after amplification. The received signal is sent back into the BERT. The polarization state of the incoming light entering the MZM and the proposed optical receiver are controlled by two PCs for optimized acceptance. In order to change the input optical power into the chip, a variable attenuator is connected between the PC2 and the fiber probe. The angle of the

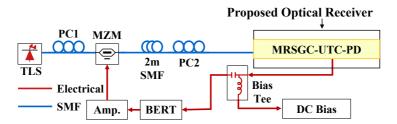


Figure 4.11: Experimental setup based on the proposed optical receiver for 10 Gb/s OOK signal; TLS: tunable laser source; PC: polarization controller; MZM: Mach-Zehnder modulator; SMF: single-mode fiber; BERT: Bit-error-ratio tester.

fiber probe is set at 8 degrees. Using a bias tee, the appropriate alternating current (AC) signal is then extracted from the waveguide PD's output electrical signal. It is eventually fed back into the BERT receiver for BER computation. Since the engaged MRSGC is polarization selective, a polarization controller is used to tune the lightwave polarization for optimized acceptance. However, in a practical system, the circularly polarized lightwave can be utilized to relieve such polarization dependence at the cost of an extra 3-dB loss [40]. The modulation depth at the transmitter, denoted as α (as referred to Equation 2.5), was determined to be 36% during the experiment. This value was calculated using the formula $\sqrt{\frac{P_s}{P_c}}$ mentioned in Section 2.2.3, which involves measuring the message optical signal (P_s) and the carrier optical power (P_c) .

Optical back-to-back performance

The BER performance of the proposed optical receiver for a 10 Gb/s OOK signal as a function of input optical power in the fiber probe is plotted in Figure 4.12. The optical receiver is biased at -1 V. The red curve is the measured data. At -1 V bias for a 10 Gb/s signal, the measured sensitivity of the proposed receiver is -4.75 dBm at the 7% FEC limit of 3.8×10^{-3} . The receiver sensitivity at the 7% FEC limit can also be calculated from received optical signal power $\overline{P_s}$ or noise current i_n . According to Eqs. 2.8 and 2.6, the receiver sensitivity denoted by optical signal power is expressed as:

$$I_{sens,power} = \overline{P_s} \times 10^{\frac{\eta}{10}} \times R_{PD} \tag{4.1}$$

At the 7% FEC limit, the total received optical power is -4.75 dBm. Considering the modulation depth of 36% in the experiment, the received optical

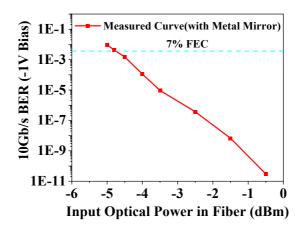


Figure 4.12: BER performance of the received 10 Gb/s OOK signal as a function of received optical power (optical power transmitted through the fiber probe's output) based on the grating-assisted waveguide photodetector with a metal mirror at -1V bias.

signal power \bar{P}_s is calculated to be 0.0385 mW (-14.15 dBm) based on Eq. 2.5. Since the -3dB bandwidth of the PD under -1 V bias is 41.3 GHz and the drop of the PD's responsivity at 7 GHz (corresponding to 10 Gbit/s OOK link) should be quite small, we use the direct current (DC) internal responsivity instead to do the calculation. The coupling efficiency η and the internal responsivity R_{PD} are equal to -4 dB and 0.7 A/W, respectively. Thus, the $I_{sens,power}$ at the 7% FEC limit is 21.4 μ A. Since no TIA is connected to this optical receiver, the $\left\langle i_n^2 \right\rangle^{1/2}$ is equal to $\sqrt{\frac{4kT\Delta f}{R_{load}}}$ [85], where k, T, Δf , R_{load} are the Boltzmann constant, temperature in Kelvin, receiver -3-dB bandwidth and load resistance. The receiver sensitivity denoted by noise current is further expressed as:

$$I_{sens,noise} = Q \times \sqrt{\frac{4kT\Delta f}{R_{load}}}$$
 (4.2)

The Q value equals 3 at the BER of 3.8×10^{-3} , and the load resistance is 50 Ω . The $I_{sens,noise}$ is calculated to be 22.2 μ A, which is consistent with that calculated from the received signal power. The calculation verified that the coupling efficiency of the MRSGC is around 4 dB.

To compare the sensitivity of optical receivers with and without an MR on

the same platform, Eq. 4.1 and Eq. 4.2 can be utilized with the assumption that the performance of the waveguide PD is the same. Since the typical maximum coupling efficiency of the standard InP-based SGC on the same platform is -5.5 dB [101], which should be 1.5 dB smaller than the MRSGC inside the proposed optical receiver, the sensitivity of the proposed optical receiver is improved by 1.5 dB according to the Eqs. 4.1 and 4.2.

When the PD is integrated with a preamplifier optimized for operation at a given bit rate, the value of the $\left\langle i_n^2 \right\rangle^{1/2}$ in Eq. 2.8 scales as the square root of detector capacitance, $\sqrt{C_D}$ [132,133]. The capacitance of the fabricated WGPD with the size of 8×2 μ m² is below 8 fF [55], which may lead to high sensitivity optical receiver when the proposed optical receiver is with an optimized preamplifier.

4.4 Chapter summary

We investigated an MR-based optical receiver enabled by a WGPD assisted by an MRSGC. The coupling efficiency of the MRSGC is -4 dB, which is 1.5 dB higher than the typical dielectric SGC without an MR on the same platform, thus improving the waveguide PD's external responsivity. The external responsivity of the WGPD assisted by an MRSGC is 0.3 A/W, and the -3 dB bandwidth is 52.2 GHz, which could support an optical signal with a baud rate above 56 GBaud/s. The sensitivity of the proposed optical receiver without an amplifier is -4.75 dBm for 10 Gb/s OOK signal at the 7% FEC limit of 3.8×10^{-3} . Due to the small capacitance of this waveguide PD, the sensitivity of the proposed receiver with an amplifier is expected to achieve high sensitivity. The proposed receiver enabled by the WGPD assisted by an MRGC contributes to a high-sensitivity and high-speed OWC receiver.

Chapter 5

Optical Receiver with Multi-stage SOAs

5.1 Introduction

In this chapter, a novel noise-reduction optical amplification scheme by integrating cascaded semiconductor optical amplifiers (SOAs) is proposed and verified. Compared with utilizing a one-stage optical amplifier, using multiple independent SOAs with the same total length as a multi-stage optical amplifier offers the advantage of optimizing the noise figure of each optical amplifier independently by tuning their injection currents, which leads to the reduction of the total noise and an improvement of the receiver sensitivity.

5.2 Design and Fabrication

For the system with *m* cascaded optical preamplifiers, the total noise factor *F* is determined by each stage, which can be explained by Friis equation [134]:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \dots + \frac{F_m - 1}{G_1 G_2 \dots G_{m-1}}$$
(5.1)

$$NF_m = 10log_{10}F_m \tag{5.2}$$

$$G_{total} = G_1 G_2 G_3 ... G_m (5.3)$$

where F_m , G_m , NF_m are the noise factor, gain and the noise figure (NF) of the section m, respectively. NF_m is obtained experimentally, given as [135]:

$$NF_m = 10log_{10}(\frac{2\rho_{ASE}}{G_m h f} + \frac{1}{G_m})$$
 (5.4)

The parameter ρ_{ASE} is the power spectral density of ASE noise within the bandwidth, expressed as $n_{sp,m}hf[G_m-1]$ [136], where f is the input optical signal frequency and $n_{sp,m}$ is the inversion factor of the section m. A mathematical relationship between $n_{sp,m}$ and the electron density injected into the conduction band by the pump source $N_{c,m}$ is empirically expressed as $n_{sp,m} = \frac{N_{c,m}}{N_{c,m}-N_{0,m}}$, where $N_{0,m}$ is the transparency carrier density [137]. Before saturation, G_m is related to gain coefficient g_m , denoted as $\exp((g_m - \alpha)L)$, where α is the loss coefficient constant and L is the length of SOA. An empirical expression is often used to represent the unsaturated gain coefficient [137], as follows

$$g_m = \Gamma a(N_{c.m} - N_{0.m}) \tag{5.5}$$

where Γ is the optical confinement factor of the waveguide, a is the material gain cross section.

By substituting the expression of ρ_{ASE} into Eq. 5.4, we get

$$NF_m = 10log_{10}(\frac{2n_{sp,m}(G_m - 1)}{G_m} + \frac{1}{G_m})$$
(5.6)

There is a monotonous decay relation between NF_m and $N_{c,m}$ before the m-th SOA is saturated, which is investigated in [89]. Increasing injection current will decrease NF and increase G_m in m-th SOA. For the successively cascaded stages, the input optical power becomes large after amplification in the previous stage. The larger input optical power will result in a smaller NF value at the same injection current before the successive SOA is saturated [81]. For each stage of SOA, the NF is jointly decided by the input optical power and the injection current. The m-th SOAs input optical power is determined by the injection current of the (m-1)-th SOA. As a result, by adjusting the injection current of each stage, the total NF can be reduced, and the system gain is optimized in a certain combination of the injection currents of each stage, leading to an improved BER performance.

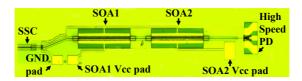


Figure 5.1: Picture of the designed monolithic integrated two-stage SOA-PIN receiver. SSC: spot size convertor; SOA: semiconductor optical amplifier; PD: photodetector.

From the Friis equation, the total NF of the system is mainly affected by the first two stages. Making a trade-off between the contribution of NF at each stage and the driving complexity, an optical pre-amplifier design with two-stage is utilized in this work. It should be noted that the driving complexity increases when more stages of SOAs are utilized. The design of two-stage SOA amplification allows the separate optimization of the injecting current of each SOA. Accordingly, the two-stage SOA-based receiver is able to achieve better system performance (lower BER values) under the same received optical power. It is worth noting that the power consumption of the driver circuits is reportedly less than one-ninth of that of an SOA [138]. This cascaded SOA design requires the utilization of additional driver circuits compared to the single-stage amplification scheme. This increased utilization of driver circuits inherently leads to slightly higher power consumption.

According to the Friis equation, it is advisable to design the first stage of the two-stage SOA with low noise performance in order to reduce the total NF of the two-stage SOA. It has been demonstrated in previous study that shortening the length of the SOA could result in a lower NF, under conditions of the same input optical power and injection current [139]. Hence, an effective strategy to enhance the NF of a cascaded optical amplifier will be to utilize a shorter SOA in the first stage. However, in this study, the length of each SOA in the twostage scheme is designed to be the same. An ideal benchmark for comparison would be a receiver with a single long SOA, whose length is equivalent to the combined length of the two-stage SOA, and a receiver with the two-stage SOA. However, practical limitations related to the available die size make it infeasible to incorporate another receiver design with a single long SOA. One alternative approach is to design the two SOAs in the two-stage design with equal lengths. By setting the injection currents of both SOA stages to the same values, the two-stage setup can be thought as a one-stage SOA. Thus, the two SOA are designed with the same length. The receiver is built on HHI's generic photonic

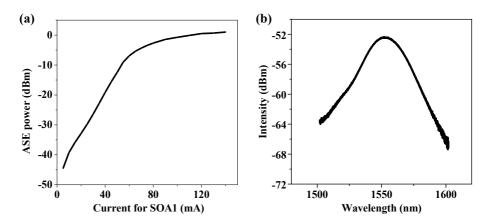


Figure 5.2: (a) The ASE power versus the injection current on the 1 mm long SOA1, and (b) The ASE spectrum of the 1 mm long SOA1 driven by 30 mA current.

integration platform, enabling the prototype with low cost, high reliability, and the potential of high yield [97]. The integrated receiver, as shown in Figure 5.1, consists of one spot size converter (SSC), two SOAs with 1 mm length, and one waveguide PIN. Single-mode InP waveguide with 2 μ m wide is used to connect the SOA and PIN. Each SOA is composed of an active region and an active/passive transition component at each side.

5.3 Device characterization and system implementation

In this section, the results of the device characterization are described first. The devices in the designed receiver were measured using the setup shown in Section 3.3.2. Subsequently, the optical receiver is tested in an optical wireless communication (OWC) transmission experiment to verify the enhancement of receiver sensitivity achieved by employing a cascaded SOA scheme.

5.3.1 Device performance

The coupling loss of SSC is measured to be 3 dB. The high-speed photodetector has a bandwidth of 45 GHz, a responsivity of 0.8 A/W, and a saturation

power of 10 dBm. The series resistance of the SOA is 14Ω . As shown in Figure 5.2 (a) and (b), the ASE power is proportional to the injection current when the values are below 60 mA, and the central response wavelength is 1550 nm. Owing to the constraint of limited chip size, the additional design with a single SOA was not implemented in the tape-out. Consequently, the noise figure of a single SOA was not measured. However, according to the HHI design manual, the reference noise figure for a single SOA is approximately 7.

5.3.2 Transmission experiment

Experimental setup

A proof-of-concept experimental setup has been built using the proposed monolithic integrated receiver for a 10 Gb/s OWC link, as shown in Figure 5.3. The transmission speed of the proposed receiver is feasible to support up to 40 Gb/s. However, the maximum transmission speed in the experiment is mainly limited by the maximum sampling rate of the used bit-error-ratio tester (BERT). A tunable laser source (TLS) with 10 dBm output optical power generates the optical carrier, which is then modulated by a 40 GHz Mach-Zehnder modulator (MZM). The tested electrical data are produced by a BERT to drive the MZM after amplification. In the experiment, 10 Gb/s OOK signal is generated in the BERT, and the received signal is fed back to the BERT. Two polarization controllers (PCs) are used to control the polarization states of the incident light into MZM and the chip by maximizing their input optical power. A variable attenuator is inserted between the PC2 and the fiber probe to adjust the input optical power into the chip. The output electrical signal from the waveguide-

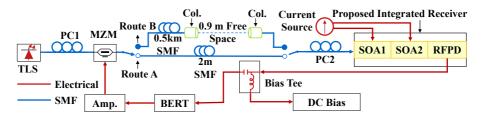


Figure 5.3: Experimental setup based on the proposed monolithic integrated SOA-PIN receiver. Route A: back-to-back; Route B: 0.9-m OWC link; TLS: tunable laser source; PC: polarization controller; MZM: Mach-Zehnder modulator; SMF: single-mode fiber; Col.: collimator; BERT: Bit-error-ratio tester.

integrated photodetector is then passed through a Bias-Tee. And the desired AC signal is outputted from one port of the bias tee, which is finally fed back into the receiver of BERT for BER calculation. Route A and B represent the back-to-back and OWC link over 0.9 m free space, respectively. The limitation of the OWC link for a collimated beam over 0.9 m is the size of our testbed. In the experiment, a fiber collimator with a focal length of 18 mm and a full angle divergence of 0.034° is used between MZM and PC2 to launch the optical beam into free space with a measured optical power below 10 dBm at 1550 nm, which meets the requirement of human eye safety. After 0.9 m free-space transmission, the optical beam is coupled into a short section of single-mode fiber via another collimator for further optical-to-electrical detection.

Optical back-to-back and OWC performance

The relationship among BER performance and currents of SOA1 and SOA2 at different input optical powers is measured. In the experiment, the injection currents into SOA1 were varied in a fixed range, starting from 40 mA and increasing in steps of 1 mA up to 51 mA. We scan the injection current into SOA2 at a fixed value of injection current into SOA1 and record the BER value of each scanning point. As shown in Figure 5.4, better BER performance can be achieved in a specific area represented by the injection currents of SOA1 and SOA2. It reveals that by separately tuning the injection currents into two SOAs, the BER values of the 10 Gb/s signal are optimized to obtain the best performance. The reason is that when the input optical power is fixed, the system total NF is jointly affected by the injection currents of SOA1 and SOA2, as stated before. Even when the combination of the injection currents of SOA1 and SOA2 is different, it still enables achieving the same BER performance. As changing the input optical power, the optimal combination of the injection currents of SOA1 and SOA2 is shown to be also changed, as shown in Figures. 5.4 (a), (b), (c), and (d). As the input optical power increases, the optimal combination of the injection currents of SOA1 and SOA2 decreases. This phenomenon occurs because as the input optical power rises, the currents in the SOAs need to be reduced to prevent saturation. The saturation of SOAs can have a detrimental effect on their noise figure [89]. The alternated optical power will lead to the change of the NF of the SOA [81]. The total gain of the optical amplification stage is determined by the product of the gains of SOA1 and SOA2. The gain of each SOA is influenced by its injection current and input optical power. It is important to note that even when the input optical power and the total gain

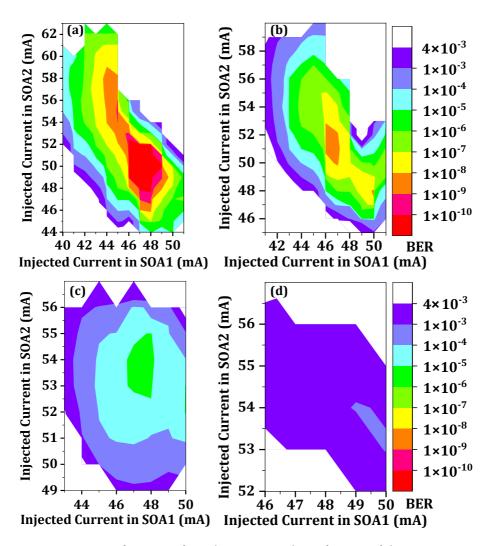


Figure 5.4: BER performance of 10 Gb/s OOK signal as a function of the injection currents of SOA1 and SOA2. The input optical power are set at (a) -22.5 dBm, (b) -24 dBm, (c) -25.5 dBm and (d) -27 dBm.

are held constant, different combinations of the injection current of SOA1 and SOA2 can still result in changes in the BER value.

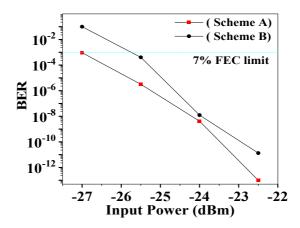


Figure 5.5: BER performance versus input optical power at different injection schemes. Scheme A: two-stage pre-amplifier with different injection currents; Scheme B: two-stage pre-amplifier with the same injection current, regarded as one-stage.

The way to optimize the pre-amplifier can be regarded as one-stage and two-stage schemes according to the injection currents. We called the operation processing as the optimization of a one-stage SOA/PIN receiver when the values of the two injection currents are the same since it can be considered as one input variable. By injecting different currents as two independent input variables into the SOAs, the two-stage scheme is formed. We measured the BER performance of 10 Gb/s signal as a function of input optical power at these two injection schemes as shown in Figure 5.5. For the two-stage and the one-stage pre-amplifier schemes, the optimal combination values of the injection currents at the different input optical powers are selected according to the measured results as illustrated in Figure 5.4. The overall BER performance by using the two-stage optical pre-amplifier scheme outperforms that of using the one-stage scheme as shown in Figure 5.5. More than 1.5 dB improvement of receiver sensitivity is successfully achieved at the BER level of 1×10^{-3} .

The proposed two-stage monolithic integrated SOA-PIN receiver is verified to have good performance at back-to-back optical link. It is then used in a 10 Gb/s OWC link over 0.9 m free-space transmission as shown in Figure 5.3 of

5.4 Discussions 75

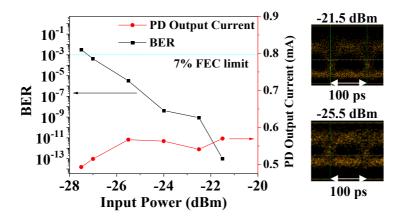


Figure 5.6: BER performance of 10 Gb/s OWC link by using the optimized monolithic integrated SOA-PIN receiver. The 10 Gb/s eye diagrams are measured at input optical power of -21.5 dBm and -25.5 dBm, respectively.

Route B. At each input optical power, the driving current combinations of SOA1 and SOA2 are optimized to achieve the best BER performance. The measured results are illustrated in Figure 5.6. At 7% FEC limit of 1×10^{-3} , the receiver sensitivity of 10 Gb/s signal is -27.1 dBm. The receiver sensitivity is further improved to -27.5 dBm at the BER level of 3.1×10^{-3} . The red curve shows the corresponding PD output currents. The flattening of the red curve can be explained by the fact that these two SOAs are approaching saturation.

5.4 Discussions

Maximizing the Proposed Receiver's Power Efficiency. For an intensity modulation direct detection (IM/DD) OWC system, power consumption also needs to be taken into consideration when the total power supply is restricted, especially for mobile terminals. The main limitation of power consumption comes from the driver circuits part and the operation part. According to the results in Figure 5.4, the best BER performance can be achieved in a particular area. Thus, to maximize the receiver's power efficiency, we can optimize the receiver's operation to choose the optimal combination schemes to achieve the 7% FEC limit, which are summarized in Table 5.1. Take the input optical power of -25.5 dBm as an example. At the total injection currents of 101 mA and 95 mA, the mea-

Optical Power (dBm)	SOA1+SOA2 (mA)	SOA1+SOA2 (mW)	BER
-22.5	47+50	68.2+74.6	1×10^{-13}
	41 + 50.2	56.0 + 75.0	1×10^{-3}
-24	46+52	66.1+79.0	4.15×10 ⁻⁹
-24	43 + 49.5	59.9 + 73.5	1×10^{-3}
-25.5	47+54	68.2+83.6	3.17×10^{-6}
	45 + 50	64.0 + 74.6	9.75×10^{-4}
-27	50+53	74.6+81.3	9.22×10^{-4}

Table 5.1: BER performance at different combination schemes

sured BER values are 3.17×10^{-6} and 9.75×10^{-4} , respectively, which are both under 7% FEC limit. The power consumption of the SOA is determined by multiplying its driving current with the corresponding record bias voltage. Thus, considering the power efficiency, the total driving current of 95 mA is the optimal choice, which can save 8.7% energy.

Maximizing the Proposed Receiver's Sensitivity. To obtain the high receiver sensitivity, the combination scheme with higher power consumption can be chosen. As illustrated in Table 5.1 at the input optical power of -25.5 dBm, the measured BER value of 3.17×10^{-6} still has margins when the total injection current is 101 mA. At the target BER goal of 3.8×10^{-3} , the input optical power can be further reduced to -27.5 dBm at the expense of high total driving current as shown in Fig. 5.6.

5.5 Chapter summary

In summary, we have proposed a two-stage cascaded SOA-PIN monolithic integrated receiver for high-sensitivity OWC. The achieved receiver sensitivity for a 10 Gb/s OWC link over 0.9 m free space is -27.5 dBm. Compared with the one-stage SOA-PIN receiver, the measured receiver sensitivity based on the proposed method is improved by 1.5 dB for 10 Gb/s OOK signal at the 7% FEC limit. Since the total system NF is reduced by tuning the SOAs' injection currents to adjust the inversion factor and gain of each SOA, the system BER performance is enhanced. The proposed monolithic integrated receiver can take advantage of the III-V integration platform, which is suitable for massive production. There-

fore, the proposed receiver with a cascaded SOAs scheme can be employed for high-speed OWC systems with high sensitivity and high reliability.

Chapter 6

Optical Receiver with Bias-Voltage Optimized PDs

6.1 Introduction

In this chapter, the bias voltage of the low-dark-current photodetector (PD) within the optical amplification module and of the large-bandwidth PD inside the high-speed O\E module, which is mentioned in Chapter 2, is optimized to be the same in order to reduce system-level complexity. By redesigning the layer stack of the uni-traveling-carrier photodetector (UTC-PD) and optimizing the fabrication process using the InP-membrane-on-Silicon (IMOS) platform, the trade-off between PD's dark current and PD's -3dB bandwidth is optimized.

6.2 UTC-PD compatible with shallowly-etched SGC

For compatibility in the fabrication process between the waveguide UTC-PD and the shallowly-etched surface grating coupler (SGC), different dry etch depths are required for the UTC-PD (especially the PD mesa) and the SGC. This requires the implementation of two separate dry etching steps, where one step is dedicated to defining the shallowly etched SGC, and another step is utilized to define the UTC-PD waveguide. This approach allows for independent optimization of each component's performance and provides increased flexibility in the fabrication of the device. In the following section, we focus on optimizing

the PD bias voltage to drive low-dark-current UTC-PD (the monitoring PD) and the high-speed UTC-PD (the data-detecting PD) at the same reverse bias. Thus, one bias feeding circuit is required, and the system complexity is required. To achieve this goal, we meticulously adjust the fabrication process to reduce the dark current at high reverse bias while maximizing the PD's bandwidth at low reverse bias by redesigning the layer stack of the PD device. This is evidenced by the experimental results described in the following subsections.

6.2.1 Design and fabrication

Optimizing the layer stack of the waveguide PD has the potential to result in a waveguide UTC-PD with wide bandwidth at a low reverse bias voltage [140]. The implementation of an appropriate passivation layer and thorough surface wet-chemical cleaning to eliminate process-induced damaged layers can significantly reduce the dark current at a specified reverse bias [110, 111, 141, 142].

Layer stack design

The first-generation waveguide UTC-PD has demonstrated a record high - 3dB bandwidth of 67 GHz when operated at a bias voltage of -4 V, making it one of the highest bandwidth heterogeneously integrated PDs on silicon reported to date [55]. However, this device exhibited strong dependence of its -3dB bandwidth on the applied bias, with a decrease to below 15 GHz when the bias was lowered to -2 V. The underlying cause is thought to be the accumulation of carriers at the heterojunction formed by the InGaAs and InP layers. To counteract this effect, previous work has suggested the implementation of a band smoothing layer at the junction between the InGaAs and InP layers [82].

In the literature, the band-smoothing layer is commonly realized as the In-GaAsP quaternary layer, which is composed of four distinct elements and can have its bandgap energy altered by adjusting the relative concentrations of the elements in the material. This provides a wide range of bandgap energies to be obtained. Two InGaAsP quaternary layers with different bandgaps or a single Q1.25 (InGaAsP) quaternary layer can be used as the band-smoothing layer. To minimize epitaxy-related challenges, this work utilizes a single InGaAsP quaternary layer as the band-smoothing layer. The exact bandgap of the InGaAsP quaternary layer must be determined. Our previous work showed that increasing the reverse bias voltage from 2V to 3 V resulted in a significant increase in the -3dB bandwidth of the device, from 15 GHz to 50 GHz. This observation

can be explained by the simulation results of conduction band discontinuity at the InGaAs/InP interface at different bias voltages, which showed a decrease in the barrier height at the InGaAs/InP interface relative to the conduction band in the p-InGaAs away from the interface, denoted as δ , from 0.08 eV to 0.04 eV [82]. Instead of using a higher voltage to reduce the barrier height, it is also possible to choose a band-smoothing layer with a specific bandgap to decrease δ .

Layer number	Material	Doping	Thickness (nm)
1	InP	n.i.d	50 nm
		graded doping profile (from 2×10 ¹⁹ cm ⁻³	
2	InGaAs	at the top to 1×10^{17} cm ⁻³	250 nm
		at the bottom)	
3	Q 1.25	n.i.d	10
4	InP	n.i.d	300
5	Q 1.25	n.i.d	20
6	InP	2×10^{18}	80
7	InGaAs	n.i.d	300
8	InP	semi-insulating	substrate

Table 6.1: Layer stack parameter of the waveguide UTC-PD

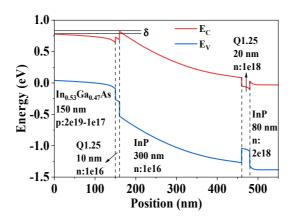


Figure 6.1: Simulated energy band diagram of the proposed UTC-PDs under zero-bias bias. The unit of doping density is cm⁻³.

The layer stack of the waveguide UTC-PD used in this work is redesigned based on our previous work [82], shown in Table. 6.1. The band-smoothing layer is the InGaAsP quaternary layer with a bandgap of 0.992 eV. The wafer is grown epitaxially on a semi-insulating InP substrate by using Metal Organic Chemical Vapor Deposition (MOCVD). The 300-nm InGaAs (In_{0.53}Ga_{0.47}As) sacrificial layer as the wet etching stop layer is grown on the InP substrate. Then an 80 nm thick n-type doped InP (n-InP) layer as the n contact layer is defined. A thin layer of Q1.25 with n.i.d doping is used as the wet etching stop layer. Next, the 300 nm thick unintentionally doped InP (i-InP) layer is set as the electron collection layer and the passive waveguide layer. The top layer is a 150 nm thick p-type doped InGaAs (p-InGaAs) layer, which is the absorption layer and the p-contact layer. In p-type doped InGaAs, a graded doping profile (from 2×10^{19} cm⁻³ at the top to 1×10^{17} cm⁻³ at the bottom) is used, which will induce a quasi-field for electrons to be drifted through this layer [143]. An unintentionally doped InGaAsP layer is inserted between the p-InGaAs layer and the i-InP layer to smooth the conduction band offset at the interface between i-InP and p-InGaAs, which can suppress the electron accumulation at the InGaAs-InP heterojunction interface [143]. By simulating the proposed UTC-PD layer stack with the defined layer parameters (thickness and carrier concentration) with nextnano software, the band diagram of the UTC-PD at zero bias is obtained and shown in Figure 6.1. The inserted O1.25 layer between the p-InGaAs and i-InP creates a low energy step at the InGaAs-InP heterojunction interface in the energy diagram, reducing the barrier height δ to 0.05 eV. This is expected to alleviate the accumulation of photogenerated electrons at the heterojunction interface, allowing smooth electron carrier transport and lowering the operating voltage.

Fabrication process design

Planarization material. The mesa structure of the PD device requires the use of planarization material, as illustrated in Figure 6.2, to create a flat surface on the semiconductor wafer. This facilitates the deposition of the ground-signal-ground pad for RF signal extraction while also serving the additional function of passivating the semiconductor surface. Semiconductor passivation involves adding a layer of material to the surface of the semiconductor to reduce or eliminate the effects of surface states and dangling bonds on the electrical properties of the device. This passivation layer can help to reduce the dark current of the PD device, thereby improving its performance [111]. A variety of materials can

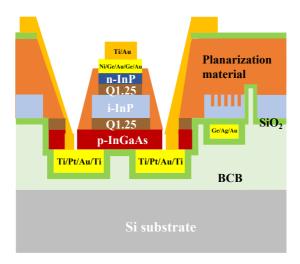


Figure 6.2: Cross-sectional schematic of the mesa of the waveguide uni-travelling-carrier photodetector. The position of the planarization material is highlighted in orange.

be used as the planarization (passivation) layer, including polymer-based and oxide-based planarization materials. Polymer-based planarization materials are typically preferred due to their superior passivation efficiency [144]. Benzocyclobutene (BCB) polymer and HD4104 polyimide material are used as the polymer-based planarization material, which is typically deposited using spincoating techniques. The polymer-based planarization material is then cured by thermal annealing, which promotes cross-linking of the polymer and enhances its adhesion to the semiconductor surface. The standard curing process for polyimide material typically requires holding at a high temperature of 375 C° for 1 hour [145]. However, such high temperatures and long curing times can pose challenges for the PD device, particularly extending the contact annealing time. In preliminary testing, some devices have failed due to short-circuiting, possibly caused by metal spiking from the n contact layer generated during the prolonged high-temperature annealing process [146]. The n-contact layer typically consists of nickel (Ni), germanium (Ge), and gold (Au). The widely used n contact metal layer of Ni/Ge/Au can result in a large amount of Au interdiffusion into the semiconductor at temperatures above 350 C° after longtime annealing [147]. Alternatively, the BCB is a good candidate to be used as the polymer-based planarization material. This is due to the relatively lowtemperature curing process employed for BCB planarization, which reduces the risk of prolonged high-temperature processing. The BCB material can be cured at 280°C for only 1 hour. Another type of planarization material is the oxidebased material. This material makes use of a plasma-enhanced chemical vapor deposition (PECVD) deposition process, and its layer thickness is highly repeatable across different runs, which can be well-controlled through careful calibration. Additionally, the uniformity of polymer-based planarization is often limited by waveguide (or mesa) density, whereas oxide-based planarization offers maximum design freedom [148]. Furthermore, the uniform thickness of the oxide-based material can help estimate the etching time required to open the SiO₂ planarization layer, thus accelerating the fabrication process and reducing the need for scanning electron microscope (SEM) examination times. Before the contact opening process, the contacts are buried inside the planarization material. It's also possible to use a composite layer of SiN_x/SiO₂ to form the planarization layer, which involves depositing a thin SiN_r layer first, followed by a SiO₂ layer. This approach can achieve better passivation efficiency than a pure SiO₂ layer [149]. However, it requires a switch in the reaction gas used in the PECVD process and demands additional preparation time. To determine the most suitable planarization material for the intended purpose, SiO₂ and BCB layers were chosen for wafers 1 and 2, respectively.

Waveguide etching depth and post-wet chemical treatment. As described in Section 4.4.1, the waveguide and the PD mesa are defined through ICP etching. This dry etching process inevitably results in damage and contamination effects in the exposed material, with impurities potentially penetrating the etched material. To remove the oxide layer and the metallic contamination during our device fabrication for reducing the device's dark current, the fabrication process can be adjusted accordingly. The distribution of the oxide layer and metallic contamination should be clarified. The depth distribution of the damage layer and contamination is depicted in Figure 6.3 [141]. The residue layer is a thin film of reactants and reaction products from the etching process, with a thickness of around tens of angstroms. In regions 2 and 3 shown in Figure 6.3, the oxide layer and metallic contaminations often contribute to the leakage current [141]. The oxide layer is close to the surface, while metallic contamination penetrates (10~250 nm) into the exposed etching material [141, 142]. Figure 6.4 (a) depicts the cross section of the PD mesa before waveguide definition. Figure 6.4 (b) shows the cross-section of the PD mesa with a thin InP layer remaining after the PD mesa definition, and this PD structure was used in the first-generation UTC-PD on the IMOS platform. The thin InP layer within

the PD mesa is exposed to the plasma during the dry-etching process, causing plasma-induced damage to be incorporated into the layer. It should be mentioned that any post-wet chemical treatment to this thin InP layer will impact the waveguide as well. The passive waveguide is susceptible to dimensional changes. To remove the damaged part of the thin InP layer on the PD mesa by post-wet chemical treatment without affecting the waveguide performance, the only feasible solution is to use a post-wet chemical treatment solution with an ultra-slow etch rate for InP. To passivate the InP surface, sulfur passivation can be utilized, only etching the InP layer for a few nanometers. However, during the preliminary experiment on sulfur passivation, sulfur particles were observed to deposit on the surface of the wafer. Further investigation revealed that the deposition of these sulfur particles was caused by the illumination light in the laboratory. To reduce the risk of particle contamination, we chose to open the InP layer on the PD mesa during the dry-etching step. Figure 6.4 (c) shows the cross-section of the updated PD mesa without the thin InP layer. This structure exposes the O1.25\InGaAs to air after the waveguide and PD mesa definition step and allows the use of selective wet chemical cleaning solutions to remove a thin layer of the Q1.25\InGaAs layer without affecting the dimension of the InP layer. In this work, we use a combination of diluted H₂SO₄/H₂O₂/H₂O and diluted HF as the post-wet chemical treatment method, which has been

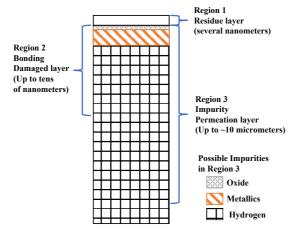


Figure 6.3: Schematic representation of plasma-based dry etching induced damage and contamination Layers with depth indication [141].

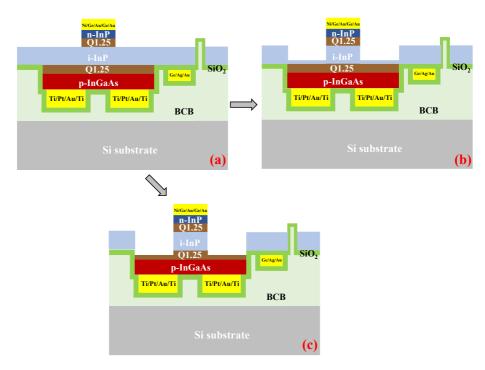


Figure 6.4: Cross-sectional schematic of PD mesa with varying etching depths: (a) Before dry etching, (b) a thin InP layer left in the PD mesa during dry etching, (c) complete removal of InP layer in the PD mesa during dry etching. The InP layer is emphasized using the blue color.

demonstrated in Ref. [110]. The purpose of the $H_2SO_4/H_2O_2/H_2O$ solution is to selectively remove the damaged Q1.25\InGaAs layer, while the dilute HF effectively removes the native oxide (In₂O₃), reducing the surface/interface state density [150, 151]. In this process, the waveguide etch depth is set at 300 nm to completely etch through the intrinsic InP layer. It is important to note that the post-wet chemical treatment is performed after the surface grating coupler definition step and prior to the planarization material deposition.

wafer number	waveguide etching depth (nm)	solution for surface wet-chemical cleaning	dielectric material for planarization
wafer 1	300	diluted H ₂ SO ₄ /H ₂ O ₂ /H ₂ O; diluted HF	SiO ₂
wafer 2	300	diluted H ₂ SO ₄ /H ₂ O ₂ /H ₂ O; diluted HF	ВСВ

Table 6.2: Iterative fabrication parameters for two wafers

Device fabrication

The general fabrication flow is the same as depicted in Section 3.2.2. The detailed planarization process is described in this section. The process of planarization starts subsequent to the surface grating coupler definition step. Depending on the type of planarization material employed, the procedure varies. If the selected material is BCB, the BCB planarization layer is coated to the wafer utilizing a spinning technique. Alternatively, if SiO_2 is chosen as the planarization material, it is deposited onto the wafer through the PECVD. Then using the lithography tool to define contact open pattern on either the BCB planarization layer or the SiO_2 planarization layer. Next, the BCB or SiO_2 planarization layer on the metal pad is opened by the dry etching tool. The main fabrication parameters of the fabrication process mentioned in before are listed for wafer 1 and wafer 2 in Table 6.2. The waveguide etching depth is set at 300 nm. And the solution for post-wet chemical treatment is the combination of the diluted $H_2SO_4/H_2O_2/H_2O$ and diluted HF.

6.2.2 Device performance

Two wafers containing UTC-PD samples were prepared, with planarization achieved using either BCB or SiO_2 material. One wafer contained three columns of UTC-PDs, with the smallest sizes of the PDs in each column being $8\times2~\mu m^2$, $8\times3~\mu m^2$, and $8\times4~\mu m^2$, respectively. The smallest PDs in each column are expected to have the lowest dark current and the highest -3dB bandwidth. Figure 6.5 shows a box plot of the dark current for UTC-PDs with these three sizes in both wafers, measured at -1 V and -4 V. Due to a fabrication process failure, the BCB layer had to be spun twice on the wafer, resulting in non-uniform BCB thickness. The pad of the $8\times4-\mu m^2$ PDs was not opened, so the dark current of these PDs could not be measured. The results indicate that the PD devices planarized with SiO_2 have a higher dark current compared to those planarized

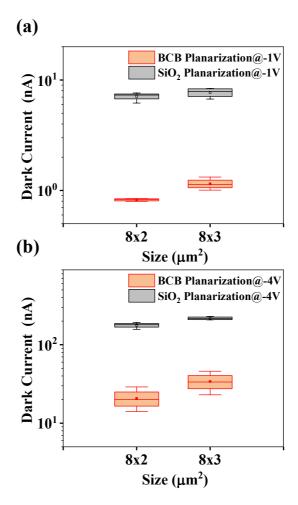


Figure 6.5: Box plots of the dark current for UTC-PDs of different sizes on two wafers planarized with BCB or SiO_2 material, measured at -1 V (a) and -4 V (b).

with BCB material. This preliminary study suggests that BCB material provides better passivation efficiency than SiO₂. The increased dark current in PD devices planarized with SiO₂ may be due to a higher surface carrier recombination rate [152, 153]. Despite this, PD devices planarized with SiO₂ can still achieve

a dark current of less than 10 nA at a reverse bias of 1 V, while PD devices planarized with BCB material achieved a dark current of less than 1 nA at a reverse bias of 1 V. However, even with BCB planarization, the dark current did not fall below 10 nA at a reverse bias of 4 V, suggesting that a lower reverse bias should be applied to the device to achieve a dark current of less than 10 nA. It is also observed that the PDs with $8\times3-\mu m^2$ size on the wafer with SiO_2 planarization material have the smallest dark current. A possible reason for this is that since the entire wafer is only dipped in the dilute HF solution for one or two seconds, the PDs with $8\times3-\mu m^2$ size located in the corner of the wafer may remain in the solution for a longer period of time.

The responsivity and the -3dB bandwidth of the UTC PD with the lowest dark current in this wafer are measured. Figure 6.6 (a) shows the output photocurrent as a function of input optical power at different bias voltages, which reveals weak bias dependence. From Figure 6.6 (a), the calculated responsivity of the UTC PD with 8*2 μm^2 at 0.75 A/W at -4 V and 0.7 A/W at -1 V. Other device with larger size has a higher responsivity. However, the increase in responsivity is minor. The possible reason for this is the high optical confinement of the IMOS platform, which enables a waveguide PD of short length to achieve sufficient quantum efficiency. Previous simulations have shown that a PD with a length of 10 μm and the same absorption thickness as this work can achieve a quantum efficiency greater than 97% [55]. Compared with the simulated responsivity values at 1550 nm reported in Ref. [55], the achieved responsivity in this work is higher. One possible reason is the difference in the calibrated value of the coupling loss from the local grating.

A commercial Agilent lightwave component analyzer with 67 GHz bandwidth is utilized to measure the 3-dB electrical bandwidth of the UTC-PD with $8*2~\mu\text{m}^2$, which is with the lowest dark current in wafer 3 at different reverse biases. The external laser source is set at 1515 nm. The modulated optical signal is amplified by an erbium-doped fiber amplifier (EDFA). One polarization controller is inserted between EDFA and the fiber probe to control the polarization state of the light. The output optical power of the fiber probe is set at 8 dBm. The normalized frequency response (S21) measured at various voltages from -1 V to -4 V ranging from 0 GHz to 55 GHz are shown in Figure 6.6 (b). The 3dB bandwidth of this PD at 0 V has not been measured yet. The bias dependence in the response is weak when the applied voltage is from -1 V to -4 V. This is due to the insertion of the Q1.25 layer to smooth the conduction band discontinuity between the InGaAs absorption layer and the InP carrier collection layer. This result is consistent with the weak bias dependence of photocurrent as shown in Figure 6.6 (a). The achieved 3-dB electrical bandwidth of the membrane-based

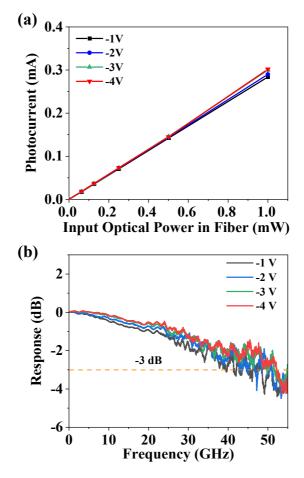


Figure 6.6: (a) Dark current as a function of reverse bias voltage curve for the UTC-PD of $8*2~\mu\text{m}^2$ passivated by BCB; (b) Measured frequency response of UTC-PD with $8*2~\mu\text{m}^2$ at 8 dBm input optical power. The 3dB bandwidth is around 52.2 GHz at -4 V.

waveguide UTC-PD is 52.2~GHz at -4 V with a dark current of 13.9~nA and an output current of 1.67~mA. The 3dB bandwidth of this UTC-PD is 41.3~GHz at -1 V.

6.2.3 Discussions

The insertion of the Q1.25 band-smoothing layer effectively reduced the strong dependence of the -3dB bandwidth of the UTC-PD and enabled the device to achieve high bandwidth at low reverse bias voltage. The use of BCB planarization material significantly reduced the dark current of the device at a given voltage. The bias-optimized PD was successfully realized on the IMOS platform. This work also lays the foundation for future heterogeneous integration of photonic InP-membranes PDs and complementary metal-oxide-semiconductor (CMOS) electronics, specifically TIA amplifiers, on the IMOS platform to realize the compact OWC receiver circuits through heterointegration. The heterointegration requires a low operating voltage of less than 1.5V for high-speed electronic driver circuits on CMOS [91]. With a -3dB bandwidth above 40 GHz at -1 V, the demonstrated PD is capable of supporting 56 Gbaud data rates and is suitable for heterogeneous integration with CMOS chips. The advantage of realizing a heterogeneous integrated OWC receiver can be referred to Section 2.2.4.

6.3 UTC-PD compatible with deeply-etched SGC

To further simplify the manufacturing process of the waveguide UTC-PD, the implementation of a deeply-etched SGC is a viable option. As previously discussed, the waveguide and SGC require separate lithography steps and etch depths of 300 nm and 120 nm, respectively. A highly efficient deep-etched SGC with a metal reflector, which requires only one lithography step to define both the SGC and the waveguide, has been developed by Amir [105]. This particular SGC features sub-wavelength nanostructures and has a waveguide etch depth of 280nm. It is crucial to explore whether we can still achieve low-dark-current UTC-PD (the monitoring PD) and the high-speed UTC-PD (the data-detecting PD) at the same voltage when the waveguide etch depth is set at 280 nm.

6.3.1 Design and fabrication

The waveguide etch depth of 280 nm was chosen to be compatible with the deep-etched SGC fabrication process. For this run, the previously effective post-wet chemical treatment solution consisting of a combination of dilute $H_2SO_4/H_2O_2/H_2O$ and dilute HF was used. Studies in the literature have shown that a thin InP layer can act as a passivation layer for the InGaAs/InP

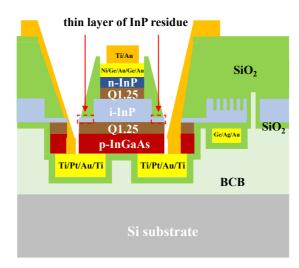


Figure 6.7: Cross-section of the UTC-PD mesa with a thin residual InP layer planarized with SiO₂ material.

junction [149, 154, 155]. In this run, the combination of the 20-nm thick InP residue layer and SiO₂ was used as the planarization and passivation layer. The use of SiO₂ simplified the fabrication process as it has a more uniform thickness and easier opening of buried contacts compared to BCB. Consequently, SiO₂ was selected as the planarization material for this run. Figure 6.7 shows the cross-section of the PD structure with the deeply-etched SGC. The general fabrication process remained the same as described in Section 3.2.2.

6.3.2 Device performance

Figure 6.8 shows a box plot of the dark current of UTC-PDs of different sizes planarized with SiO_2 on a single wafer, measured at -1 V and -4 V, respectively. The results show that when a thin InP layer is left as an etch residue, the UTC-PD device with silicon dioxide planarization material can achieve an extremely low dark current at a reverse bias of 1 V. However, the dark current of these devices increases rapidly with increasing voltage. At a reverse bias of 4 V, the dark current of these devices exceeds 100 nA. This preliminary study suggests that when low reverse biases are used in practical applications, the combination of a thin InP capping layer and a SiO_2 planarization layer can be used to simplify the fabrication process.

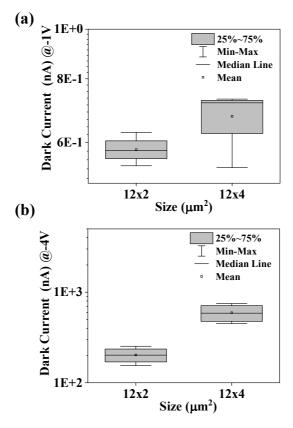


Figure 6.8: Box plots of the dark current for UTC-PDs (with a thin layer of InP residue) of different sizes on one wafer planarized with SiO_2 material, measured at -1 V (a) and -4 V (b).

6.3.3 Discussions

Using a diluted HF solution requires extreme care. In an effort to avoid the use of diluted HF, we tested the dilute $H_2SO_4/H_2O_2/H_2O$ solution without the use of diluted HF during the post-wet chemical treatment. However, in another wafer that underwent only the dilute $H_2SO_4/H_2O_2/H_2O$ treatment, the PDs with the smallest size exhibited a high dark current of over 100 nA even at a reverse bias of 1 V. This high dark current is attributed to the conductive surface oxide

generated during the dilute $H_2SO_4/H_2O_2/H_2O$ wet-chemical cleaning [110]. A combination of dilute $H_2SO_4/H_2O_2/H_2O$ and diluted H_3PO_4 acid for post-wet chemical treatment may need to be tested.

The responsivity and -3dB bandwidth of the PD is primarily influenced by its size, with the effect of the passivation material being minimal. The results for the responsivity and -3dB bandwidth of the photodetector from this experiment are not repeated here.

6.4 Chapter summary

In summary, this chapter provides a method for optimizing the bias voltage of the low-dark-current PD within the optical amplification module and the large-bandwidth UTC-PD inside the high-speed O\E module to be the same, which reduces system complexity by redesigning the layer stack of the UTC-PD and using suitable planarization materials. A new layer named the Q1.25 layer is introduced between the p-InGaAs and i-InP to "smooth" the energy band at the InGaAs-InP heterojunction interface. This can enhance the transportation of photo-generated carriers across the heterojunction interface. A UTC-PD has been demonstrated, which is biased at -1V to achieve a -3dB bandwidth above 40 GHz and a responsivity around 0.7 A/W, while its dark current is below 1 nA. These results prove that the optimized UTC-PD can meet the requirements of the system design, which involves biasing both the data-detecting PD and the monitoring PD through a single bias feeding circuit. Furthermore, our experimental results suggest that tuning the waveguide etching depth of a waveguide UTC-PD in order to be compatible with a deeply-etched SGC developed for reducing one lithography step did not noticeably degrade the performance of the UTC-PD at low reverse bias. This result reduces the fabrication complexity of the CAO-Rx.

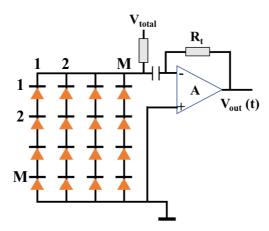
Chapter 7

Passive Receiver Unit Based on A Zero-Volt-Bias UTC-PD

7.1 Introduction

For indoor optical wireless communication (OWC) systems, the transmitted laser beam power is limited to below 10 dBm for $\lambda > 1.4~\mu m$ due to the eye safety regulation. Compared with the OWC receivers with a small aperture, the OWC receivers with a large aperture are expected to collect more optical power at a given field of view (FoV) and decrease the required alignment accuracy of the tracking unit in the transmitter [35]. The high-speed optical receiver with one TIA and a $M \times M$ photodetector array (PDA) connected in series and parallel, shown in Figure 7.1, is a promising OWC receiver, which achieves a large aperture (active area) and wide FoV at the same time [156]. Due to the special interconnection of photodetectors (PDs) in the $M \times M$ PDA, the total capacitance of the PDA is equivalent to that of a single PD, resulting in the same -3 dB bandwidth of the PDA as that of the single PD unit [35].

Recent demonstrations of PDA-based OWC receivers have employed top-illuminated PDs with sub-square millimeter-sized apertures [49,156,157]. These receivers have shown promising performance. Further increasing the aperture of PDA-based OWC receivers would be beneficial to improve their optical power collection efficiency. For a $M \times M$ -PDA-based receiver with top-illuminated PDs, its aperture is equal to the size of the PDA. The maximum allowable side length of a PDA is determined by the product of the maximum



A M×M top-illuminated PDA-based Rx

Figure 7.1: A $M \times M$ top-illuminated-PDA-based receiver (Rx) with series and parallel interconnection [35].

allowable data-dependent jitter (DDJ) at a given transmission speed and the signal propagation speed within the PDA. The signal propagation speed is mainly determined by the material surrounding the PDA transmission line, which is essentially fixed. The DDJ of a PDA is the maximum difference in arrival time of the electrical signal generated by the PDs connected in series within the PDA. The DDJ has a significant impact on the signal integrity of the data eye diagram. If it exceeds the system tolerance, it can degrade the receiver's bit error rate (BER) performance [158]. Consequently, the maximum size of the receiver aperture is primarily limited by the signal integrity of the PDA.

In contrast to top-illuminated PDs, surface grating coupler (SGC)-assisted waveguide PDs decouples the position of the light collection and optical-to-electrical conversion [40]. For a receiver based on a $M \times M$ PDA that incorporates SGC-assisted waveguide PDs, the size of the receiver aperture is primarily determined by the SGC array rather than the size of the waveguide PD array. This decoupling between the waveguide PD array and the receiver aperture provides greater flexibility in designing and optimizing receiver performance. The optical delay in the waveguide leading to the DDJ can be mitigated by adjusting the waveguide length of the SGC-assisted waveguide PD. This adjustment can ensure that the optical signal reaches the PDs simultaneously. The signal

7.1 Introduction 97

integrity of the PDA and the aperture of the receiver can be optimized independently. In other words, waveguide PDs inside a PDA can be put as close as possible to reduce the DDJ without affecting the PDA's light collection and the aperture of the OWC receiver based on SGC-assisted PDs can be tens of times larger than the size of the array of the waveguide PD. Given these benefits, SGC-assisted PDs are expected to be a promising candidate for the next generation of large $M \times M$ PDAs. It should be noted that the coupling efficiency of the SGC is dependent on the incident angle of the optical beam. To increase the coupling efficiency of the beam to the SGC array, a lens can be used to collimate the beam prior to illumination. However, when using external optics, the receiver's FoV is constrained by the étendue law.

A low-bias-voltage OWC receiver is a suitable choice for smartphone platforms as the typical operating voltage of the components is less than 4V [159]. Up to now, the widely used PD is the biased PD. When the bias voltage of a single PD is denoted as V_{bias} , the total bias voltage of a PDA is given as MV_{bias} . The typical bias voltage of a single PIN PD is between -1 V and -5 V. For a large-scale $M \times M$ PDA with an aperture up to dozens of square millimeters, the value M is expected to be large enough, and the total bias voltage will exceed the system budget. If the unit is based on a zero-volt-bias SGC-assisted PD, it converts the optical signal to an electrical signal without an external power supply, and it is a passive unit. By using passive units, the receiver's circuit can be simplified, reducing its complexity [160, 161]. Moreover, previous research has demonstrated that it can realize amplifier-free bias-free optical receivers with high speed and low power consumption by using bias-free waveguide PDs with a capacitance below a femtofarad and a load resistor (e.g., 7 kΩ) [63, 162]. Such optical receivers generate a large voltage swing that can drive the readout circuit without using the power-hungry transimpedance amplifier. However, a single waveguide PD with such a small capacitance is associated with small size, resulting in lower overload current [63]. Using a multiple-PD array $(M \times M\text{-PDA})$ is a good solution. By distributing the received optical power among multiple PDs within a PDA, the risk of PD saturation can be reduced, leading to improved linearity and dynamic range while also mitigating associated performance limitations. Although a zero-volt-bias waveguide PD has a lower bandwidth, it is an option worth considering for large-scale PDA-based receivers, where the total bias voltage supply is limited, and power consumption must be minimized. Since rare reports about the application of the passive unit based on a zero-volt-bias SGC-assisted PD in an OWC system, the performance of a single passive unit should be investigated first in an OWC link before realizing a zero-volt-bias-SGC-assisted-PD-array-based OWC receiver.

7.2 Design and fabrication

Typical types of low-bias PDs include PIN photodetectors (PIN-PDs) and UTC-PDs. Here avalanche photodetectors (APDs) are not considered for zerobias application since the gain of an APD is dependent on the applied bias. Compared with the PIN-PD, the UTC-PD has more potential to be employed in high-speed links with no external bias owing to its wider linear output and higher bandwidth [163, 164]. In the case of a zero-biased PIN-PD, the photogenerated carrier in the undepleted absorption layer is far from the carrier collection layer. Thereby, the linearity performance and the electrical bandwidth of a PIN-PD are restricted by photo-generated carrier transportation, especially photo-generated holes, with low diffusion velocity in the undepleted absorption region [165, 166]. In a UTC-PD, a thin p-doped narrow-bandgap layer with the functions of light absorption and photo-generated hole collection and an unintentionally doped wide-bandgap electron carrier collection layer make up the active area and the heterojunction [167]. Even with no external bias driving, the thin absorption layer can be depleted due to the built-in electric field in the heterojunction [165]. Since the photo-generated holes respond very fast due to the collective motion inside the p-doped layer, the photoresponse of a UTC-PD is determined by the electron transport [163]. By optimizing the layer parameter of the photo-generated electron collection layer, the electron collection layer can be depleted and large electron drift velocity can be maintained at zero bias with the build-in field of the heterojunction, resulting in wide linear output and high bandwidth. Here, we employ a waveguide UTC-PD in our demonstration and implement it for a bias-free OWC receiver.

The waveguide UTC-PD is customized and fabricated on the TU/e Indium Phosphide membrane on Silicon platform, which has high optical confinement [55]. The general fabrication flow for preparing the silicon wafer with membrane-based waveguide UTC-PD devices is described in Section 3.2.2. The high optical confinement, which can decrease the absorption length of the waveguide PD, is essential to obtaining small-size waveguide PD with high responsivity and large bandwidth [168]. The size of the UTC-PD is chosen to be $10 \times 2~\mu\text{m}^2$. A $10~\mu\text{m}$ length, combined with a 150 nm absorption layer thickness, has been demonstrated to achieve maximum absorption efficiency on the IMOS platform [82]. This compact size of the UTC-PD results in reduced capacitance, which is crucial for attaining a large bandwidth. The redesigned layer stack of the waveguide UTC-PD can be referred to Fig. 6.1 (a). Chapter 6 contains a detailed description and discussion of the layer stack used in this study. The bending of the conduction band of p-InGaAs and i-InP, which is shown in Fig. 6.1 (b), means

that those layers are fully depleted, which allows electron carrier to drift from the p-InGaAs absorption layer to the n-InP contact layer at zero bias. Since carrier drift velocity is higher than the carrier diffusion velocity, a large bandwidth zero-bias UTC-PD can be obtained [166]. The insertion of the Q1.25 layer between the p-InGaAs and i-InP results in the formation of a low energy step at the InGaAs-InP heterojunction interface, as observed in the energy diagram shown in Fig. 6.1 (b). This modification is to alleviate the accumulation of photo-generated electrons at the InGaAs-InP heterojunction interface under zero bias conditions. Consequently, this allows smooth electron carrier transportation at the interface of p-InGaAs and i-InP, thus decreasing the required operating voltage.

7.3 Device characterization and system implementation

The basic device performance of the utilized UTC-PD, such as dark current, photocurrent (responsivity), and -3 dB bandwidth, are investigated first. Then the system performance under the 10 Gb/s back-to-back link and the OWC link over 1.1 m are evaluated by utilizing this proposed zero-volt-bias UTC-PD as the passive receiver unit.

7.3.1 Device performance

Figure 7.2 (a) shows the structure of the waveguide UTC-PDs, consisting of an SGC (grating size: $10 \times 10~\mu\text{m}^2$), a 500- μ m waveguide, a waveguide UTC-PD, and a GSG pad. To calibrate the coupling loss from the fiber to the waveguide and the propagation loss of the waveguide, we performed standard waveguide loss measurements on a reference waveguide array fabricated on the same chip. The grating coupling loss was measured to be 4 dB at 1529 nm for an input fiber angle of 7 °, and the propagation loss of the waveguide was 10 dB/cm. By optimizing the fabrication process and the design of the SGC, the center wavelength of the SGC can be shifted to 1550 nm, as the optimization of the surface grating and the waveguide UTC-PD are decoupled.

The membrane-based waveguide UTC-PD has a size of $10 \times 2 \mu m^2$, and Figure 7.2 (b) shows the dark current of three such devices as a function of bias voltage. The dark current is less than 1.5 nA, even at -1 V. This low dark current is due to the effective surface wet cleaning method used after ICP dry etching

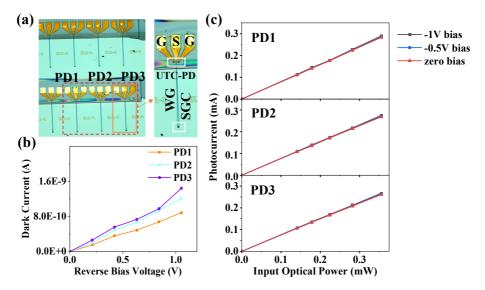


Figure 7.2: (a) Optical microscope image of the photodetector array enabled by SGC-UTC-PDs. SGC: surface grating coupler; WG: waveguide; UTC-PD: unitravelling carrier photodetector; GSG pad: ground-signal-ground pad;(b) Dark current as a function of reverse bias voltage curve for three membrane-based waveguide UTC-PDs with PD size of $10 \times 2 \ \mu m^2$ and (c) Photocurrent versus optical power coupled to three UTC-PDs of $10 \times 2 \ \mu m^2$, showing good linearity and weak bias dependence.

and BCB passivation. At zero bias, the dark current can be considered negligible.

A grating coupler and a UTC-PD are connected by a 500- μ m waveguide. Based on the measurement of grating coupling loss and waveguide propagation loss, the power loss from the fiber probe to the membrane-based waveguide UTC-PD is calculated to be 4.5 dB. The responsivity of the $10 \times 2~\mu\text{m}^2$ UTC-PD is determined by measuring the photocurrent as a function of input optical power at 1529 nm, and the results are presented in Figure 7.2 (c). The input optical power refers to the optical power that is injected into the UTC-PD, accounting for the insertion losses of the SGC and the waveguide here. The static performance of three such PDs is summarized in Table 7.1, with PD1 showing a responsivity of 0.80 A/W and 0.82 A/W at bias voltages of 0 V and -1 V, respectively. The output photocurrent demonstrates a good linear relationship

No. PD	Internal responsivity (A/W)			Dark current (nA)		
	0 V	-0.5 V	-1 V	0 V	-0.5 V	-1 V
PD 1	0.8	0.81	0.81	\	0.4	0.83
PD 2	0.76	0.77	0.77	\	0.56	1.1
PD 3	0.75	0.76	0.76	\	0.63	1.36

Table 7.1: Basic device performance of three PDs

with the input optical power at zero bias, and the maximum linear input power at zero bias is 0.75 dBm, corresponding to an output current of 0.95 mA, as measured from a UTC-PD with the same size and from the same wafer. The responsivity of this membrane-based waveguide UTC-PD displays weak bias dependence, indicating that it can be used as a bias-free receiver.

A commercial Agilent lightwave component analyzer (LCA) with 67 GHz bandwidth is utilized to measure the -3 dB electrical bandwidth of the UTC-PD with the size of $10 \times 2 \mu m^2$. The tunable laser source is modulated by the sweeping frequency signal from 0 to 50 GHz generated from LCA. The modulated optical signal is amplified by an erbium-doped fiber amplifier (EDFA). One polarization controller is inserted between an EDFA and the fiber probe to control the polarization state of the light. The setup for measuring the bandwidth of the PD is shown in Figure 7.3 (a). The output optical power of the fiber probe is set at 4 dBm. The normalized frequency response (S21) measured at various voltages from -1 V to 0 V ranging from 0 GHz to 30 GHz is shown in Figure 7.3 (b). The -3 dB bandwidth of this waveguide UTC-PD (PD1) is 13.3 GHz at 0 V and 24 GHz at -1V, respectively. The results show that it is sufficient to support 10 Gbaud signal detection at zero bias condition without introducing obvious distortion since 7 GHz electrical bandwidth is required to hold 10 Gbaud signal, which corresponds to only 1.7 dB loss as shown in Figure 7.3 (b). In Figure 7.3 (b), a discrepancy in the -3dB bandwidth of the device is observed under varying bias conditions (0V and -1V). The observed discrepancy may be due to the existence of a residual energy band discontinuity at the interface between InP and p-InGaAs. This discontinuity still exists even when the introduction of a band-smoothing layer reduces the energy band step. This energy band step might continue to trap photogenerated electrons at the interface, thereby affecting the bandwidth under various biases.

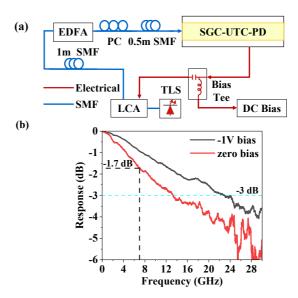


Figure 7.3: (a) Experimental setup for 3-dB bandwidth measurement. TLS: tunable laser source; LCA: lightwave component analyzer; EDFA: erbium-doped fiber amplifier; PC: polarization controller; SGC-UTC-PD: surface grating coupler-assisted uni-travelling-carrier photodetector; SMF: single-mode fiber. (b) Measured frequency response of the membrane-based waveguide UTC-PD with the PD size of $10 \times 2 \ \mu \text{m}^2$.

7.3.2 Transmission experiment

Experimental setup

The proposed monolithic integrated bias-free optical receiver is further implemented in a 10 Gb/s OWC link, whose experimental setup is shown in Figure 7.4 (a). Due to the limitation of the maximum sampling rate of the employed bit-error-ratio tester (BERT), the transmitted signal is set to 10 Gbaud with OOK modulation. In our demonstration, a tunable laser source with 12 dBm output optical power combined with a Mach-Zehnder modulator (MZM) is used to generate the modulated optical signal, which is driven by the electrical data produced from the BERT after amplification. We built two separate routes, represented as Route A and Route B for back-to-back and 1.1 m OWC links, respectively. The transmitted free space distance of the collimated beam with the

beam diameter of 7 mm by the fiber collimator with a focal length of 18 mm and the full angle divergence of 0.034° is limited by our testbed. For the collimated beam, the path loss is mainly caused by optical alignment, not the indoor wireless channel. Thus, it is feasible to extend the wireless transmission distance to the practical interest value of no less than 3 m [169]. The launched optical power into free space is measured to be less than 10 dBm at 1529 nm after optical amplification by an EDFA, which meets the requirement of human eye safety. At the receiver, the received optical beam is coupled into a short section of single-mode fiber via another fiber collimator and then fed into the proposed integrated bias-free optical receiver for further optical-to-electrical detection. A variable optical attenuator is inserted between the PC2 and the fiber probe to adjust the input optical power into the chip. The fiber probe is set at 7° and the coupling loss is 4 dB. The output electrical signal from the membrane-based waveguide UTC-PD is passed through a bias tee to extract the desired AC signal,

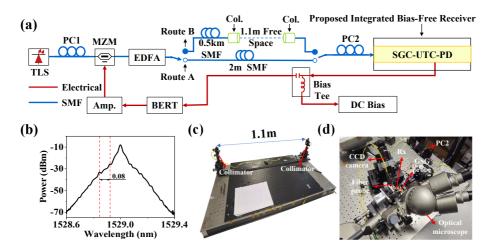


Figure 7.4: (a) Experimental setup based on the proposed bias-free optical receiver. Route A: back-to-back; Route B: 1.1 m OWC link; TLS: tunable laser source; PC: polarization controller; MZM: Mach-Zehnder modulator; EDFA: erbium doped fiber amplifier; SMF: single-mode fiber; Col.: collimator; SGC-UTC-PD: surface grating coupler-assisted uni-travelling-carrier photodetector; BERT: Bit-error-ratio tester; (b) Optical spectrum modulated by 10 Gb/s OOK signal; (c) Photo of the OWC link; (d) Photo of the chip coupling system. Rx: receiver.

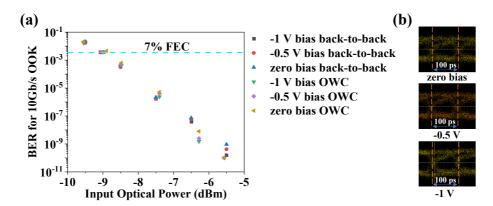


Figure 7.5: (a) BER Performance of received 10 Gb/s OOK signal by using the monolithic integrated membrane-based waveguide UTC-PD receiver unit at different biases; (b) The eye diagrams of 10 Gb/s OOK signal are measured from OWC link at input optical power of -6 dBm at different bias.

which is finally fed back into the receiver side of BERT for BER calculation. No electrical amplifier was utilized When conducting this transmission experiment. Figures 7.4 (b), (c), and (d) show the optical spectrum of the modulated 10 Gbaud OOK signal centered at 1529 nm and pictures of the OWC link and chip coupling system, respectively.

Optical back-to-back and OWC performance

The performance of the proposed bias-free receiver unit with 10 Gb/s signal modulation is verified both at back-to-back and after a 1.1 m OWC link. We measured the BER performance of the 10 Gb/s signal as a function of input optical power at different reverse bias voltages as shown in Figure 7.5 (a). At the 7% FEC limit of 3.8×10^{-3} , the receiver sensitivity of 10 Gb/s signal is -8.99 dBm at zero external bias voltage. The receiver sensitivity is further improved to -9.08 dBm at the same 7% FEC limit under -1 V bias voltage. After 1.1 m free-space transmission, the receiver sensitivity of 10 Gb/s signal is -8.85 dBm at zero external bias voltage and is further improved to -9.01 dBm under -1 V bias voltage at the 7% FEC limit of 3.8×10^{-3} . The measured results in Figure 7.5 (a) show that the maximum sensitivity difference of 0.16 dB at different bias voltages is observed for both back-to-back and 1.1 m OWC link, which reveals

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the feasibility of our proposed bias-free receiver. This result suggests that the difference in bandwidth has minimal influence on the receiver sensitivity of this receiver unit operating at a 10-Gb/s optical link. In Figure 7.3, the electrical power output at a 7-GHz frequency response is observed to show a 0.76 dB difference between the device operating at 0 V and -1 V while maintaining the same input optical power. The calculated responsivity drop of the PD is 0.38 dB when detecting the optical signal at 0 V and -1 V. The explanation for this phenomenon is that this device's smallest bandwidth, measured at 0 V, exceeds the minimum requirement for transmission of a 10 Gb/s OOK signal by a factor of two. Besides, the dark current of this receiver unit at 0 V is significantly lower than that at -1 V. Consequently, the reduced bandwidth (resulting in longer pulse duration) and the increased intersymbol interference (ISI) have negligible impact on receiver sensitivity [170, 171]. It is noticed that the values of receiver sensitivities are excluded the 4 dB coupling loss from the surface grating. Since the linear regime input power of this zero-bias UTC-PD is below 0.75 dBm, the dynamic range of this proposed bias-free receiver is around 9.6 dB. Figure 7.5 (b) shows the measured eye diagrams of 10 Gb/s OOK signal after 1.1 m OWC link, corresponding to the BER values of around 10^{-9} . Our proposed optical receiver unit achieves a 10 Gbps data rate by combining a zero-bias UTC-PD with cost-efficient OOK modulation without requiring digital signal processing. This design meets the requirements for low cost and low power consumption in OWC applications. Furthermore, by fully utilizing the 3-dB bandwidth of 13.3 GHz, the detected signal baud rate can be increased to 19 Gbaud by using this demonstrated zero-bias receiver unit.

7.4 Discussions

Recent advances in zero-Bias PD for optical communications

Table 7.2 compares our work with previously reported high-speed zero-bias PDs, including edge-coupled silicon-based PDs and top-illuminated and edge-coupled InP-based PDs [174–176]. However, these devices are not fully compatible with a large PD matrix scheme. Edge-coupled PDs, despite their high speed, have a limited aperture and input ports located at the edge of the chip, making them unsuitable for use in a large-scale PD array compared to SGC-assisted PDs or top-illuminated PDs. In a PD array with top-illuminated PDs, the light collection and opto-electrical conversion occur at the same position, resulting in a high DDJ. To ensure signal integrity within a PD-array-based receiver, it is

Table 7.2: Comparison of the passive unit enabled by different types of zero-bias PD

Zero-volt-bias PD type	This work (SGC-assisted InP-based PD)	edge-coupled InP-based PD [172]	back-illuminated InP-based PD [173,174]	top-illuminated InP-based PD [175]	edge-coupled Si-based PD [176]
Aperture scalability	///	✓	√ √	√√)	✓
Internal responsivity	0.8A/W	0.48A/W	\	\	0.78A/W
External responsivity	0.28A/W	0.17A/W	0.19A/W	0.09A/W)	\
-3dB bandwidth (GHz)	13.3	66	>110	>170	\(support 40 Gb/s link)
Receiver unit sensitivity (7% FEC)	-8.85dBm (10Gb/s OWC link	Experiment was not performed.	9dBm(56Gb/s fiber link	Experiment was not performed.	Experiment was not performed.
Power penalty of unit under reverse bias/ zero-volt bias	0.16dB (10Gb/s OWC link)	Experiment was not performed.	Experiment was not performed.	Experiment was not performed.	Experiment was not performed.

necessary to control the DDJ to a level below 17 % of the unit interval. This control level is specified in the IEEE standard 802.3 ap-2007 for receiver interference tolerance [177], with a target bit error rate (BER) below 10^{-12} . For a 10 Gb/s link, the unit interval of the signal is 100 ps, and the DDJ should be less than 17 ps. To realize on-chip metal interconnection, low-permittivity materials such as BCB layer or SiO₂ are often used as interlayer dielectrics. In this work, we assume the use of BCB material, which has a permittivity between 3.2 and 3.9 [178]. If we choose the permittivity of the BCB to be 3.5, the signal propagation speed on the transmission line inside the BCB is around 160 μ m/ps. For a 10 Gb/s signal, the maximum tolerance for the length difference in signal propagation is below 2720 um for a PDA using top-illuminated PDs. Thus, the PDA's side length must be less than 2720 μ m. In contrast, SGC-assisted PDs decouple light collection and optical-to-electrical conversion, allowing waveguide PDs to be placed closer and enabling a larger PDA aperture. Our demonstrated zero-bias SGC-assisted UTC-PD has a relatively high internal responsivity, which can be further improved by enhancing the coupling efficiency of the SGC. The -3dB bandwidth of the zero-bias SGC-assisted PD has the potential to achieve high enough -3dB bandwidth to meet the requirement of 40 Gbps transmission speed since some high-performance zero-bias PDs were demonstrated with -3dB bandwidth over 110 GHz [174, 175]. In this work, the minor power penalty be7.4 Discussions 107

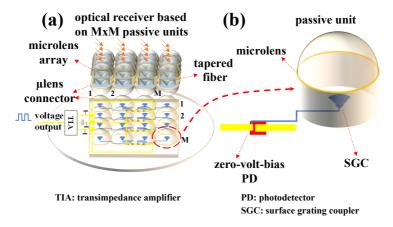


Figure 7.6: (a) Schematic of a large-aperture OWC receiver based on a $M \times M$ proposed passive unit. The output signal from the PD array is amplified by a TIA. The combination of a microlens array, a tapered fiber array, and a μ lens connector is proposed to couple light from free space for $M \times M$ passive unit. (b) Passive unit based on a SGC-assisted zero-volt-bias PD with a microlens of the μ len connector to couple light.

tween an optical link with this customized zero-bias PD and that with the same PD under bias is experimentally demonstrated, which is not discussed in previous work. It is attractive to realize the passive unit based on an SGC-assisted PD for the large-aperture PD-array-based OWC receiver and evaluate its system performance under bias/zero-bias conditions.

Feasibility to realize a PD-array based OWC receiver by SGC-assisted PDs

To determine the feasibility of using this device in a large-scale PD array, it is necessary to evaluate it within that context. In our previous work, the aperture of the 1 Gbps OWC receiver was 0.86 mm \times 0.86 mm. Our goal is to achieve a 10 Gbps OWC receiver with a larger aperture of 5 mm \times 5 mm.

The Power Budget of This Receiver with Large Aperture. To estimate the received optical power of this receiver, we focused primarily on the coupling loss between free-space light and the SGC array. Given that the field of view (FoV) of the microlens-SGC unit reported in Ref. [46] is less than 2°, and an SGC has a limited FoV, it is not appropriate to couple light directly from free space to the SGC-assisted PD array through a microlens array. Instead, we used the insertion

loss values for each component mentioned in the previous work as a reference to estimate the path loss between free space and an SGC for a single unit. Figure 7.6 shows the proposed new structure for coupling light from free space to an SGC-assisted PD array using a microlens array, a tapered multimode fiber array, and a fiber-to- μ Lens-to-SGC connector.

We expect this structure to have the lowest insertion loss. In Ref. [179], a microlens array connected to a fiber array was used to couple light from free space. To achieve a large field of view (FoV) and collect as much optical power as possible, a unit combining a microlens with a suitable focal length and a tapered fiber with a multimode fiber input with a large numerical aperture is more effective than a unit combining a microlens with a single mode fiber input, since multimode fibers have larger diameters and numerical apertures. To ensure compatibility with the fiber-to- μ Lens-to-SGC connector described in Ref. [180], the tapered fiber should have a single-mode fiber output. This connector has an array pitch of 250 μ m, so the PD array with an aperture of 5 mm \times 5 mm will have a matrix size of 20 \times 20.

Figure 7.7 illustrates the various components that contribute to the total insertion loss. The insertion loss between the single-mode fiber inside the fiber-to- μ Lens-to-SGC connector and each SGC (denoted as IL_1) is equal to the coupling loss between the single-mode fiber and each SGC [180]. In our case, the coupling loss (CL_1) is 4 dB. In work done by Yang et al. [181], a tapered multimode fiber with a multimode fiber input diameter of 200 μ m and a single mode fiber output diameter of 10 μ m was reported, with a mode conversion efficiency > 95% (-0.2 dB). The insertion loss of this tapered multimode fiber is denoted as IL₂. To couple sufficient light from free space to the tapered multimode fiber, a high filling factor of the microlens array is required, and the FoV of the unit formed by a microlens and a tapered multimode fiber should be large enough. This requires the microlens to have a small enough focal length and the fiber to have a large enough diameter. Microlens with a large diameter provides high light collection efficiency but also results in a longer focal length. To balance these factors, we selected the microlens parameters reported in Ref. [182], with a diameter of 200 μ m and a focal length of 250 μ m. The insertion loss (IL₃) of this unit primarily comes from the small filling factor, which is 0.64 and results in a power loss of -1.9 dB. The expected FoV of this unit is around 43 degrees. The coupling loss between a microlens and a fiber is 0.92 dB (IL_4), as reported in Ref. [179]. The waveguide insertion loss between the SGC and the waveguide PD is denoted as IL_5 . The maximum transmit optical power for an OWC link is limited to 10 dBm due to eye safety regulations. The maximum received effective power of a PD array with aperture dimensions of 5 mm × 5 mm can

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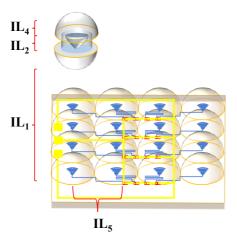


Figure 7.7: A schematic diagram illustrating the five components contributing to the total insertion loss. IL_1 represents the insertion loss between the single-mode fiber within the fiber-to- μ Lens-to-SGC connector and each SGC. IL_2 refers to the insertion loss of the tapered multimode fiber. IL_3 is predominantly due to the fill factor of the microlens, although this particular aspect is not shown in the diagram. The filling factor refers to the ratio of the area covered by the microlens array to the total aperture area. IL_4 corresponds to the coupling loss between a microlens and a fiber, while IL_5 denotes the propagation loss of the waveguide.

be expressed as 10 - 10 $\log_{10}(M)$ - IL_1 - IL_2 - IL_3 - IL_4 - IL_5 , where M is the number of elements in the array. In our proposed PD array, M is equal to 20.

When the beam size is 7 mm, it nearly matches the 5 mm \times 5 mm aperture size. Under illumination with a beam diameter of 7 mm, the maximum received power of this PDA-based optical receiver is estimated to be around -10.5 dBm, with each individual photodiode receiving -23.5 dBm of optical power. The 7 % FEC receiver sensitivity of a 10 Gbps PIN-TIA receiver is approximately -26 dBm [66], which suggests that the OWC link can be built using this receiver configuration. Developing these new components to couple free-space optical signals for the SGC array requires further investigation.

The Signal Integrity in This Receiver with a Large-Scale PDA. To simplify the model, we consider only the PDs located on the longest transmission line. The signal propagation delay is largest along this path from the upper left PDs to the lower left PD. We set the pitch of the photodiode array to $50 \mu m$, which is

six times the maximum length of one PD and should be sufficient for the required layout. The side length of the square filled with a 20×20 PDA will be 950 μ m. Since the signal propagation speed on the transmission line inside the BCB is around 160 μ m/ps, the propagation delay is 5.94 ps, which is well below the maximum allowed data-dependent jitter of 17 ps for 10 Gbps signals. The receiver with a 20×20 PDA is expected to be an aperture of 5 mm × 5 mm². This indicates that the maximum aperture of the optical receiver with an SGC-assisted PD array can be up to 14.3 mm × 14.3 mm.

Comparison Between the PD Array Realized by Zero-Bias\Biased PDs.

The typical bias voltage of a PIN PD is between -1 V and -3 V. We chose a bias voltage of -1 V here to do the estimation. For a 20×20 PDA, the total bias voltage is -20 V. Our demonstrated zero-bias and -1 V biased PD exhibit similar responsivity. The advantage of a biased PD is its higher bandwidth and higher saturation optical power. In the next generation of zero-bias SGCPDs, we can optimize device size, fabrication process, and photodiode layer stack to achieve a -3 dB bandwidth greater than 13.3 GHz, satisfying the required bandwidth for our future application requirement. Although the demonstrated zero-bias PD saturates at 0.75 dBm, the maximum received optical power of a zero-bias PD in a PDA with a 5 mm \times 5 mm aperture is -23.5 dBm, as calculated in the previous section.

7.5 Chapter summary

In this chapter, we experimentally demonstrate a 10 Gb/s bias-free OWC receiver enabled by a zero-bias UTC-PD. The zero-bias waveguide UTC-PD is designed and fabricated with the size of $10 \times 2~\mu\text{m}^2$. Without external voltage driving, it exhibits good performance with a -3 dB bandwidth of 13.3 GHz and responsivity of 0.80 A/W. Enabled by the proposed bias-free optical receiver, we further successfully achieve a receiver sensitivity of -8.85 dBm at 7% FEC limit of 3.8×10^{-3} for the 10 Gb/s OWC link over 1.1 m free space. The experimental results also show the weak bias dependence property of BER performance for 10 Gb/s OOK signal at zero-bias and -1V bias. The feasibility of realizing a PDA based on this zero-bias SGC-assisted waveguide PD is discussed, which paves the way to the realization of the large-aperture optical receiver based on zero-bias SGC-assisted waveguide PD array in the future.

Chapter 8

Summary and future outlook

8.1 Summary

In the research work described in this thesis, major steps have been made towards a high-sensitivity large-aperture cascaded aperture optical receiver (CAO-Rx) using a surface grating coupler (SGC), cascaded semiconductor optical amplifiers (SOAs) and a uni-traveling-carrier photodetector (UTC-PD), which is used as an optical wireless receiver. These components have been designed, implemented, and verified by developing customized components on photonic integration platforms. The CAO-Rx demonstrated in this work has an aperture size of $10 \times 10~\mu m^2$ and a 1-dB field-of-view (FoV) of 2 degrees. This work is the first step towards realizing a complete fully integrated high-sensitivity large-aperture cascaded aperture optical receiver (CAO-Rx) on the IMOS platform in the future. Additionally, the receiver unit based on a high-performance zero-volt-bias CAO-Rx has been validated in a 1.1-m indoor free-space 10Gb/s link using an optical beam with a diameter of 7 mm. The proposed receiver unit paves the way to the realization of a high-speed array-based optical wireless communication (OWC) receiver with an aperture beyond $5 \times 5~\text{mm}^2$ in the future

The key findings from this research are listed below.

A CAO-Rx with a metal reflector-assisted grating coupler (SGC) was proposed and demonstrated in chapter 4. A reflector is introduced under the grating area for reflecting more light and enhancing the light coupling into a waveguide. First, we developed a prototype of a linear metal reflector-assisted SGC

(MRSGC), which demonstrated high coupling efficiency of -3 dB at the central wavelength of 1540 nm. The size of MRSGC is $10 \times 10 \ \mu m^2$, and it has a -1 dB bandwidth of 30 nm and a 1-dB FoV of 2 degrees. This MRSGC design is optimized for TE polarization (with polarization-dependent loss >20 dB). Subsequently, we experimentally verified, for the first time, the monolithic cointegration of the MRSGC and the UTC-PD in the Indium Phosphide membrane on Silicon (IMOS) platform. The validation begins with the fabrication. In order to achieve a precise definition of the dimension of the SGC during fabrication, it is necessary to address the issue of dimension mismatch between the lithography mask and the fabricated size. This can be achieved by performing an additional run to modify the lithography mask to compensate for the dimensional loss during fabrication. Given the stability of the e-beam lithography equipment, this adjustment remained constant over the subsequent three runs. While the use of BCB as a bonding material provides the flexibility to adapt to the topology of a quarter of a 2-inch InP wafer during the fabrication of the CAO-Rx, the wafer bonding process remains a significant challenge. Spinning the BCB onto the InP wafer and the silicon carrier wafer separately and bonding them together directly using soft-baked BCB has been shown to achieve good bonding quality. The use of a soft-baked BCB layer during the bonding process has been shown to improve tolerance to variations in the height topology caused by the mesa structure of the wafer and the spinning process. However, caution must be taken to avoid the incorporation of air bubbles into the soft-baked BCB during the bonding process, which can compromise the bonding quality. The dry etching rates of the grating groove above the metal layer and the one above the dielectric layer differ, which makes it difficult to ensure performance-optimized etching for both SGC types in a single run. Consequently, a comparison between the SGC with and without a metal reflector was performed using separate runs. Finally, we measured the back-to-back sensitivity of the CAO-Rx with a metal reflector without any amplifiers for a 10 Gb/s link, which was calculated to be 1.5 dB better than that of a CAO-Rx without a metal reflector. Overall, our results demonstrate the potential of the proposed CAO-Rx with a MRSGC for improving coupling efficiency in optical communication systems.

An optical receiver based on a novel noise-reduction optical amplification scheme by integrating cascaded SOAs has been designed, fabricated, and validated to achieve high sensitivity based on photonic integration technology in Chapter 5. Compared with utilizing just a one-stage optical amplifier, using multiple independent SOAs with the same total length in a multi-stage optical amplifier offers the advantage of being able to optimize the noise figure of each optical amplifier independently by tuning their injection currents, which leads

8.1 Summary 113

to the reduction of the total noise and an improvement of the receiver sensitivity. While making a trade-off between the contribution of the noise figure at each stage and the complexity of driving the injection currents individually, the tested receiver consists of a single waveguide PIN photodetector integrated with two cascaded SOAs. The achieved receiver sensitivity for a 10 Gb/s OWC link over 0.9 m free space is -27.5 dBm. Compared with the one-stage SOA-PIN receiver, the measured receiver sensitivity based on the proposed method is improved by 1.5 dB for 10 Gb/s OOK signal at the 7% FEC limit. By combining optical and electrical amplification (SOA-OBPF-PIN-TIA), where an optical bandpass filter (OBPF) is added to further reduce ASE noise, a higher sensitivity receiver is achieved. The OBPF is expected to further enhance the receiver sensitivity by a minimum of 2 dB or more [69].

An optical receiver with bias voltage-optimized PDs is achieved by implementing updates to the PD fabrication process of the IMOS platform, shown in Chapter 6. In particular, we have refined the PD's layer stack design to achieve a -3-dB bandwidth of 40 GHz when operating at a reverse bias voltage of 1 V. Additionally, we developed new passivation techniques to decrease the dark current of the waveguide UTC-PD at specific bias voltages. The updated UTC-PD layer stack on the IMOS platform incorporates an extra O1.25 (InGaAsP) quaternary layer, which is undoped, positioned between the InGaAs absorption layer and the InP carrier collection layer. This unintentional doping approach can be reliably reproduced during the wafer epitaxy process. This Q 1.25 layer is demonstrated to be effective for suppressing the electron accumulation at the InGaAs-InP heterojunction interface and decreasing the bias dependence of the -3 dB bandwidth. Moreover, the use of passivation (planarization) materials should be dependent on the PD mesa structure. Our results show that the BCB material is effective in passivating the PD mesa when the waveguide layer is etched away and the Q1.25/InGaAs layers are opened. On the other hand, it appears that the SiO₂ material can effectively passivate the PD mesa when a thin InP layer (part of the waveguide layer) is retained. Finally, a UTC-PD has been demonstrated, which is biased at -1V to achieve a -3dB bandwidth above 40 GHz and a responsivity around 0.7 A/W, while its dark current is below 1 nA. The results of this study demonstrate that the optimized UTC-PD is capable of meeting the system design requirements. It is crucial to note that the low drive bias of this type of UTC-PD satisfies the requirement for heterointegration of the UTC-PD on a CMOS chip, which is necessary to fully utilize the advantages of the IMOS platform. Specifically, the operating voltage for CMOS circuits is below 1.5 V [91]. To achieve the heterointegration of UTC-PD and CMOS circuit on the IMOS platform, it is crucial to maintain the driving voltage of the UTC-PD component above -1.5 V [82]. This is particularly important for the close integration of a photodetector and electronic amplifier, which can result in optimal receiver performance and a compact design [39].

A high-speed passive unit based on a zero-volt-bias CAO-Rx is demonstrated for the potential large-scale array-based OWC receiver. In earlier work [35], a large-aperture receiver concept was proposed to achieve a square millimeter-sized aperture, which was demonstrated to enhance light collection and field of view with minimal bandwidth degradation. The architecture of a CAO-Rx array can be used to further increase the aperture of an on-chip OWC receiver, utilizing the same approach. The number of PDs in a PD array is inherently greater than in an optical receiver using a single PD. This increase in the number of PDs may require a bias voltage that exceeds the capacity of the system. A non-biased PD, or zero-volt biased PD, with sufficient bandwidth to meet data rate requirements is an effective alternative to biased PDs for arraybased OWC receivers. In Chapter 7, we not only developed a zero-volt-bias CAO-Rx with an acceptable large bandwidth for the prototype of a 10-Gb/s OOK array-based receiver but also validated its transmission performance in a 10 Gb/s OWC link. A new layer stack of the UTC-PD on the IMOS platform is designed for maintaining large carrier drift velocity in order to achieve an acceptable bandwidth at zero-volt bias. And the size of the UTC-PD is optimized to improve PD's responsivity while maintaining an acceptable -3 dB bandwidth (for supporting a data rate > 10 Gb/s). The photocurrent of the zero-voltbias waveguide UTC-PD shows good linearity when the input optical power of the UTC-PD stays below 0.75 dBm. Based on the measured beam-to-receiver coupling efficiency of -7 dB (comprising -4 dB for the MRSGC coupling efficiency and -3 dB for the transmitter-collimator-to-receiver-collimator coupling efficiency) in this study, the OWC link with an OWC receiver based on a single zero-bias UTC-PD should have a maximum allowable beam power of 7.75 dBm or less. The low coupling efficiency between the transmitter and receiver collimators is primarily caused by the beam-to-receiver-collimator misalignment. Although the aperture of the receiver collimator is 7 mm, the collimator used in the OWC link has a narrow full FoV of only 0.03 °. Precise alignment is crucial for further improving the coupling efficiency. If the coupling efficiency of beam-to-receiver improves, the maximum allowable beam power should be correspondingly reduced. In terms of the transmission performance of a 10 Gb/s OOK signal OWC link with a zero-volt-bias CAO-Rx, it was found that there was only a minor receiver sensitivity penalty (<0.2 dB) when compared to the same CAO-Rx with -1V bias. The results in the previous study show that the bandwidth performance of a single receiver unit is the same as that of the 8.2 Future outlook 115

novel large-aperture receiver concept based on a large-scale M x M receiver unit array [35], where the receiver array is based on series and parallel interconnections. Therefore, the demonstrated zero-volt-bias CAO-Rx can potentially serve as a unit in a CAO-Rx array to relieve the power supply stress of the CAO-Rx-array-based receiver, as suggested by these findings.

8.2 Future outlook

This work is the first step towards realizing a fully integrated high-sensitivity large-aperture cascaded aperture optical receiver (CAO-Rx) on the IMOS platform in the future.

In this study, a mature SGC design optimized for transverse electric (TE) polarization (with polarization-dependent loss >20 dB) is used to decrease the fabrication challenge. In practical application, a polarization-insensitive SGC will be preferable. As noted by Zhao et al. [183], the polarization state of a laser beam remains unchanged as it propagates in free space. However, when the laser beam is emitted from the fiber laser at the transmitter side, the polarization state of the laser beam may change. Utilizing an SGC design optimized for TE polarization may result in lower coupling efficiency. To mitigate this challenge, it is recommended to consider adopting a polarization-insensitive SGC design. Two types of polarization-insensitive SGCs have been developed: the two-dimensional (2D) SGC and the one-dimensional (1D) SGC [122, 184]. The 2D SGC has two outlets, one for TE and the other for TM polarization [184], and is considered more mature. However, for successive signal detection or amplification, a polarization rotator or two identical functional devices (without rotators) should be used at the cost of a larger footprint or additional power loss. Song et al. (2015) developed a polarization-insensitive 1D SGC that consists of the intersection or union of two TE and transverse magnetic (TM) mode grating designs [122]. This approach enables TE and TM light to be coupled into a single waveguide without the need for polarization rotators or the use of two identical functional devices without rotators. This type of SGC has lower coupling efficiency, but it is still a viable option. Exploring the possibility of extending these two SGC structures to larger apertures and evaluating their fabrication challenges and compatibility with grating apodization techniques for OWC application would be worthwhile. The grating apodization technique is crucial for SGCs with larger apertures as it prevents degradation of the coupling efficiency compared to the SGCs optimized for the signal-mode fiber coupling [40].

In the future, a large-aperture CAO-Rx can be proven, and the SGC can be

optimized for a large aperture to catch the light as much as possible. One effective method to achieve this is by tuning the SGC's design to lower its scattering efficiency, either by decreasing its filling factor or groove etching depth, as demonstrated in Ref. [185,186]. If the laser beam waist exceeds 250 μ m, updating the SGC design to match the SGC with a larger beam waist using methods such as decreasing the filling factor or groove etching depth may be challenging. This is because of the high fabrication requirements, which demand etching depth < 10 nm and width < 90 nm. To couple light from free space to the SGC, a combination of aspherical or cylindrical lenses can be utilized, as shown in [187, 188]. Incorporating these external optics to enlarge the aperture of the CAO-Rx receiver inevitable makes the module larger. Collecting a free-space expanded beam using on-chip components for the SGC remains a challenge. The term "expanded beam" refers to a beam with a larger beam waist than that of the SGC's mode field diameter. Two on-chip components have been developed to couple the expanded beam emitted from the fiber to the SGC [46, 189]. The first method involves integrating an on-chip microlens with the SGC [46]. This approach successfully couples the expanded beam, achieving a -1 dB FoV for fiber-to-grating coupling with an angle of 0.6°. The second method, proposed by Israel et al. [189], focuses the large-diameter beam onto the chip with the SGC using on-chip mirrors. These mirrors are created by bonding a thick substrate with curved mirrors on both sides to the chip with the SGC. This technique has been demonstrated with a -1 dB FoV for fiber-to-grating coupling at an angle of 0.35°. Both these on-chip components exhibit a power penalty of less than 1 dB. Further investigation is needed to determine whether these two components can be utilized for coupling light from space, potentially enabling the development of a compact CAO-Rx.

The OWC receivers with wide FOV are generally preferred due to their ability to simplify the alignment process between the transmitter and receiver. However, in this study, the -1-dB FoV of the CAO-Rx is only approximately 2°. Hence, it is attractive to explore potential strategies for enhancing the FoV of the SGC in the CAO-Rx in future research. Specifically, efforts can be undertaken to refine the design of the SGC or using the beam with multi-mode in the OWC link. One potential approach is to incorporate a metasurface layer (metalens) on top of the SGC. This specially designed metal lens enables beam deflection, thereby improving the SGC's ability to couple light from a wide range of angles [190] Consequently, it is worth investigating the feasibility of integrating an SGC with a metasurface layer and a high-speed PD together. Another potential approach is that the utilization of multi-mode light as the input beam has been demonstrated to effectively double the FOV of the SGC [191]. A previous study has also

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confirmed the feasibility of an OWC link employing a multi-mode beam [192]. However, in order to ensure compatibility with the multi-mode beam, it is necessary to redesign the SGC of the CAO-Rx to achieve optimal coupling efficiency. Investigation into this aspect is still required.

Chapter 6 describes two PD mesa structures designed to be compatible with the shallowly-etched SGC and the deeply-etched SGC, respectively. The first type of PD mesa, which has Q1.25\InGaAs opened and not protected by a thin InP layer, was tested using two planarization materials: SiO2 and BCB. It was found that BCB achieved better passivation efficiency compared to SiO2, resulting in a lower dark current for the PD covered with BCB. The second type of PD mesa, which has Q1.25\InGaAs protected by a thin InP layer, is only planarized with SiO2. The BCB planarization was not performed due to fabrication time constraints. It is unclear whether it can still achieve much better passivation efficiency compared to the SiO2 planarization method. An additional fabrication run may be necessary to clarify this.

A TIA-less (receiver-less) optical receiver is a good solution to reduce the power consumption of the optical receiver, which is important for mobile terminals. The design of a "TIA-less" optical receiver involves a zero-bias PD and a large load resistance. The sensitivity of a receiver-less design is expected to be comparable to that of a CMOS TIA configuration, provided the load impedance is carefully designed [82]. This design eliminates the need for a power-hungry electronic transimpedance amplifier typically used in conventional receivers. Connecting the PD to a large load resistance enables a significant voltage swing for the read-out circuit in an optical receiver. To ensure acceptable bandwidth and high-speed data rate transmission, the PD's capacitance must be sufficiently small in this configuration. However, a zero-bias PD with small capacitance in a TIA-less design has a small size, resulting in a low overload current [63]. Owing to this constraint, the demonstrated TIA-less configuration, based on a single PD, exhibits a decrease in optical saturation power below -10 dBm, leading to a restricted dynamic range for such receivers [162]. The limited optical saturation power is a challenge when using this TIA-less optical receiver in an OWC link. The array-based architecture is a good solution to solve the challenge of the single "TIA-less" optical receiver associated with low saturation current. In an array-based architecture, each unit of the array only receives a fraction of the total optical power that is illuminated on the receiver. Hence, an optimal design ensures that each unit is not saturated. The array-based architecture, with the series and parallel PD connection, is with the same capacitance value of the PD unit [35], which suggests that array-based architecture can also support the "TIA-less" mode. Developing a "TIA-less" unit is essential to realizing a "TIA-less" array-based receiver. The "TIA-less" CAO-Rx unit can be achieved by utilizing the designed layer stack of the PD presented in Chapter 7 and reducing the PD's size to achieve a capacitance value below 1 fF [63,82]. Based on these discussions, it is promising to investigate the CAO-Rx-array-based architecture with a TIA-less design.

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Acronyms

1D one-dimensional
2D two-dimensional
AC alternating current
ACP air coplanar probe
ADR angle-diversity receiver

Ag Silver

ANSI American National Standards Institute

APD avalanche photodetector

ASE amplified spontaneous emission

Au Gold

AWG array waveguide grating
BCB Benzocyclobutene
BER bit error ratio
BERT Bit-error-ratio tester

BS-ILC beam-steered infrared light communication

CAO-Rx cascaded aperture optical receiver

CCD charge-coupled device DBR Distributed Bragg Reflector

DC direct current

DDJ data-dependent jitter DFB laser distributed feedback laser

EB exabyte

EBL electron beam lithography

EDFA Erbium-doped optical fiber amplifier

EMI electromagnetic interference FDTD finite-difference time-domain

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FEC forward error correction

ff filling factor FoV field of view Ge Germanium

GSG ground-signal-ground ICP inductively coupled plasma

IEC International Electrotechnical Commission

IM intensity modulator

IM/DD intensity modulation direct detection

IMOS InP-membrane-on-Silicon ISI intersymbol interference

ITU International Telecommunication Union
JFET junction-gate field-effect transistor
LCA lightwave component analyzer

LED light-emitting diode LiFi Light-Fidelity LOS line-of-sight

MMI multi-mode interferometer

MOSFET metal-oxide-semiconductor field-effect transistor

MOCVD Metal-Organic Chemical Vapor Deposition

MR metal reflector

MRSGC metal-reflector-assisted surface grating coupler

MZM Mach-Zehnder modulator

Ni Nickel

OBPF optical bandpass filter O\E optical-to-electrical

OFDM Orthogonal Frequency Division Multiplexing

OOK on-off keying

OWC Optical Wireless Communication PAM-4 pulse amplitude modulation 4-level

PC polarization controller PCB printed circuit board

pc-LED phosphor-converted light-emitting diode

PDA photodetector array PD photodetector

PECVD plasma-enhanced chemical vapor deposition

PIC photonic integrated circuit

Rx receiver

SEM scanning electron microscope

SGC surface grating coupler SMF single-mode fiber SNR signal-to-noise ratio

SOA semiconductor optical amplifiers

SSC spot size converter TE transverse electric

Ti Titanium

TIA transimpedance amplifier
TLS tunable laser source
TM transverse magnetic

Tx transmitter

UTC-PD uni-traveling-carrier photodetector

UV ultraviolet

VLC visible light communication
WDM Wavelength Division Multiplexing
WGPD high-speed waveguide photodetector

WiFi Wireless Fidelity

Acknowledgments

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List of Publications

YU LEI has the following publications:

Journal papers

- Lei, Y., Yan, X., Li, C., Huang, J., Zhang X., Jiao, Y., Yao, W., Cao, Z. & Koonen, T. Monolithic Integrated Optical Receiver Cascaded with Metal Reflector-Assisted Grating Coupler. *IEEE Photonics Technology Letters*. **35**, 373-376 (2023)
- Lei, Y., Yan, X., Li, C., Bente, E., Yao, W., Cao, Z. & Koonen, T. Monolithic Integrated Two-Stage Cascaded SOA-PIN Receiver for High-Speed Optical Wireless Communication. *Optics Letters*. 47, 2578-2581 (2022)
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154 List of Publications

• Yue, G., Lei, Y., Die, J., Jia, H. & Chen, H. Fabrication of 4-Inch Nano Patterned Wafer with High Uniformity by Laser Interference Lithography. *Chinese Physics Letters*. **35**, 054207 (2018)

Curriculum Vitae

Yu Lei was born June 20th 1993 in Huanggang, China. He received his bachelor degree in Inorganic Non-Metallic Materials Engineering from Wuhan University of Technology in Wuhan, China (2015), where he ranked 7th out of 72 graduating students. After completing his undergraduate studies, Yu Lei pursued his master degree in Physics of Institute, Chinese Academy of Sciences. During his time there, he conducted research on the fabrication of III-V semiconductors and developed a keen interest in semiconductor fabrication. He obtained his master's degree in 2018. Later, Yu Lei began working towards his Ph.D. in the Electro-Optical Communication group at the Technische Universiteit Eindhoven (Eindhoven University of Technology, TU/e) in 2018. His research focuses on developing advanced photonic integrated circuits for indoor optical wireless communication. The findings of his research are presented in this thesis.