Low Power and Small Area Mixed-Signal Circuits

Low Power and Small Area Mixed-Signal Circuits: ADCs, Temperature Sensors and Digital Interfaces

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This work was supported by the Dutch Research Council (NWO) under project 16594.

Cover design by Yuting Shen

Shen, Y.
Low Power and Small Area Mixed-Signal Circuits: ADCs, Temperature Sensors and Digital Interfaces
Proefschrift Technische Universiteit Eindhoven, 2023.
A catalogue record is available from the Eindhoven University of Technology Library
ISBN 978-90-386-5722-6

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PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr. S.K. Lenaerts, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op vrijdag 12 mei 2023 om 13:30 uur

door

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geboren te Zhejiang, China

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Contents

List of symbols and abbreviations

Symbol	Description	Unit
ADC	Analog-to-digital converter	
BER	Bit error rate	
BTL	Backplane transceiver logic	
BW	Bandwidth	Hz
CDS	Correlated double sampling	
CML	Current mode logic	
CMOS	Complementary metal-oxide-semiconductor	
DAC	Digital-to-analog converter	
DDNR	Data-driven noise reduction	
DEM	Dynamic element matching	
DNL	Differential non-linearity	LSB
DR	Dynamic range	
DWA	Data weighted averaging	
ECG	Electrocardiogram	
EEG	Electroencephalogram	
ENOB	Effective number of bits	bit
FoM	Figure of merit	
FOM_S	Schreier figure of merit	
FOM_W	Walden figure of merit	fJ/conv.step
FS	Digital full scale amplitude	
f_s	Sampling frequency	Hz
G_e	Gain error	
H.O.T	Higher order terms	
IC	Integrated circuits	
INL	Integral non-linearity	LSB
IoT	Internet-of-Things	
LSB	Least significant bit	
LVCMOS	Low-voltage CMOS	
LVDS	Low-voltage differential signals	
LVPECL	Low-voltage positive emitter-coupled logic	
MES	Mismatch error shaping	
MIM	Metal-insulator-metal	

Symbol	Description	Unit
MOM	Metal-oxide-metal	
MSB	Most significant bit	
OSR	Oversampling ratio	
PCB	Printed circuit board	
PVT	Process voltage and temperature	
RMS	Root mean square	
SAR	Successive-approximation-register	
SFDR	Spurious-free dynamic range	
SNDR	Signal to noise and distortion ratio	
SNR	Signal to noise ratio	
THD	Total harmonic distortion	
T&H	Track and hold	
V_{CM}	Common-mode voltage	V
WhB	Wheatstone bridge	

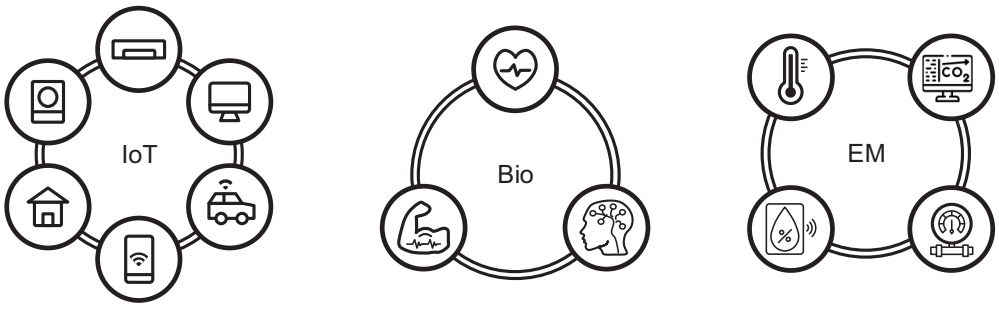
Chapter 1

Introduction

1.1 Background

With the development of internet, semiconductor devices are becoming increasingly more pervasive in our society over the last decades. Starting with the first transistor demonstrated by William Shockley, John Bardeen and Walter Brattain in 1947, the worldwide semiconductor industry revenue reached 300 billion dollars in 2012 and is expected to reach 676 billion dollars in 2022 [1], which is a doubling in the last 10 years. The demand for semiconductor products is expected to be even higher in the near future. In 2021, the semiconductor market size grew by more than 20% [1].

One key trend for applications of semiconductors is miniaturization. This is especially



(a) (b) (c)

Figure 1.1: Some semiconductor industry applications: IoT (a), biomedical sensing (b) and environmental monitoring (c).

true for Internet of Things (IoT), biomedical sensing and environmental monitoring systems (Fig. 1.1). For these applications, devices might need to be portable, wearable, or even implantable. Hence, a compact chip area is critical to achieve size reduction as well as cost reduction.

To align with this trend, the average power consumption of the circuity also needs to be low so that small batteries or energy harvesters can be used while maintaining sufficient operational time.

Thanks to the rapid development of technology in the past decades [2], the power consumption and chip size of integrated circuits (IC) have been significantly reduced. While the power consumption and chip size of digital circuits follow an exponentially decreasing trend thanks to the technology evolution according to Moore's law, the scaling of analog and mixed-signal circuits is limited by noise, matching, etc., resulting in both challenges and opportunities for innovation. Moreover, as the technology nodes are approaching the atomic scale, technology scaling is expected to be much slower or even come to an end, making circuit-level innovation more important.

1.2 Problem statement

As discussed above, power-efficiency and area-efficiency are two main design considerations for analog and mixed-signal circuits used in IoT, biomedical sensing and environmental monitoring systems.

Fig. 1.2 shows a simplified model of a typical signal digitalization chain, which consists of an analog front-end to acquire the signal, an analog to digital conversion block to digitalize the signal and a digital communication block for data transmission. The analog front-end usually contains an amplification block and a filtering block or it could simply be a sensing front-end such as a resistive bridge or a capacitive bridge. For analog to digital conversion, many analog-to-digital converter (ADC) architectures such as flash, successive-approximation-register (SAR) and sigma-delta converters have been proposed for different resolution and speed requirements. For

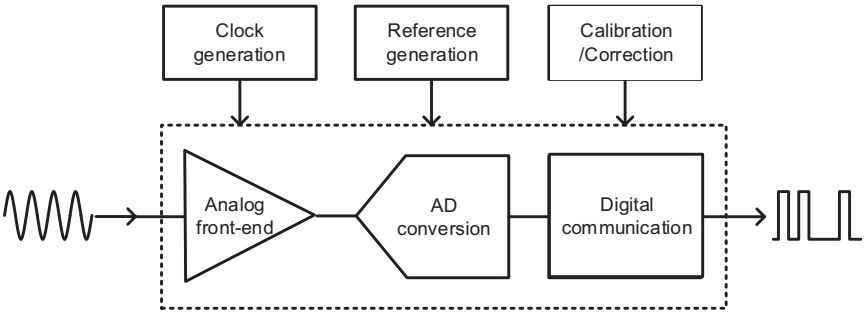


Figure 1.2: A typical signal digitalization chain.

digital communication, channels like copper wires, wireless and optical fibers are commonly used.

On top of this, other auxiliary circuits are essential to make the whole system functional, for example, clock generation and reference generation. For some systems, extra digital correction or calibration is needed to counteract circuit imperfections.

From an analog signal to a digital signal, a continuous signal becomes discrete in both time and amplitude. Equation (1.1) and (1.2) show two figures of merit (FoM) for AD conversion [3, 4]. Equation (1.3) shows the FoM for temperature sensing [5]. Equation (1.4) and (1.5) show the channel capacity and signal to noise ratio (SNR) per bit for digital communication, respectively [6].

$$FOM_W = Power/(2^{ENOB} \times 2 \times BW) \tag{1.1}$$

$$FOM_S = SNDR + 10 \times \log 10(BW/Power) \tag{1.2}$$

$$FoM = Energy/Conversion \cdot (Resolution)^2 \tag{1.3}$$

$$C = BW \times (1 + SNR) \tag{1.4}$$

$$SNR_b = E_b/N_0 = Energy\,per\,bit/Noise\,density \tag{1.5}$$

As (1.1), (1.2), (1.3), (1.4) and (1.5) indicate (directly or indirectly), the consumed power for a circuit is related to its bandwidth (BW) and signal to noise and distortion ratio (SNDR). In low-power applications, it is desirable to make the power consumption proportional to BW, though at very low absolute BW the leakage can become a dominant factor. If distortion is the dominant factor limiting the performance, calibration or correction techniques need to be implemented and this should be done in an area-efficient and power-efficient way. On the other hand, if noise is the limiting factor, it cannot be improved with calibration techniques, but better architectures [7, 8] and circuits with a better noise-efficiency (e.g. inverter-based amplifier [9–11]) can pay off.

In the context of the above problems, this thesis focuses on three aspects.

- Efficient AD conversion

ADCs are the core of the signal digitalization chain. Among various ADC architectures, SAR ADCs are the most popular ADC choice for the mentioned applications due to their high efficiency and simple architecture. As analyzed in [12], noise, mismatch and physical size are 3 main limitations for a SAR ADC. Depending on the target resolution, different factors will dominate the power consumption of the overall design. For high resolution SAR ADCs, the main constraint is mismatch. For low to medium resolution ADCs, the main constraint is physical size. This is because the digital-to-analog converter (DAC) capacitors are physically limited to a minimum value due to technology limitations.

- Efficient correction techniques for temperature sensors

  A temperature sensor is chosen as an example analog front-end since temperature is one of the most commonly monitored parameters. One design challenge for temperature sensors is that they are usually sensitive to random mismatch and process variations, leading to offset, gain errors and distortion [13, 14]. Hence, correction needs to be done for each chip. The key challenge here is to implement efficient correction techniques.

- Efficient digital communication

  Nowadays, many electronic devices contain multiple different chips to realize complex functionalities or multiple channels to obtain signals with higher quality. Fig. 1.3 shows an electroencephalogram (EEG) headset where multiple printed circuit boards (PCBs) are connected with each other in an electronic system. In these systems, efficient chip-to-chip digital communication is necessary. Most existing wireline standards (low-voltage differential signaling (LVDS), current mode logic (CML), etc.) require constant power consumption and their efficiency is only optimized for high-speed digital communication. For low-speed (< 100 Mb/s) digital communication, the Low-Voltage CMOS (LVCMOS) standard whose energy is proportional to speed is more efficient. Still, the transmitted signal amplitude for LVCMOS is far above the channel noise level if it is used on a PCB level, which indicates that the transmitted amplitude as well as the power consumption can be further reduced.

1.3 Aim of the thesis

This thesis aims to push the boundary of the power and area costs for several exemplary analog and mixed-signal circuits. Three circuit blocks including ADCs, on-chip calibration/correction techniques (for temperature sensors) and digital communication interfaces are studied. The main objectives are summarized as follows:

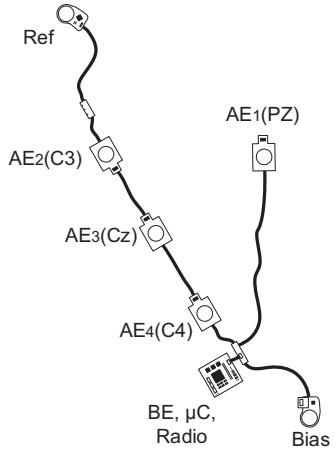


Figure 1.3: Internal electronics of an EEG headset [15].

- Literature study on the power consumption and chip size of ADCs, correction techniques for temperature sensors and wired digital communication interfaces.
- Develop new techniques to enable efficient AD conversion, efficient temperature sensor correction and efficient digital communication.
- Validate experimentally the proposed techniques with prototype IC implementations.

1.4 Methods

To achieve the goal, several general ideas are summarized here below.

One general approach to save power is to design all-dynamic circuits. Circuits can be shut down when they are not needed, which is particularly useful when the intrinsic circuit speed is higher than the application requirement. Besides, integrated circuit real estate that is not fully used, and time intervals when some circuits are idle can be taken advantage of as much as possible to minimize the area overhead:

- Use existing hardware in idle timing phases

  For example, a SAR ADC usually consists of 4 blocks (track and hold, DAC, comparator and logic) and has 3 operating phases (tracking, conversion and reset). DACs are used to generate reference levels during SAR conversion phase. During tracking phase and reset phase, they can be utilized to realize other functions, for example, mismatch error shaping, input range extension, gain, offset, nonlinearity correction and so on. By re-using hardware for other functions during spare timing phases, more functionality can be achieved with the same chip area.

- Exploit unused IC real estate

  For instance, capacitors can be placed on top of active circuits to maximize the area utilization.

1.5 Scope of the thesis

Some limitations on the scope of the thesis are listed here below:

- The research topics of this thesis are limited to SAR ADCs, on-chip correction techniques (for temperature sensors) and wired digital communication interfaces. Other circuit blocks, such as clock generation and reference voltage generation, are also essential but they are not in the scope of this thesis.
- This thesis is focused on IoT, biomedical and environmental sensing applications, where moderate-to-high resolution ($<$ 16-bit effective number of bits (ENOB) or $>$ 0.5 °C temperature inaccuracy), moderate speed ($<$ 100 MS/s), low-power and small area circuits are required. High-precision temperature sensors and high-speed wireline/wireless communication are not in the scope of this thesis.
- All ICs in this thesis are implemented in a standard 65nm complementary metal-oxide-semiconductor (CMOS) technology.

1.6 Own contributions

New techniques and architectures have been proposed to minimize the power consumption and chip area for the target 3 circuit blocks. The contribution can be summarized as follows:

- A pre-comparison technique which, combined with mismatch error shaping (MES), can shape the DAC mismatch error without input range loss. A pre-comparison technique based on conventional top-plate sampling is proposed first. Secondly, a pre-comparison technique based on flying-capacitor sampling is proposed, which has the advantage that it avoids prediction errors.
- Smart DAC switching techniques which, combined with the above pre-comparison techniques, can increase the input range of a SAR ADC by 1.5× and 2×, respectively. As a result, a higher SNR can be achieved resulting in better power and area efficiency.

- On-chip gain, offset and non-linearity correction techniques for a dynamic resistive temperature sensor front-end. By implementing these corrections in the analog domain, and co-integrating these with the ADC, they result in power and area efficient correction.
- A simplex and a full duplex digital communication interface with data rate and load capacitance adaptability and high energy efficiency.

To verify the proposed ideas, 7 prototypes have been implemented and characterized.

- Implementation and characterization of an oversampled SAR ADC with mismatch error shaping and pre-comparison techniques [16] which achieves 103 dB spurious-free dynamic range (SFDR) with a Schreier figure of merit (FoM_S) of 180.6 dB. By applying pre-comparison and MES, DAC mismatch errors can be shaped without input range loss. Hence, small DAC capacitors can be used, which results in effective reduction of both power and area.
- Implementation and characterization of an oversampled SAR ADC with flying-capacitor based sampling and input range compensation [17] which achieves 80.4 dB SNDR and a FoM_S of 178.3 dB. Compared to the previous SAR ADC [16], prediction errors are avoided [17].
- Implementation and characterization of a 10-bit SAR ADC with 1.5× input range which achieves 9.74 ENOB with a Walden figure of merit (FoM_w) of 2.2 fJ/conv.step [18]. Thanks to the enhanced input range, the absolute noise requirement for the comparator is relaxed and the usable supply voltage can be lower. Also, DAC area is relatively low as it needs less resolution than the ADC.
- Implementation and characterization of a SAR ADC with 2× equivalent input range which achieves 10.04 ENOB with a FoM_w of 3.28 fJ/conv.step [19]. Compared to the previous work [18], the input range of the SAR ADC is further enhanced and potential prediction errors are avoided.
- Implementation and characterization of a dynamic resistive temperature sensor front-end with on-chip gain and offset correction [20]. It achieves a 6.3% gain correction range with a step of 0.8% and a full code range offset correction with a step of 0.5 least significant bits (LSB). The sensor consumes 2.74 pJ per conversion and occupies an area of 0.0018 mm^2 including the extra correction techniques. It has a root mean square (RMS) resolution of 0.47 K, leading to a FoM of 0.6 $\text{pJ}\cdot\text{K}^2$.
- Implementation and characterization of a dynamic resistive temperature sensor front-end with on-chip gain, offset and non-linearity correction [21]. The temperature sensor consumes 2.98 pJ/conversion with an area of 0.0023 mm^2 including all the correction techniques and achieves +0.7/-0.6 °C inaccuracy.

- Implementation and characterization of a simplex interface and a full duplex interface for wired digital communication [22] which achieve an energy consumption of 0.38 pJ/b and 1.2 pJ/b respectively (with 19 pF load) at a bit error rate (BER) of $< 5 \cdot 10^{-12}$. Thanks to the all dynamic architecture, the proposed interfaces allow efficient power scaling as a function of speed and load capacitance.

1.7 Outline of the thesis

This thesis includes 9 chapters, as shown in Fig. 1.4.

After the first introductory chapter, area reduction and power reduction techniques for high-resolution ADCs and low-to-medium resolution ADCs will be introduced in Chapter 2 and 3, and Chapter 4 and 5, respectively.

Chapter 2 will introduce an oversampled SAR ADC with mismatch error shaping and pre-comparison techniques. Chapter 3 will extend this concept to an ADC with flying capacitor based sampling.

Chapter 4 will introduce a 10-bit SAR ADC with 1.5× input range and Chapter 5 will introduce a SAR ADC with an improved input range of 2×.

Chapter 6 and 7 will introduce on-chip correction techniques for temperature sensors. Chapter 6 will introduce on-chip gain and offset correction techniques for a dynamic resistive temperature sensor. As an extension, various non-linearity correction techniques will be discussed in Chapter 7.

Chapter 8 will introduce a simplex interface and a full duplex interface for digital communication.

Finally, Chapter 9 will draw conclusions and discuss opportunities for future work.

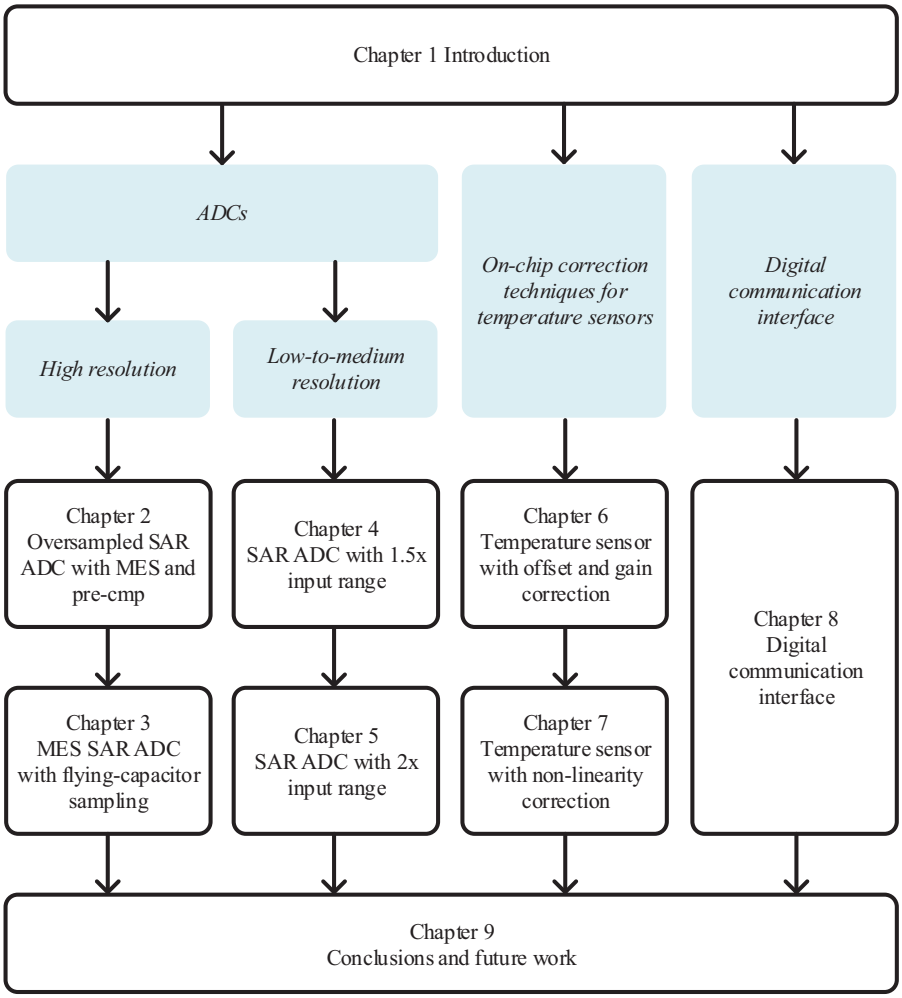


Figure 1.4: Thesis outline.

Chapter 2

SAR ADC with MES and pre-comparison

In this chapter, power-efficiency and area-efficiency for high-resolution ADCs are discussed. The DAC is one of the main contributors to power consumption and area. For high-resolution ADCs, the DAC capacitance is usually limited by mismatch. In this chapter, a 14-bit oversampled SAR ADC with mismatch error shaping (MES) and pre-comparison techniques is presented. MES is used to alleviate the impact of DAC mismatch. A pre-comparison technique is proposed to solve the overrange problem caused by MES. With MES and pre-comparison, the DAC mismatch error can be first-order shaped, while a full input range is maintained. Besides, data-driven noise reduction and chopping techniques are combined to reduce the comparator noise efficiently.

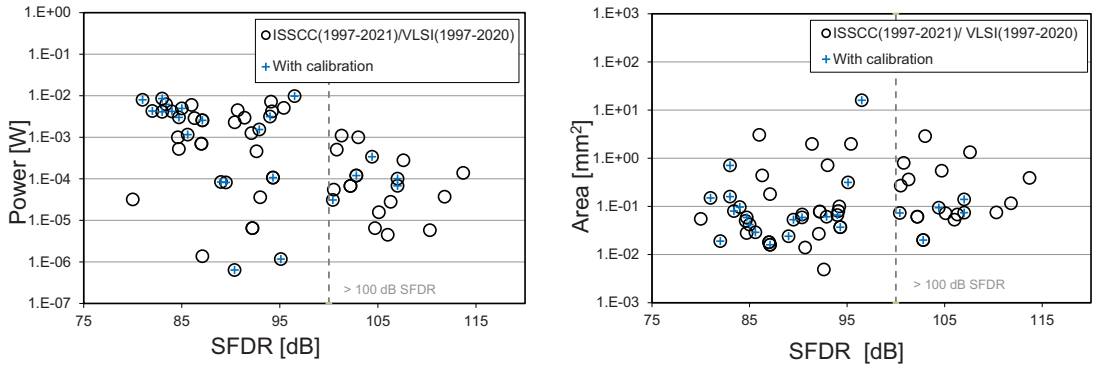
The content of this chapter has been published in [16] and [23].

2.1 Introduction

With the development of electronic devices, highly-linear ADCs are essential and are becoming more and more popular for IoT, bio-recording and environmental sensing applications. For example, a 13-bit ADC is used for fetal electrocardiogram (ECG) monitoring [24]. If better tolerance against motion artifacts is desired, then ADCs with even higher resolution are required [25]. In the applications mentioned above, the ADCs should work with a low absolute power consumption. Moreover, they should be inexpensive, and thus should minimize chip area, use a cost-effective technology node, and be calibration-free. While the power-efficiency and area-efficiency are already optimized a lot for low-resolution ADCs, it is still challenging to reduce the power and area cost for high-resolution ADCs. As shown in Fig. 2.1, to achieve above 100-dB SFDR, power consumption above 4 μW and an area larger than 0.05 mm^2 are still needed for state-of-the-art ADCs without off-chip DAC mismatch calibration.

As discussed in Section 1.2, for high-resolution SAR ADCs, the DAC is one of the dominant contributors for both power consumption and area. Theoretically, the switching power for a capacitive DAC is proportional to the capacitor value, which is ultimately determined by the kT/C noise requirements. However, in practical implementations, capacitors suffer from mismatch, which causes non-linearity. In many cases, especially for high-resolution ADCs, the used capacitor value as well as the DAC power consumption are not limited by noise, but by mismatch requirements [12].

To address this problem, many DAC mismatch error mitigation techniques have been developed. One solution is to use calibration techniques [11, 27, 28]. Sufficient calibration accuracy is needed to enable high resolution, which complicates the design and increases cost. Dithering can also be used to alleviate DAC mismatch [29]. It can flatten the harmonics caused by DAC mismatch and is easy to implement. However, applying dithering reduces the input range of the ADC and till now this technique has not been able to provide an SFDR better than 100 dB. Another method is based on random element selection and rotation, for example, DEM [30], DWA [31, 32],



(a) (b)

Figure 2.1: Benchmark of state-of-the-art designs: (a) Power vs SFDR (b) Area vs SFDR data from [26].

A-DWA [33], bi-DWA [34], vector based-DWA [35] and so on. Depending on the implementation, DAC mismatch errors can be turned to white noise or shaped with different orders. However, the circuit implementation for this type of solution is usually relatively complex. Also, these techniques are typically applied to unary cells, causing an exponential increase of the DAC elements with resolution, which makes them unpractical for DACs beyond 5-bit. One method to solve this problem is to use segmentation [36, 37]. By applying DWA to segmented parts, the total number of used elements is reduced and the logic is simplified. However, extra redundancy is needed to avoid distortions according to [36]. Besides, extra thermometer-to-binary decoders might be needed.

Recently, [38] proposed a MES technique which is based on error feedback and shaping. It can be applied to binary cells and thus is suitable for high resolution DACs. One disadvantage of this technique is that it suffers from input range loss. To realize MES, a feedback of the previous LSB value is required, which occupies part of the input range. To solve this issue, [38] applies DWA to the 3-bit MSBs and applies MES to the remaining LSBs. Then, the input range is reduced by $\frac{1}{8}$ instead of $\frac{1}{2}$. In [39] and [40], a 3-level digital prediction method is proposed to recover the signal range. By combining DWA with digital prediction, the input range can be fully recovered if a sufficient oversampling ratio is chosen.

This chapter discusses an analog pre-comparison technique, which is conceptually a prediction technique similar to the ones described in [39] and [40], but it is implemented in the analog domain, uses only 2 level-prediction, and therefore does not need DWA. Overall, the proposed architecture remains simple while it can efficiently shape the DAC mismatch errors and maintain the full input range.

A 14-bit oversampled SAR ADC is implemented to verify the idea. As a result, the prototype achieves 84.5-dB SNDR and 103-dB SFDR with a calibration-free and power-efficient architecture in a small chip area of 0.033 mm^2.

This chapter is organized as follows: Section 2.2 reviews the principle of mismatch error shaping. Section 2.3 describes the proposed pre-comparison technique applied to the MES. Section 2.4 presents the circuit implementation details. Measured results are presented in Section 2.5, and conclusions are drawn in Section 2.6.

2.2 Review of the MES technique

Fig. 2.2 shows the basic architecture and working principle of a SAR ADC. Firstly, a track and hold (T&H) circuit is used to track and hold the analog input V_{in}(n) for the n^{th} sample. Then, a DAC generates reference voltages (DAC_{MSB}(n), DAC_{LSB}(n)) depending on the bit decisions from a comparator. They will be subtracted from V_{in}(n). After obtaining all the bit decisions, the signal will be reconstructed in the

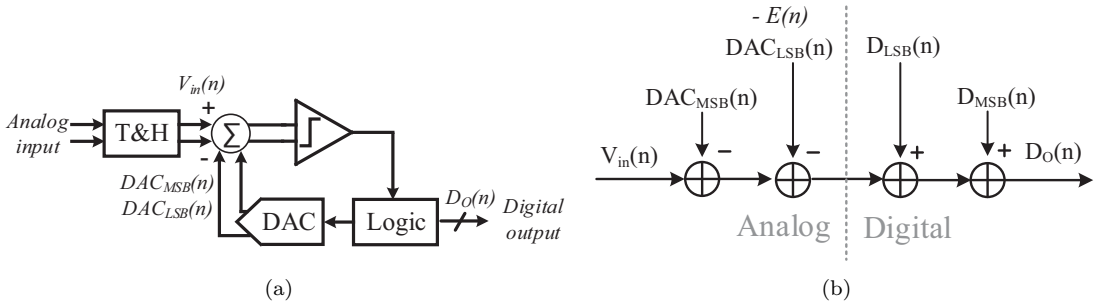


Figure 2.2: SAR ADC architecture (a) and principle (b).

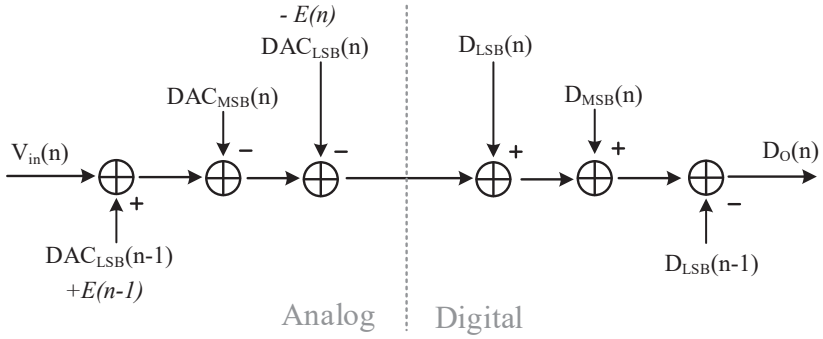


Figure 2.3: Principle of MES.

digital domain by combining the digital output (D_{MSB}(n), D_{LSB}(n)).

Due to imperfections in fabrication, DAC elements have mismatch. Mismatch is a relative error. Taking the MSB value as a reference, this results in LSB conversion errors E(n). It will also be subtracted from V_{in}(n), along with DAC_{LSB}(n), but it is not compensated in the digital reconstruction (unless digital calibration is used). As a result, the existence of E(n) leads to distortion. To address this issue, MES is proposed [38]. Its basic principle is shown in Fig. 2.3. Before the normal SAR conversion, the previous DAC LSB value DAC_{LSB}(n-1) as well as the related error E(n-1) are replicated and added to the n^{th} cycle. DAC_{LSB}(n-1) will be subtracted in the digital domain afterwards. The digital output now can be calculated as:

$$D_O(n) = V_{in}(n) + E(n-1) - E(n) \tag{2.1}$$

It can be seen that this operation results in a first-order high-pass filter function for E(n). With oversampling, DAC mismatch errors can thus be shaped out of band and then filtered out.

Fig. 2.4 shows the DAC operation for a normal SAR ADC and a SAR ADC with MES. For a normal SAR ADC, during the sampling phase, the DAC is reset to mid-scale and there is no memory from the previous sample. For a SAR ADC with MES, only the MSB of the DAC is reset while the LSBs of the DAC remain at the previous

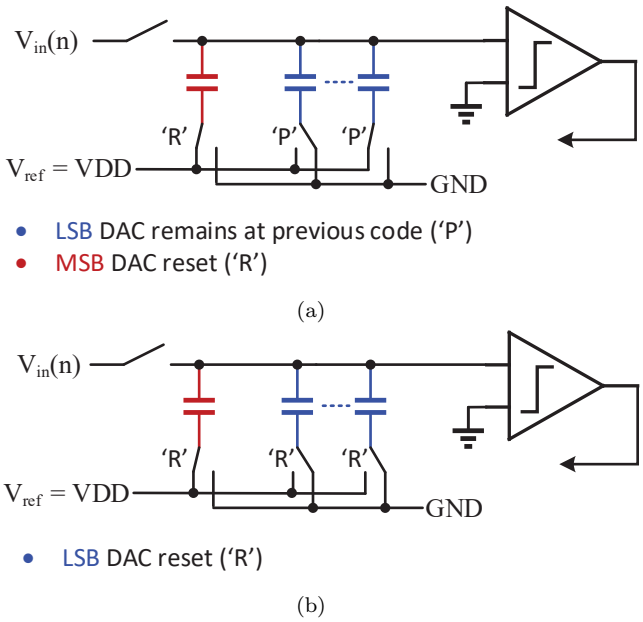


Figure 2.4: DAC operation for SAR ADCs with MES. (a) sampling phase (b) reset phase. For simplicity, only half of the differential topology is shown.

code ('P') during the sampling phase. As shown in Fig. 2.4, after the sampling phase, an additional reset phase is introduced before the SAR conversion starts. During this reset phase, the LSBs of the DAC are reset to mid-scale (code 'R'), which effectively feeds back the LSB value of the previous sample as well as its mismatch error.

The feedback of the previous LSB value occupies half of the ADC range, and thus only the other half remains available for the actual input signal. This reduces the maximum achievable SNR by 6 dB. Therefore, it is preferable to restore the full input range. In [39], this was done by applying a 3-level digital prediction technique. Here, a pre-comparison technique is proposed, which can be seen as a 2-level analog prediction method.

2.3 Proposed pre-comparison with MES

2.3.1 Concept

To solve the input range loss issue brought by MES, a pre-comparison technique is proposed. The principle is to generate a negative input to compensate for the input range loss (Fig. 2.5). With the architecture given in Fig. 2.4, the input range is [-V_{ref}, V_{ref}] because of the differential topology. Due to the feedback of the LSB value, which is located in the range of [-$\frac{1}{2}V_{ref}$, $\frac{1}{2}V_{ref}$], the DAC voltage at the comparator

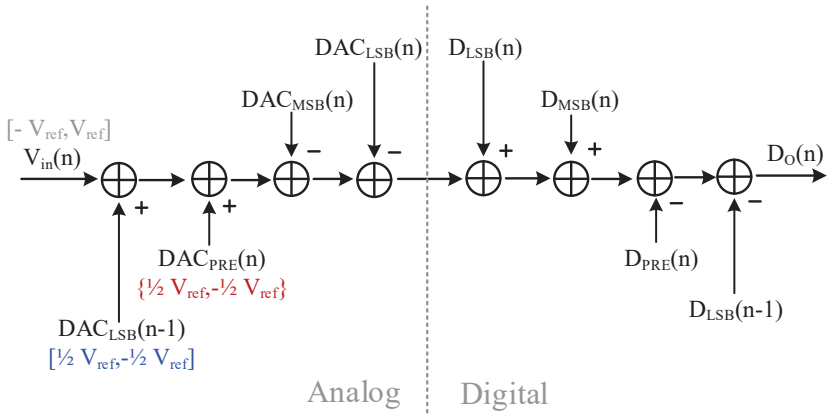


Figure 2.5: Principle of pre-comparison.

input is increased to $[-\frac{3}{2}V_{ref}, \frac{3}{2}V_{ref}]$ before SAR conversion, which is out of the ADC conversion range. To shift it back to the nominal conversion range, a compensation voltage needs to be generated.

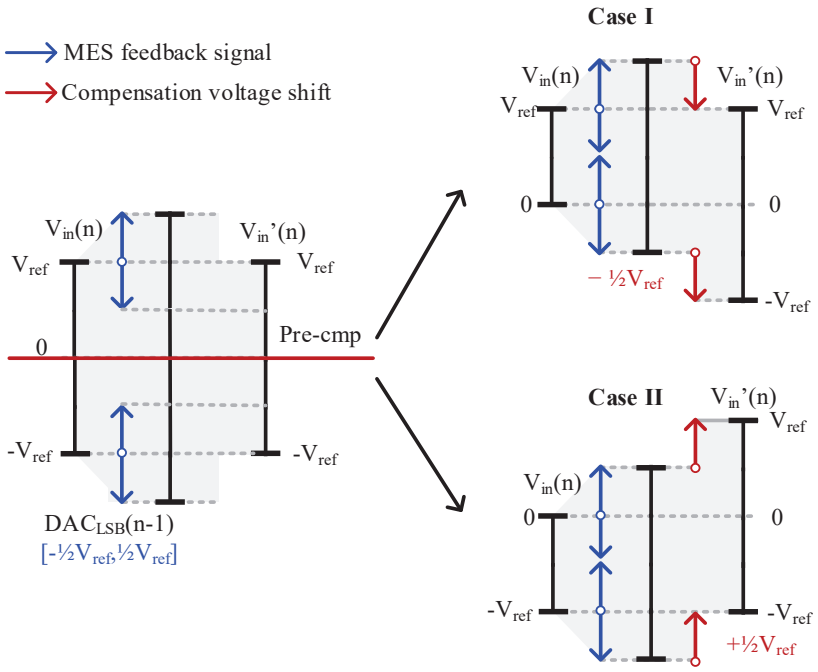


Figure 2.6: Concept of pre-comparison.

Fig. 2.6 shows the concept of pre-comparison. An additional comparison is performed to detect the polarity of the signal before the sampling moment. If V_{in} is positive (case I), an additional $-\frac{1}{2}V_{ref}$ voltage shift is created to ensure that V_{in} fits into the ADC conversion range once MES feedback takes place. Correspondingly, if V_{in} is negative (case II), a voltage shift of $+\frac{1}{2}V_{ref}$ is created. As can be seen, the direction of the compensation depends on the pre-comparison result. In this way, it is ensured that the signal to be quantized is always within the nominal ADC range.

2.3.2 Operation

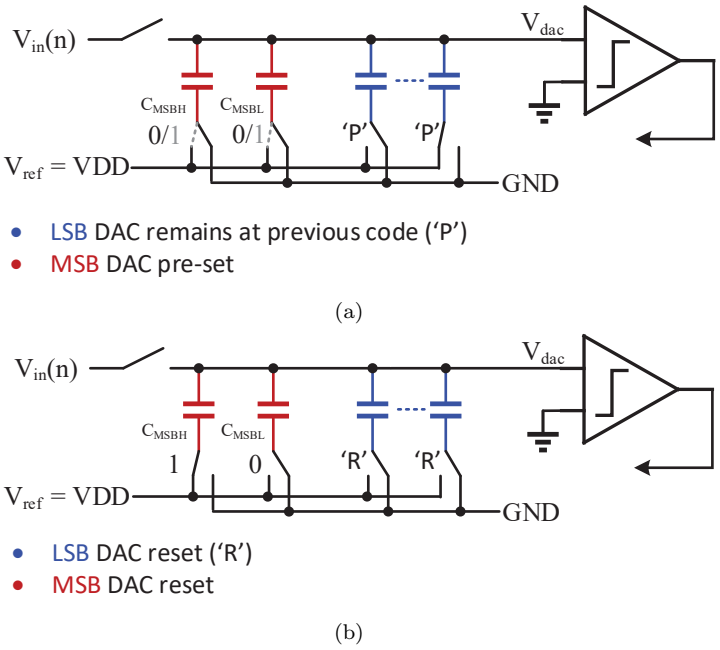


Figure 2.7: Circuit level operation for SAR ADCs with pre-comparison and MES. (a) pre-comparison phase (b) reset phase.

Fig. 2.7 shows the circuit level operation of the proposed technique. A single-ended diagram is shown for simplicity. The MSB capacitor is split into two half capacitors, C_{MSBH} and C_{MSBL}. An additional comparison using the regular comparator of the SAR ADC is performed before the sampling moment. Depending on the pre-comparison result, both the bottom plates of C_{MSBH} and C_{MSBL} will be either connected to V_{ref} (if V_{in} is in the range of [0, V_{ref}]) or ground (if V_{in} is in the range of [-V_{ref}, 0]. After that, sampling of V_{in}(n) takes place, and then, a reset phase follows. During the reset phase, the bottom plate of C_{MSBH} will always be reset to V_{ref} while the bottom plate of C_{MSBL} will always be reset to ground. This operation will cause a -$\frac{1}{2}V_{ref}$ shift for V_{dac} if V_{in} is positive or a $\frac{1}{2}V_{ref}$ shift for V_{dac} if V_{in} is negative. The MES operation will cause a voltage shift between -$\frac{1}{2}V_{ref}$ and +$\frac{1}{2}V_{ref}$ during the same reset phase. Thanks to this pre-comparison technique, the signal to be quantized is inside the nominal range, and thus no signal range is lost due to the MES feedback. After the reset phase, the MSB and LSBs are at mid-scale, and a regular SAR conversion can be performed.

2.3.3 Behavioral model simulations

Fig. 2.8 shows the simulated output spectrum of a behavioral model in MATLAB, where a 14-bit SAR ADC with an OSR of 16 is used as an example. Only quantization

noise and DAC mismatch errors are included. The standard deviation of the mismatch is set to 6% for each unit capacitor. This is relatively large because very small unit capacitors are targeted in this design, to save power and area. It can be seen that with both pre-comparison and MES enabled, the DAC mismatch error can be first-order shaped with a full range input. The simulated SNDR versus different input amplitudes is shown in Fig. 2.9. It proves that the maximum input amplitude available is increased from -6 dBFS to 0 dBFS by using the pre-comparison technique.

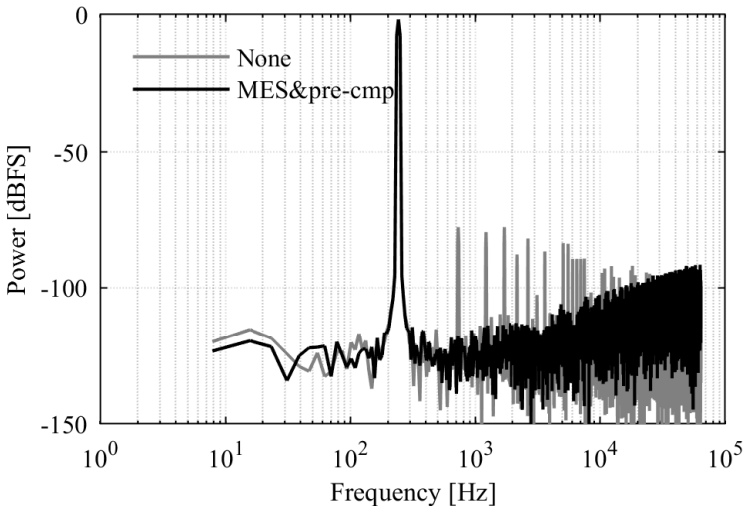


Figure 2.8: Simulated output spectrum without and with MES and pre-comparison.

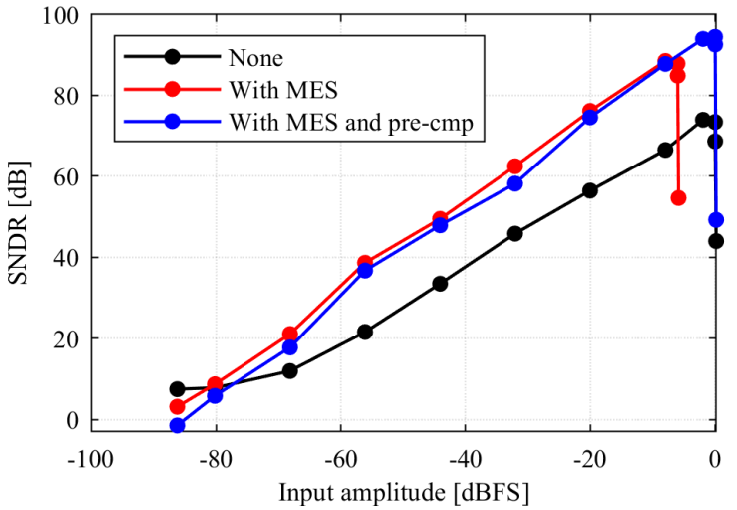


Figure 2.9: Simulated SNDR versus input amplitude.

Fig. 2.10 shows the simulated SNDR versus the number of DAC bits N and with various OSRs (4× or 16×). Each point is obtained by averaging the results from 100 Monte Carlo simulations. The black solid lines show that without mismatch, a higher OSR improves the SNDR. With 6% capacitor mismatch but without MES, the ADC performance is limited by distortion caused by DAC mismatch (red dashed lines),

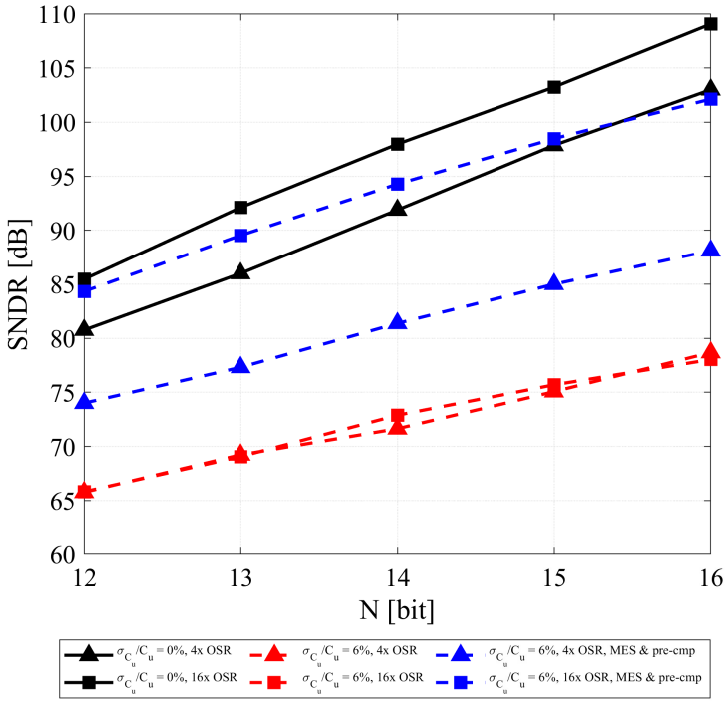
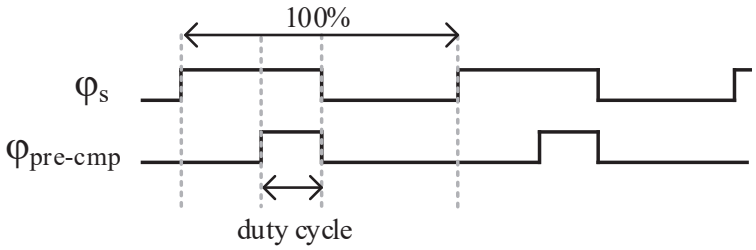


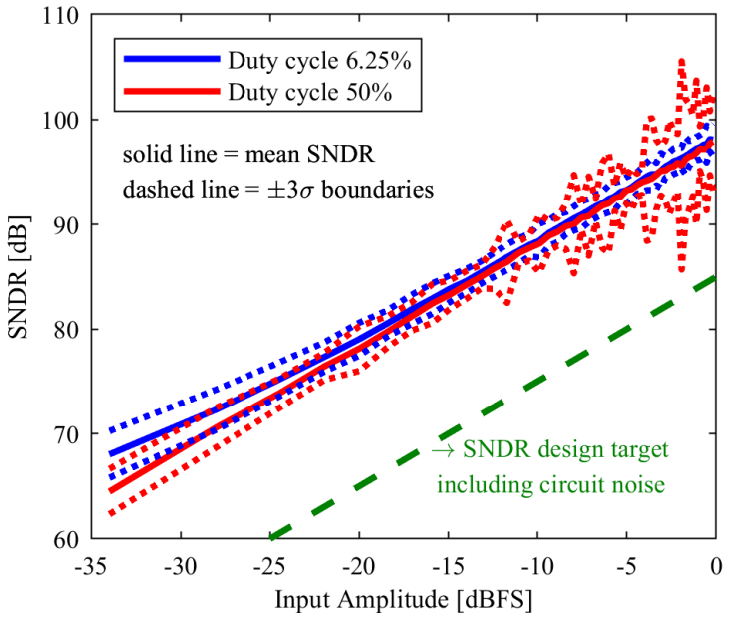
Figure 2.10: Simulated SNDR versus the number of DAC bits with various OSRs. Here, σ_{C_u}/C_u is the standard deviation of the unit capacitance divided by the unit capacitance, which represents for the capacitor mismatch level.

and increasing OSR does not help. With MES and pre-comparison, the distortion is shaped to higher frequencies and the in-band linearity is significantly improved. The simulated SNDR can be improved by 8-10 dB with an OSR of 4, and by 16-24 dB with an OSR of 16, respectively. For ADCs with mismatch and MES, there is still some SNDR loss compared to ADCs with ideal DACs, because the MES can only shape the DAC mismatch errors but not remove them. The SNDR loss depends on the mismatch level, the number of bits and the OSR of the system. Sufficient OSR or higher order error shaping is required to minimize the performance loss caused by DAC mismatch. In the example of Fig. 2.10, an OSR of at least 16 is required to achieve sufficient error shaping and recover from most of the mismatch-related losses. In this design, targeting at 80-90 dB SNDR, an OSR of 16 and a 14-bit DAC are chosen to ensure that DAC mismatch will not limit the performance.

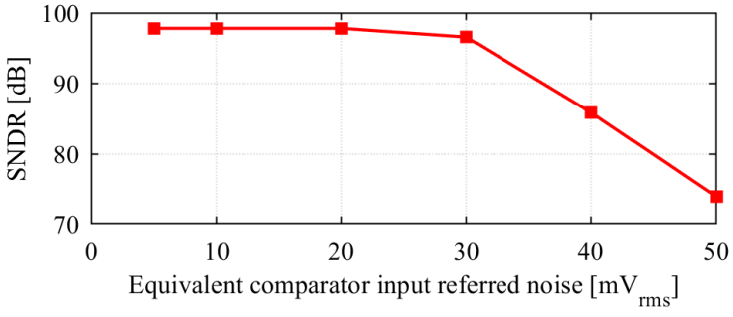
Note that besides capacitor mismatch within the LSB array, which is shaped by MES, there are potentially 3 other mismatch problems: first, there can be mismatch between the LSB array and the MSB capacitor. However, this is taken care of by the error feedback loop, as MES inherently shapes the LSB mismatch errors with respect to the actual MSB value as a reference. This is confirmed by the measurements in Section 2.5, where the measured INL shows a large MSB mismatch relative to the LSBs, which is nonetheless shaped effectively when MES is enabled. Secondly, in theory there can be mismatch between the MSB step-size and the pre-comparison compensation steps.



(a)



(b)



(c)

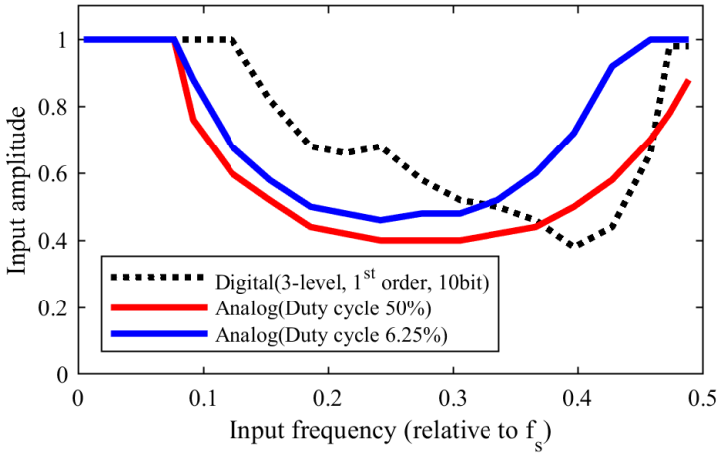
Figure 2.11: Timing diagram of sampling and pre-comparison phases (a), simulated SNDR versus signal amplitude, where each point is simulated over 100 frequencies (b), and simulated SNDR with comparator noise (c).

Fortunately, since both steps are generated by the same physical capacitors, this mismatch does not occur. Thirdly, mismatch within the capacitor array creating the pre-compensation steps could happen. Since this work only uses 2-level prediction, the pre-compensation is inherently linear as it only has 2 levels. This is different from 3-level compensation, where the 3 levels may form a non-linear function that may require DWA, calibration, multiple reference voltages, or other means to guarantee linearity.

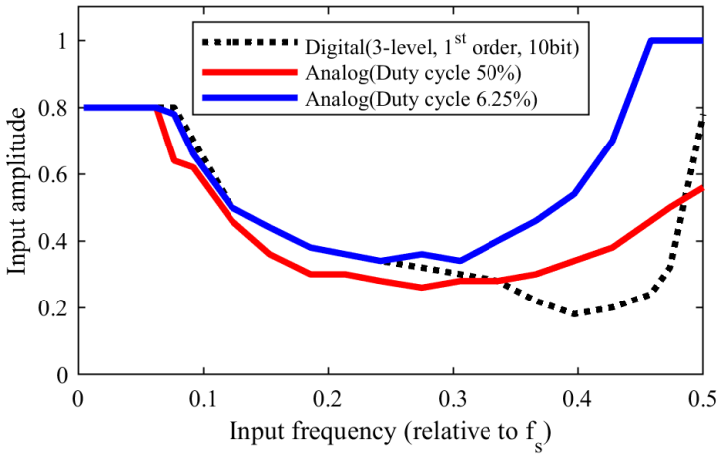
Fig. 2.11(a) shows the relative timing of pre-comparison versus sampling: the pre-comparison takes place on the rising edge of $\varphi_{pre-cmp}$, and sampling takes place on the falling edge of φ_s. The pre-comparison occurs before the sampling moment and the input signal can still change within this time. Thus, there is a chance that the pre-comparison makes a mistake when the input signal crosses the comparator's threshold voltage between the pre-comparison moment and the sampling moment. However, even when the pre-comparison makes a mistake, this does not often lead to overrange of the converter, as it also depends on the specific value of the previous LSB value that is fed back by the MES algorithm. With sufficient oversampling, causing correlation between the previous LSB value and the present sample, the probability of overrange can be minimized such that its impact on overall SNDR and SFDR becomes minimal. Fig. 2.11(b) shows the simulated SNDR as function of the input signal amplitude, when an OSR of 16x is used, and the duty-cycle of $\varphi_{pre-cmp}$ is either 6.25% or 50%. Note that 6.25% is the minimal duty-cycle that gives enough time for pre-comparison and DAC settling (in our implementation), while 50% is the maximum value as it equals the duration of φ_s. For each amplitude, 100 different signal frequencies spread over the signal bandwidth (0 to $f_s/(2 \times OSR)$) are simulated and the statistical spread on SNDR is shown. With a low duty-cycle of 6.25%, few mistakes are made, and SNDR is consistent. With 50% duty-cycle, there is an increased probability of overrange causing more variation in the SNDR, but the average SNDR is still similar as before.

Overall, a short duty cycle is beneficial to reduce the prediction error probability, and thus improve the SNDR. However, it leads to a significant impact on the requirement of the input driver for ADCs with active input drivers. For instance, a duty-cycle reduction from 50% to 6.25% may imply an 8× higher peak current from the driver. Therefore, in case of active drivers, the duty cycle should be chosen as a trade-off between the input driver requirements versus the MES performance. On the other hand, some ADCs are used to passively read out a resistive sensor bridge or capacitive sensor bridge. In case a duty-cycled resistive sensor bridge is used [41], or a passive capacitive sensor bridge [42], the energy consumption of the frontend is only affected by the load capacitance from the ADC while the duty cycle does not matter as long as the RC constant of the sensor/ADC combination satisfies the tracking time, and thus a minimal duty-cycle could be selected. For the presented ADC, at 128 kS/s with 6.25% duty-cycle, the sensor should have an output-resistance below 20 kΩ to satisfy the timing conditions with sufficient accuracy.

Comparator noise could also result in mistakes in the pre-comparison. However, this



(a)



(b)

Figure 2.12: Simulated input amplitude versus input frequency without interference (a) and with interference (b).

probability is very low as it can only happen if V_{in} is near the decision threshold. As shown in Fig. 2.11(c), the simulated SNDR is insensitive to the comparator noise (applied to the pre-comparison only), and thus a low-power comparator can be used.

Depending on the exact application, out-of-band signals or interferences may exist, in which case the prediction error probability increases. Similar to the study in [40], Fig. 2.12 shows the simulated input amplitude versus input frequency that can be supported with 2-level analog or 3-level 1^{st} order digital prediction, based on a 32768-point transient simulation. Without interference (Fig. 2.12(a)), analog prediction degrades earlier, which implies that a higher OSR is required. On the other hand, when a 20% full-scale interference at 13103/32768 f_s is assumed (Fig. 2.12(b)), analog prediction sometimes performs better than digital prediction. This is because the analog prediction precedes the sampling moment by 6.25% to 50% of the clock period, while digital prediction is 100% earlier, as it depends on the previous sample. Therefore, analog prediction can give a better prediction of the input signal at the

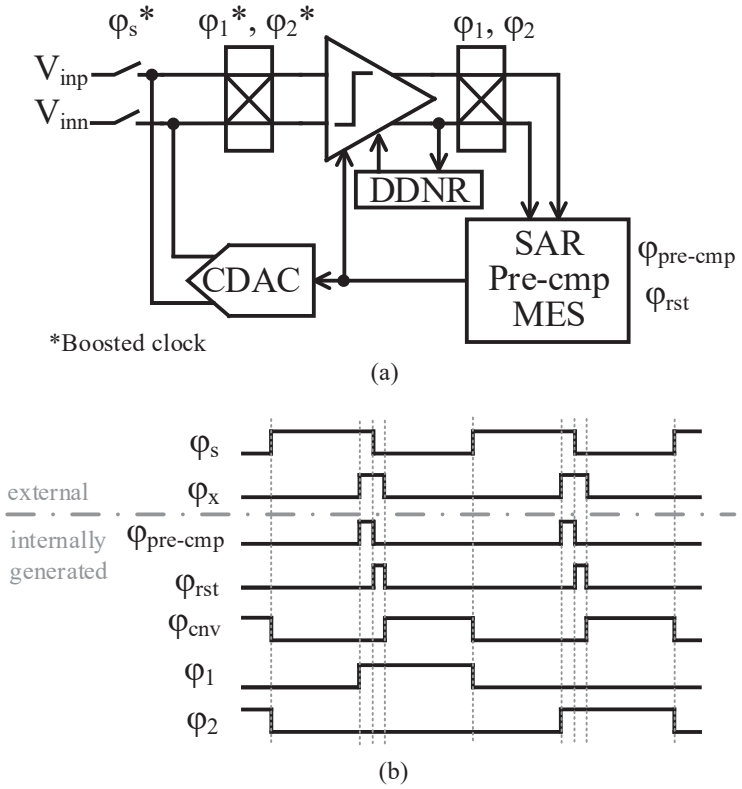


Figure 2.13: Block diagram (a) and timing diagram (b) of the ADC.

sampling moment when the input signal frequency is high.

Overall, a disadvantage of the 2-level prediction scheme compared to a 3-level scheme is that it is more susceptible to prediction errors. The probability of these errors can be reduced by increasing the oversampling ratio or by reducing the duty-cycle (which may increase the input driver power), but they cannot be avoided entirely. However, as long as the target SNDR is below the worst-case SNDR caused by these prediction errors, they can be tolerated. For example, this work aims for an SNDR of 85 dB, which can be achieved despite the presence of prediction errors (see Fig. 2.11(b)).

2.4 Circuit implementation

2.4.1 ADC Architecture

Fig. 2.13(a) shows the block diagram of the ADC. A 14-bit oversampled SAR ADC with self-synchronized logic is implemented. It operates from a single 0.8-V supply, which is also used as the reference voltage. The sampling rate is 128 kS/s with an OSR

of 16. Pre-comparison, MES, data-driven noise reduction (DDNR) [29] and chopping techniques are combined to improve the SNDR efficiently. The input switches are driven by boosted clocks [43].

Fig. 2.13(b) shows an overview of the timing diagram. Clock signals φ_s and φ_X are provided externally (for flexibility), while the remaining clocks are all generated inside the ADC. During the sampling phase, an additional comparison is performed at the rising edge of $\varphi_{pre-cmp}$ to detect the signal range. Then the MSB of the DAC will be switched for input range compensation according to the pre-comparison result. Later, sampling happens at the falling edge of φ_s. After that, there is a reset phase before the SAR conversion. During the reset phase φ_{rst}, the LSB DAC will be reset to realize the MES function while the MSB DAC will be used for input range compensation. After the reset phase, a regular SAR conversion starts in φ_{cnv}.

2.4.2 Comparator

Fig. 2.14 shows the schematic design of the comparator. The core is formed by a dynamic comparator composed of a pre-amplifier and a latch [44]. Besides, chopping and DDNR techniques are added. Also, a few logic gates are used to generate the timing for the SAR logic [45].

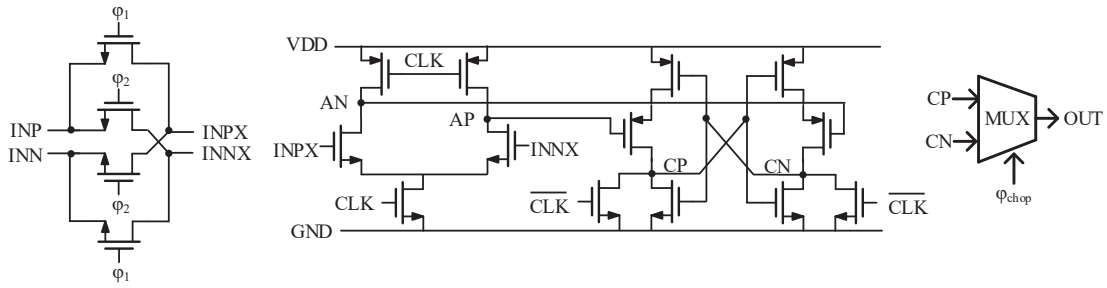


Figure 2.14: Schematic of the comparator, with analog input chopper and digital output chopper.

The comparator noise is a bottleneck for high resolution ADCs. Targeting at 80-90 dB SNDR, this work applies DDNR [29] to reduce the comparator noise in a simple and efficient way (Fig. 2.15). By averaging the results of multiple repeated comparisons, the noise of the comparator is reduced. This averaging is only done for the noise-critical decisions in the conversion when the input magnitude is small. In other cases, a single comparison is performed to save power. The noise reduction depends on two parameters: NC and NV. Here, NC stands for the number of voting cycles and NV stands for the number of voting bits. For a DDNR setting with NC = 5 and NV = 3, voting will be enabled for 3 critical bits and for each bit, at most 5 comparison cycles will be performed. Once the majority is reached, voting ends and the majority value of the results becomes the final output. Compared to noise-shaping architectures, the implementation of DDNR does not require any additional

integration phase, amplifiers or multi-input comparators to achieve noise reduction. Only digital logic is required, which tends to be more area-efficient and robust over PVT.

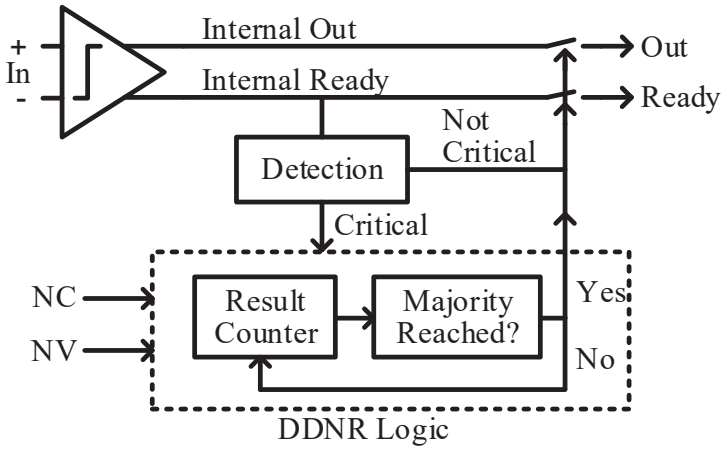


Figure 2.15: Block diagram of DDNR.

To reduce the comparator's 1/f noise, chopping is applied. In order to avoid interference with the MES technique, which uses a system-level feedback loop, local chopping instead of system level chopping is applied. The input chopping switches are inserted in front of the comparator instead of being inserted in front of the ADC (Fig. 2.13(a)), and the output chopping switches are placed directly after the comparator (in the digital domain). The on-resistance of the input chopping switches introduces extra noise. Moreover, it also affects the ADC linearity because the on-resistance is signal-dependent and results in a signal-dependent settling at the comparator input. Thus, the input chopping switches are designed as small NMOS switches driven by two boosted clocks [43] working at half the sampling rate.

2.4.3 DAC

The DAC is implemented as a 14-bit charge-redistribution DAC in this design. Custom designed finger capacitors made with metal layers 6 and 7 are used. The sampling capacitance is 2.2 pF per side while the unit capacitor of the LSB is only 125 aF. Due to layout parasitics (C_p), the full-scale range of the DAC is reduced to [-0.7 V, +0.7 V] for a 0.8-V supply, which results in 90-dB kT/C-noise limited SNR with an OSR of 16. Note that the reduction of the full-scale due to C_p is not affecting the SQNR, as the LSB step-size is reduced at the same time. This is different from the signal range loss due to MES feedback, as the MES feedback occupies half of the range, while the LSB step-size is not scaled, thus resulting in 6 dB SQNR loss. Therefore, the signal range loss due to MES should be compensated, while the loss due to C_p is acceptable.

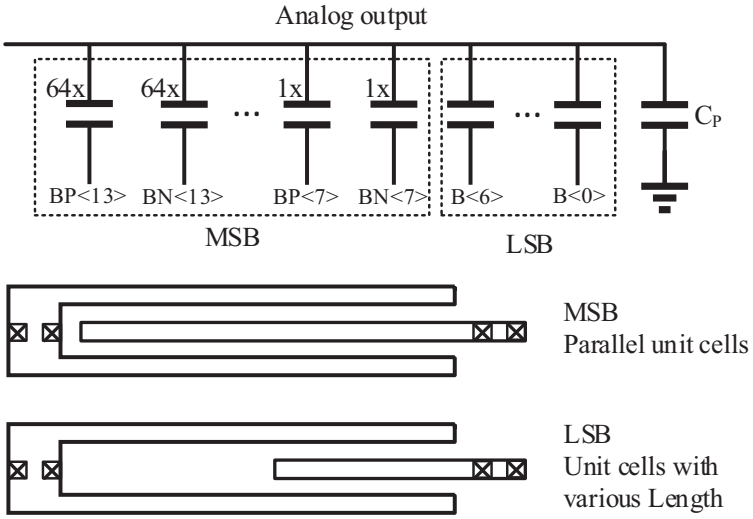


Figure 2.16: DAC schematic overview, and layout sketch of DAC capacitors.

The 7 MSBs (B⟨13⟩ down to B⟨7⟩ in Fig. 2.16) are implemented by parallel unit cells in the layout to achieve relatively good matching. On the other hand, the 7 LSBs are implemented by binary-scaled layout cells by changing the finger lengths, resulting in relatively poor matching. This largely reduces the number of used elements from 16383 to 261 and thus reduces the area cost. As simulated in Section 2.3, a unit mismatch of $\sigma = 6\%$ can be tolerated. In the actual implementation, the 7 MSB capacitors are implemented by unit cells and expected to achieve a unit mismatch below 1%. For the LSB capacitors, their mismatch is expected to be much larger. For instance, with a $\sigma = 1\%$ for the MSB capacitors and a pessimistic expectation of a $\sigma = 20\%$ for the LSB capacitors, the ADC is still able to achieve an SNDR of 92 dB considering mismatch errors only, according to a Monte Carlo analysis in Matlab.

Thanks to the MES and pre-comparison techniques, capacitors with such small values and area are able to achieve sufficient linearity. To further reduce the DAC power and enable the pre-comparison technique, a split monotonic switching scheme is employed to the MSBs.

2.4.4 Power and area overhead

In this section, the overhead in terms of area and power consumption of the proposed analog pre-comparison technique is discussed and compared to a digital prediction technique, using our particular ADC as an example. With the proposed MES and pre-comparison, the additional pre-comparison logic occupies an area of 49 μm^2, which is negligible. The additional DAC switching consumes 5% of the total power while the pre-comparison logic and the extra comparison consume only 4% of the total power. The extra comparison is performed by the regular comparator working in high-noise

mode, which makes it power efficient. For comparison, a simplified 2-level 3-bit digital prediction technique similar to [15] was also designed and simulated using the 65-nm CMOS technology of this work. In that case, the extra DAC switching still adds 5% to the power consumption, while the extra logic occupies 132 μm^2 and adds 3.1% instead of 4% to the overall power consumption. Since the above values all depend on the exact implementation and the level of optimization, it should be stressed that they serve as a rough indication only. However, overall, both the digital and analog prediction methods result in simple methods with a practically negligible overhead in area and power.

2.5 Measurement results

Fig. 2.17 shows a die photo of the prototype. The implemented ADC occupies an area of 0.033 mm^2 in a 65-nm CMOS technology and consumes 0.98 μW from a 0.8-V supply at 128 kS/s. The signal bandwidth is 4 kHz with an OSR of 16. The differential input range is 1.4-V peak-to-peak. The input signal is provided by a differential signal generator with 100-Ω differential output impedance.

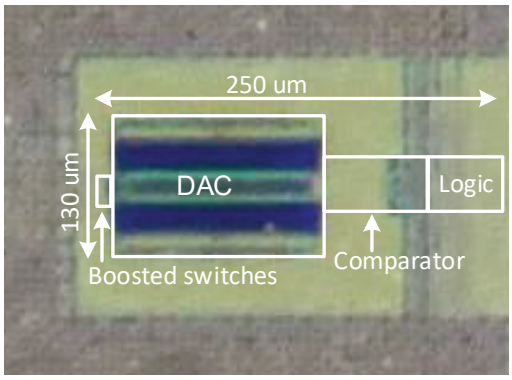
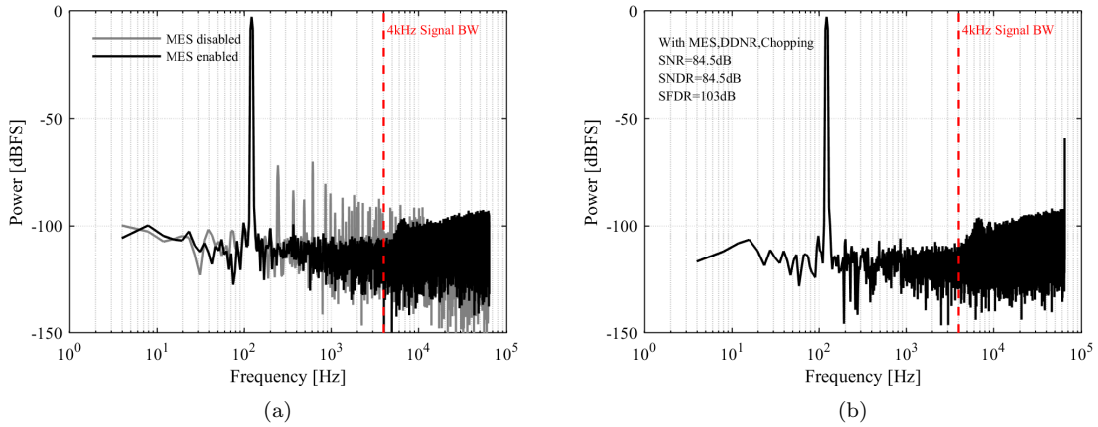


Figure 2.17: Die photo in 65-nm CMOS.

Fig. 2.18 shows the measured spectra under various conditions. Without any enhancements, at 128 kS/s with an OSR of 16 and an input frequency of 122.09 Hz, the measured SNDR and SFDR of the ADC are 64.4 dB and 67.5 dB, respectively. There are lots of distortions shown in the output spectrum and the ADC performance is limited by the DAC mismatch. Fig. 2.19 shows the measured INL and DNL for four chip samples when MES and pre-comparison are turned off. The INL and DNL are measured by a histogram test with 1 million points. The measured maximum INLs are 8.7LSB, 10.7LSB, 9.3LSB and 9.9LSB, respectively. Compared to [29] which uses a 9 pF DAC capacitance with a similar DAC implementation approach and achieves an INL of 3.5LSB, the intrinsic DAC mismatch is in line with the expectations.

With pre-comparison and MES techniques enabled, the SNDR is enhanced to 80.7 dB while the SFDR is improved to 97.2 dB. To further enhance the performance, the



(a) (b)

Figure 2.18: Measured spectrums: with MES disabled/enabled and other techniques off (a), with MES, DDNR, and chopping enabled (b).

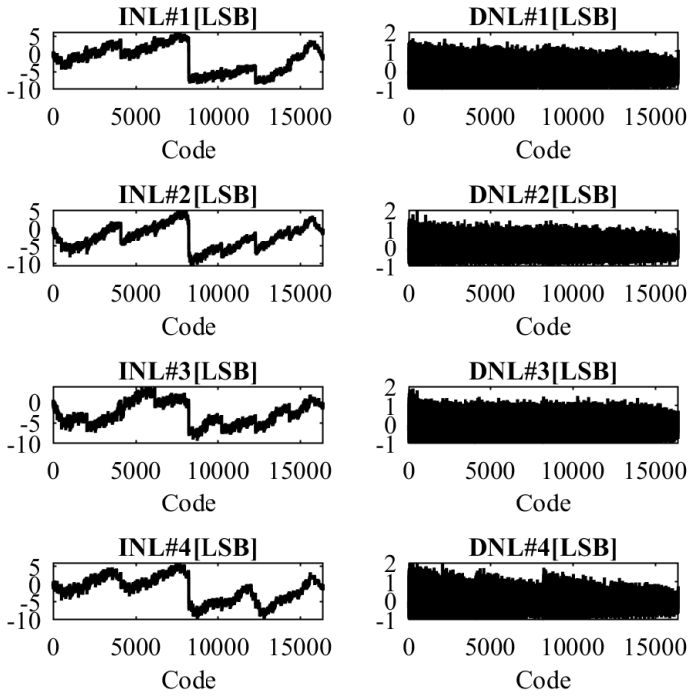


Figure 2.19: Measured INL and DNL with MES and pre-comparison off for 4 samples.

application of chopping and DDNR improves the SNDR to 84.5 dB and the SFDR to 103 dB with an extra power consumption of 0.24 μW (Fig. 2.18(b)). Fig. 2.20 shows the measured SNDR and power consumption with different DDNR settings. According to the measured results, the DDNR is set to vote with 5 cycles on 4 bits for the best combination of noise performance and efficiency. Fig. 2.21 shows the measured SNDR and SFDR versus different input frequencies and amplitudes when all techniques are enabled. It shows that this work attains more than 84 dB

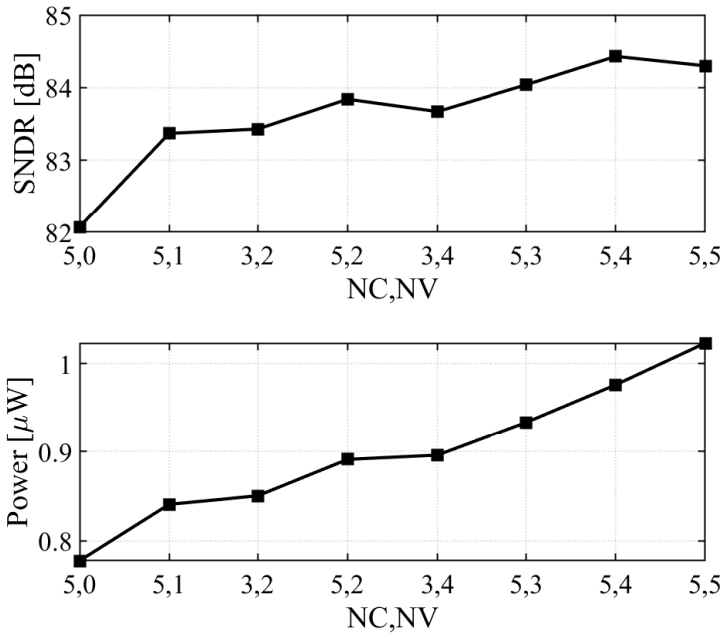


Figure 2.20: Measured SNDR and power consumption with different DDNR settings.

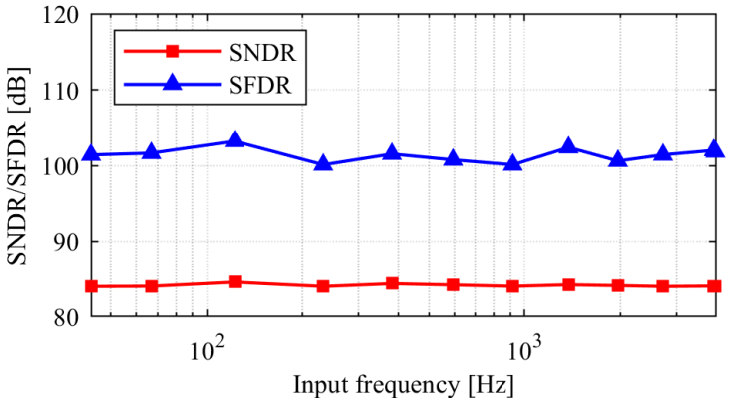
SNDR and 100 dB SFDR over the whole signal bandwidth. The measured SNDR and SFDR versus input amplitude indicate a dynamic range (DR) of 85 dB. The maximum Schreier and Walden FoM (FOM_S and FOM_W, respectively) are 180.6 dB and 8.9 fJ/conversion-step, respectively.

The duty cycle of the pre-comparison phase is controlled by an external clock for flexibility. Fig. 2.22 shows the measured SNDR and SFDR versus the duty cycle of the pre-comparison phase. With an OSR of 16, the pre-comparison phase can be as large as the sampling phase (50%) in this design. When the duty cycle is less than 6.25%, the timing is not sufficient for the pre-comparison logic and DAC preparation, distortions occur and the measured SNDR and SFDR drop down. The performance is not very sensitive to the duty cycle of the pre-comparison phase as long as it is in the nominal range.

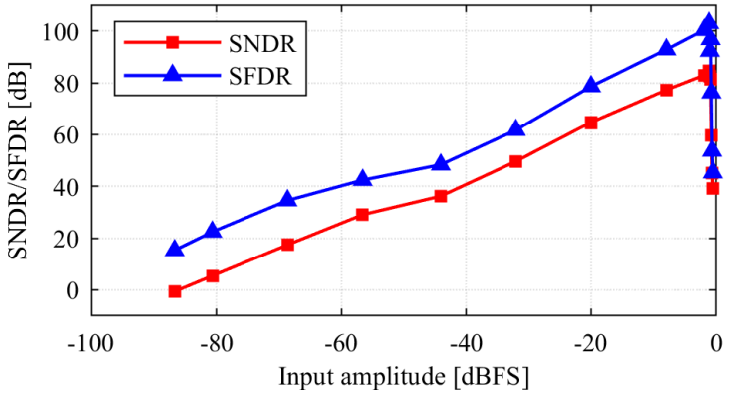
The power breakdown of the ADC is shown in Fig. 2.23. Thanks to the MES and pre-comparison techniques, the used capacitors are relatively small and the DAC consumes only 33% of the total power. The comparator consumes 57% of the total power, which dominates the overall power consumption.

Fig. 2.24 shows the measured SNDR and SFDR over 5 samples with all techniques enabled. The mean SNDR over 5 samples is 83.9 dB with a standard deviation of 0.4 dB. The mean SFDR is 101.2 dB with a stand deviation of 1.1 dB.

Table 2.1 summarizes the performance of this prototype and benchmarks it with state-of-the-art designs. Compared to other ADCs with similar SNDR, this work



(a)



(b)

Figure 2.21: Measured SNDR/SFDR versus different input frequencies (a) and amplitudes (b).

achieves state-of-the-art power-efficiency and good area-efficiency with a robust, process insensitive and calibration-free architecture. As shown Fig. 2.25, among ADCs with above 100-dB SFDR, this prototype is the smallest design without calibration. Moreover, at this SFDR, it is the only sub-μW (and sub-1V) design.

2.6 Conclusion

In this chapter, a 14-bit oversampled SAR ADC for IoT, bio-recording and environmental sensing applications is presented. MES, pre-comparison, DDNR and chopping techniques are combined to improve the linearity and SNR efficiently. Overall, this work achieves 84.5-dB SNDR and 103-dB SFDR with a sampling frequency of 128 kS/s, an OSR of 16, a power consumption of 0.98 μW from a 0.8-V supply and an area of 0.033 mm^2, resulting in a Schreier FoM of 180.6 dB and a Walden FoM of 8.9 fJ/conversion-step.

The proposed pre-comparison technique is combined with MES to shape DAC mis-

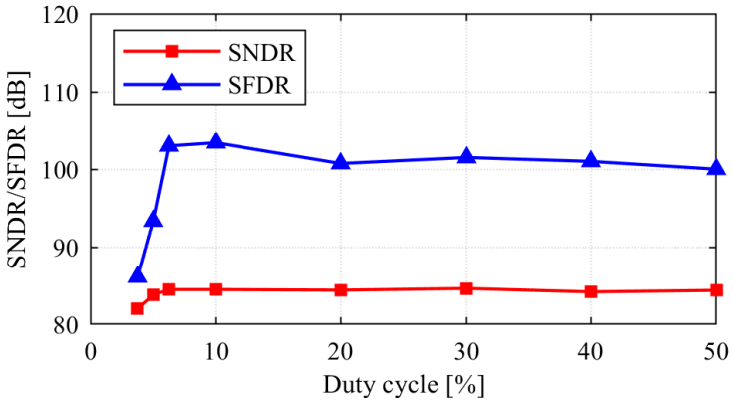


Figure 2.22: Measured SNDR and SFDR versus the duty cycle of the pre-comparison phase with a 1.4-V peak-to-peak input and an f_{in} of 122.09 Hz.

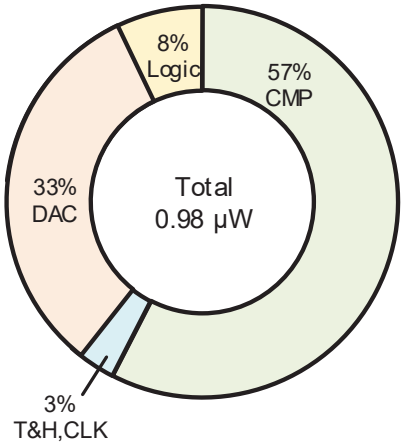


Figure 2.23: Power breakdown of the ADC.

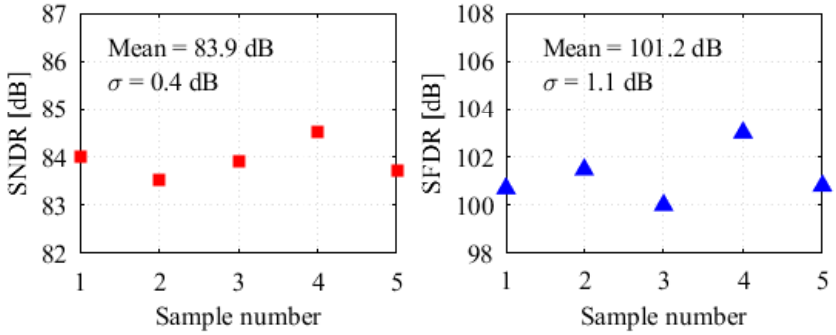
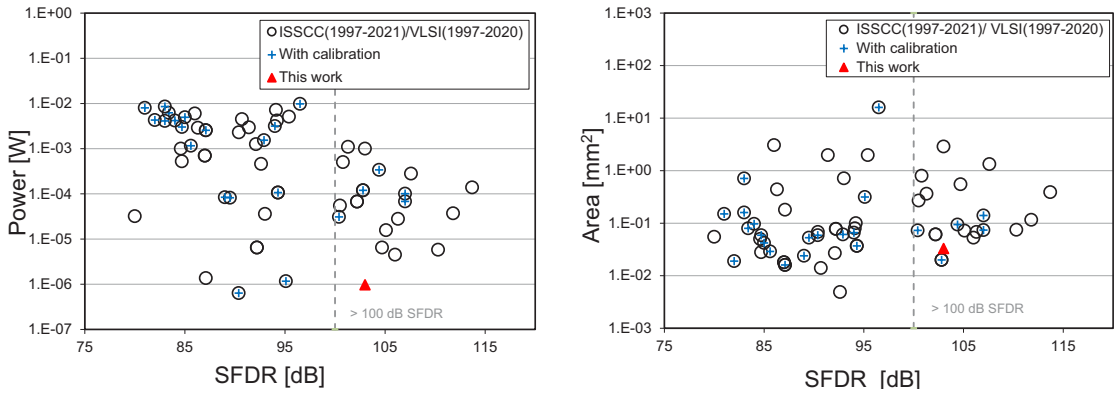


Figure 2.24: Measured SNDR/SFDR for 5 samples.

match errors while maintaining the full input range. Hence, a small DAC capacitance can be used for a high-resolution SAR ADC and the ADC's power-efficiency and area-efficiency are improved significantly.

By applying MES and pre-comparison, non-linearity caused by DAC mismatch is largely mitigated and comparator noise starts to dominate. To further improve its



(a) (b)

Figure 2.25: Benchmark of this work and state-of-the-art designs: (a) Power vs SFDR (b) Area vs SFDR data from [26].

power-efficiency, noise shaping techniques could be applied as a next step [38, 46].

One drawback of this work is that since the input range compensation is based on prediction, there is a chance that the prediction is wrong. The prediction accuracy is related to the shape of the input signal, the OSR of the system and out-of-band interference. This is also true for other prediction based methods [39, 40]. In Chapter 3, a MES SAR ADC with flying capacitor based sampling is introduced, which can avoid these prediction errors.

Table 2.1: Performance Summary and Comparison

	[27]	[11]	[28]	[29]	[32]	[38]	[39]	This work
Technology (nm)	40	40	28	65	28	55	40	65
Area (mm^2)	0.094	0.037	0.02	0.18	0.0049	0.072	0.061	0.033
Supply voltage (V)	1.1	0.8/1.1	1	0.8	1	1.2	1.1	0.8
Sample rate (kS/s)	5000	10000	2000	128	132000	1000	2000	128
Oversampling ratio	10	8	10	16	13.2	250	25	16
Bandwidth (kHz)	250	625	100	4	5000	4	40	4
Total DAC cap [pF]	32	4	15.4	18	3.2	4.8	36	4.4
Power (μW)	340	107	120	1.37	460	15.7	67.4	0.98
SFDR (dB)	104.4	94.3	102.8	97.1	92.6	105.1	102.2	100-103
SNDR (dB)	93.3	83.8	87.6	79.1	79.74	96.1	90.5	84-84.5
DR (dB)	95	85.5	89	-	81.8	-	94.3	85
FOM_W(fJ/conv.step)[1]	18	6.8	30.6	23.2	5.8	37.61	30.77	8.9-9.4
FOM_S(dB)[2]	182	181.5	176.8	173.8	180.1	180	178.2	180.1-180.6
Calibration-free	No	No	No	Yes	Yes	Yes	Yes	Yes
Architecture	NS SAR	NS SAR	NS SAR	OS SAR	NS SAR	NS SAR	NS SAR	OS SAR

[1] $FOM_W = Power/(2^{ENOB} \times 2 \times BW)$
[2] $FOM_S = SNDR + 10 \times \log 10(BW/Power)$

Chapter 3

MES SAR ADC with flying capacitor sampling

As mentioned in Chapter 2, DAC mismatch is a major challenge for high resolution SAR ADCs and MES with input range compensation is an efficient way to address this issue. In this chapter, an improved input range compensation technique based on analog detection will be presented. By adopting flying capacitor sampling, the prediction errors described in Chapter 2 can be avoided.

The content of this chapter has been published in [17].

3.1 Introduction

According to the analysis presented in Section 2.1, a major challenge for high-resolution SAR ADCs is DAC mismatch, which sets a minimum to the used capacitor value and dictates the required power consumption and area. Many techniques have been proposed to address the DAC mismatch issue [23, 29, 38, 39, 47–49]. Among these techniques, MES is an efficient choice for high-resolution SAR ADCs thanks to its capability of being applied to binary-scaled cells [38]. One disadvantage of MES is that the ADC will lose half of the input range, which tightens the absolute noise requirements for high-resolution systems. To solve this problem, existing solutions can be divided into two categories. The first option is applying MES only to the LSBs [38,48]. For segmentation-based methods, part of the input range is still lost and DWA is required to solve the MSB capacitor mismatch. The second option is to compensate the input range by prediction [23, 39, 49]. The main challenge for prediction-based methods is that the prediction might be wrong. Its accuracy is highly related to the OSR of the system (usually requires an OSR $\geq$16) and the presence of interferers.

In this chapter, an input range compensation technique based on analog detection will be discussed. By performing a pre-comparison and switching the DAC MSB accordingly, the input range is then fully recovered and no DWA is required while MES can be applied to all bits in the converter. By using a flying capacitor sampling technique, the pre-comparison is done after the sampling moment. Hence, prediction errors are avoided. A prototype SAR ADC with a 14-bit resolution is implemented in 65 nm CMOS. The circuit achieves 80.4 dB SNDR with 0.656 μW in a 0.034 mm^2 area.

This chapter is organized as follows: Section 3.2 reviews the principle of MES with input range compensation. Section 3.3 discusses the proposed analog detection and compensation technique with flying capacitor sampling. Section 3.4 presents the circuit implementation in detail. Section 3.5 provides the measured results and Section 3.6 draws the conclusion.

3.2 Review of MES with input range compensation

Fig. 3.1 shows the principle of MES with input range compensation. Mismatch is a relative error. Taking the DAC MSB as a reference, the LSB mismatch can result in conversion errors $E[n]$ at the nth conversion cycle. For ADCs with MES, the previous LSB code ($D_{LSB}[n-1]$), together with its conversion error $E[n-1]$, will be fed back to the current input signal ($V_{in}[n]$) before SAR conversion. Afterwards, $D_{LSB}[n-1]$ will

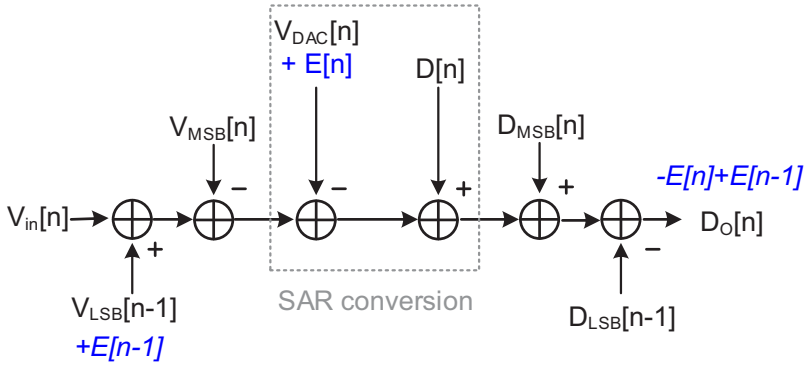


Figure 3.1: Principle of MES with input range compensation.

be subtracted in the digital domain. During the nth SAR conversion, a new $E[n]$ is generated. This results in a function of $-E[n]+E[n-1]$ at the output, which behaves as a high-pass filter for DAC mismatch errors. Thus, the DAC mismatch errors are 1st-order shaped to high frequencies and can be filtered out in an oversampled system.

Assume that the original input range of a differential ADC is [-V_{ref},V_{ref}]. $D_{LSB}[n]$ can be any value within [-$\frac{1}{2}V_{ref}$, $\frac{1}{2}V_{ref}$]. Hence, half of the original input range is occupied by the MES feedback signal, resulting in overrange of the ADC if the same input range is maintained. A prediction can be done to estimate the direction of overrange. Depending on the predicted signal range, a compensating voltage shift created by the available MSB capacitors can be applied to the input prior to sampling, to avoid overrange. Then, this compensation voltage is removed again in the digital domain. In this way, DAC mismatch errors can be shaped without input range loss. Depending on the actual design, either analog or digital, 2-level or 3-level prediction can be adopted [23, 39, 49].

One drawback of prediction-based methods is that the prediction accuracy is sensitive to OSR and interference. Hence, a certain OSR is required to ensure prediction accuracy, which is necessary to avoid conversion errors.

3.3 Proposed input range compensation with analog detection

3.3.1 Architecture and operation

This work adopts the same principle described in Fig. 3.1. However, instead of prediction, this work proposes an input range compensation technique based on analog

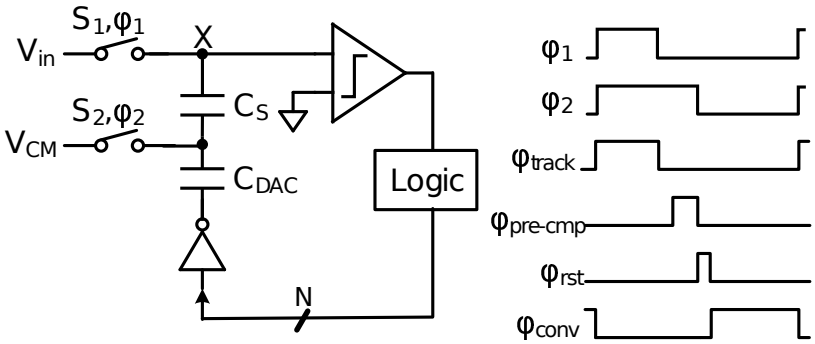


Figure 3.2: A simplified diagram of a SAR ADC with the proposed input range compensation technique and its timing diagram.

detection. A simplified diagram of a SAR ADC with the proposed input range compensation technique and its timing diagram are shown in Fig. 3.2. Note that C_{DAC} represents an N-bit binary-scaled array of capacitors, as required for the SAR operation. Further, a single-ended diagram is shown here for simplicity. Compared to a conventional top-plate sampled SAR ADC, a separate sampling capacitor (C_S) in series with the DAC capacitors (C_{DAC}) and an extra sampling switch are introduced. The two sampling switches (S_1 and S_2) are controlled by φ_1 and φ_2, respectively. Besides, an extra pre-comparison phase is generated after the sampling moment and the reset phase is positioned after the pre-comparison phase and before the SAR conversion phase.

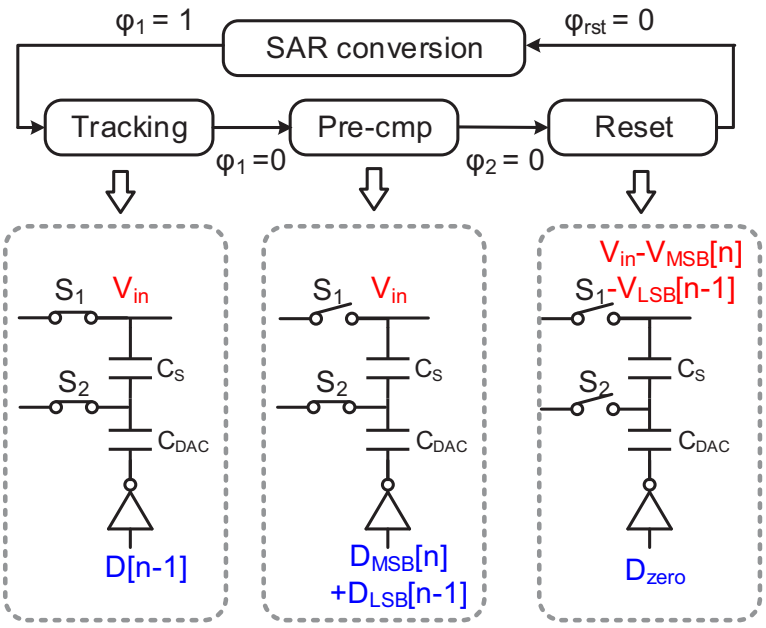


Figure 3.3: Circuit operation of the proposed input range compensation technique.

As shown in Fig. 3.3, the circuit-level operation consists of 4 phases, tracking, pre-comparison, reset and SAR conversion. The signal processing for the n^{th} cycle starts at the rising edge of φ_1. First, during the tracking phase, the sampling capacitor (C_S)

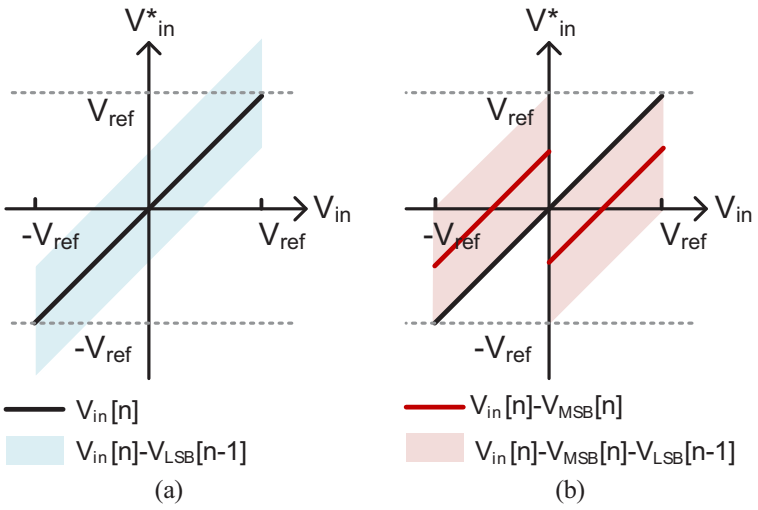


Figure 3.4: A conceptual diagram of the equivalent input signal without (a) and with (b) input range compensation.

tracks the input. The DAC capacitors remain at their state of the previous cycle. After V_{in} is sampled on C_S at the falling edge of φ_1, a pre-comparison using the existing comparator of the ADC will be done to determine the polarity of V_{in}. While the sampling capacitor continues holding the input, the DAC MSB capacitors are now set to the polarity of the input signal, which was detected by the pre-comparison. The DAC LSB capacitors still remain at their previous value. Then, at the falling edge of φ_2, S_2 is opened. The sampling capacitor is now floating. Both MSB and LSB capacitors are reset by changing the control codes from $D_{MSB}[n] + D_{LSB}[n]$ to D_{zero}. Here, D_{zero} represents the DAC code in the reset state. The equivalent sampled signal at the comparator input (V_{in}^*) becomes $V_{in} - V_{MSB} - V_{LSB}$, where V_{LSB} enables the MES operation, and V_{MSB} creates the compensation to prevent overrange. As conceptually shown in Fig. 3.4, the input range of the ADC is recovered to [-V_{ref},V_{ref}] when compensation is applied. A regular SAR conversion starts afterwards and sets the DAC control codes to $D[n]$.

The main advantage of this detection scheme is that it determines the compensation voltage after sampling, whereas previous prediction methods determine the compensation prior to the sampling moment. As a result, the proposed method does not suffer from prediction errors.

3.3.2 Discussion

By using the proposed analog-detection-based input range compensation, two samplings steps are performed and now the sampling noise power is equal to:

$$\frac{2kT}{C_S} + \frac{2kT}{C_{DAC}} \tag{3.1}$$

To minimize the noise overhead, C_S should preferably be larger than C_{DAC}. For instance, if C_S is equal to 2.7 C_{DAC}, it degrades the SNR by only 1.4 dB.

On the other hand, by performing two samplings steps, the information of the current input signal can be known without prediction, and thus without errors. For comparison against prior prediction schemes, Fig. 3.5 shows the maximum input amplitude without overrange as a function of the input frequency with and without an interference tone, simulated using a behavioral model. If interference is enabled, it is set to a 20% full-scale tone at $0.4f_s$, so it can be compared against the results in [23, 39]. Thus, ideally, the input signal should reach 100% full-scale without interference or 80% full-scale with interference, unless prediction errors occur. As can be seen, with digital [39] or analog [23] prediction schemes, the maximum input amplitude drops for higher input frequencies due to prediction errors, which thus implies a minimum required OSR to limit the signal bandwidth. Besides, the existence of interference will further degrade the prediction accuracy. On the other hand, the proposed analog detection method can avoid these concerns.

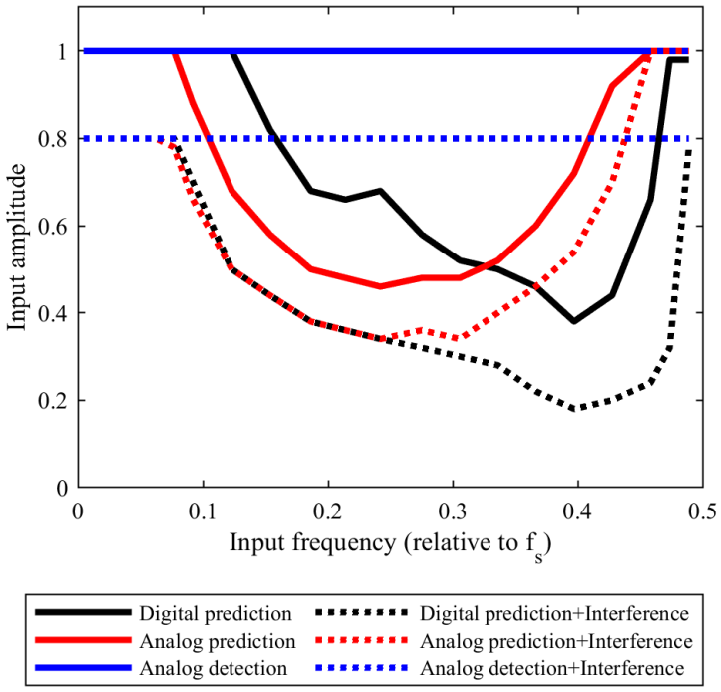


Figure 3.5: Simulated input amplitude as a function of input frequency with and without interference.

3.4 Circuit implementation

3.4.1 Track and hold

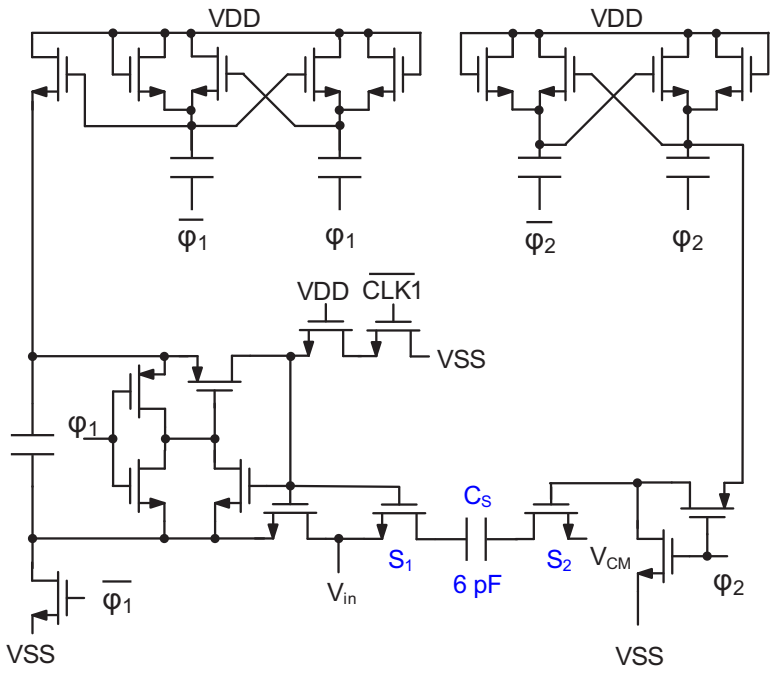


Figure 3.6: Schematic of the proposed flying capacitor sampling circuit.

The schematic design of the new track and hold circuit is shown in Fig. 3.6, which consists of sampling switches S_1, S_2 and a sampling capacitor C_S. S_2 is driven by a boosted clock for simplicity and lower power overhead. S_1 is driven by a bootstrapping circuit for higher linearity requirement.

Theoretically, the absolute value of C_S does not affect the operation of the ADC. In the actual implementation, the mismatch of C_S and the mismatch of parasitic capacitances may result in even order distortion and affect the SNDR for a high-linearity system. A large C_S results in lower sampling noise and better matching. However, it may also degrade the maximum operation speed of the ADC and costs more area. As a trade-off, in this work, C_S is implemented by regular metal-oxide-metal capacitors with a minimal spacing of 100nm and its value is chosen to be 6 pF. It occupies 15% of the ADC area and results in 93 dB SNR with 2.2 pF DAC capacitance for an input range of 1.6 V and an oversampling ratio of 16. A 7% mismatch of C_S versus C_{DAC} can be tolerated to achieve above 100 dB SFDR, which is easy to satisfy with a 6 pF capacitance in the used technology.

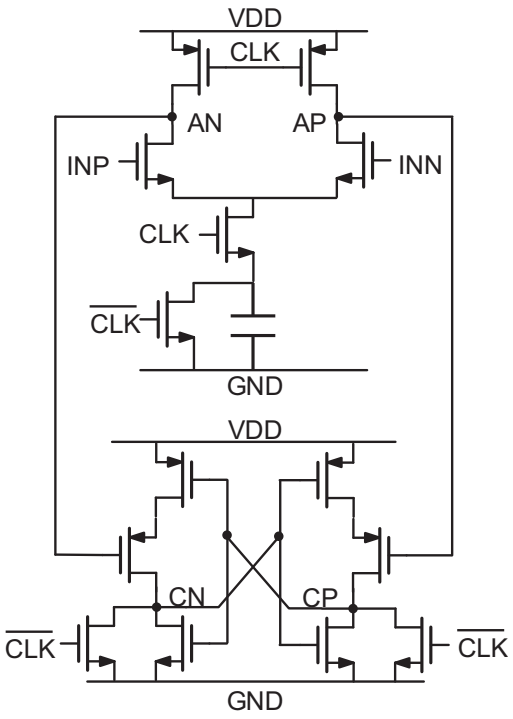


Figure 3.7: Schematic of the comparator [50].

3.4.2 Comparator

The comparator is another bottleneck for high-resolution SAR ADCs and one of the dominant power consumption sources. Fig. 3.7 shows the schematic design of the used dynamic comparator, which consists of a pre-amplifier and a latch. A tail capacitor and an NMOS switch are added to the bottom of the pre-amplifier to reduce the energy consumption by means of self quenching [50]. In this work, a 300 fF tail capacitor is used, which reduces the comparator power by around 23%.

3.5 Measurement results

The prototype ADC is implemented in 65 nm CMOS as shown in Fig. 3.8. It occupies an active area of 0.034 mm^2 and was measured to consume 0.656 μW at a sampling rate of 128 kHz from a 0.8 V supply.

The measured spectrum with a 128 kHz sampling rate and a 122 Hz input frequency is shown in Fig. 3.9. The peak-to-peak input signal range is around 1.36 V. With an OSR of 16, the prototype ADC achieves 80.4 dB SNDR and 92.8 dB SFDR in a 4 kHz signal bandwidth. The DAC mismatch error is first order shaped.

Fig. 3.10 shows the measured SNDR versus input frequency for a full range input

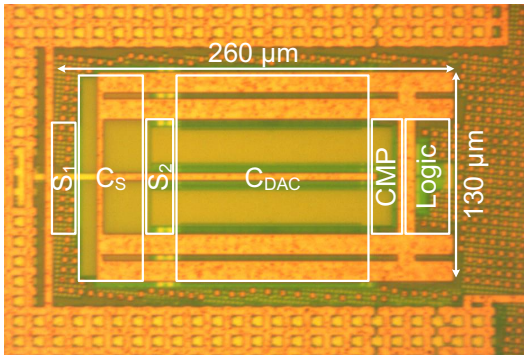


Figure 3.8: Chip micrograph.

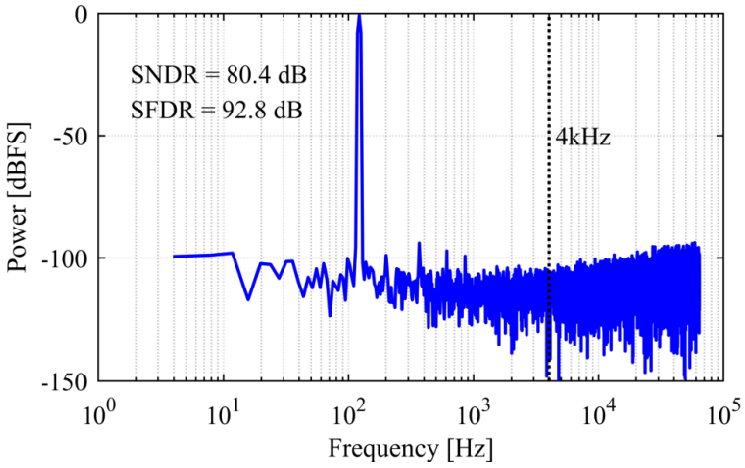


Figure 3.9: Measured spectrum for f_{in} = 122 Hz, at 128 kS/s and an OSR of 16.

and an OSR of 1 for this work and [23], respectively. Due to the lack of oversampling, the SNDR in this case is lower than before since all noise and distortion contributions count. However, this result confirms that the ADC does not saturate for any input frequency, as this would otherwise lead to a major SNDR reduction. For prior-art prediction methods, their SNDR will quickly drop for high input frequencies due to prediction errors as shown in Fig. 3.10.

Fig. 3.11 shows the post-layout simulated power breakdown of the ADC. Thanks to MES, small DAC capacitors can be used and the DAC switching occupies only 37.4% of the total power.

Table 3.1 summarizes the performance of this work and compares it to state-of-the-art designs with on-chip DAC mismatch calibration techniques. Compared to [23, 29, 38, 39, 47–49], this work achieves competitive energy and area efficiency with a simple architecture and zero prediction errors.

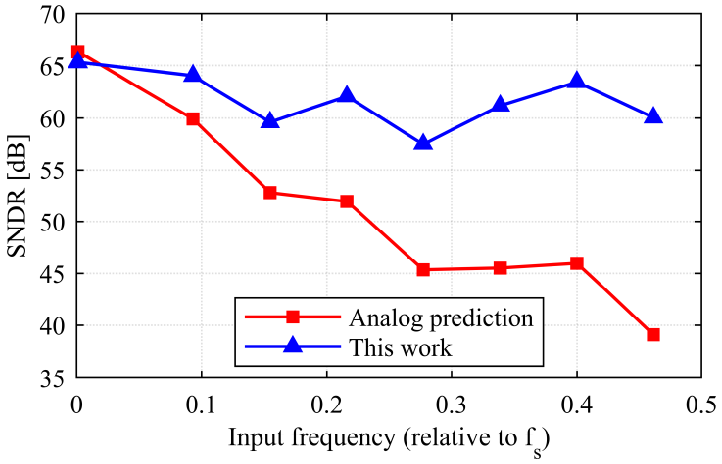


Figure 3.10: Measured SNDR versus input frequency under a full range input (OSR = 1) at f_s = 128kHz.

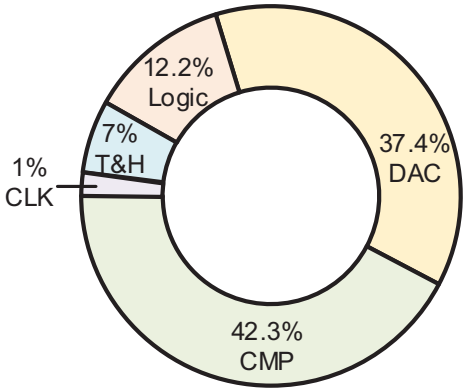


Figure 3.11: Power breakdown of the ADC.

3.6 Conclusion

This chapter presents a 14-bit SAR ADC with mismatch error shaping and analog-detection-based input range compensation. The proposed pre-comparison technique with flying capacitor sampling, can detect the input range without prediction errors. Combined with MES and smart MSB switching, the DAC mismatch error can be shaped without input range loss. The prototype ADC fabricated in 65 nm CMOS occupies an area of 0.034 mm^2 and consumes 0.656 μW at a sampling frequency of 128 kHz. The achieved SNDR and SFDR are 80.4 dB and 92.8 dB, respectively. The resulting Schreier FoM is 178.3 dB and the resulting Walden FoM is 9.57 fJ/conversion.

Compared to the pre-comparison technique shown in Chapter 2, prediction errors are avoided at the cost of extra bootstrapped switches and sampling capacitors. They only consume 3.5% power and occupy 3% area, which is negligible for high-resolution ADCs.

Besides, since C_S is 3× larger than C_{DAC}, it requires more power from the driver. On the other hand, the entire tracking period is used for tracking, whereas the C_{DAC} in

Chapter 2 needs to pre-set and resettle within a short pre-comparison phase, which may cause some trouble for the driver as well.

Another design consideration is the timing requirement of the pre-comparison phase. It is more critical in Chapter 2 since the pre-comparison happens before the sampling moment and its timing is directly related to the prediction errors. While for this design, pre-comparison happens after the sampling moment and the exact duty cycle of the pre-comparison phase does not matter.

Overall, for applications where a large OSR is anyway needed or the energy consumption of the front-end is not related to the duty cycle, the technique shown in Chapter 2 is simpler and more energy efficient. For applications with a limited OSR and potential interferences, the technique shown in this chapter is more suitable.

Table 3.1: Performance summary and comparison

	[47]	[29]	[38]	[48]	[39]	[49]	[23]	This work
DAC mismatch calibration	Vector-based DEM	Dither	MES +DWA	MES +DWA	MES +Digital prediction	MES +Digital prediction	MES +Analog prediction	MES +Analog detection
Technology [nm]	40	65	55	40	40	65	65	65
Supply voltage [V]	1.1	0.8	1.2	1.1	1.1	1.2	0.8	0.8
Sample rate [kS/s]	32000	128	1000	12800	2000	1000	128	128
Oversampling ratio	64	16	250	64	25	16	16	16
Bandwidth [kHz]	250	4	4	100	40	31.25	4	4
Power [μW]	4700	1.37	15.7	1998	67.4	7.3	0.98	0.656
SNDR [dB]	94.8	79.1	96.1	98.3	90.5	80	84.5	80.4
SFDR [dB]	103.0	87.1	105.1	108.5	102.2	98	103	93
DR [dB]	96	-	-	101.2	94.3	81.4	85	80.5
FoM$_W$ [fJ/conv-step] [1]	209.3	23.2	37.61	148.6	30.77	14.3	9.4	9.57
FOM$_S$[dB][2]	172.1	173.8	180	175.3	178.2	176.3	180.6	178.3
Area [mm^2]	0.37	0.18	0.072	0.48	0.061	0.043	0.033	0.034

[1] $FOM_W = Power/(2^{ENOB} \times 2 \times BW)$
[2] $FOM_S = SNDR + 10 \times \log 10(BW/Power)$

Chapter 4

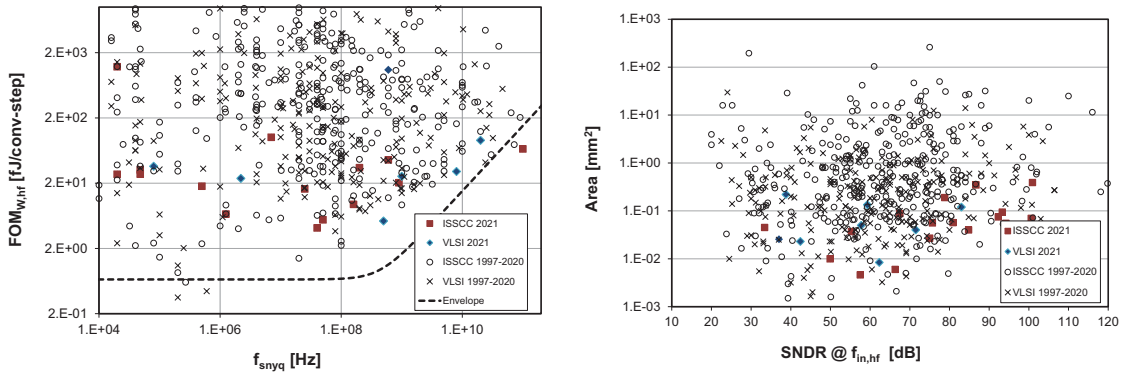
SAR ADC with 1.5× input range

This chapter presents a 10.5-bit 10 MS/s SAR ADC with 1.5× input range (IR) which aims to improve the power-efficiency and area-efficiency for low-to-medium resolution ADCs. By pre-setting and resetting the MSB of the DAC to shift the input signal accordingly, the input range of the ADC is enhanced by 50% compared to the ADC not using it. This effectively relaxes the noise requirements and thus improves the power efficiency of the ADC. Also, an N+0.5 bit resolution can be realized by using N-bit hardware, which improves the area efficiency of the ADC.

The content of this chapter has been published in [18].

4.1 Introduction

In the last decades, moderate-resolution ADCs have been widely used in a large range of applications. For example, for miniature ultrasound probes, ADCs with a resolution of 10-12bit and tens of MHz sampling rate are needed [51–53]. For imaging, an array of digitizers is required. Hence, the chip area and power consumption of each channel are critical. SAR ADCs are the most popular choice in these applications thanks to their high efficiency. As shown in Fig. 4.1, many designs aimed to improve the energy and area efficiency of ADCs, for example, various DAC switching schemes, comparator topologies, noise cancellation techniques and so on [8, 50, 54] were proposed.



(a) (b)

Figure 4.1: Efficiency benchmark (a) and area benchmark (b), data from [26].

The energy and area cost of low resolution ADCs are relatively low. Hence, extra enhancing techniques should also have a very low overhead. Usually, the area of a low resolution ADC is dominated by the DAC. On the circuit level, a good implementation of the DAC [55] is needed. On the system level, more resolution could be squeezed from an N bit DAC, for instance, by using oversampling or smart DAC switching techniques. The ADC power consumption is usually dominated by the comparator, and the comparator power is directly related to the noise requirement. On the circuit level, efficient comparators could be used [50, 56]. On the system level, signal power can be increased so that a higher comparator noise power can be tolerated for the required resolution.

Extending the equivalent input range of the ADC is one of the options. From one perspective, with the same supply voltage and SNR requirement, the absolute noise constraint of the circuits is effectively relaxed when a larger input signal is used. From another perspective, for a required input signal range, the used supply voltage can be lowered to reach the same SNR and thus the power consumption of the ADC can be reduced, which often scales with VDD^2. This is also convenient for applications with limited supply voltages, for example, an environment monitoring system powered by an energy harvester, where the usable supply voltage is usually below 1 V [57–59]. For these applications, techniques which can extend the input range can be very helpful.

To enhance the equivalent input range of an ADC, [60] proposes a MSB prediction technique. The MSB is obtained by prediction and the used reference voltage can be halved for the LSBs of a given input range. Multi-bit prediction and redundancy are used to guarantee the prediction accuracy. Extra capacitors are introduced for prediction. The simulated FoM_W is 9.5 fJ/conversion-step. Reference [59] proposes to use two identical sub-ADCs with different input ranges. Depending on the MSB decision, one of the two sub-ADCs will be enabled and thus the input range of the ADC increases by a factor of 2. [59] is very energy efficient and achieves a FoM_W of 0.44 fJ/conversion-step. However, redundancy is required to guarantee a sufficient overlap range for the sub-ADCs. Besides, to guarantee the linearity of the ADC, foreground calibration is required to calibrate the mismatch between the sub-ADCs

Different from the above approaches, this work proposes to use an MSB compensation technique which enhances the input range of the ADC by a factor of 1.5 and increases the ideal resolution by 0.5-bit with negligible area cost and limited power cost. A 10 MS/s SAR ADC is implemented in 65-nm CMOS technology to verify the idea, which achieves 9.74 ENOB with a FoM_W of 2.2 fJ/conversion-step and occupies an area of 0.0013 mm^2.

The rest of the chapter is organized as follows. Section 4.2 introduces the proposed MSB compensation technique. Section 4.3 describes the circuit implementation details. Section 4.4 presents the measured results and summarizes the performance of this work. Finally, Section 4.5 draws the conclusion.

4.2 Proposed MSB compensation technique

4.2.1 Principle and operation

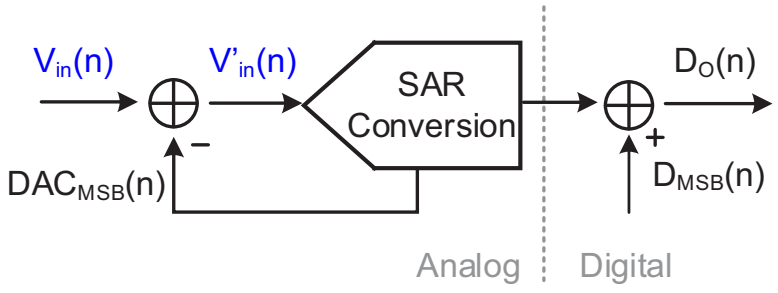


Figure 4.2: Behavioral model of SAR conversion with MSB compensation.

Fig. 4.2 shows a behavioral model of the SAR conversion with the proposed MSB compensation technique. The basic principle is to inject a negative input to partly cancel the input signal swing and then add it back in the digital domain. In this

way, the effective input range of the ADC is extended. This compensation can be implemented using the already available MSB capacitors inside the DAC.

Assume that the ideal input range is $[-V_{ref}, V_{ref}]$ for a SAR ADC with a differential input. As conceptually shown in Fig. 4.3, the MSB compensation technique will shift positive input signals V_{in} downwards by $\frac{1}{2}\ V_{ref}$, and will shift negative input signals upwards by $\frac{1}{2}\ V_{ref}$ prior to the actual SAR conversion. As a result, the input range is extended to $[-\frac{3}{2}\ V_{ref},\ +\frac{3}{2}\ V_{ref}]$.

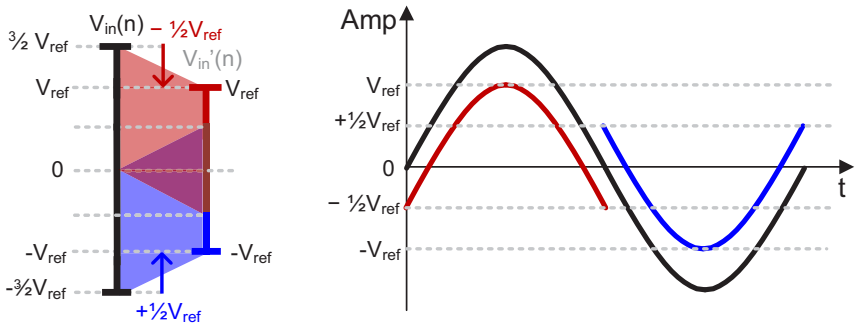


Figure 4.3: Equivalent input signals before and after MSB compensation.

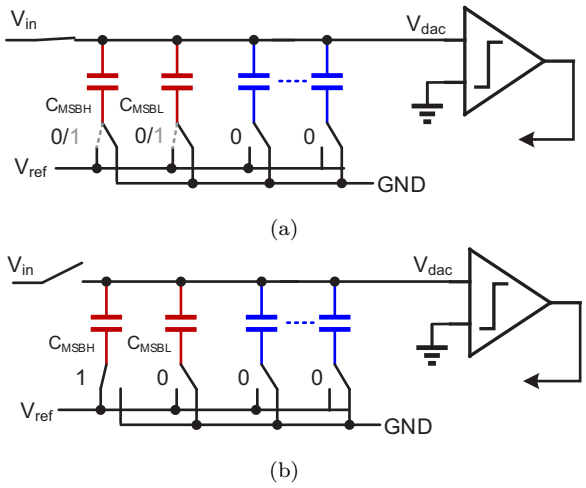


Figure 4.4: DAC operation during pre-set phase (a) and reset phase (b).

The circuit level operation of the proposed MSB compensation technique is shown in Fig. 4.4. A single-ended diagram is shown for simplicity. The MSB capacitor is split in two capacitors C_{MSBH} and C_{MSBL}. An additional pre-set phase will be inserted before the sample moment and an additional reset phase will be inserted after the sampling moment. During the pre-set phase, an additional comparison is performed to detect the polarity of V_{in} and the MSBs of the DAC are pre-set. For positive V_{in}, both MSB capacitors will be pre-set to 1. During the reset phase, the bottom plate of C_{MSBH} will be reset to 1 and the bottom plate of C_{MSBL} will be reset to 0. This operation will cause a $-\frac{1}{2}V_{ref}$ voltage shift for V_{dac}. Then, a normal SAR conversion starts.

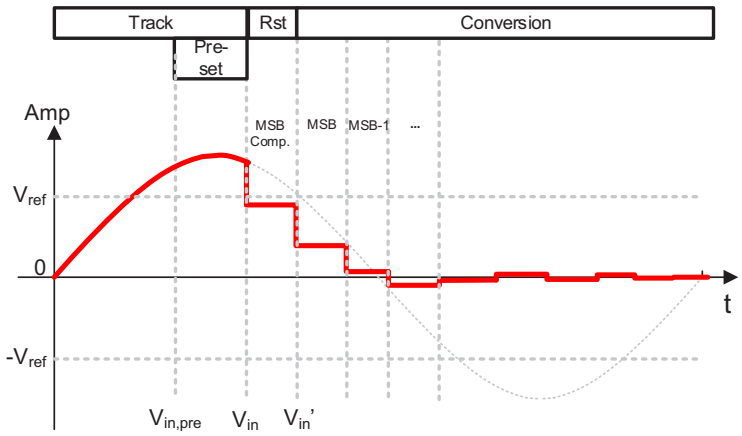


Figure 4.5: Signal behavior at the comparator input.

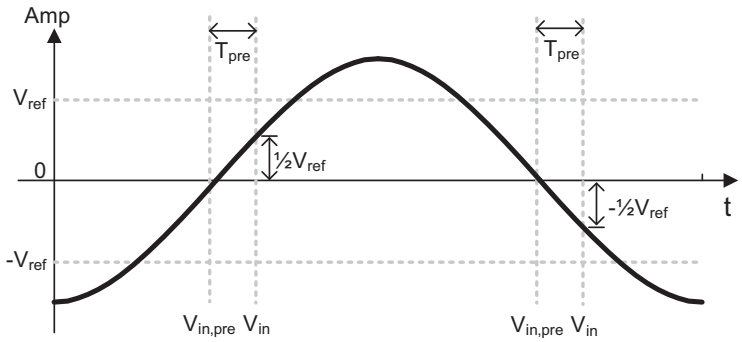


Figure 4.6: Critical cases where compensation errors may occur.

Correspondingly, for negative V_{in}, the MSB capacitors are pre-set to 0 and then the reset creates a $\frac{1}{2}V_{ref}$ shift for V_{dac}. By pre-setting and resetting the MSB capacitors, the input range of the ADC is thus enhanced by a factor of 1.5. Fig. 4.5 shows an example of the signal at the comparator input when $V_{in,pre} > 0$. After the MSB compensation, $V_{in}^{'} = V_{in} - \frac{1}{2}V_{ref}$, and the regular conversion is performed, starting with the MSB decision.

4.2.2 Pre-comparison timing requirements

Because the MSB compensation step is decided based on the polarity of $V_{in,pre}$ prior to the sampling moment, V_{in} and $V_{in,pre}$ may have different polarities, causing an incorrect compensation step. When V_{in} is in the range of $[-\frac{1}{2}V_{ref}, \frac{1}{2}V_{ref}]$, the converted signal $V_{in}^{'}$ is always in the conversion range regardless of being shifted up or down. In this case, it does not matter whether the MSB compensation is correct.

For $V_{in} > \frac{1}{2}V_{ref}$ or $V_{in} < -\frac{1}{2}V_{ref}$, a correct compensation should be made. The most critical case happens when V_{in} is near $\frac{1}{2}V_{ref}$ (or $-\frac{1}{2}V_{ref}$). As shown in Fig. 4.6, when

$V_{in,pre}$ is negative and V_{in} is larger than $\frac{1}{2}V_{ref}$ (or $V_{in,pre}$ is positive and V_{in} is smaller than $-\frac{1}{2}V_{ref}$), $V_{in}^{'}$ will overrange due to a wrong compensation. The tolerable pre-set timing margin T_{pre} can be calculated according to:

$$\frac{1}{2}V_{ref} = \frac{3}{2}V_{ref}sin(2\pi f_{in}T_{pre}) \tag{4.1}$$

Since $f_{in} < \frac{1}{2}f_s$ and $f_s = \frac{1}{T_s}$, it can be derived from (4.1) that:

$$T_{pre} \leq 11\%T_s \tag{4.2}$$

The duration of T_{pre} should be smaller than 11% of one sampling period to ensure an accurate compensation. It should be noted that a short duration of T_{pre} may imply a penalty in the required driving strength.

Overall, by applying the proposed MSB compensation technique, the ideal resolution of a SAR ADC is improved to N+0.5 bit using a N-bit hardware, which makes it area efficient. Also, the ideal input range of the ADC is enhanced to $\pm 1.5V_{ref}$, which effectively relaxes the noise requirement and is especially helpful for cases with a limited supply.

4.3 Circuit implementation

To verify this idea, a 10(+0.5) bit 10 MS/s SAR ADC is implemented as an example. Fig. 4.7(a) shows the architecture of the ADC, which consists of a sample and hold circuit, a comparator, a DAC, SAR logic and the new-added MSB compensation logic. The input switches are NMOS transistors driven by a clock boosting circuit [43] for linearity requirements. The used comparator is a fully dynamic two-stage comparator composed of a pre-amplifier and a latch [44]. Conventional self-synchronized SAR logic is used [45]. A 10-bit charge-redistribution DAC is used with custom designed unit-length finger capacitors [55] to minimize chip area. However, the proposed method could be applied equally well to other DAC implementations. The total sampling capacitance is around 250 fF, which results in 64 dB SNR for a normal SAR ADC with a supply voltage of 0.8-V and 67 dB SNR for this design with 1.5× input range.

Fig. 4.9 shows the DAC capacitor implementation, which is the same as [55]. Each capacitor consists of two sub cells (C_p and C_n). The effective DAC capacitance (C_{eff})

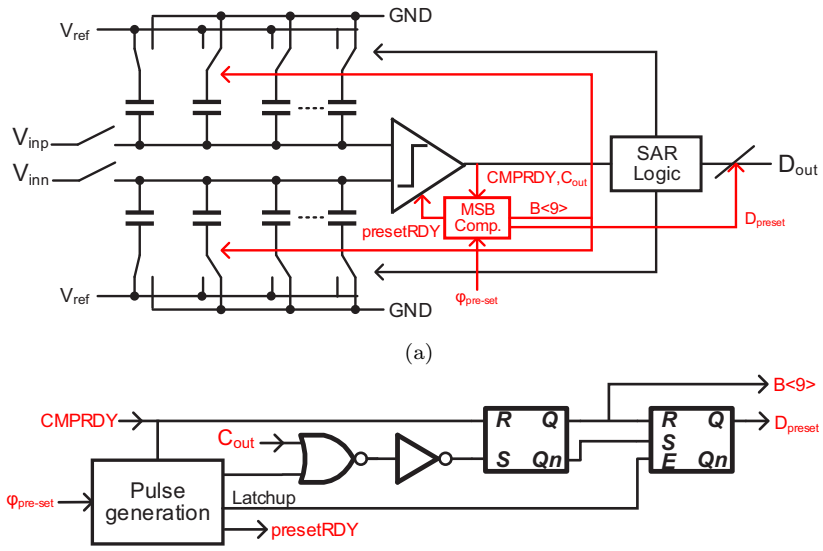


Figure 4.7: ADC architecture (a) and MSB compensation logic (b).

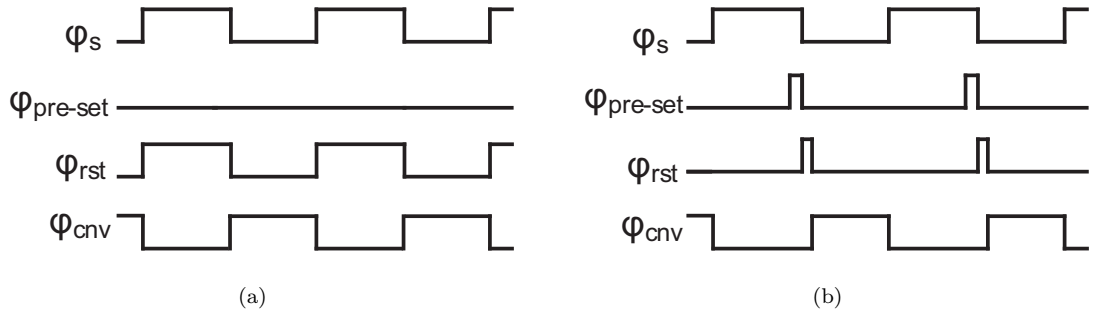


Figure 4.8: Timing diagrams:'IR×1' mode (a) and 'IR×1.5' mode (b).

is equal to the difference between the two sub cells which are almost equal except for a small $2 \times C_{\Delta}$. Thus, a very small unit capacitance can be achieved with decent matching [55]. Moreover, binary scaled capacitors can be made by changing Δ in a binary scaled fashion, which is much more area efficient compared to placing identical units in parallel to achieve binary scaling. The DAC capacitors are placed on top metals (Metal 6 and 7) and are vertically connected to the DAC drivers underneath. The rest of the ADC is also placed underneath to minimize chip area.

The detailed implementation of the MSB compensation logic is shown in Fig. 4.7(b). During the pre-set phase ($\varphi_{pre-set}$), the dynamic comparator of the SAR ADC will be enabled. After the comparison, a comparison ready signal (CMPRDY) and a comparator output signal (C_{out}) will be generated. Depending on the comparator output, a DAC control signal $B\langle 9 \rangle$ will be generated to control the switching of the MSBs of the DAC, a pre-set ready signal (presetRDY) will be generated to disable the dynamic comparator and a digital output signal D_{preset} will be generated.

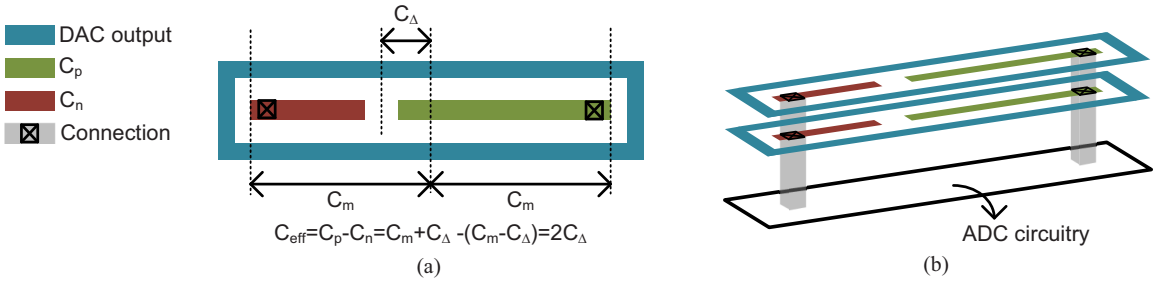


Figure 4.9: DAC capacitor implementation: top view (a), and 3D view (b).

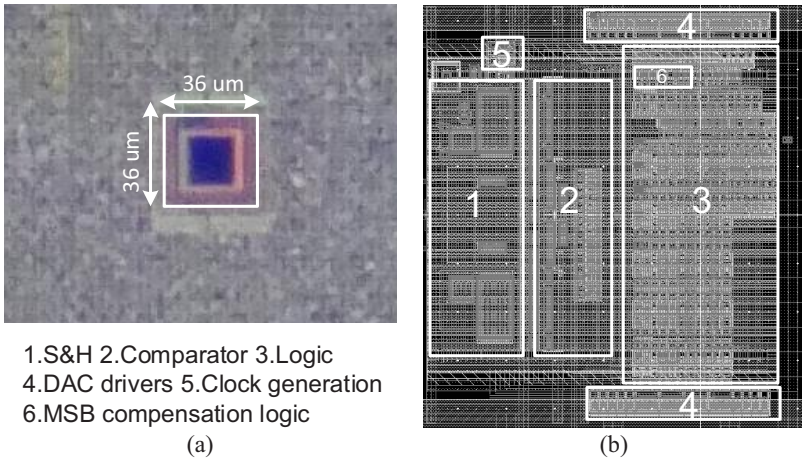


Figure 4.10: Die micrograph (a) and layout-view (b).

Fig. 4.8 shows an overview of the timing diagram. The ADC can operate in two input range modes: a conventional 'IR×1' mode (Normal SAR mode) and an 'IR×1.5' (SAR with 1.5× input range) mode. When working in 'IR×1' mode, the DAC will reset (φ_{rst}) during the sampling phase (φ_s) and after that the SAR conversion starts (φ_{cnv}). When working in 'IR×1.5' mode, the MSB of the DAC will be pre-set in the pre-set phase ($\varphi_{pre-set}$) and then be reset in an extra reset phase (φ_{rst}). After that, a normal SAR conversion starts (φ_{cnv}).

4.4 Measurement results

The prototype fabricated in 65-nm CMOS is shown in Fig. 4.10. It occupies an area of 0.0013 mm^2. The implemented ADC consumes 18.65 μW in 'IR×1.5' mode at 10 MS/s with a 0.8-V supply voltage.

Fig. 4.11 shows the measured spectra with an input frequency of 4.901 MHz. When working as a normal SAR ADC, this design achieves 56.8 dB SNDR, 82.9 dB SFDR and 9.14-bit ENOB with a maximum input amplitude of -0.37 dBFS. In this case, the

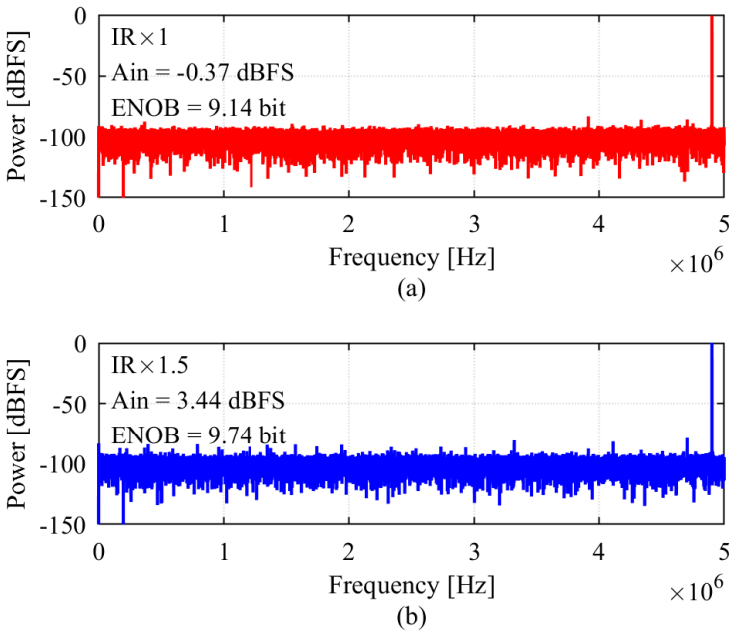


Figure 4.11: Measured spectrum with an input frequency of 4.901 MHz in 'IR×1' mode (a) and 'IR×1.5' mode (b).

ADC achieves a Schreier FoM of 167.7 dB and a Walden FoM of 2.9 fJ/conversion-step. When working in 'IR×1.5' mode, the maximum input amplitude is improved to 3.44 dBFS while the noise level remains the same. Thus the SNDR is improved to 60.37 dB and the ENOB is improved to 9.74-bit. The measured SFDR is 82.2 dB. The resulting Schreier FoM and Walden FoM are improved to 174.7 dB and 2.2 fJ/conversion-step, respectively.

The measured INL and DNL of the ADC are shown in Fig. 4.12. The INL/DNL measurement is done by a histogram test with 1 million points. The measured maximum INL and DNL for this work in 'IR×1' mode are 0.32LSB and 0.49LSB, respectively. In 'IR×1.5' mode, the measured maximum INL is 0.39LSB and the measured maximum DNL is 0.50LSB, which is similar to 'IR×1' mode.

Fig. 4.13 shows the measured SNDR versus the input amplitude. By applying the proposed MSB compensation technique, the maximum input of the ADC is improved by around 3 dB and the ADC achieves a dynamic range of 60.64 dB in 'IR×1.5' mode.

Table 4.1 shows the post-layout simulated power dissipation and breakdown of the ADC working in different modes. In measurements, this ADC consumes 18.65 μW at 10 MS/s in 'IR×1.5' mode, which is an increase of 14% compared to the regular 'IR×1' mode where it consumes 16.28 μW. The additional logic only occupies an area of 13 μm^2, which is negligible and can easily fit into the existing design. No extra capacitors are needed.

Table 4.2 summarizes the performance of this work and compares it with state-of-

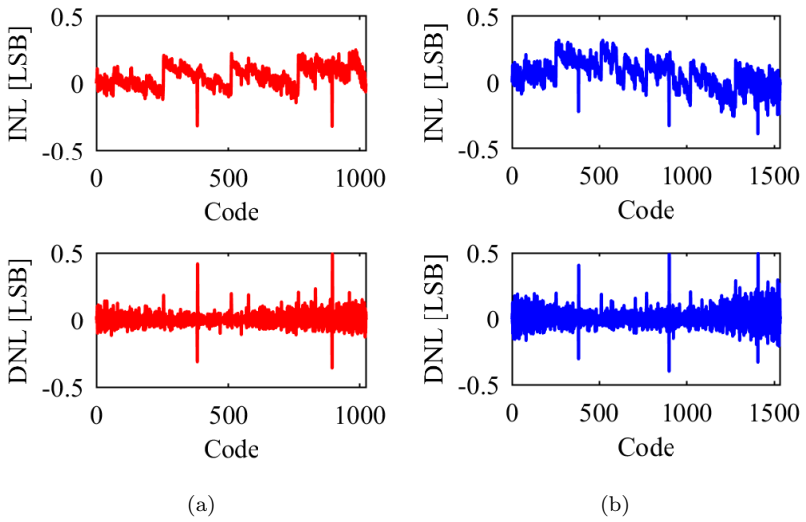


Figure 4.12: Measured INL and DNL in 'IR×1' mode (a) and 'IR×1.5' mode (b).

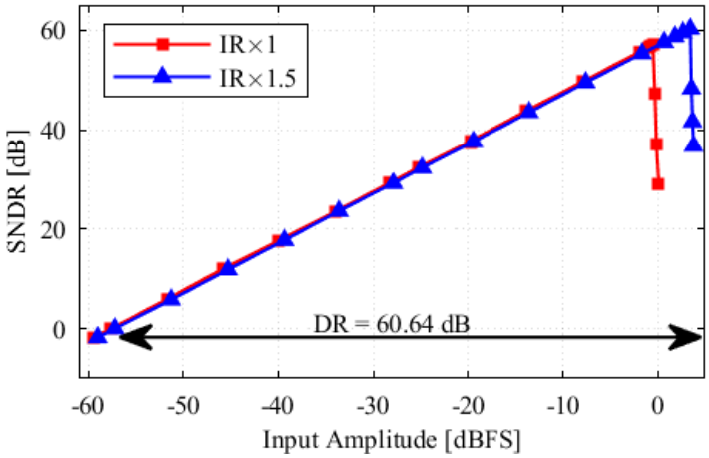


Figure 4.13: Measured SNDR versus input amplitudes.

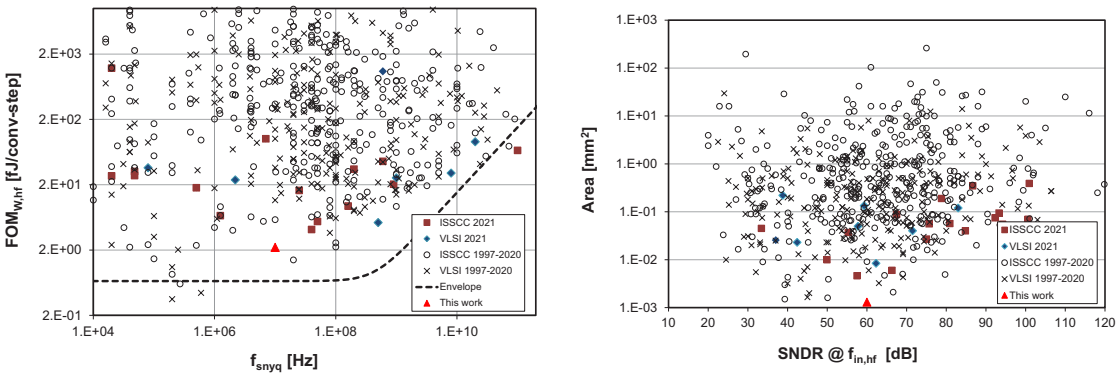
the-art designs. Compared to advanced designs [59,60] with $\pm 2V_{ref}$ input range, only a few logic gates are needed for this work and thus this work is much more area efficient. The supply voltage of this work could be further reduced to save power. Compared to SAR ADCs with similar SNDR and bandwidth (Fig. 4.14), this work achieves state-of-the-art energy efficiency and area efficiency.

4.5 Conclusion

This chapter presents a 10(+0.5) bit 10 MS/s SAR ADC in 65-nm CMOS technology. With the proposed MSB compensation technique, the input range of the ADC is

Table 4.1: Power dissipation and breakdown at 10 MS/s.

	'IR×1'	'IR×1.5'
Comparator	8.8μW	9.68μW
Logic	3.75μW	4.33μW
DAC	2.6μW	3.37μW
T&H	0.92μW	0.92μW
Clock	0.19μW	0.32μW
Total	16.3μW	18.6μW



(a) (b)

Figure 4.14: Benchmark of this work against prior art FOM_W(a) and area (b), data from [26].

improved by a factor of 1.5 while the resolution is improved by 0.5-bit with negligible area cost and 14% power cost. The prototype consumes 18.65 μW at 10 MS/s from a 0.8-V supply voltage and occupies an area of 0.0013 mm^2. The achieved SNDR, SFDR, ENOB are 60.37 dB, 82.2 dB and 9.74-bit, respectively. This results in a FoM_W of 2.2 fJ/conversion-step, which is competitive among state-of-the-art designs. It is also area efficient, which makes it suitable for low-power low-cost applications.

Thanks to the enhanced input range, an ADC can achieve higher resolution with the same noise condition and thus its power efficiency is improved. It is also area efficient since for the same resolution, less hardware is needed.

Similar to the pre-comparison technique described in Chapter 2, the MSB compensation accuracy depends on the duration of T_{pre}. To further enhance the performance for low-to-medium resolution ADCs, a SAR ADC with 2× input range and zero compensation errors will be introduced in Chapter 5.

Table 4.2: Performance summary and comparison

	[60][3]	[59]	[44]	[55]	[61]	[62]	[46]	This work	
Technology [nm]	180	90	65	65	65	20	130	65	
Area [mm^2]	-	0.035	0.026	0.0013	0.046	0.0012	0.052	0.0013	
Supply voltage [V]	0.8	0.3	1	1	1.2	1	1.2	0.8	
Resolution [bit]	10	11	10	10	8	10	10	10	
Sample rate [MS/s]	2	0.6	1	10	90	320	50	10	
Bandwidth [MHz]	1	0.3	0.5	5	11	160	25	5	
Ideal input swing [V_{ref}]	±2	±2	±1	±1	±1	±1	±1	±1	±1.5
Power [μW]	16.07	0.187	1.9	24	806	1520	826	16.28	18.65
ENOB [bit]	9.72	9.46	8.75	9.18	10	9.2	9.18	9.14	9.74
SFDR [dB]	69.35	72.0	-	75.7	72.46	78.1	65.9	82.9	82.2
FoM$_W$ [fJ/conv-step] [1]	9.53	0.44	4.42	4.1	35.8	8.1	28.5	2.9	2.2
FOM$_S$[dB][2]	168.2	180.8	168.6	170.2	163.3	167.4	161.8	167.7	174.7

[1] $FOM_W = Power/(2^{ENOB} \times 2 \times BW)$
[2] $FOM_S = SNDR + 10 \times \log 10(BW/Power)$
[3] Simulated results

Chapter 5

SAR ADC with 2× input range

Similar to what is discussed in Chapter 3, flying capacitor sampling can also be applied to low-to-medium resolution ADCs. Combined with smart DAC switching techniques, the input range of a SAR can be doubled with limited power and area overhead. Compared to the design from Chapter 4, the input range of the ADC can be made twice the original one and the requirement on the pre-comparison timing is relaxed.

The content of this chapter has been published in [19].

5.1 Introduction

In the previous chapter, a 1.5× input range extension technique based on analog prediction was discussed. The resulting area overhead is small by reusing most of the existing hardware. However, a maximum timing duration for prediction is required to ensure accurate compensation, which may increase the required input driving strength.

This chapter presents a SAR ADC with 2× input range adopting a similar principle as [18]. Flying capacitor sampling is used to avoid prediction errors and the equivalent input range is further boosted to 2× without doubling the hardware.

The rest of this chapter is organized as follows: Section 5.2 introduces the proposed input range boosting technique. Its operation and circuit imperfections are discussed. Section 5.3 describes the implementation details of this work. Section 5.4 presents the measured results. Finally, Section 5.5 concludes this chapter.

5.2 Proposed input range boosting technique

5.2.1 Operation

The operation of the proposed input range boosting procedure in different timing phases, together with the timing diagram, is shown in Fig. 5.1. For simplicity, a single-ended diagram is shown. The actual work is implemented in a differential way and the original input range is [-V_{ref}, V_{ref}]. Instead of the conventional top plate sampling, the input signal is now sampled via a sampling capacitor C_S with two sampling switches S_1 and S_2.

During the tracking phase, both S_1 and S_2 are closed. The top plate of C_S tracks the input. The bottom plate of C_S and the top plate of C_{DAC} are connected to a common mode voltage (V_{CM}). Here, C_{DAC} represents the regular binary-scaled DAC capacitor array. Then, V_{in} is sampled on C_S at the falling edge of φ_1, and the pre-comparison phase starts. During this phase, a comparison is done to detect the input signal polarity and the bottom plate of C_{DAC} will be set to D_{pre}. For $V_{in} > 0V$, D_{pre} equals to D_{ref}. For $V_{in} < 0V$, D_{pre} is assigned to D_{-ref}. Here, D_{ref} and D_{-ref} are the codes corresponding to V_{ref} and -V_{ref}, respectively. Then, S_2 is opened at the falling edge of φ_2. After that, the bottom plate of C_{DAC} is set to D_{zero}, which is the code in the reset mode. Due to the voltage shift caused by the DAC, the signal at the comparator input will be either shifted up or down by V_{ref}. As a result, an input range of [-2V_{ref}, 2V_{ref}] can be compressed to the nominal ADC range of [-V_{ref}, V_{ref}] thanks to this pre-comparison and compensation step. Fig. 5.2 shows a conceptual

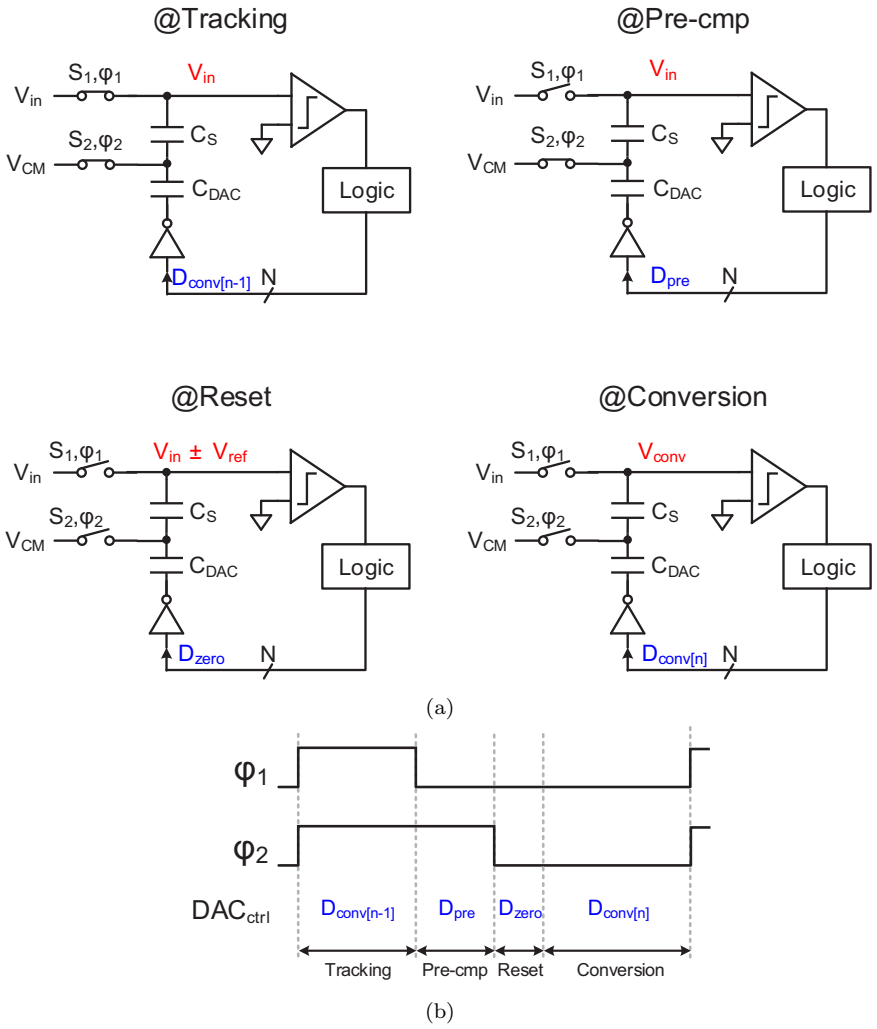


Figure 5.1: Operation of the proposed input range boosting technique (a) and timing diagram (b).

diagram of the resulting output code versus input signal with the proposed input range boosting technique.

5.2.2 Non-idealities

Sampling noise

By sampling the input signal with a flying-capacitor, the sampling noise power of the differential converter is now calculated as:

$$\frac{2kT}{C_S} + \frac{2kT}{C_{DAC}} \tag{5.1}$$

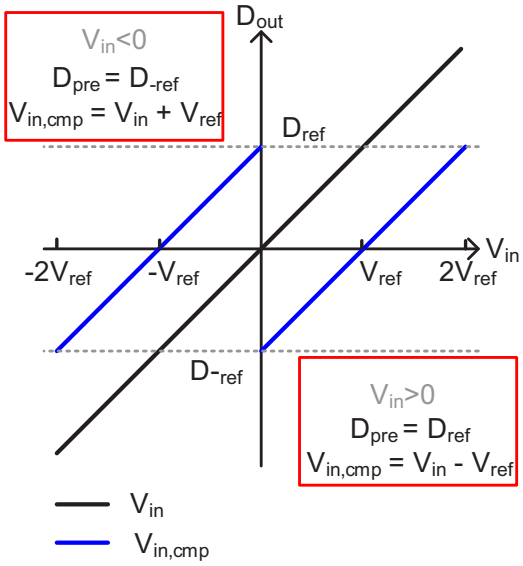


Figure 5.2: Conceptual diagram of the output code with the proposed technique.

which is $\frac{C_S+C_{DAC}}{C_S}$ times larger than the original sampling noise ($2kT/C_{DAC}$). A larger C_S helps to reduce this overhead. Fortunately, C_S is not that sensitive to mismatch and thus can be implemented in an area-efficient way.

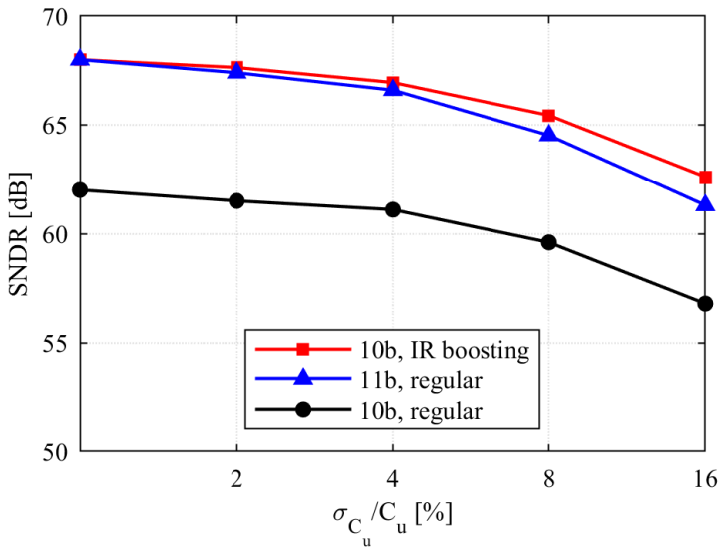


Figure 5.3: Simulated SNDR with DAC mismatch. Here, σ_{C_u}/C_u is the standard deviation of the unit capacitance divided by the unit capacitance, which represents the capacitor mismatch level.

Mismatch

The matching of C_S does not matter for the ADC performance, since it affects all voltage steps in the same way, and thus linearity is maintained. However, the matching of the C_{DAC} capacitors is critical. Fig. 5.3 shows the simulated SNDR of a 10-bit SAR ADC with the proposed input range boosting technique, a regular 11-bit SAR ADC and a regular 10-bit SAR ADC with DAC mismatch. Each point is obtained by 1000 Monte Carlo simulations. As can be seen, with the proposed technique, the SNDR of a SAR ADC can be improved by 6 dB. What's more, compared to a conventional 11-bit SAR ADC, it can achieve slightly better SNDR with 50% less DAC area, because there are less elements (and thus less errors) involved in the DAC operation.

5.3 Circuit implementation

5.3.1 Overview

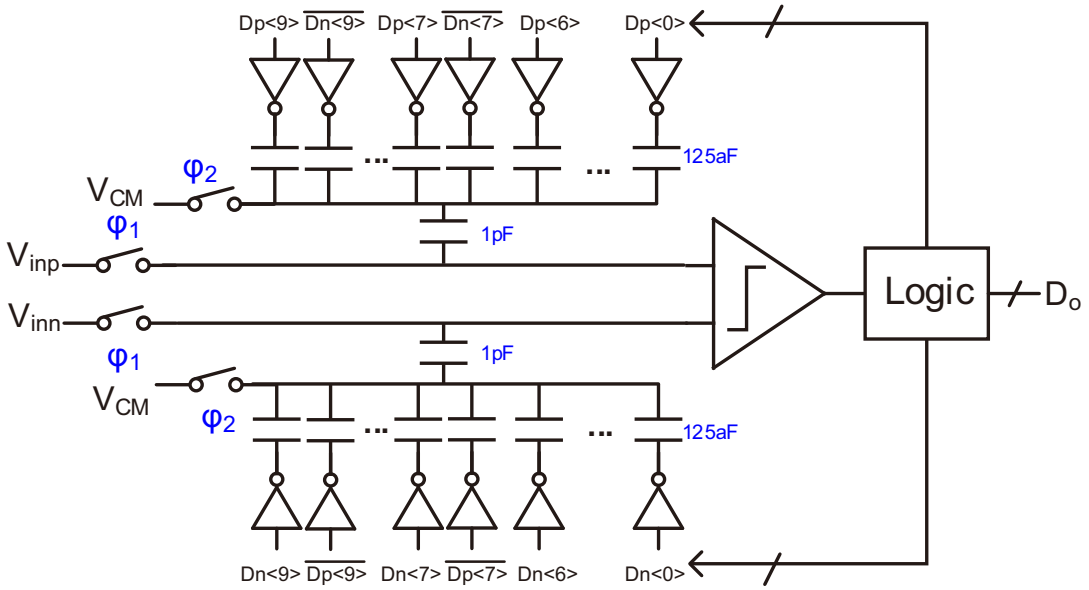


Figure 5.4: Schematic of the SAR ADC with input range extension.

Fig. 5.4 shows the schematic and main design parameters of this work. For the track and hold (T&H) circuit, a 1 pF sampling capacitor is used. S_1 is implemented as a bootstrapped switch and S_2 is implemented as a clock boosted switch for linearity requirements. For the DAC implementation, the 3 MSBs adopt a split monotonic switching scheme and the remaining LSBs adopt a conventional switching scheme as

a compromise of DAC switching energy and logic energy. The total DAC capacitance is 0.25 pF. Besides, self-synchronized SAR logic [55] and a two-stage dynamic comparator [44] are used. On top of that, the input range boosting logic is integrated.

5.3.2 Logic implementation

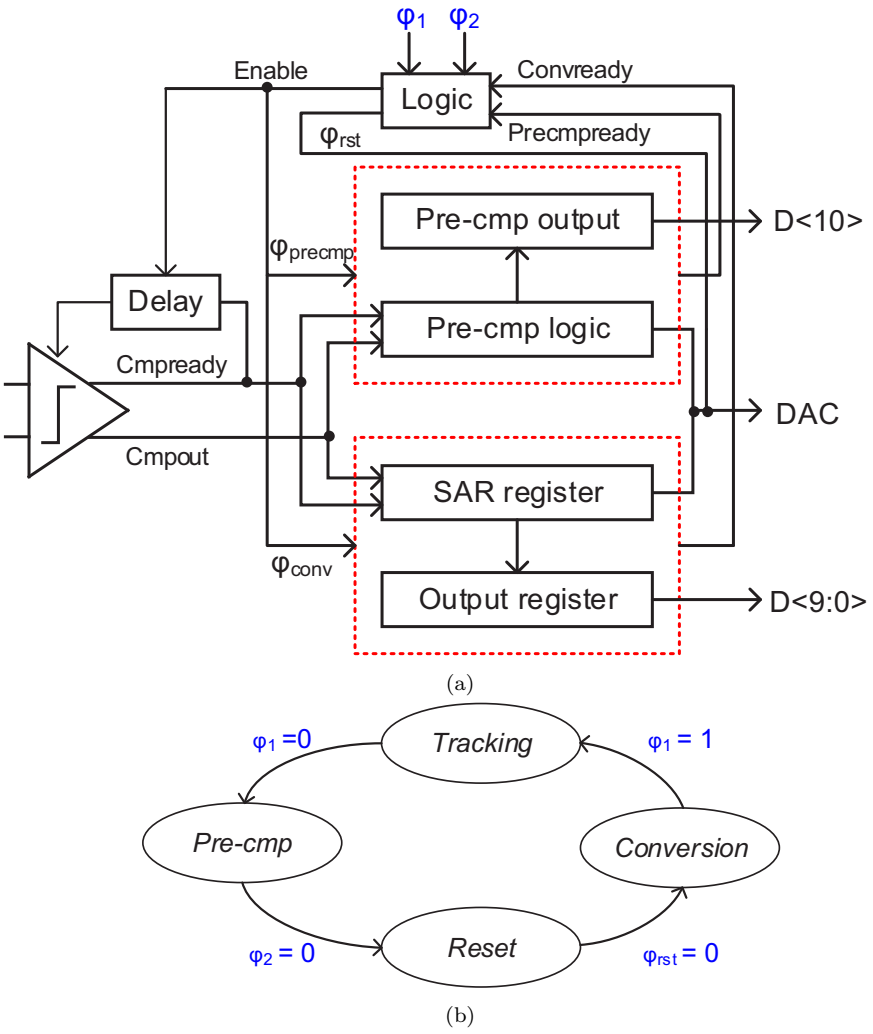


Figure 5.5: The asynchronous logic used in this converter (a) and a simplified state machine (b).

An overview of the asynchronous logic used in this converter, as well as a simplified state machine, are shown in Fig. 5.5. The clocks signals of φ_1 and φ_2 are provided externally. The other clock phases are generated internally. As shown in Fig. 5.5(b), a falling edge of φ_1 will move the ADC from the tracking state to the pre-cmp state. Here, the DAC is controlled by the pre-cmp logic. A falling edge of φ_2 will move the ADC from the pre-cmp state to the reset state, where the DAC is reset. A falling edge of the reset phase, which is generated by an internal delay, will move the ADC

from the reset state to the SAR conversion state, where the DAC is controlled by the SAR register. The circuit operation of each state is as explained in Section 5.2.1.

5.3.3 Layout implementation

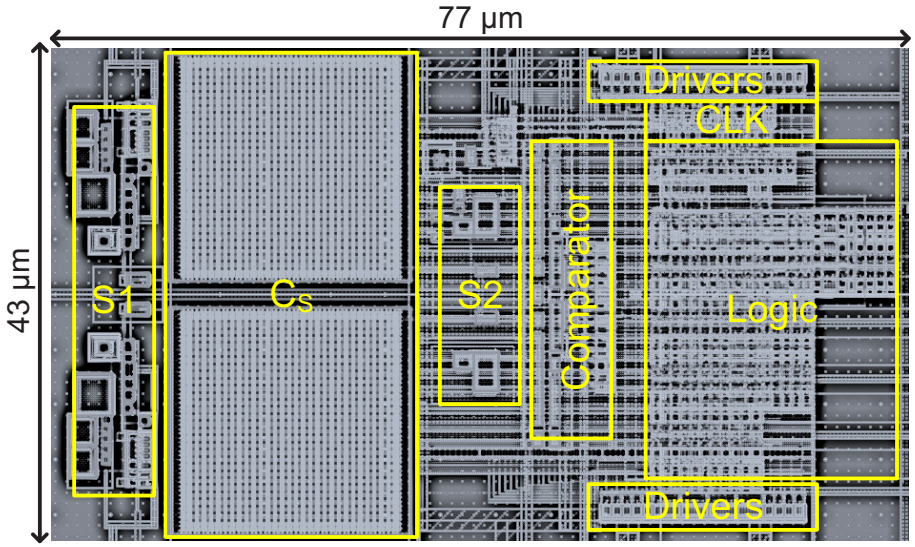


Figure 5.6: Layout view in 65nm CMOS (up to metal 3).

The overall layout design is shown in Fig. 5.6. Since the capacitors occupy most of the area, their implementation is the most important consideration in terms of layout design. In this work, the sampling capacitor C_S is implemented by regular MOM capacitors from the library. The DAC capacitors are implemented by custom designed unit-length capacitors proposed in [55]. To further save area, the DAC capacitors are placed on the top of the ADC circuity (Metal 6 and 7) and vertically connected to the drivers, as shown in Fig. 4.9.

5.4 Measurement results

The prototype ADC is fabricated in 65 nm CMOS and occupies an area of 0.0033 mm^2. Fig. 5.7 shows its die micrograph. It is operated from a 1 V supply voltage. The V_{CM} voltage is set to 0.5 V in measurements, but its accuracy does not affect the overall performance.

Fig. 5.8 shows the measured spectra with the regular SAR mode ('IR×1') and with the proposed input range boosting mode ('IR×2'), respectively. They are measured with a near-bandwidth input and a 10 MHz sampling rate. The measured ENOB is

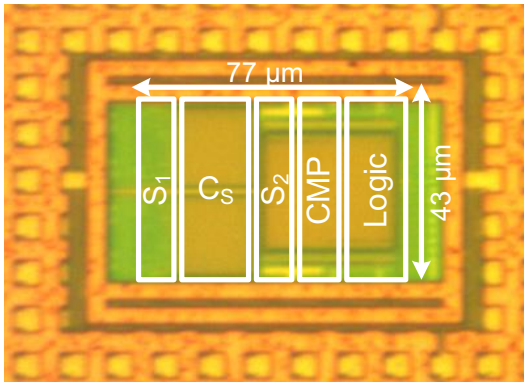


Figure 5.7: Chip micrograph.

9 bit for this prototype at 'IR×1' mode, where the maximum input signal power is -0.32 dBFS. With input range boosting, the maximum input signal power is improved to 5.72 dBFS and the measured ENOB is improved to 10.04 bit. The measured INL and DNL without and with input range boosting are shown in Fig. 5.9, using a 1 million points histogram test.

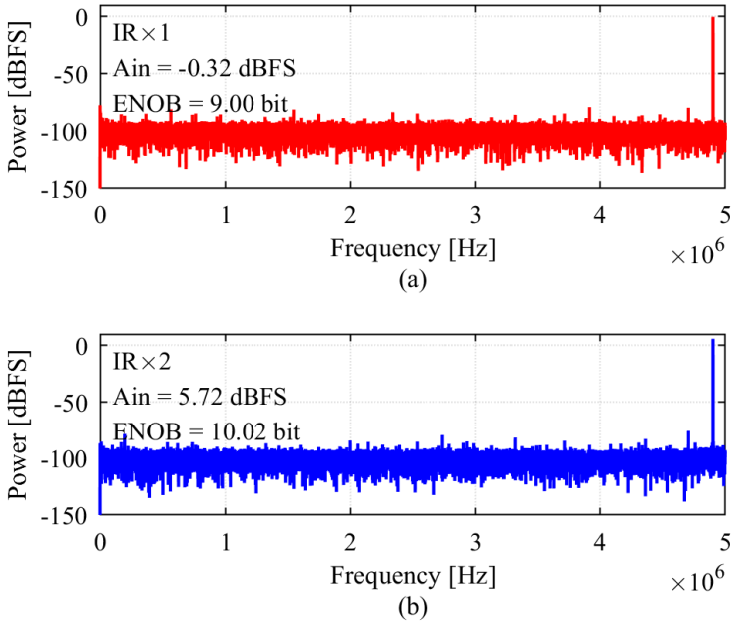
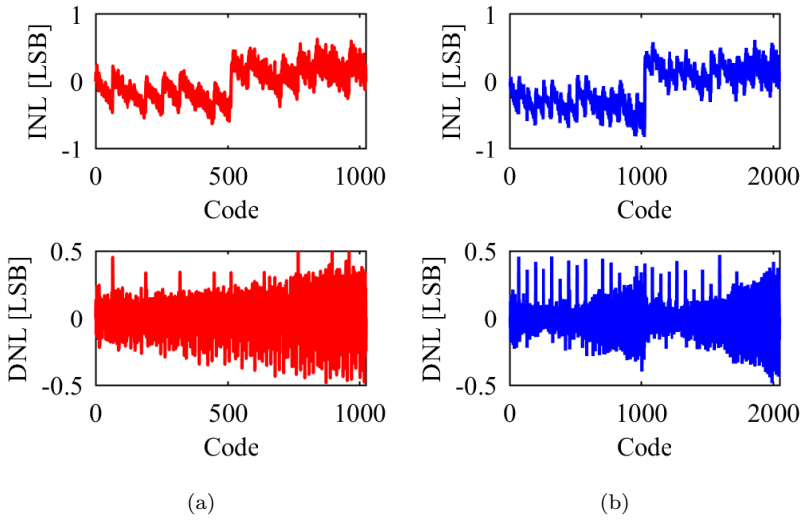


Figure 5.8: Measured spectra without (a) and with (b) 2× input range boosting.

Fig. 5.10 shows the measured SNDR for both operation modes as a function of input amplitude. The measured DR is 56 dB for 'IR×1' mode and 62.1 dB for 'IR×2' Mode. As can be seen, the maximum input amplitude as well as the DR are improved by 6 dB with the proposed input range boosting technique.

Fig. 5.11 shows the power breakdown of this prototype at 10 MHz sampling rate without and with input range boosting. The total power consumption with input



(a) (b)

Figure 5.9: Measured INL and DNL without (a) and with (b) input range boosting.

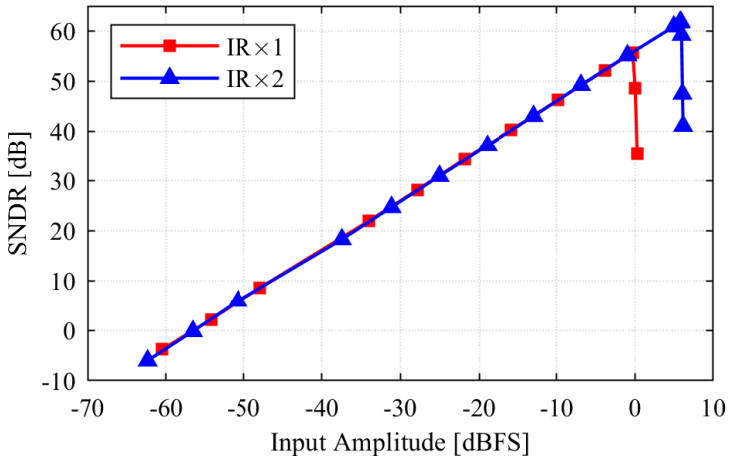


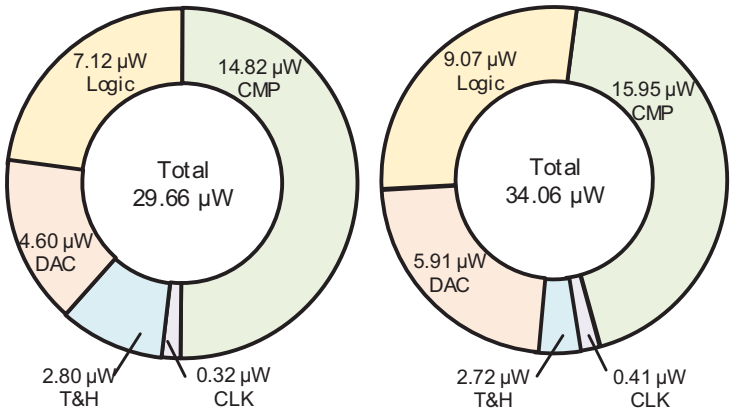
Figure 5.10: Measured SNDR versus input amplitudes.

range boosting is 34.06 μW, which is 14.8% more compared to its regular SAR mode.

Finally, table 5.1 summarizes the performance of this ADC and compares it with other designs. Compared to [59] with 2× input range, this work is 11× smaller. Compared to other state-of-the-art designs, this work achieves comparable energy-efficiency and area efficiency with 2× input range.

5.5 Conclusion

This chapter presents a SAR ADC with an input range boosting technique. With input range boosting, N-bit hardware can be used to realize N+1 bit resolution, which



(a) (b)

Figure 5.11: Power breakdown without (a) and with (b) 2× input range boosting.

Table 5.1: Performance summary and comparison

	[59]	[18]	[55]	This work	
Technology [nm]	90	65	65	65	
Area [mm^2]	0.035	0.0013	0.0013	0.0033	
Supply voltage [V]	0.3	0.8	1	1	
Resolution [bit]	11	10	10	10	
Sample rate [MS/s]	0.6	10	10	10	
Bandwidth [MHz]	0.3	5	5	5	
Ideal input swing [V_{ref}]	±2	±1.5	±1	±1	±2
Power [μW]	0.187	18.65	24	29.66	34.06
ENOB [bit]	10	9.74	9.18	9.00	10.04
SFDR [dB]	72.0	82.2	72.46	76.3	83.3
FoM$_W$ [fJ/conv-step] [1]	0.44	2.2	4.1	5.79	3.28

[1] $FOM_W = Power/(2^{ENOB} \times 2 \times BW)$

improves the area efficiency. Also, the absolute noise requirement is relaxed, which improves the power efficiency. The prototype fabricated in 65 nm CMOS occupies an area of 0.0033 mm^2 and consumes 34.06 μW at 10 MHz sampling rate. The measured SNDR is 62.1 dB and the SFDR is 83.3 dB, resulting in a Walden figure of merit of 3.28 fJ/conversion. These features make it suitable for applications where power and area efficient ADCs are desired.

Compared to the design in Chapter 4, analog detection instead of prediction is used. Without prediction errors, the input range of the SAR ADC can be boosted further.

Similar to what was discussed in Chapter 3, extra switches and a capacitor C_S are required. For low-to-medium resolution ADCs, the resulting power and area overhead are relatively large (17% and 114%, respectively). A larger C_S requires more power from the input driver but the pre-comparison phase timing constraint is avoided.

Both designs achieve high energy efficiency. For applications where area is critical, the design in Chapter 4 is more suitable. For applications where a larger input range is preferred, the design in this chapter can achieve a more aggressive input range boosting.

Chapter 6

Temperature sensor with on-chip offset and gain correction

Temperature sensors are widely used in many electronic devices and control systems. To overcome the output variation caused by process corners and random mismatch, correction is usually needed and is done off-chip in most scientific publications. However, when integrated on-chip, it may lead to even more power and area cost than the sensor itself. In this chapter, efficient on-chip offset and gain correction techniques for temperature sensors used in low-power systems are discussed. By shifting the reset phase of the N-bit ADC, offset correction with a range of $\pm 2^{(N-1)} LSB$ is realized. Fine tuning capacitors are introduced to improve the offset correction accuracy to 0.5LSB. By adding programmable parasitic capacitors, gain errors up to 6.3% can be compensated with a correction accuracy of 0.8%. Thanks to the proposed analog correction techniques, the offset and gain corrections of a dynamic resistive sensor can be integrated with minor overhead in area and power.

The content of this chapter has been published in [20].

6.1 Introduction

Nowadays, temperature sensors are used in a wide range of applications such as IoT, biomedical and environmental monitoring systems. For these applications, moderate-resolution temperature sensors are needed. As mentioned in Section 1.1, a key trend for these applications is miniaturization. Hence, small area ICs are desired. More importantly, they should be ultra-low power so that small batteries can be used.

One challenge for temperature sensors is that they are sensitive to mismatch and process corners, which could result in significant offset and gain variations chip to chip. Also, they usually suffer from non-linearity errors. Offset, and to a lesser extent gain errors, are mostly determined by random mismatch and thus individual correction is needed. For non-linearity errors, it is often a more systematic problem (dependent on the implementation) and might be addressed with a batch-level correction [63]. In this chapter, offset and gain correction will be discussed first while non-linearity correction will be discussed in the next chapter.

The temperature sensor is an analog circuit and its power consumption scales up exponentially with resolution. Depending on the implementation, its area also tends to increase rapidly with resolution as it is an analog circuit. On the other hand, the correction can be implemented with a predominantly digital function, which will consequently scale less rapidly as function of resolution. As a result, for high-resolution sensor interfaces, digital correction is affordable, but for low-to-medium resolution sensor interfaces, digital correction is relatively expensive. While the power consumption of temperature sensors can be reduced already to the pW-level [5], the digital corrections are usually done off-chip in most scientific publications. When integrated on-chip, digital correction may consume more power and area than the sensor itself [64]. Thus, low-power analog correction methods are preferred, at least for low to medium resolution sensors.

To address the above issue, [65,66] use a Wheatstone bridge as the sensing element and add trimming resistors to compensate for the spread of the resistors. Reference [13] uses an accurate electrothermal filter based sensor to calibrate an inaccurate but efficient Wien-bridge based sensor. However, these sensors aim for high precision, and their energy per conversion (6.45 to 790 nJ) and area (0.12 to 0.43 mm^2) are relatively large. For very small, low power sensors (e.g [67] with 2.18 pJ/conversion and 0.0017 mm^2), it is even more challenging to efficiently implement on-chip correction.

The goal of this work is to implement on-chip offset and gain corrections for temperature sensors used in low power systems. A dynamic resistive temperature sensor with integrated analog correction techniques is proposed. By shifting the reset phase of the readout ADC and adding tunable capacitors, the gain and offset errors of the temperature sensor are corrected with limited area and power cost. The final sensor dissipates 2.74 pJ per conversion and only occupies an area of 0.0018 mm^2 including the on-chip gain and offset correction.

The rest of this chapter is organized as follows. Section 6.2 reviews the architecture of a resistive sensor and analyses its gain and offset errors. Section 6.3 reviews the correction procedure. Section 6.4 presents the proposed analog gain and offset correction techniques. Section 6.5 introduces the circuit implementation details. Measured results are shown in Section 6.6 and conclusions are drawn in Section 6.7.

6.2 Review of a resistive temperature sensor

6.2.1 Architecture

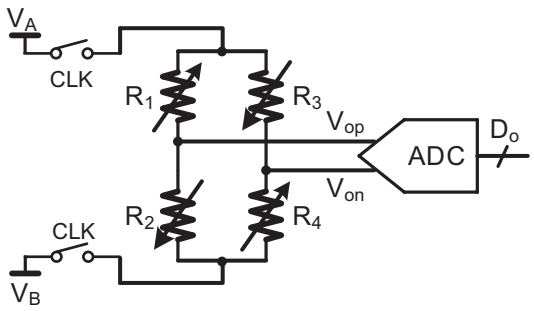


Figure 6.1: A simplified model of a dynamic resistive temperature sensor.

Fig. 6.1 shows a simplified model of a resistive temperature sensor which consists of a Wheatstone bridge sensing front-end and an ADC back-end [68]. The differential output of the resistive bridge can be calculated as:

$$V_{out} = V_{op} - V_{on} = \left(\frac{R_2(1+\alpha_2\Delta T)}{R_1(1+\alpha_1\Delta T) + R_2(1+\alpha_2\Delta T)} - \frac{R_4(1+\alpha_1\Delta T)}{R_4(1+\alpha_1\Delta T) + R_3(1+\alpha_2\Delta T)} \right)(V_A - V_B) \tag{6.1}$$

Here, resistor 1 and 4 are resistors with a temperature coefficient α_1 and a resistance of R_1 and R_4. Resistor 2 and 3 are resistors with a temperature coefficient α_2 and a resistance of R_2 and R_3. When $R_1 = R_2 = R_3 = R_4$, V_{out} only depends on the resistor temperature coefficients and the temperature.

An ADC is used to read out the output of the resistor bridge. The overall gain (code range/temperature range) of the sensor can then be calculated as:

$$gain = gain_{WhB} \times gain_{ADC} \tag{6.2}$$

Here, $gain_{WhB}$ is defined as the output voltage range of the Wheatstone bridge divided by the temperature range and $gain_{ADC}$ is defined as the output code range divided by the input voltage range.

The overall offset of the sensor is equal to:

$$offset = offset_{WhB} + offset_{ADC} \tag{6.3}$$

Here, $offset_{WhB}$ represents the offset of the Wheatstone bridge, and $offset_{ADC}$ represents the input-referred offset of the ADC.

Based on the system of Fig. 6.1, a system-level correlated double sampling (CDS) can be introduced, to mitigate 1/f noise. This can be implemented by swapping the supply voltages of the resistive bridge (V_A,V_B) [68], as will be shown later in Fig. 6.5.

6.2.2 Analysis of offset and gain errors

Due to process corners and random errors, resistors suffer from mismatch. This results in gain and offset errors for the output of the resistive bridge [63].

Assume R_1, R_2, R_3, R_4 have relative errors of e_1, e_2, e_3, e_4, respectively, then (6.1) can be rewritten as:

$$V_{out} = \frac{A}{B}(V_A - V_B) \tag{6.4}$$

where,

$$\begin{aligned} A = {} & (e_2 + e_3 - e_1 - e_4) + 2(\alpha_2 - \alpha_1)\Delta T \\ & + (e_2\alpha_2 + e_3\alpha_2 - e_1\alpha_1 - e_4\alpha_1)\Delta T + H.O.T \end{aligned} \tag{6.5}$$

$$B = 4 + 2(e_2 + e_3 + e_1 + e_4) + 2(e_2\alpha_2 + e_3\alpha_2 + e_1\alpha_1 + e_4\alpha_1)\Delta T + H.O.T \tag{6.6}$$

since both e and α are relatively small, this is approximately:

$$V_{out} \approx \left(Off + \frac{1}{2}(\alpha_2 - \alpha_1)\Delta T + Gain_{err}\Delta T \right)(V_A - V_B) \tag{6.7}$$

where,

$$Off = \frac{1}{4}(e_2 + e_3 - e_1 - e_4) \tag{6.8}$$

$$Gain_{err} = \frac{1}{4}(e_2\alpha_2 + e_3\alpha_2 - e_1\alpha_1 - e_4\alpha_1) \tag{6.9}$$

The offset (Off) is directly related to the resistance error. Assume that α is in the order of $2e^{-3}$ and the temperature range is about 140 °C, when e_1 is in the order of 10%, this could result in a 3σ error similar to the full-scale range. The gain error ($Gain_{err}$) is related to the derivative of the resistance versus temperature. The gain variation will be a secondary effect as (6.9) shows, as both e and α are small.

The temperature coefficients also suffer from random variations. Assume that α_1 has a relative error of $e_{\alpha 1}$, then the actual value of R_1 can be expressed as:

$$R_{1,real} = R_1(1 + e_1)\Big(1 + \alpha_1(1 + e_{\alpha 1})\Delta T\Big) \tag{6.10}$$

$e_{\alpha 1}$ only affects R_1 in the order of $e_1 \times \alpha_1 \times e_{\alpha 1}$. Since α and e_α are small, the random variation of α will be less important than the random variation of the resistance.

Besides resistive bridge imperfections, there are also gain and offset errors from the ADC, which affect the final output as equations (6.2) and (6.3) show. The ADC offset is mainly determined by the comparator offset and the ADC gain is determined by the DAC capacitance and parasitic capacitance. However, they trend to be minor factors compared to the relatively large resistive bridge errors.

6.3 Review of correction procedure

Because the offset and gain errors are different for each chip, each individual chip should be measured once to correct the various errors. In general, the offset and gain correction procedure is summarized as follows:

1. For each sample, the output for two pre-defined temperatures (e.g. 0 and 100 °C) will be measured once.
2. With the measured output, offset and gain errors of the sample can be calculated and then the corresponding correction coefficients can be set.
3. For each measurement, the sample's output is corrected with the above fixed correction coefficients.

Overall, step 1 and 2 are done once manually (or via an automated procedure, e.g. in a factory). Step 3 is required continuously and is intended to be integrated on-chip. Because of that, its area and power overhead are relevant.

6.4 Proposed gain and offset correction

According to (6.2) and (6.3), either $gain_{WhB}$ and $Offset_{WhB}$ can be corrected directly [65, 66] or $gain_{ADC}$ and $Offset_{ADC}$ can be tuned to compensate for the gain and offset errors caused by the resistive bridge. In this work, gain and offset correction techniques based on the later option are proposed. Compared to tuning the resistive bridge itself, tuning the ADC's gain and offset is more area efficient thanks to the ability to re-use most of the existing DAC capacitors, and the area efficiency of capacitors in general. On top of this, implementing gain and offset correction in the resistive bridge is more cumbersome. Firstly, because the resistors are relatively large components. Secondly, because adding trimming resistors also adds parasitics, which is disadvantageous in a dynamic structure [68]. Thirdly, because the extra switches in the bridge could cause additional non-linearity.

6.4.1 Regular SAR conversion

A charge redistribution SAR ADC is chosen as the read out back-end thanks to its high efficiency at moderate resolutions [68]. Fig. 6.2(a) shows its timing diagram and the corresponding DAC control signals (DACctrl). During the tracking phase, the DAC control code remains at D_{zero} and the bottom plates of the DAC capacitors are reset to 0. After V_{in} is sampled, a regular SAR conversion starts. When the SAR conversion is completed, the DAC control signals is set to D_{zero} until the next SAR conversion phase comes.

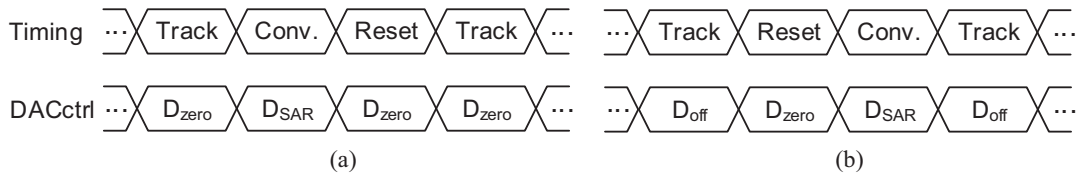


Figure 6.2: Timing diagram and DAC control signals of (a) conventional SAR conversion (b) SAR conversion with the proposed offset correction.

6.4.2 Offset correction

As analyzed in Section 6.2, the offset error caused by the resistive bridge mismatch has a wide spread. To realize such a wide range offset correction, the following offset correction technique is proposed (Fig. 6.3), which is similar to the comparator offset calibration technique proposed in [69] but now being used to correct the sensor's front-end variation with a full code range. Compared to the conventional SAR ADC

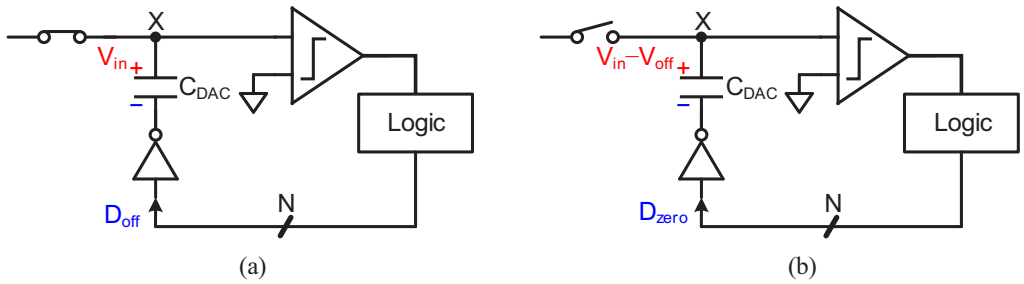


Figure 6.3: Operation of offset correction (a) tracking phase (b) reset phase.

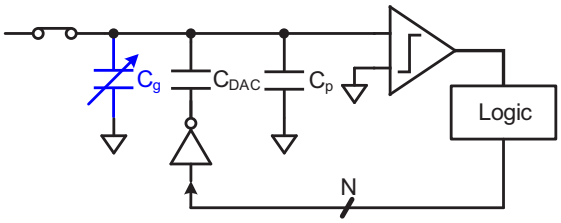


Figure 6.4: Diagram of gain correction in the SAR ADC.

operation, the DAC reset phase is shifted in time, and the DAC is preset to an offset value during tracking (Fig. 6.2(b)).

During the tracking phase, the DAC control code is set to D_{off}, which corresponds to the offset voltage to be compensated (Fig. 6.3(a)). Then, after V_{in} is sampled at the top plates of the DAC capacitors, the bottom plates of the DAC capacitors are reset to 0 by changing the digital control code from D_{off} to D_{zero} (Fig. 6.3(b)). The charge redistribution that takes place effectively subtracts the offset voltage from the input signal. Because node X is floating, the voltage at the comparator input is now equal to $V_{in} - V_{off}$. In this way, an offset correction with a range of $\pm 2^{(N-1)}$LSB can be realized. Here, N stands for the number of bits of the ADC.

6.4.3 Gain correction

Fig. 6.4 shows a diagram of the proposed analog gain correction. With a tunable capacitor C_g, the ADC's gain can be calculated from the original ADC gain as:

$$gain_{ADC,C_g} = \frac{C_{DAC} + C_p + C_g}{C_{DAC} + C_p} \times gain_{ADC} \tag{6.11}$$

where C_{DAC} is the regular DAC capacitors and C_p is the parasitic capacitance. Depending on the estimation of the front-end gain variation, the tunable range of C_g can be chosen accordingly.

6.5 Circuit implementation

6.5.1 Architecture

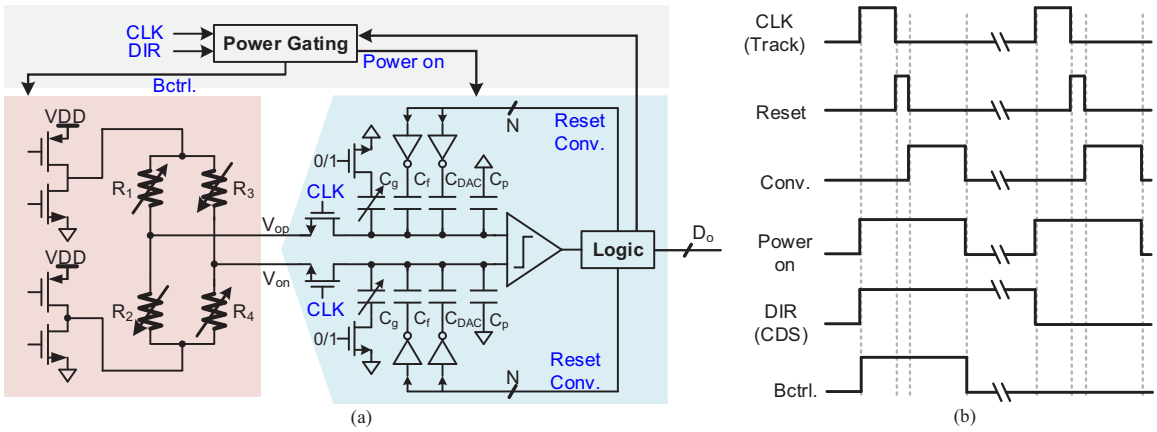


Figure 6.5: Architecture of the sensor (a) and timing diagram (b).

Fig. 6.5(a) shows the architecture of the dynamic resistive sensor, which is based on the design in [67]. Here, resistor 1 and 4 are N-type diffusion resistors with a positive temperature coefficient, while resistor 2 and 3 are P-type polysilicon resistors with a negative temperature coefficient. The nominal value of all resistors is 100 $k\Omega$. This is selected as a trade-off between sensitivity and small area.

A 9-bit asynchronous charge redistribution SAR ADC is used to read out the resistive bridge. NMOS transistors are used as sampling switches. A 2-stage dynamic comparator is used. The DAC cells are implemented as unit-length capacitors placed on top of the active circuits to minimize area cost. The nominal value of the total DAC capacitance is 300 fF.

Besides the sensing front-end and the ADC back-end, an automatic power gating control block is applied to maximize the stand-by time and to minimize the leakage power of the system [67]. Once the conversion is done, a latched signal will be generated and the power supply will be switched off.

The power gating system and the sampling switches of the ADC are driven by a 1-V supply voltage (VDDH). The rest of the circuit is driven by a 0.6-V supply (VDD).

Fig. 6.5(b) shows the timing diagram of the sensor. The sampling clock (CLK) and the direction signal (DIR) are provided externally. The other clock signals are generated internally and included in the power consumption. The DIR signal controls the polarity of the system to implement CDS.

6.5.2 Offset and gain correction

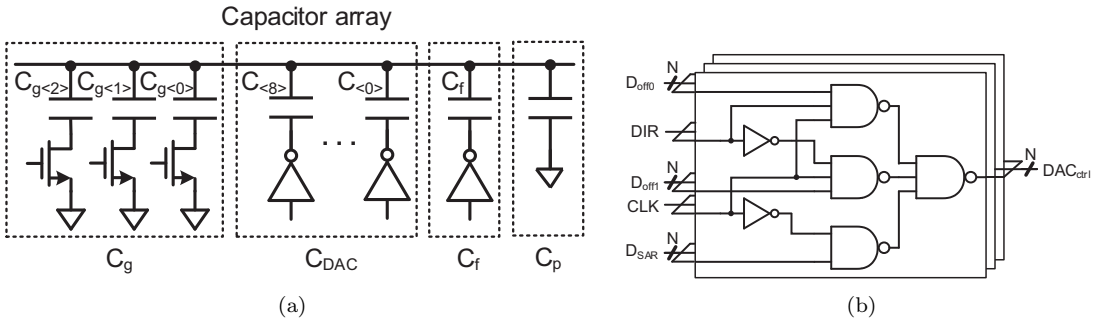


Figure 6.6: Capacitor array (a) and logic cell of the offset correction (b).

The capacitor array implementation of this work is shown in Fig. 6.6(a). Except for the normal DAC capacitors and parasitic capacitance, a 3-bit programmable capacitor C_g is designed to calibrate the gain of the sensor, which can achieve gain correction in a range of 6.3% with a step size of 0.8%. The offset can be corrected in a range of $\pm 2^{(N-1)}$LSB. To enable a step size of 0.5LSB, one additional fine tuning capacitor C_f (with a value of 0.5LSB) is added.

Fig. 6.6(b) shows the design of the logic cell for the proposed offset correction technique. When the CLK signal is high (tracking phase), the DAC drivers are controlled by the pre-set values. Depending on the direction signal (DIR), the corresponding pre-set signal will be chosen. Thus, the bottom plate of the DAC is pre-set to an offset value during the tracking phase. When the CLK signal is low, the DAC follows the output from the SAR logic. The bottom plate of the DAC is firstly switched back to the reset mode and then a normal SAR conversion is performed.

6.6 Measurement results

This work is fabricated in 65-nm CMOS and occupies an area of 0.0018 mm^2 (Fig. 6.7). Supplies of 1-V and 0.6-V are used. 20 samples are measured over a temperature range from -20 to 120 °C. The on-chip gain and offset correction coefficients are set based on 2 measured temperature points (0 and 100 °C).

Fig. 6.8 shows the output codes for 20 samples when the proposed analog correction is enabled and disabled. The measured gain and offset distribution are summarized in Fig. 6.9. When the on-chip correction is disabled, the measured gain has a variation of 6.47% while the offset value varies from 12 to 35LSB. With correction, the gain variation is reduced to 0.73%. The offset values are calibrated to within 0.5LSB from the desired value.

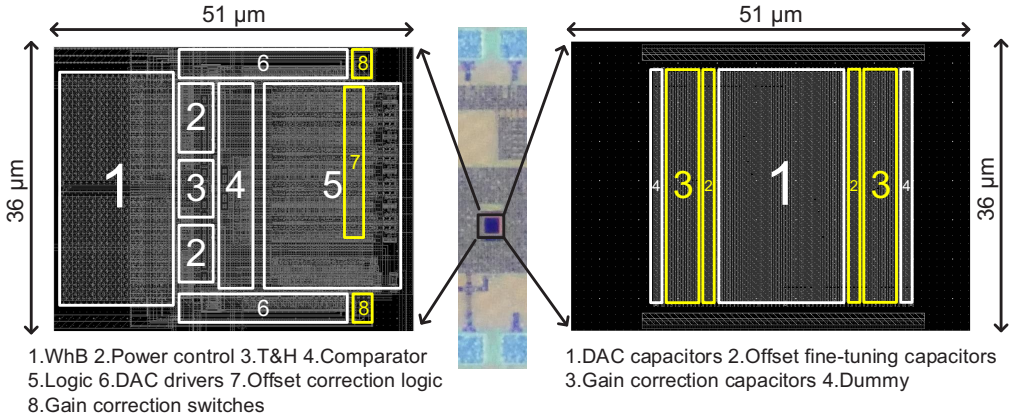
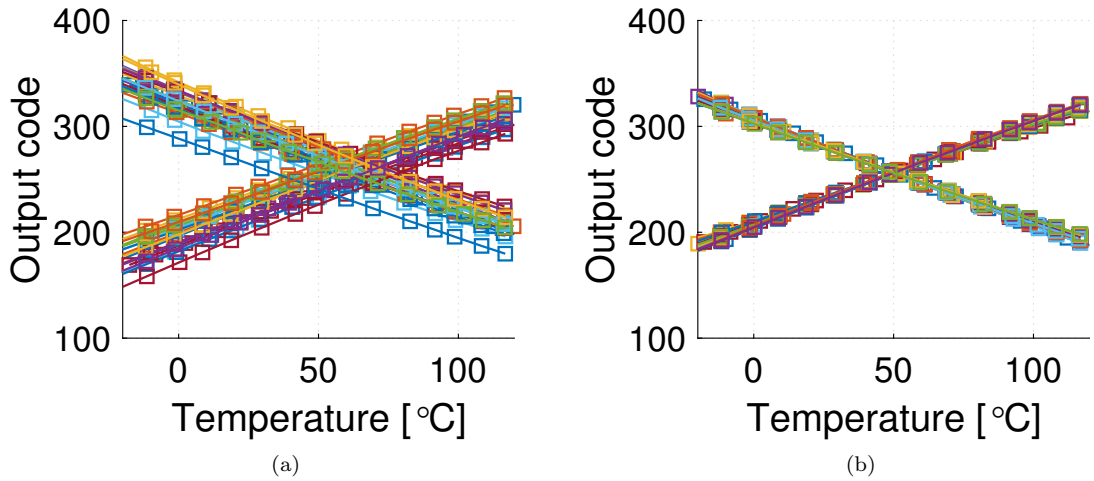


Figure 6.7: Die photo and layout view (left: up to Metal 5; right: Metal 6 and 7).



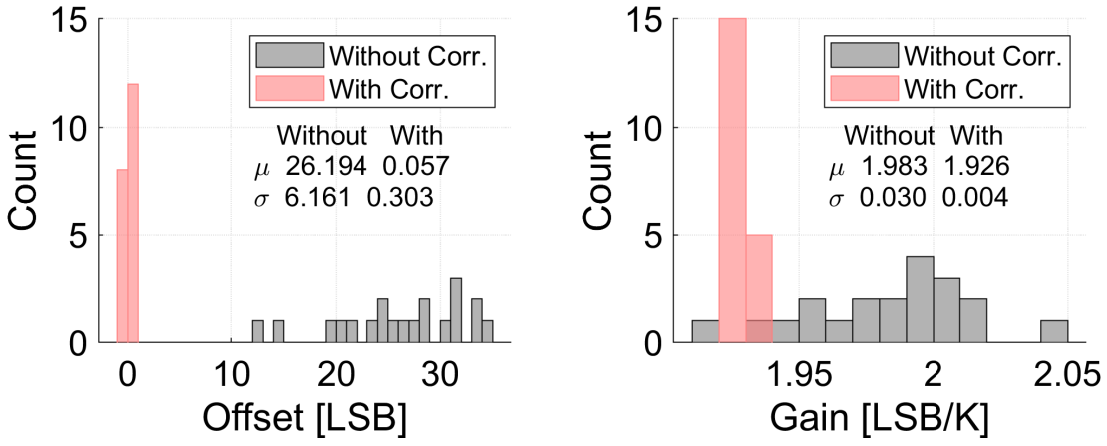
(a) (b)

Figure 6.8: Output code when analog correction is disabled (a) and enabled (b).

Fig. 6.10 shows the temperature error of the sensor with off-chip digital and on-chip analog correction. After digitally removing the systematic non-linearity with a fixed 5th order polynomial batch correction, the residual temperature error can be observed in Fig. 6.11. As can be seen, the analog correction performs at least as well as digital correction and may have a benefit due to better cancellation of ADC mismatch thanks to CDS [70]. This sensor (with on-chip gain/offset correction and off-chip systematic distortion correction) has an inaccuracy of -0.3/0.4 °C, resulting in a relative inaccuracy of 0.5%.

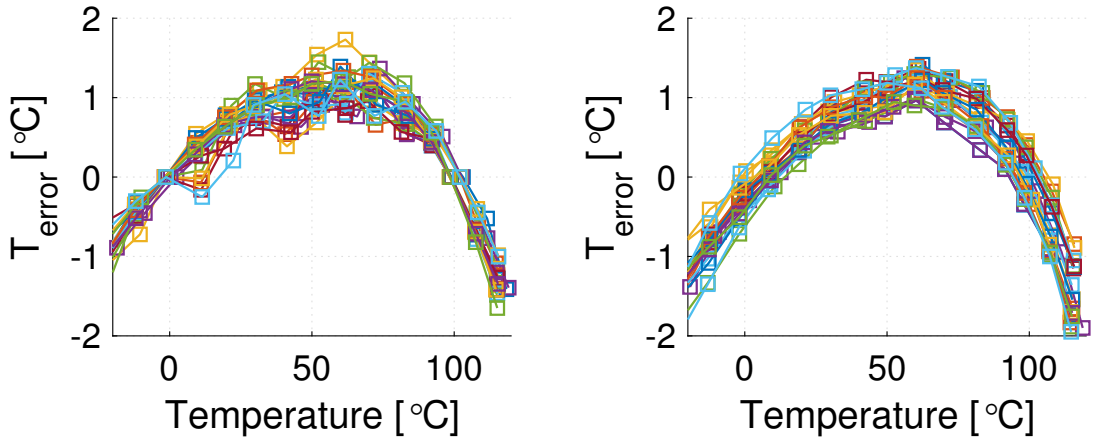
The RMS resolution is 0.471K and 0.473K at room temperature for this sensor with and without correction, respectively. They are similar because the noise contribution is almost the same for both cases.

This temperature sensor consumes 2.62 pJ without correction and 2.74 pJ per conversion with the proposed analog correction techniques with an increase of 4.6%. For both gain and offset correction, the extra capacitors are placed on the top of the existing circuitry. The extra logic only occupies an area of 180 μm^2 (Fig. 6.7). Overall,



(a) (b)

Figure 6.9: Distribution of offset (a) and gain (b), without and with analog correction.



(a) (b)

Figure 6.10: Temperature error with off-chip digital gain/offset correction (a), and with on-chip analog correction (b).

the proposed on-chip offset and gain correction is very area and power efficient.

Table 6.1 summarizes the performance of this work and compares it to state-of-the-art designs. Compared to prior art with on-chip correction techniques [13, 65, 66], this work achieves a competitive resolution FoM with much lower conversion energy and a 67× to 239× smaller area. However, these references aim for much higher precision at higher power levels. Compared to [67], which used off-chip gain and offset calibration, this work integrates these calibrations on-chip at the cost of 11% extra area and 25% extra energy, while achieving better accuracy, resolution, and FoM. Fig. 6.12 shows a benchmark of relative inaccuracy versus area. The relative inaccuracy (in percentage) is defined as 100× the worst case inaccuracy divided by the specified temperature range [5]. Among state-of-the-art designs, this work is the smallest design with a relative inaccuracy $< 0.5\%$. Moreover, the offset and gain correction of this design is implemented on-chip.

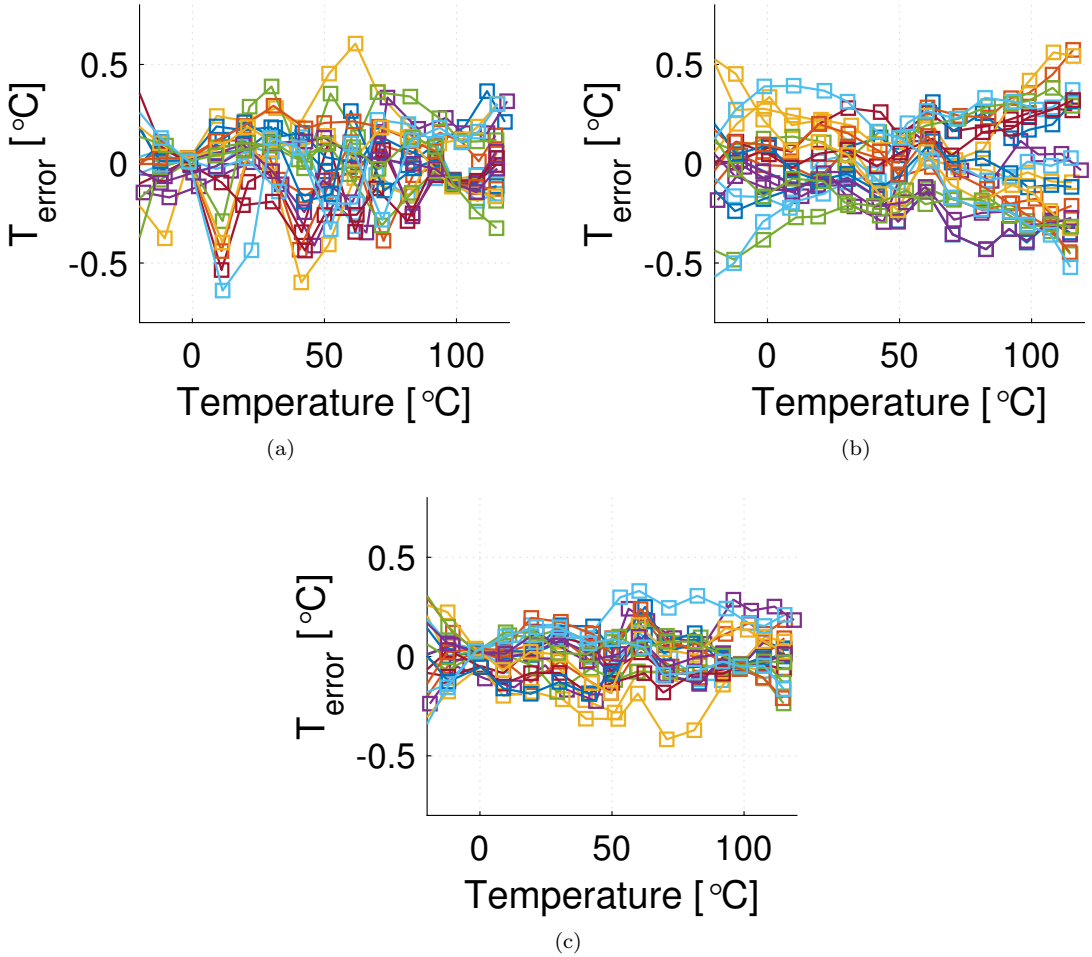


Figure 6.11: Temperature error after fixed systematic error removal with off-chip digital gain/offset correction (a), with on-chip analog correction (b), and with analog correction plus 1^{st} order fit (c).

6.7 Conclusion

This chapter presents an ultra-low power temperature sensor with on-chip gain and offset correction. Thanks to the proposed efficient analog correction techniques, this sensor achieves a full code range offset correction with a step of 0.5LSB and a 6.3% gain correction with a step of 0.8%. The overall design consumes 2.74 pJ conversion energy, uses 0.0018 mm^2 area, and achieves an RMS resolution of 0.47K. This results in a resolution FoM of 0.6 $pJ{\cdot}K^2$.

These results show that even for very small and low power sensors, gain and offset correction can be done on-chip with limited overhead. Moreover, compared to off-chip digital correction, the proposed on-chip analog correction may have a benefit due to better cancellation of INL errors in combination with CDS [70].

As can be seen from Fig. 6.10, systematic non-linearity errors still exist. To also include efficient non-linearity correction on-chip, various techniques will be discussed

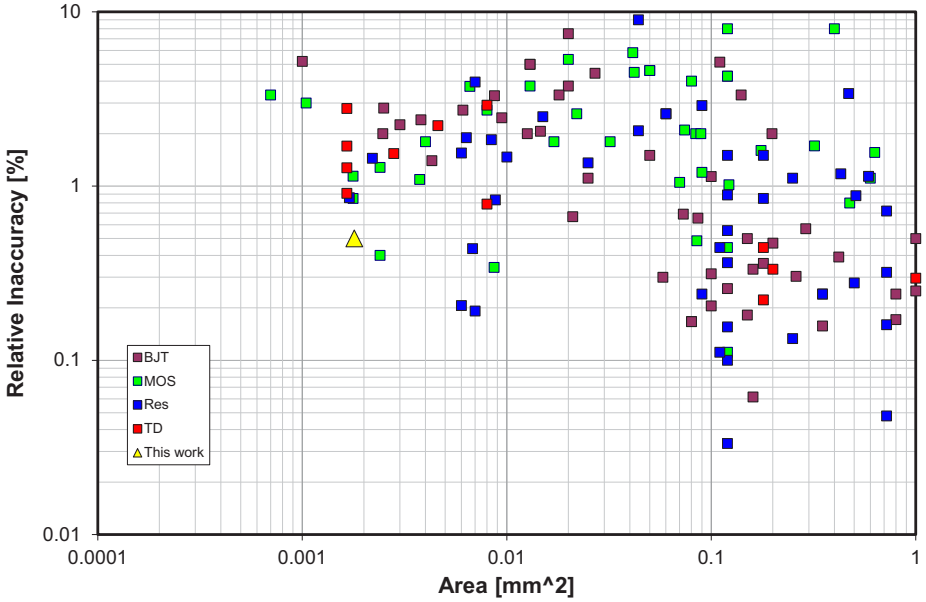


Figure 6.12: Benchmark of this work again state-of-the-art designs, data from [5].

and implemented in Chapter 7.

Table 6.1: Performance summary and comparison

	[65]	[66]	[13]	[67]	[68]	This work
Sensor type	Res	Res	Res	Res	Res	Res
Technology [nm]	180	180	180	65	65	65
Area [mm^2]	0.12	0.43	0.2	0.0017	0.084	0.0018
Supply voltage [V]	1.8	1.5	1.8	1/0.6	1/0.6	1/0.6
Temp. range [°C]	-55 to 125	-45 to 125	-55 to 125	-20 to 120	-10 to 120	-20 to 120
Samples	20	14	20	16	10	20
Inaccuracy (Trimming points) [K]	$\pm 0.14(2^{ac})$	$\pm 0.4(2^{ac})$	$\pm 0.03(2^{ac})$	1.2 (2^{bc})	-0.34/0.29 (2^{bc})	-0.3/0.4 (2^{bc})
Resolution [K]	0.16m	0.01	0.45m	0.53	0.38	0.47
Power [μW]	79	64.5	66	0.108	0.571	0.137
Conversion time [s]	10m	100μ	10m	20.6μ	10μ	20μ
Conversion energy [pJ]	790000	6450	660000	2.18	5.71	2.74
Resolution FoM[1] [pJ·K^2]	0.02	0.65	0.13	0.61	0.82	0.60

[a] 3σ values [b] Maximum values [c] With nonlinearity removal

[1] $FoM = Energy/Conversion \cdot (Resolution)^2$

Chapter 7

Temperature sensor with on-chip non-linearity correction

In this chapter, efficient on-chip non-linearity correction techniques for low-power temperature sensors are discussed. An analog correction method and a digital correction method are proposed and compared. By pre-setting and resetting an auxiliary DAC, the non-linearity error of a resistive temperature sensor can be corrected in the analog domain. Besides, the correction coefficients can be programmed with a bridge capacitor. The non-linearity error can also be corrected with a digital correction with the same correction function and fixed correction coefficients. Both methods can achieve efficient non-linearity correction. The analog method achieves a better precision thanks to its programmable correction coefficients.

The content of this chapter has been published in [21].

7.1 Introduction

As discussed in Section 6.1, WhB temperature sensors suffer from offset, gain error and systematic non-linearity errors (Fig. 7.1). Generally, a 2-point trim and systematic error removal are required, especially for resistors-based sensing front-ends with two types of resistors whose spread is partially uncorrelated. For state-of-the-art WhB temperature sensors [66, 67, 71–73], these corrections are either done off-chip or done on-chip digitally but the power consumption of the digital blocks is not accounted for.

In this chapter, energy-efficient and area-efficient on-chip non-linearity correction techniques will be discussed. An analog method and a digital method are implemented and compared. This chapter is organized as follows. Section 7.2 analyses the non-linearity errors of a dynamic resistive sensor. Section 7.3 introduces the proposed analog correction and digital correction techniques. Their circuit implementation details are shown in Section 7.4. Section 7.5 presents the measured results of the two sensors and finally Section 7.6 concludes this chapter.

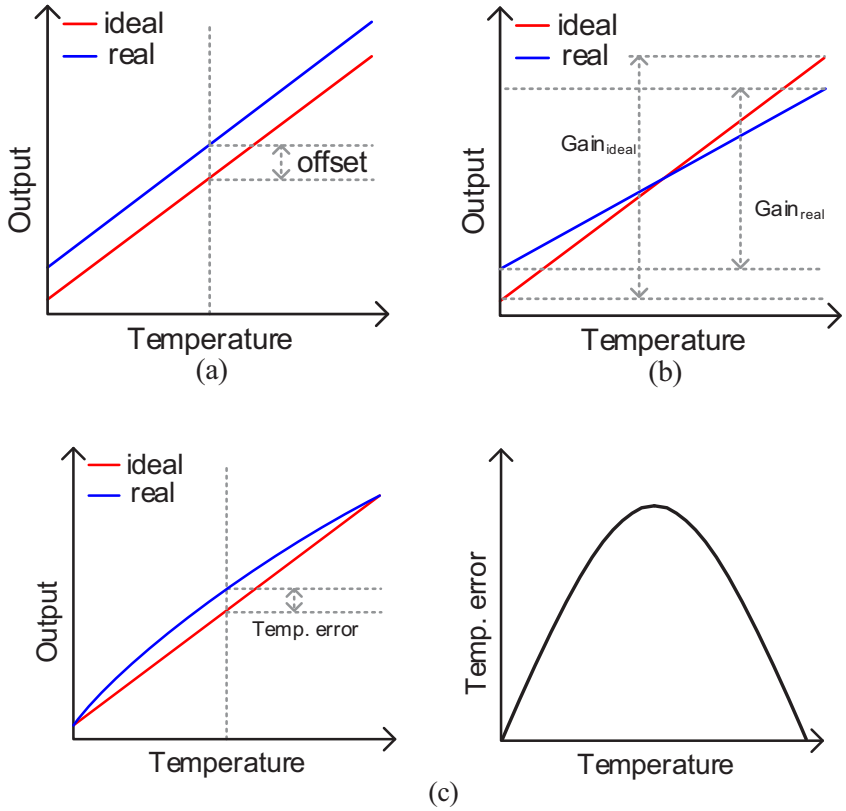


Figure 7.1: Offset, gain and non-linearity errors of a dynamic resistive temperature sensor.

7.2 Analysis of non-linearity errors

As mentioned in section 6.2, the differential output of a WhB temperature sensor can be calculated as (6.1). Ideally, if $R_1 = R_2 = R_3 = R_4 = R$, V_{out} can be simplified as:

$$V_{out} = \frac{(\alpha_2 - \alpha_1)\Delta T}{2 + (\alpha_2 + \alpha_1)\Delta T}(V_A - V_B) \tag{7.1}$$

When $\alpha_1 + \alpha_2 = 0$,

$$V_{out} = \alpha_2 \Delta T(V_A - V_B) \tag{7.2}$$

and thus V_{out} is linearly proportional to the temperature change.

When $\alpha_1 + \alpha_2 \neq 0$, V_{out} is inherently a non-linear function of ΔT.

Assume that $(\alpha_2 + \alpha_1)\Delta T \ll 2$, (7.1) can be approximated as:

$$V_{out} \approx \frac{2(\alpha_2 - \alpha_1)\Delta T - (\alpha_2 + \alpha_1)(\alpha_2 - \alpha_1)(\Delta T)^2}{4}(V_A - V_B) \tag{7.3}$$

This mostly second-order distortion is the dominant non-linearity source.

Besides, α is also temperature dependent. Assume that $\alpha_2 = \alpha_{2,0} + \alpha_{2,0}\alpha_{\Delta T2}\Delta T$, (7.2) can be rewritten as:

$$V_{out} = \alpha_{2,0}\Delta T(V_A - V_B) + \alpha_{2,0}\alpha_{\Delta T2}\Delta T^2(V_A - V_B) \tag{7.4}$$

which also results in a second-order distortion but in the order of $\alpha_{2,0}\alpha_{\Delta T2}$. Here, $\alpha_{\Delta T2}$ is the temperature-dependent coefficient of α_2.

Besides, the read-out ADC also suffers from non-linearities (e.g. DAC mismatch). Since the ADC has a differential input, its second-order distortion is canceled. Other distortions are typically relatively minor factors compared to the second-order distortion caused by α as described in (7.3).

While offset and gain errors are randomly distributed for each sample and thus require individual correction, non-linearity errors are more systematic within a batch of samples and could be corrected with batch-level characterization [74]. As conceptually shown in Fig. 7.2, this correction can either be generated in the analog domain before the AD conversion or in the digital domain after the AD conversion. In the following sections, the two methods based on a dynamic WhB temperature sensor will be discussed and compared.

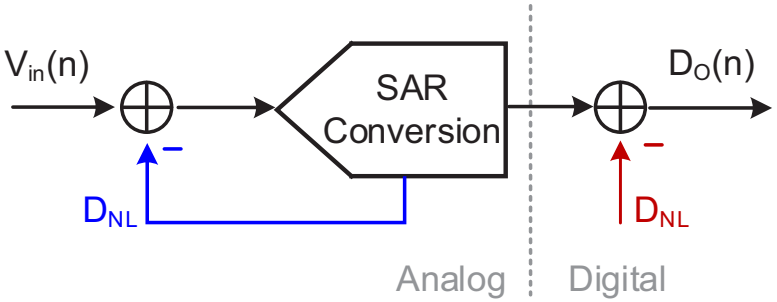


Figure 7.2: Two methods to correct the non-linearity error of a dynamic resistive temperature sensor.

7.3 Proposed non-linearity correction techniques

7.3.1 Proposed analog non-linearity correction

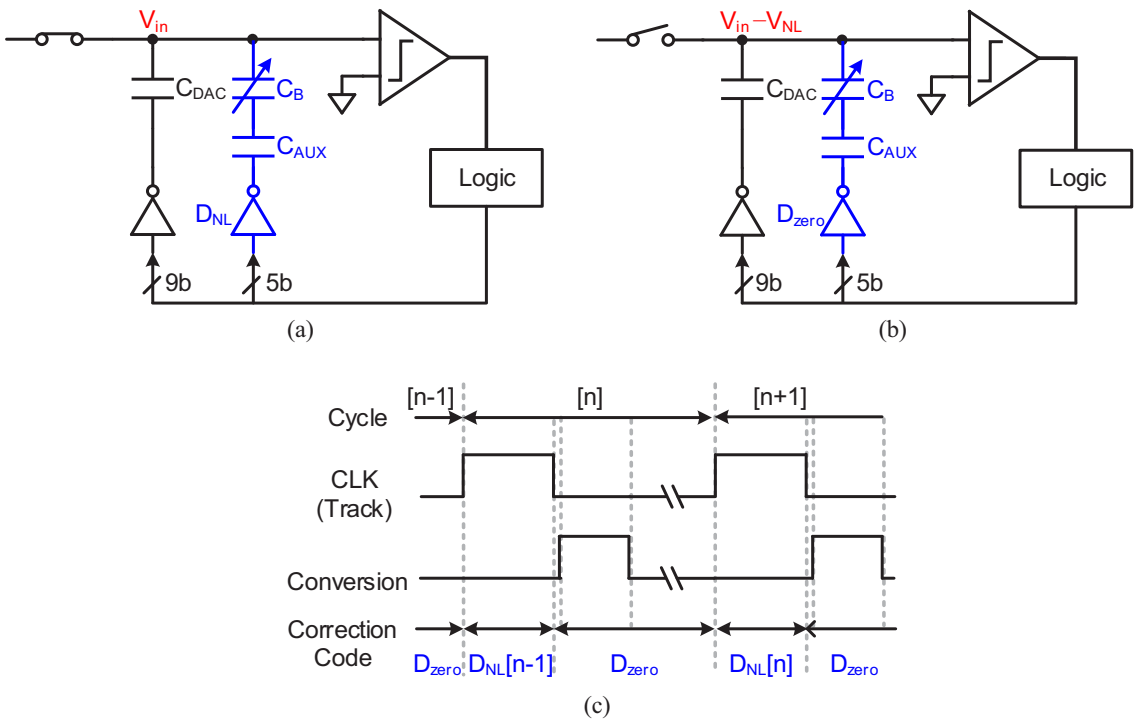
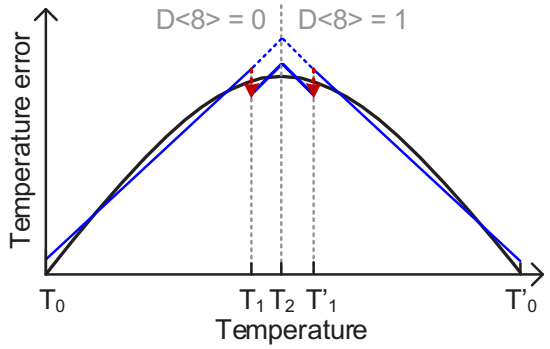


Figure 7.3: Operation of the proposed non-linearity correction, (a) tracking phase, (b) reset phase and (c) timing diagram.

Fig. 7.3 shows the operation of the proposed analog non-linearity correction. A fixed 5-bit C_{AUX} capacitor array, controlled by a digital correction function, creates an approximation $f(x)$ of a second-order function. A programmable capacitor C_B is placed in series, with which the magnitude of $f(x)$ can be adjusted. During the



$$f(x) = \begin{cases} ax, & x \in [T_0, T_1] \\ ax - b, & x \in (T_1, T_2] \\ a\overline{x} - b, & x \in (T_2, T_1'] \\ a\overline{x}, & x \in (T_1', T_0'] \end{cases}$$

Figure 7.4: The used piecewise linear approximation function.

tracking phase, the C_{AUX} capacitors are pre-set to D_{NL}, which corresponds to the non-linearity error of the sensor. After sampling, C_{AUX} will be reset to zero before the regular SAR conversion starts. Due to charge redistribution of C_{AUX} via C_B, the corresponding non-linearity error is subtracted from the input signal at the comparator input. Since temperature changes slowly, the previous output sample is used to predict the correction code D_{NL} of the current sample. While the overall non-linearity is mostly a systematic distortion, there can be minor variations in the distortion coefficient over process corners. By means of the programmable bridge capacitor C_B, the non-linear correction created by C_{AUX} can be scaled, effectively fine tuning the distortion compensation coefficient. Also, because the non-linearity error is relatively small, with a bridge capacitor C_B, the capacitance of C_{AUX} can be made larger so that the matching of the C_{AUX} capacitors is improved. Considering the target accuracy and area overhead, a piecewise linear approximation instead of a polynomial function is adopted in this work (Fig. 7.4) to reduce the overhead to the minimum.

7.3.2 Proposed digital non-linearity correction

For comparison, an on-chip digital correction engine performing the same $f(x)$ as shown in Fig. 7.4 is implemented in this work. Considering the design complexity and overhead, the magnitude of $f(x)$ is fixed for the proposed digital non-linearity correction. If scalability of $f(x)$ is required, either a digital multiplication or a look up table with adjustable weights is needed. Both of them would lead to a substantial increase of complexity, and that's why fixed binary coefficients are chosen in this work. The detailed implementation will be discussed in Section 7.4.

7.4 Circuit implementation

7.4.1 Overview

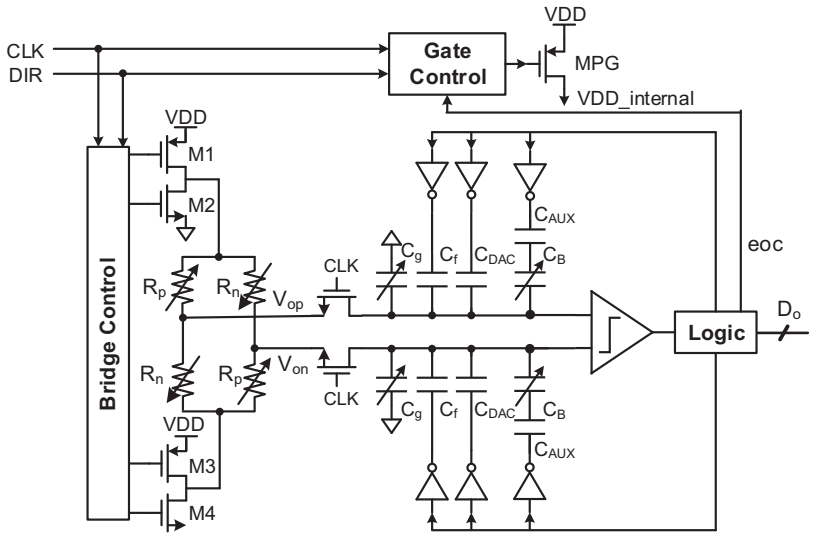


Figure 7.5: Architecture of the temperature sensor with on-chip analog non-linearity correction.

The main architectures of the two temperature sensors are similar to [20]. Fig. 7.5 and Fig. 7.6 show the architecture of the temperature sensors with analog correction and digital correction, respectively.

Both of them consist of a dynamic resistive bridge to sense the temperature, a 9-bit asynchronous SAR ADC to read out the temperature and a power gating switch (MPG) to minimize the leakage of the system. Power switches (M1-M4) are applied to the Wheatstone bridge to duty-cycle the resistive sensing front-end and to realize system level correlated double sampling (controlled by a direction signal DIR). Thanks to the dynamic operation, P-type polysilicon resistors (R_p) and N-type diffusion resistors (R_n) with a relatively small value of 100 kΩ can be employed with high energy efficiency [68]. On top of this, the offset and gain correction techniques are integrated into the ADC. The basic principle of the two corrections is to replicate the errors caused by the resistive sensing front-end in the ADC but with an opposite polarity so they will cancel each other out in the final output. To minimize area overhead, the corrections re-use the existing DAC capacitance, supplemented with several small capacitors (C_f and C_g) and extra logic. First, offset correction with a range of $\pm 2^{N-1}$ LSB is realized by pre-setting the DAC capacitors of an N-bit DAC during the tracking phase and then resetting them after the sampling moment [20] to induce a voltage step that compensates for the offset. Fine tuning capacitors (C_f) are added to further improve the offset correction accuracy to $\frac{1}{2}$LSB. By adding a

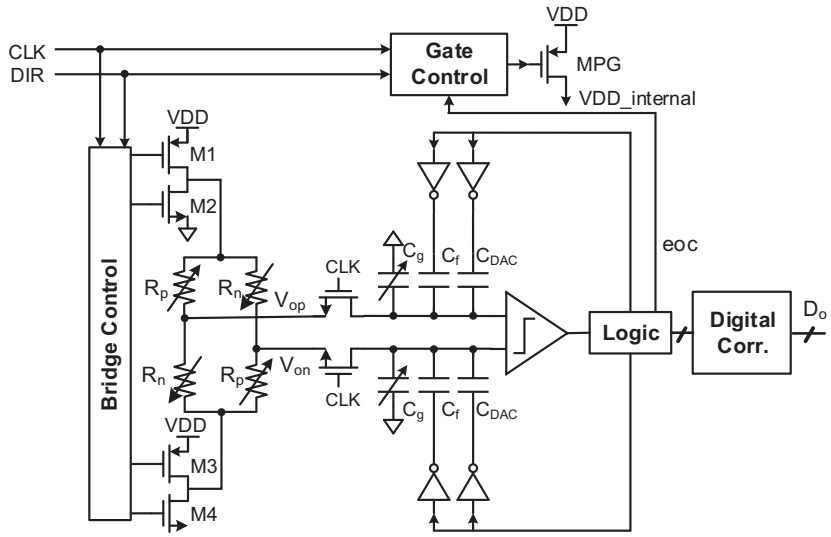


Figure 7.6: Architecture of the temperature sensor with on-chip digital non-linearity correction.

programmable capacitor (C_g), the ADC range can be adjusted to compensate gain errors [20]. A 3-bit C_g array is used in this work to achieve a gain correction range of 6.4% with a step size of 0.8%. Since the errors are corrected before AD conversion, the proposed analog offset and gain correction may obtain more benefits from the system-level CDS [70]. Also, signals are more concentrated, which allows a reduction of the ADC input range.

7.4.2 Analog non-linearity correction

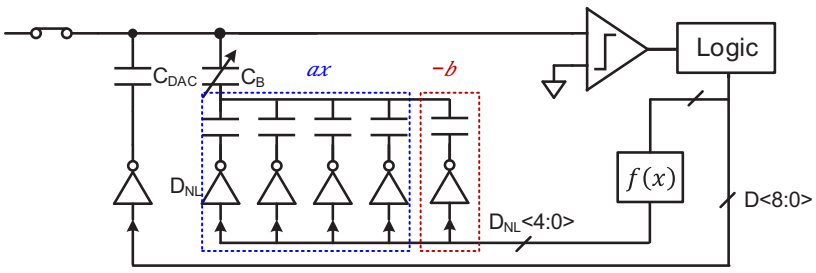


Figure 7.7: Circuit implementation of the analog non-linearity correction.

The detailed circuit implementation of the analog non-linearity correction is shown in Fig. 7.7.

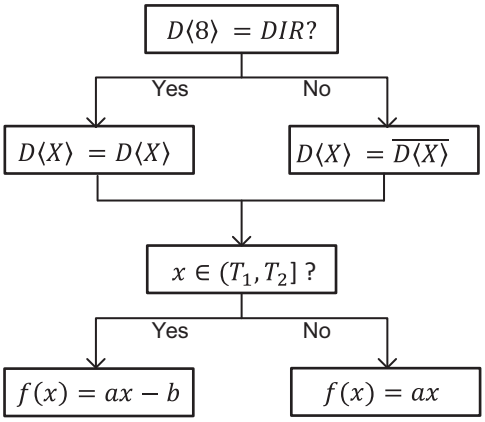


Figure 7.8: Block diagram of the correction logic.

After the offset and gain correction, the output codes for a certain temperature are consistent for all samples. In this work, the output code after offset and gain correction is at the mid-scale (256) at the middle temperature (50°C). Hence, the MSB transition coincides with the middle of the second-order distortion curve, which simplifies the logic to create the required piecewise linear function, as the function is mirrored around the MSB transition point. This can be achieved by flipping the bits dependent on the polarity of the MSB, D< 8 >. Likewise, the bits may need to be inverted depending on the phase of the correlated double sampling technique (determined by the DIR signal). After this first step, the only required function is ax or ax–b, dependent on the code range (see Fig. 7.4). Fig. 7.8 shows the block diagram of the correction logic.

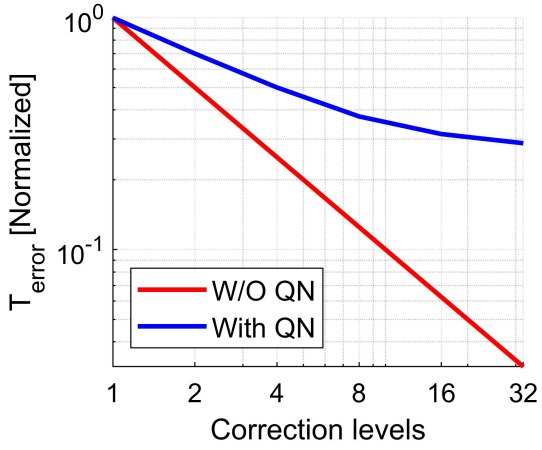


Figure 7.9: Simulated temperature error versus corrections levels.

The gain factor a is implemented by selecting appropriate bits of code D, and by scaling the C_{AUX} and C_B capacitors. A 4-bit linear compensation is chosen to minimize design overhead. Moreover, more precise compensation has little benefit due to

quantization noise limitations (Fig. 7.9). The conditional subtraction of b is done in the analog charge-sharing domain by a dedicated capacitor, which prevents the overhead of a digital subtraction. During the tracking phase, C_{AUX} is controlled by the non-linearity correction function. During the reset phases, C_{AUX} is reset to ground, which effectively subtracts the correction value from the sampled input voltage prior to AD conversion. The values of the C_{AUX} capacitors are 4fF, 2fF, 1fF, 0.5fF and 1fF respectively, of which the last 1fF capacitor is used to create the value b near the mid code. Unit-length capacitors are used for both the main DAC and for C_{AUX} to ensure the correction accuracy with small capacitors [55]. A 1-bit programmable C_B is used, whose nominal values are 5fF and 7fF. More programmability could be added to C_B to cover more process spread if desired. The extra capacitors for correction are placed on top of the ADC circuitry so that no extra area is needed for them. In total, the analog non-linearity correction logic requires 6 XOR, 11 NAND and 12 NOT gates.

7.4.3 Digital non-linearity correction

The digital non-linearity correction follows the same logic function as the analog correction (Fig. 7.8). Instead of implementing the correction in the analog domain by switching small capacitors, the correction is now implemented in the digital domain by full adders and half adders. In total, the digital non-linearity correction logic requires 6 XOR, 1 NAND and 2 NOT gates, 6 full adders and 7 half adders.

7.5 Measurement results

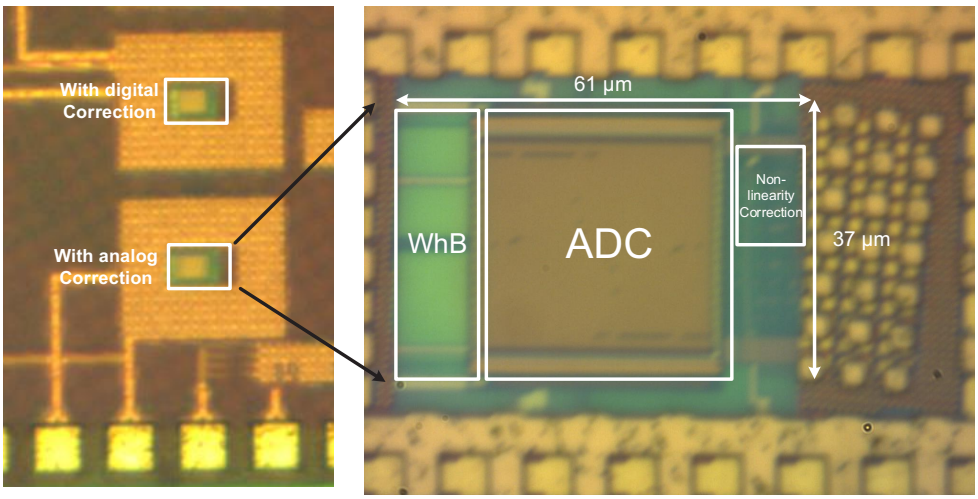
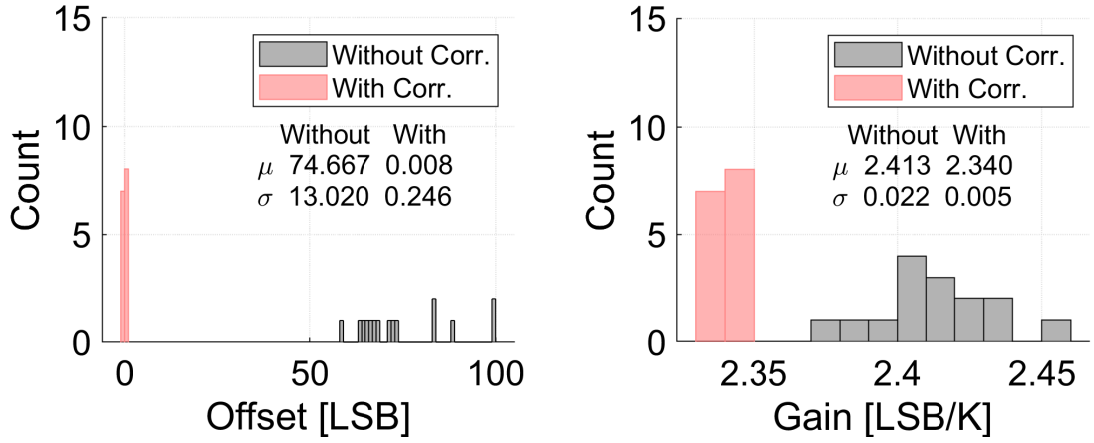


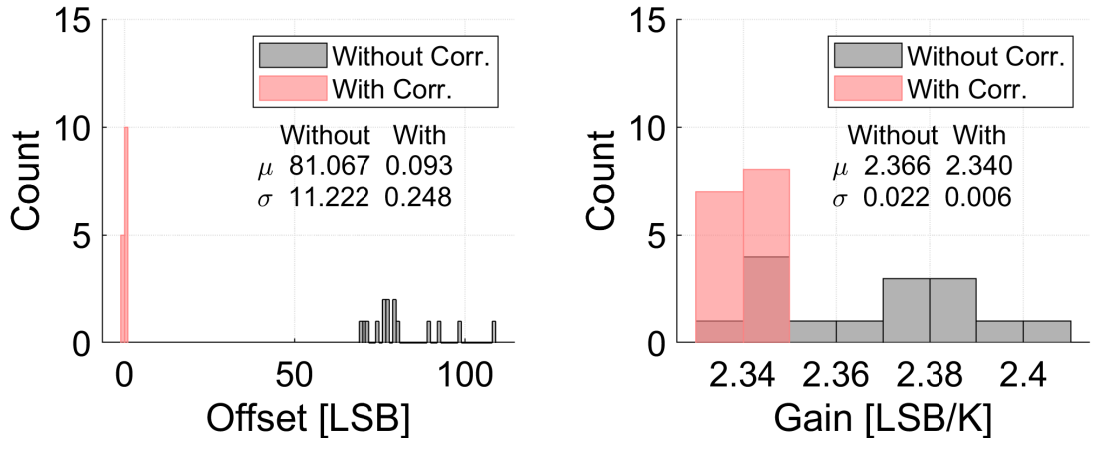
Figure 7.10: Die photo.

The two temperature sensors including corrections are fabricated and measured in 65-nm CMOS technology (Fig. 7.10). The sensors with analog correction and digital correction occupy an area of 0.0023 mm^2 and 0.0025 mm^2 respectively. The extra analog correction occupies an area of 170 μm^2, while the extra digital correction occupies an area of 500 μm^2. Most circuits operate from a 0.6-V supply, but the bridge switches and power gating switches are driven by 1-V drivers to reduce the drain-source leakage. 15 samples are measured in a temperature range from -20 to 120 °C.



(a) (b)

Figure 7.11: Measured offset and gain variation of the temperature sensors with analog non-linearity correction (15 samples).



(a) (b)

Figure 7.12: Measured offset and gain variation of the temperature sensors with digital non-linearity correction (15 samples).

As mentioned in Section 6.3, firstly, offsets and gain errors are corrected. The offset and gain corrections are done based on 2 trimming points at 50°C and 100°C. The measured offset and gain variation of the two designs with and without correction are summarized in Fig. 7.11 and Fig. 7.12, respectively. For both sensors, the measured

offset values are improved from 58 - 100LSB to -0.5 - 0.5LSB. The average offset before correction is around 80LSB, which indicates that the measured sensors are at the FF corners. The sensors' gain variation is improved from 3.5% to 0.8%. The offset and gain characteristics are similar for both designs since they have similar implementations. With the proposed analog offset and gain corrections, the offset and gain error of a dynamic sensor is corrected before the read-out circuit. Once the offset and gain of the sensor are corrected, the output code versus temperature curves are almost the same for different samples. Also, the output code for the middle temperature is at the mid-scale. There are still residual offset and gain errors remaining due to the correction step sizes, but their effects on the non-linearity correction function are negligible.

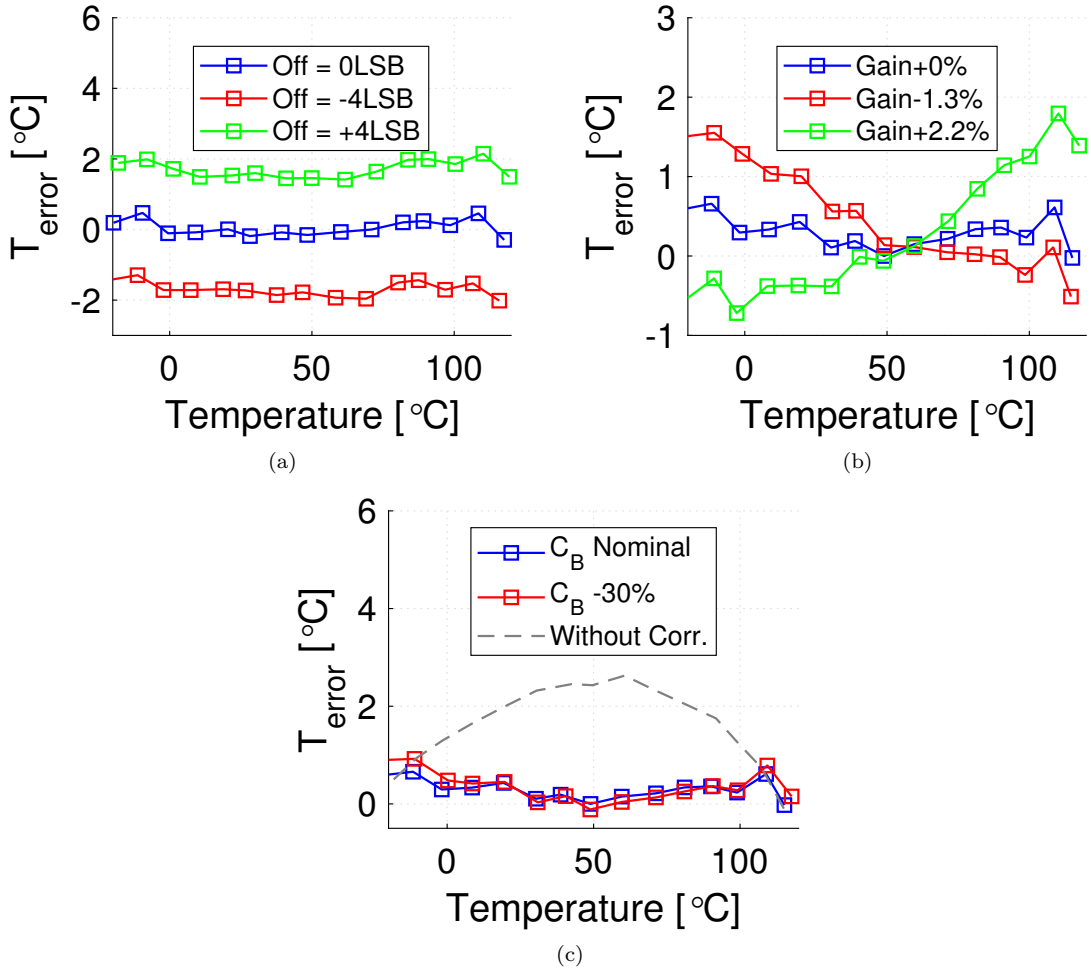


Figure 7.13: Measured temperature error curves with various offset (a), gain (b) and non-linearity (c) correction settings.

After the analog offset and gain corrections, non-linearity correction can be performed. To confirm functionality, Fig. 7.13 shows the measured temperature error curves with various offset, gain and non-linearity correction settings for the analog correction. As shown in Fig. 7.13(a), a ±4 LSB offset could already result in significant temperature errors (around 2 °C). Simulations show that the offset of the sensor can be tens of

LSBs, which makes it the largest error source. Mismatch also results in random gain variations but in a secondary way. As can be seen from Fig. 7.13(b), a 2.2% variation could result in a temperature error of around 2.5 °C. Besides, the temperature error also depends on the non-linearity compensation setting, whose magnitude is controlled by C_B (Fig. 7.13(c)). For the given batch of samples, an appropriate compensation coefficient helps to improve the maximum inaccuracy from approximately 2.73 °C to 0.68 °C. The effects of different offset and gain settings are the same for the temperature sensor with digital non-linearity correction. However, the non-linearity correction setting is fixed for the digital correction.

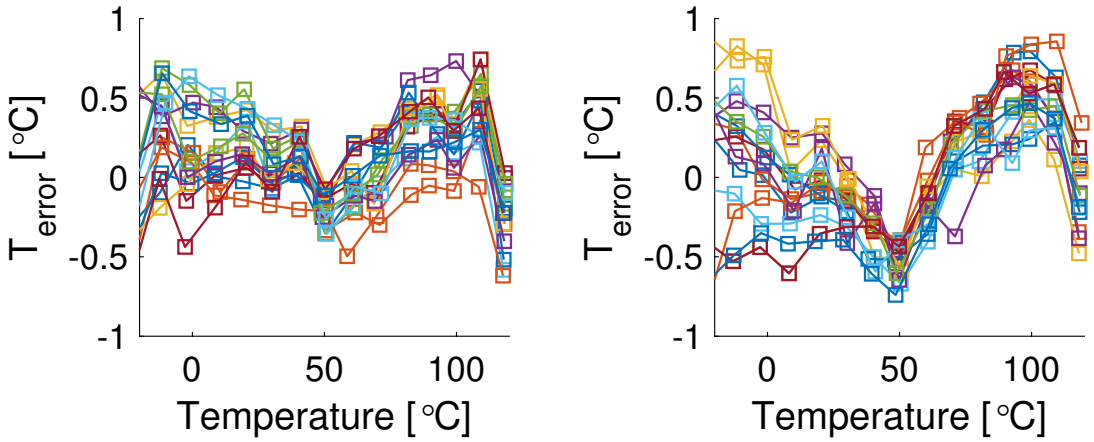


Figure 7.14: Measured temperature error curves with analog non-linearity correction (a) and digital non-linearity correction (b).

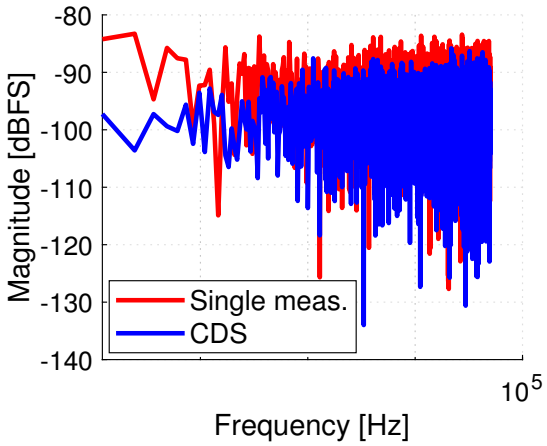


Figure 7.15: Measured output spectra of the temperature sensor with analog non-linearity correction.

Fig. 7.14 shows the measured temperature errors of both sensors. As can be seen from Fig. 7.14, with the proposed analog or digital non-linearity correction, the systematic non-linearity is significantly mitigated. With analog correction, the sensor achieves an inaccuracy of +0.7/-0.6 °C and the resulting relative inaccuracy is 0.97%. With digital correction, the sensor achieves an inaccuracy of +0.8/-0.8 °C. The proposed

analog correction works slightly better than the digital correction. This is because the designed digital correction has a fixed compensation magnitude, which does not fit optimally for the actual process corner.

For both sensors, the measured RMS resolution is around 0.47K at room temperature. Thanks to CDS, 1/f noise is mitigated. Exemplary measured output spectra of the temperature sensor with analog non-linearity correction without and with CDS are shown in Fig. 7.15.

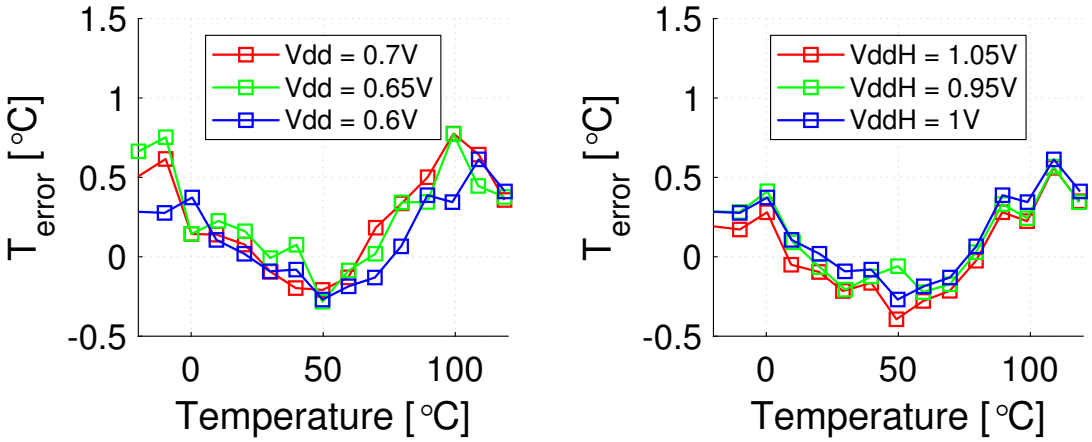


Figure 7.16: Measured temperature error curves with supply variation (a) Vdd (b) VddH.

The measured temperature error curves with supply variation are shown in Fig. 7.16. The correction settings are fixed for all the measurements according to the measurement results at the nominal supplies. As can be seen, the supply variation has little effect on the correction of the sensor. This is because that the resistive bridge and the ADC share the same supply voltage (Vdd), resulting in a ratiometric measurement. While the output of the resistive bridge is scaled with Vdd, the input range of the ADC will also be scaled with the same factor. Hence, the Vdd variation does not matter. The VddH supply only drives the bridge switches and the power-gating switches. Its absolute value is not critical either.

Table 7.1: Power and area dissipation with various on-chip correction techniques.

Case	Offset Corr.	Gain Corr.	Non-linearity Corr.	Power [nW]	Area [μm^2]
1	×	×	×	131	1656
2	✓	✓	×	137	1836
3	✓	✓	✓, analog	149	2257
4	✓	✓	✓, digital	150	2461

Table 7.1 summarizes the power and area consumption of the dynamic resistive sensor with various on-chip correction techniques. Here, case 1 is a previous design [67] without any on-chip correction techniques. Case 2 is a previous design [20] with

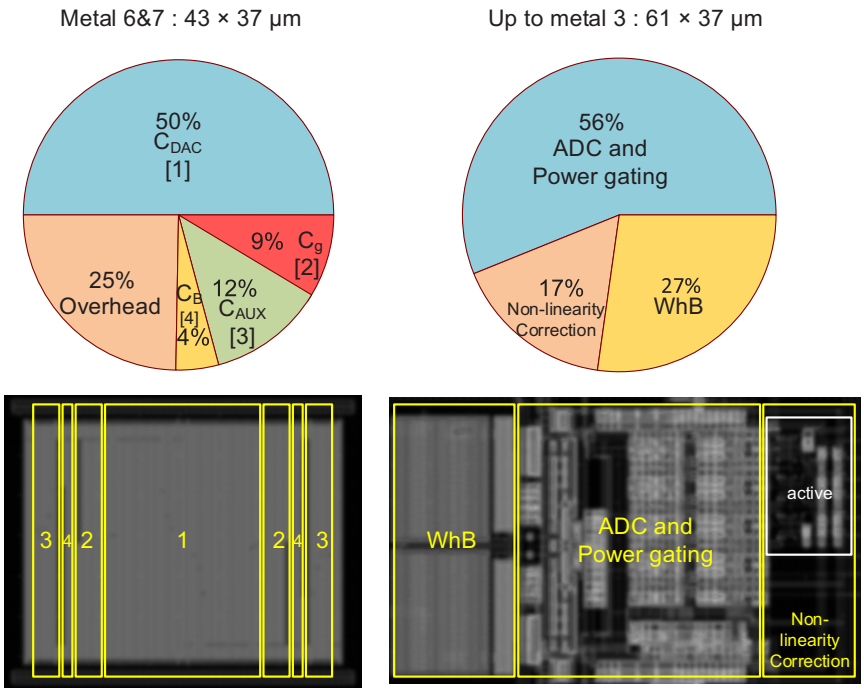


Figure 7.17: Area breakdown and layout view of the temperature sensor with analog non-linearity correction.

analog offset and gain correction techniques. Case 3 is the proposed design with analog offset, gain and non-linearity correction techniques. Case 4 is the design with analog offset, gain correction and on-chip digital non-linearity correction techniques. The detailed area breakdown and layout views of case 3 and 4 are shown in Fig. 7.17 and Fig. 7.18. For both sensors, the capacitors are placed on Metal 6 and 7. Metal 4 and 5 are shielding layers. The other circuity is placed underneath. Since the area of the capacitors is smaller than the area of the other circuity, no extra area is required to implement the non-linearity correction capacitors (C_B and C_{AUX}). The proposed sensor with analog offset, gain and non-linearity correction consumes 0.149 μW and occupies 2257 μm^2. The proposed sensor with analog offset and gain correction and digital non-linearity correction has a similar power overhead, but a bit larger area overhead. Thanks to the compact capacitor layout technique [55], the active area of the analog correction is only around 1/3 of the active area of the digital correction. Besides, the correction coefficients for the digital non-linearity correction are binary-scaled and fixed. To design a programmable digital correction with non-binary coefficients, the required power and area may grow up substantially. Compared to a stand-alone design without any correction techniques, the power consumption is increased by 13.7% and the area is increased by 36%. Compared to the design with only analog offset and gain correction, the power consumption is increased by 8.8% and the area is increased by 23%. Overall, the work described in this chapter proves that for ultra-low power sensors, on-chip correction can be done with minor power and area overhead.

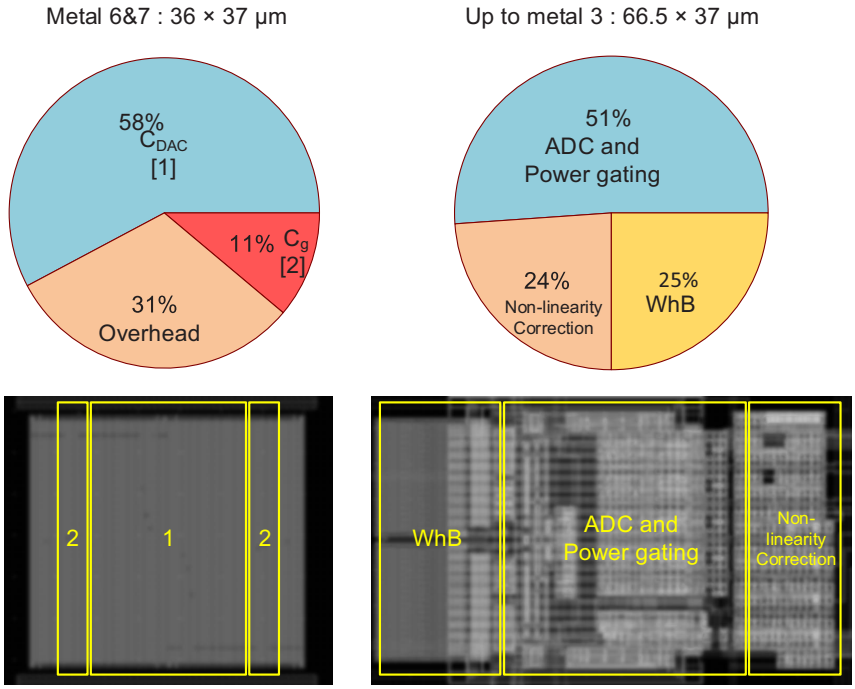


Figure 7.18: Area breakdown and layout view of the temperature sensor with digital non-linearity correction.

Table 7.2 summarizes the performance of this work and compares it with state-of-the-art WhB temperature sensors. It is the first low-power and compact WhB temperature sensor which integrates on-chip offset, gain and non-linearity error corrections and maintains state-of-the-art power and size performance. These features make it suitable for IoT ambient temperature monitoring applications in which low power and small size are demanded, together with moderate resolution.

7.6 Conclusion

This chapter presents two dynamic temperature sensors with on-chip analog and digital non-linearity correction, respectively. Thanks to the simplified correction logic, the sensor with analog non-linearity correction achieves an inaccuracy of +0.7/-0.6 °C with 2.98 pJ/conversion and 2257 μm^2. The sensor with digital correction achieves an inaccuracy of +0.8/-0.8 °C with 3 pJ/conversion and 2461 μm^2. These results show that systematic non-linearity removal can be done efficiently on-chip for low-power temperature sensors.

Compared to the digital non-linearity correction, the proposed analog non-linearity correction requires similar energy consumption and less area. Its correction coefficients can be scaled easily with a bridge capacitor. Also, it has more flexibility in

choosing compensation coefficients.

The digital correction is less affected by capacitor mismatch and its layout design is easier since no custom designed capacitors are required. On top of this, it may have an advantage in terms of overhead for temperature sensors with higher resolutions because analog correction scales up exponentially with resolution while digital correction scales less rapidly.

Table 7.2: Performance summary and comparison

	[66]	[71]	[72]	[73]	[67]	[20]	This work	
Technology [nm]	180	180	65	65	65	65	65	
Area [mm^2]	0.43	0.11	1.37	0.044	0.0017	0.0018	0.0025	0.0023
Supply voltage [V]	1.5	1.8	0.75	0.8	1/0.6	1/0.6	1/0.6	
Temp. range [°C]	-45 to 125	-55 to 125	0 to 90	-45 to 85	-20 to 120	-20 to 120	-20 to 120	
Inaccuracy (Trimming points) [K]	$\pm 0.4(2^a)$	$\pm 0.1(2^a)$	$\pm 0.2(4^a)$	$+1.6/-1(2^b)$	$1.2(2^b)$	$+0.6/-0.6(2^b)$	$+0.8/-0.8(2^b)$	$+0.7/-0.6(2^b)$
Resolution [K]	0.01	0.15m	1.75m	0.121	0.53	0.47	0.47	
Power [μW]	64.5	55	15*	47.2	0.108	0.137	0.150	0.149
Conversion time [s]	100μ	8m	100m	10μ	20.6μ	20μ	20μ	20μ
Conversion energy [pJ]	6450	440000	1500000	472	2.18	2.74	3	2.98
Resolution FoM[1]	0.65	0.01	4.6	6.9	0.61	0.6	0.66	0.66
On-chip corr.	Trimming resistors	Trimming resistors	Digital polynomial generator	None	None	Offset, gain	Offset, gain, digital non-linearity	Offset, gain, analog non-linearity
Off-chip corr.								
1^{st} order fit	✓	✓	Not available	✓	✓	×	×	
Decimation filter	✓	✓	Not available	×	×	×	×	
Polynomial engine	✓	✓	×	✓	✓	✓	×	

[a] 3σ values [b] Maximum values * Excluding the on-chip digital blocks.
[1] $FoM = Energy/Conversion \cdot (Resolution)^2$

Chapter 8

Digital communication interface

This chapter presents a simplex and a full duplex digital communication interface with enhanced efficiency for low-speed low-power systems. A capacitive fully dynamic simplex interface is proposed first. A self-interference cancellation network is then applied to achieve full duplex operation. Thanks to the all-dynamic architecture, the proposed interfaces allow efficient power scaling with data rates and load capacitance.

The content of this chapter has been published in [22].

8.1 Introduction

Thanks to CMOS scaling, electronics is becoming increasingly more power-efficient and integrated. Sensor interface circuits are following this trend and can already achieve sub-nW power consumption, as shown e.g. in [41]. The power consumption of digital chip-to-chip communication, thus, starts to become dominant in these ultra-low power sensing systems. As discussed in Section 1.2, energy efficient chip-to-chip digital communication is required (Fig. 8.1) when several sensor interfaces and digital signal processing blocks need to be connected on a PCB, in a multi-die package, or via short cables. Examples include versatile sensing for IoT, where multiple parameters such as temperature, humidity, pressure, etc., need to be measured, or biomedical sensing systems with multiple active electrodes connected to a central processing unit via short cables.

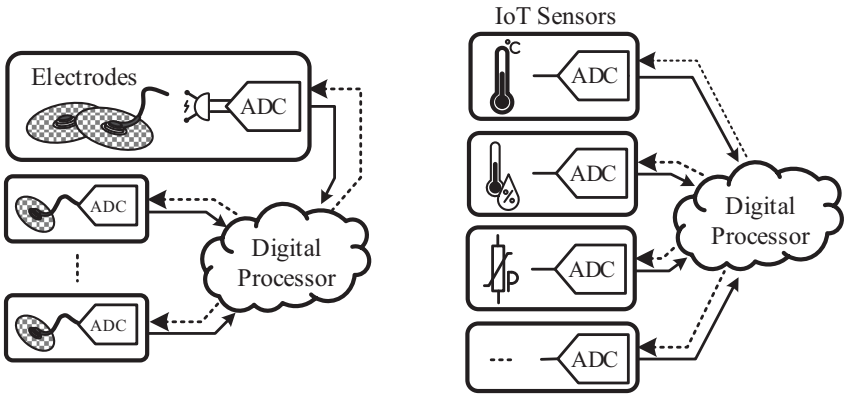


Figure 8.1: Chip-to-chip communication in low-power low-speed systems.

Most chip-to-chip communication systems focus on improving the speed of operation, and efficiency is particularly optimized for high speeds. Fig. 8.2 shows a benchmark of prior art [75–83] and existing standards [84–87]. For backplane transceiver logic (BTL)/Gunning transceiver logic (GTL)/LVDS/CML/ Low-voltage positive emitter-coupled logic (LVPECL), they require static power consumption, so their efficiency degrades at low data rates. LVCMOS is the only standard with dynamic consumption, so it remains equally efficient at lower rates, but its energy efficiency is not outstanding. State-of-the art designs can achieve 1.1 pJ/b at 100 GS/s [75], but most of them are also only optimized for higher data rates. The efficiency for low communication speed (data rates $<$ 100 Mb/s) remains limited and leaves room for improvement.

To address digital communication efficiency in low-power low-speed systems, a conventional approach is to use LVCMOS communication, where rail-to-rail signals are transmitted at a reduced supply level. Fig. 8.3 shows a simplified model of LVCMOS. The average energy consumption per bit of a conventional LVCMOS driver is given by:

$$E_{LVCMOS} = \frac{1}{4} C_L V DD^2 \tag{8.1}$$

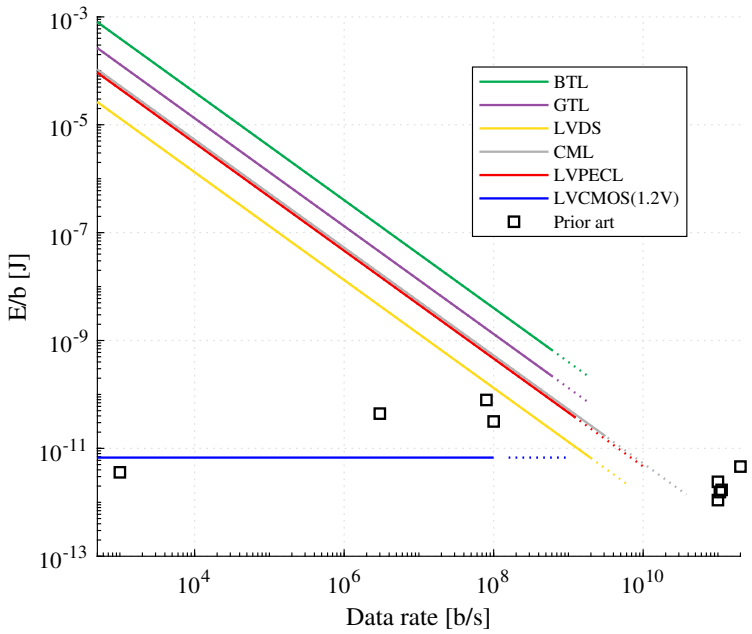


Figure 8.2: Benchmark of prior art and existing standards, data from [75–87].

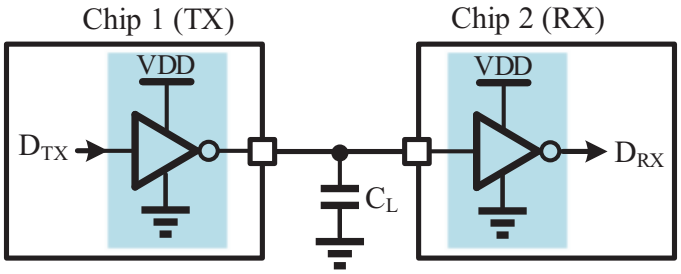


Figure 8.3: Simplified model of an LVCMOS interface.

where C_L is the load capacitance, VDD the supply voltage and the factor $\frac{1}{4}$ takes into account the fact that only a 0→1 transition costs energy. (It is assumed that the probabilities of a 0→0, 0→1, 1→0, and 1→1 transition are equal.) The load capacitance between two chips on a PCB can easily be in the order of 5 pF. This means that an energy of 1.8 pJ/b is required using a 1.2-V LVCMOS interface. This will dominate the power budget when applied e.g. to the 10-bit temperature sensor interface described in [41], which needs 2.43 pJ per temperature sample, and thus consumes only 0.24 pJ/b for sensing and digitalization. Therefore, it is necessary to reduce the energy consumption of the digital chip-to-chip interface. Existing low-power wireline interfaces [76, 77] use smart supplies to further improve the energy efficiency. However, the achievable efficiency depends on the operating frequency and the maximum efficiency point is only possible with an ultra-low supply voltage (0.24 V) and low data rate (< 1 kb/s). As a result, an extra DC-DC converter may be needed, which causes overhead at the system level. Body channel communication circuits also aim for low-power communication [78, 79], but use the human body as a

transmission medium and are not immediately comparable to wireline interfaces.

Besides energy efficiency, full duplex communication is sometimes preferred to minimize wire count, for instance in biomedical systems with active digital electrodes as shown in Fig. 8.1.

This chapter presents a simplex digital interface and a full duplex digital interface enabling energy-efficient, reliable and adaptable chip-to-chip communication for low-speed low-power systems. The adaptability makes the interfaces suitable for a variety of applications, with data rates from 10 kb/s to 50 Mb/s and load capacitances from a few pF to a few tens of pF, while maintaining high energy efficiency.

This chapter is organized as follows: the proposed simplex digital interface and full duplex digital interface are introduced in Section 8.2, measurement results are presented in Section 8.3, and conclusions are drawn in Section 8.4.

8.2 Architecture

8.2.1 Simplex interface

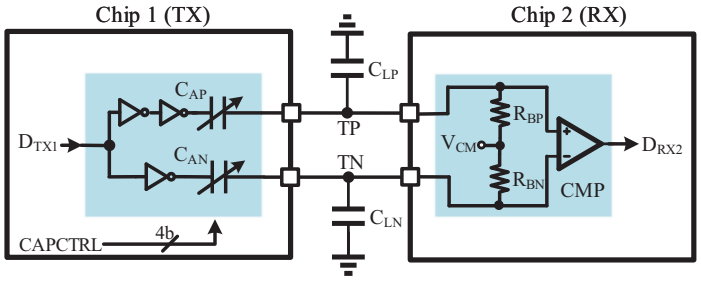


Figure 8.4: Architecture of the proposed simplex interface.

As shown in (8.1), the transmission power for LVCMOS is related to the transmission levels which are rail to rail. Hence, smart supply or signal attenuation techniques could be used to reduce the transmission power. Supply scaling was used in prior-art, but requires adaptable supplies, and low supply voltages (e.g. sub-threshold) will degrade the maximum speed of operation. Therefore, in this work, a nominal 1.2-V supply is used and a programmable signal attenuation is implemented to reduce power.

Fig. 8.4 shows the architecture of the proposed differential simplex digital interface. The transmitter (TX) is built by two programmable attenuation capacitors (C_{AP}, C_{AN}) and drivers. By inserting these attenuation capacitors, the transmitted signal

amplitude is reduced to:

$$A_{TX} = \frac{C_A}{C_A + C_L} VDD \tag{8.2}$$

As the load capacitance seen by each inverter is the series of C_A and C_L, the average energy consumption of the driver is reduced to:

$$E_{TX,S} = \frac{1}{2} \frac{C_A}{C_A + C_L} C_L VDD^2 \tag{8.3}$$

The original factor $\frac{1}{4}$ in (8.1) is increased to $\frac{1}{2}$ in (8.3) due to the differential implementation. By adjusting the signal amplitude with capacitors, no extra power supply is needed to reduce power, while the capacitive division results in a dynamic consumption that scales down with the actual data rate, enabling low-power low-speed operation.

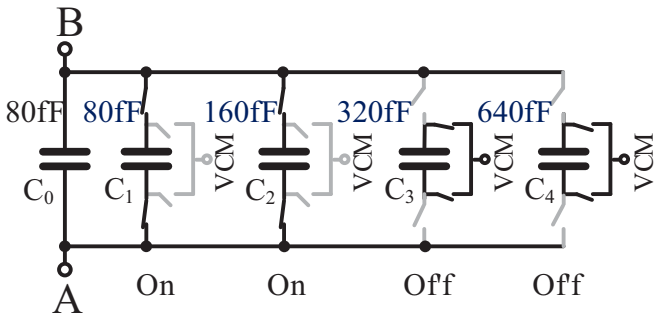


Figure 8.5: Tunable attenuation capacitor for C_{AP} and C_{AN}. (4-bit control).

The attenuation capacitors (Fig. 8.4) are programmable to adjust the attenuation factor, and to accommodate different loading scenarios. For example, when the load capacitance is 24 pF and the supply voltage is 1.2 V, a 1.2-pF attenuation capacitor can be selected to have about 60-mV signal range or a 0.4-pF capacitor can be selected to have about 20-mV signal range. The tunable capacitors are implemented as metal insulator metal (MIM) capacitors with switches (Fig. 8.5). Their value can be programmed from 80-fF to 1.2-pF with a step of 80-fF by the 4-bit word CAPCTRL. This will enable the interface to drive up to 24-pF load capacitance with about 60-mV signal range or up to 72-pF load capacitance with about 20-mV signal range. Larger or smaller tunable capacitors could be added to accommodate other loads. The matching of the capacitors is not critical as it only results in minor deviations of the amplitude.

A fully dynamic comparator working in the subthreshold region is used as receiver (RX). The minimum transmitted amplitude should be larger than the comparator's offset and noise level to prevent bit errors. A low-offset and low-noise comparator leads to lower TX power but higher RX power.

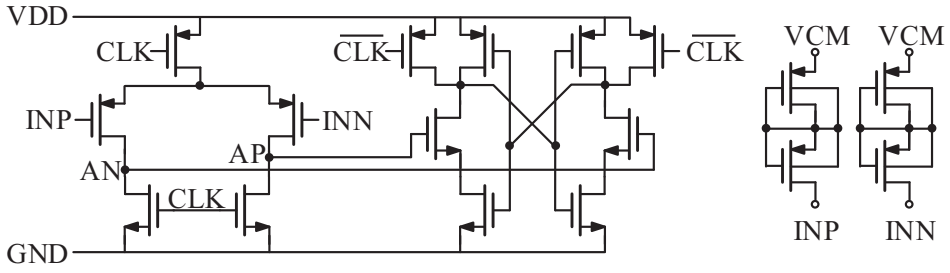


Figure 8.6: Dynamic comparator with DC bias via pseudo resistors.

As (8.2) and (8.3) show, the TX energy scales linearly with A_{TX} for a given C_L and VDD. On the other hand, the offset and noise level of the comparator in the RX also have to go down proportionally to A_{TX}. As a result, the RX energy goes up with $1/A_{TX}^2$. When A_{TX} is too small, the RX power increases rapidly. Moreover, external disturbance and mismatches exist depending on the applications and environment. A larger A_{TX} improves immunity to these disturbances and mismatches. Overall, a bit larger A_{TX} can be chosen, as it reduces RX power, gives better immunity to external disturbances, and can still save a reasonable factor of TX power. For example, with a TX amplitude of 60-mV at 1.2-V supply, the transmission power is reduced to $<$ 10% of LVCMOS. At the same time, an amplitude of several tens of mV still enables a rather low power comparator in the receiver.

In this work, a fully dynamic comparator composed of a pre-amplifier and a latch is used [44] (Fig. 8.6). A PMOS input comparator is used for lower flicker noise. The comparator has a simulated input-referred noise of 0.45-mVrms and an estimated 3σ-offset of 11-mV while consuming 0.14 pJ/b. A 20-mV TX amplitude, which covers about 5σ of offset, is sufficient for such a comparator.

As the input signal is AC coupled, bias resistors (R_{BP}, R_{BN}) are added to define the DC bias voltage at the comparator input. These are implemented as highly resistive pseudo resistors (about 3.5 GΩ), to enable correct interface operation down to low data rates ($<$ 10 kb/s). The pseudo resistors suffer from large mismatch, which could result in comparator offset due to input leakage currents. However, thanks to the relaxed noise requirements, the input transistors of the comparator are only 4μm/60nm in size, which limits their gate leakage current. In this way, the mismatch of the pseudo resistors is acceptable.

Note that similar to LVCMOS, this work does not yet include clock synchronization between the chips, as this depends on the application and optional data encoding. Like LVCMOS which has typically separate data and clock connections, one option is to use the proposed power-saving TX to transmit a master clock signal to all nodes. However, the receivers of such clocks will require continuous time receivers or clocked receivers with a clock recovery circuit. Alternatively, data encoding and suitable circuits could be used such that the clock can be recovered from the data itself.

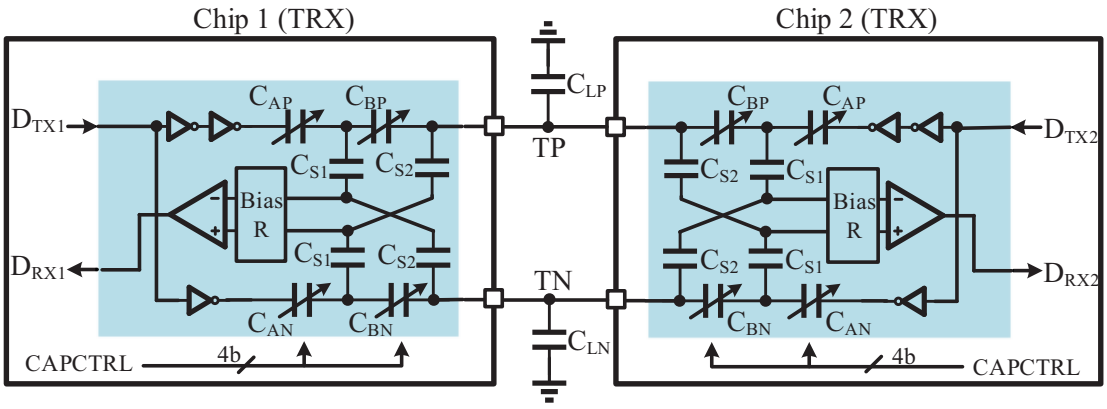


Figure 8.7: Architecture of the proposed full duplex interface.

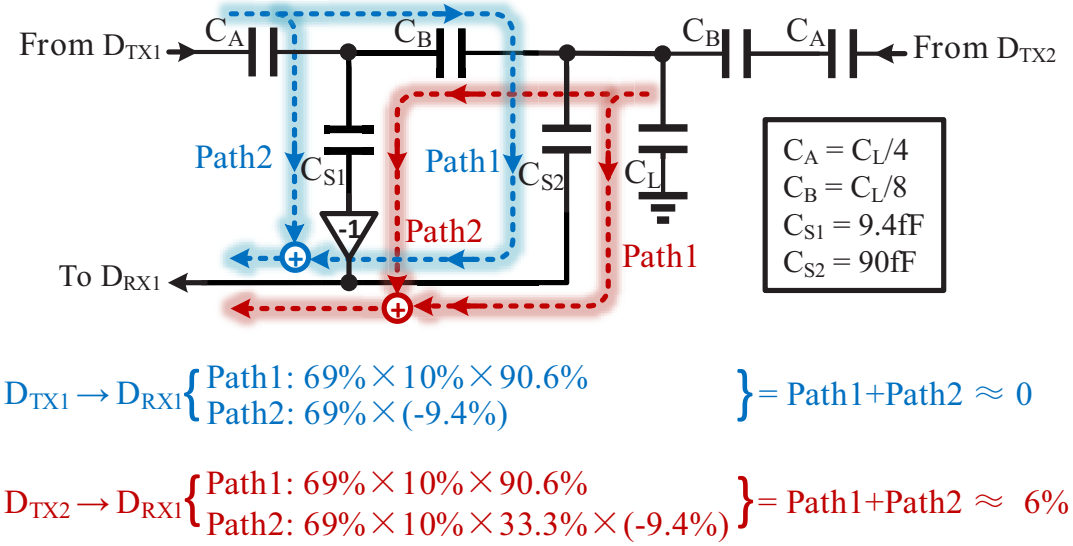


Figure 8.8: Model of the self-interference cancellation network.

8.2.2 Full duplex interface

In some applications, simultaneous reception and transmission of data are required and are preferred to be realized via the same pair of wires to reduce the number of connections. Besides, multiplexing signals also means less pads, less bonding wires and less package pins, which is critical in some applications, for instance, 3-D miniature ultrasound probes, where area requirements are very stringent [88]. To achieve full duplex communication, self-interference cancellation is required so that the transmitted signal can be removed from the received signal.

Fig. 8.7 shows the architecture of the proposed full duplex digital interface. Based on the simplex interface, a passive capacitive self-interference cancellation network (Fig. 8.8) is added. The bias network is implemented in the same way as in Fig. 8.4.

The self-transmitted signal will go through two paths with opposite polarity back to

its own receiver (path1: $C_B + C_{S2}$, path2: C_{S1}), the transmitted signal amplitude at the RX comparator input can be approximated by:

$$A_{TX1\rightarrow RX1} = k_1 VDD\left(k_2\frac{C_{S2}}{C_{S1}+C_{S2}} - \frac{C_{S1}}{C_{S1}+C_{S2}}\right) \tag{8.4}$$

where k_1 is the attenuation factor caused by C_A,

$$k_1 = \frac{2C_A^2C_B + C_A^2C_L + C_AC_B^2 + C_AC_BC_L}{(2C_AC_B + C_AC_L + C_BC_L)(C_A + C_B)} \tag{8.5}$$

and k_2 is the attenuation factor caused by C_B,

$$k_2 = \frac{C_B^2 + C_AC_B}{2C_AC_B + C_AC_L + C_B^2 + C_BC_L} \tag{8.6}$$

The received signal (Fig. 8.7 and Fig. 8.8) will also go through two paths (path1: C_{S2}, path2: $C_B + C_{S1}$), the received signal amplitude at the RX comparator input can be approximated by:

$$A_{TX2\rightarrow RX1} = k_1k_2 VDD\left(\frac{C_{S2}}{C_{S1}+C_{S2}} - \frac{C_{S1}}{C_{S1}+C_{S2}} \times \frac{C_B}{C_A+C_B}\right) \tag{8.7}$$

The received signal is only mildly affected (e.g. $<$ 1dB loss with the selected capacitors) due to the self-cancellation network. It will still be attenuated by the series of the capacitors C_A and C_B to save transmission power.

To maintain self-cancellation for different load capacitances, both C_A and C_B need to be adjusted as function of C_L, such that k_2 remains approximately constant and (8.4) remains approximately zero. In the prototype, C_A can be programmed from 320-fF to 4.8-pF while C_B can be programmed from 160-fF to 2.4-pF. This enables the full duplex interface to drive about 20-pF load capacitance with about 60-mV differential signal at the comparator input. The existence of capacitors C_{S1} and C_{S2} has an attenuation effect on the transmitted signals. Hence, their values are preferably much smaller than the values of C_A and C_B, and thus they are set to 9.4 fF and 90 fF, respectively. The ratio of C_{S1} and C_{S2} is determined by the desired signal swing and the ratio of C_A and C_B. In this design, C_{S1} and C_{S2} are fixed and C_A and C_B are programmable. To reach the lower boundary of the signal swing, C_{S1} and C_{S2} could also be realized as programmable capacitors. With the implemented capacitor values, signal attenuation and self-cancellation are achieved as shown in Fig. 8.8. During full-duplex operation, the received and transmitted signal are of equal magnitude at nodes TP and TN, but the received signal will dominate at the

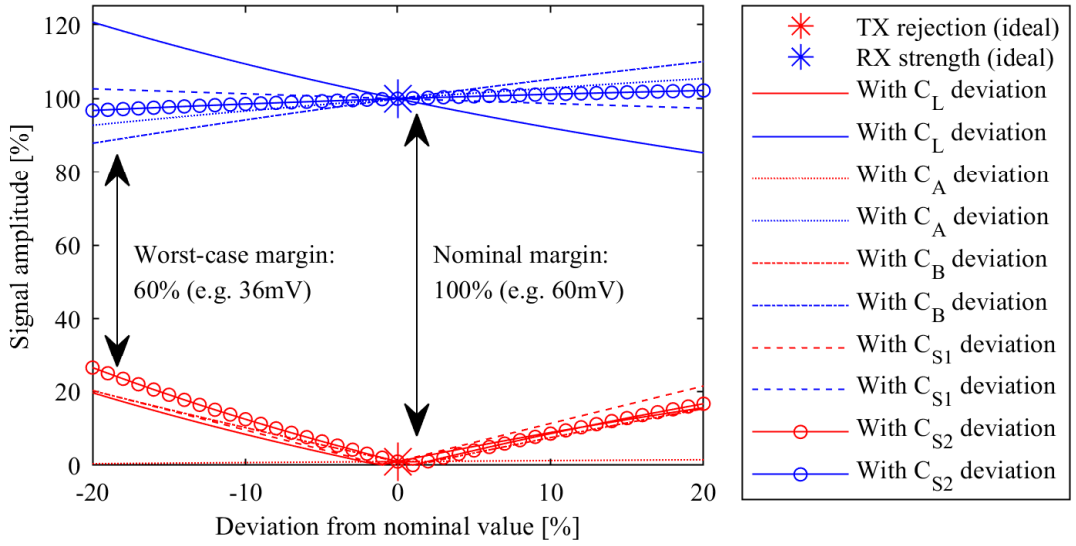


Figure 8.9: Sensitivity of the desired and undesired signal vs capacitor deviations.

RX comparator input.

Theoretically, the self-transmitted signal can be cancelled by appropriate sizing of the capacitors to make (8.4) equal to zero. In practice, considering capacitor mismatch and extra parasitic capacitance, the self-transmitted signal will not be perfectly cancelled, while the received desired signal strength may also vary. However, if the residue from the self-transmitted signal combined with the worst-case comparator offset and noise is smaller than the received signal, the received signal can still be recovered correctly. Fig. 8.9 shows the simulated sensitivity of the desired and undesired signal components as function of individual capacitor deviations. As shown, with up to 20% deviation, there is still 60% of the nominal margin remaining. With a 60-mV nominal amplitude, this provides sufficient margin to cover for comparator offset and noise under mismatch conditions.

The energy consumption of the driver is reduced to approximately:

$$E_{TX,FD} = \frac{1}{2}\frac{C_A C_B (C_A C_B + C_A C_L + C_B C_L)}{(C_A + C_B)(2C_A C_B + C_A C_L + C_B C_L)} VDD^2 \tag{8.8}$$

With about 60mV differential signal at the comparator input, the transmission power can be reduced to 13% of LVCMOS with the same load capacitance.

Similar to the simplex interface, the bias resistors and the capacitor network filter out low frequency signals. The cut-off frequency of the full duplex interface is higher than the cut-off frequency of the simplex interface because C_{S1} and C_{S2} are much smaller than C_A, C_B, and they determine the new cut-off frequency. Also, the energy consumption of a full duplex interface is a bit higher since extra attenuation

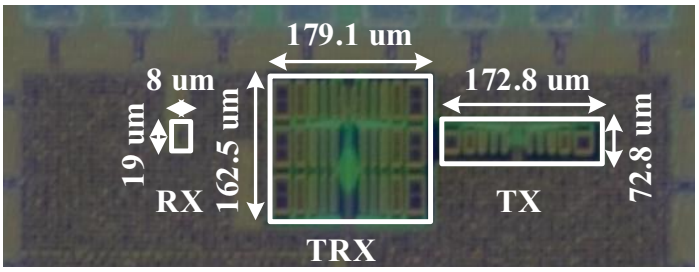


Figure 8.10: Chip micrograph in 65-nm CMOS.

is introduced by the self-interference cancellation network and margins need to be included to overcome the residual self-interference, both of which are overcome with a proportionally larger signal amplitude.

8.3 Measurement results

The proposed digital interfaces are fabricated in 65-nm CMOS, as shown in Fig. 8.10. The simplex TX, simplex RX and full duplex transceiver (TRX) occupy an area of 0.0125 mm^2, 0.00015 mm^2, and 0.029 mm^2 respectively. More than 90% of the area is occupied by the tunable capacitors.

The interfaces use a 1.2-V supply since it is a standard supply voltage in 65-nm CMOS. Lower supply voltages are also feasible, at the cost of maximum data rate. The control clocks are provided externally for enhanced flexibility. Two chips are placed on one PCB at a few centimeters distance. To test the interface adaptability to different load capacitances, additional capacitors are soldered to the nodes TP and TN. The CAPCTRL signal is provided through an on-chip serial register.

Fig. 8.11(a) shows the measured power consumption of the simplex interface (including TX with capacitor drive circuitry and RX) with different data rates and load capacitances using a 20-mV signal swing. Most of this power is used in the TX to drive the capacitor network. Compared to LVCMOS, additional RX power is introduced, which is about 0.16 pJ/b at 50 Mb/s and 0.84 pJ/b at 10 kb/s (the imperfect dynamic scaling is due to an increased impact from static leakage power at low data rates). When the load capacitance becomes larger, the RX power becomes less relevant. The proposed simplex interface works for a large range of data rates (10 kb/s to 50 Mb/s) and load capacitances (0 to 72 pF). It achieves a power reduction of 27× with a 72-pF load capacitance at 50 Mb/s and a power reduction of 2.4× with a 9-pF load capacitance at 10 kb/s compared to conventional 1.2-V LVCMOS. The maximum data rate of 50 Mb/s is limited by the comparator decision time, as well as the RC constants formed by the capacitive network in combination with the output resistance of the TX drivers and the on-resistance of the switches in the tunable ca-

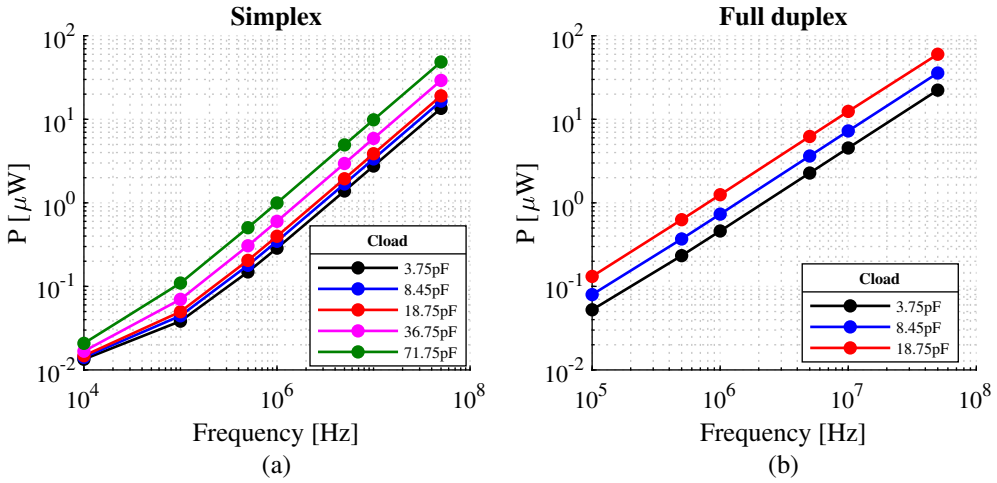


Figure 8.11: Measured power consumption vs data rate for the simplex interface (a) and the full duplex interface (b) for different load capacitors.

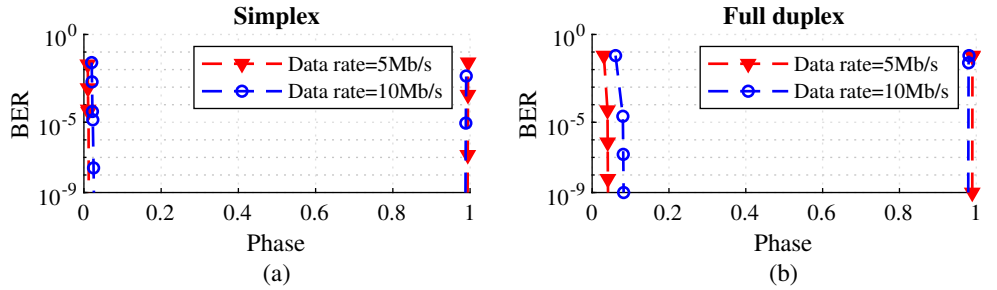
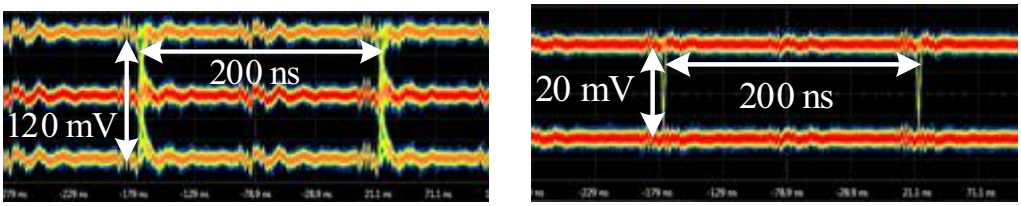


Figure 8.12: Measured BER bathtub curves for the simplex interface (a) and the full duplex interface (b). For most of the phase settings, the BER is better than 10^{-9}.

pacitors. The maximum data rate could be increased by resizing these components, at the cost of lower efficiency.

The power consumption of the full duplex interface at about 60-mV signal swing shows a similar trend as the simplex interface (Fig. 8.11(b)), but the absolute consumption is higher, mainly due to the larger signal swing. Even so, the proposed full duplex interface consumes much less power than LVCMOS and can maintain its power efficiency for a large range of data rates and load capacitances. The power consumption of the full duplex interface could be further reduced by extending the programmability of C_{S1} and C_{S2} to lower the signal amplitude. According to simulations, the power consumption of the full duplex interface would be about 10% larger than that of the simplex interface, if the same signal amplitude would be used.

In terms of reliability, both interfaces have a BER of $< 5 \cdot 10^{-12}$ (99% confidence level, 1T bits were measured at 10 Mb/s, and no errors were detected). Fig. 8.12 shows the measured BER bathtub curves with the same signal amplitudes as mentioned before, where each point is obtained by measuring 1 Gbit of data: in terms of phase error, both interfaces can achieve a BER $< 10^{-9}$ over 90% of the phase. Fig. 8.13(a) shows the eye diagram of the simplex interface while communicating at 5 Mb/s. The



(a) (b)

Figure 8.13: Recorded signals (at nodes TP, TN) at 5 Mb/s for the simplex interface (a) and the full duplex interface (b).

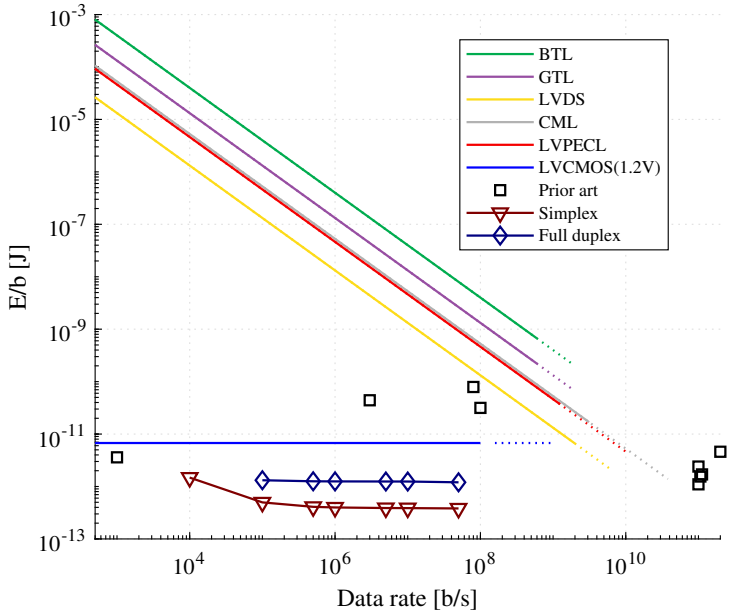


Figure 8.14: Benchmark of the proposed interfaces against prior art, data from [75–87].

recorded eye heights and widths at BER $< 10^{-9}$ are 20 mV and 0.988UI. Fig. 8.13(b) shows the recorded signal between two chips of the full duplex interface. The signal for the full duplex interface is a mix of equal-magnitude TX and RX signals and thus shows 3 levels. The RX signal can be recovered at the receiving chip after self-interference cancellation. Two chips can also communicate with each other at different data rates and phases simultaneously.

Table 8.1 summarizes the measured performance and the comparison against state-of-the-art. Compared to [77–79], this work has a wider tunability of data rate, a lower BER, and an energy efficiency that is about 2.5× to 60× better, thanks to the fully dynamic and mostly passive architecture. Fig 8.14 shows that the simplex interface achieves a power reduction of 2× to 27× compared to conventional LVCMOS with the same VDD and the same load capacitance (10 kb/s to 50 Mb/s), while the full duplex interface achieves a power reduction of 5× to 11× (100 kb/s to 50 Mb/s). Also, compared to existing high-speed standards and state-of-the-art low-power interfaces, this work achieves the best efficiency.

Table 8.1: Performance summary and comparison

	[77]	[78]	[79]	This work	
Technology [nm]	130	65	180	65	
Supply voltage [V]	0.24-1	1.2,1	1	1.2	
Simplex/Full duplex	Simplex	Full duplex	Simplex	Simplex	Full duplex
Data rate [b/s]	1k-3M	5M-80M	100M	10k-50M	100k-50M
Power [μW]	0.0054-132	1700-2600	3155	0.018-30.88[1]	0.13-60.09[1]
E(pJ/b)	3.61-44.1	78.8	31.55	0.38-1.47[1]	1.2-1.31[1]
BER	10^{-6}	10^{-5}	10^{-9}	$< 5 \cdot 10^{-12}$ [2]	$< 5 \cdot 10^{-12}$ [2]
Area [mm^2]	0.0012	5.76	1.26	0.0412	0.029

[1] With 19-pF load capacitance.
[2] With 99% confidence level; no errors detected for 1Tbit data.

8.4 Conclusion

In this chapter, chip-to-chip digital communication interfaces with data rate and load capacitance adaptability for low-speed, low-power systems are presented. A capacitive fully dynamic simplex interface and a full duplex interface with passive self-interference cancellation are proposed. Their signal amplitudes are adaptable to save power. The simplex and full duplex interfaces achieve an energy consumption of 0.38 pJ/b and 1.2 pJ/b respectively (with 19-pF load). The simplex interface achieves a power reduction of 2× to 27× compared to conventional LVCMOS for data rates from 10 kb/s to 50 Mb/s. The full duplex interface achieves a power reduction of 5× to 11× for data rates from 100 kb/s to 50 Mb/s.

Thanks to the fully dynamic, mostly passive, data rate and load capacitance adaptability, chip-to-chip digital communication efficiency in low-power, low-speed systems is improved. For ultra-low speed (< 10 kb/s) digital communication, leakage power could be optimized.

Chapter 9

Conclusions and future work

9.1 Conclusions

Miniaturization is a key trend for semiconductor industry applications (e.g. IoT, biomedical sensing and environmental monitoring). In terms of IC implementation, power and area costs are two critical concerns for these applications and the main focus of this thesis.

From a general point of view, the energy efficiency of a circuit with static power consumption is at its best when the operating speed is at its maximum. Hence, an effective way to save power for low-speed applications is to design duty-cycled or all-dynamic circuits. The circuits in this thesis are indeed all based on all-dynamic circuits, or duty-cycled circuits (which otherwise would have had a static bias).

Besides, circuits suffer from all kinds of imperfections which may degrade their performance. To mitigate the influence of these imperfections, the corresponding errors could be either predicted or detected and then be compensated accordingly. An area-efficient way to realize these correction functions (mismatch error shaping, input range compensation, offset, gain and non-linearity correction, etc.) is to reuse existing hardware in idle timing phases. In this thesis, the SAR ADC's switched-capacitor DAC is reused in various ways to implement such correction functions in idle timing phases.

To push the lower boundary of power and area costs for analog and mixed-signal circuits, three topics, including efficient analog-to-digital conversion, efficient corrections for temperature sensors and efficient digital communication, are discussed in detail.

In a first domain, power-efficient and area-efficient techniques for high-resolution ADCs are discussed (Chapter 2 and 3). For high-resolution ADCs, DAC mismatch is a major challenge. MES is an efficient way to alleviate the DAC mismatch errors at the cost of losing half of the input range. In Chapter 2, a pre-comparison technique based on analog prediction is firstly proposed to address the input range loss issue caused by MES. Besides, oversampling, data-driven noise reduction and chopping techniques are combined to improve the SNR efficiently. Then, an improved input range compensation technique based on analog detection is presented in Chapter 3. The prediction errors that were still present using the approach described in Chapter 2 are avoided by adopting flying capacitor sampling. Overall, by applying MES and analog input range compensation techniques, DAC mismatch errors can be shaped efficiently without input range loss, which is useful for high-resolution ADCs.

Besides, input range boosting techniques for low-to-medium resolution ADCs are discussed (Chapter 4 and 5). Extending the equivalent input range is an effective way to enhance the SNR of a moderate-resolution moderate-speed converter. On the one hand, less hardware can be used to achieve higher resolution, which improves the area efficiency. On the other hand, the absolute noise requirements are relaxed, which enhances the power efficiency. By performing a pre-comparison and switching the DAC accordingly, the input range of a SAR ADC can be increased by 50% (Chapter 4) and 100% (Chapter 5) respectively with limited power and area overhead.

In the second domain, efficient on-chip correction techniques for temperature sensors are discussed (Chapter 6 and 7). Due to process variation and random mismatch, temperature sensors suffer from offset, gain and non-linearity errors. Hence, efficient correction techniques are required, especially in low power low resolution systems. Firstly, by pre-setting and resetting the existing DAC in the ADC, a full code range offset correction is realized. Secondly, programmable parasitic capacitors are introduced to correct the gain errors. Thirdly, the non-linearity errors are corrected by pre-setting and resetting an auxiliary DAC with a piecewise linear approximation function. The prototypes show that even for very small and low power temperature sensors, correction can be integrated on-chip with limited overhead.

In the third domain, chip-to-chip digital communication in low speed low power systems is discussed in Chapter 8. To save power, the transmitted signal amplitude can be reduced adaptively. A dynamic simplex communication interface is firstly proposed. Based on it, a passive self-interference cancellation network is presented to achieve full duplex operation. By using the above fully dynamic interfaces exploiting capacitive division, energy-efficient digital communication with date rate and load capacitance adaptability can be achieved.

9.2 Future work

Due to limited time, some thoughts have not been further investigated and the developed work could be further extended or exploited in the future as follows:

- Thanks to MES and input range compensation techniques, DAC mismatch errors can be shaped efficiently without input range loss. Hence, small DAC capacitors can be used, which reduces the power and area costs of the DAC. As a result, the comparator power starts to dominate. A data-driven noise reduction technique and an efficient comparator architecture have been employed in this thesis, but they are not aggressive enough for ADCs with even higher resolution. For future work, various noising shaping techniques [38, 46, 49, 89] could be investigated to shape the comparator noise in an efficient way.

- For the ADCs with boosted input range, their supply voltages could be further lowered to achieve higher efficiency, as it was done in [59].

- Besides, the ADCs presented in Chapter 2-5 use two external clocks to generate different operation phases. One is for sampling, the other one is for flexibly controlling the pre-comparison phase. To make the circuit more practical to use, the generation of the pre-comparison clock can also be integrated on-chip and its circuit implementation can be further explored.

- Although corrections are done on-chip efficiently, the temperature sensors presented in Chapter 6 and 7 still require 2 trimming points, which is expensive in production. Investigations on the sensing front-end could be done to reduce the number of trimming points. Besides, the resolution of the temperature sensor is limited by the read-out ADC. This can be further improved by using a higher-resolution ADC, for example, SAR ADCs as described in Chapter 2 and 3.

- From the measurement results, a 60-mV signal swing is a bit conservative for the proposed digital communication interfaces. It can be lowered by changing the self-interference cancellation coefficients to further improve the energy efficiency of the full duplex communication interface. Besides, the leakage power could be optimized when the interfaces are used in low-speed (<10kb/s) applications. Besides, clock synchronization between chips could be exploited. As mentioned in Chapter 8, for example, the proposed power-saving TX can be employed to transmit a master clock to all nodes.

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Summary

Low Power and Small Area Mixed-Signal Circuits : ADCs, Temperature Sensors and Digital Interfaces

This PhD thesis aims to push the boundaries of the power cost and area cost for mixed-signal circuits used in cost-constrained applications. Efficient analog to digital conversion, temperature sensor correction, and digital communication are studied. General design approaches and new methods have been proposed to achieve the goal. Seven prototypes have been implemented and characterized for the target 3 circuit blocks to verify the proposed ideas.

Chapter 2 presents a 14-bit oversampled Successive Approximation Register (SAR) Analog to Digital Converter (ADC) with Mismatch Error Shaping (MES). A pre-comparison technique is proposed which, combined with MES, can shape the DAC mismatch errors without input range loss and thus improves the power and area efficiency for high-resolution ADCs. It achieves 103 dB spurious-free dynamic range (SFDR) with an above 180 dB Schreier figure-of-merit (FoM) and a 0.033 mm^2 active area.

In Chapter 3, an improved pre-comparison technique based on flying-capacitor sampling is proposed. Compared to the design in Chapter 2, it has the advantage of avoiding prediction errors.

Chapter 4 presents a 10-bit SAR ADC with 1.5× input range. An input range extension technique is proposed, which can relax the absolute noise requirement of the ADC to save power and area for low-to-medium resolution ADCs. The prototype ADC achieves an Effective Number Of Bits (ENOB) of 9.74 bit, with 2.2 fJ/conversion-step efficiency and a chip area of 0.0013 mm^2.

In Chapter 5, an improved input extension technique which can boost the equivalent input range of a SAR ADC by 2× is presented. It achieves 10.04 ENOB with 3.28 fJ/conversion-step. Compared to what is presented in Chapter 4, the input range is further enhanced and potential input driving problems are avoided by re-using the

flying capacitor sampling technique from Chapter 3.

In Chapter 6 and 7, efficient on-chip correction techniques for temperature sensors are discussed. A dynamic resistive temperature sensor with analog offset and gain correction is firstly presented in Chapter 6. A full range offset correction with a step of 0.5 Least Significant Bit (LSB) and a 6.4% gain correction range with a step of 0.8% are achieved with limited power and area overhead.

Then, non-linearity correction techniques for temperature sensors are discussed in Chapter 7. As a result, the prototype temperature sensor consumes 2.98 pJ/conversion with an area of 0.0023 mm^2 including all three correction techniques and achieves +0.7/-0.6 °C inaccuracy. The resulting FoM is 0.66 $pJ{\cdot}K^2$. These features make it suitable for IoT ambient temperature monitoring applications in which low power and small size are demanded.

Chapter 8 presents a simplex and a full duplex digital communication interface with data rate and load capacitance adaptability. The proposed interfaces achieve an energy consumption of 0.38 pJ/b and 1.2 pJ/b, respectively, at a bit error rate of $< 5 \cdot 10^{-12}$. Thanks to the all-dynamic feature, efficient power scaling as function of data rate and load capacitance is achieved.

Chapter 9 concludes the thesis.

Acknowledgments

How time flies. It seems like just yesterday when I started this interesting journey, and yet here I am, approaching the finish line. When looking back, this journey has been filled with challenges, excitement, and also the support and encouragement of many people whom I would like to thank.

First and foremost, I must thank Dr. Pieter Harpe for being my supervisor in this Ph.D. journey, as well as my bachelor and master graduation projects. Thank you for opening the door to the world of integrated circuit design and guiding me through each step of the process. When writing this acknowledgment, many moments flood my mind. During these nearly seven years, we have created a pile of tape outs, measurement set-ups, and paper submissions. We have experienced many non-working ideas, rejections, and also many beautiful results and more acceptances. I have learned a lot from you, not only in scientific research but also in how to approach and solve problems in both work and life. I have no doubt that I will continuously benefit from this for the rest of my life. I really appreciate the trust you have placed in me and the time you have invested in my growth.

I would also like to express my heartfelt thanks to Prof. Eugenio Cantantore. You are always so elegant and warm. Thank you for your warm encouragement before every presentation, meticulous polishing of each paper, and every valuable suggestion.

I would also like to thank the other members of the doctoral committee: Prof. Peter Baltus, Prof. Peter Rombouts, Prof. Marain Matters-Kammerer, and Dr. Michiel Pertijs for your time and valuable inputs.

I would also like to extend my sincere thanks to all the current and past members of the IC group. Thank you, Peter, Rainier, Margot, and all the other staff members for building such a wonderful research environment. Thanks, Haoming, Xi, Xiao, Qilong, Kevin, Daan, Bas, Martijn, Enrico, Kaijie, Johan, and all the other fellow members. I was very fortunate to collaborate with and learn from so many talented and motivated individuals. Special thanks to Hanyue for the pleasure of working together on the same project. Special thanks to Meiyi and Yijing for our enjoyable girls' moments.

Apart from the research, I would also like to thank my friends Rui, Liang, Hao, Yuanhao, Ming, Lu, Liuyan, Chengyang, and Qihao. Special thanks to Yahui. Thank you all for bringing me a lot of joy and happiness, which makes this journey less lonely.

Additionally, I would like to thank my colleagues in AMSIP, NXP Semiconductors, where I did my master thesis internship and where I am currently working. Special thanks to Robert for your supervision and mentoring. Special thanks to Alphons and Erik for your guidance and all the pleasant coffee breaks.

Last but not least, thank you, my parents and family. Thanks for your unconditional love and unwavering support, which has been the foundation and driving force of this journey.

Biography

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