Rectifiers - Analysis and Optimization for Wireless Energy Transfer

Rectifiers analysis & optimization for Wireless Energy Transfer

HANS W. PFLUG

Rectifiers — Analysis and Optimization for Wireless Energy Transfer

PROEFSCHIRFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op 21 april 2023 om 11:00 uur

door

Hans Willem Pflug

geboren te Eindhoven

Dit proefschrift is goedgekeurd door de promotoren en de samenstelling van de promotiecommissie is als volgt:

voorzitter:	prof.dr.ir. P.M.J. Van den Hof
promotor:	prof.dr.ir. H.J. Visser
copromotor:	prof.dr.ir. M.C. van Beurden
leden:	prof.dr.ir. W.A. Serdijn (TU Delft)
	prof.dr.ir. P. Mitcheson (Imperial College London)
	prof.dr.ir. P.G.M. Baltus
	dr.ir. S. Hemour (Université de Bordeaux)
adviseur:	dr.ir. J.F. Bakker (INBRAIN Neuroelectronics)

Het onderzoek dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

Publisher: Eindhoven University of Technology
Author: Hans W. Pflug
Printed by: Gildeprint
Cover design: Esther Poulissen, Sterdesign
ISBN: 978-90-386-5714-1
NUR: 959 — Electrical Engineering
A catalogue record is available from the Eindhoven University of Technology Library.

Contents

Acronyms

ADS Advanced Design System 10
CANCER Computer Analysis of Nonlinear Circuits, Exlcuding Radiation . 44
COTS commercial off-the-shelf 8
CW Continuous Waveform 41
DAC ADS data access component 167
dc direct electrical current 3
DFT discrete Fourier transform 42
ECC European Communication Committee 155
EIRP effective isotropic radiated power 156
EM electromagnetic 1
ERP effective radiated power 156
ETE energy transfer efficiency 27
FET field effect transistor 163
FDD frequency-domain defined device 36
HB Harmonic Balance 10
IDFT inverse discrete Fourier transform 16
IEEE Institute of Electrical and Electronics Engineers 155
imec Interuniversity Microelectronics Centre 5
IoT Internet of Things 4
ISM industrial, scientific and medical 155
JEDEC Joint Electron Device Engineering Council 79
KCL Kirchoff's current law 42
MDIF ADS measurement data interchange format 167
MPP maximum power point 162

MPPT	maximum power point tracking	162
MS	metal-semiconductor	50
NRMSE	normalized root mean square error	65
OC	open circuit	162
PCB	printed circuit board	42
PCE	power conversion efficiency	4
rms	root mean square	19
RF	radio frequency	5
RFID	radio-frequency identification	156
SBD	Schottky barrier diode	2
SDD	symbolically defined device	75
SMD	surface-mounted device	159
SOT	small outline transistor	79
SPICE	Simulation Program with Integrated Circuit Emphasis	1
SRD	short-range device	155
TI	Texas Instruments	160
ULP	Ultra Low Power	4
WEH	wireless energy harvesting	4
WET	wireless energy transfer	1
WPT	wireless power transfer	3
WSN	wireless sensor network	2

List of Symbols

Latin Letters

A	diode junction area	m^2	50
a	I_S temperature coefficient	K^{-1}	51
a_f	flicker noise exponent		47
A_R	diode effective Richardson constant	$A/m^2/K^2$	50
C'_{j0}	C_{j0} at T'	F	56
C_j	diode capacitance	F	56
C_{j0}	zero-bias junction capacitance	F	47
d_i	Russell method data point i		63
E	electric field	V/m	52
eV	Electron volt 1.60218×10^{-19}	J	47
f_0	fundamental frequency	Hz	12
FC	junction capacitance coefficient		47
G_i	impedance efficiency factor		127
g_j	diode conductance	$\mho$	93
G_m	gain mismatch factor		36
GMIN	minimum conductance. default: 10^{-12}	$\mho$	55
h	harmonic term $\{0,1,2,\cdots\}$		89
h_0	dc harmonic index		89
h_1	odd harmonics index		89
h_2	even harmonics index		89
i	harmonic approximation summation index		89
i_{sc}	short circuit current	A	112
I_B	current at breakdown voltage	A	47
I_d	diode current	A	45
I_j	diode junction current	A	45
I_r	reverse bias diode current	A	52
I_s	diode saturation current	A	45
I'_s	diode saturation current at T'	A	51
k	maximum number of harmonics taken into account		16

k_B	Boltzmann's constant 1.38065×10^{-23}	J/K	51
k_f	flicker noise coefficient		47
L_η	Efficiency loss factor		126
m	junction grading coefficient	V	47
n	diode emission coefficient		45
N_D	donor impurity density	cm^{-3}	52
P_{CCM}	complex conjugately matched source		28
P_{in}	active power flowing into a circuit input port	W	24
P_{out}	active power flowing out of a circuit output port	W	24
P_d	diode power dissipation	W	111
p_i	I_S temperature exponent		51
P_s	source power level	W	11
q	elementary charge 1.60218×10^{-19}	C	51
Q_d	diffusion charge	C	55
$\Re_I$	diode current responsitivity	A/W	112
$\Re_{I_0}$	diode quadratic current responsivity	A/W	181
R_j	diode junction resistance	Ω	26
R_L	Rectifier load resistor resistance	Ω	24
R_s	diode series resistance	Ω	45
S	S-parameter matrix		36
$S_{R_L}^{\eta}$	normalized η sensitivity to R_L		96
$S_{R_L}^{P_{\mathrm{act}}}$	normalized P_{act} sensitivity to R_L		96
T	physical temperature	K	51
T'	reference temperature (SPICE2 default: 300 K)	K	51
T_0	parameter specification temperature	°C	47
V_B	breakdown voltage	V	47
V_j	diode junction voltage (without R_s)	V	45
V_s	source voltage amplitude	V	10
V_T	thermal voltage kT/q	V	45
V_{bi}	build-in potential	V	52
W_0	principal branch of the Lambert W function		47
Z''_{in}	circuit impedance at higher frequencies	Ω	119
Z'_{in}	circuit impedance at lower frequencies	Ω	119
Z_0	characteristic or default impedance	Ω	20
Z_s	source impedance	Ω	10
Z_x	impedance with arbitrary complex value	Ω	35
Greek Letters			
α	energy gap material parameter	eV/K	57
β	energy gap material parameter	K	57
Δ	linear detection deviation factor		182

δ_{Pg}	percent source output power error	%	37
ϵ_{NRMS}	normalized root mean square error (NRMSE)		65
ϵ_i	normalized error		65
ϵ_s	semiconductor permittivity	F/cm	52
η	energy transfer efficiency		27
η_{boost}	boost-converter and storage capacitor η		167
η_{buck}	buck converter η		167
η_{harv}	harvester η		167
η_{opt}	optimal η		101
η_{rect}	matched rectifier η		165
η_{stor}	$\eta_{\text{rect}}\eta_{\text{boost}}$		167
Λ_L	diode dc-offset calculation term $\frac{I_s R_L}{nV_T}$		91
Λ_d	diode equation term $\frac{V_d}{nV_T}$		47
Λ_s	diode equation term $\frac{I_s R_s}{nV_T}$		47
Λ_0	diode equation dc-offset term $\frac{\langle V_j \rangle_0}{nV_T}$		88
Λ_1	diode equation fundamental amplitude term $\frac{\langle V_j \rangle_1}{nV_T}$		87
ϕ'_B	ϕ_B at T'	V	56
ϕ_B	Schottky junction potential	V	51
ϕ_{B0}	Schottky junction potential including V_j sensitivity	V	52
ψ	MS Schottky energy gap	eV	51
ψ'	ψ at T'	eV	51
ψ_0	gap's width extrapolated to $T = 0$ K	eV	57
τ_d	average transit time	s	55

Summary

The still emerging field of wireless energy transfer can roughly be divided in two categories: the one providing energy to relatively low power sensor devices, typically bridging distances of several meters, and the one of inductive transfer — typically used at distances below a meter at various power levels, from electric toothbrushes to electric vehicles. The first category makes use of antennas and electromagnetic (EM) waves and is therefore called *radiative* wireless energy transfer (WET). The second category uses typically inductors to transfer a dominantly magnetic field and is referred to as *inductive* WET. This work focusses on the radiated category, where the receiving side can be analysed without taking the transmitting side into account. The focus will be on the rectifying circuit, making use of semiconductor discrete diodes. All insights obtained in this work are also usable in the inductive, second category.

To be able to design an optimal rectifier circuit, insight into the rectifier operation is required. The non-linear nature of a rectifying device calls for the use of a circuit simulator. The important quantity in WET is the rectifier efficiency, which is typically simulated using a standard Simulation Program with Integrated Circuit Emphasis (SPICE) *pn*-junction diode model based on manufacturer supplied SPICE-model parameters. To provide more insight in and to be able to optimize the design of the rectifier circuit, this work addresses the following topics:

Rectifier analysis. Three *methods* are presented. a) WET systems include a non-linear element, the rectifier, to obtain a dc output signal. In systems with large signal levels, the topics of impedance definition and matching are of special interest. The method of time-domain trajectory impedance analysis is described to provide more insight in the time dependent rectifier impedance. b) The optimization of a non-linear rectifier circuit for optimal efficiency is not straightforward. An adaptive simulation source to aid in optimization is presented. This simultaneously provides a method to objectively compare diode types as well as rectifier topologies. c) An ideal rectifier circuit is discussed, which eases the basic understanding of the rectifier topic. This ideal rectifier is used in following chapters.

Diode model. Two aspects are covered. a) The choice of simulation domain: time or frequency. b) The typical WET rectifier used is based on a Schottky barrier diode (SBD), which has different properties compared to the *pn*-junction diode. In SPICE the only available diode model is a *pn*-junction diode model. Alternative Schottky barrier diode (SBD) models are introduced, including temperature effects, the diode package and model parameter spread.

Rectifier efficiency optimization. To design for optimal *rectifier efficiency*, several aspects are discussed. a) Finding the optimal rectifier load resistance. b) The properties of the rectifier input impedance. c) Defining the diode dissipation. d) The diode model parameters and temperature relation to the rectifier efficiency.

Optimal topology. The choice for the optimal topology is discussed by comparing different *rectifier circuit topologies*. Next to the peak detector topology, the Villard-, Greinacher- and Graetz families are discussed. A comparison shows that efficiency is not the main differentiator between the topologies.

Application. A *far field application* provides a practical example. A wireless sensor network (WSN) application is provided including a power management example. The design is compared with a commercial off-the-shelf (COTS) product.

Chapter 1

Introduction

1.1 History

In the late 19th century, Nikola Tesla introduced the idea of the transmission of electrical energy. He described the freedom to transfer energy between two points without the need for a physical connection to a power source [1, 2]. Alternating electromagnetic fields are used for the transfer from transmitter to receiver. In most cases of wireless energy usage, a rectifier is required on the receiving side to obtain a direct electrical current (dc). Since the early days, the diode has been the rectifying element in these circuits. Many persons contributed to the development of vacuum tube (thermionic) diodes and semiconductor (solid state) diodes. The two different diode structures where discovered around the turn of the 20th century [3, 4]. Rectifiers played an important role in early 20th century electronics. As an example: by 1928 Philips[1] had six product groups of which one focussed on rectifiers (product group Industry 1) [5].

In the early 1960s inductive wireless energy transfer was used successfully in implantable medical devices, like pacemakers and artificial hearts [6].

In 1964, William Brown demonstrated a practical application of radiative power transfer, in the form of a microwave-powered model helicopter [7]. Recently in 2008 non-radiative, resonant coupling wireless power transfer (WPT) has been intoduced by Karalis et al. [8, 9]. The non-resonant version of this technology is now becoming commercially available for charging smart phones wirelessly on a short distance (millimeters). For longer distances (meters) we need to apply radiative power transfer as Brown did. For consumer applications we are limited though by restrictions on the allowed Effective Isotropic Radiated Power (EIRP) to avoid interference [10] and negative health aspects [11].

The still emerging field of wireless energy transfer can roughly be divided in

[1] current official name 'Koninklijke Philips N.V.', at that time 'N.V. Philips Gloeilampenfabrieken'.

two categories: the one providing energy to relatively low power sensor devices, typically bridging distances of several meters, and the one of inductive transfer - typically used at distances below a meter at various power levels, from electric toothbrushes to electric vehicles. The first category makes use of antennas and EM waves and is therefore called *radiative* WET [12]. The second category uses typically inductors to transfer a magnetic field and is referred to as *inductive* WET [13]. In Radiative WET the received power levels are very low. To get optimal rectifier performance a special analysis is required, which is what will be discussed in this work. An advantage of this category is: the receiving side can be analysed without taking the transmitting side into account, as they are far apart. The focus will be on the rectifying circuit, making use of semiconductor discrete diodes.

1.2 Modern Developments

Over the last years, the Internet of Things (IoT) concept has emerged, in which physical objects are connected to the internet without the need for human interaction [14]. Key in this concept is a long term, self-sustainable operation for a rapid growing amount of devices. Energy aware devices are preferred, capable of harvesting their required energy from ambient sources. Far-field wireless energy harvesting (WEH) is, among other methods, one of the most promising techniques for its ease of implementation and availability [15]. A logical step towards WEH is WET — commonly known as WPT[2] — making use of intentional RF transmitting energy sources. The current trend in the reduction of consuming devices' energy consumption paired to an increase in WET circuitry efficiency will make IoT based on WEH feasible. The power needed to perform a task requiring a fixed number of computations for example will fall by half every 1.5 years [16]. Examples of Ultra Low Power (ULP) applications [17–33].

The benefit of using RF signals over e.g. solar cells is three-fold: RF signals can be co-used for communication, they are ubiquitous available in most urban environments, day and night, and they propagate through more materials as daylight does [34].

Typical IoT applications span a wide range of fields including smart buildings, healthcare, transportation, agriculture and surveillance [35]. Supplying energy to this rapid growing system is a dominant implementation barrier. WET is seen as a promising approach for IoT powering. WET works by rectifying an RF signal, that is received by an antenna. To achieve a high RF-to-dc power

[2] In this work we prefer to use the term wireless *energy* transfer instead of wireless *power* transfer. Where power cannot be stored, energy can. Also energy can be converted from e.g. chemical (battery) to electrical (EM-wave) and back, power cannot.

conversion efficiency (PCE) of the WET circuitry, an objective topology comparison for WET circuits is required. This calls for realistic circuit models and an objective analysis technique [36].

1.3 Wireless Sensor Nodes

A generic type of electronic circuit, used in the above mentioned IoT applications is the wireless sensor network (WSN). For WSNs, network life time is an import parameter [37]. With the predicted high density of sensor nodes in the near future, obtaining power autonomous nodes will be key in achieving low cost solutions — think for example of regularly checking and replacing batteries on hundreds of nodes in a building [38]. One way to realize this is by using radio frequency (RF) energy transfer to transport the required energy over a distance up to about 5 to 10 meters.

In a radiative WET system, the energy is transferred from an intentional or unintentional source and received in the far-field region of the transmit antenna by a receiving antenna, capturing part of the radiated energy [39]. The typical useful receiver input power level for IoT and WSN application ranges from -15 to -5 dBm [40]. A block-diagram of such a system is shown in Fig. 1.1. The received RF energy is delivered to an impedance matched rectifier, discrete or integrated. The RF input power level will determine the amount of available dc output energy, which is transferred to an energy storing device by means of a power management circuit. This circuit contains typically a boost converter and voltage stabilizer, providing a higher voltage to efficiently store the received energy. A battery or capacitor is typically used for storage of the energy. An Interuniversity Microelectronics Centre (imec) WET receiver example is shown in Fig. 1.2. The complex conjugately matched antenna is directly connected to a double-diode rectifier stage, followed by a power management circuit. WSNs often operate in a duty cycled mode. For optimal performance and range of operation, still the available energy levels should be maximized. This leads to the research objective of this work.

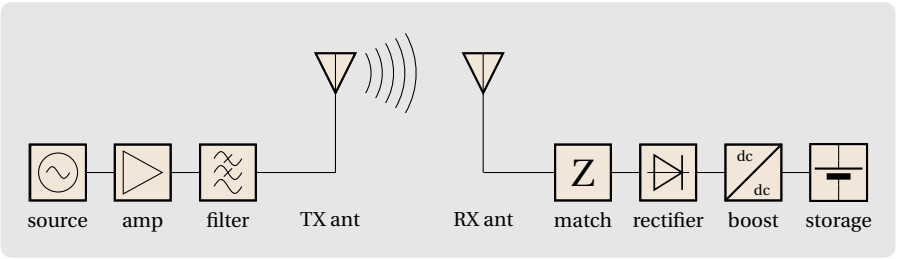


Figure 1.1 Radiative WET system block-diagram, with an intentional source (left) and impedance matched receiver (right). The source typically consists of an oscillator at the carrier frequency (source), an amplifier to obtain the required output amplitude (amp), a low- or band pass filter to suppress the amplifier generated higher order harmonic frequency components (filter) and an antenna to radiate the signal as EM waves (TX ant). The receiver antenna picks up the EM waves (RX ant) followed by an impedance matching circuit (match) after which a rectifying circuit converts the RF signal into a dc current (rectifier). A boost converter increases the voltage level (boost) to efficiently store the energy in a battery or capacitor (storage). The stored energy can be used by e.g. a wireless sensor device.

Research Objective

The primary research objective is the maximization of the rectifier energy transfer efficiency. The rectifier energy transfer efficiency is the ratio of the rectifier dc output energy to the RF input energy. The primary objective can be subdivided into various aspects, which will be covered in the following chapters.

The state-of-the-art work, like e.g. [41–46], is making use of design techniques that still have room for improvement. This work discusses several areas for improvement for the WET application: usage of an adaptive source in simulation for improved efficiency optimization and a more objective diode and rectifier topology comparison, improved diode models for more accurate rectifier impedance prediction and a thorough rectifier efficiency analysis leading to different insights in the choice of diode, load resistance and rectifier topology.

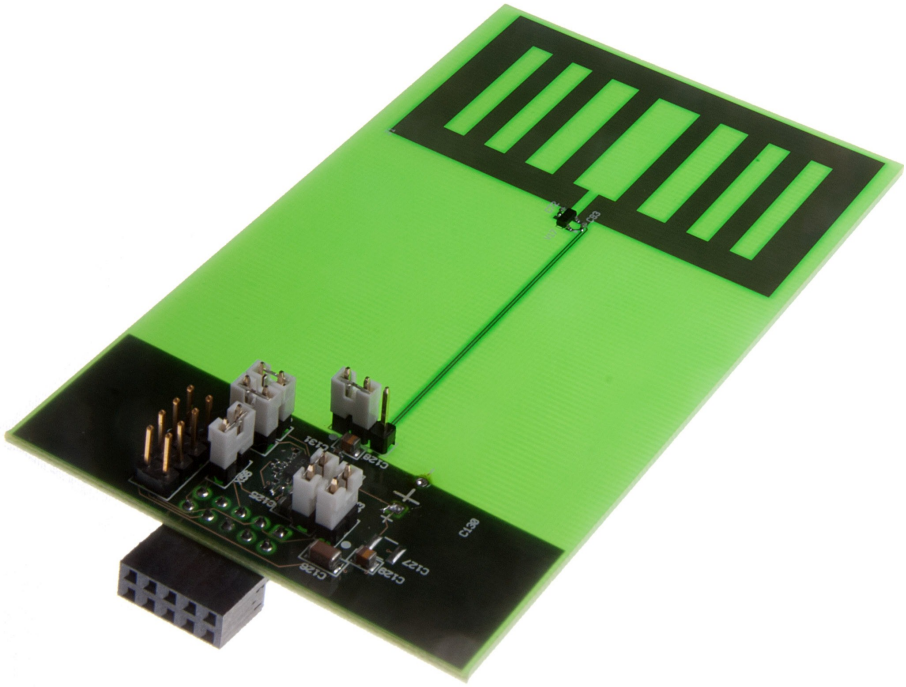


Figure 1.2 Imec WET receiver example consisting of an antenna (top-right), impedance matched to the rectifier stage, which is connected to a power management circuit (bottom-left) and connections for storage and usage of the rectified energy. [photo: H.J. Visser].

1.4 Organization of the Thesis

To be able to design an optimal rectifier circuit, more insight is required. The non-linear nature of a rectifying device calls for the use of a circuit simulator. The important quantity in WET is the rectifier efficiency, which is typically simulated using a standard SPICE *pn*-junction diode model based on manufacturer supplied SPICE-model parameters. To provide more insight in the design of the optimal rectifier circuit, the next chapters will address the following:

Chapter 2 — Methods: Three *methods* are presented. a) WET systems include a non-linear element, the rectifier, to obtain a dc output signal. In systems with large signal levels, the topics of impedance matching and -definition are of special interest. The method of time-domain trajectory impedance analysis is described to provide more insight in the time dependent rectifier impedance [47]. b) The optimization of a non-linear rectifier circuit for optimal efficiency is not straightforward, as its load resistance affects both efficiency and its input impedance. An adaptive simulation source to serve this purpose is presented. This simultaneously provides a method to objectively compare diode types and rectifier topologies [13, 48]. c) An ideal rectifier circuit is discussed, which eases the basic understanding of the rectifier topic and is used in following chapters.

Chapter 3 — Diode Model: For the *diode model*, two aspects are covered. a) The choice of simulation domain: time or frequency. b) The typical WET rectifier used is based on a Schottky barrier diode (SBD), which has different properties compared to the *pn*-junction diode. In SPICE the only available diode model is a *pn*-junction diode model. Alternative SBD models are covered, including temperature effects, the diode package and model parameter spread [36, 48].

Chapter 4 — Rectifier Efficiency: To design for optimal *rectifier efficiency*, several aspects are discussed. a) Finding the optimal rectifier load resistance. b) The properties of the rectifier input impedance. c) Defining the diode dissipation. d) The relation of the rectifier efficiency to the diode model parameters and temperature.

Chapter 5 — Rectifier Circuits: The choice for the optimal topology is discussed by comparing different *rectifier circuit topologies*. Next to the peak detector topology, the Villard-, Greinacher- and Graetz families are discussed. A comparison shows that efficiency is not the main differentiator between the topologies [13].

Chapter 6 — Far Field Application: A *far field application* provides a practical example. A WSN application is provided including a power management example and an alternative approach. The design is compared with a commercial off-the-shelf (COTS) product [40].

Chapter 7 — Conclusions & Recommendations: The *conclusions and recommendations* are summarized in the final chapter of this work.

Chapter 2

Methods

Before diving into the details of wireless energy transfer rectifiers, a few methods are covered in this chapter. The first one will help in studying and understanding the involved non-linear rectifier circuits, which involves the use of the impedance time trajectory. The presented ideal rectifier circuit, i.e. the second method, will ease the analysis of diode rectifier properties. The third method forms a foundation for the subsequent chapters on how to optimize for optimal energy transfer efficiency.

2.1 Energy Transfer and Complex Impedances

With the topic of WET there is typically a rectifier circuit involved, which is a non-linear circuit by definition. The rectifying elements have parasitic effects in the form of inductance and capacitance, which play a role with the use of ac-signals. This makes that we are dealing with complex impedances. For the design and analysis of these rectifying circuits, it is beneficial to describe the circuit behaviour both in the frequency and in the time domain. In this section we will introduce the notation used in this work, we will calculate active power, used to provide an insight in the energy flow in both domains within a circuit and we will show how to obtain an impedance time trajectory. We will see that rectifier impedances are time-variant and the time- and frequency domain views on these will be brought together.

2.1.1 Time domain view

In time-domain, the instantaneous power flowing into a circuit port is defined as

$$p(t) = v(t)i(t), \tag{2.1}$$

see Fig. 2.1 for an example circuit with time domain voltages and currents at various locations [49].

This applies to all waveforms, also the non-sinusoidal ones, like in rectifier circuits. It applies to any circuit element type. E.g. in a reactive circuit, the voltage and current are not proportional, meaning they are not in phase. With non-linear circuit elements, the voltage and current phase difference can even change during the cycle of the input signal. Therefore it is useful to calculate the average power over the complete cycle, with duration T. This gives the active power, the power flowing into a circuit port, regardless of the harmonic content of the waveforms:

$$P_{\text{act}} = \frac{1}{T}\int_T v(t)i(t)\mathrm{d}t. \tag{2.2}$$

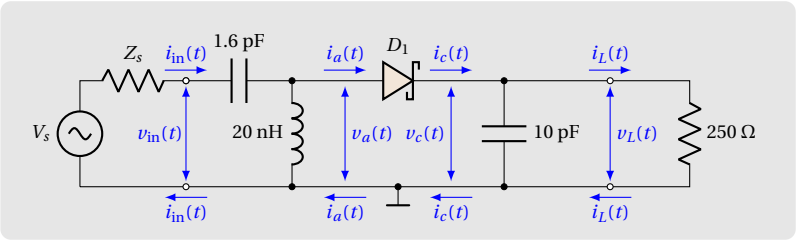


Figure 2.1 Example single diode or peak detector rectifier circuit with, shown in blue, the time domain voltages and currents at (in) the circuit input port, (a) the diode anode side and (c) cathode side and (L) the load side of the circuit. Note that $i_a(t) = i_c(t)$ and $v_c(t) = v_L(t)$. V_s is the source voltage amplitude and Z_s the source impedance.

The time domain active power includes the complete harmonic content of the signals. This means that not only the fundamental (wanted) signal at the input is accounted for, but also the non-wanted[1] higher order harmonic frequency components. The circuit of Fig. 2.1 is simulated using Advanced Design System (ADS) [50], see Fig. 2.2. Although the Harmonic Balance (HB) simulation engine used in ADS is a frequency domain simulation, time domain information can be obtained using the ADS function *ts()*, which performs a frequency-to-time domain transform. From this simulation, the active power values at the four different circuit locations (*in*, *a*, *c* and *L*) are calculated and listed in Table 2.1. Although this circuit is properly impedance matched to the source impedance ($|\Gamma_{\text{in}}| = -29.4$ dB), the active circuit input power is almost 0.5 dB less than the source power P_s (+10 dBm[2]). To understand this, we need

[1] These terms are non-wanted as they are generated by the diode and do not contribute to a dc current in the load resistor, as they are shorted to ground by the capacitor.

[2] The expected mismatch-loss is only $10\log\left(1-|\Gamma|^2\right) = -0.005$ dB.

Table 2.1 Active power example for the peak detector circuit in Fig. 2.1 and Fig. 2.2, at P_s = +10 dBm and f_0 = 915 MHz, using an Avago HSMS-2850 SPICE diode model.

	$P_{\text{act,in}}$ (dBm)	$P_{\text{act,a}}$ (dBm)	$P_{\text{act,c}}$ (dBm)	$P_{\text{act,}L}$ (dBm)
P_{act}	+9.53	+9.53	+7.54	+7.54

to distinguish between the different harmonic frequency components. To do this we have to analyse the circuit behaviour in the frequency domain.

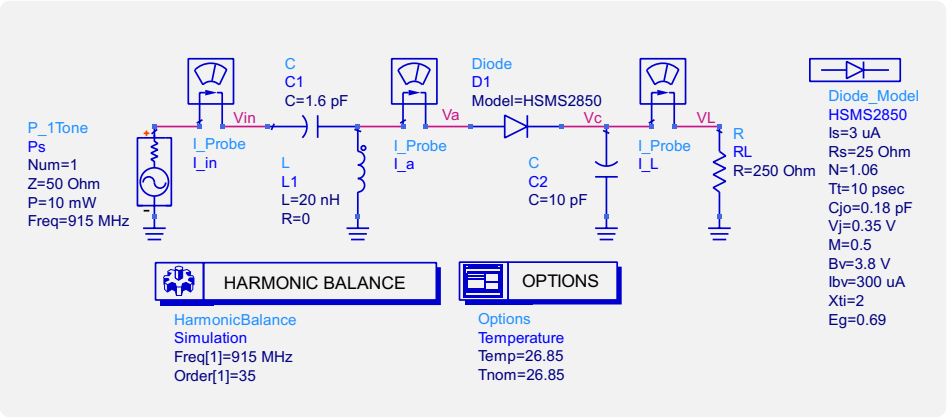


Figure 2.2 ADS implementation of the example peak detector rectifier circuit shown in Fig. 2.1.

The reason that $P_{\text{act,in}}$ and $P_{\text{act,a}}$ are equal in Table 2.1 is that C_1 and L_1 (see Fig. 2.2) are ideal components; they don't give rise to energy loss due to resistive dissipation. The same is true on the other side of the diode ($P_{\text{act,c}} = P_{\text{act,L}}$), as C_2 is also an ideal capacitor.

2.1.2 Frequency domain view

The typical use of sinusoidal source signals and the generation of higher order harmonics in a diode, make using the frequency domain a logical choice for WET rectifier circuits analysis. The signals can be described with enough detail, in a compact form, using a limited number of harmonic frequency components. The intended conversion from the fundamental frequency to dc can be easily analysed.

h-phasors and time trajectory

In this work, $\langle \mathbf{A} \rangle_{\mathbf{h}}$ will be used to represent the complex phasor $Ae^{j\alpha}$, which is a static complex number corresponding to the function $Ae^{j(h\omega_0 t+\alpha)}$, with amplitude A, harmonic frequency number index h, $\omega_0 = 2\pi f_0$, time t and phase α. f_0 is the fundamental frequency. The phasor notation is used to ease the indexing of specific harmonic frequency coefficients [51]. For example, $\langle A \rangle_1$ is the 1-phasor which represents a signal at the fundamental frequency f_0 (as $h = 1$), with amplitude A. Time-constant amplitudes will be designated with an upper-case symbol in this work, time varying amplitudes and instantaneous signal values with a lower-case symbol. So we will use e.g. $\langle A \rangle_h$, $\langle a \rangle_h(t)$ and $a(t)$. Time varying complex values will be designated with a lower case symbol with a hat: $\hat{\mathbf{a}}(\mathbf{t})$. This is indicated as a *time trajectory function*.

Fig. 2.3 shows the circuit of Fig. 2.1 with frequency domain voltages and currents indicated at various locations. For each frequency index h, a complex value exists for the voltage and current.

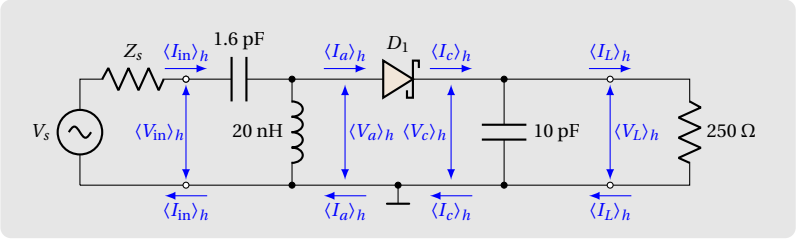


Figure 2.3 Example peak detector rectifier circuit with, shown in blue, the frequency domain voltage and current phasors at (in) the circuit input port, (a) the diode anode side and (c) cathode side and (L) the load side of the circuit. Note that $\langle I_a \rangle_h = \langle I_c \rangle_h$ and $\langle V_c \rangle_h = \langle V_L \rangle_h$.

Table 2.2 provides an overview of the voltage and current phasor amplitudes, indicated in Fig. 2.3, using a sinusoidal +10 dBm circuit input power at 915 MHz and a HSMS-2850 SPICE model for the SBD.

For WET rectifier circuit design, an optimal energy transfer is a design goal. Therefore, we will now show how to calculate the active power at different locations in the circuit. Thus, we will provide a frequency domain view on the energy flow through the rectifier circuit[3].

[3] An indirect method can also be used, using power waves [47, 52, 53]

Table 2.2 Simulated voltages and currents corresponding to the peak detector example circuit in Fig. 2.1, Fig. 2.2 and Fig. 2.3 for a sinusoidal input signal with a $P_s = +10$ dBm and $f_0 = 915$ MHz, using an Avago HSMS-2850 SPICE diode model. The other circuit elements are modelled as ideal components.

h	$\lvert\langle V_{\text{in}}\rangle_h\rvert$ (V)	$\lvert\langle I_{\text{in}}\rangle_h\rvert$ (mA)	$\lvert\langle V_a\rangle_h\rvert$ (V)	$\lvert\langle I_a\rangle_h\rvert$ (mA)	$\lvert\langle V_L\rangle_h\rvert$ (V)	$\lvert\langle I_L\rangle_h\rvert$ (mA)
0	0.00	0.00	0.00	4.74	1.19	4.74
1	1.01	19.8	2.44	8.78	0.15	0.61
2	0.30	6.05	0.45	4.80	0.04	0.17
3	0.09	1.77	0.11	1.60	0.01	0.04

Active power

The *active power* P_{act} entering a circuit port, can be obtained for each harmonic component as[4]:

$$P_{\text{act}}^h = \frac{1}{2}\,\text{Re}\left(\langle V\rangle_h \langle I\rangle_h^*\right), \tag{2.3}$$

in which the symbol * denotes the complex conjugate operation.

Table 2.3 shows the active power levels of the example circuit for the various locations in the circuit. Notice the equal values for the two pairs of active power locations. This equality changes when the components in between the circuit locations (1.6 pF capacitor, 20 nH inductor and 10 pF capacitor) include a parasitic resistance, which will be the case in reality. The summed active input power value (+9.53 dBm) is lower than the power entering the circuit at the fundamental frequency (+10 dBm). This is a result of all non-fundamental harmonic components being negative in direction sign (reflected energy), which is not visible when converting the values in dBm[5].

The simulation is setup such, that at the fundamental frequency, +10 dBm is injected into the circuit input port. Due to the non-linear rectifier diode, this energy is partly converted to other frequency components, which are flowing in the opposite direction, i.e. towards the source. This makes that the total

[4] We use the notation P^h instead of $\langle P\rangle_h$ as power is expressed as a real value, only having a sign corresponding to the direction of power flow.

[5] In this case we only use $\sum_{h=0}^{3} P^h$ instead of $\sum_{h=0}^{\infty} P^h$, as the higher order harmonics ($h > 4$) are not significant in this example and therefore left out of the equation.

Table 2.3 Active power levels for the circuit in Fig. 2.2, at $P_s = +10$ dBm and $f_0 = 915$ MHz, using an Avago HSMS-2850 SPICE diode model.

h	$P^h_{\text{act,in}}$ (dBm)	$P^h_{\text{act,a}}$ (dBm)	$P^h_{\text{act,c}}$ (dBm)	$P^h_{\text{act},L}$ (dBm)
0	–	–	+7.50	+7.50
1	+10.0	+10.0	−13.3	−13.3
2	−0.39	−0.39	−24.6	−24.6
3	−11.1	−11.1	−37.6	−37.6
$\sum$	+9.53	+9.53	+7.54	+7.54

power entering the circuit at the input port is less than +10 dBm. In the example circuit of Fig. 2.1, the higher order harmonic energy is dissipated in the source impedance. For the WET application, the interest is in how well the active power at the input port at frequency f_0, which is $P^1_{\text{act,in}}$, is converted into a dc power at the output port $P^0_{\text{act},L}$. This makes that the higher order harmonic components at the input are not of interest for the calculation of energy transfer efficiency[6]. In this work we use P^1_{in} as short for $P^1_{\text{act,in}}$ and P^0_L as short for $P^0_{\text{act},L}$. Having the frequency domain active power values, provides a useful insight in designing an optimal rectifier circuit, as will be explained later.

The fundamental frequency impedance of a circuit port is given by:

$$\langle Z \rangle_1 = \frac{\langle V \rangle_1}{\langle I \rangle_1}. \tag{2.4}$$

Going back to the time domain: the instantaneous port impedance is changing in time for a rectifier circuit, due to its non-linear behaviour. Not only the phase difference between voltage and current varies within a fundamental frequency cycle, also the amplitude ratio. In order to visualize this 'wobbling impedance' around $\langle Z \rangle_1$ in time, a time trajectory impedance function $\hat{\mathbf{z}}(\mathbf{t})$ is defined[7].

This step is taken, as the traditional way of looking at voltages and currents in the time domain has its limitations. Fig. 2.4 shows the input voltage and current signals corresponding to Fig. 2.2. It is not intuitive to obtain the circuit

[6] The higher order harmonic components, dissipated in the source impedance, might result in unwanted radiation if the source represents the WET receiver antenna.

[7] The 'hat'-notation $\hat{}$ indicates a time-varying complex value.

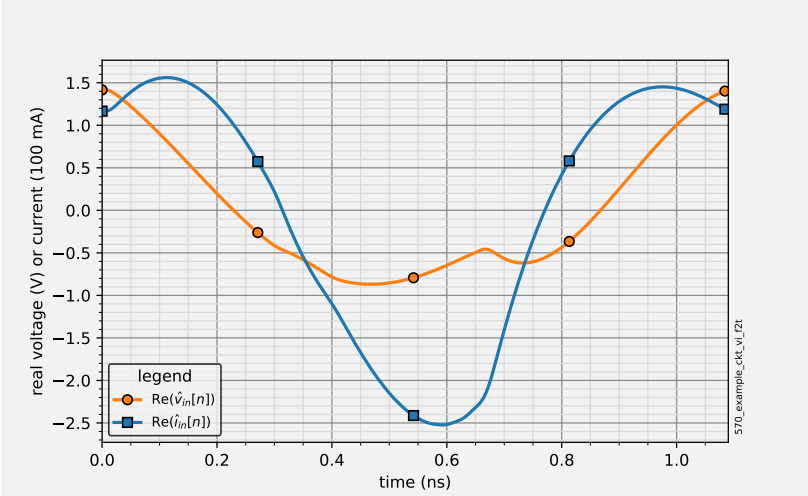


Figure 2.4 Example peak detector rectifier simulation result (see Fig. 2.2) showing: the input voltage- and current signals $\mathrm{Re}(\hat{v}_{in}[n])$ and $\mathrm{Re}(\hat{i}_{in}[n])$, calculated from the HB simulation frequency domain result, using 35 harmonics of the fundamental frequency f_0. $P_{\mathrm{forw}} = +10$ dBm and $f_0 = 915$ MHz, using an Avago HSMS-2850 SPICE diode model. Using a time domain simulator will obtain the same result.

input impedance from this graph. The signals are not sinusoidal and the signal peaks are at different moments in time for voltage and current. Due to the zero crossings it is obvious that taking the ratio of the two does not result in the circuit input impedance.

With the design challenge of an optimal performing rectifier in mind, we will see how to calculate the instantaneous impedance using a time trajectory, obtain a common value from this as design input value and relate this variation in the time domain to the 'missing' energy in the frequency domain of Table 2.3.

2.1.3 Impedance time trajectory

In order to define and simulate the instantaneous impedance of a complex circuit, it is convenient to describe and visualize the voltages and currents as complex valued time trajectories.

Before introducing these time trajectories, we will first look at time numeric sequences. In a transient simulator, time-continuous voltage and current information (the real-world signals) is represented by discrete-time numeric sequences of real valued floating point numbers: $[v_0, v_1, v_2, \cdots, v_{N-1}]$ and $[i_0, i_1, i_2, \cdots, i_{N-1}]$ at equally spaced time instances $[t_0, t_1, t_2, \cdots, t_{N-1}]$. This is also the case for frequency to time converted information in a frequency domain

simulator. Following the Nyquist-Shannon sampling theorem [54, 55], a sufficient sample-rate is $2kf_0$ samples/second, or anything larger, when the signal contains no frequencies higher than kf_0 Hertz. k is the maximum number of fundamental frequency harmonics taken into account. The sample frequency (f_s) should be an integer multiple of the fundamental frequency to obtain useful Fourier transformation results and can be adjusted to the number of harmonics taken into account. At a circuit port, the voltage and current sequences are defined as

$$\begin{aligned} v[n] &= v(nT_s), \qquad n = 0, \cdots, N-1 \qquad n \in \mathbb{N}^0 \\ i[n] &= i(nT_s), \qquad n = 0, \cdots, N-1 \qquad n \in \mathbb{N}^0 \end{aligned} \tag{2.5}$$

with N being the number of time samples used, $T_s = 1/f_s$ being the sample interval and $\mathbb{N}^0 = \{0, 1, 2, 3, \cdots\}$ the set of natural numbers including zero.

Voltage- and current time trajectories

The discrete versions of the complex *voltage* $\hat{\mathbf{v}}(\mathbf{t})$ *and current* $\hat{\imath}(\mathbf{t})$ *time trajectories* are constructed from the frequency domain h-phasors using the inverse discrete Fourier transform (IDFT). Using $T_s = 1/f_s = 1/(Nf_0)$ with $N = 2k$, the time trajectories are:

$$\hat{v}[n] = \sum_{h=0}^{N-1} \langle V \rangle_h e^{jh\omega_0 nT_s}, \quad \hat{\imath}[n] = \sum_{h=0}^{N-1} \langle I \rangle_h e^{jh\omega_0 nT_s}, \tag{2.6}$$

in which ω_0 is equal to $2\pi f_0$, $\langle v \rangle_h$ and $\langle i \rangle_h$ are the h-phasors for the respective harmonic components. The real-valued simulator results, typically provided in a circuit simulator, are equal to the real-parts of the complex-valued time trajectories: $v[n] = \mathrm{Re}(\hat{v}[n])$ and $i[n] = \mathrm{Re}(\hat{\imath}[n])$. [8]

For the example circuit of Fig. 2.1, these complex valued voltage and current time trajectories are shown in polar form in Figs 2.5 and 2.6. The trajectories are normalized, see the figure captions for details. This shows nicely how both $\hat{v}_{\mathrm{in}}[n]$ and $\hat{\imath}_{\mathrm{in}}[n]$ fluctuate around an amplitude of one (marked 'linear' in the figure), due to the higher order harmonics. The centre point of the trajectories is the centre of the polar figure as no dc component is present due to the series input capacitor. Over a complete cycle, both trajectories have an average magnitude value of one. The two figures also show how the impedance matching circuit (C_1, L_1) not only changes voltage and current values, it also changes the phase of the signals. The positive peak in the diode current occurs around a trajectory period

[8] This method is similar to the multi-harmonic load-pull concept [56], also known as X-parameters [57], where the voltage and current information is obtained from the measured power waves a and b.

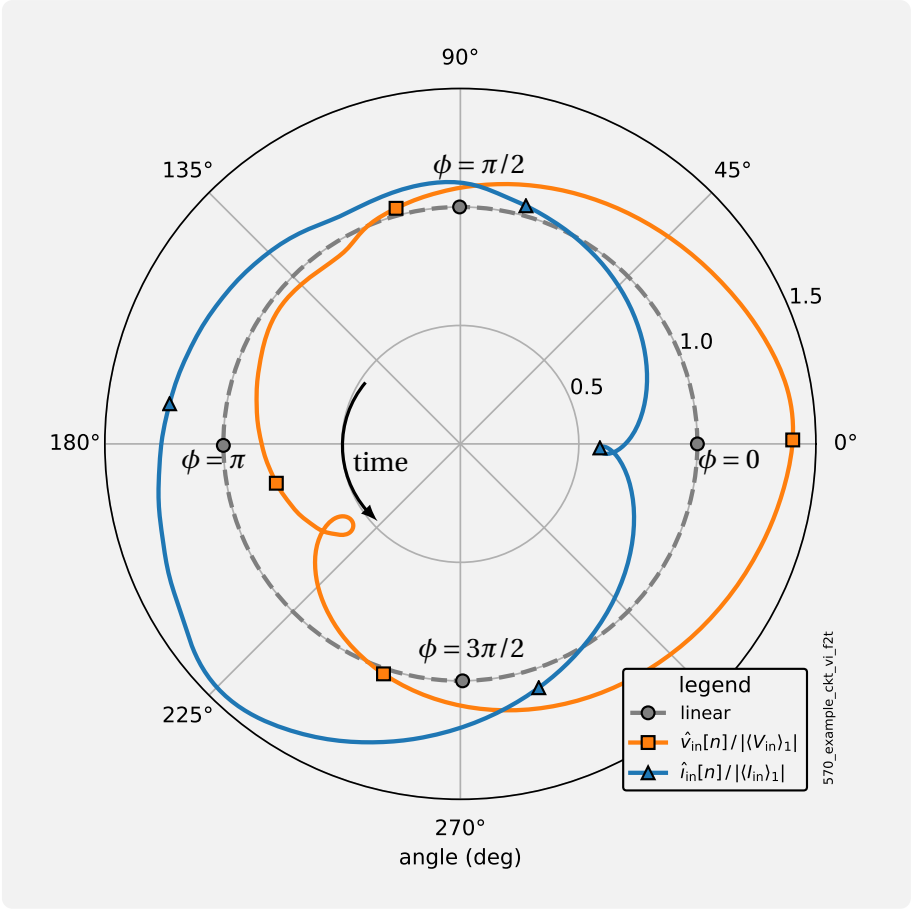


Figure 2.5 Example peak detector rectifier simulation result (see Fig. 2.2) showing: the normalized time trajectory signals $\hat{v}_{in}[n]$ and $\hat{i}_{in}[n]$, calculated from the HB simulation frequency domain result, using $k = 35$ harmonics. $P_{forw} = +10$ dBm and $f_0 = 915$ MHz, using an Avago HSMS-2850 SPICE diode model. $\hat{v}_{in}[n]$ is divided by $|\langle V_{in} \rangle_1| = 1.010$ V and $\hat{i}_{in}[n]$ by $|\langle I_{in} \rangle_1| = 19.814$ mA to obtain the respective normalized values. These signals would be on the 'linear' marked (dashed) amplitude level in case of a linear circuit. The trajectory period phase ϕ is marked for both graphs.

phase $\phi = 3\pi/2$, at the maximum value of $\mathrm{Re}(\hat{i}_a[n])$, where the peak in input voltage occurs at $\phi = 0$. The output voltage and current peak is also at $\phi = 0$.

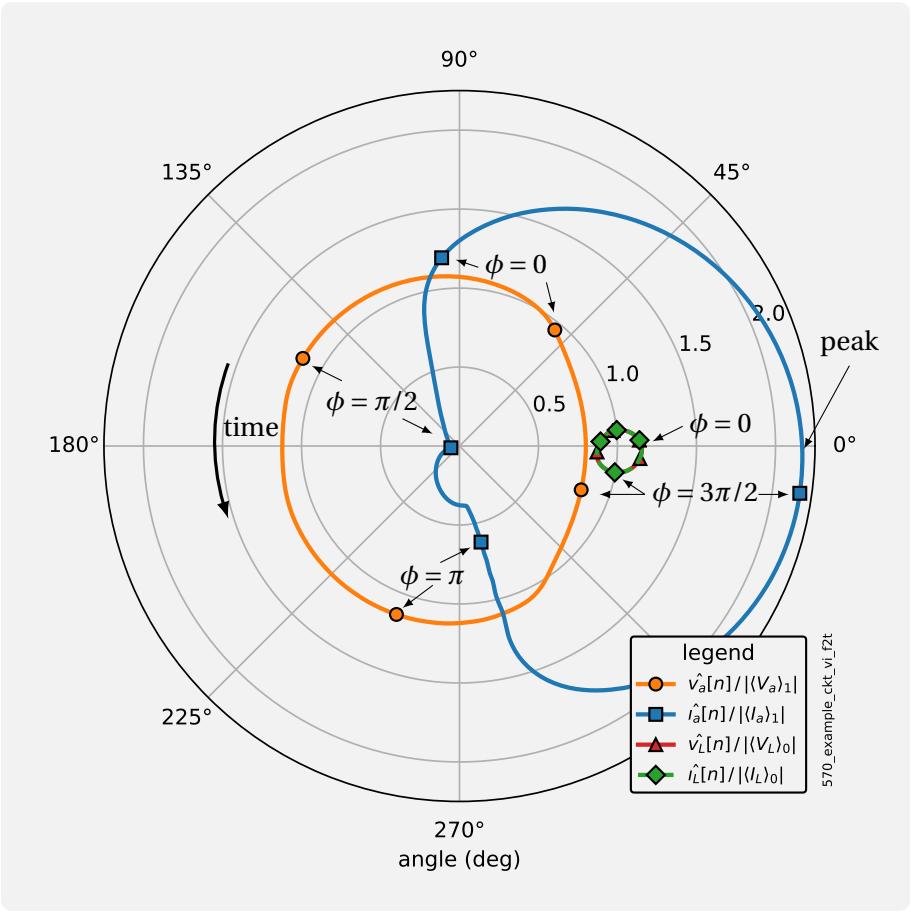


Figure 2.6 Example peak detector rectifier simulation result (see Fig. 2.2) showing: the normalized time trajectory signals $\hat{v}_a[n]$, $\hat{i}_a[n]$, $\hat{v}_L[n]$ and $\hat{i}_L[n]$ (the latter two overlap), calculated from the HB simulation frequency domain result using $k = 35$ harmonics, at $P_{\text{forw}} = +10$ dBm and $f_0 = 915$ MHz, using an Avago HSMS-2850 SPICE diode model. $\hat{v}_a[n]$ is divided by $|\langle V_a \rangle_1| = 2.438$ V, $\hat{i}_a[n]$ by $|\langle I_a \rangle_1| = 8.783$ mA, $\hat{v}_L[n]$ by $|\langle V_L \rangle_0| = 1.185$ V and $\hat{i}_L[n]$ by $|\langle I_L \rangle_0| = 4.742$ mA to obtain the respective normalized values. The trajectory period phase ϕ is marked for the four graphs. The diode current $\hat{i}_a[n]$ positive peak in rectified current occurs after $\phi = 3\pi/2$, at the maximum value of $\text{Re}(\hat{i}_a[n])$ marked *peak*.

Impedance time trajectory

From the voltage- and current time trajectory values, the discrete version of the *instantaneous impedance time trajectory* $\hat{\mathbf{z}}(\mathbf{t})$ is calculated using:

$$\hat{z}[n] = \frac{\hat{v}[n]}{\hat{\imath}[n]}. \tag{2.7}$$

It is insightful to visualize the instantaneous impedance trajectory, but we will not be able to realize a circuit which provides the optimal impedance match in time accordingly. To design a circuit for the proper impedance match we use the mean impedance value. There are different ways to find the mean value of real numbers. For complex numbers this is not the case. The geometric mean is found to be useful to calculate the complex impedance mean value [58], when we use the following definition for the mean of a complex number: a complex mean is a function $m : \mathbb{C}^+ \times \mathbb{C}^+ \rightarrow \mathbb{C}^+$ such that $\min\{|a|,|b|\} \leq |m(a,b)| \leq \max\{|a|,|b|\}$ and for all $a \in \mathbb{C}^+, m(a,a) = a$ where $\mathbb{C}^+ = \{x + jy | x > 0\}$. E.g. the standard arithmetic mean and the power mean or root mean square (rms) do not comply to this definition for all $\mathbb{C}^+$ values.

The geometric mean of two real numbers a and b is found as $\sqrt{ab}$. Applying this to the complex impedance trajectory magnitude, we use

$$\left|\overline{\hat{z}[n]}\right| = \sqrt[N]{\prod_{n=0}^{N-1} \left|\hat{z}[n]\right|}, \tag{2.8}$$

with $z \in \mathbb{C}^+$ where $\mathbb{C}^+ = \{x + jy \,|\, x > 0\}$, with $\mathbb{C}$ being the set of all complex numbers $x + jy$.

When using (2.8) for relatively small values of $|z[n]|$, the product of the magnitude values for large N quickly approaches zero and for larger values of $|z[n]|$ infinity (arithmetic under- and overflow): when e.g. all $z[n]$ values are equal, the product results in $z[n]^N$. For large N and $z[n] < 1$ this leads to very small values, for $z[n] > 1$ to very large values. To prevent this, an equivalent equation is derived and used instead, using logarithmic summation. With the use of

$$\sqrt[N]{b} = \mathrm{e}^{\left(\frac{1}{N}\ln b\right)}, \tag{2.9}$$

Equation (2.8) can be rewritten as

$$\left|\overline{\hat{z}[n]}\right| = \sqrt[N]{\prod_{n=0}^{N-1} \left|\hat{z}[n]\right|} = \mathrm{e}^{\left(\frac{1}{N}\ln\prod_{n=0}^{N-1}\left|\hat{z}[n]\right|\right)}, \tag{2.10}$$

and as

$$\ln(ab) = \ln(a) + \ln(b), \tag{2.11}$$

we can use

$$\ln \prod_{n=0}^{N-1} f(n) = \sum_{n=0}^{N-1} \ln f(n). \tag{2.12}$$

We can now rewrite Equation (2.10) as:

$$\left|\overline{\hat{z}[n]}\right| = \exp\left(\frac{1}{N}\sum_{n=0}^{N-1} \ln\left|\hat{z}[n]\right|\right). \tag{2.13}$$

For the complex mean angle we use [58] as well:

$$\angle\overline{\hat{z}[n]} = \frac{1}{N}\sum_{n=0}^{N-1} \angle\hat{z}[n]. \tag{2.14}$$

Applying this to the example circuit input impedance, we do observe that

$$\overline{\hat{z}[n]} \approx \langle Z\rangle_1, \tag{2.15}$$

which relates the time- and frequency domain impedance view[9]. This eases the design work as we can just make use of $\langle Z\rangle_1$ which is frequency domain simulation output information by having $\langle V\rangle_1$ and $\langle I\rangle_1$ available[10].

Reflection coefficient time trajectory

From the impedance time trajectory, a Möbius transformation is applied to obtain the corresponding *reflection coefficient time trajectory* [59]:

$$\hat{\gamma}[n] = \frac{\hat{z}[n] - Z_0}{\hat{z}[n] + Z_0}, \tag{2.16}$$

where Z_0 is the characteristic impedance. Likewise for the average impedance, to obtain the fundamental frequency reflection coefficient

$$\langle\Gamma\rangle_1 = \frac{\overline{\hat{z}[n]} - Z_0}{\overline{\hat{z}[n]} + Z_0} = \frac{\langle Z\rangle_1 - Z_0}{\langle Z\rangle_1 + Z_0}. \tag{2.17}$$

[9] Since proving an equality in Equation (2.15) is beyond the scope of this work, we use an approximately equal sign.

[10] This method of finding $\langle Z\rangle_1$ and $\overline{\hat{z}[n]}$ can also be used for linear reactive circuits: the voltage and current amplitudes are constant, therefore also the impedance. For linear resistive networks, next to constant voltage and current amplitudes, also the voltage-current phase difference is zero, resulting in a real impedance.

The result is shown in Fig. 2.7 in the Smith chart. This Smith-chart is scaled to $|\Gamma| = 0.5$ to provide more detail. The impedance grid inside the chart is normalized using $Z_0 = 50\,\Omega$. The same simulation result is shown in Fig. 2.8 for a different number of harmonics k. In each chart, the $\langle\Gamma\rangle_1$ marker corresponds to the $k = 1$ case. This series provides an idea how the number of harmonics, taken into account, affects the resulting graph. This number is e.g. limited when measuring the impedance using a non-linear vector network analyzer.

rms of the average reflection coefficient magnitude

For power flow calculations, we define the power mean[11] or *rms of the average reflection coefficient magnitude*, which is calculated from the $\hat{\gamma}[n]$ time trajectory as:

$$\overline{|\gamma|} = \left|\hat{\gamma}[n]\right|_{\text{rms}} = \sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\left|\hat{\gamma}[n]\right|^2}. \tag{2.18}$$

For the example circuit values (using $k = 35$ harmonics) this results in $\overline{|\gamma|} = 0.3216$ and this corresponds to a mismatch loss of $1 - \overline{|\gamma|}^2 = -0.474$ dB, which matches the reduction of summed power flowing into this example circuit, as calculated in the frequency domain and shown in Table 2.3. This shows that, for this example, only using the first three harmonics provides enough accuracy in the calculated active input power level.

From eqns (2.15), (2.16) and (2.17), we find[12]

$$\overline{\hat{\gamma}[n]} \approx \langle\Gamma\rangle_1. \tag{2.19}$$

In this section we obtained insight into the complex valued impedance time trajectory method, which provides valuable insight in the behaviour of a non-linear rectifier. We also see how the time- and frequency domain results relate and that making use of the frequency domain results is easing the design work, as it provides harmonic dependent information and requires less calculations. This is the case when using steady state input signals.

[11] For power calculations, the square of the reflection coefficient has to be used, therefore the use of the arithmetic or geometric mean functions is not adequate.

[12] Note that $\overline{\hat{\gamma}[n]} \neq \overline{|\gamma|}$ as the former represents the *complex* average of the *complex valued* reflection coefficient trajectory and the latter represents the *real* average of the *real valued magnitudes* of the reflection coefficient trajectory.

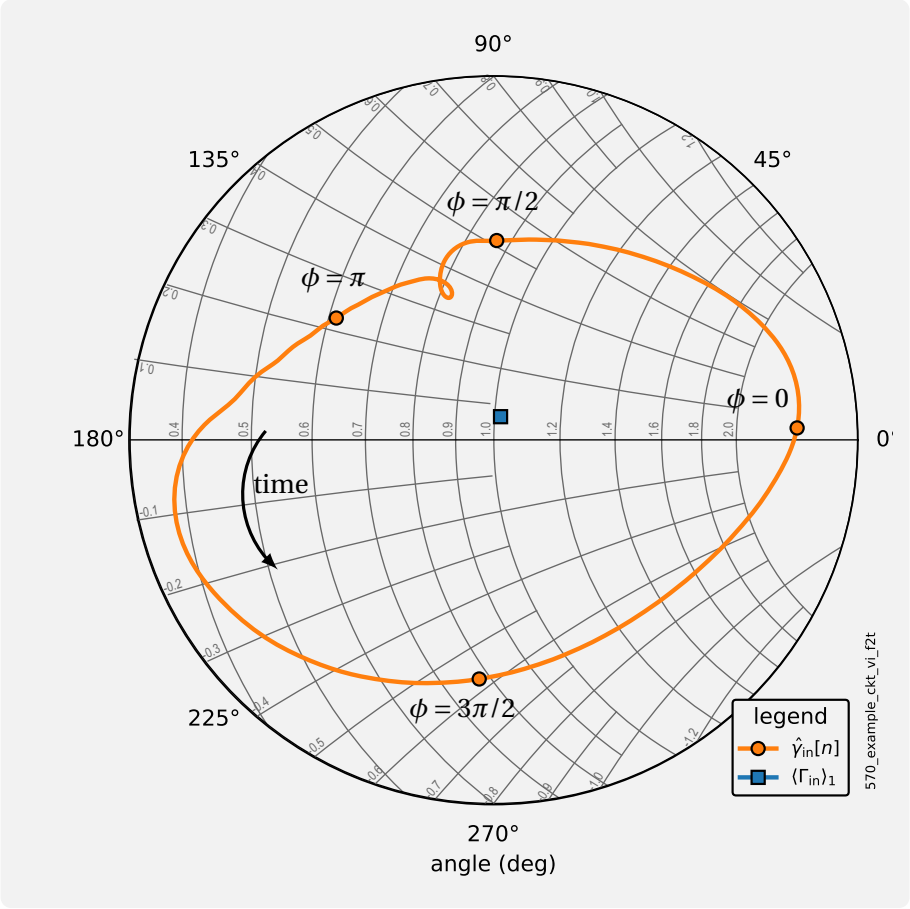
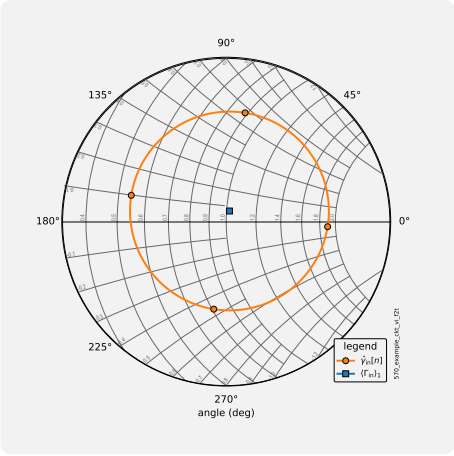
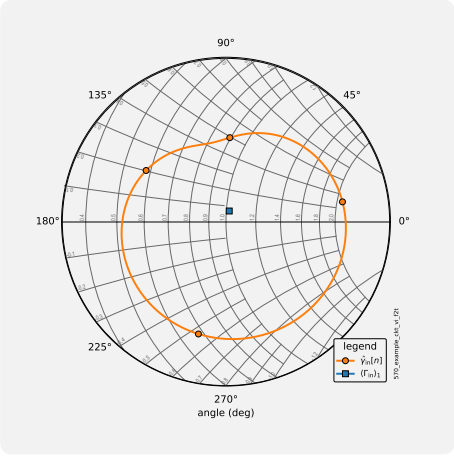


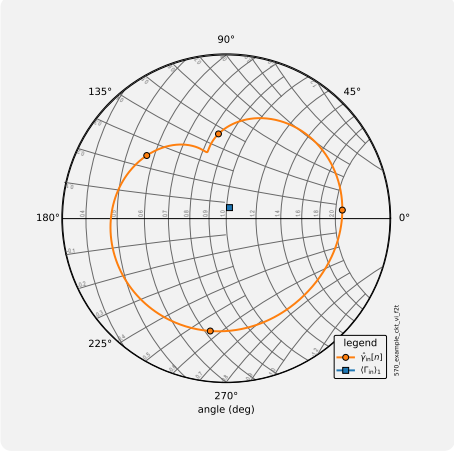
Figure 2.7 Example peak detector rectifier simulation, showing the circuit input time trajectory reflection coefficient $\hat{\gamma}_{\text{in}}[n]$ and the reflection coefficient of the mean input impedance $\langle\Gamma_{\text{in}}\rangle_1$, calculated from the HB simulation frequency domain result using $k = 35$ harmonics, at $P_{\text{forw}} = +10$ dBm and $f_0 = 915$ MHz, using an Avago HSMS-2850 SPICE diode model and $Z_0 = 50\ \Omega$. $|\langle\Gamma_{\text{in}}\rangle_1| = -29.4$ dB and the corresponding mismatch-loss equals $10\log\left(1-|\Gamma|^2\right) = -0.005$ dB. The Smith-chart is scaled to $|\Gamma| = 0.5$ to provide more detail. The impedance grid inside the chart is normalized using $Z_0 = 50\ \Omega$. The trajectory period phase ϕ is marked and indicates a non-uniform movement along the trajectory.



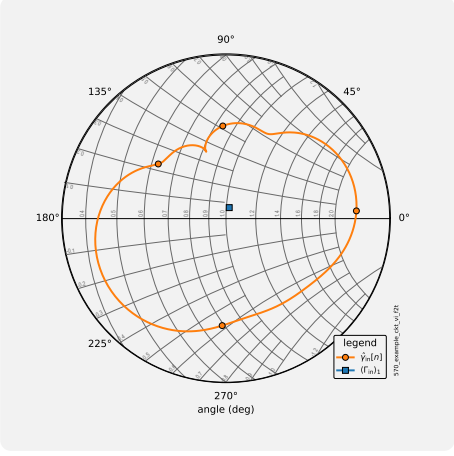
(a) $k = 2$



(b) $k = 3$



(c) $k = 4$



(d) $k = 7$

Figure 2.8 Same simulation as in Fig. 2.7, using a different number of harmonics k.

2.2 Ideal Rectifier

Transporting electrical energy in a wireless fashion is done with alternating current (ac) signals, where the consuming circuits typically make use of dc voltages and currents. The rectifying circuit in the WET receiver is therefore a key component. Typically a diode is used in these rectifier circuits. To ease the analysis of the diode rectifier properties, an ideal single diode rectifier is presented, which will be used in later chapters as basic circuit. The ideality will simplify the calculations without preventing a thorough analysis.

2.2.1 Ideal single diode rectifier

To ease the study of the essential behaviour of a diode rectifier, it is practical to start with an ideal rectifier circuit topology. This circuit will be used in chapter 4 to derive the fundamental functioning of the diode rectifier.

Ideal rectifier

With the single diode rectifier circuit, shown in Fig. 2.9, an ideal situation can be created by taking the following measures:

a. a sinusoidal waveform signal source is used unless otherwise noted,
b. an ideal harmonic filter F_1 is applied between the diode anode and ground, having an insertion resistance R with $\langle R\rangle_{0,2\cdots\infty} = 0$ and $\langle R\rangle_1 = \infty$,
c. an ideal diode is used, having no junction capacitance ($C_{j0} = 0$ F), no series resistance ($R_s = 0\ \Omega$), and ideal diode ideality factor[13] ($n = 1.0$),
d. an ideal high-pass filter, represented by capacitor C_1, is used between the diode's cathode and ground, shorting the fundamental current $\langle i\rangle_1$ and all higher harmonics $\langle i\rangle_{2\cdots\infty}$.

The result of this idealized circuit is:

1. $\langle V_{\text{in}}\rangle_{h\neq 1} = 0$,
2. $\langle V_{\text{out}}\rangle_{h>0} = 0$ and $\langle V_{\text{out}}\rangle_0 = \langle I_{\text{out}}\rangle_0 R_L$,
3. $\langle I_{\text{out}}\rangle_{h>0} = 0$,
4. $P_{\text{in}}^{h\neq 1} = 0$ and $P_{\text{in}}^{h=1} = \frac{1}{2}\,\text{Re}\left(\langle V_{\text{in}}\rangle_1 \langle I_{\text{in}}\rangle_1^*\right)$,
5. $P_{\text{out}}^{h>0} = 0$ and $P_{\text{out}}^{h=0} = \langle I_{\text{out}}\rangle_0^2 R_L$.

In this two-port circuit, P_{in} is equal to $P_{\text{act,in}}$ at the input port, and P_{out} is equal to $P_{\text{act,L}}$ at the output port.

[13] The ideal diode equation will be discussed in chapter 3, which contains the diode ideality factor.

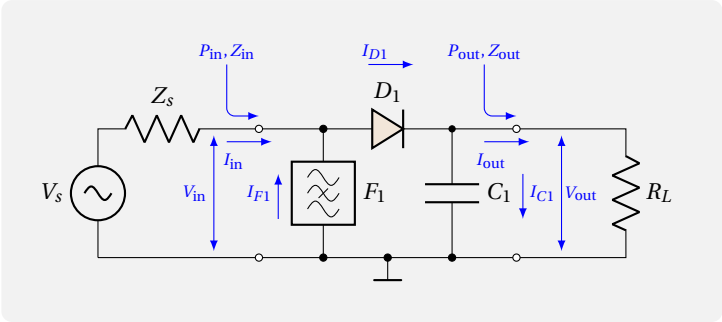


Figure 2.9 Single diode rectifier configuration with a bandstop filter F_1, tuned at the circuits operating frequency f_0. The diode voltage is defined as $V_{D1} = V_{in} - V_{out}$. The impedance of F_1 should be low at $f \neq f_0$ and high at $f = f_0$. The reactance of C_1 should be low at $f \geq f_0$ and can be seen as a high-pass filter.

The flow of the different current h-phasors in the rectifier circuit is shown in Fig. 2.10 by colored arrows. The result of using filter F_1 is that the waveform of V_{in} remains equal to V_s, as the $\langle I_{D1} \rangle_{h>1}$ current terms are not flowing through the source impedance Z_s. As $\langle V_{in} \rangle_{h\neq 1} = 0$ and $\langle V_{out} \rangle_0 = \langle I_{out} \rangle_0 R_L$ the diode voltage is $V_{D1} = \langle V_{in} \rangle_1 - \langle I_{out} \rangle_0 R_L$. An ADS implementation of this rectifier circuit is discussed at the end of the next section.

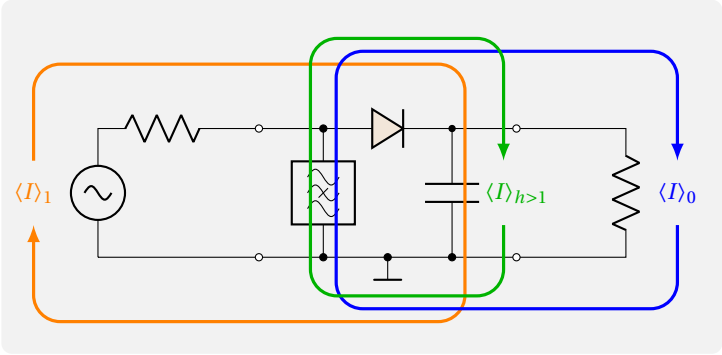


Figure 2.10 The flow of the different current h-phasors in the single diode rectifier configuration with a bandstop filter. The harmonic current terms $\langle I \rangle_{h>1}$ will not dissipate energy in the circuit due to the ideality of the circuit.

2.2.2 Simplified model

Following the implications described above, the diode and circuit can be described with a simplified model as shown in Fig. 2.11. This will be used for basic concept insights later in this work. A more detailed model will be covered in the next chapter. The simplified diode model consists of a non-linear junction resistance R_j and voltage controlled current source $\langle I_j \rangle_0(V_j)$.

Junction resistance

The *junction resistance* is defined as the fundamental diode voltage over current:

$$R_j = \frac{\langle V_j \rangle_1}{\langle I_j \rangle_1(V_j)}, \tag{2.20}$$

in which the current is non-linearly related to the junction voltage V_j consisting of both $\langle V_j \rangle_1$ and $\langle V_j \rangle_0$ with $\langle V_j \rangle_0 = \langle I_j \rangle_0 R_L$.

In the next chapter we will see how the diode current is defined in detail. The non-dc currents are all shorted to ground by the capacitor and band stop filter; only the dc current will flow through the load resistor. This is reflected in the controlled current source used in this model. The bandstop filter F_1 and load capacitor C_1 don't play a role in this simplified model and are omitted.

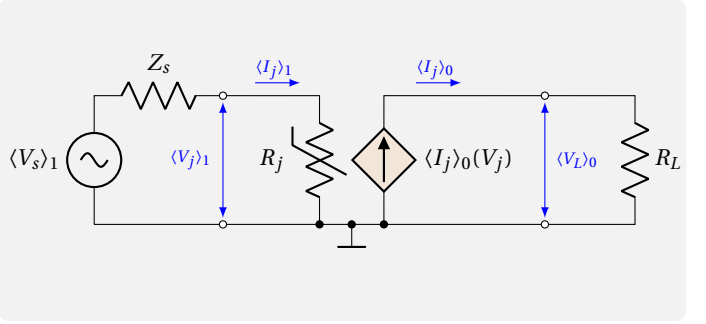


Figure 2.11 Simplified single diode rectifier circuit model, consisting of a non-linear junction resistance R_j and a voltage controlled current source $\langle I_j \rangle_0(V_j)$.

2.3 Energy Transfer Efficiency

In the field of radiated wireless energy transfer, the most important characteristic is the obtained energy transfer efficiency η. For low power wireless sensor node

applications, a higher efficiency leads to a larger possible distance between transmitter and receiver or e.g. higher update rates of sensor nodes. For high power applications, efficiency also plays an important role in power dissipation: better efficiency results in lower device temperatures, larger operating range conditions, longer battery lifetime, etc.

Energy transfer efficiency

When taking a closer look at the *energy transfer efficiency*[14] (from receiver RF input to receiver dc output[15]), we should focus on the result of energy in time: power. All that counts is the ratio of obtained dc power in a load P_L^0 to the required fundamental frequency power P_{in}^1 to accomplish this:

$$\eta = \frac{P_L^0}{P_{\text{in}}^1}. \tag{2.21}$$

2.3.1 Efficiency optimization

From the radiative WET system block-diagram in Fig. 1.1, we can derive the minimal block-diagram, needed to optimize the rectifier circuit for a WET receiver. The receiver antenna can be seen as a source, generating the incoming signal, which comes from a distant origin. Fig. 2.12 shows the block-diagram of the minimal receiver. The following matching circuit is used to minimize the impedance mismatch loss between source output- and rectifier input impedance. This circuit has typically a frequency dependent transfer function. The rectifier transfers the incoming RF energy to a dc output energy consumed by a load, represented by a resistance in this diagram.

Optimizing a rectifier circuit for best efficiency is done by maximizing Equation (2.21), which looks fairly straightforward[16]. Unfortunately when using rectifier devices that are inherently non-linear, like a semiconductor diode, this is not straightforward. The reason for this is easily overlooked. There is a dependency on signal amplitude in the rectifier. Later we will see that the rectifier input

[14] In this work, rectifier energy transfer efficiency (ETE) is equal to PCE.

[15] Due to the extremely low value, the transmitter-input to receiver-antenna efficiency has no practical value. Optimizing the receiver efficiency is of more interest as this consists typically of a circuit running on a battery or the-like.

[16] From the maximum power transfer theorem a difference can be seen between power efficiency and power transfer. For radiated WET applications, the receiver is placed in the far field of the source. This means the source dissipation is left out of the equation when designing an optimal efficient receiver rectifier. This makes that in this work maximizing the power- and efficiency transfer provides the same result.

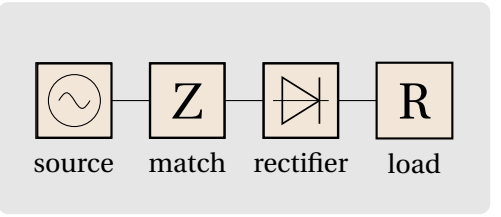


Figure 2.12 Block diagram of a minimal WET rectifier. The source represents the incoming signal at the antenna (source), connected to the impedance matching network (match). The rectifying circuit (rectifier) is connected to a load.

impedance has a dependency on the load resistance. The load resistance value for optimal efficiency has a dependency on the rectifier input signal amplitude, due to the non-linear rectifier behaviour.

2.3.2 Adaptive source

In this work we use the approach to leave out the impedance matching network as a first design step. This to ease the design of the rectifier circuit and the comparison of different types of rectifiers. The resulting impedance mismatch between source and rectifier can be countered by ensuring a specific power level flowing into the circuit, using an adaptive source we refer to as *complex conjugately matched source* and indicated as '**P_CCM**' in ADS or $\mathbf{P_{CCM}}$ in circuit diagrams. First an example is discussed to outline the need for this approach.

For a signal source, whether a physical lab-generator or e.g. a standard 'P_1Tone' ADS source, the output power can be specified. This is done with the assumption of having a load, connected to the source, with an impedance equal to the complex conjugate of the source impedance [60]. The source can be represented by a voltage source V_s in series with the source impedance Z_s.

From circuit theory [51, 52] the maximum available power from the source at the fundamental frequency f_0, P_s^1, can be found as

$$P_s^1 = \frac{|\langle V_s \rangle_1|^2}{8\,\mathrm{Re}(Z_s)}, \tag{2.22}$$

with $\langle V_s \rangle_1$ being the source voltage[17].

The equation for the source voltage amplitude is given by

$$|\langle V_s \rangle_1| = 2\sqrt{2P_s^1\,\mathrm{Re}(Z_s)}. \tag{2.23}$$

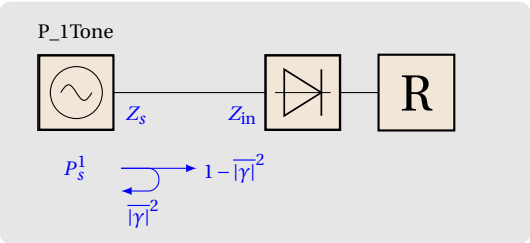
[17] In [52, 53], rms values are used for voltages and currents. In this work, peak values are used unless otherwise stated.

This will result in power dissipation P_s^1 in the load impedance Z_L. For different load impedances, the dissipation will also differ. Fig. 2.13 (a) shows an example of using a standard 'P_1Tone' source, set to an output power of P_s^1 with a rectifier and load resistor used as loading circuit for the source. In this case, the rectifier input impedance Z_{in} determines the input reflection coefficient using eq. (2.16):

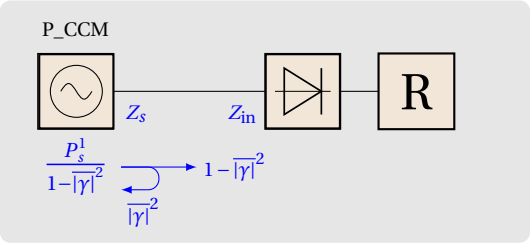
$$\hat{\gamma}_{\text{in}}[n] = \frac{\hat{z}_{\text{in}}[n] - Z_s}{\hat{z}_{\text{in}}[n] + Z_s}. \tag{2.24}$$

The level of power entering the circuit $P_{\text{in}}{}^1$ is calculated as

$$P_{\text{in}}^1 = P_s^1(1 - \overline{|\gamma|}^2). \tag{2.25}$$



(a) Rectifier with load and normal P_1Tone source. The rectifier input power $P_{\text{in}}^1 = P_s^1(1 - \overline{|\gamma|}^2)$.



(b) Rectifier with load and adaptive P_CCM source. The rectifier input power $P_{\text{in}}^1 = P_s^1$.

Figure 2.13 Minimal rectifier analysis setup, without impedance match between source and rectifier: a) using a normal P_1Tone source with fixed source voltage and b) using an adaptive P_CCM source with reflection coefficient dependend source voltage.

The usage of a typical circuit simulator optimizer will not result in the optimal rectifier efficiency, when using a standard signal source like the 'P_1Tone' source in ADS. The source output power parameter P_s only ensures the specified level when the load connected to the source has a complex conjugately matched

impedance to the source output impedance. For other load impedances, the power flowing into the load will be higher or lower than the specified value. A similar approach can be used in measurements [61].

As an example, an ideal single diode rectifier[18] is simulated. The circuit diagram is shown in Fig. 2.14 and does not have an input impedance matching network. This-way the optimization of the matching network is left out of the equation and kept for a later stage in the design steps. To show the difference in results, both the P_1Tone and the P_CCM source will be used in the example.

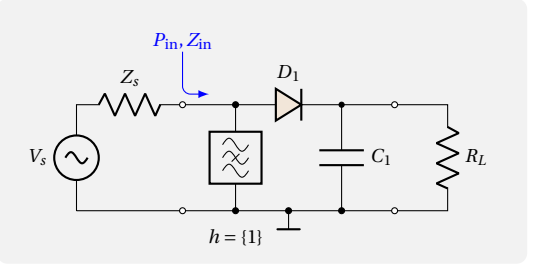
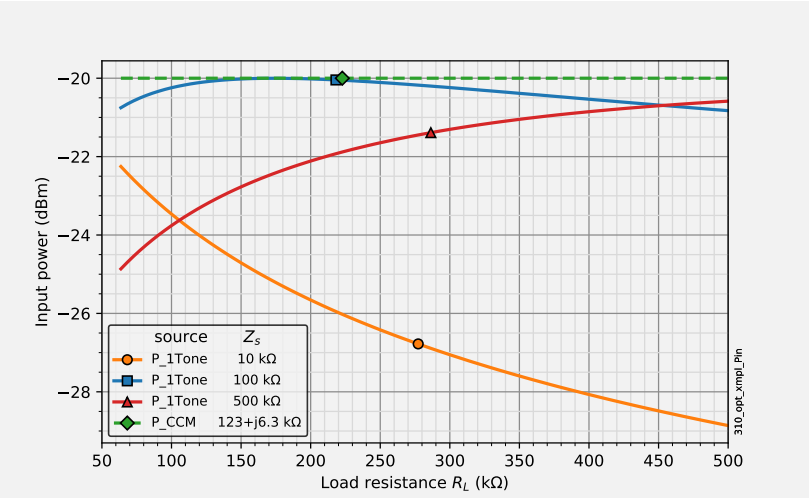


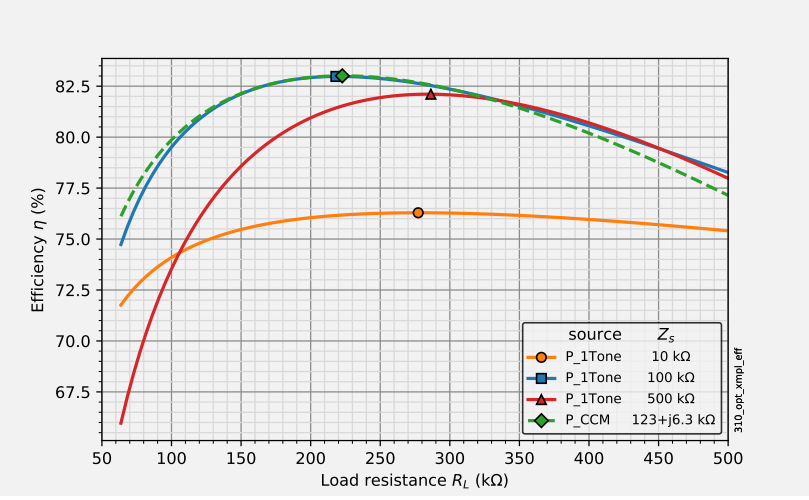
Figure 2.14 Peak detector rectifier circuit. The source power level $\langle P_s \rangle_1 = -20$ dBm. The band stop filter blocks the fundamental frequency $f_0 = 1$ MHz only, $h = \{1\}$ references the fundamental frequency component being blocked.

The rectifier circuit has an input impedance Z_{in}. Two different sources are used: a standard P_1Tone and an adaptive P_CCM type. When the source impedance Z_s is not equal to the complex conjugate of the circuit input impedance, mismatch loss will occur. The power flowing into the circuit equals the source power multiplied with a factor $1 - |\overline{\gamma}|^2$. To ensure a specific rectifier input power level, the source impedance can be made equal to the complex conjugate of the circuit input impedance to obtain zero mismatch loss, or we adapt the source amplitude $|\langle V_s \rangle_1|$, which is done in the P_CCM source. If we vary the load resistance R_L using a simulation optimizer routine, a change in circuit input impedance is observed for the P_1Tone source cases. The result is a varying level of power entering the circuit due to the varying impedance mismatch loss. This is illustrated in Fig. 2.15 (a) with the example circuit simulation of Fig. 2.14. The mismatch loss plays a role in the power transfer efficiency. Fig. 2.15 (b) shows the efficiency versus load resistance variation. The corresponding load voltage increases with load resistance for the four cases, the levels are different between the cases as shown in Fig. 2.15 (c). This also shows that optimizing a rectifier for highest output voltage does not result in the most energy efficient rectifier. This example is used to underpin the need for an adaptive source, to obtain optimal

[18] A peak detector rectifier topology is used with a Skyworks SMS7621 diode.

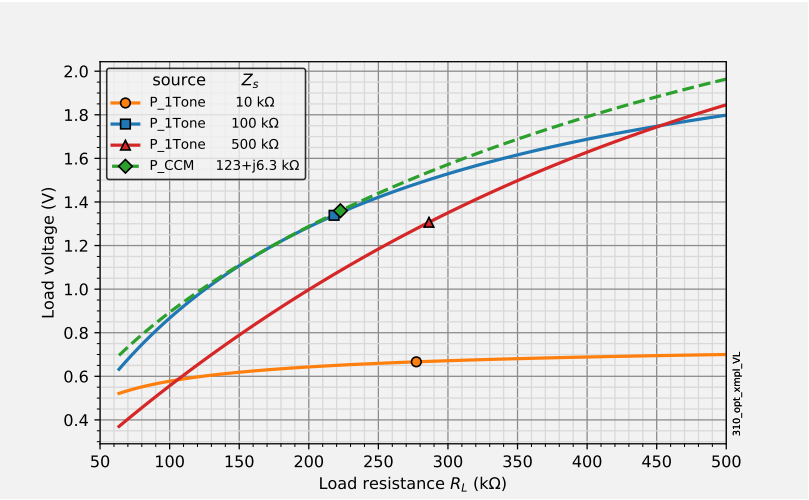


(a) Circuit input power versus load resistance.



(b) Power transfer efficiency versus load resistance. The markers are placed at the peak efficiency values.

Figure 2.15 Single diode rectifier ADS simulation (see Fig. 2.14), showing (a) circuit input power, (b) power transfer efficiency and (c) circuit load voltage, all versus load resistance and for four different source impedance Z_s values (the P_CCM curve is dashed).



(c) Circuit load voltage versus load resistance.

Figure 2.15 Single diode rectifier ADS simulation (see Fig. 2.14), showing (a) circuit input power, (b) power transfer efficiency and (c) circuit load voltage, all versus load resistance and for four different source impedance Z_s values.

rectifier efficiency. The explanation of the behaviour seen will be provided in the following chapters.

Tabel 2.4 shows the circuit input power level and -impedance and the load voltage and -resistance for the different source impedance values used, at the maximum efficiency η points. From these results we observe that the rectifier power transfer efficiency depends on load resistance and source impedance. If the circuit is operated at higher frequencies, the input impedance will show a larger reactive component. It is observed that an optimization routine will have difficulty finding the optimal load resistance and source impedance at the same time. A manual adaptive approximation approach did improve the result. A source which always ensures the same level of power flowing into the circuit, provides the best result in optimizing the rectifier energy transfer efficiency[19], see Fig. 2.13 (b). This is the P_CCM adaptive source and can be realized in ADS as we will see later.

[19]Typically the efficiency is analysed over a range of rectifier input power levels. The design goal is to find the optimal efficiency for each input power level. The adaptive source is swept over the range of power levels and at each level, the source output power is kept constant.

Table 2.4 Single diode rectifier ADS simulation, showing maximal efficiency η and corresponding circuit input power and -impedance and load voltage and -resistance versus source impedance Z_s.

Source (type)	Z_s (kΩ)	η (%)	P_{in}^1 (dBm)	$\langle Z_{\text{in}} \rangle_1$ (kΩ)	$\langle V_L \rangle_0$ (V)	R_L (kΩ)
P_1Tone	10	76.3	−26.8	$168.8 - j13.8$	0.67	277.3
P_1Tone	100	83.0	−20.1	$121.4 - j6.15$	1.36	218.2
P_1Tone	500	82.1	−21.4	$156.6 - j10.3$	1.34	286.4
P_CCM	123+j6.3	83.0	−20.0	$123.4 - j6.33$	1.36	222.7

2.3.3 Diode rectifier optimization

The following sequence of design steps is presented for obtaining an optimal (i.e. maximized efficiency) rectifier design. See Fig. 2.16 for a visual representation.

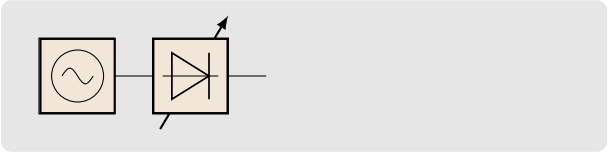
a. First choose a diode and rectifier topology for the required range of input power levels. This will be covered in Chapter 4 and 5.

b. Add a load resistance R_L and optimize R_L for the range of input power levels, using an adaptive source which ensures a constant power flow into the circuit. Note: the effective load resistance might change in step (d) due to the insertion of a buck/boost converter.

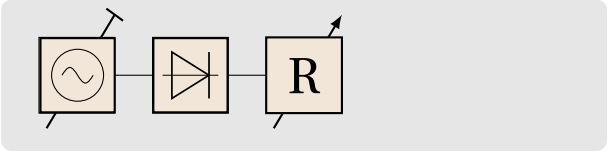
c. design an input impedance matching network, which results in an optimal PCE across the input power range. Mismatch loss should be minimized.

d. design an optimal power management circuit as stage between the rectifier and the loading application circuit. This circuit will typically convert the variable rectifier output voltage to a constant output voltage with a circuit input impedance close to the rectifier ideal load resistance for optimal PCE.

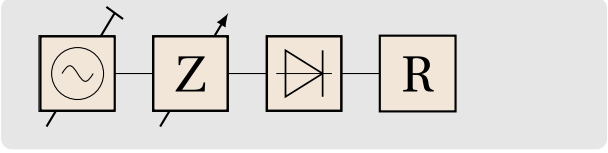
To accommodate (b), the method of using a complex conjugately matched source is introduced. This is an adaptive source which ensures that a specific power level is flowing into the connected circuit, for any arbitrary load circuit impedance. For a normal source, the specified source output power level flows only into a connected load when the source impedance is the complex conjugate of the load impedance, therefore the choice of name for this adaptive source. If the load resistance has a different value, this results in a mismatch loss of $1 - \overline{|\gamma|}^2$, reducing the power flowing into the circuit. We will see later that the input impedance of a rectifier is also dependent on the input signal level. This



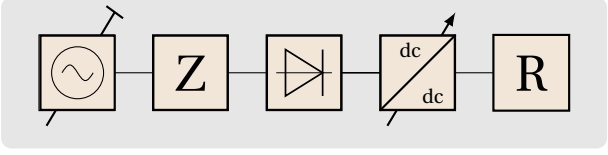
(a) Select a rectifier diode and -topology suitable for a range of input power levels P_{in}.



(b) Optimize R_L for the range of input power levels P_{in}.



(c) Design an input impedance matching circuit for the range of input power levels P_{in}.



(d) Design an optimal power management circuit for the range of input power levels P_{in}.

Figure 2.16 Diode rectifier optimization: sequence of design steps.

means that we have an undefined situation for the level of power flowing into the circuit and therefore also for the power flowing out of the circuit output. Obtaining convergence for a circuit simulator optimization routine will be difficult, especially for larger signal amplitudes. A signal source capable of adapting its output signal level to the amount of power flowing out of the source, into the connected circuit, is required for this non-linear optimization job. The ADS implementation will be shown below. When applied to the above example of Fig. 2.14, the optimal rectifier power transfer efficiency is found to be $\eta = 83.0$ % at an input power of -20.0 dBm and input impedance $\langle Z_{\text{in}} \rangle_1 = 123.4 - j6.33$ kΩ. The load voltage is $V_L = 1.36$ V at a load resistance of $R_L = 222.7$ kΩ. This is close to the source resistance case of $R_s = 100$ kΩ.

Complex conjugately matched source

A design challenge is finding the optimal impedance match between the rectifier input impedance and the source impedance. As the rectifier input impedance varies with input power (next to frequency and load resistance), a matching circuit will typically not provide an optimal match over a large input power range. In order to get a view on the performance (power transfer efficiency) of a rectifier circuit, it is effective to use a complex conjugately matched source. This source is constructed such that a specific power level is always entering the circuit, regardless of its input impedance. This is realized by adjusting the source output level to obtain the desired power flow into the load circuit. This is equivalent to a constant adaptation of the source resistance to be complex conjugately matched to its load — therefore the choice of its name.

2.3.4 ADS implementation

To enable a circuit simulator like ADS to mimic a complex conjugately matched source, an adaptive approach is used to ensure a specific power level P_s^1 to enter into the connected load circuit with an arbitrary impedance $Z_x \neq Z_s^*$. Fig. 2.17 shows the block diagram used to implement this source in ADS.

This ADS source makes use of two, equation based, components: a 3-port non-linear frequency-domain defined device (FDD) and a 3-port linear equation based S-parameter component (S3P_Eqn). The latter one is used as a 3-port circulator at the output of the source with its S-parameters defined as

$$S = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}, \tag{2.26}$$

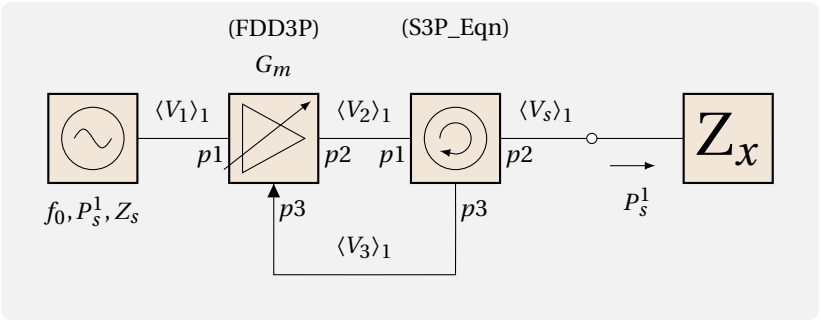


Figure 2.17 Complex conjugately matched source block-diagram, connected to a load with an arbitrary impedance Z_x. $p1$, $p2$, $p3$ indicate the port numbers used in the ADS implementation. FDD3P is an ADS frequency-domain defined device (FDD) component, S3P_Eqn is an ADS S-parameter component.

to ensure an ideal separation between the outgoing and returned energy. This is done for all frequencies, therefore a time-domain defined linear equation based S-parameter component is suitable. The FDD component is used to calculate the reflection coefficient at the source output port by taking the complex ratio of the voltage of the reflected wave $\langle V_3\rangle_1$ to that of the incident wave $\langle V_2\rangle_1$:

$$\langle\Gamma\rangle_1 = \frac{\langle V_3\rangle_1}{\langle V_2\rangle_1}, \tag{2.27}$$

which is used to calculate the required gain mismatch factor

$$G_m = \frac{1}{1-|\langle\Gamma\rangle_1|^2}. \tag{2.28}$$

As the reflection coefficient $\langle\Gamma\rangle_1$ is calculated at the fundamental frequency only, a frequency-domain FDD device is used[20]. The source amplitude $\langle V_1\rangle_1$ is multiplied by $\sqrt{G_m}$ to obtain the specified amount of power flowing into the connected load Z_x. For the FDD, the ports are defined as Z_s impedance ports by relating the port current to the -voltage and impedance. Port 2 is used to implement the feedback mechanism on the required output power ($\langle I_2\rangle_1$ in Equation (2.29) below). The ADS implementation is shown in Fig. 2.18. The adjustable gain block, implemented in the FDD component, makes use of the following equations:

[20]Note that $\langle V_2\rangle_h = 0$ for $h > 1$.

$$\begin{aligned}\langle I_1\rangle_1 &= \frac{\langle V_1\rangle_1}{Z_s},\\ \langle I_2\rangle_1 &= -\frac{\langle V_1\rangle_1\sqrt{G_m}}{Z_s},\\ \langle I_3\rangle_1 &= \frac{\langle V_3\rangle_1}{Z_s}.\end{aligned} \tag{2.29}$$

$\langle I_1\rangle_1$ defines the impedance of the FDD port p_1 being Z_s, like $\langle I_3\rangle_1$ does for port p_3. The adjustable gain is implemented in the port p_2 equation, specifying $\langle I_2\rangle_1$ based on the p_1 voltage and G_m value. For the ADS FDD component, the port voltages are accessible using `_sv(p,h)`, with `p` being the port number and `h` being the frequency harmonic number.

Example

To show the functioning of the adaptive source, an ADS example is used based on the example rectifier circuit of Fig. 2.14 as shown in Fig. 2.19. The adaptive source is shown on the left in this circuit, as a sub circuit symbol of Fig. 2.18 (a).

During the ADS simulation, for each optimizer step, the source is ensuring adaptively a constant power level, flowing into the connected circuit[21]. This is important as with the change in load resistance, also the junction resistance changes and with that the power flowing into the circuit changes when using a standard source, as shown in the example of Figs 2.14 and 2.15. The requested power is P_s (which is swept in dBm) and the actual power entering the circuit is defined as

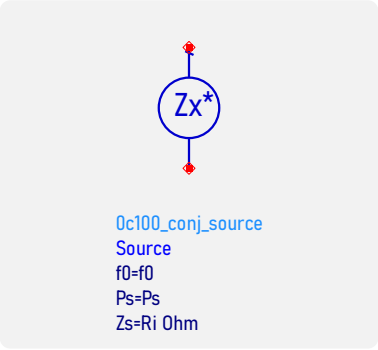
$$P_{\text{act}} = \frac{1}{2}\,\text{Re}(\langle V_{\text{in}}\rangle_1\langle I_{\text{in}}\rangle_1^*). \tag{2.30}$$

The percent source output power error can be expressed using the normalized requested- P_s and actual power level P_{act} difference:

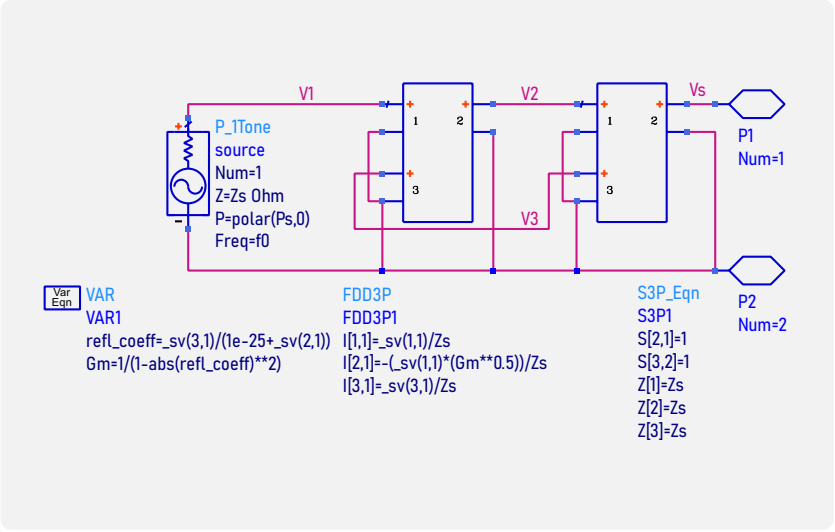
$$\delta_{Ps} = \frac{|P_s - P_{\text{act}}|}{P_s} \times 100\,\%. \tag{2.31}$$

The ADS example shows $\delta_{Ps} < 0.0001\,\%$ for $P_s = -60$ to $+30$ dBm, as shown in Fig. 2.20. The optimal load resistance value R_L is stable within four optimization iterations. For each iteration, the optimizer calculates the value of the error

[21] This is equivalent of a source with a fixed output power and a source impedance which adaptively matches with the complex conjugate of the load impedance. In a circuit simulator, a source delivering power consists of a voltage source in series with a source impedance. The source voltage is calculated based on the required output power and chosen source impedance, with the assumption that the load impedance is the complex conjugate of the source impedance. Therefore, using the source output level adaptation is a logical choice in this work.



(a) The ADS symbol.



(b) The circuit implementation.

Figure 2.18 ADS implementation of the complex conjugated source: (a) shows the ADS component symbol, (b) provides the corresponding circuit diagram. The component has three parameters: The source frequency f_0 (Hz), the source output power P_s (W) and the source impedance Z_s (Ω). The output power is flowing into the load circuit with the specified amount, regardless of the load impedance.

function, which consists in this example of the obtained efficiency, and estimates a better value for the parameter(s) to optimize — in this case — the load resistor. In the mean time, the adaptive source has its own mechanism of adjusting its output power using the built-in equations. A low number of optimization iterations means the chosen optimization method converges easily. For non-linear circuits this is an important property to keep simulation time under control. The P_CCM source results shown in Fig. 2.15 are simulated using the ADS example in Fig. 2.19.

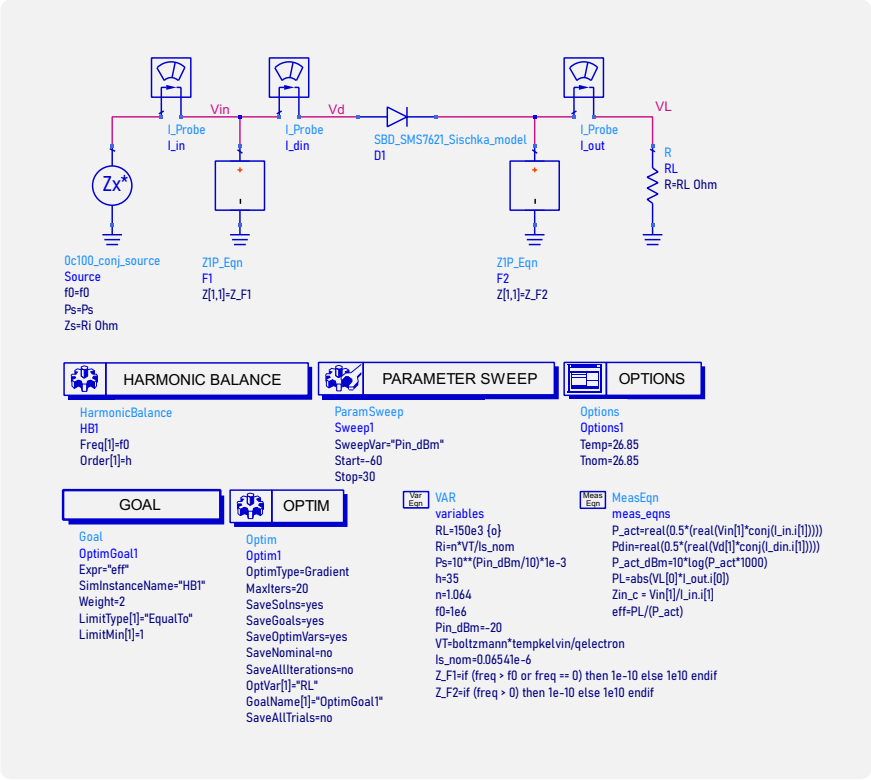


Figure 2.19 ADS example of the complex conjugated source usage in the example rectifier circuit of Fig. 2.14. The sub-circuit of the source is shown in Fig. 2.18. The equation based component F1 represents the input band-stop filter. F2 is used to model an ideal capacitor, acting as short for $f > 0$ Hz. The load resistor RL has a resistance which can be optimized.

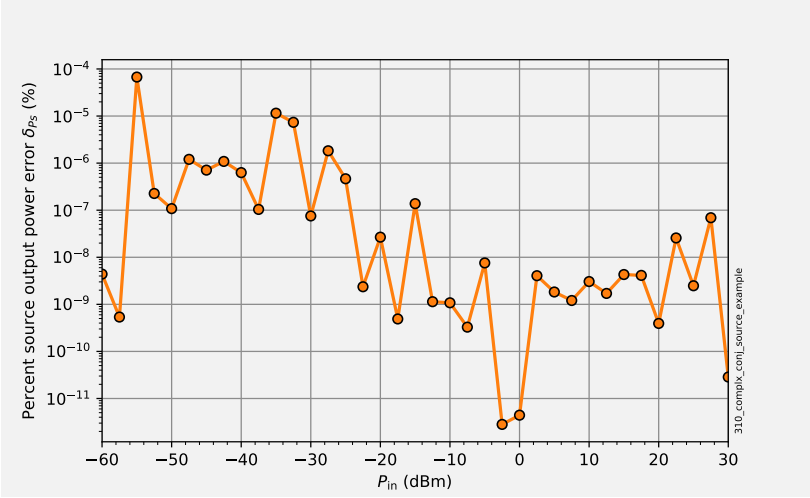


Figure 2.20 Simulated percent source output power error, resulting from the complex conjugately matched source ADS example shown in Fig. 2.19.

2.4 Summary

In this chapter three items have been presented:

a) The benefit of using frequency domain simulation to obtain harmonic insight in the flow of energy through a non-linear circuit, together with the notation used to address the different time- and frequency domain quantities used in this work. The topic of impedance time trajectory is discussed and related with the frequency domain view. This shows that the time domain view gives useful insight, where the frequency domain is easier for the design and analysis of rectifier circuits.

b) An ideal rectifier circuit is discussed, which eases the basic understanding of the rectifier topic and is used in following chapters.

c) Optimal energy transfer is key in making WET beneficial. The optimization of a non-linear rectifier circuit for optimal efficiency is not straightforward. A special adaptive simulation source to serve this purpose is presented. This also provides a method to objectively compare diode types and rectifier topologies by leaving out the impedance matching circuit. This approach is used in subsequent chapters. The process of designing the optimal rectifier circuit is presented.

Chapter 3

Diode Model

In designing WET electronic circuits a rectifying component model is needed to enable finding the optimal design through circuit simulation. In WET circuits often a diode is used as the rectifying device. In this work we only focus on the diode as a rectifying element and more specifically only on the discrete diode — not the integrated diode or equivalent circuits like diode-switched transistors. In this chapter we discuss the diode model by looking into the equations that describe its ideal behaviour and the different methods used to model realistic diodes.

3.1 Circuit Simulation

The electronic circuit simulations in this work are based on Keysight Technologies' ADS software [50]. ADS contains different simulation engines. Two main types can be identified: the first of them being a SPICE based time domain engine named *Transient*. The other is a frequency domain engine named *Harmonic Balance* (HB). Most WET applications make use of Continuous Waveform (CW) signal sources, producing a signal with constant amplitude and frequency. In this work we are focusing on the energy transfer performance of WET circuits. With a CW source, we can apply a steady state analysis as we are not interested in the circuit start-up behaviour. For steady state circuit simulations, the HB frequency domain simulation engine is the most efficient one. When we look into the details of energy transfer using non-constant signal sources, we will resort to time domain analysis.

Three problems can make a time-domain technique impractical:

1. Dispersive elements are difficult to analyse in the time domain (e.g. transmission lines, S-parameter described sub-networks). They are typically

defined in the frequency domain and the translation to a time domain model require an extra step in calculating the impulse response.

2. Circuit's time constants may be large compared to the fundamental excitation frequency period. This requires many excitation cycles for the numerical integration encountered in the circuit equations.

3. Each linear or non-linear reactive element adds a differential equation to the set of equations describing the circuit. This makes time-domain simulation slow. HB makes use of a numerical method without differential equations.

For WET circuits, the first problem is applicable, especially when elements of the circuit are based on frequency domain measured data or if e.g. printed circuit board (PCB) transmission lines play a role in the circuit behaviour. The second problem is also applicable as the circuit load capacitance typically results in a large time constant compared to the frequency of operation period. The number of reactive elements is typically not high in a WET rectifier, as each additional element adds losses. This is the case for discrete circuits and even more for integrated versions. Therefore the third problem is not applicable, unless a high number of parasitic elements is included in the model.

An advantage of time-domain analysis is its ability to handle strong non-linear component behaviour. This robustness requires the non-linearities to be continuous, so that the time steps can be made short enough to obtain small enough circuit voltage and current differences [62, 63].

In HB analysis, circuits with both linear and non-linear circuit elements are divided into two sub-circuits. One with the linear and the other with the non-linear components. The linear sub-circuit is treated as a multi-port, described by its admittance-, scattering- or other parameters and analysed in the frequency domain. The non-linear elements are described by their I-V or Q-V characteristics and analysed in the time domain. By making use of the inverse discrete Fourier transform (IDFT) and discrete Fourier transform (DFT) functions the results are converted between the two domains. We will see later in this chapter how to model the non-linear diode elements in the time domain. An example of the HB method is shown in Fig. 3.1 and the HB process is described in Algorithm 1.

The basic HB analysis process can be described as shown in Algorithm 1, where Kirchoff's current law (KCL) is used as pivotal point. This description uses pseudocode, which is a plain language description of the steps used in the algorithm. The := sign means assignment. For instance, $v[t] := \langle V \rangle_h$ means that the value of (time domain) voltage $v[t]$ changes to the value of (frequency domain) $\langle V \rangle_h$, by using the IDFT function. Same-wise in line 6 $\langle I_{NL} \rangle_h := i_{NL}[t]$

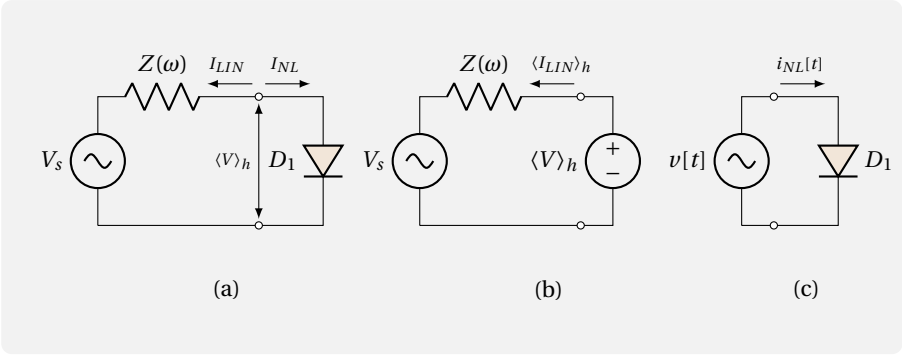


Figure 3.1 HB analysis process for a diode circuit example: (a) division into a linear- (left) and non-linear (right) sub-circuit, (b) the linear part is analysed in the frequency domain with I_{LIN} being equal to the voltage $\langle V \rangle_h$ divided by the source impedance $\langle Z \rangle_h$, (c) the non-linear part in the time-domain with I_{NL} being equal to the voltage $v[t]$ divided by the diode impedance $Z_{D_1}[t]$.

means that the value of (frequency domain) current $\langle I_{NL} \rangle_h$ changes to the value of (time domain) $i_{NL}[t]$, by using the DFT function. The loop with $\langle V \rangle_h$ adaptation is repeated until the resulting KCL current-error is below $\max_{f_h}$. The result is a possibly[1] correct $\langle V \rangle_h$ solution with the corresponding currents.

Algorithm 1: Harmonic Balance analysis process.
$h = 0, 1, \cdots, k$ with k the maximum number of harmonics concerned.

Data: $\max_{f_h}$ - max KCL error
Result: $\langle V \rangle_h$, $\langle I \rangle_h$

$\langle V \rangle_h := \langle V \rangle_h[0]$; /* initial estimate */
while $|f_h| > \max_{f_h}$ **do**
  $\langle I_{LIN} \rangle_h := \langle V \rangle_h / \langle Z \rangle_h$; /* sim linear circuit */
  $v[t] := \langle V \rangle_h$; /* IDFT */
  $i_{NL}[t] := v[t] / z_{D_1}[t]$; /* sim non-linear circuit */
  $\langle I_{NL} \rangle_h := i_{NL}[t]$; /* DFT */
  $f_h = \langle I_{LIN} \rangle_h + \langle I_{NL} \rangle_h$; /* KCL */
  modify $\langle V \rangle_h$
end while

[1] In general non-linear circuits have multiple solutions. In a practical circuit, a single solution usually dominates.

3.2 SPICE Model

From the preceding section, it follows that the HB simulation approach is the preferred method to use for WET circuits. HB requires that the non-linear device, typically a diode, should be modelled in the time-domain with continuous functions. The de-facto standard diode model used by circuit simulation tools is the Simulation Program with Integrated Circuit Emphasis (SPICE) model. This model will be analysed in more detail.

SPICE was first released under the name Computer Analysis of Nonlinear Circuits, Exlcuding Radiation (CANCER) in 1970 [64] and acquired the name SPICE1 in 1972 [65]. SPICE2 was released in 1975 [66][2] and SPICE3 in 1987 [67, 68][3]. The junction diode model available in CANCER had a basic functionality, containing only six parameters without including the breakdown effect. The SPICE2 diode model is described using 14 parameters, adding the saturation current I_s and junction capactiance C_j temperature dependence, flicker noise and the breakdown effect. The SPICE3 diode model is based on the SPICE2 model also using 14 parameters, with a slight extension, e.g. the addition of the series resistance R_s temperature dependency [69, 70]. The Keysight ADS *pn*-junction diode model is described using 68 parameters. The model is built on top of the SPICE2 model, adding extra parameters for more model details.

This work is based on the SPICE2 diode model, without making use of the noise equations. One reason for using this model is the fact that diode suppliers provide SPICE2 model parameters. Another reason is that with the use of the SPICE2 model as described in this work, enough detail can be obtained to design efficient rectifier circuits. What follows in the next section is a description of the relevant SPICE2 *pn*-junction diode model parameters for WET applications. Another part of our model is discussed in the Schottky Diode section 3.4, as the *pn*-junction diode and Schottky diode models have a considerable overlap in parameters used for both models. In the remainder of this work, we will use the word SPICE when referring to the SPICE2 version.

3.3 *pn*-Junction Diode

The Shockley *ideal diode equation* [71] or the diode law is used to describe the diode's *pn*-junction current I_j dependency on the diode junction voltage V_j:

$$I_j = I_s \left(\mathrm{e}^{\frac{V_j}{nV_T}} - 1 \right), \tag{3.1}$$

[2] stable release: 2G.6 / 1983.

[3] stable release: 3f.5 / July 1993.

with I_s being the saturation current (A), V_j the diode junction voltage (V), n the diode ideality factor (emission coefficient), that is assumed to be temperature independent[4]. $V_T = k_B T/q$ is the thermal voltage (V) where q is the elementary charge (1.60218×10^{-19} C), k_B is Boltzmann's constant (1.38065×10^{-23} J/K) and T is the physical temperature (K). In all diode related equations, the temperature is always in kelvin. We will mostly use degree Celsius in text, tables and figures for readability. In the reverse bias domain, following

$$\lim_{V_j \to -\infty} I_j = -I_s, \tag{3.2}$$

the diode current saturates at $-I_s$ for the ideal diode. The ideality factor n was not part of Shockley's equation, but was added later to better match with non-ideal diode behaviour seen in measurements. Therefore Equation (3.1) is a semi-empirical equation.[5]

Both the *pn*-junction diode and Schottky barrier diode can be modeled using an equivalent SPICE diode model as shown in Figure 3.2. The model consists of a voltage dependent current source, parallel to a junction and diffusion capacitance C_j both in series with a resistance R_s. This resistance represents different ohmic resistances present in the semiconductor diode [74]. C_j is defined by both Q_j and Q_d, which represent the two types of charge storage in a semiconductor *pn*-junction, the depletion and diffusion charge. They will be defined later in this chapter. I_j models the impedance of the barrier layer itself and is V_j and temperature dependent [75]. V_j is defined across the current source, excluding R_s. V_d is the diode voltage, defined across the diode terminals including R_s.

The diode equation (3.1) can also be written as a function of the complete diode voltage V_d, to include the diode series resistance R_s:

$$I_j = I_s \left[\mathrm{e}^{\frac{V_d - R_s I_d}{n V_T}} - 1 \right]. \tag{3.3}$$

In this equation R_s plays a role as well. Typically, SBDs have a larger R_s value when the saturation current I_s is larger.

Fig. 3.3 shows the I_j-V_j relationship from Equation (3.1) and the I_j-V_d relationship from Equation (3.3) for an example SBD. Both the forward- and reverse bias regimes are shown for absolute values of voltage and current. Next to the effect of the series resistance, also the temperature effect is clearly visible in the dashed curves. Besides V_T, also I_s is temperature dependent, which will be discussed later.

[4] For low temperatures (below 250 K), the number of parameters being dependent on temperature increases [72, 73].

[5] A diode's ideality factor n with a value larger than one, is not directly related to diode energy dissipation. It only affects the current-voltage dependency and with that the diode's conductance.

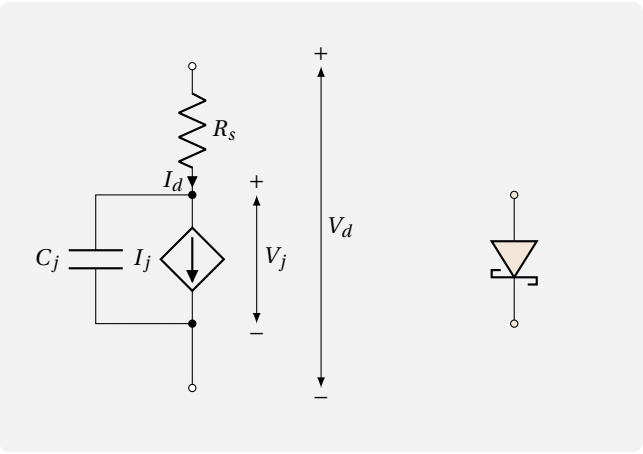


Figure 3.2 Equivalent SPICE diode model (left) and Schottky barrier diode symbol (right).

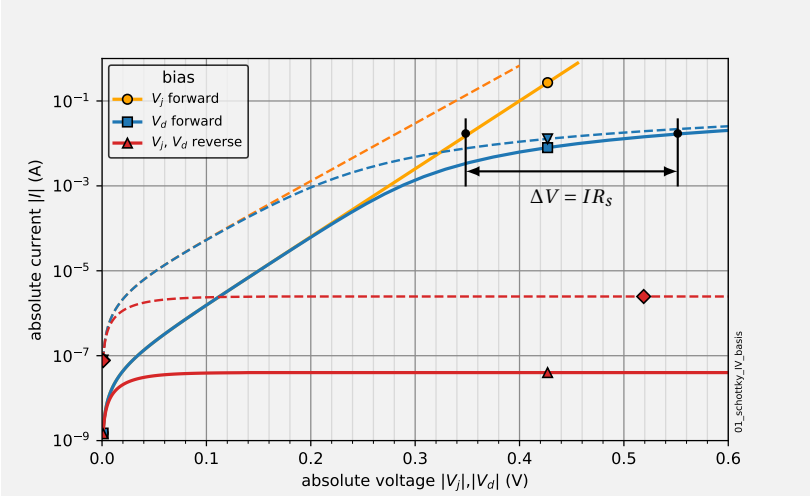


Figure 3.3 Calculated dc Shockley diode current versus voltage, for a Skyworks SMS7621 Schottky diode, both for forward and reverse bias conditions, at a temperature of $T = 300$ K (solid) and $T = 353$ K (dashed). The SPICE diode model parameters, supplied by the vendor, are used. Also shown is the deviation due to R_s from the curve without R_s being $\Delta V = IR_s$.

Non-linear recurrence relations, as Eq. (3.3), are usually difficult to change into closed-form equations with standard techniques. If we want to plot the function $I_j(V_d)$ we need to get rid of I_d in Equation (3.3)[6]. To accomplish this, we make use of the main branch of the Lambert W function [76]: W_0. The Lambert W function is defined to be the multivalued inverse of the function $f(z) = ze^z$. See Appendix A for details. Rewriting the equation for the diode current as a function of the complete diode voltage V_d (exluding C_j, so $I_d = I_j$), and using $\Lambda_s = I_s R_s / (nV_T)$ and $\Lambda_d = V_d / nV_T$, results in:

$$I_j = I_s \left(\frac{W_0\left(\Lambda_s \mathrm{e}^{\Lambda_s} \mathrm{e}^{\Lambda_d}\right)}{\Lambda_s} - 1 \right). \tag{3.4}$$

This equation is used for the I_j-V_d curve in Fig. 3.3.

3.3.1 Diode SPICE parameters

In most WET work, e.g. [41,42], the SBD is modelled using the SPICE *pn*-junction diode model. The model parameters are listed in Table 3.1. These are typically specified by the manufacturer on a diode data-sheet. In this work, I'_s, C'_{j0} and ϕ'_B are the values of I_s, C_{j0} and ϕ_B respectively at a reference temperature T_0.

To give an idea of several commercial available SBDs, an overview is provided in Table 3.2. These parameter values have been used in the construction of Fig. 3.3.

[6] The other parameters I_s, R_s, n and V_T are given for a specific diode and temperature.

Table 3.1 Diode SPICE parameters

Symbol	Name	Parameter	Unit	Default
I_s	IS	Saturation current[a]	A	1×10^{-14}
R_s	RS	Parasitic resistance	Ω	0
n	N	Emission coefficient	-	1
τ_d	TT	Transit time	s	0
C_{j0}	CJO	Zero-bias junction capacitance[a]	F	0
ϕ_B	VJ	Junction potential[a]	V	1
m	M	Junction grading coefficient[b]	-	0.5
ψ_0	EG	Energy gap[c]	eV	1.11
p_i	XTI	I_S temperature exponent[d]	-	3.0
k_f	KF	Flicker noise coefficient	-	0
a_f	AF	Flicker noise exponent	-	1
FC	FC	Forward bias depletion capacitance coeff.	-	0.5
V_B	BV	Breakdown voltage	V	∞
I_B	IBV	Current at breakdown voltage	A	1×10^{-3}
T_0	TNOM	Parameter specification temperature[a]	°C	27

[a] In this work I_s', C_{j0}', ϕ_B' and T' are used to indicate that I_s, C_{j0}, ϕ_B are specified at T_0.
[b] linearly graded junction: 0.33, abrupt junction: 0.5
[c] Si: 1.11 eV, Ge: 0.67 eV, Schottky: 0.69 eV(Al-Si), see [77] for other materials.
[d] pn junction: 3.0, Schottky: 2.0

Table 3.2 Commercially available Schottky barrier diode SPICE model parameters

Part	IS (μA)	RS (Ω)	N	CJ0 (pF)	VJ (V)	M	FC	BV (V)	IBV (μA)
HSMS-282x	0.022	6.0	1.08	0.7	0.65	0.5	-	15	100
HSMS-285x	3	25	1.06	0.18	0.35	0.5	-	3.8	300
HSMS-286x	0.05	6.0	1.08	0.18	0.65	0.5	-	7.0	10
CDB7620	0.04	4	1.20	0.15	0.495	0.35	0.5	10	10
CDF7621	0.09	6	1.10	0.11	0.510	0.30	0.5	2.5	10
CDB7619	0.03	30	1.04	0.11	0.540	0.32	0.5	3.0	10
CDC7623	0.11	5	1.10	0.20	0.510	0.30	0.5	2.5	10
SMS1546	0.3	4	1.04	0.38	0.51	0.36	0.5	3	10
SMS7621	0.04	12	1.05	0.10	0.51	0.35	0.5	3	10
SMS7630	5	20	1.05	0.14	0.34	0.40	0.5	2	100
SMS7621-060	0.026	10.3	1.01	0.13	0.51	0.35	0.5	3	10
RBE05SM20A	5.646	0.234	1.05	40.0	0.50	0.49	0.5	30	1000

For all diodes: TT = 10 ps, EG = 0.69 eV, XTI = 2.

3.4 Schottky Diode

In many cases, energy transfer circuits make use of the metal-semiconductor (MS) Schottky barrier diode (SBD) or in short 'Schottky Diode'. The main reason is the low so-called threshold voltage of the SBD[7]: due to their typically larger I_s value and lower n value compared to *pn*-junction diodes, the SBD reaches a certain current at a lower (forward biased) junction voltage. In other words: the diode current of a SBD is more sensitive to the applied voltage than the current of a *pn*-diode. As can be seen in Fig. 3.3, a diode does not have a specific threshold voltage. A threshold voltage could be defined at a specified diode current, but lacks standardization[8]. Therefore it is better to plot the diode's current-voltage relation to compare one diode with another diode, where a logarithmic current scale provides best insight.

Different semiconductor physics theories exist to model the Schottky diode current. The single thermionic emission-diffusion theory by Crowell and Sze [78] combines the isothermal thermionic emission theory by Bethe [79] and the isothermal diffusion theory by Schottky [80], and describes the total diode current using Equation (3.1) but with the restriction: $V_j > -3V_T$. For the reverse bias domain, the SBD is modelled using a special function as we will see later in this chapter.

We will see that an important difference in modelling, between the ideal *pn*-junction model and a Schottky diode, is the reverse bias characteristic. Where the ideal *pn*-junction diode model saturates at a fixed $-I_s$ level, the Schottky diode shows a reverse bias current which keeps getting more negative with more negative bias voltage.

3.4.1 Saturation current model

Shockley's ideal diode equation (3.1) contains the saturation current variable I_s. This saturation current[9] I_s is dependent on temperature. For SBDs, the diode equation (3.1) is also applicable but the saturation current is described by [78], named Sze model in this work,

$$I_s = AA_R \cdot T^2 \mathrm{e}^{\frac{-\phi_B}{nV_T}} \tag{3.5}$$

with A being the junction area[10], A_R being the effective Richardson constant and ϕ_B the Schottky junction potential. A_R is not dependent on temperature

[7] Another reason is a significant difference in diode capacitance, which will be discussed later.

[8] Multimeters with a diode measurement option indicate the diode voltage drop at a fixed diode current.

[9] In fact, the *reverse* saturation current, as I_d saturates at $-I_s$ in an ideal diode.

[10] for the SMS 7621 estimated to be 638×10^{-9} cm^2

but on the typical semiconductor being used and the crystal orientation. E.g. for metal-Si systems with an impurity concentration of 10^{16} cm^{-3}, for n-type Si, A_R has a value of about 110 A/cm^2/K^2. For p-type Si this is around 30 A/cm^2/K^2. In equation (3.5), the emission coeffient n is added to obtain a proper fit between the forward and reverse I_s-functions. This is like the n factor used in the semi-empirical pn-junction diode model which ideally also doesn't need this factor. The equation has proven to match measurements well, as will be shown later.

The SPICE pn-junction diode model is based on another equation for the saturation current. In the early 50s this was modeled as [81], and in this work named the Schaffner model,

$$I_s = I'_s \mathrm{e}^{a(T-T')}, \tag{3.6}$$

with a being the I_s temperature coefficient. Later, this relationship was adjusted and is what is used in SPICE [70]:

$$I_s = I'_s \left(\frac{T}{T'}\right)^{p_i/n} \mathrm{e}^{\left[\frac{\psi'}{nV_T}\left(\frac{T-T'}{T'}\right)\right]}, \tag{3.7}$$

with I'_s being the saturation current at T' — the reference temperature [11], p_i being the I_S temperature exponent. The quantity ψ' is the energy gap (barrier height, band gap or activation energy) at T', used to differentiate between different types of diodes [12]. Equation (3.7) is equal to Equation (3.6) at $T = T'$ for $a = \psi'/(n\,V_T\,T') \approx 0.089\ K^{-1}$. Figure 3.4 shows the difference between the three models, Equations (3.5), (3.6) and (3.7), for a SMS 7621 Schottky diode. Comparing the SPICE- with the Sze model, we see that the SBD I_s parameter is modeled within 50 % error above 20 °C. The largest difference, at the lower temperatures: a factor of 10 around $T = -30$ °C.

3.4.2 Reverse bias model

Connecting a pn-junction with the n-type region to the positive- and with the p-type region to the negative terminal of a battery makes the junction reverse biased. In this situation, almost no current will flow through the diode. The current flowing is the reverse bias leakage current that flows until the diode breaks down, when a sufficient high voltage is applied to the pn-junction. For the SPICE model, Shockley's ideal diode equation (3.1) describes also the reverse bias behaviour, where the diode current saturates at $-I_s$ for large reverse bias voltage values.

[11] the default value in SPICE is 300 K (26.85 °C).

[12] ψ' equals for Si: 1.11 eV, Ge: 0.67 eV and for Schottky: 0.69 eV.

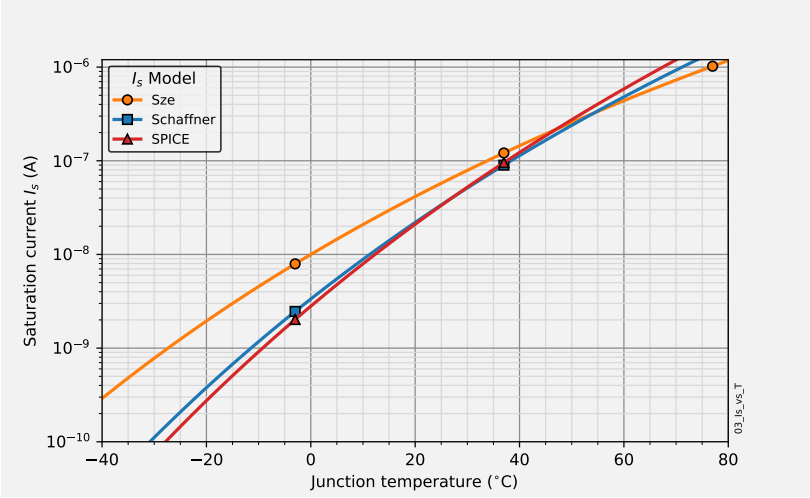


Figure 3.4 Calculated diode saturation current versus temperature of a SMS 7621 diode, showing the SBD model by Sze [78] using $\phi_B = 0.47$, the earlier *pn*-junction diode model by Schaffner [81] and the SPICE model [70] using $p_i = 2$ and $\psi' = 0.69$. These correspond to Equations (3.5), (3.6) and (3.7). The other relevant diode parameter is: $n = 1.064$. Both ϕ_B and n are adjusted to match measured data, which we will see later in this chapter.

The Schottky barrier diode is of a physically different construction compared to the *pn*-junction diode [69]. Therefore a different equation should be used to model its behaviour properly. In this work, the reverse SBD characteristics are modelled using [78]:

$$I_r = -I_j = AA_R T^2 \mathrm{e}^{\left(-\frac{\phi_{B0}}{V_T}\right)} \mathrm{e}^{\left(+\frac{\sqrt{qE/4\pi\epsilon_s}}{V_T}\right)}, \tag{3.8}$$

with

$$E = \sqrt{\frac{2qN_D}{\epsilon_s}\left(-V_j + V_{bi} - V_T\right)}, \qquad -V_B < V_j < -2.8V_T, \tag{3.9}$$

being the magnitude of the electric field and where $\phi_{B0} = \phi_B + \frac{d\phi}{dV} V_j$ is the Schottky junction potential including its sensitivity to V_j, N_D is the donor impurity density, ϵ_s is the semiconductor permittivity and V_{bi} is the built-in potential. The junction voltage range has a lower limit at the breakdown voltage $-V_B$ (more on that later) and an upper limit which is in literature set at $-3V_T$ but taken here slightly higher at $-2.8V_T$ to have a more smooth transition between the different domains. This eases convergence in circuit simulation.

The reverse bias current is shown in Fig. 3.5 as a function of the junction reverse voltage. It is composed of the reverse bias equation (3.8) and the part

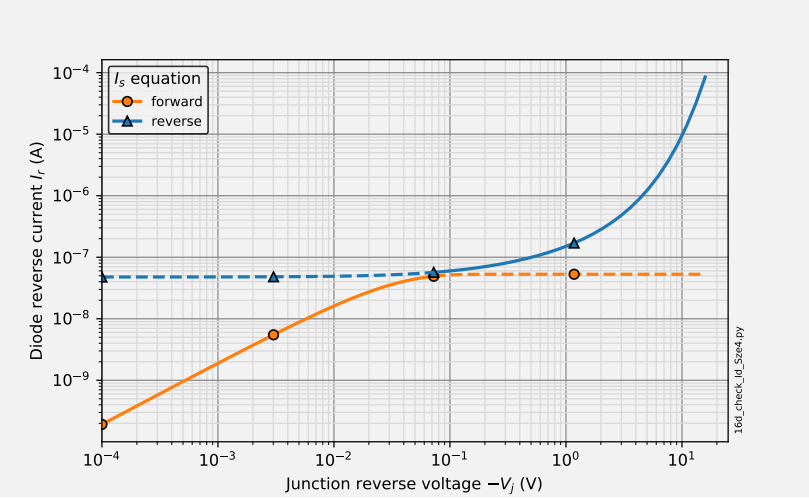


Figure 3.5 Reverse bias diode current versus reverse bias junction voltage of a SMS 7621 diode, using the SBD model by Sze [78]. Equation (3.1) for the junction voltage range $V_j > -2.8V_T$ is named 'forward' (orange), the reverse bias equation (3.8) 'reverse' is used for the range $V_j < -2.8V_T$ (blue). We call the $V_j = -2.8V_T$ point the model switch-over voltage. The curves used are shown solid, the dashed ones are the non-used ranges of the corresponding equations. The diode model parameters used are $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $\phi_B = 0.47$ V, $d\phi_B/dV_j = 0.008$, $R_s = 23\ \Omega$, $I_s = 65.41$ nA and $n = 1.064$, at a temperature of 27 °C.

corresponding to the forward equation (3.1)[13]. We will see later in this chapter that the Sze I_s and reverse bias equations better match with measured data. For the $V_j > -2.8V_T$ region the Sze SBD equation is equal to the SPICE equation and fits well with measured data.

3.4.3 Breakdown region

When the reverse bias voltage is increased, the diode can enter the breakdown region. There are three breakdown mechanisms: thermal instability, tunnelling effect and avalanche multiplication [78]. These are non-destructive and reversible, as long as the semiconductor material is not overheated, which causes thermal damage. The avalanche multiplication is the most important mechanism in junction breakdown.

In simulations, the reverse-bias breakdown effects should be taken into account. In the SPICE model, two parameters are available in this respect[14]: BV (breakdown voltage V_B) and IBV (current I_B at breakdown voltage V_B). A

[13] which is also the SPICE forward- *and* reverse bias equation.

[14] see Table 3.1.

Table 3.3 Reverse-bias low current leakage region

Author	Equation	Region	Ref.
SPICE[a]	$I_j = -I_s + V_j G_{\min}$	$-V_B < V_j < -5nV_T$	[69, 83]
Vladimirescu	$I_j = -I_s + V_j G_{\min}$	$-V_B < V_j < -5nV_T$	[70]
Brinson[b]	$I_j = I_s(e^{V_j/nV_T} - e^{-(BV_{\text{eff}}+V_j)/nV_T} + \frac{BV_{\text{eff}}}{nV_T})$		[84]
Sandler[c]	$I_j = -IBVe^{-(V_B+V_j)/V_T}$		[85]
ADS[d]	$I_j = -Is - IBVe^{-(V_B+V_j)/n_{\text{bv}}V_T}$	$V_j < -10nV_T$	[82]
Piotrowski[e]	$I_j = -I_s\frac{V_j}{nV_T}$	$-XBV < V_j < 0$	[86]

[a] The SPICE diode model, as described by Massobrio [69].
[b] n equals forward emission coefficient, BV_{eff} is based on $V_B - nV_T\ln(IBV/I_{d\text{BV}})$ with $I_{d\text{BV}} = -I_s(e^{-V_B/nV_T} - 1)$.
[c] This is the PSpice® model [69].
[d] n_{bv} is reverse breakdown ideality factor (default = 1.0).
[e] $n = 1$ in forward- and $n = 0.1\cdots1.0$ in reverse-bias regime. XBV is a SPICE generated term: $XBV = V_B - nV_T\ln(\frac{IBV}{IDBV})$ with $IDBV = -I_s(e^{-V_B/nV_T} - 1)$.

common understanding of the SPICE model for the reverse-bias region seems to be lacking. Tables 3.3 and 3.4 list different versions for the junction current, found in literature for both the reverse bias leakage and breakdown regions. In the exponential terms, the factor V_T is sometimes multiplied by n, being often the forward emission coefficient, but sometimes n represents a reverse breakdown ideality factor. It can also be noticed that continuity is not always guaranteed at the boundary between the leakage and breakdown region (in case of Vladimirescu). In the Piotrowski equation, the SPICE internal parameter XBV is used and required to maintain continuity between the two regions. The ADS diode model is the most extensive one. Several extra parameters are available like N_{bv}, being the reverse breakdown ideality factor (ADS equation), for more see [82]. Fig. 3.6 provides a view on the different models for the reverse-bias region. Fig. 3.7 shows the same reverse bias model curves at different temperatures. This gives a better insight into the different temperature dependencies of the various models. When we compare these models with measured data[15], the Piotrowski comes closest but is far from accurate. In this work we will make use of a model based on measured data, to be more accurate.

[15] this will be presented later in this chapter

Table 3.4 Reverse-bias breakdown region

Author	Equation	Region	Reference
SPICE	$I_j = -I_s(e^{-(V_B+V_j)/V_T} - 1) + V_B/V_T$	$V_j < -V_B$	[69, 83]
Vladimirescu	$I_j = -I_s(e^{-(V_B+V_j)/V_T} - 1) - IBV$	$V_j < -V_B$	[70]
Brinson	$I_j = I_s(e^{V_j/nV_T} - e^{-(BV_{\text{eff}}+V_j)/nV_T} + \frac{BV_{\text{eff}}}{nV_T})$		[84]
Sandler	$I_j = -IBVe^{-(V_B+V_j)/V_T}$		[85]
ADS	$I_j = -I_s - IBVe^{-(V_B+V_j)/n_{\text{bv}}V_T}$	$V_j < -10nV_T$	[82]
Piotrowski	$I_j = -I_s(e^{-(XBV+V_j)/nV_T} - 1 + \frac{XBV}{nV_T})$	$V_j < -XBV$	[86]

3.4.4 GMIN element

To prevent failure of the time-domain analysis, in SPICE a variable named minimum conductance (GMIN) is build-in. This minimum conductance is used to protect against an ill-conditioned set of nodal equations and has a default value of 10^{-12} ℧. This conductance is placed parallel across the diode junction (in fact from every node to ground). It is also highly recommended to have a ratio between large and small resistances of less than 10^{12} [70].

3.4.5 Charge storage

Two types of charge storage control the variation in time of a semiconductor *pn*-junction, the diffusion and the depletion- or junction charge. The diffusion charge Q_d is defined as [69]

$$Q_d = \tau_d \, I_j \tag{3.10}$$

with τ_d being the SPICE diode model average transit time TT of the minority carriers. A Schottky barrier diode has $\tau_d = 0$, because of the absence of minority carriers — therefore the diffusion charge plays no role. The junction charge equation is shown next.

The complete diode capacitance equation, containing both forms of charge storage (with the diffusion capacitance in the left term and the junction capacitance in the right one):

$$C_j = \tau_d \cdot g_d + \begin{cases} \dfrac{C_{j0}}{(1 - V_j/\phi_B)^m} & \text{for } V_j < FC \cdot \phi_B, \\ \dfrac{C_{j0}}{(1-FC)^m}\left(1 + \dfrac{m(V_j - FC\cdot\phi_B)}{\phi_B(1-FC)}\right) & \text{for } V_j \geq FC \cdot \phi_B. \end{cases} \tag{3.11}$$

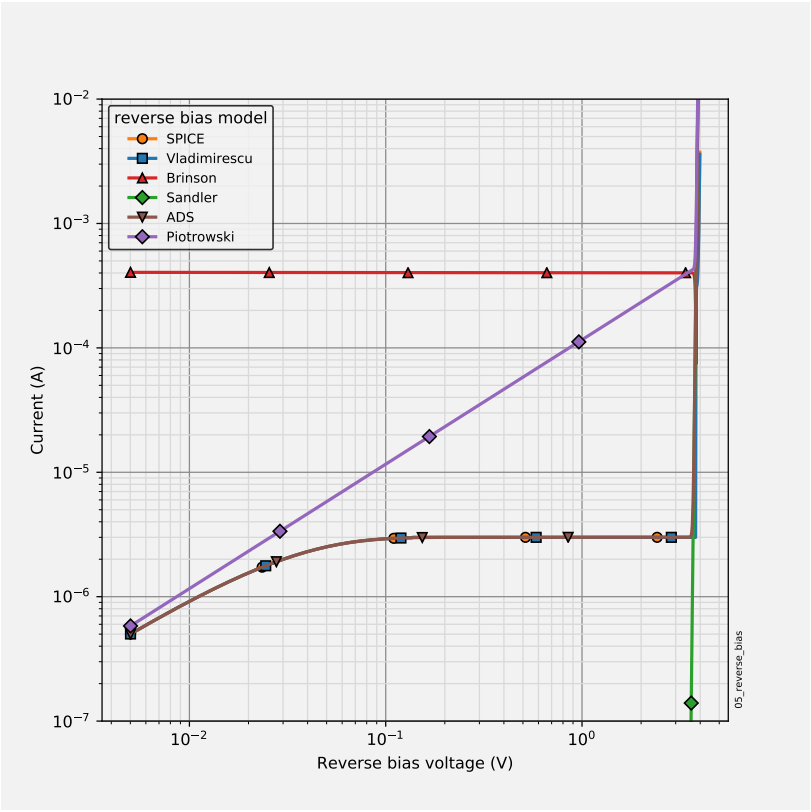


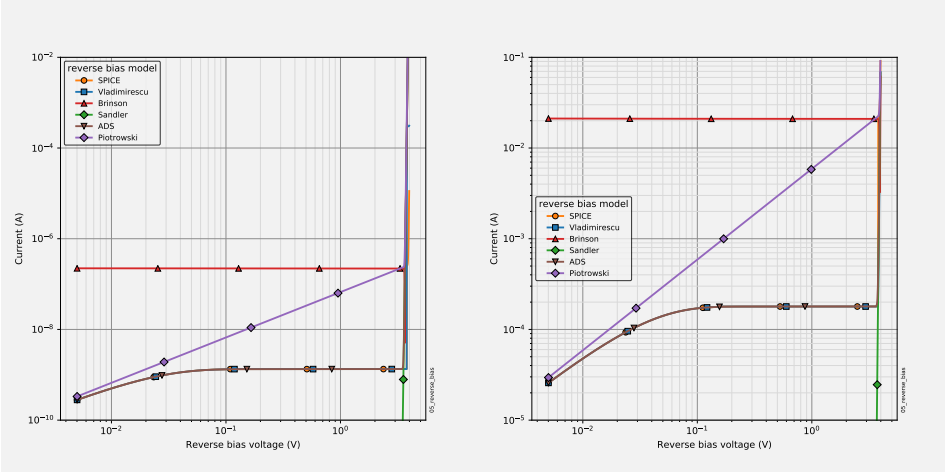
Figure 3.6 Calculated diode reverse bias current against reverse junction voltage of an Avago HSMS-2852 shown for different models at a temperature of 27 °C. BV is set to 3.8 V. In the Piotrowski model, $n = 1.0$ was used.

C_{j0}, ϕ_B, FC and m represent the zero-bias junction capacitance CJO, built-in junction potential VJ, junction capacitance coefficient FC and junction grading coefficient M, respectively[16]. C_j is formed by the insulating barrier between the two diode contacts, being the depletion layer in the substrate. From this equation we see that the value of C_j is dependent on the large-signal, time-varying voltage V_j across the diode junction (excluding R_s) [87]. The junction capacitance C_j is also dependent on temperature as both C_{j0} and ϕ_B are temperature dependent and modeled as [70]

$$C_{j0} = C'_{j0}\left\{1 + m\left[400 \times 10^{-6}(T - T') - \frac{\phi_B - \phi'_B}{\phi'_B}\right]\right\}, \tag{3.12}$$

in which C'_{j0} is the zero-bias junction capacitance as specified at reference

[16] CJO, VJ, FC and M are SPICE diode model parameters as presented in table 3.1.



(a) $T = -40\,°\mathrm{C}$. **(b)** $T = 80\,°\mathrm{C}$.

Figure 3.7 Calculated diode reverse bias current against reverse junction voltage of an Avago HSMS-2852 shown for different models at (a) a temperature of −40 °C and (b) a temperature of 80 °C. BV is set to 3.8 V. In the Piotrowski model, $n = 1.0$ was used.

temperature T', m is the junction gradient coefficient and ϕ_B and ϕ'_B are the junction potential of which the latter is specified at T' and the former, being temperature dependent, is defined as [70]

$$\phi_B = \frac{T}{T'}\phi'_B - 2V_T \ln\left(\frac{T}{T'}\right)^{1.5} - \left[\frac{T}{T'}\psi' - \psi\right], \tag{3.13}$$

with ψ' and ψ being the energy gaps EG at T' and at the actual temperature, respectively. The energy gap ψ is also temperature dependent. Calculations and measurements show that ψ decreases for most materials with rising temperature and is usually modeled in compact form by use of the Varshni equation [88]

$$\psi \approx \psi_0 - \alpha\frac{T^2}{T+\beta}, \tag{3.14}$$

where ψ_0 is the gap's width extrapolated to $T = 0$ K, $\alpha > 0$ and $\beta > 0$ are material parameters. Table 3.5 provides values of α and β for Si and GaAs.

The above equations provide enough detail and accuracy for the type of work described in this thesis. More details on e.g. the nonlinear bias dependence of the barrier height or general Schottky barrier modeling details can be found in literature [89, 90]. As ψ_0 is defined at $T = 0$ K in Equation (3.14), the 0.69 value at room temperature should be specified using $\psi_0 = 0.735$, which will

Table 3.5 Energy gap of silicon and gallium arsenide

Material	α(eV/K)	β(K)
Si[a]	7.02×10^{-4}	1108
Si[b]	4.9×10^{-4}	655
GaAs	5.80×10^{-4}	300

[a] After Varshni [88], accurate up to 415 K (142 °C)
[b] After Alex [91], accurate up to 750 K (477 °C)

be used in this work when $\psi' = 0.69$ is applicable. The SBD energy gap or the Schottky barrier voltage EG parameter is typically set to a value of 0.69. When SPICE just came out, this value was used as a SBD default, corresponding to an aluminium-silicon contact [69, 70]. The actual value depends on the type of materials chosen and can vary form 0.3–0.9 [77].

The diode capacitance equation (3.11) consists of two parts. The upper one is the Fleri-Cohen equation [87] and becomes singular at $V_j = \phi_B$. For this reason numerical simulators, like SPICE, make use of the extra lower part of Equation (3.11), which is a linear approximation to the upper part. A new parameter FC is introduced for this approximation. Normally under a large forward bias situation, the diffusion capacitance will dominate over the junction capacitance, which is not exactly modeled using this two-equation approach. The diffusion capacitance is approximately proportional to the square of the intrinsic carrier concentration and thus depends on the semiconductor bandgap and temperature in an exponential fashion $\left(e^{-\psi/k_B T}\right)$. Therefore the junction capacitance tends to be significant for devices with a large energy band-gap and/or operating at low temperatures. As the diffusion capacitance is not present in Schottky diodes, Equation (3.11) should be used with care for these devices in this region. A physically justified model for the semiconductor space charge region capacitance is proposed by Van Halen [92]. This model only requires the zero bias capacitance, the built-in potential and the junction grading coefficient as input parameters, eliminating the fitting parameter FC used in SPICE. For voltages larger than the built-in potential the space charge layer consists of charge carriers being injected into the regions adjacent to the metallurgical junction, and the junction capacitance value will decrease [93]. This effect is not accounted for in the current SPICE diode model. The Van Halen equation for

the space charge region junction capacitance is [92]

$$C_j = C_{j0}\left(1 - \frac{V_j}{\phi_B} + \frac{V_T}{2\phi_B}\mathrm{e}^{(V_j-\phi_B)/V_T}\right)^{-m}. \tag{3.15}$$

An example of using the above set of equations, defining the diode's junction capacitance, is provided in Fig. 3.8. For an Avago HSMS-2852 Schottky diode, the following is shown: the Fleri-Cohen equation (3.11 upper part), the SPICE equation (3.11) and the Van Halen equation (3.15). In this figure, the singularity of the Fleri-Cohen model is clearly visible.

Later in this chapter we will present an ADS implementation of a SBD including the model of the diode capacitance. The three equation options are included in this model. From using this model in the rectifier circuits presented in this work, we see that the diode junction typically stays below the point where the three equations diverge. This is due to the rectifier self-biasing effect caused by the dc-current causing a dc-voltage at the rectifier output. The conclusion is that for the circuits in this work, it doesn't matter which of the three equations is used.

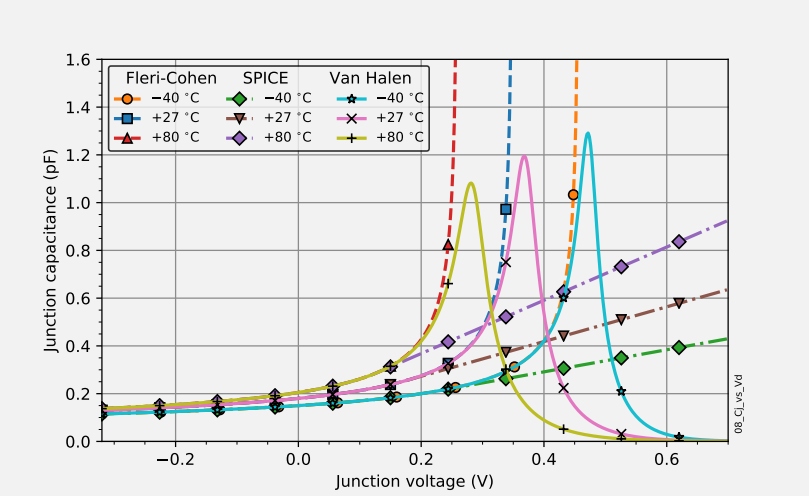


Figure 3.8 Diode junction capacitance value of an Avago HSMS-2852 using Eqs (3.11)-(3.15), as a function of diode junction voltage V_j and temperature, shown for the Fleri-Cohen (dashed), SPICE (dash-dot) and Van Halen (solid) models.

3.5 Diode Current-Voltage Measurement

In order to verify the typically used SPICE diode models, a series of dc current-voltage measurements is carried out. The data is compared with the diode

equation (3.1) part of the diode model. This is the voltage controlled current source and series resistance in Fig. 3.2. In this section two different SBD types are measured on their dc characteristics and compared to the SPICE diode dc performance, including the temperature dependency.

To validate the diode current-voltage (I-V) model, a measurement is carried out on five Avago HSMS-2852 and Skyworks SMS7621 diode pairs (ten diodes of each type). Using multiple diodes provides insight into component to component variation. The limited number of 10 diodes for each type was chosen for practical reasons. The ability to manually switch between the diode samples, when using a temperature chamber, did set the practical boundary. For accurate current measurement results an Agilent (Keysight) B1500A Semiconductor Device Analyzer is used together with a CTS climatic test cabinet (series C) to control the environmental temperature. For each of the diodes, both the forward and reverse dc I-V characteristic is measured by applying a voltage between the anode and cathode and measuring the resulting diode current. This is done at temperatures of −40, 0, 26.85, 40 and 80 °C. Fig. 3.9 shows the test PCB used for the measurements and Fig. 3.10 shows the B1500A, measuring an Avago HSMS-2852 forward I-V curve at 0 °C.

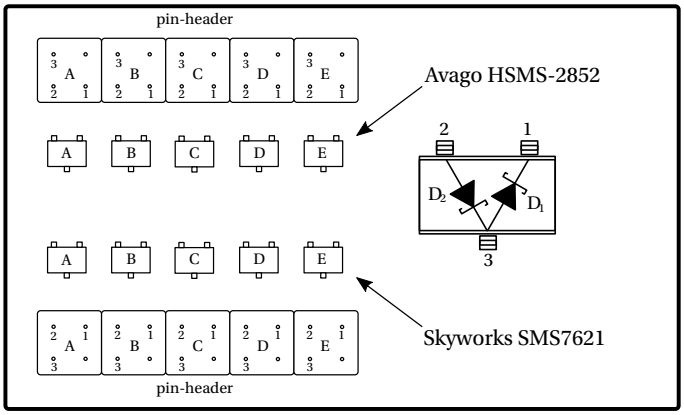


Figure 3.9 Test PCB used to measure Avago HSMS-2852 (upper) and Skyworks SMS7621 (lower) Schottky diode pairs containing 10 diodes named D1–D10. The 5 diode pairs are named A–E for each type and connected to pin-headers above/below, numbered A1, A2, etc. The diodes are accessible as (anode-cathode): D1 = A3-A1, D2 = A2-A3, D3 = B3-B1, etc.

The measured SMS7621 reverse- and forward-bias currents are shown for $T = 26.85$ °C in Fig. 3.11. From this figure we can see that among the 10 diodes, a minimum and maximum diode response can be found, as well as a calculated mean response. For the SMS7621 a minimum response is found for diode 5 (D5) and a maximum response for diode D2, where diode D6 shows the closest

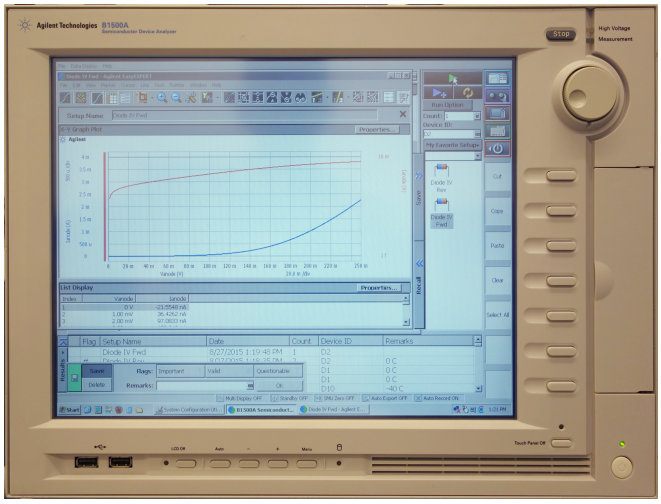
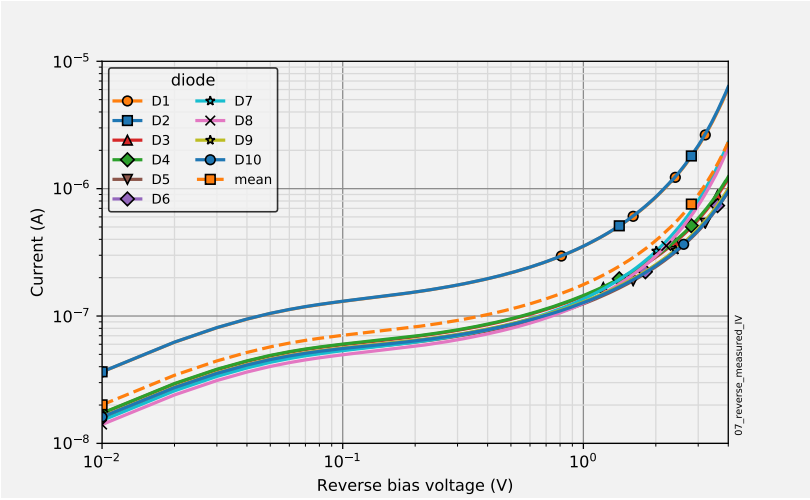


Figure 3.10 Agilent B1500A Semiconductor Device Analyzer measuring an Avago HSMS2852 diode forward I-V curve at 0 °C.

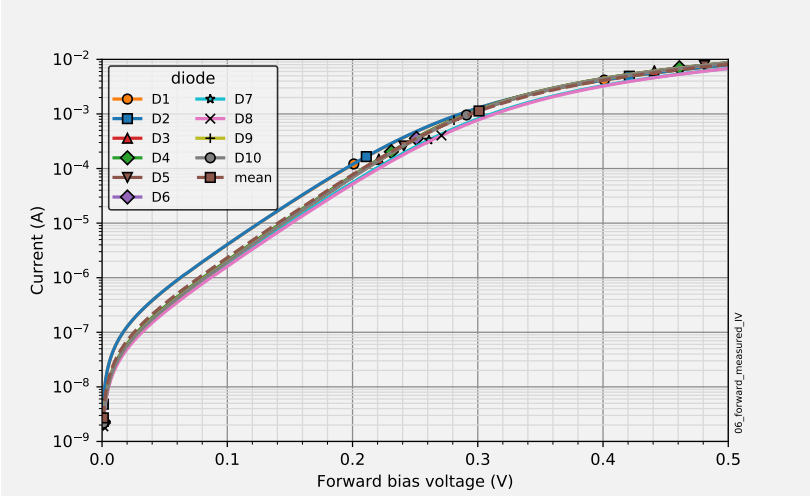
response to the mean response. For the HSMS-2852 these diodes are D10, D5 and D3, respectively.

The measured HSMS-2852 reverse bias current at its specified breakdown voltage of BV = 3.8 V matches the data sheet[17]. For the SMS 7621 this is not the case as the measured value of 0.5 μA at BV = 3 V is a lot less compared to the specified 10 μA. A measurement based model will result in a more accurate SMS 7621 model on this aspect.

[17] The measured HSMS-2852 bias currents are available at a later section.



(a) Reverse bias response.



(b) Forward bias response.

Figure 3.11 Skyworks SMS7621 current measurement on 10 devices against bias voltage at $T = 26.85\,^{\circ}\mathrm{C}$, together with the mean response (dashed line).

3.6 Schottky Diode Model

As the SBD has a clear difference in behaviour compared to the *pn*-junction diode, it is useful to create a SBD model for circuit simulation. Different techniques can be applied to obtain a proper model, being a representation of the real world within acceptable margins. In this work, two different approaches are investigated: the use of a macro model and an equation based model. A macro model consists of available simulator circuit element models and therefore doesn't require a user to build an equation based model.

For both the Avago HSMS-2852 and Skyworks SMS 7621 diodes, the two approaches are applied. The first approach makes use of the first Russell method [94] (three-point I-V method), as forward bias region model. The reverse bias region is modelled using a macro model. Secondly the diodes are modelled using equations only, corresponding to the physical Schottky barrier devices, which are different from the *pn*-junction diodes.

3.6.1 Forward bias model

First the Avago HSMS-2852 and Skyworks SMS 7621 diodes are modelled, following Russell's method by selecting three data points d_1, d_2, d_3 on the measured I-V curves, corresponding to V_1, V_2, V_3 for the forward voltage points and I_1, I_2, I_3 for the corresponding forward current points. Secondly, the series resistance R_s is calculated using

$$R_s = \frac{(V_2 - V_1) + (V_1 - V_3)\left\{\frac{\ln\left(\frac{I_1}{I_2}\right)}{\ln\left(\frac{I_1}{I_3}\right)}\right\}}{(I_2 - I_1) + (I_1 - I_3)\left\{\frac{\ln\left(\frac{I_1}{I_2}\right)}{\ln\left(\frac{I_1}{I_3}\right)}\right\}}, \tag{3.16}$$

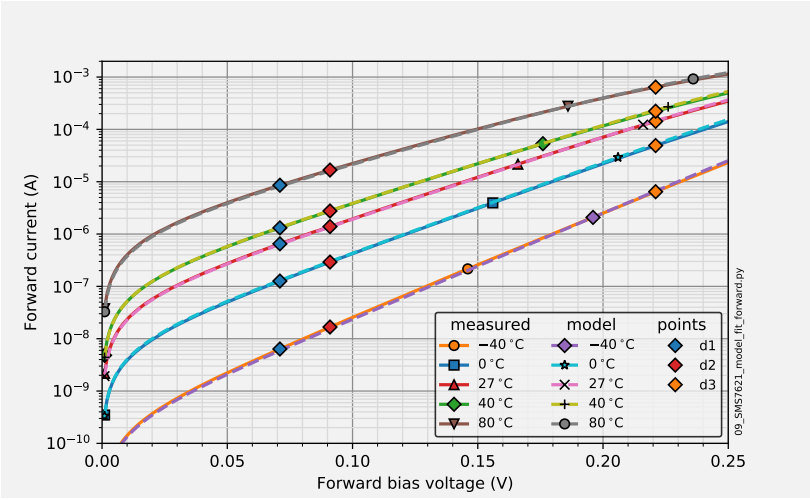
the emission coefficient N is calculated using

$$n = \frac{(V_1 - V_2) + R_s(I_2 - I_1)}{V_T \ln\left(\frac{I_1}{I_2}\right)}, \tag{3.17}$$

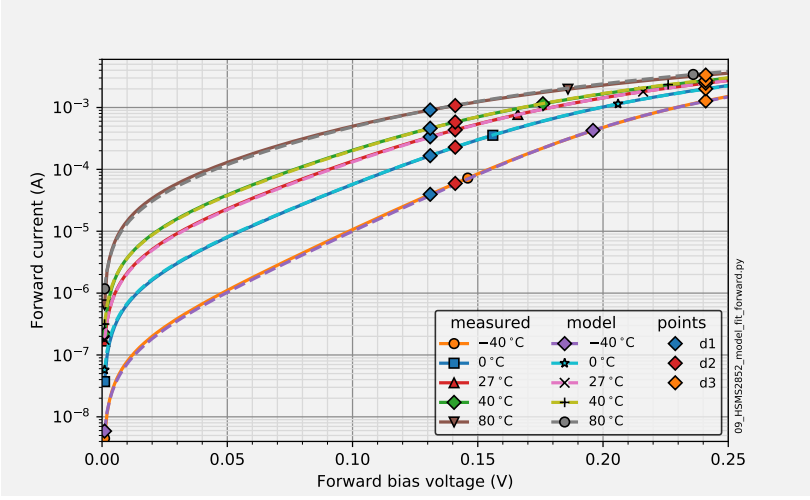
and the saturation current I_s as

$$I_s = \frac{I_1}{e^{\left(\frac{V_1 - R_s I_1}{nV_T}\right)}}. \tag{3.18}$$

With the obtained R_s,n and I_s values, the dc diode model is available using Equation (3.3). Fig. 3.12 shows the results. To draw the model curves in this figure, Equation (3.4) is used.



(a) Skyworks SMS7621 (nominal = D6).



(b) Avago HSMS2852 (nominal = D3).

Figure 3.12 Forward I-V nominal diode measurement at a temperature of $T = -40$, 0, 27, 40 and 80 °C together with the Russell model (dashed) and -data points d_1, d_2, d_3.

The obtained error between model and measured values is calculated using a normalized root mean square error (NRMSE) ϵ_{NRMS} defined as

$$\epsilon_{\text{NRMS}} = \sqrt{\frac{\sum |\epsilon_i|^2}{N}} \tag{3.19}$$

with N being the number of data-points and ϵ_i being the normalized error at the i-th measured data point, defined as

$$\epsilon_i = \frac{I_{d,\text{model}} - I_{d,\text{meas}}}{I_{d,\text{meas}}}. \tag{3.20}$$

The choice for the d_1, d_2 and d_3 values is made to obtain the lowest ϵ_{NRMS}. When applying the first Russell-method to the measured data, temperature dependent values become available for R_s, n and I_s. A comparison shows that using a fixed value for R_s and n (taken at T = 300 K or 26.85 °C) gives almost the same error between model and measurement, compared to the use of temperature dependent values. As diode simulation models typically don't provide a temperature dependence on these parameters, the fixed values are used.

With fixed R_s and n values, the method still obtains a temperature dependent saturation current I_s. This temperature dependence is modelled in SPICE using Equation (3.7), and shows an almost straight line, when plotted on a logarithmic scale against temperature. To further improve the measured data fit of the model, the energy gap at a temperature of T = 300 K, ψ', is manually optimized. For Schottky Barrier Diodes (SBD) the energy gap is equal to 0.69 eV at T = 300 K, according to literature and datasheets [69, 78, 94]. The value for ψ' giving the lowest ϵ_{NRMS} value, is found to be ψ'=0.310 eV (ψ_0 = 0.355 eV) for the Avago and ψ'=0.460 eV (ψ_0 = 0.505 eV) for the Skyworks type[18]. This provides the lowest ϵ_{NRMS} value for the error in the modelled saturation current against the 5 different temperature values. The ψ' value can be used for I-V modelling over all temperatures and junction capacitance C_j modelling at T = 300 K only. A diode C-V measurement is necessary to verify Equation (3.13). Apparently the datasheets of the Avago HSMS-2852 and Skyworks SMS7621 look inaccurate in stating EG = 0.69 as value for this SPICE parameter. These Schottky diodes likely have a different combination of semiconductor material and metal-type compared to other — previously more commonly used — Schottky diodes. Semiconductor physics literature provides tables which report the EG value for different material combinations [78]. Fig. 3.13 shows the mismatch between

[18] Correcting the obtained saturation current at 25 °C to 26.85 °C (300 K), we have I_s' =5.541 × 10^{-6} A for the Avago HSMS-2852 (the Skyworks SMS7621 was measured at 26.85 °C, therefore no correction is needed for this type).

the datasheet SPICE model parameters and the measured data. Modifying the SPICE Energy gap EG parameter is not new. A power Schottky diode example shows lowering of the EG value of a silicon 1N5817 diode from the original supplier value of 1.11 eV into 0.6 eV, found from temperature dependent I-V measurements [95]. They also report a series resistor R_s temperature dependence. The energy gap EG value is in reality even temperature dependent, as shown in literature [73, 96, 97].

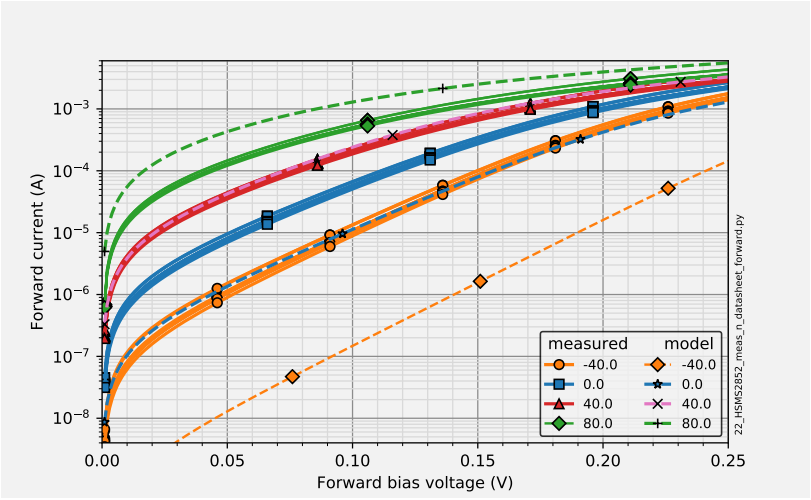


Figure 3.13 Avago HSMS2852 forward I-V measurement on 10 devices at a temperature $T = -40$, 0, 40 and 80 °C (straight). Also shown are the calculated SPICE model curves, based on the Avago data-sheet SPICE parameter values (dashed) for the same temperature values. The mismatch between model and measurement is clear with a $\epsilon_{\text{NRMS,forw}}$ of 77.1 %.

Tables 3.6 and 3.7 provide an overview of the obtained forward bias model parameter values. The obtained ϵ_{NRMS} error is clearly smaller for the Russell method model result compared to the data-sheet SPICE model parameter values. This is mainly due to the improved ψ' value, resulting in a more accurate diode current temperature dependency.

3.6.2 Reverse bias macro model

For the reverse bias situation, the ideal *pn*-junction diode model does not result in a fit on the measured values. One way to obtain a more accurate SBD model is to make use of a macro model, which can e.g. be based on standard SPICE elements. This will result in a model that corresponds better with a realistic diode instead of an ideal diode. Diode macro model examples are suggested by Sandler [85], Piotrowski [86], Lepkowski [98], Sischka [99] and Wong [100].

Table 3.6 HSMS-2852 Russell method forward-bias model result and data-sheet SPICE model parameters. Extracted temperature range: $-40\cdots+80\,^{\circ}\mathrm{C}$.

Parameter	minimal	nominal	maximal	data-sheet	unit
R_s	26.2	24.0	21.0	25	Ω
n	1.130	1.141	1.141	1.06	
I_s	4.96	5.57	6.55	3.00	μA
ψ'	0.32	0.31	0.31	0.69	eV
ψ_0	0.365	0.355	0.355	-	eV
ϕ'_B	0.335[a]	0.335[a]	0.335[a]	0.35	V
$\epsilon_{\mathrm{NRMS,forw}}$	4.28	4.35	5.30	77.44 [a]	%
diode	D10	D3	D5		

[a] Compared with nominal diode D3. See also Fig. 3.12.

Table 3.7 SMS7621 Russell method forward-bias model result and data-sheet SPICE model parameters. Extracted temperature range: $-40\cdots+80\,^{\circ}\mathrm{C}$.

Parameter	minimal	nominal	maximal	data-sheet	unit
R_s	26	17	40	12	Ω
n	1.055	1.068	1.081	1.05	
I_s	51.6	55.0	121	40	nA
ψ'	0.465	0.460	0.404	0.69	eV
ψ_0	0.510	0.505	0.449	-	eV
ϕ'_B	0.335[a]	0.335[a]	0.335[a]	0.35	V
$\epsilon_{\mathrm{NRMS,forw}}$	5.26	3.88	7.16	72.48 [a]	%
diode	D5	D6	D2		

[a] Compared with nominal diode D6. See also Fig. 3.12.

As an example the Sischka macro model is applied to the Avago HSMS-2852 and Skyworks SMS 7621 SBDs using a reverse diode, placed parallel to the forward diode. The advantage of this model is the usage of a second SPICE diode model, only having a few odd (not typical for a diode) parameter values. Fig. 3.14 shows the schematic of the macro model. Due to the fact that the breakdown effect is included in the measured curves by nature, we should not make use of the SPICE breakdown parameter BV when the model is fitted to the measured data. The reverse-bias leakage region is mainly modelled by the reverse diode D_r. This diode has special values for the series resistance R_{sr}, the emission coefficient n_r, the saturation current I_{sr} and its temperature coefficient p_{ir}. The reverse diode zero-bias junction capacitance C_{j0r} is set to zero as this capacitance is already modelled by the forward diode. All other parameters have the same values as in the forward diode model.

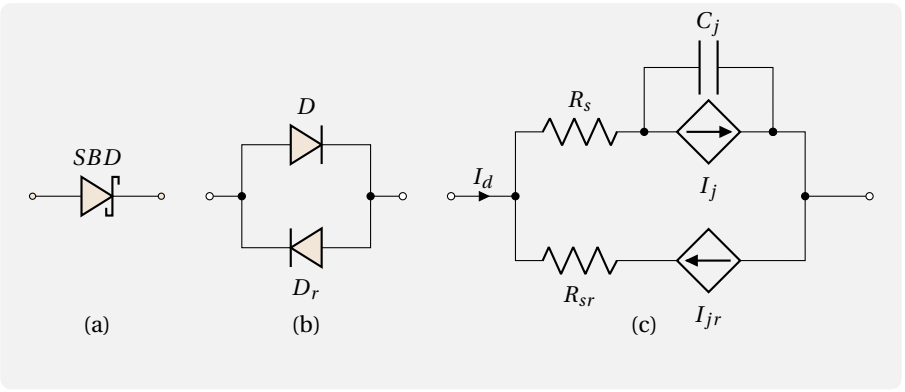


Figure 3.14 SBD Sischka macro model schematic with forward- and reverse-bias elements: a) Schottky diode circuit component, b) macro model consisting of SPICE diode models. D is the forward- and D_r the reverse-biased diode, c) detailed diode macro model. The model parameters are given in Table 3.8. I_d is the diode current, R_s is the forward diode series resistance, R_{sr} is the reverse diode series resistance, I_j the forward diode junction current, I_{jr} is the reverse diode junction current, C_j is the forward diode junction capacitance.

The reverse diode parameter values are found by manually matching the calculated response with the measured mean result for minimal ϵ_{NRMS}, after first applying the first Russell method for the forward diode parameter values.

The resulting HSMS-2852 and SMS 7621 reverse-bias SPICE diode parameters are provided in Tables 3.8 and 3.9.

Table 3.8 HSMS-2852 SPICE Sischka reverse-bias macro model and data-sheet SPICE model parameter.

Parameter	minimal	nominal	maximal	data-sheet	unit
ϕ'_B	0.335[a]	0.335[a]	0.335[a]	0.35	V
R_{sr}	3.50	2.80	1.42	-	kΩ
n_r	31.1	30.2	30.0	-	
I_{sr}	6.9	8.0	11.97	-	μA
p_{ir}	415	368	320	-	
$\epsilon_{\text{NRMS,rev}}$	13.14	12.88	12.48	143.8 [b]	%
diode	D10	D3	D5		

[a] Derived from measured data in equation based Sze-model process.
[b] Compared with nominal diode D3. See also Fig. 3.12.

Table 3.9 SMS7621 SPICE Sischka reverse-bias macro model and data-sheet SPICE model parameter.

Parameter	minimal	nominal	maximal	data-sheet	unit
ϕ'_B	0.470[a]	0.470[a]	0.470[a]	0.51	V
R_{sr}	3.6	42	10	-	kΩ
n_r	48	47	48	-	
I_{sr}	42	43.4	200	-	nA
p_{ir}	860	862	730	-	
$\epsilon_{\text{NRMS,rev}}$	19.36	17.52	23.34	126.3 [b]	%
diode	D5	D6	D2		

[a] Derived from measured data in equation based Sze-model process.
[b] Compared with nominal diode D6. See also Fig. 3.12.

ADS Sischka macro model

The ADS implementation of the SBD Sischka macro model is shown in Fig. 3.15. This model includes the reverse bias breakdown effect — up to the maximum reverse bias voltage used — and is based on the measured nominal SMS 7621 diode.

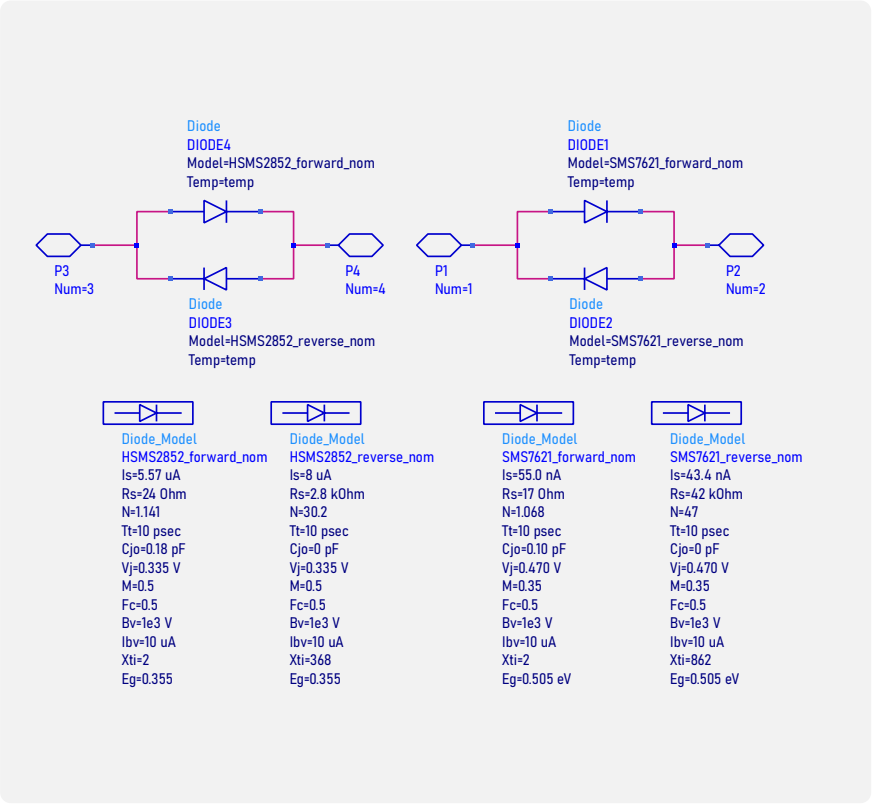
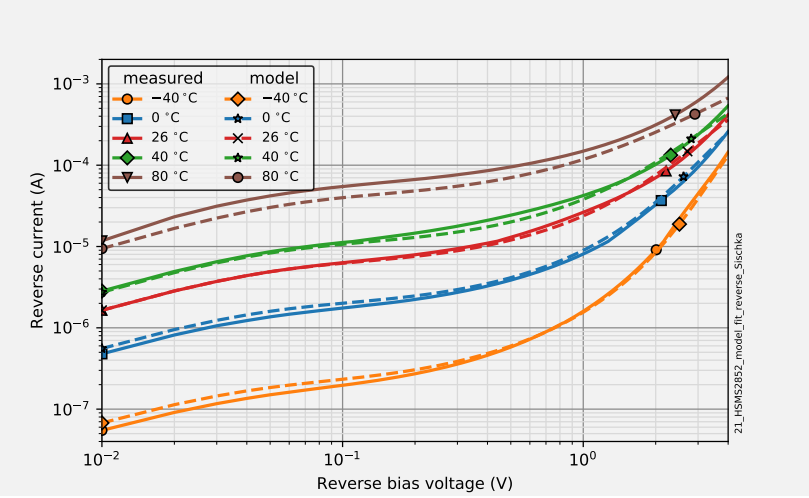


Figure 3.15 ADS Sischka macro SBD model based on nominal measured HSMS-2852 and SMS 7621 diodes. The reverse bias breakdown effect is inherently covered in the model as this effect is included in the fitted reverse diode behaviour.

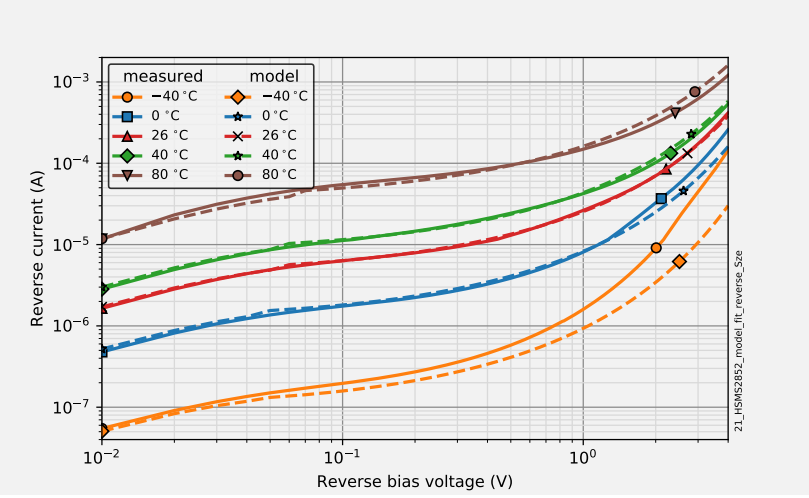
The HSMS-2852 comparison between this model and the nominal measurement D3 is shown in Fig. 3.16 (a). Likewise for the SMS 7621 the comparison between the macro model and the nominal measurement D6 is shown in Fig. 3.17 (a). The model provides a better match compared to the ideal SPICE model. The reverse current model ϵ_{NRMS} for the nominal HSMS-2852 diode, equals 12.9 % where the SPICE model with supplier parameter values obtains 143.8 %. For the SMS 7621 these numbers are 17.5 % and 126.3 % respectively. Having a different series resistance for forward (R_s) and reverse (R_{sr}) bias voltages is an

advantage for the Sischka model, compared to the Sze model (presented in the next section). This model is compared to the measured data in Figs. 3.16 (b) and 3.17 (b) and shows a larger error mainly at $T = -40\,^{\circ}\mathrm{C}$.

A likely cause for this is the fixed series resistance R_s value used both for the forward and reverse bias regions, where a different reverse bias R_{sr} is included in the Sischka macro model.

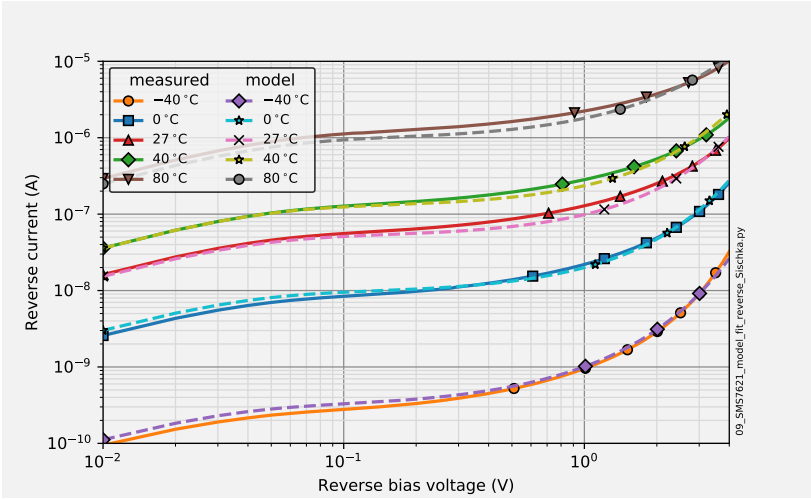


(a) Sischka macro model, $\epsilon_{\mathrm{NRMS,rev}} = 20.4\ \%$.

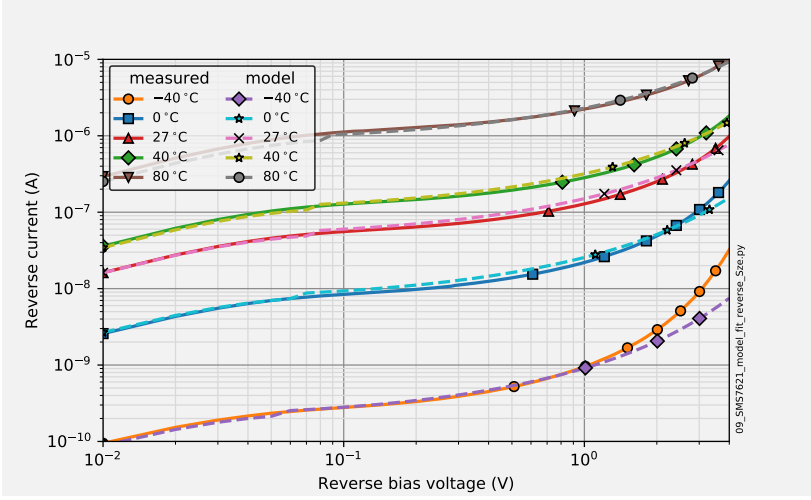


(b) Sze equation model, $\epsilon_{\mathrm{NRMS,rev}} = 23.9\ \%$.

Figure 3.16 Comparision of calculated HSMS2852 reverse bias models and nominal diode D3 measured data for different temperatures T.



(a) Sischka macro model, $\epsilon_{\mathrm{NRMS,rev}} = 17.5\ \%$.



(b) Sze equation model, $\epsilon_{\mathrm{NRMS,rev}} = 16.4\ \%$.

Figure 3.17 Comparision of calculated SMS7621 reverse bias models and nominal diode D6 measured data for different temperatures T.

Table 3.10 Statistical data for the HSMS-285X family[a].

Param.	data-sheet	max	min	mean	std. dev.	percent	unit
R_s	25.0	49.3	25.7	42.2	6.03	14.3 %	Ω
n	1.055	1.176	1.056	1.098	0.03	2.6 %	
I_s	3.0	4.20	1.43	2.56	7.02	27.4 %	μA
C_{j0}	0.17	0.256	0.185	0.218	0.018	8.2 %	pF
BV	3.8	6.3	3.3	4.8	0.93	19.4 %	V

[a] Avago data taken from lot 5549#05 (January, 1997)(C.L. Lim – Avago, personal communication, 21 September 2015).

To provide another viewpoint on the possible spread on the SPICE parameters, statistical data measured on a batch of 20 HSMS-285X diodes, provided by Avago is shown in Table 3.10. Note the difference between the data-sheet nominal and mean values. The observed offset in ψ_0 with the data-sheet value of 0.69 was not recognized by Avago[19]. Also $\phi' = 0.35$ is kept as is.

3.6.3 Equation based Sze model

The equation based SBD model, named Sze model in this work, is based on equations (3.1), (3.5), (3.8) and with one of the reverse-bias low current leakage and breakdown region equations from Tables 3.3 and 3.4. From the I-V measurements it follows that $BV > 4$ V, which means that for the typical RF-power levels ($P_s < -5$ dBm) used in radiated WET, the breakdown region is not reached for both measured diode types. This work also contains simulation graphs with input power levels up to +30 dBm. In these results, the breakdown effects of the specific diodes are not included. This is done to keep the results more generally applicable, as each diode type has a different breakdown voltage.

Tabel 3.11 contains the parameter values for the Sze-model, obtained using a manual optimization process. For the forward biased region, this model is equal to the Sischka macro model, they differ on the reverse bias region. A reverse bias comparison of the Sze model results with the measured data is shown in Fig. 3.16 (b) for the HSMS2852 SBD and in Fig. 3.17 (b) for the SMS 7621 SBD. For finding the diode model parameter values: first estimate $d\phi_B/dV_j$ based on a forward biased dc-measurement, to find the proper gradient for the I_j versus V_j curve. Next estimate the reverse bias parameters to have a smooth transition

[19] Personal communication with C.L. Lim – Avago, 21 September 2015.

Table 3.11 HSMS2852 and SMS7621 derived physical Sze-model parameter values.

Parameter	HSMS2852	SMS7621	unit
R_s	24.0	23.0	Ω
n	1.140	1.064	
A^*	32	24	A/cm^2/K^2
ϕ'_B	0.335	0.470	V
N_D	15×10^{22}	1×10^{23}	
V_{bi}	0.12	0.05	V
ϵ_s/ϵ_0	11.8	11.8	
ϕ_{B0}	$\phi_B + 0.015V_D$	$\phi_B + 0.008V_D$	V
A	185×10^{-9}	638×10^{-9}	cm^2
V_{th} [a]	$-2.0V_T$	$-2.8V_T$	V
ψ_0	0.355	0.505	eV
$\epsilon_{\text{NRMS,forw}}$	4.35	3.88	%
$\epsilon_{\text{NRMS,rev}}$	24.5	17.2	%
nominal diode	D3	D6	

[a] Switch-over voltage between reverse and forward current model (see Fig. 3.5).

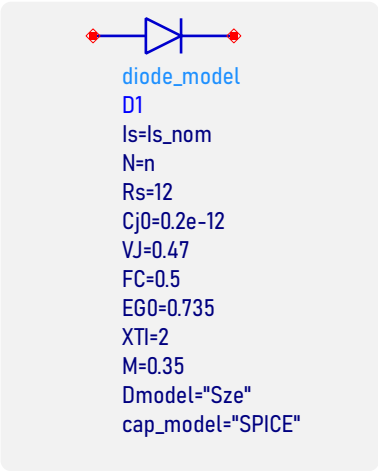
between forward- and reverse bias functions, also for the first- and preferably second derivatives, as that eases convergence in simulations.

The Sze reverse bias model shows in particular a mismatch with the measured data for the $T = -40\,^\circ$C case and high drive level (which causes the dc bias voltage to be larger, resulting in a more negative diode voltage swing). A likely cause for this is the fixed series resistance R_s value used both for the forward- and reverse bias regions, where a different reverse bias R_{sr} is included in the Sischka macro model. See Fig. 3.18 (b) for a schematic representation of the Sze model.

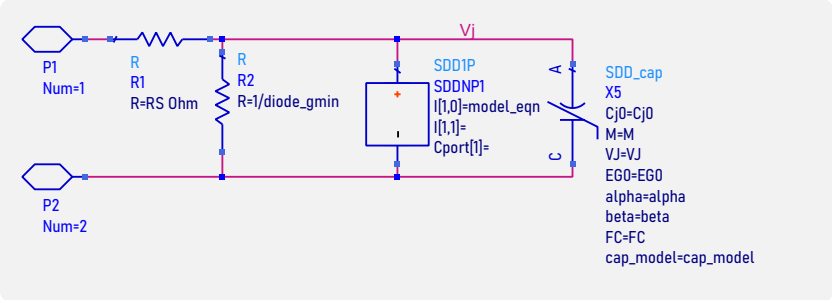
ADS Sze model

The ADS implementation of the SBD Sze model is shown in Fig. 3.18, showing the series resistance R_s as R1, the parallel GMIN element as R2 (see Section 3.4.4),

the non-linear junction resistance symbolically defined device (SDD) element and the non-linear junction capacitance C_j as X5. The junction resistance equations implementation is shown in Fig. 3.19 and the junction capacitance model sub-circuit is shown in Fig. 3.20.



(a) Sze SBD circuit component with parameters.

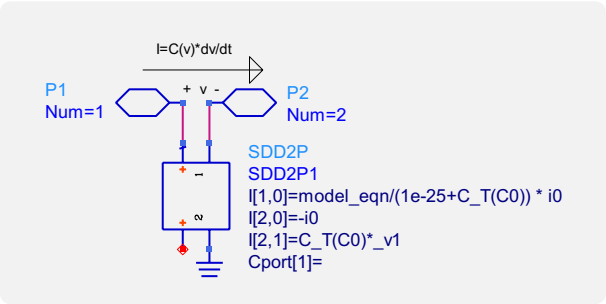


(b) Sze model sub-circuit implementation. R2 respresents the GMIN element, X5 the junction capacitance C_j.

Figure 3.18 ADS Sze SBD model implementation. See Fig. 3.19 and 3.20 for more details.

```
Var Eqn VAR
VAR7
model_eqn=if (Dmodel == "SPICE") then SPICE_eqn else Sze_eqn endif
SPICE_eqn=Istemp*(exp_soft(_v1/(N*Vt))-1)
Istemp=Is*(tempkelvin/300)**(XTI/N)*exp(EG(300)/(N*Vt)*(tempkelvin-300)/300)
exp_soft(x)=if (x < max_arg) then exp(x) else (x+1-max_arg)*max_exp endif
Sze_eqn=if (_v1 > (-2.8*Vt)) then Sze_fwd_eqn else Sze_rev_eqn endif
Sze_fwd_eqn=Ismod*(exp_soft(_v1/(N*Vt))-1)
Ismod=A*Ass*tempkelvin**2*exp_soft(-VJ0/(N*Vt))
Sze_rev_eqn=-A*Ass*tempkelvin**2*exp_soft(-VJ0/Vt)*exp_soft(sqrt(qelectron*ee/(4*pi*eps))/Vt)
A=638e-9
Ass=24
VJ0=VJ+0.008*_v1
ee=sqrt(2*qelectron*ND/eps*(-_v1+vbi-Vt))
eps=11.8*e0
ND=1e23
vbi=0.05
Vt=boltzmann*tempkelvin/qelectron
EG(T1)=EG0-alpha*T1**2/(T1+beta)
alpha=7.02e-4
beta=1108
max_arg=ln(max_exp)
max_exp=1.0e60
diode_gmin=1e-9
```

Figure 3.19 ADS Sze model parameter equations and values, linked by **model_eqn** to the SDD element in Fig. 3.18 (b).



(a) ADS SBD Cj implementation.

(b) ADS SBD Cj equations, linked to the SDD element in (a) by **C_T(C0)** and **i0**.

Figure 3.20 ADS Sze model Cj implementation, being the sub-circuit of element X5 in Fig. 3.18 (b).

3.6.4 Model comparison

To compare the equation-based and macro-based SBD models with the widely used SPICE model, an ADS HB circuit simulation is performed using an ideal single diode rectifier circuit (as discussed in Section 2.2.1) with a complex conjugately matched source, at a frequency of 1 MHz and room temperature of $T = 300$ K. The circuit load resistance value is optimized for energy transfer efficiency. This circuit's energy transfer efficiency η is shown in Fig. 3.21 as a function of input power. As the equation- and macro-based models have the same forward bias characteristic, the different efficiency behaviours can be explained from the difference in the reverse bias curves, as can be observed in Fig. 3.17 for the $T = 27\,^{\circ}$C curves. The general drop in efficiency at high drive levels for all curves is caused by the diode series resistance, which mechanism will be explained in the next chapter in more detail. The SPICE model curve shows the highest efficiency at low input power levels. This is due to the reverse bias current, clipping to the saturation current value and resulting in a higher diode junction resistance. Just below an input power level of −30 dBm, the SPICE breakdown voltage starts to kick in, resulting in a sudden rise in reverse bias current causing a drop in diode junction resistance. At an input power level of e.g. 0 dBm, the optimal load resistance for the SPICE model is ten times smaller compared to the one for the Sze model. In Chapter 5 we will look in more detail into this topic.

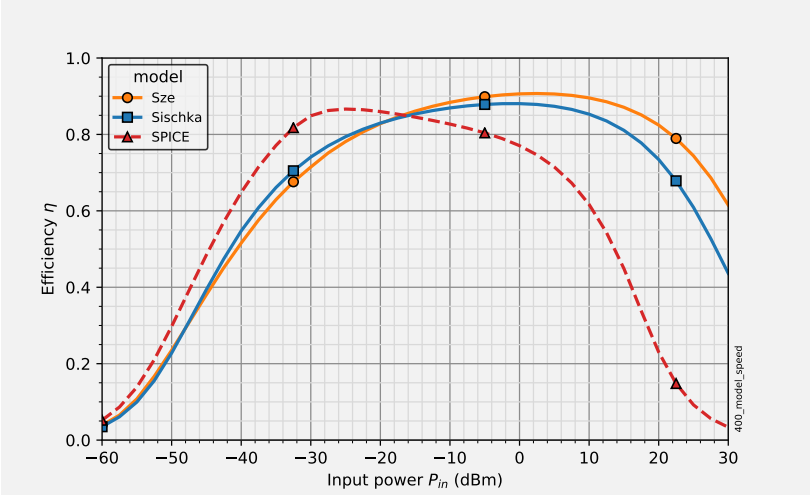


Figure 3.21 Efficiency vs. input power, optimized for maximum efficiency, for an ideal single SMS 7621 SBD rectifier circuit at $f_0 = 1$ MHz, $T = 300$ K, using the different diode models: the equation based Sze model (orange), the Sischka macro model (blue) and the SPICE model (red dashed).

Table 3.12 Single diode rectifier ADS HB simulation time, using 35 harmonics and 37 input power levels between −60 and +30 dBm.

SBD model type	simulation duration
Sze	228.5 s
Sischka	134.0 s
SPICE	157.8 s

The required simulation times are shown in Table 3.12. This shows that the macro model (Sischka) results in a simulation time duration shortening of roughly a factor of two compared to the Sze model. The SPICE model has an in-between result.

3.7 Package Model

Manufacturers typically sell the diodes packaged. As these packages introduce extra parasitic elements (e.g. bondwires for connecting the diode to the package pins introduce inductance), a model can be made for each type of package. Suppliers often provide these models, normally built with lumped components for easy insertion in simulations. Different types of packages exist. For military systems, typically high performance packages are used. They result in small parasitic elements but are relatively expensive. E.g. the old HP outline 60 and 61 package is used for the HP 5082-3140, having a series parasitic inductance of 200 pH or less, see Fig. 3.22 [101]. Consumer and commercial applications require low-cost packages, which are easy to assemble. The Joint Electron Device Engineering Council (JEDEC) standard surface mount package small outline transistor (SOT)-23 is a plastic package with tin/lead plated leads, suited for various soldering processes, and a good low-cost example [102]. A disadvantage of this SOT-23 package is the inherently long bondwire leading to a rather large inductance inside the package (1.0 nH) and the bent leads leading to additional inductance (0.5 nH each). Fig. 3.23 shows the SOT-23 package outline drawing. Fig. 3.24 shows how the parasitic inductances relate to the SOT-23 packaging, with the parasitic inductance elements L_B (bondwire related inductance) and L_L (bent leads related inductance) [103].

Fig. 3.25 shows the Avago supplied model of the diode connected into the SOT-23 plastic package [104], which is valid up to 3 GHz and can be used both for the double diode series configuration package as well as for the single diode configuration. The component values are listed in Table 3.13. The Skyworks

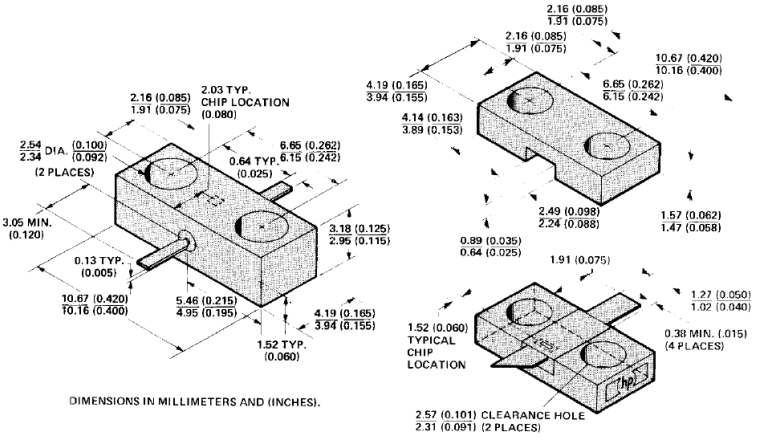


Figure 3.22 Hewlett Packard Outline 60 and 61 diode packages, used for military systems, having small parasitic values [101].

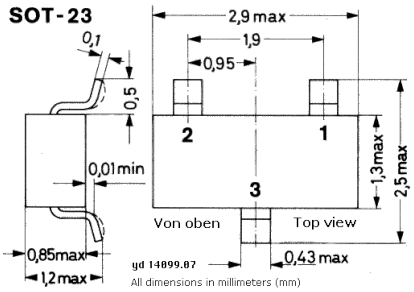


Figure 3.23 Plastic SOT-23 package outline.

SOT-23 diode package model is slightly different and is shown in Fig. 3.26 [105].

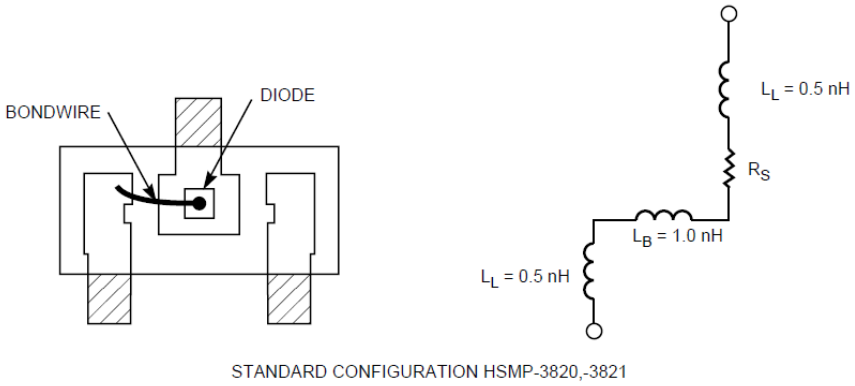


Figure 3.24 An Avago SOT-23 package construction showing the parasitic inductances of bondwire and bent leads on the left side and a corresponding first order model on the right side [103]. A second order model, including capacitances as well, will be shown below.

Table 3.13 Avago SOT-23 package model component values, corresponding to the model shown in Fig. 3.25.

Element	Description	Value	Unit
L_L	Leadframe Inductance	0.50	nH
C_L	Leadframe Capacitance	0	pF
C_P	Package Capacitance	0.080	pF
C_C	Coupling Capacitance	0.060	pF
L_B	Bondwire Inductance	1.0	nH

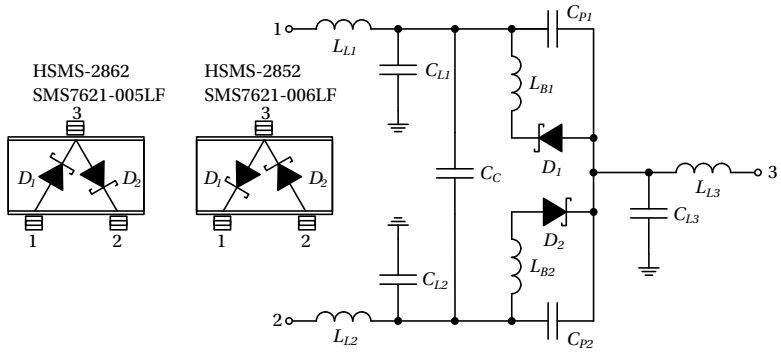


Figure 3.25 Second order model of the Avago HSMS-2852 and HSMS-2862 with leads in a SOT-23 plastic diode package, valid up to 3 GHz. A single diode version is also available, in that case only diode D_1 is mounted. The HSMS-2852 and HSMS-2862 have a different configuration as shown in the figure on the left side, the equivalent circuit model on the right side represents the HSMS-2852 version.

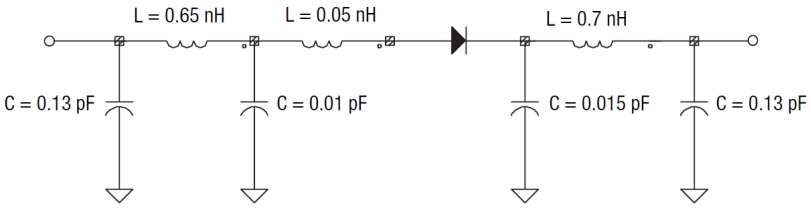


Figure 3.26 Model of the Skyworks SOT-23 packaged single diode configuration [105].

3.8 Summary

In this chapter we discussed different diode models. We showed the state-of-the-art SPICE model, that is commonly used, and we presented two other models providing a better fit to measurements: the Sischka macro model and equation based Sze model. The different model elements where treated in detail, including their temperature dependences. Together with the rectifier efficiency theory, to be covered in the next chapter, the diode model plays an important role in the correct modelling and designing of WET rectifier circuits. The conclusions are:

a) For simulation of a WET circuit, a frequency domain HB approach is preferred over a time domain approach.

b) The SPICE model yields an incorrect temperature dependency of the variables. This is most visible for the extreme temperatures. The proposed Sischka and Sze models, based on measurements, result in a proper model.

c) The reverse bias current is not modelled realistically in the SPICE model. This is a significant short coming for WET applications, as the energy transfer efficiency is affected by this. The proposed Sischka and Sze models, based on measurements, provide a proper model.

d) Manufacturer-supplied SPICE diode parameters are not necessarily correct. A dc I-V measurement provides useful insight, especially when carried out as a function of temperature. These parameters can also show significant device to device spread. The recommendation is to execute this measurement first before creating a diode model.

e) For higher diode voltages, the reverse bias breakdown effect plays a role in efficiency as well. The reverse breakdown characteristics of a real diode tend to be soft; the reverse leakage current gradually increases towards the breakdown current as the reverse-bias voltage increases. The SPICE model has a hard breakdown characteristic with parameter IS being constant up to the breakdown point. The proposed Sischka and Sze models, based on measurements, include the soft current characteristic towards the breakdown state.

f) For the circuits used in this work, it doesn't matter which diode junction capacitance model is used as the diode junction voltage typically stays below the point of divergence of the different models.

Chapter 4

Rectifier Efficiency

In this chapter we discuss the optimal energy transfer efficiency achievable with an ideal single diode rectifier circuit. Fig. 4.1 shows this circuit as defined in Chapter 2. The diode's rectifying behaviour will be analysed step-by-step together with the relationship between the circuit's load resistance R_L and the amount of energy transferred from the RF input signal to the load. Firstly, the *ideal* diode model will be analysed for its relation with respect to the rectifier efficiency. Secondly the *Schottky* diode model will be discussed with respect to efficiency.

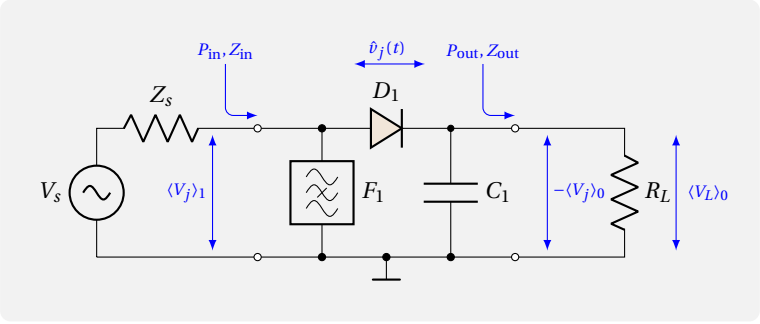


Figure 4.1 Ideal single diode rectifier configuration as defined in Chapter 2. The diode voltage is defined as $\hat{v}_j(t) = \langle V_j \rangle_1 - \langle V_L \rangle_0 = \langle V_j \rangle_1 + \langle V_j \rangle_0$.

4.1 Ideal Diode Equation

4.1.1 Natural exponential function

The diode current dependency on the diode junction voltage is typically described using the diode equation, which is based on the natural exponential function. It is useful to just look at the following two equations first:

$$f_1(x) = \mathrm{e}^x, \tag{4.1}$$

$$f_2(x) = \mathrm{e}^x - 1. \tag{4.2}$$

Both f_1 and f_2 are shown in Fig. 4.2 as a function of x. Both functions have the same derivative function $f'(x) = \mathrm{e}^x$ but the logarithmic graphs in Fig. 4.2 show a difference in slope over the first decades of x; the effect of the '-1' term in Eq. (4.2).

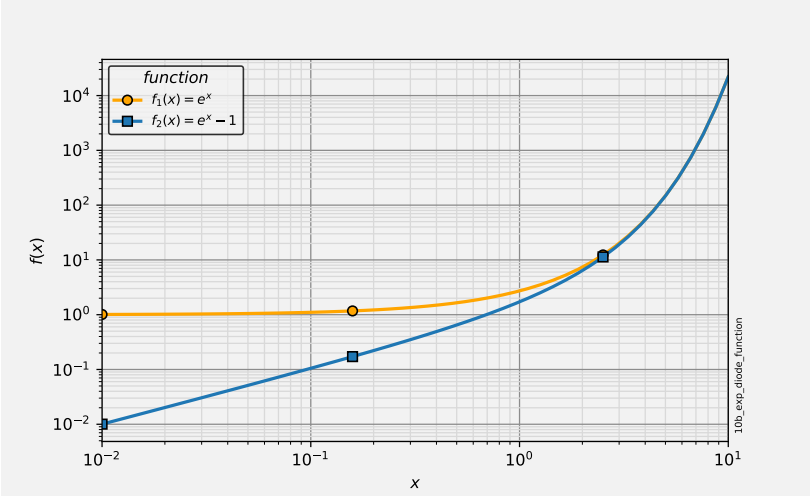


Figure 4.2 A comparison of the natural exponential function (4.1) and the basis of the diode Equation Eq. (4.2), shown in a log-log fashion.

Diode basics are often explained using graphs with linear scales (lin-lin) on both axes. Within the context of radiative WET, low power levels are typically of interest. Fig. 4.2 is used as an example to show the importance of using logarithmic (log-log) scales as they show best the low-level details. On a lin-lin scale, the difference between the two functions would be practically invisible.

The natural exponential function can be approximated, using a finite form of its Taylor series expansion (taken around $x = 0$, which is also called a Maclaurin

series). The series expansion is defined as:

$$e^x = \sum_{h=0}^{N} \frac{x^h}{h!} = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} + \cdots \quad (N \to \infty), \tag{4.3}$$

with N the number of terms used for the approximation and harmonic index h. For the diode equation, based on the function $f_2(x)$ from Equation (4.2), the approximation can be simplified for small x values to

$$\lim_{x \to 0} f_2(x) = x, \tag{4.4}$$

and for large negative values of x

$$\lim_{x \to -\infty} f_2(x) = -1. \tag{4.5}$$

The first limit shows that for small values, the exponential diode equation becomes linear. This will be shown in more detail later in this chapter. The second limit shows that for large negative values, the exponential function saturates to a fixed negative value. This corresponds to a fixed reverse biased diode current value as we will see later in this chapter.

The Taylor series expansion will be used in the next section to study the behaviour of a diode rectifier in more detail. It eases the separation of the dc and RF terms of the voltages and currents, which is useful as a rectifier acts as an RF to dc converter.

4.1.2 Harmonic approximation

To separate the diode equation in its dc and RF terms, the ideal diode equation (3.1) is rewritten in a harmonic term form. First the equation is rewritten as

$$I_j = I_s \left(e^{\frac{V_j}{nV_T}} - 1 \right) = I_s \left(e^x - 1 \right), \tag{4.6}$$

with x being the junction voltage divided by nV_T. In this chapter we make use of the ideal rectifier discussed in Chapter 2. This rectifier has a sinusoidal input signal at frequency f_0. When applied to Eq. (4.6) we get

$$I_j = I_s \left(e^x - 1 \right) = I_s \left(e^{\Lambda_1 \cos(\omega_0 t) + \Lambda_0} - 1 \right), \tag{4.7}$$

with the fundamental frequency amplitude term

$$\Lambda_1 = \frac{|\langle V_j \rangle_1|}{nV_T}, \tag{4.8}$$

and the dc-offset term Λ_0, being related to the dc-offset V_L (across the load resistance R_L), as

$$\Lambda_0 = \frac{\langle V_j \rangle_0}{nV_T} = -\frac{\langle V_L \rangle_0}{nV_T}. \tag{4.9}$$

Using $e^{(a+b)} = e^a e^b$ Eq. (4.7) can be rewritten into

$$I_j = I_s \left(e^{\Lambda_1 \cos(\omega_0 t)} e^{\Lambda_0} - 1 \right). \tag{4.10}$$

For the Taylor expansion x^h-terms we fill in the input signal from Eq. (4.10):

$$x^h = (\Lambda_1 \cos(\omega_0 t))^h. \tag{4.11}$$

The next step is to rewrite Eq. (4.10) using the Taylor expansion of e^x, Eq. (4.3):

$$I_j = I_s \left(\sum_{h=0}^{N} \left[\frac{(\Lambda_1 \cos(\omega_0 t))^h}{h!} \right] e^{\Lambda_0} - 1 \right). \tag{4.12}$$

To expand this equation into harmonic terms, we make use of the binomial coefficient being defined as

$$\binom{h}{i} = \frac{h!}{i!(h-i)!}, \tag{4.13}$$

and the following series expansion

$$\cos^h x = \begin{cases} \frac{2}{2^h} \sum_{i=0}^{\frac{h-1}{2}} \binom{h}{i} \cos((h-2i)x), & \text{for } h \in \{1,3,5,\cdots\}, \\ \\ \frac{1}{2^h} \binom{h}{\frac{h}{2}} + \frac{2}{2^h} \sum_{i=0}^{\frac{h}{2}-1} \binom{h}{i} \cos((h-2i)x), & \text{for } h \in \{0,2,4,\cdots\}. \end{cases} \tag{4.14}$$

From this, the diode junction current approximation can be written in its harmonic terms h. First the dc-term can be written as[1]:

$$I_{j,\mathrm{dc}} = I_s \left\{ \sum_{i=0}^{N} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} e^{\Lambda_0} {\Lambda_1}^{h_0} - 1 \right\}, \quad \text{with } (h_0 = 2i, N \to \infty), \tag{4.15}$$

in which i is the index of approximation for the dc-term and h_0 the dc harmonic index $h_0 = \{0,2,4,\cdots\}$.

[1] This dc-term equation is referred to as the $h = 0$ term. This is not the same as the $h = 0$ term in Eq. (4.12), as all the even h-terms in Eq. (4.12) result in harmonics which include a dc-term: the $\frac{1}{2^h}\binom{h}{\frac{h}{2}}$ part of the lower term in Eq. (4.14)

The odd harmonic terms result samewise in:

$$I_{j,\text{odd}} = I_s \sum_{h=1}^{k} \left\{ \sum_{i=0}^{N} \frac{1}{h_1!} \frac{2}{2^{h_1}} \binom{h_1}{i} e^{\Lambda_0} {\Lambda_1}^{h_1} \cos((2h-1)\omega_0 t) \right\}, \quad (4.16)$$
$$\text{with } (h_1 = 2i + 2h - 1, N \to \infty),$$

in which i is the index of approximation for the odd harmonic terms and h_1 the odd harmonic index.

The even harmonic terms results in the following equation:

$$I_{j,\text{even}} = I_s \sum_{h=1}^{k} \left\{ \sum_{i=0}^{N} \frac{1}{h_2!} \frac{2}{2^{h_2}} \binom{h_2}{i} e^{\Lambda_0} {\Lambda_1}^{h_2} \cos((2h)\omega_0 t) \right\}, \quad (4.17)$$
$$\text{with } (h_2 = 2i + 2h, N \to \infty),$$

in which i is the index of approximation for the even harmonic terms and h_2 the even harmonic index.

Combined diode junction current approximation

The dc-, odd- and even-terms from Eqs (4.15), (4.16) and (4.17) can now be combined into a single equation as

$$\begin{aligned} I_j = I_s &\left\{ \sum_{i=0}^{N} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} e^{\Lambda_0} {\Lambda_1}^{h_0} - 1 \right\} \\ &+ I_s \sum_{h=1}^{k} \left\{ \sum_{i=0}^{N} \frac{1}{h_1!} \frac{2}{2^{h_1}} \binom{h_1}{i} e^{\Lambda_0} {\Lambda_1}^{h_1} \cos((2h-1)\omega_0 t) \right. \\ &\left. + \sum_{i=0}^{N} \frac{1}{h_2!} \frac{2}{2^{h_2}} \binom{h_2}{i} e^{\Lambda_0} {\Lambda_1}^{h_2} \cos((2h)\omega_0 t) \right\}, \\ &\text{with } (h_0 = 2i,\ h_1 = 2i + 2h - 1,\ h_2 = 2i + 2h, N \to \infty), \end{aligned} \quad (4.18)$$

in which the first i-summation term, on the right hand side, represents the dc-component, the $h = 0$ term. The second i-summation term accounts for the odd- and the third one for the even harmonics. h_0, h_1 and h_2 are the harmonic indices for the dc-, odd- and even harmonics, k is the maximum number of fundamental frequency harmonics taken into account and i is the index of approximation for each harmonic. N is the maximum number of summation iterations used for each harmonic term.

Taking the dc-term e^{Λ_0} out of the equation, the harmonic term multiplication factors of Eq. 4.18 are shown in Table 4.1. The diode dc current flowing

Table 4.1 Diode junction current approximation i-summation values (without the e^{Λ_0} and $\cos(\omega_0 t)$ terms), used in Eq. (4.18).

	i					
h	0	1	2	3	4	$\cdots$
0	1	$\frac{{\Lambda_1}^2}{4}$	$\frac{{\Lambda_1}^4}{64}$	$\frac{{\Lambda_1}^6}{2304}$	$\frac{{\Lambda_1}^8}{147456}$	$\cdots$
1	Λ_1	$\frac{{\Lambda_1}^3}{8}$	$\frac{{\Lambda_1}^5}{192}$	$\frac{{\Lambda_1}^7}{9216}$	$\frac{{\Lambda_1}^9}{737280}$	$\cdots$
2	$\frac{{\Lambda_1}^2}{4}$	$\frac{{\Lambda_1}^4}{48}$	$\frac{{\Lambda_1}^6}{1536}$	$\frac{{\Lambda_1}^8}{92160}$	$\frac{{\Lambda_1}^{10}}{8847360}$	$\cdots$
3	$\frac{{\Lambda_1}^3}{24}$	$\frac{{\Lambda_1}^5}{384}$	$\frac{{\Lambda_1}^7}{15360}$	$\frac{{\Lambda_1}^9}{1105920}$	$\frac{{\Lambda_1}^{11}}{123863040}$	$\cdots$
4	$\frac{{\Lambda_1}^4}{192}$	$\frac{{\Lambda_1}^6}{3840}$	$\frac{{\Lambda_1}^8}{184320}$	$\frac{{\Lambda_1}^{10}}{15482880}$	$\frac{{\Lambda_1}^{12}}{1981808640}$	$\cdots$
5	$\frac{{\Lambda_1}^5}{1920}$	$\frac{{\Lambda_1}^7}{46080}$	$\frac{{\Lambda_1}^9}{2580480}$	$\frac{{\Lambda_1}^{11}}{247726080}$	$\frac{{\Lambda_1}^{13}}{35672555520}$	$\cdots$
6	$\frac{{\Lambda_1}^6}{23040}$	$\frac{{\Lambda_1}^8}{645120}$	$\frac{{\Lambda_1}^{10}}{41287680}$	$\frac{{\Lambda_1}^{12}}{4459069440}$	$\frac{{\Lambda_1}^{14}}{713451110400}$	$\cdots$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\ddots$

through the load resistor will result in a positive voltage across the resistor and therefore between the diode's cathode and ground. For the diode's junction voltage, this is equal to a negative offset voltage $\langle V_j \rangle_0$ as the junction voltage is defined between the anode and cathode, and the anode is grounded for dc in the ideal single diode rectifier circuit.

Combining the dc-term Eq. (4.15) with Eq. (4.9), the current through the load resistor gets:

$$I_s \left\{ \sum_{i=0}^{N} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} e^{\Lambda_0} {\Lambda_1}^{h_0} - 1 \right\} = -\Lambda_0 \frac{nV_T}{R_L} = -\Lambda_0 \frac{I_s}{\Lambda_L} \qquad (4.19)$$
$$\text{with } (h_0 = 2i, N \to \infty),$$

with R_L being the load resistance and introducing the diode dc-offset calculation term

$$\Lambda_L = \frac{I_s R_L}{nV_T}. \qquad (4.20)$$

Using

$$\sum_{i=0}^{N} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} e^{\Lambda_0} {\Lambda_1}^{h_0} = e^{\Lambda_0} \sum_{i=0}^{N} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} {\Lambda_1}^{h_0}, \qquad (4.21)$$

and $e^a / e^b = e^{a-b}$ Eq. (4.19) can be re-written as:

$$(\Lambda_L - \Lambda_0)e^{\Lambda_L - \Lambda_0} = e^{\Lambda_L}\Lambda_L \sum_{i=0}^{N} \frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}{\Lambda_1}^{h_0}, \tag{4.22}$$

from which Λ_0 can be extracted using the principal branch of the Lambert W function, W_0 [76]:

$$\Lambda_0 = \Lambda_L - W_0\left(e^{\Lambda_L}\Lambda_L \sum_{i=0}^{N} \frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}{\Lambda_1}^{h_0}\right), \tag{4.23}$$
$$\text{with } (h_0 = 2i, N \to \infty).$$

Fig. 4.3 relates the rectified dc voltage $\langle V_L \rangle_0$ against diode junction voltage $\langle V_j \rangle_1$ for different harmonic approximation values k, defined as

$$\begin{aligned}\langle V_L \rangle_0 &= -\Lambda_0 n V_T \\ &= -\left\{\Lambda_L - W_0\left(e^{\Lambda_L}\Lambda_L \sum_{i=0}^{k} \frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}\left(\frac{\langle V_j \rangle_1}{nV_T}\right)^{h_0}\right)\right\} nV_T, \\ &\text{with } (h_0 = 2i),\end{aligned} \tag{4.24}$$

and compares it with an ADS simulation result, based on an HB simulation with $k = 65$ harmonics. From this graph it is clear that with larger signal levels ($\langle V_j \rangle_1 > 100$ mV), more harmonics are required (larger value for k). For the ideal single diode rectifier, the combined dc- and first harmonic term diode junction voltage can be described as

$$\hat{v}_j(t) = \langle V_j \rangle_1 - \langle V_L \rangle_0 = \langle V_j \rangle_1 + \langle V_j \rangle_0. \tag{4.25}$$

Combining Equations (4.18) and (4.23), the harmonic terms can be calculated against the diode junction voltage $\langle V_j \rangle_1$ for the first fews harmonic terms, as shown in Fig. 4.4. This shows the rate at which the different harmonic terms increase, with increasing fundamental diode junction voltage level $\langle V_j \rangle_1$. Both the dc- and second harmonic terms follow a two decades increase per decade of voltage rise, where the fundamental current increases only at 1 decade per decade. The third harmonic rises three times as fast as the fundamental and the fourth harmonic four times as fast. The bend in the $h = 0$ curve is caused by the exponential diode equation. In this ideal single diode rectifier, the harmonic terms for $h > 1$ do not dissipate energy and reach the same level as for the $h = 1$ term, for the high $\langle V_j \rangle_1$ levels.

At this stage it is good to realize that the single diode rectifier circuit can be seen as an RF input voltage to dc output current converter, which incorporates a feedback mechanism. The feedback is provided by the induced voltage across

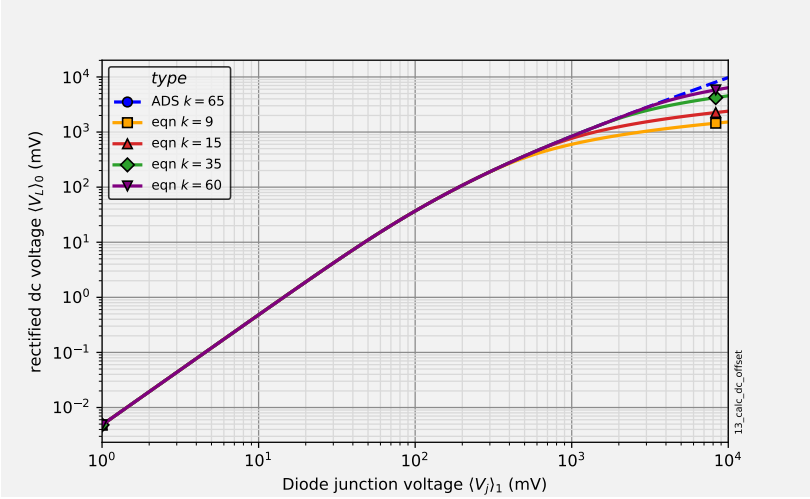


Figure 4.3 Simulated and calculated rectified dc voltage $\langle V_L \rangle_0$ versus diode junction voltage $\langle V_j \rangle_1$. Comparison of an ADS HB simulation (using $k = 65$, dashed) with eq. (4.24) for different values of k for an ideal single diode rectifier with $I_s = 3\,\mu$A and a load resistor of 8.6174 kΩ, at $T = 300$ K. The combined diode junction voltage equals $\hat{v}_j(t) = \langle V_j \rangle_1 - \langle V_L \rangle_0$.

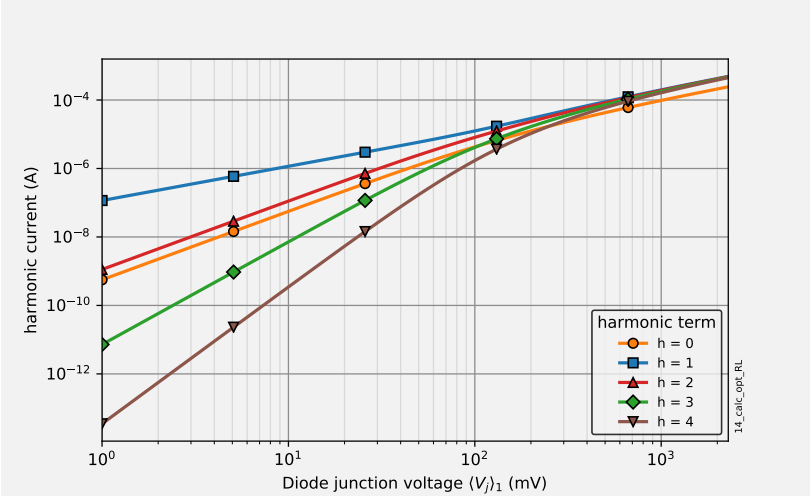


Figure 4.4 Calculated harmonic term current versus diode junction voltage $\langle V_j \rangle_1$, using $I_s = 3\,\mu$A and $R_L = 8.6174$ kΩ, at $T = 300$ K.

the load resistor, acting as a negative offset voltage on the RF input voltage across the diode junction. This results in a smaller dc current at the output, decreasing the negative offset voltage — finally finding an equilibrium, expressed in Equation (4.24).

4.2 Load Experiment

To get insight into the dependency of the diode junction resistance on a varying rectifier input power level for different rectifier load resistances, a series of different diode saturation current and load resistance combinations is analysed. The cases for this load experiment are listed in Table 4.2, in which different diodes are used. They are labelled D_A, D_B and D_C – having a corresponding saturation current I_s of 0.040 μA, 0.40 μA and 3.0 μA respectively. This way they cover the range of diodes from the Skyworks SMS7621 to the Avago HSMS-285x. The circuit diagram, as shown in Fig. 4.5, is simulated in ADS. The source voltage V_s is swept from 1 mV to 250 V[2]. The cases are subdivided based on the load resistance value being used. The naming of these sub-categories is explained after the next three equations.

The diode's conductance, corresponds to the derivative of the diode equation (3.1):

$$g_j = \frac{\partial I_j}{\partial V_j} = \frac{I_s}{nV_T} \mathrm{e}^{\frac{V_j}{nV_T}}, \tag{4.26}$$

From this equation we see that

$$\lim_{V_j \to 0} g_j = \frac{I_s}{nV_T}, \tag{4.27}$$

showing a junction resistance, which is only dependent on the diode parameters n, V_T and I_s with

$$\lim_{V_j \to 0} R_j = \frac{nV_T}{I_s}. \tag{4.28}$$

The fixed load resistance R_L is chosen to be either equal to this small signal junction resistance value ($R_{L,A}$ for diode A, $R_{L,B}$ for diode B and $R_{L,C}$ for diode C), twice this value ($2R_{L,A}$ for diode A, etc.) or equal to this resistance corresponding to one of the other two diodes ($\{R_{L,A}, R_{L,B}, R_{L,C}\}$).

[2] As the relatively high circuit input impedance is not transformed to e.g. 50 Ω, a high source voltage amplitude is required to obtain the indicated input power levels. Due to the missing input impedance matching circuit, part of the source energy is reflected, requiring even more source amplitude.

Table 4.2 Load experiment cases using different I_s and R_L values.

diode	D_A				D_B				D_C			
I_s (μA)	0.040				0.40				3.0			
R_L[a]	A	$2A$	B	C	B	$2B$	A	C	C	$2C$	A	B
case	1	2	3	4	5	6	7	8	9	10	11	12

[a] R_L: $A = 646.30$ kΩ, $B = 64.631$ kΩ, $C = 8.6174$ kΩ.

At large input voltage levels, the dc-voltage across the load resistance equals the peak input voltage, which has a sinusoidal shape[3]. Therefore the junction resistance value should be half the load resistance value, in order to have equal in- and output power for the lossless case. Using the circuit simulator ADS, this ratio of two was verified to be correct (and it is reached only at a very high input voltage in the order of 1000 V). This also corresponds to the ratio of $\langle I_j \rangle_1$ and $\langle I_j \rangle_0$, shown in Fig. 4.4 on the high input voltage side, being equal to 2 : 1.

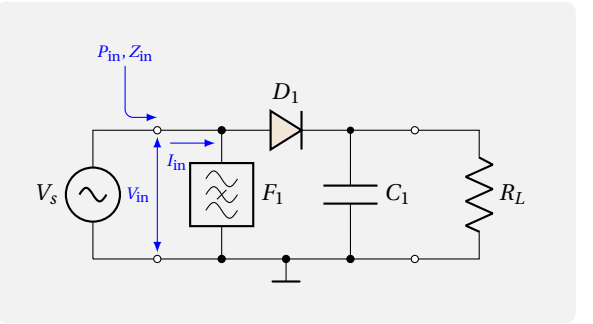


Figure 4.5 Ideal single diode rectifier configuration as described in section 2.2.1, used for the load resistance effect investigation. The bandstop filter F_1 is tuned at the circuits operating frequency f_0. The diode has $n = 1.00$, $R_s = 0\ \Omega$, $C_{j0} = 0$ pF and the simulation uses $f_0 = 6.78$ MHz and $T = 300$ K. The circuit input power is calculated as $P_{in} = 0.5\,\mathrm{Re}(\langle V_{in} \rangle_1 \langle I_{in} \rangle_1^*)$. Due to the ideal diode and circuit, the junction resistance equals $R_j = \mathrm{Re}(\langle Z_{in} \rangle_1)$. The source voltage is swept from 1 mV to 250 V.

The analysis result is shown in Fig. 4.6 and shows the following important aspects of an ideal single *pn*-junction diode rectifier:

1. For low signal levels, $\langle V_j \rangle_1 < 10$ mV, $R_j = nV_T/I_s$ applies, with R_j being

[3] This is in fact the envelope detection function, this circuit has served for decades. For low input voltage levels, the dc output voltage is not reaching the peak level due to losses and the reverse bias current being more dominant.

independent of R_L.

2. For large signal levels, $P_{\text{in}} > 10$ dBm, $R_j = R_L/2$ applies, independent of the diode parameters.

3. R_j can be controlled against input power by choosing both I_s (the diode) and R_L correctly.

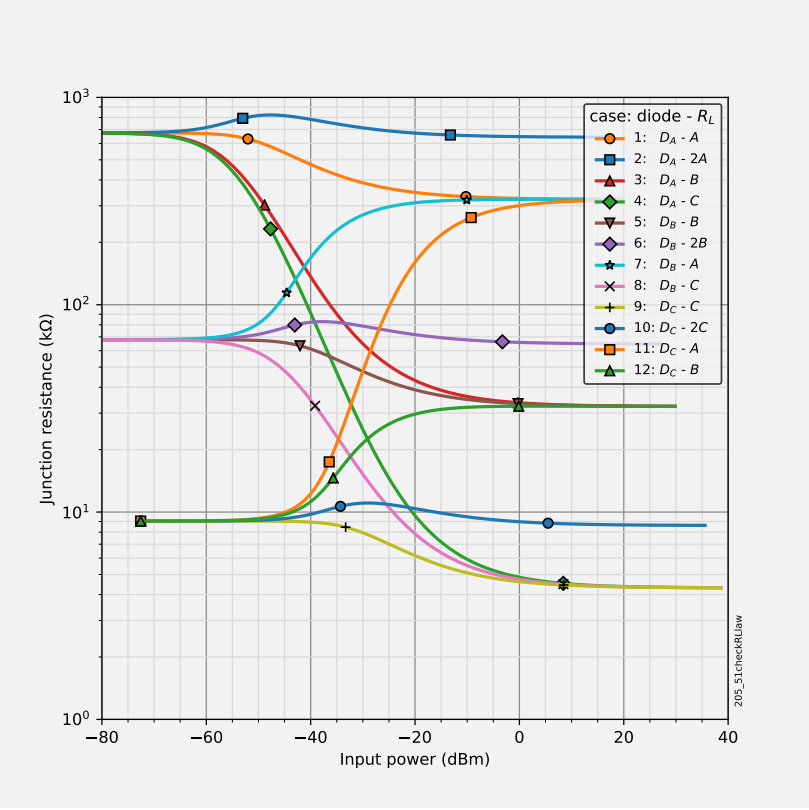


Figure 4.6 Simulated diode junction resistance R_j versus RF input power P_{in} for various load experiment cases, for an ideal single diode rectifier having $n = 1$, $R_s = 0\ \Omega$, $C_{j0} = 0$ pF, $f_0 = 6.78$ MHz and $T = 300$ K. Two regimes are visible: for $\langle V_j \rangle_1 < 10$ mV: $R_j = \frac{nV_T}{I_s}$ (the boundary becomes visible when plotting R_j against $\langle V_j \rangle_1$) and for $P_{\text{in}} > 10$ dBm: $R_j = \frac{R_L}{2}$. See Table 4.2 for the case parameter values.

Load resistance sensitivity

In Section 2.3.1 we discussed the efficiency optimization topic and concluded that a complex conjugately matched source is required. In this section we make

use of the previous load experiment to add a different view on the topic of efficiency optimization. We take the same rectifier circuit cases from Table 4.2, to illustrate the need for an adaptive source.

The normalized input power P_{in} sensitivity- and energy transfer efficiency η sensitivity to the load resistance R_L are defined as

$$S_{R_L}^{P_{\text{in}}} = \frac{\partial P_{\text{in}}}{\partial R_L} \frac{R_L}{P_{\text{in}}}, \tag{4.29}$$

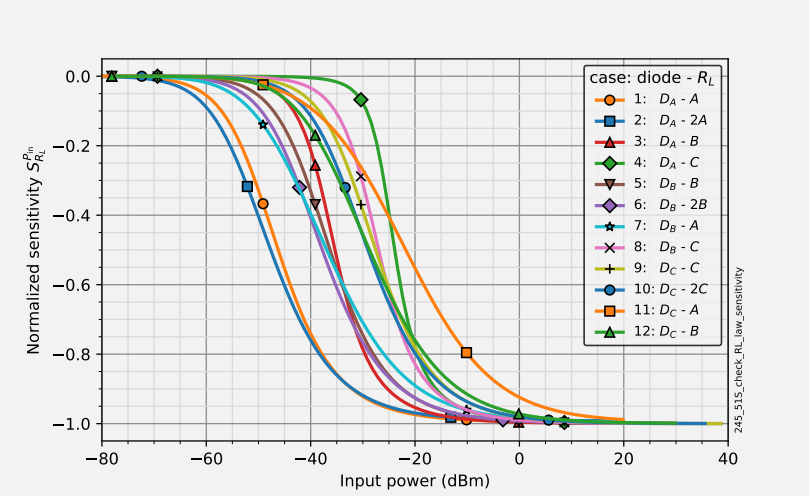
and

$$S_{R_L}^{\eta} = \frac{\partial \eta}{\partial R_L} \frac{R_L}{\eta}. \tag{4.30}$$

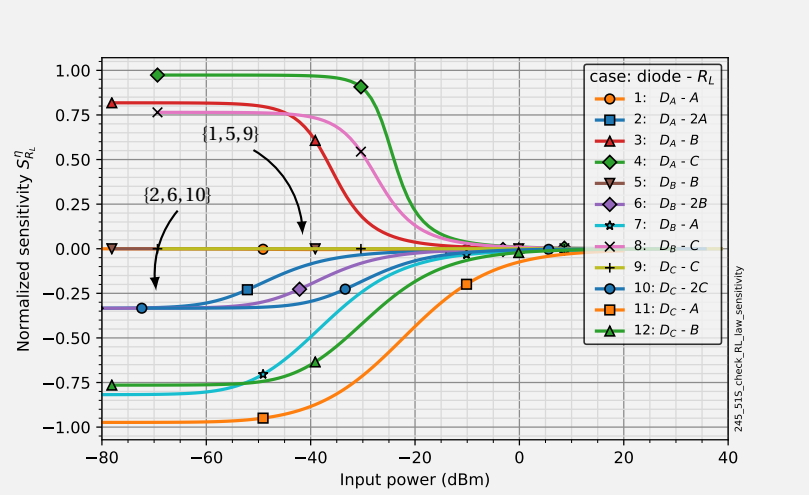
Simulating these, using an ADS HB Sensitivity[4] simulation on the same circuit diagram as used in the previous load experiment, provides the result as shown in Fig. 4.7. This shows that the input power, entering the rectifier, is affected significantly by a load resistance change, for the larger input levels where the effect on efficiency is more pronounced for the small signal range. From Eq. (4.28) follows that the junction resistance is not dependent on the rectifier load resistance for small signals, therefore we see $S_{R_L}^{P_{\text{in}}}$ at low input power values being small.

From this we can conclude that an adaptive source is particularly of value for the large signal range and will show no significant sensitivity $S_{R_L}^{P_{\text{in}}}$ as the source keeps P_{in} constant. Note in the $S_{R_L}^{\eta}$ figure (b) the cluster of case $\{1,5,9\}$ cases showing no sensitivity over the whole junction voltage range and the $\{2,6,10\}$ cluster with a minimal sensitivity.

[4] A dedicated ADS analysis component, based on finite difference approximation (taking partial derivatives) requiring $N+1$ circuit simulations, where N is the number of optimization variables. The normalized sensitivities use the approximate gradient (single-point sensitivity) to predict the percentage change in the response due to a 1 % change in the design variable.



(a) Normalized sensitivity $S_{R_L}^{P_{\text{in}}}$.



(b) Normalized sensitivity $S_{R_L}^{\eta}$

Figure 4.7 Simulated rectifier normalized sensitivity of (a) P_{in} to R_L and (b) efficiency η to P_{in} for various load experiment cases (see Table 4.2), for an ideal single diode rectifier having $n = 1.00$, $R_s = 0\ \Omega$, $C_{j0} = 0$ pF, $f_0 = 6.78$ MHz and $T = 300$ K. The arrows mark the case= $\{1,5,9\}$ and $\{2,6,10\}$ clusters of three cases each.

4.3 Small Signal Approximation

In analysing rectifier circuits, we can define the special *small signal* case. In this case the diode junction voltage amplitude has a value below a specific level, which is defined as $\langle V_j \rangle_1 < V_T = \frac{kT}{q}$ being the thermal voltage[5].

4.3.1 Small signal load voltage

In this section, we will have a closer look at the small signal load voltage. It is not straightforward to provide the equation for the load voltage, based on the diode equation (3.1), for the complete input power range. This is why we make use of the Lamber-W function, see Eq. (4.23).

In the small signal regime, $\langle V_L \rangle_0$ can be approximated. For small $\langle V_j \rangle_1$ values we see that

$$\sum_{i=0}^{\infty} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} {\Lambda_1}^{h_0} \approx 1 + \frac{{\Lambda_1}^2}{4}, \tag{4.31}$$

which is Eq. (4.15) diode current dc-term multiplication factor — see table 4.1 ($h = 0$). We found that for the small signal regime, the *optimal* load resistance equals the junction resistance: $\lim_{V_j \to 0} R_L = \lim_{V_j \to 0} R_j = nV_T / I_s$. This makes $\Lambda_L = I_s R_L / nV_T = 1$, therefore $\mathrm{e}^{\Lambda_L} \Lambda_L = \mathrm{e}$, and $W_0(z)$ has its lowest value. Analysing the Eq. (4.23) W_0 function for these small $\langle V_j \rangle_1$ values shows:

$$W_0 \left\{ \mathrm{e} \cdot \left(1 + \frac{{\Lambda_1}^2}{4} \right) \right\} \approx 1 + \frac{{\Lambda_1}^2}{8}. \tag{4.32}$$

Therefore Eq. (4.23) results in

$$\Lambda_0 \approx -\frac{{\Lambda_1}^2}{8} = -\frac{\langle V_j \rangle_1^2}{8(nV_T)^2}, \tag{4.33}$$

with Eq. (4.9) leading to

$$\langle V_L \rangle_0 \approx \frac{\langle V_j \rangle_1^2}{8nV_T}. \tag{4.34}$$

Having $R_j = nV_T / I_s$ in this regime gives for the circuit input power P_{in}:

$$P_{\mathrm{in}} = \frac{\langle V_j \rangle_1^2 I_s}{2nV_T}. \tag{4.35}$$

This leads to

$$\langle V_L \rangle_0 \approx \frac{P_{\mathrm{in}}}{4I_s}. \tag{4.36}$$

[5] At a temperature of 300 K, $\frac{kT}{q} = 25.85$ mV.

From these equations we see that the rectifier load voltage is independent from I_s in the small signal regime as a function of V_{in}[6]. Against the input power level P_{in} the load voltage is dependent on I_s in this regime, where we see that a lower I_s will result in a higher load voltage. Fig. 4.8 shows the calculated load voltage and the simulated voltage versus diode junction voltage. The calculated small signal load voltage is within 10 % of the simulated load voltage even up to a junction voltage of 100 mV at $T = 300$ K.

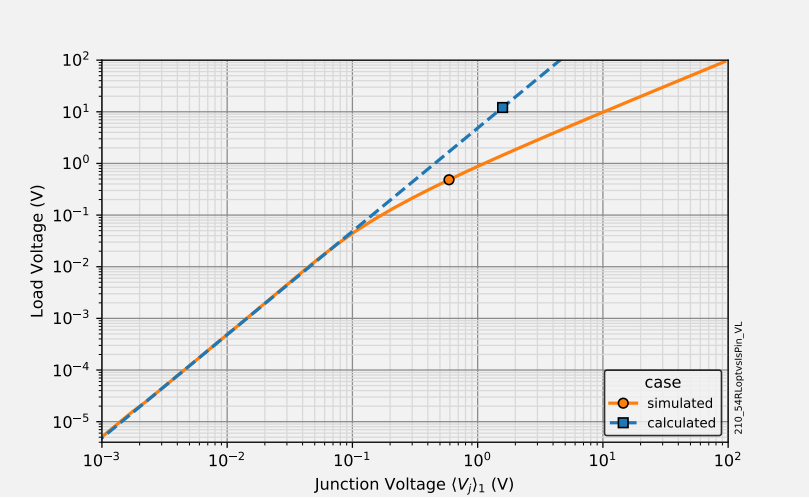


Figure 4.8 Simulated load voltage V_L at optimal efficiency against junction voltage $\langle V_j \rangle_1$, of an ideal single diode rectifier at a temperature of $T = 300$ K, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$) and $n = 1$. Also drawn is the calculated V_L from Eq. (4.34) which shows that both curves differ less than 10 % up to a junction voltage $\langle V_j \rangle_1 = 100$ mV.

4.3.2 Small signal efficiency

In this section we will derive an equation for the rectifier energy transfer efficiency in the small input signal regime. The rectifier load power is calculated using eq. (4.24) as:

$$P_{\text{out}} = \frac{(-\Lambda_0 n V_T)^2}{R_L} = \frac{\left(\left(\Lambda_L - W_0\left\{e^{\Lambda_L}\Lambda_L \sum_{i=0}^{\infty} \frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}\Lambda_1{}^{h_0}\right\}\right) n V_T\right)^2}{R_L}. \quad (4.37)$$

In the previous section, we have seen that the diode junction resistance R_j is constant in the small signal regime, from which the input power Eq. (4.35) results, where P_{in} is independent on R_L. To find the load resistance for optimal

[6] For the ideal single diode rectifier, $\langle V_{\text{in}} \rangle_1 = \langle V_{\text{j}} \rangle_1$ due to the ideal load capacitor.

efficiency, it is therefore sufficient to find the zero crossing of the derivative of the output power eq. (4.37) to R_L: $\frac{dP_{\text{out}}}{dR_L}$. To get this derivative we start with the derivative of the dc-offset term Λ_L, using Eq. (4.20):

$$\frac{d\Lambda_L}{dR_L} = \frac{I_s}{nV_T}. \tag{4.38}$$

Then we use the help variable z defined as

$$z = \mathrm{e}^{\Lambda_L}\Lambda_L \sum_{i=0}^{\infty} \frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}{\Lambda_1}^{h_0} \approx \mathrm{e}^{\Lambda_L}\Lambda_L\left(1+\frac{{\Lambda_1}^2}{4}\right), \tag{4.39}$$

and

$$\frac{dz}{dR_L} = \frac{I_s}{nV_T}\mathrm{e}^{\Lambda_L}(\Lambda_L+1)\left(1+\frac{{\Lambda_1}^2}{4}\right). \tag{4.40}$$

The derivative of the Lambert W function is known as [76]:

$$\frac{dW_0(z)}{dz} = \frac{1}{z+\mathrm{e}^{W_0(z)}} = \frac{W_0(z)}{z(1+W_0(z))}. \tag{4.41}$$

Using

$$\frac{dW_0(z)}{dR_L} = \frac{dW_0(z)}{dz}\frac{dz}{dR_L}, \tag{4.42}$$

we can now write

$$\frac{dP_{\text{out}}}{dR_L} = \frac{\Lambda_L - W_0(z) - \frac{2I_s}{nV_T}\left\{1-\frac{W_0(z)}{z(1+W_0(z))}\mathrm{e}^{\Lambda_L}(\Lambda_L+1)\left(1+\frac{{\Lambda_1}^2}{4}\right)\right\}}{R_L^2}(nV_T)^2. \tag{4.43}$$

Plotting the numerator of Eq. (4.43) shows that, in the low $\langle V_j\rangle_1$ regime, the load resistance for optimal efficiency is $R_L = nV_T/I_s$, equal to the junction resistance, as also derived in Eq. (4.28). This might seem logical due to its similarity to the maximum power transfer theorem. This theorem states that, to obtain maximum external power from a source with a fine internal resistance, the resistance of the load must equal the resistance of the source. In this case R_j is defined at the fundamental frequency and can be seen as an analogy to the theorem's source resistance, R_L is defined at dc and acts as the load.

Combing Eq. (4.33) with Eq. (4.37) leads to

$$P_{\text{out}} \approx \left(\frac{\langle V_j\rangle_1^2 nV_T}{8(nV_T)^2}\right)^2 \frac{1}{R_L}. \tag{4.44}$$

Using $R_j = R_L = nV_T/I_s$, the obtained small signal optimal efficiency η_{opt} can be written, using Eqs (2.21) and (4.35), as

$$\eta_{\text{opt}} = \frac{P_{\text{out}}}{P_{\text{in}}} \approx 2\left(\frac{\langle V_j\rangle_1}{8nV_T}\right)^2 = \frac{P_{\text{in}}}{16nV_T I_s}. \tag{4.45}$$

This shows that $\eta_{\text{opt}}(V_j)$ is in the small signal $\langle V_j\rangle_1$ regime not dependent on I_s, when using the optimal load resistance $R_L = nV_T/I_s$ (which *is* dependent on I_s). Contrary $\eta_{\text{opt}}(P_{\text{in}})$ linearly depends on P_{in} but is inversely proportional to I_s.

Looking at Eq. (4.45), $\eta_{\text{opt}} = \frac{P_{\text{in}}}{16nV_T I_s}$, lowering the temperature will on one hand increase the efficiency linearly with temperature at a fixed input power level, due to the V_T term. On the other hand, the temperature dependency of I_s will result in a non-linear dependency of efficiency on temperature at a fixed input power level, see Eq. (3.5) for the SBD and Eq. (3.7) for the *pn*-junction diode. These characteristics will be shown graphically in the next section.

4.4 Large Signal Approximation

4.4.1 Large signal efficiency

To express the rectifier efficiency over the *complete* range of input signals we can not make use of the approximations used in the previous section. For the output power, Eq. (4.37) is still valid. For the input power, using Eq. (2.20), we get

$$P_{\text{in}} = \frac{V_j^2}{2R_j} = \frac{\langle V_j\rangle_1^2\langle I_j\rangle_1}{2\langle V_j\rangle_1}. \tag{4.46}$$

Using Section 2.2.1, $\langle V_{D1}\rangle_1 = \langle V_j\rangle_1$. From Eq. (4.18) we use ($h = 1$):

$$\langle I_j\rangle_1 = I_s \sum_{i=0}^{\infty} \frac{1}{h_1!}\frac{2}{2^{h_1}}\binom{h_1}{i} e^{\Lambda_0}{\Lambda_1}^{h_1}, \tag{4.47}$$

with $h_1 = 2i+1$. The efficiency is expressed as

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{2\left(\left(\Lambda_L - W_0\left\{e^{\Lambda_L}\Lambda_L \sum_{i=0}^{\infty}\frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}{\Lambda_1}^{h_0}\right\}\right)nV_T\right)^2}{R_L\langle V_j\rangle_1 I_s \sum_{i=0}^{\infty}\frac{1}{h_1!}\frac{2}{2^{h_1}}\binom{h_1}{i}e^{\Lambda_0}{\Lambda_1}^{h_1}}, \tag{4.48}$$

with $\Lambda_0 = \Lambda_L - W_0\left(e^{\Lambda_L}\Lambda_L\sum_{i=0}^{\infty}\frac{1}{h_0!}\frac{1}{2^{h_0}}\binom{h_0}{\frac{h_0}{2}}{\Lambda_1}^{h_0}\right)$, $\Lambda_L = \frac{I_s R_L}{nV_T}$, $\Lambda_1 = \frac{V_j}{nV_T}$. Note that this is not the equation for *optimal* efficiency like Eq. (4.45), the efficiency is still dependent on R_L.

This total equation for efficiency is too complex for finding the derivative with respect to R_L. Having the ability to use a circuit simulator, like ADS, for this purpose (deploying the method of Section 2.3.1), the R_L values for optimal efficiency can be found against a range of input signal levels at a specific temperature. Fig. 4.9 shows the result, when using an ideal single diode rectifier as discussed in Section 2.2.1 and an ideal SPICE *pn*-junction diode model.

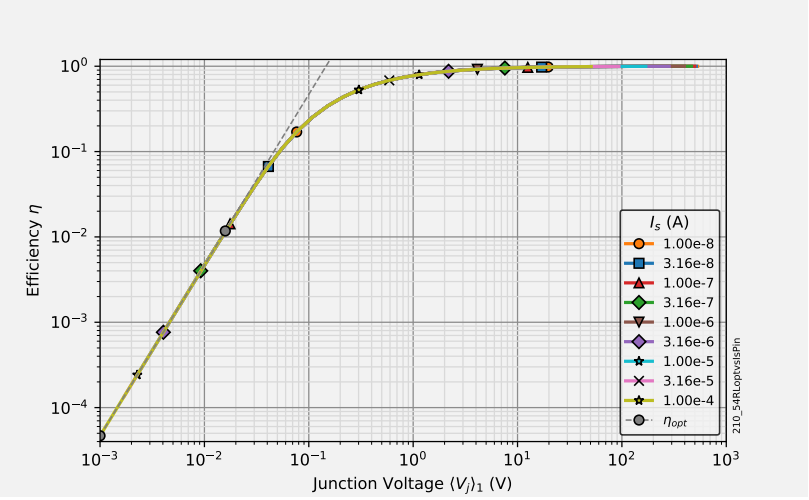


Figure 4.9 Simulated optimal efficiency η against junction voltage $\langle V_j \rangle_1$ for various diode saturation currents I_s, of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$) and $n = 1$. Also shown is the calculated η_{opt} from Eq. (4.45) which shows the $\langle V_j \rangle_1$-range for which this small signal efficiency matches the full range simulated efficiency. The difference between the simulated optimal efficiency and small signal approximation is only 6.9 % at $\langle V_j \rangle_1 = V_T$.

Although the swept variable in this simulation is the input power level, the graph shows efficiency against the resulting junction voltage $\langle V_j \rangle_1$. The curves for the different I_s values are all on the same line of optimal efficiency, they only have a different junction voltage range as they have different R_j values. Fig. 4.10 shows a 3D perspective of the same result to illustrate this.

In the preceding section we already noted the independence of $\eta(V_j)$ to I_s for the small signal regime line, when choosing the optimal R_L value. From this simulation result we see that this is also the case for the large signal regime. The picture changes, when we plot (for the same simulation) efficiency against the input power level, as shown in Fig. 4.11.

The reason for the shift in efficiency curves, for the different I_s values, is that R_j varies with I_s, not only in the small signal regime but across the whole

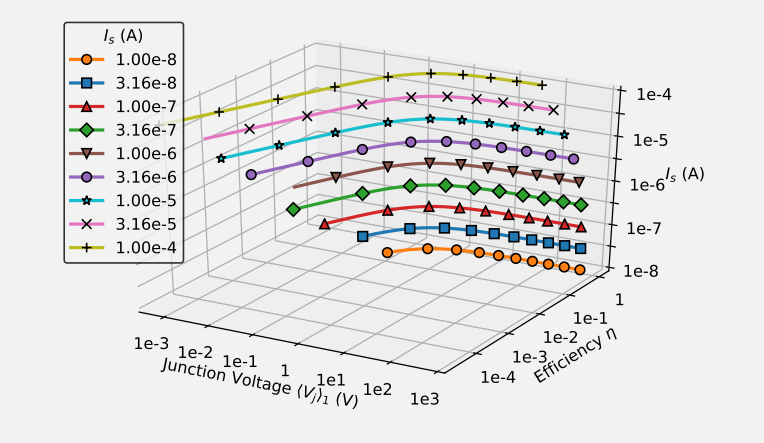


Figure 4.10 Three dimensional view of the simulated optimal efficiency η against junction voltage $\langle V_j \rangle_1$ and diode saturation current I_s of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$) and $n = 1$. This data is equal to the data shown in Fig. 4.9. The markers show the input power points for the −60 to +30 dBm range, in 10 dB steps.

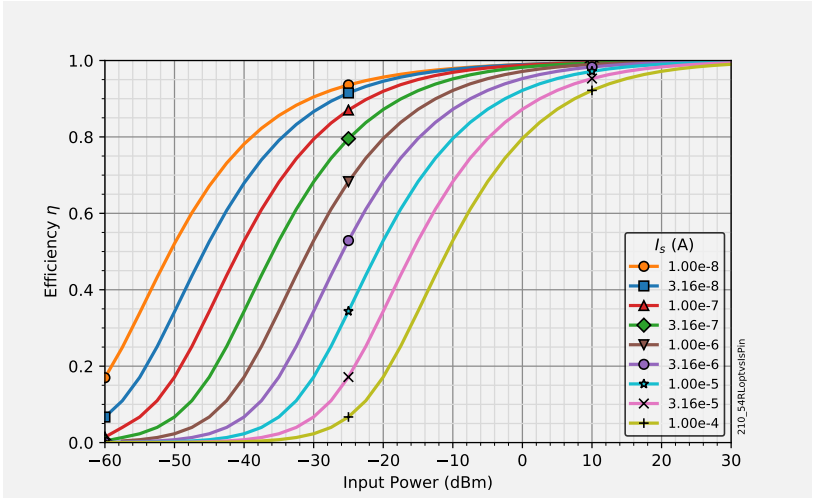


Figure 4.11 Simulated optimal efficiency η against input power P_{in} for various diode saturation currents I_s of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$) and $n = 1$. The curves shift by 10 dB in input power, per decade in I_s change.

input signal range. This makes that for a specific input power level, the junction voltage is different depending on the R_j value. Note that the shift in efficiency curves is exactly 10 dB per decade in I_s change[7]. For the small signal case this was already shown in Eq. (4.45), now we see this is also valid in the large signal case. With this, the optimal efficiency curve for any I_s value is known.

Fig. 4.12 shows the corresponding optimal load- and junction resistance R_L and R_j respectively. Their ratio R_L/R_j is shown in Fig. 4.13 (a) against input power and $R_L/R_j - 1$ against junction voltage $\langle V_j \rangle_1$ in (b). The minus one operation reveals the small signal straight curve without I_s dependency.

4.4.2 Emission coefficient dependency

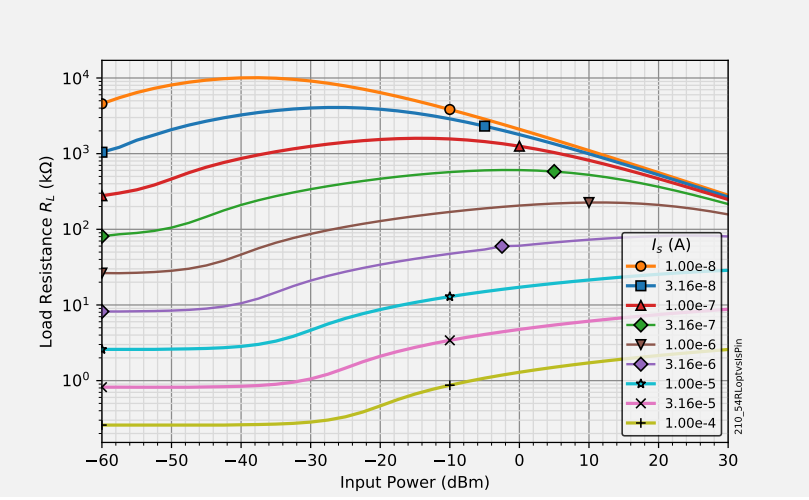
In the preceding section we have seen the dependency of efficiency and optimal load resistance on the diode's saturation current. The diode's emission coefficient n also plays a role, as can be seen from Eq. (3.1): $I_j = I_s(\mathrm{e}^{\frac{V_j}{nV_T}} - 1)$. Introducing $n \neq 1$ leads to a $\frac{1}{n}$ multiplication factor to V_j. This makes that the efficiency η versus V_j curve shifts, as is shown in Fig. 4.14 (a) using a scaled junction voltage on the x-axis. Also the corresponding efficiency versus input power level curve is shifted samewise as shown in Fig. 4.14 (b).

In the small signal regime, we have seen for the junction resistance $R_j = \frac{nV_T}{I_s}$, see Eq. (4.28). Therefore introducing $n \neq 1$ leads to a n multiplication factor to R_j for the small signal regime, resulting in an increase in diode dissipation and lowering of the efficiency (for $n > 1$). R_j is plotted scaled against scaled input power in Fig. 4.14 (c). This makes optimal efficiency predictable for different n values, when using an ideal *pn*-junction diode rectifier. The range for n is chosen to include *pn*-junction diode values.

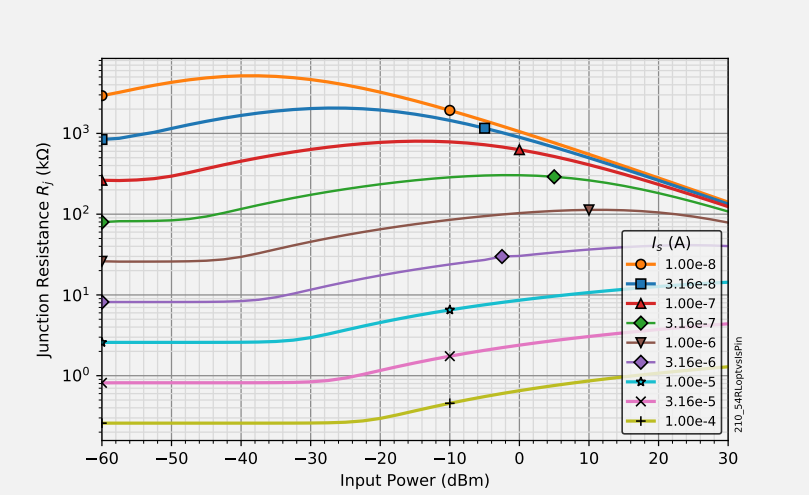
4.4.3 Temperature dependency

The diode equations have an implicit temperature dependency. E.g. the small signal optimal efficiency η_{opt} in Eq. (4.45) has $V_T I_s$ in the denominator. The thermal voltage is related to temperature as $V_T = k_B T/q$ and in Section 3.4.1 we saw that I_s is also temperature dependent. Fig. 4.15 shows a simulation result (optimal efficiency and junction resistance versus junction voltage or input power) when varying the junction temperature in an ideal single diode rectifier circuit. The optimal efficiency versus junction voltage graph in Fig. 4.15 (a) shows a little variation for the different temperature values. It is important to notice the variation in junction resistance and what shift this brings in the corresponding input power level for a fixed junction voltage. Clearly, from

[7] This is verified by plotting the curves with shifted input power levels resulting in a figure with all curves on top of each other.

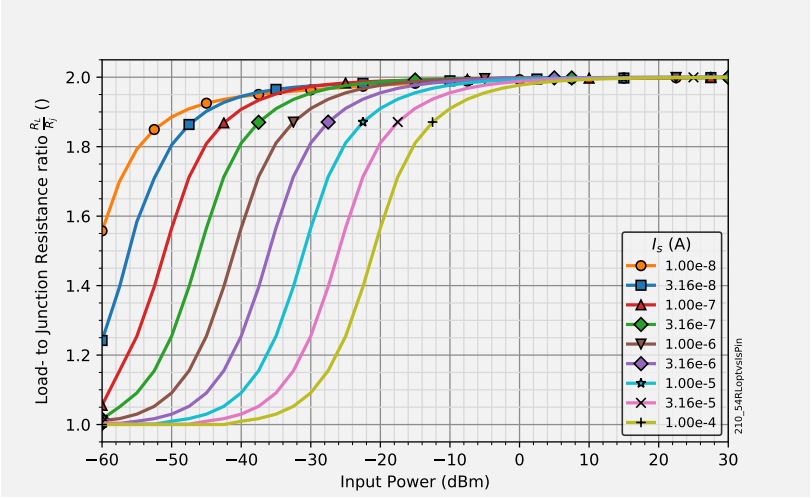


(a) Optimal load resistance R_L

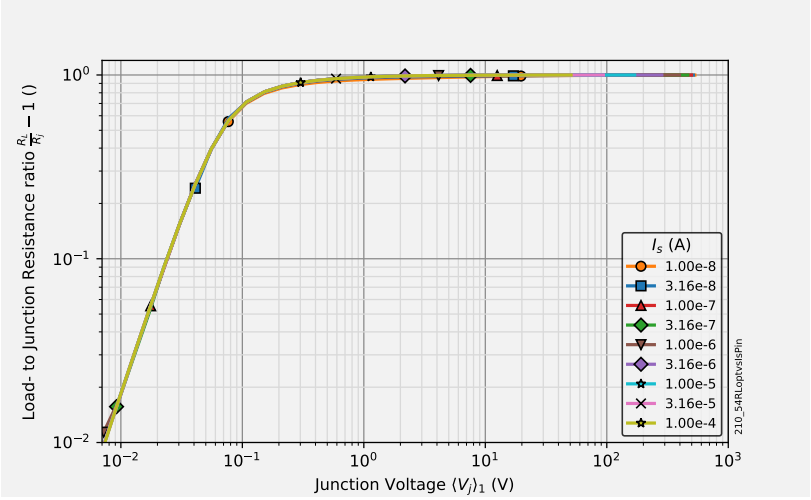


(b) Optimal junction resistance R_j

Figure 4.12 Simulated optimal (a) load and (b) junction resistance against input power P_{in} for various diode saturation currents I_s of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$) and $n = 1$. See Fig. 4.11 for the legend.

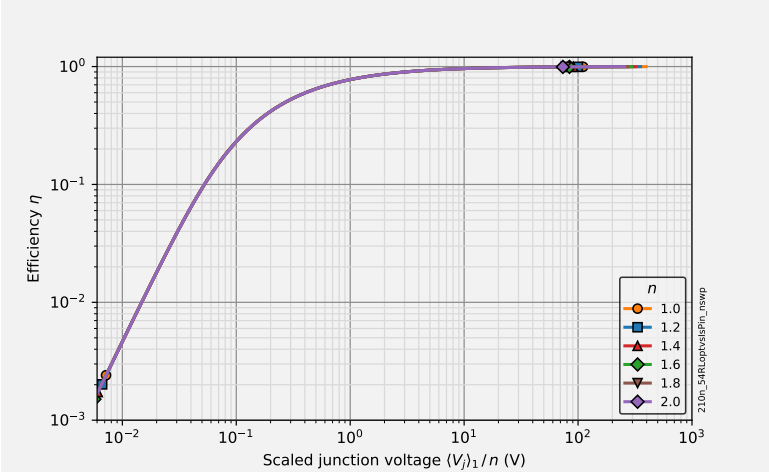


(a) Optimal load- to junction resistance ratio $\frac{R_L}{R_j}$

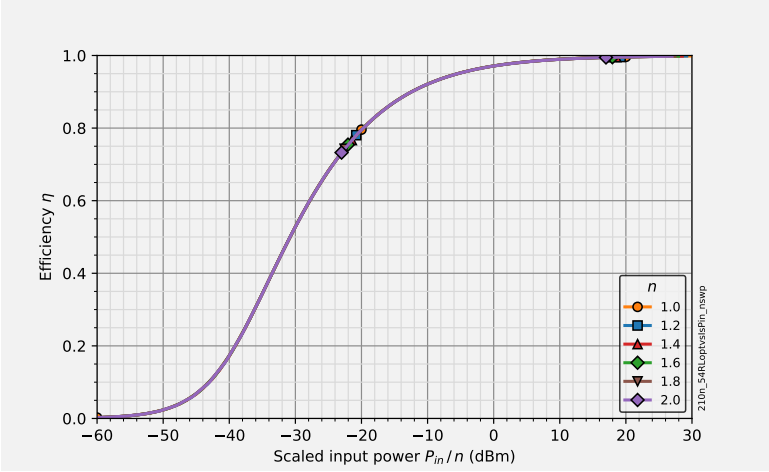


(b) Optimal load- to junction resistance ratio minus one $\frac{R_L}{R_j} - 1$

Figure 4.13 Simulated optimal load- to junction resistance ratio against (a) input power P_{in} and (b) the resistance ratio minus one against diode junction voltage$\langle V_j \rangle_1$ and diode saturation current I_s of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$) and $n = 1$.

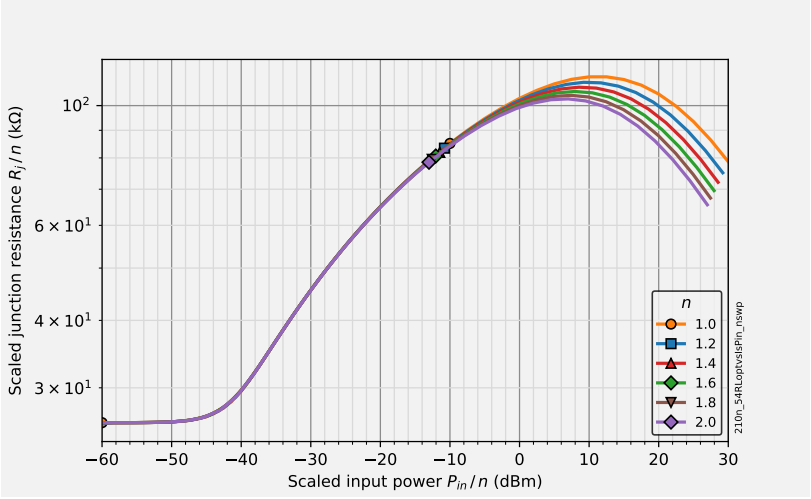


(a) Optimal efficiency versus scaled junction voltage $\langle V_j \rangle_1 / n$.



(b) Optimal efficiency versus scaled input power P_{in} / n.

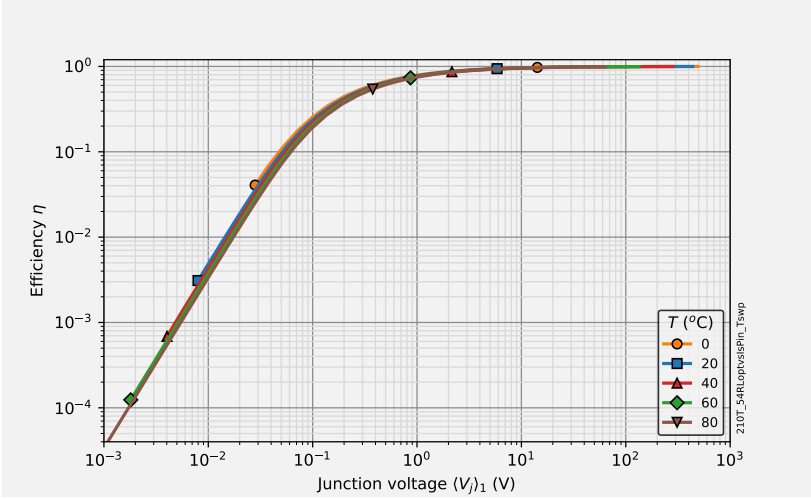
Figure 4.14 Simulated optimal efficiency versus (a) junction voltage and (b) input power and (c) junction resistance at optimal efficiency versus input power of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $I_s = 1$ μA and $n = 1$–2. In this case the junction voltage, input power and junction resistance are multiplied by a factor $\frac{1}{n}$ in a post-processing step.



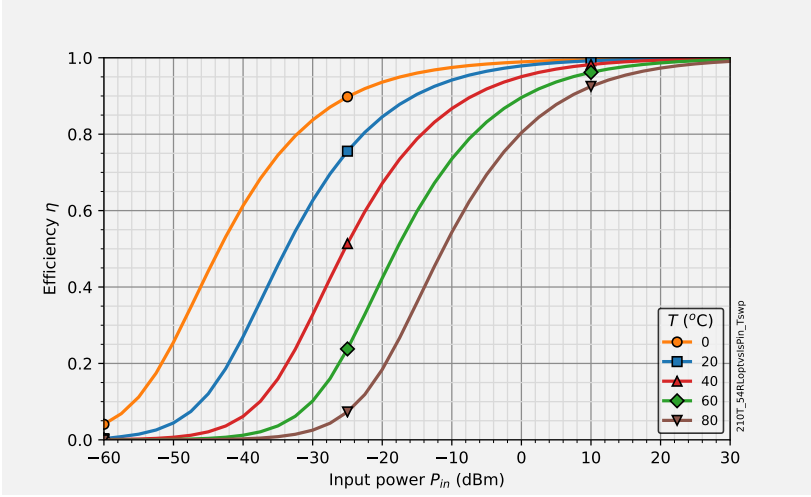
(c) Scaled junction resistance R_j/n at optimal efficiency versus scaled input power P_{in}/n.

Figure 4.14 Simulated optimal efficiency versus (a) junction voltage and (b) input power and (c) junction resistance at optimal efficiency versus input power of an ideal single diode rectifier at a temperature of $T = 300$ K, $f_0 = 6.78$ MHz, $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $I_s = 1$ μA and $n = 1$–2. In this case the junction voltage, input power and junction resistance are multiplied by a factor $\frac{1}{n}$ in a post-processing step.

Fig. 4.15 (b) we can conclude that a lower temperature will result in a better efficiency at the same input power level.

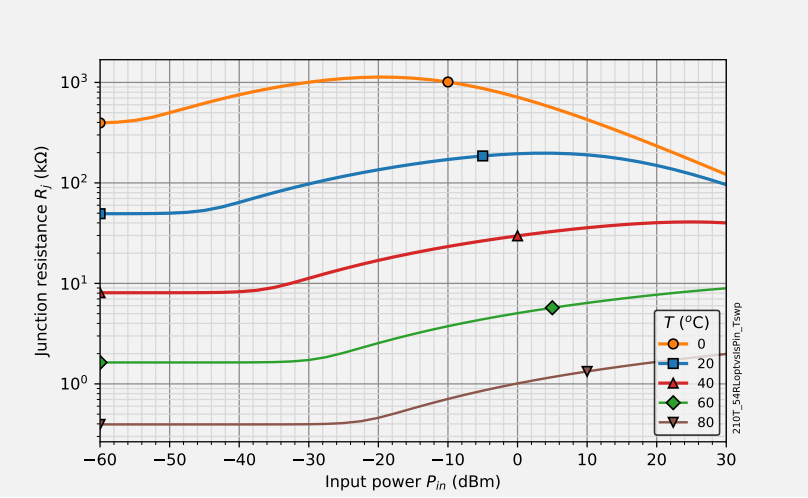


(a) Optimal efficiency versus junction voltage $\langle V_j \rangle_1$.



(b) Optimal efficiency versus input power.

Figure 4.15 Simulated optimal efficiency versus (a) junction voltage and (b) input power and (c) junction resistance versus input power of an ideal single diode rectifier at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $I_s = 1$ μA, $f_0 = 6.78$ MHz, $n = 1$ at different junction temperatures.



(c) Junction Resistance versus input power.

Figure 4.15 Simulated optimal efficiency versus (a) junction voltage and (b) input power and (c) junction resistance versus input power of an ideal single diode rectifier at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $I_s = 1$ μA, $f_0 = 6.78$ MHz, $n = 1$ at different junction temperatures.

4.4.4 Diode dissipation

From the preceding efficiency figures we see that the ideal diode rectifier is able to achieve a power conversion efficiency between zero and 100 %, depending on the input signal power level. The law of conservation of energy states that the total energy of an isolated system remains constant. This means that when having no efficiency ($\eta = 0$ %) all energy is dissipated in the diode, as the ideal rectifier circuit doesn't contain other dissipative elements. Vice versa, at $\eta =$ 100 % no energy should be dissipated in the diode. The simplified single diode rectifier circuit model is used as reference, see Fig. 2.11. In this circuit, the energy put into the ideal diode is only present at the fundamental frequency, which is calculated as

$$P_{\text{in}} = P_{\text{in}}^1 = \frac{1}{2}\,\text{Re}\left(\langle V_j\rangle_1 \langle I_j\rangle_1^*\right). \tag{4.49}$$

In fact, the simplified diode rectifier circuit model uses a (non-linear) resistor to absorb this energy; in reality we should see this as a resistor of which the dissipation depends on the signal level. The fundamental current $\langle I_j\rangle_1$ flows towards the non-grounded side of the resistor indicating the diode is dissipating energy (power dissipation passive sign convention). This means power is removed (dissipated as heat) from the electrical domain. In the case of a rectifier, besides energy transformed into heat there is also a part translated from the fun-

damental frequency to other harmonic frequencies including dc. For this ideal circuit, only the dc current is applicable[8] and translates into energy delivered to the load resistor R_L. The diode's power dissipation can therefore be written as[9]

$$P_d = P_{\text{in}}^1 - P_L^0 = \frac{1}{2}\,\text{Re}\left(\langle V_j\rangle_1 \langle I_j\rangle_1^*\right) - \langle I_j\rangle_0^2 R_L. \tag{4.50}$$

As the dissipation is dependent on the input power level, we define the *relative diode dissipation* as

$$\frac{P_d}{P_{\text{in}}^1} = \frac{\frac{1}{2}\,\text{Re}\left(\langle V_j\rangle_1 \langle I_j\rangle_1^*\right) - \langle I_j\rangle_0^2 R_L}{P_{\text{in}}^1} = 1 - \eta, \tag{4.51}$$

with η being the efficiency as defined in Eq. (2.21). Fig. 4.16 shows the relative power dissipation of an ideal single diode rectifier, for different junction temperatures and using a complex conjugately matched source. The curves are drawn for the optimal efficiency case at each point of input power temperature.

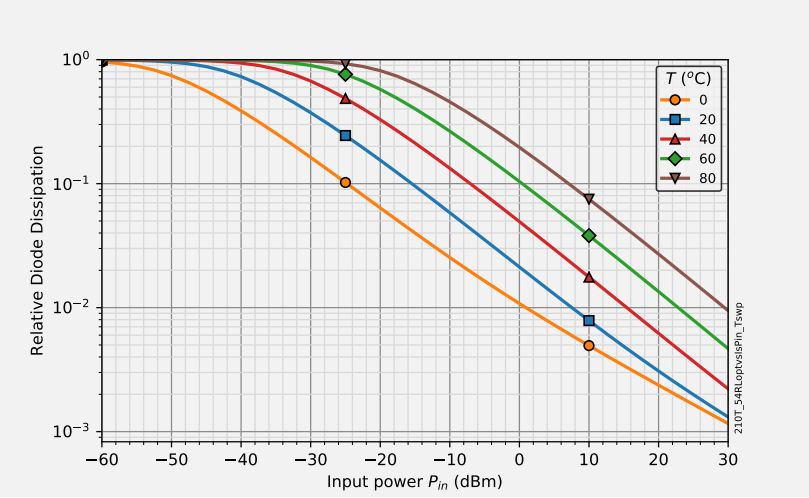


Figure 4.16 Relative diode dissipation Eq. (4.51) (at optimal efficiency) versus input power for different values of the junction temperature in an ideal single diode rectifier at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $I_s = 1$ μA, $f_0 = 6.78$ MHz and $n = 1$.

[8] At a later stage we will see that this simplification doesn't hold for a real diode, in which the parasitic series resistance R_s also dissipates energy, and not only at the fundamental frequency.

[9] In this equation we assume the circuit's capacitor being ideal, which is the case for the ideal rectifier circuit.

4.4.5 Current responsivity

To quantify the rectifying energy transfer capabilities of a diode, the current responsivity $\Re_I$ is sometimes used [15]:

$$\Re_I = \frac{\langle i_{\text{sc}} \rangle_0}{P_{\text{in}}^1}, \tag{4.52}$$

in which $\langle i_{\text{sc}} \rangle_0$ represents the dc short circuit current (first term in Eq. (4.18)) and P_{in}^1 the power flowing into the diode:

$$P_{\text{in}}^1 = \frac{1}{T} \int_0^T v_j(t) i_j(t) \mathrm{d}t = \frac{1}{2} V_j I_j. \tag{4.53}$$

In Appendix B we elaborate why we don't see the current responsivity to be a useful quantity to design efficient WET rectifier circuits.

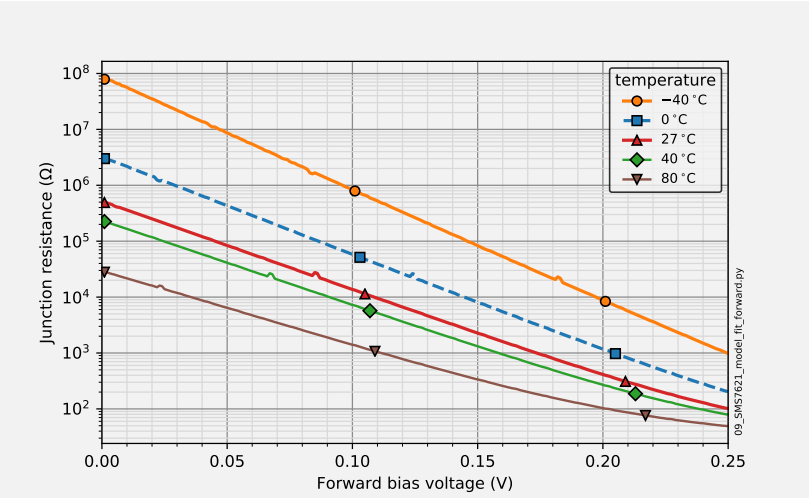
4.5 Schottky Diode Efficiency

An important conclusion that can be drawn from Fig. 4.11 is that a lower diode saturation current I_s enables a higher efficiency at a certain input power level. This is contrary to the idea that a SBD should be preferred over a *pn*-junction diode for its higher current at a certain voltage level. In this section, the SBD will be analysed in more detail to unravel this contradiction.

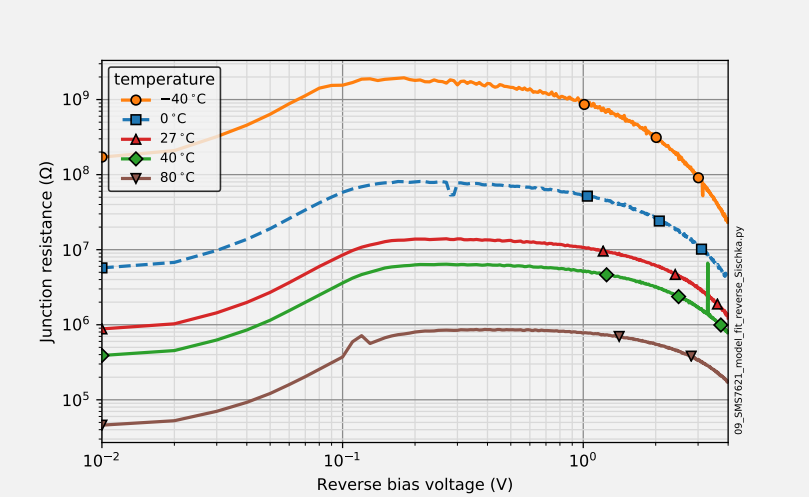
The two main differences between an ideal *pn*-junction diode and an SBD are the reverse bias regime behaviour and the voltage dependent junction potential. The details are discussed in Section 3.4.2. The focus here is on the different reverse bias behaviour: for the SBD, the junction resistance R_j doesn't saturate at a (close to) infinite value for large reverse bias conditions. The value is lower and an example is shown in Fig. 4.17 (b). This figure is derived from measured SMS 7621 data shown in Fig. 3.17 (a), using the inverse of the diode conductance gradient Equation (4.26): $R_j = \partial V_j / \partial I_j$. Using Eq. (4.28) at 300 K, we find for the SMS 7621: $\lim_{V_j \to 0} R_j = nV_T / I_s = 502\ \text{k}\Omega$. The forward biased junction resistance, shown in Fig. 4.17 (a), is equal for the ideal *pn*-junction diode and the SBD.

In the large signal rectifier situation, the reverse bias junction resistance curve results in a lower average R_j value for the Schottky diode, compared to using the Shockley equation (3.1). This is demonstrated when repeating the load experiment from Section 4.2, this time with a Schottky diode model named 'Sze model' (see Section 3.6.3). The comparison between the two diode models is shown in Fig. 4.18.

For the small signal region, the results are equal for the SPICE and Sze models. But in the large signal region, the Schottky diode Sze model shows a steady drop



(a) Forward biased junction resistance, derived from Fig. 3.12 (a).



(b) Reverse biased junction resistance, derived from Fig. 3.17 (a).

Figure 4.17 Measured (a) forward- and (b) reverse biased diode junction resistance versus junction voltage of a SMS 7621 diode. Both figures are derived using the inverse of the diode conductance gradient equation (4.26) to calculate the junction resistance: $R_j = \partial V_j / \partial I_j$.

in junction resistance. For power levels above +10 dBm, it is also noticed that the curves are not grouped on R_L-value but on I_s-value, like for the small signal region. This is due to the dropping junction resistance with larger negative voltages. The figure shows that it is difficult to design for a constant R_j value over a large power range when using a Schottky diode. In the following section the impact on efficiency will be analysed.

4.5.1 Comparing models

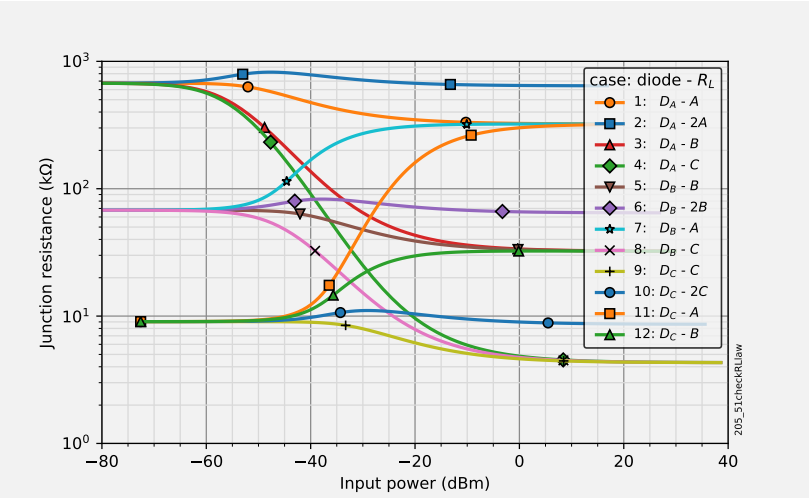
Following an equal approach as for the *pn*-junction diode efficiency simulations, the Schottky diode is used in the same ideal single diode rectifier from Section 2.2.1. The diode is taken ideal in a sense that its series resistance $R_s = 0$ and the junction capacitance $C_{j0} = 0$. Two versions of the diode current-voltage equation are used: 'Sze fwd' being Shockley's ideal diode equation (3.1), also for the reverse biased region but with a voltage dependent junction potential ϕ_{B0}, see Eq. (3.8), and 'Sze' which makes use of the reverse bias equation (3.8) as well. Both are compared to 'SPICE' which is based on the standard SPICE *pn*-junction model, using the same parameter values and $I_s = 65.41$ nA. To see a comparison between the Sze-, Sischka- and SPICE models including realistic R_s and C_{j0} values, we refer to Fig. 3.21.

The deviation of the Schottky diode from the *pn*-junction diode is shown from the results, provided in Fig. 4.19 and 4.20. The 'Sze fwd' curves show the deviation caused just by the voltage dependency of the junction potential $d\phi_B/dV_j$, resulting in a varying saturation current I_S with junction voltage V_j, which in turn results in a change in junction resistance. The 'Sze' curves show an extra deviation, when also the reverse bias equation is used. This results in a declining junction resistance for larger junction voltages. The rectifier starts to make use of the $V_j < -2.8V_T$ regime for an input power above -52.5 dBm, nicely visible in Fig. 4.20 (b), see also Fig. 4.21 for the junction voltage to input power relation. The efficiency versus junction voltage curves are all on top of each other, like in Fig. 4.9. The junction resistance shows a significant deviation for the large signal regime: up to three orders of magnitude. This corresponds to a different input matching requirement for the practical case.

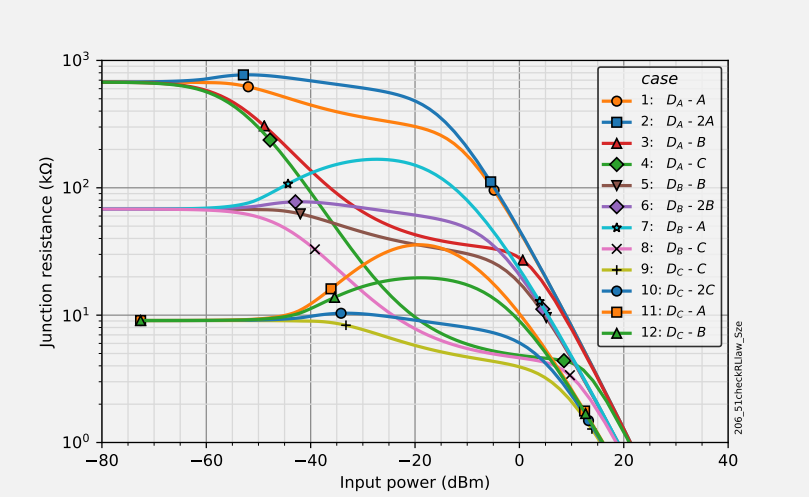
4.5.2 Effect of R_s and C_j

Fig. 4.22 shows the basic diode model based on Fig. 3.2, modified to reflect the fundamental frequency junction resistance R_j approach of Eq. (2.20). Both diode parasitics R_s and C_j have an effect on the diode junction voltage V_j, which will be analysed in this section.

To better understand the implications of adding these parasitic elements,

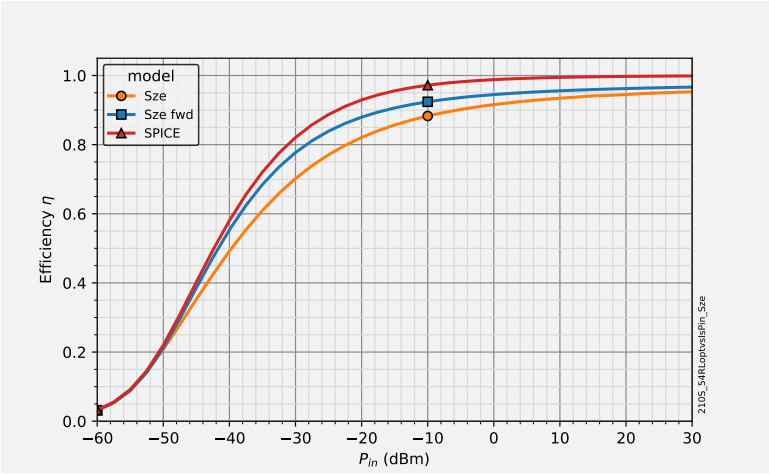


(a) SPICE model

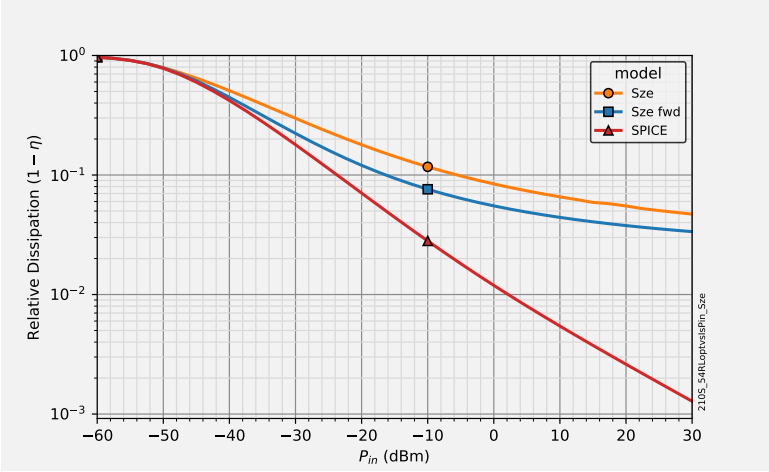


(b) Sze model

Figure 4.18 Simulated diode junction resistance R_j versus RF input power P_{in} for various load experiment cases, for an ideal single diode rectifier having $n = 1$, $R_s = 0\ \Omega$, $C_{j0} = 0$ pF, $f_0 = 6.78$ MHz and $T = 300$ K. See Table 4.2 for the case parameter values. (a) using a SPICE diode model, (b) using the Sze diode model.

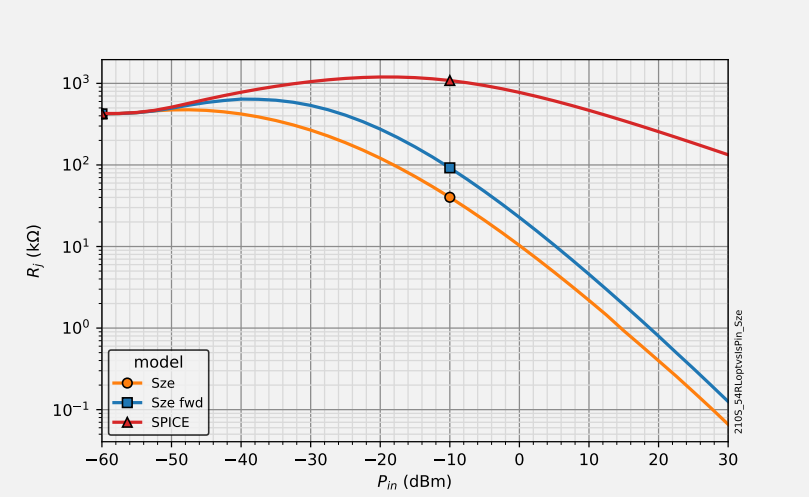


(a) Efficiency versus input power.

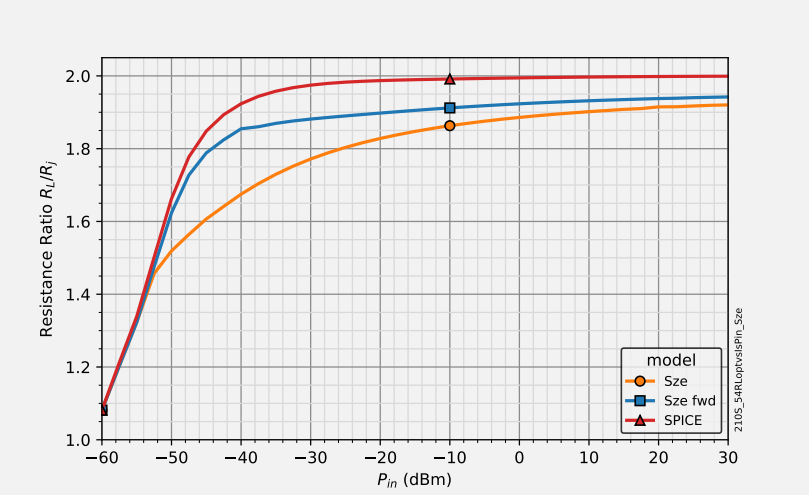


(b) Relative Diode Dissipation $(1-\eta)$.

Figure 4.19 Simulated ideal Schottky diode rectifier efficiency and relative dissipation at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $\phi_B = 0.47$ V, $d\phi_B/dV_j = 0.008$, $R_s = 0$, $C_{j0} = 0$, $I_s = 65.41$ nA, $f_0 = 6.78$ MHz and $n = 1.064$. The comparison is made between the full 'Sze' model, the voltage dependent junction potential model 'Sze fwd' and the standard SPICE *pn*-junction model 'SPICE', including the breakdown effect.



(a) Junction Resistance versus input power.



(b) Resistance Ratio $\frac{R_L}{R_j}$ versus input power.

Figure 4.20 Simulated ideal Schottky diode rectifier junction resistance and resistance ratio at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $\phi_B = 0.47$ V, $d\phi_B/dV_j = 0.008$, $R_s = 0$, $C_{j0} = 0$, $I_s = 65.41$ nA, $f_0 = 6.78$ MHz and $n = 1.064$. The 'Sze' model is compared with the voltage dependent junction potential model 'Sze fwd' and the standard SPICE *pn*-junction model 'SPICE' including the breakdown effect.

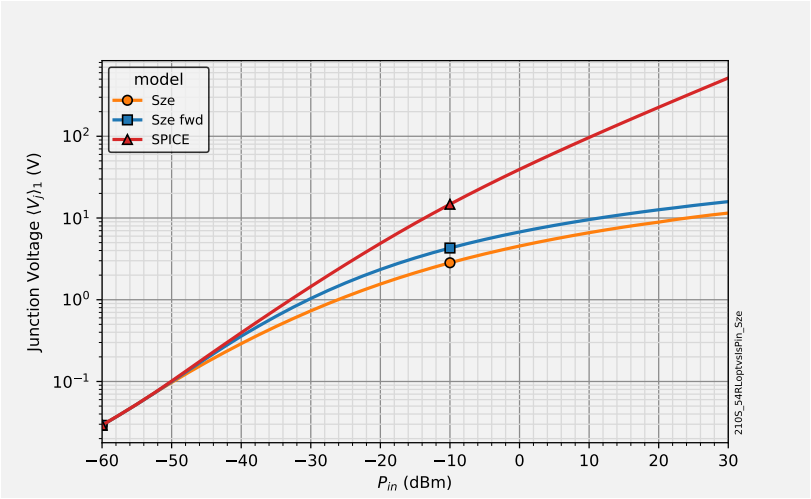


Figure 4.21 Simulated diode junction voltage $\langle V_j \rangle_1$, as a function of input power P_{in} to an ideal Schottky diode rectifier at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $\phi_B = 0.47$ V, $d\phi_B/dV_j = 0.008$, $R_s = 0$, $C_{j0} = 0$, $I_s = 65.41$ nA, $f_0 = 6.78$ MHz and $n = 1.064$. The comparison is made between the full 'Sze' model, the voltage dependent junction potential model 'Sze fwd' and the standard SPICE *pn*-junction model 'SPICE'.

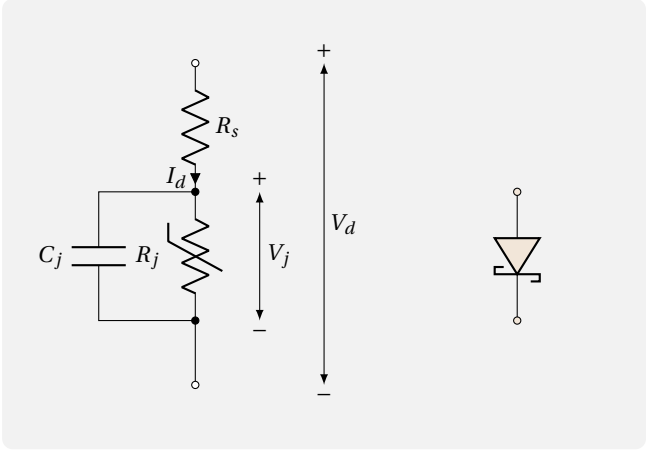


Figure 4.22 Equivalent diode model at the fundamental frequency.

the diode model is complemented with the rectifier circuit elements from Section 2.2.1, as shown in Fig. 4.23 (a) and (b). This represents the rectifier input impedance $\langle Z_{\text{in}} \rangle_1$ as a parallel R-C model $R_{\text{in}} \parallel C_{\text{in}}$, see Fig. 4.23 (c). This circuit is simulated using the complex conjugately matched P_{CCM} source from Section 2.3.1, set to a circuit input power $P_s^1 = 1$ mW, and component values corresponding to a large signal situation (small R_j and R_L values) and a relatively large $C_j = 1$ pF value to show its impact starting at a lower frequency (compared to using a lower realistic capacitance value which starts to have impact at a higher frequency). The result is shown in Fig. 4.24. From this we can see that for lower frequencies (< 100 kHz), the C_j capacitance doesn't play a role: C_L is dominant and is not acting as a short as assumed in the ideal rectifier (Section 2.2.1). In this case both R_j and R_L dissipate the circuit input power. Between 10 MHz and 200 MHz C_L shorts R_L and C_j still doesn't contribute, resulting in an equivalent R_{in} of 212 Ω ($R_s + R_j$). The equivalent parallel $\langle Z_{\text{in}} \rangle_1$ R-C model is shown in Fig. 4.23 (b). The input power is dissipated mainly in R_j and some in R_s (due to their respective resistance values). For higher frequencies, C_j starts to play a role in shorting R_j, resulting in more current flow through R_s and therefore also more power dissipation in R_s and less in R_j. This makes that the energy transfer efficiency drops. As this is just a fundamental frequency model, the higher order harmonic currents are not taken into account. In the real circuit, they do play a role in this regime as they dissipate energy in R_s as well, further degrading the circuit efficiency.

For the lower frequencies, the equivalent impedance of the circuit can be described as

$$Z'_{\text{in}} = \frac{j\omega R'_j R_L C_L + R'_j + R_L}{j\omega R_L C_L + 1}, \tag{4.54}$$

with $R'_j = R_s + R_j$. For the higher frequencies (no power dissipation in R_L), the equivalent impedance is

$$Z''_{\text{in}} = \frac{j\omega R_s R_j C_j + R_s + R_j}{j\omega R_j C_j + 1}. \tag{4.55}$$

To calculate the equivalent R_{in} and C_{in} values, we use $R_{\text{in}} = 1/\operatorname{Re}(Y_{\text{in}})$ and $C_{\text{in}} = \operatorname{Im}(Y_{\text{in}})/\omega$. For the specific frequency ranges the corresponding equivalent impedance is used to obtain the admittance.

Another effect of C_j is that the junction impedance becomes complex. The insight that the energy conversion efficiency is independent of I_s when plotted as a function of V_j for a non-complex diode junction impedance also holds for a complex impedance. Adding a junction capacitance parallel to the junction resistance doesn't change the voltage magnitude across the pair, only its phase.

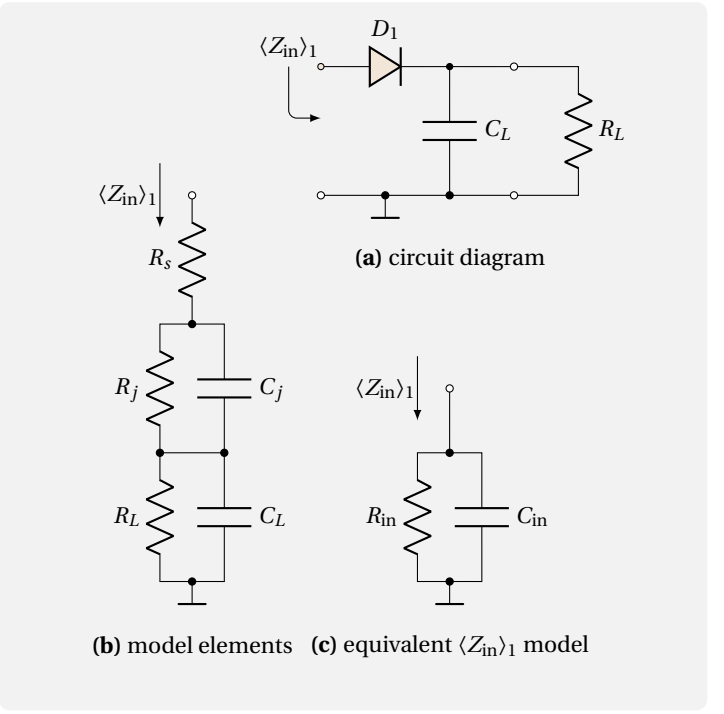
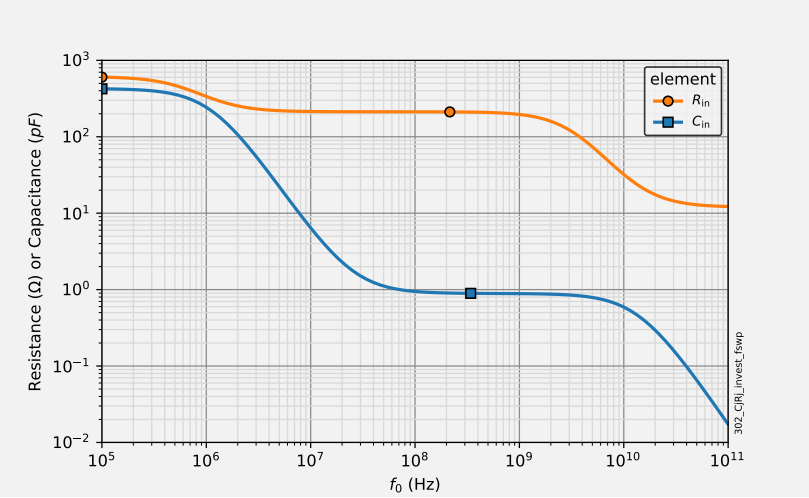
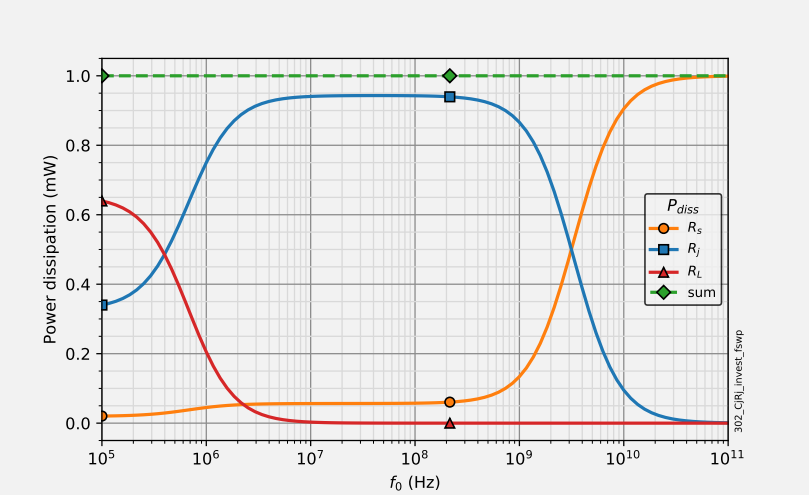


Figure 4.23 Single diode rectifier: (a) circuit diagram with (b) equivalent impedance model elements and (c) parallel R-C model at the fundamental frequency. Values used: $R_s = 12\ \Omega$, $R_j = 200\ \Omega$, $C_j = 1$ pF, $R_L = 400\ \Omega$, $C_L = 1$ nF.



(a) Parallel resistance and capacitance value versus frequency.



(b) Power dissipation for the different resistors versus frequency.

Figure 4.24 Simulated linear single diode rectifier model (see Fig. 4.23) with fixed component values $R_s = 12\ \Omega$, $R_j = 200\ \Omega$, $C_j = 1$ pF, $R_L = 400\ \Omega$ and $C_L = 1$ nF and $P_{\text{in}} = 1$ mW. (a) Equivalent parallel R_{in}-C_{in} model component values, (b) power dissipation in the three rectifier resistors R_s, R_j, R_L and their sum.

This is verified by ADS simulation. To verify the junction capacitance model, the diode junction impedance can be derived from a measurement. If a matching circuit is included, this should first be de-embedded from the measurement data. After that, the R_s value — obtained from a dc I-V measurement — can be subtracted. Taking the imaginary part of the remaining admittance provides the diode junction capacitance.

Simulating the single diode rectifier input capacitance in ADS results in a response corresponding to Eq. (4.55), as shown in Fig. 4.25. For this simulation, an ideal load capacitor C_L is used, except for the $C_L = 3.3\ \mu$F case which provides a reactance of $X_C = -j0.2\ \Omega$ at 1 MHz. One would normally expect this to be low enough for shorting RF signals. The graph shows the impact of the small junction resistance in the large-signal case. The shown increase in capacitance results in an extra challenge to match the rectifier input impedance in case a range of input power levels of e.g. 0 to 30 dBm should be served by the circuit.

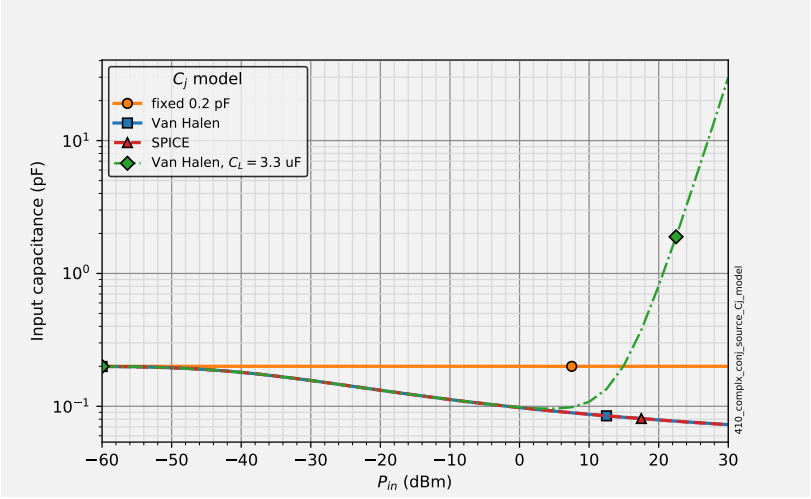
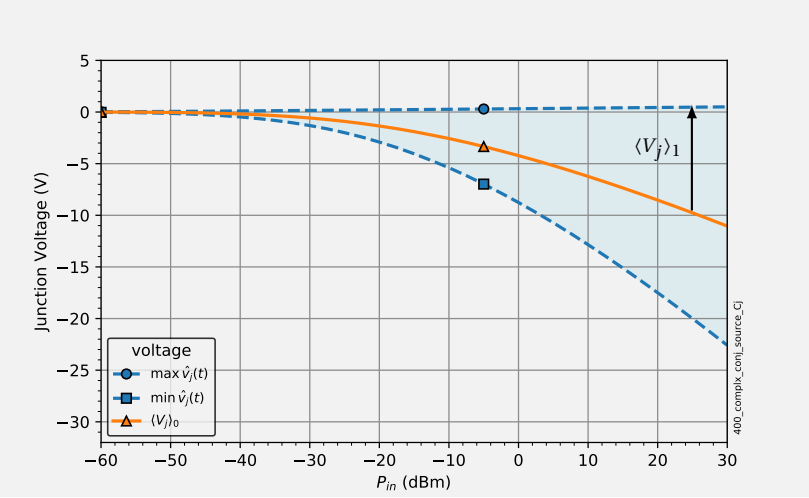


Figure 4.25 Simulated rectifier input capacitance C_{in} for different capacitor models as a function of input power to an ideal Schottky Diode rectifier with ideal C_L at a frequency of 1 MHz and $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $\phi_B = 0.47$ V, $d\phi_B/dV_j = 0.008$, $R_s = 0$, $C_{j0} = 0.2$ pF, $I_s = 65.41$ nA and $n = 1.064$. The curve for the $C_L = 3.3\ \mu$F case (dot-dash) shows the impact of small junction- and load resistance.

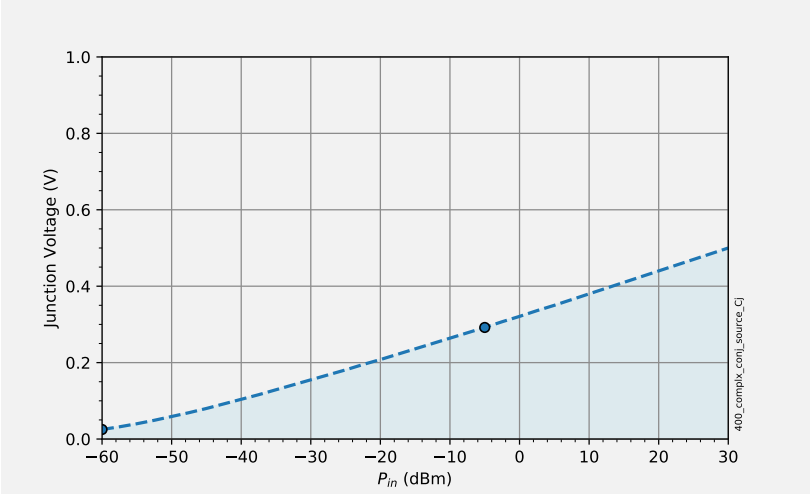
For an input power level of $-50 < P_{\text{in}} < 0$ dBm we see a drop in capacitance with increasing signal level. This is a result of the increasing negative dc-bias voltage across the diode, as the junction capacitance is voltage dependent for the Van Halen and SPICE models. Their different capacitance-voltage response is masked due to the fact that most of the time, the junction voltage is negative. Fig. 4.26 shows the diode junction voltage in this simulation.

Another effect R_s has, is on its energy dissipation. Not only at f_0 but also for the generated dc current and harmonic frequencies. In the ideal circuit used, the diode anode is at ground for dc and the harmonic frequencies but the diode junction (other side of R_s) is not. This will influence the amount of energy available for R_j and will also affect the efficiency equation.

On top of these effects, the varying optimal source impedance due to the varying R_j and C_j values with input power, results in a varying mismatch loss when making use of a fixed matching circuit.



(a) Junction voltages $\hat{v}_j(t)$ (blue) and $\langle V_j \rangle_0$ (orange) and indication of $\langle V_j \rangle_1$ (arrow).



(b) Detail of max $\hat{v}_j(t)$.

Figure 4.26 Simulated diode junction voltage as a function of input power of an ideal Schottky diode rectifier at $p_i = 2$, $\psi_0 = 0.735$ ($\psi' = 0.69$), $\phi_B = 0.47$ V, $d\phi_B / dV_j = 0.008$, $R_s = 0$, $C_{j0} = 0.1$ pF, $I_s = 65.41$ nA and $n = 1.064$ at 1 MHz. Shown is the dc term $\langle V_j \rangle_0$ and the amplitude of $\hat{v}_j(t)$.

4.6 Load Resistance Choice

Till this point we have focussed on obtaining the optimal power transfer efficiency for the rectifier circuit by choosing the best load resistance values, as indicated in Fig. 2.16 (b). Next we will add the impedance matching circuit, corresponding to Fig. 2.16 (c), and show two different approaches.

To obtain an optimal transfer of energy between source (typically a signal receiving antenna) and rectifier input, we need some form of impedance matching between these components. A mismatch in source- and circuit input impedance will lead to a mismatch loss, reducing the rectifier efficiency. From that perspective a constant circuit input resistance is preferred, otherwise the circuit can only be perfectly matched at a specific input power level. In Fig. 4.18 we see that having a lower saturation current diode type results in more diode junction resistance variation against input power variation between −30 and 0 dBm. This junction resistance variation corresponds to a circuit input resistance variation as well.

In this section we discuss the comparison between the case of using the optimal load resistance, being input power dependent, and the case of using a fixed load resistance. The choice of this fixed load resistance value is made such as to obtain the least mismatch loss at the rectifier input over the above mentioned input power range. The comparison is based on the circuit simulation shown in Fig. 4.27: a single diode rectifier with load resistor and complex conjugated source P_{CCM}.

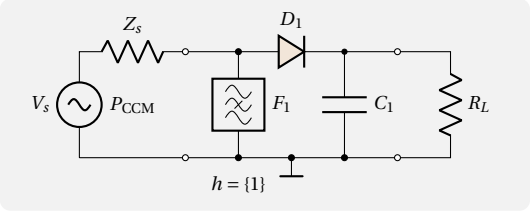


Figure 4.27 Ideal peak detector simulation circuit diagram as described in Section 2.2.1, using a packaged SMS7621 SBD Sischka macro model. The bandstop filter F_1 is tuned at the circuits operating frequency $f_0 = 868$ MHz.

For the optimal load resistance, only the input power is swept and the load resistance optimized for rectifier efficiency. For the fixed load resistance case, both circuit input power and load resistance are swept to picture the result of having non-optimal load resistance values. From this a fixed value is selected: in this example (SMS7621 SBD at 868 MHz) we use $R_L = 40$ kΩ.

The resulting optimal achievable efficiency for the single diode peak detector

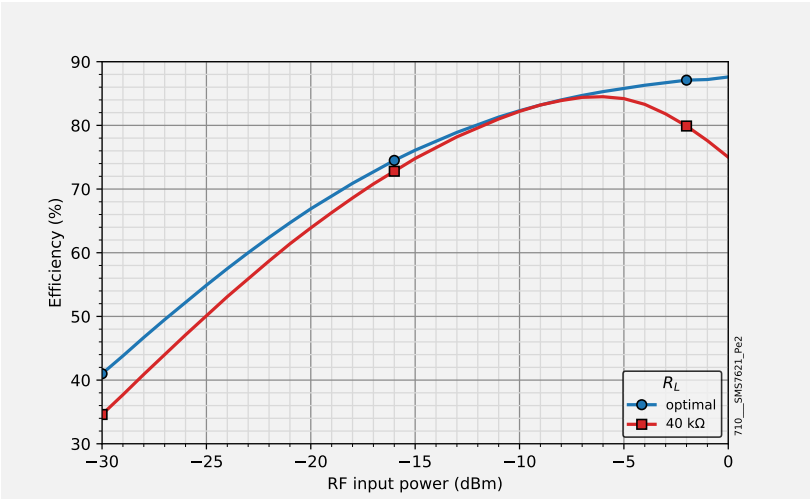


Figure 4.28 Both optimal and $R_L = 40$ kΩ efficiency η_2 of an ideal single diode peak detector rectifier configuration, using an SMS7621 SBD, simulated at $f_0 = 868$ MHz using the Sischka macro model including diode package.

rectifier, is shown in Fig. 4.28 for two different load resistances, using an SMS7621 SBD[10]. For the fixed load resistance case, post simulation calculations were used for which Fig. 4.29 was used as reference.

Fig. 4.30 (a) shows the optimal load resistance, efficiency loss L_η for arbitrary load resistance and in (b) rectifier input impedance Z_{rect} result of the same rectifier topology, at 868 MHz. The efficiency loss factor for the non-matched rectifier, is calculated as

$$L_\eta = \frac{\eta_{2,\text{opt}}}{\eta_2}, \tag{4.56}$$

with $\eta_{2,\text{opt}}$ being the optimal achievable efficiency at each input power level by optimizing the load resistance R_L of the circuit. η_2 is the obtained efficiency at any load resistance R_L. The ratio L_η corresponds to the loss due to having a non-optimal load resistance. From these figures we see that a fixed load resistance of 40 kΩ results in an efficiency loss of less than 1 dB across the input power range of −30 to 0 dBm. In Fig. 4.30 (b) we can see that a fixed load resistance of 40 kΩ doesn't correspond to a fixed input impedance: the variation is between $(17 - 817\,j)$ Ω and $(65 - 1045\,j)$ Ω. From the same figure, the rectifier input impedance for the optimal efficiency case shows a larger variation with values between $(9.3 - 837\,j)$ Ω and $(146 - 995\,j)$ Ω.

The next step is to analyse the efficiency of the complete rectifier circuit of both input impedance matching and the diode rectifying parts. To keep the

[10]This is for the un-matched case. The input filter F_1 and loading capacitor C_1 are ideal.

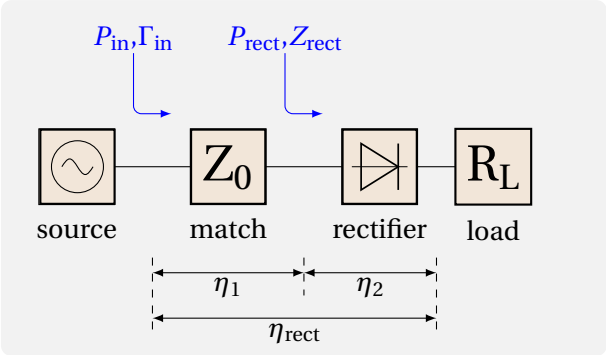


Figure 4.29 Block diagram showing the post simulation approach. The input matching circuit is modelled using Eq. (4.57) with a selectable reference impedance Z_0. The load resistance is either optimized for efficiency as a function of input power or kept constant at a fixed value. η_1 is the input impedance mismatch to Z_0 loss factor, η_2 the diode rectification efficiency.

example general, the choice is made to make use of calculating the circuit input reflection coefficient referenced to a complex reference impedance instead of designing a specific impedance matching circuit. This reflection coefficient can be defined, for a complex reference impedance Z_0, as [106]:

$$\Gamma_{in} = \frac{Z_{rect} - Z_0^*}{Z_{rect} + Z_0}, \tag{4.57}$$

with Z_0^* being the complex conjugate of Z_0. This reference impedance is chosen as $Z_0 = Z_{rect}^*$, with Z_{rect} selected somewhere in the range of rectifier input impedances found for the different input power levels.

The input impedance efficiency factor is calculated as:

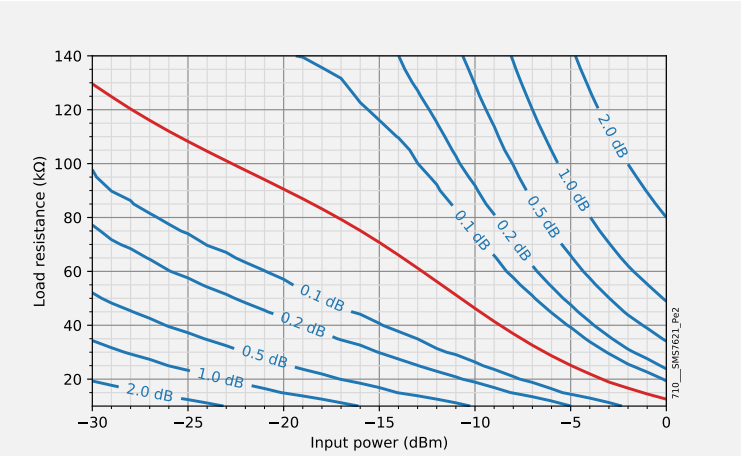
$$G_{i,in} = 1 - |\langle \Gamma_{in} \rangle_1|^2 = \eta_1, \tag{4.58}$$

which can be seen as the efficiency factor of input match. This input mismatch results in a difference between the source- and rectifier circuit input power levels. As the P_{CCM} source is used in the simulation, all results are related to the rectifier circuit input power level P_{rect}. The corresponding source power level[11] can be calculated using

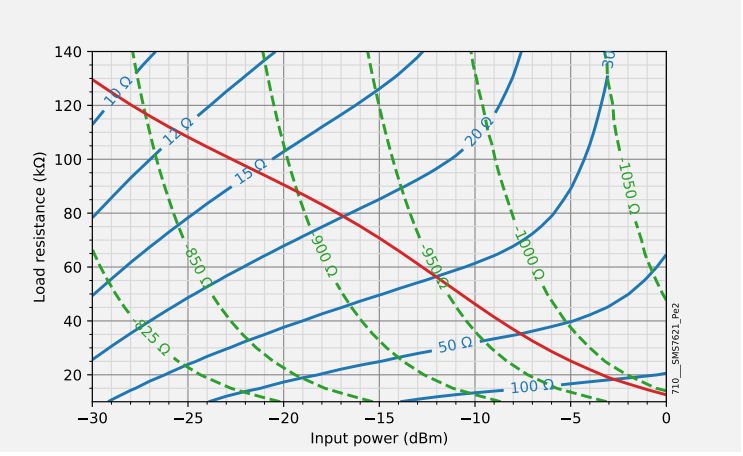
$$P_s = \frac{P_{in}}{G_{i,in}}. \tag{4.59}$$

Fig. 4.31 shows in (a) the impedance mismatch loss factor versus *source* power level, for both the 40 kΩ fixed load resistance case as for the optimal

[11] Which would relate to the power coming from e.g. an antenna.



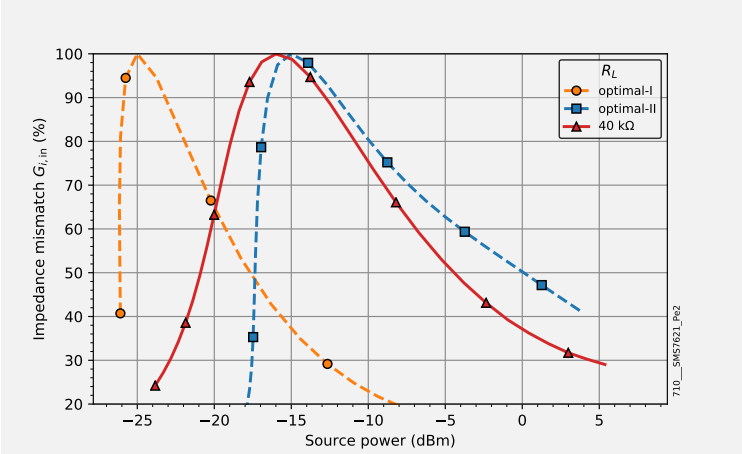
(a) Load resistance for optimal efficiency η_2 curve (red) and efficiency loss L_η contours for an arbitrary load resistance (blue).



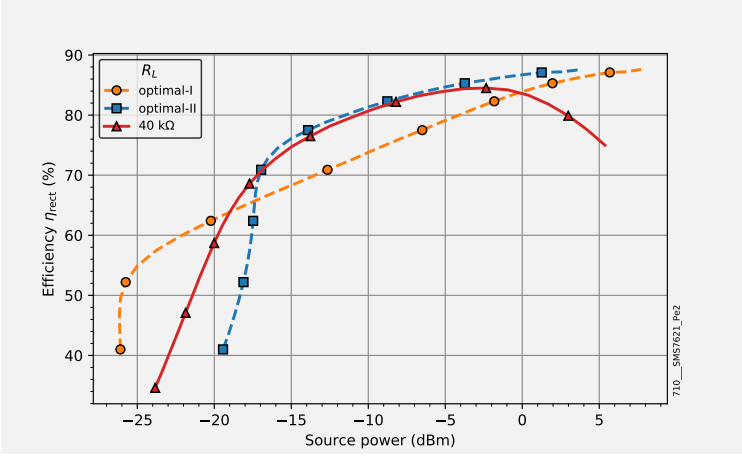
(b) Load resistance for optimal efficiency η_2 curve (red) and rectifier input impedance Z_{rect} contours for a arbitrary load resistance: real (blue) and imaginary values (green dashed).

Figure 4.30 Load resistance for optimal efficiency together with (a) efficiency loss L_η and (b) rectifier input impedance Z_{rect} for a varying load resistance R_L, of an ideal single diode peak detector rectifier configuration, using an SMS7621 SBD. Simulated at f_0 = 868 MHz using the Sischka model including diode package.

efficiency case with different reference impedances chosen (optimal-I: $Z_0 = 12.3 + 862\,j\ \Omega$, optimal-II: $Z_0 = 23.0 + 930\,j\ \Omega$, and for $R_L = 40$ kΩ a reference impedance of: $Z_0 = 35.0 + 900\,j\ \Omega$). In Fig. 4.31 (b) the corresponding efficiencies are shown, also versus *source* power level. This graph shows the impact of choosing a fixed- or optimal load impedance and also the choice for reference impedance, i.e. the impedance on which the impedance matching circuit is based. The efficiency curves shown, are equal to Fig. 4.28 — they are only shifted to the right by a varying amount. This shift is input power dependent, and calculated in dBs as $10\log_{10}(L_{i,\text{in}})$.



(a) Impedance mismatch.



(b) Efficiency.

Figure 4.31 For the optimal load resistance case and a fixed load resistance (R_L = 40 kΩ), in (a) the impedance mismatch and in (b) the efficiency is shown for an ideal single diode peak detector rectifier, using an SMS7621 SBD. Simulated at 868 MHz using the Sischka macro model including diode package. The corresponding reference impedance chosen is for optimal-I: $Z_0 = 12.3 + 862\,j\ \Omega$, optimal-II: $Z_0 = 23.0 + 930\,j\ \Omega$ and for $R_L = 40$ kΩ: $Z_0 = 35.0 + 900\,j\ \Omega$.

4.7 Summary and Conclusions

In this chapter we discuss the WET rectifier energy transfer efficiency and show how the diode characteristics relate to this. The main conclusions are:

a) The rectifier load resistance has an effect on the rectifier input impedance. For the ideal diode model this is at high input power levels. In that regime we see: $R_j \propto R_L$, shown in the Load Experiment Fig. 4.6, described in Section 4.2. For the Schottky diode model, the same experiment is repeated in Section 4.5. This shows in Fig. 4.18 (b) that $R_j \propto R_L$ applies for input power levels between -20 and 0 dBm.

b) The diode saturation current also plays a role in the rectifier input impedance, at low input power levels for both the ideal and Schottky diode model. In that regime we see: $R_j \propto 1/I_s$. For the Schottky diode model, the rectifier input impedance is also determined by the diode saturation current at high input power levels, but is also input power dependent. See Fig. 4.18.

c) An adaptive source is required for proper efficiency optimization of a non-linear rectifier circuit.

d) A clear relation is seen between diode junction voltage and circuit input power on one hand and rectifier efficiency, optimal load resistance and circuit input impedance on the other hand.

e) A clear difference exists between the results obtained with an ideal SPICE diode model and a realistic SBD model, for circuit input impedance and energy transfer efficiency.

f) When using a fixed rectifier load resistance and a range of input power levels, it is useful to define and analyse the efficiency loss. This to find the optimal load resistance value.

g) The choice of diode type, more specifically the I_s and R_s value, is dependent on the design requirements. The effect of R_s is frequency and input power dependent. A low I_s value increases efficiency in the low input power regime.

h) Designing an efficient rectifier for a larger input power range can be done using a varying optimal load resistance or a fixed load resistance. Depending on the range of input power levels, the latter can outweigh the former approach.

Chapter 5

Rectifier Circuits

In this chapter we compare different basic rectifier configurations. This provides insight in how beneficial topology choices can be for the rectifier efficiency. For objective rectifier circuit topology comparison, the complex conjugately matched source (P_{CCM}) method is used in this chapter, to ensure an equal input power situation. The circuit load is optimized for maximum energy transfer efficiency. The details on these methods are discussed in chapter 2.

Due to the chosen complex conjugately matched source technique, the rectifiers do not need to be input impedance matched with the source. This enables a proper comparison over a wide range of input power — the input impedance typically varies significantly with input power. The input impedance should be matched differently at each input power level, when using a normal fixed impedance source. In chapter 6 a rectifier example will be shown including a matching circuit.

To obtain a high energy transfer efficiency at low input power levels, designers often tend to choose a diode with a low forward voltage specification for a given current , e.g. [107]. As discussed in chapter 4, such a diode corresponds to a high saturation current I_s, which doesn't result in an optimal efficiency performance versus input power level. In this chapter the difference between two different diode types[1] becomes more visible, when comparing different rectifier topology efficiencies.

[1] The diode types are: the Skyworks SMS 7621 and the Avago HSMS-2852, with a low respectively high saturation current. See tabel 3.2 for an overview of the SPICE model parameters of these diodes.

5.1 Topology Comparison

In the previous chapters, the rectifier theory is mainly build around the single diode peak detector topology, abbreviated as **Pe**. This circuit is used for decades for peak detection and demodulation purposes, but serves also as a WET rectifier circuit. This configuration will be compared with several other rectifier families: the Villard rectifier (**Vi**) [108], the Greinacher voltage doubler (**Gr**) [109] and Graetz (**Gz**), diode-bridge or full-wave rectifier [110]. See Fig. 5.1 for examples of the different rectifier families.

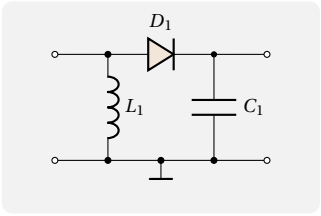
The rectifying diodes are modelled using the Sischka macro model (chapter 4, tables 3.8 and 3.9 and Fig. 3.15) for two different SBDs: the SMS 7621 and HSMS-2852. For some circuit topologies, also the ideal diode model is used, using the specific SBD saturation current value and the ideal diode parameter values $n = 1$, $R_s = 0$ and $C_j = 0$, see Fig. 5.2. The purpose is to show the theoretical maximum efficiency limit, for that particular topology.

All circuits in this chapter are simulated using ADS with the non-linear HB engine. For the simulations, the following parameter values are used: $f_0 = 1$ MHz, number of harmonics[2] $n = 35$, the adaptive source impedance Z_s is equal to the diode small signal junction resistance[3], see eq. (4.28). Fig. 5.2 provides and overview of the ideal circuit components, used in the ADS simulations, together with the circuit schematic equivalent components, used in the different rectifier topologies overview to be discussed next.

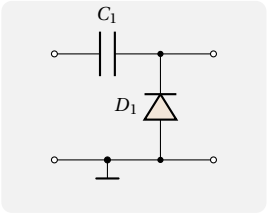
The different topologies contain frequency selective elements: ideal filters. These are defined in the frequency domain, using ADS' Z1P_eqn component which is an equation defined impedance. They refer to an IF-THEN-ELSE equation shown in the 'VAR' block. E.g. Z_F1 has an impedance of 10^{-10} Ω at f_0 and 10^{10} Ω for other frequencies. For these ideal filters, the frequency domain harmonic number h is shown below the filter, to be passed through or being blocked, depending on the filter type. A bandpass filter with $h = \{1\}$ means that only the fundamental frequency f_0 is passed through. The variation in the configurations shown is not complete: more combinations are possible.

[2] Using 35 harmonics is seen as a good compromise between obtaining an accurate enough result and having sufficient simulation convergence, for all configurations analysed.

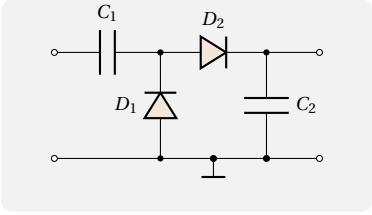
[3] This value of $\lim_{V_j \to 0} R_j = \frac{nV_T}{I_s}$ results in converging optimization over the complete input power range of $\{-60 \cdots +30\}$ dBm. E.g. $Z_s = 50$ Ω results in HB solver convergence issues.



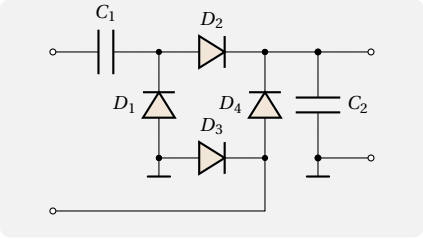
(a) Peak detector (Pe) family.



(b) Villard (Vi) family.



(c) Greinacher (Gr) family.



(d) Graetz (Gz) family: diode-bridge or full-wave rectifier.

Figure 5.1 Examples for the different detector rectifier families, with the abbreviation used in parentheses.

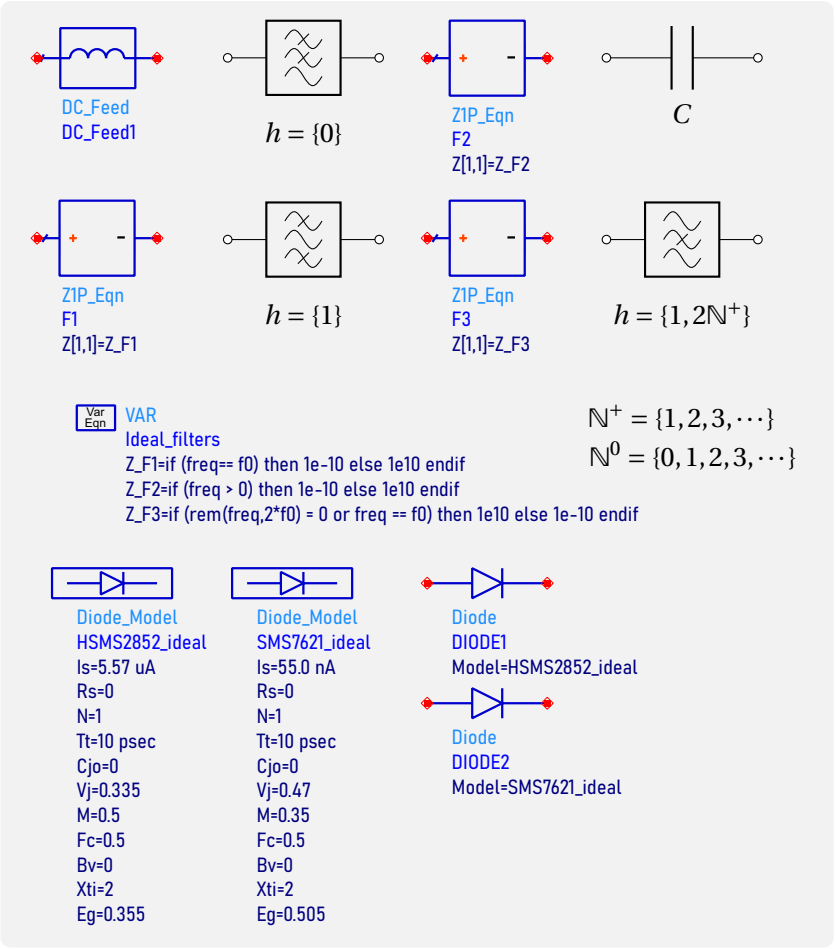


Figure 5.2 ADS implementation of the ideal circuit components (blue) and the circuit schematic equivalent components (black) used in the different rectifier topologies overview to be discussed next. For the ideal filters, the frequency domain harmonic number(s) h are shown to be passed through or being blocked, depending on the filter type. The non-ideal SBDs (not shown in this figure) are modelled as shown in table 3.8 and 3.9 and Fig. 3.15.

5.2 Peak Detector

The basic peak detector topology, indicated as Pe1, is shown in Fig. 5.3 (a) and is sometimes called a class-C rectifier for its zero dc-bias voltage at the diode's anode by using a dc-short to ground (the lowpass, $h = \{0\}$-filter). This element is used to avoid the dc-current passing through the source-resistance causing unwanted loss of energy. Often the function is filled in by a shunt inductor, being part of the input impedance matching circuit.

The Pe2 variation shown in sub-figure (b) is an improved form of Pe1 and corresponds to the ideal rectifier circuit described in section 2.2.1. To compare the performance, Fig. 5.4 shows the rectifier efficiency of the different topologies for (a) the SMS 7621 and in (b) for the HSMS-2852 SBD.

Another derivation to the rectifier topology can be made using harmonic load termination. In amplifier design, the use of a harmonic load termination is used to improve the amplifier efficiency, e.g. [111, 112] describe the class-F type amplifier. A similar approach is used in rectifier designs, e.g. [41] describes an inverse[4] class-F amplifier (F^{-1}). In this case, the odd-harmonic frequencies are shorted to ground and the even ones are allowed to pass between source and rectifying diode. This class-F^{-1} rectifier is shown in Fig. 5.3 (c). Pe2 and Pe3 perform almost equal, except for the high drive levels, where Pe3 outperforms Pe2, see Fig. 5.4. The drawback is that Pe3 requires more components to implement.

Shorting only the odd harmonics at the output of the rectifier doesn't work well, as shown with variant Pe4 in Fig. 5.3 (d), see Fig. 5.4.

The implementation of Pe5, as shown in Fig. 5.3 (e), doesn't result in an optimal efficiency as shown in Fig. 5.4 (a) and (b).

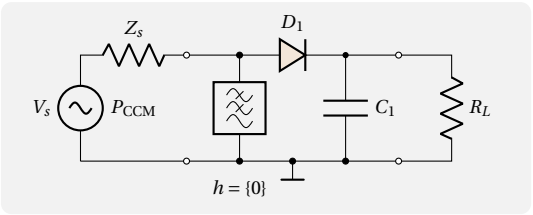
The difference between class-F amplifier and -rectifiers is that in the case of the amplifiers the voltage and current are 180° out of phase and result in a zero voltage-current product for the harmonics. In case of the rectifier, they are in-phase (more or less, as reactive parasitics will introduce a slight shift depending on the frequency used). If a harmonic term is not shorted, the voltage-current product will be non-zero and represent energy, not ending up in the dc-term. Therefore no significant improvement is seen in rectifier efficiency. In this case the class-C and class-F^{-1} filters present only a *zero*- or *infinite* resistance for a harmonic term. It would also be possible to optimize the harmonic term *amplitudes*, like described in [111], but this is not taken into account in this work.

Making use of the measured diode performance spread information, resulting in a minimum and maximum fitted model as shown in table 3.8 and 3.9,

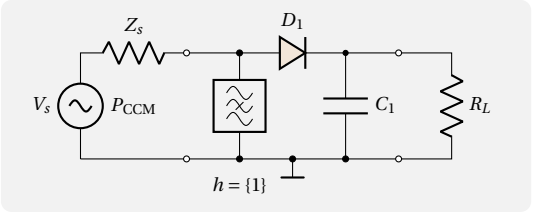
[4] In an RF to dc converting rectifier, the usage of a frequency selective filter at the output doesn't work. Therefore the filter is used at the RF input side – hence the usage of 'inverse'.

the corresponding Pe2 spread in rectifier efficiency is simulated[5]. The result is shown in Fig. 5.4 (c)[6]. On top of this efficiency spread, the spread on the other rectifier (lumped-) component values will add variation. Comparing the spread for the different topologies, adding this additional spread, doesn't show a different order in performance between the variants.

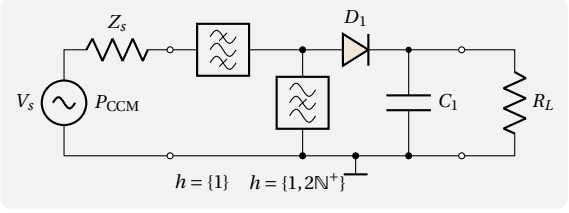
As expected from chapter 4, the SBD SMS 7621 diode with lower I_s value, outperforms the HSMS-2852 one, having a higher I_s value.



(a) Pe1: class-C rectifier, with dc-short at input, shorting $h = \{0\}$ to ground.



(b) Pe2: shorting all but $h = 1$ at input.

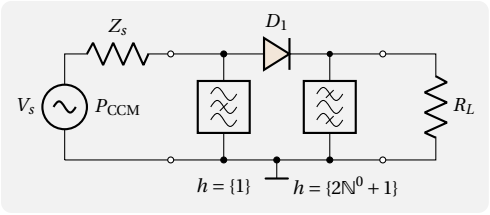


(c) Pe3: class-F^{-1} rectifier, passing f_0 and shorting dc and odd h to ground, at input.

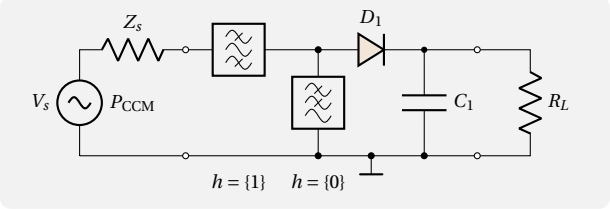
Figure 5.3 The single diode peak detector rectifier family.

[5]Note that this spread is taken from a limited number of ten samples. Real spread is expected to be larger.

[6]In this simulation, the optimal achievable efficiency is calculated for the three cases: the three cases have different load resistances. This is not the same as keeping the load resistance values equal to the nominal case, when simulating the maximum and minimum cases.

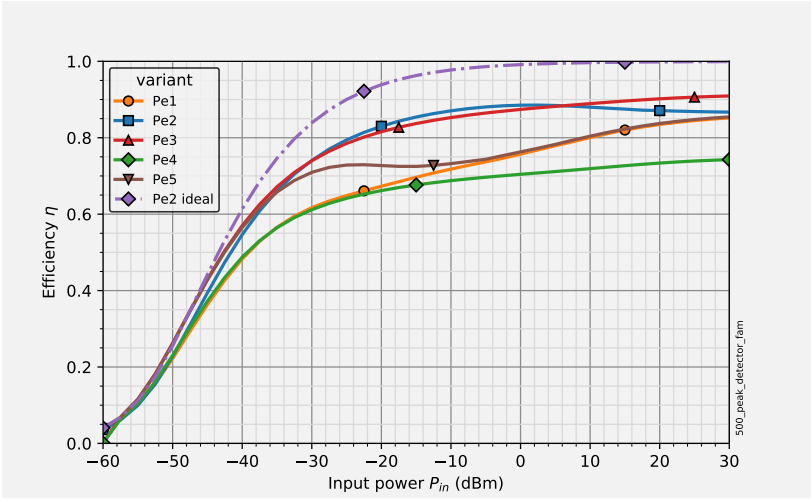


(d) Pe4: shorting all but $h = 1$ at input, shorting odd h at output.

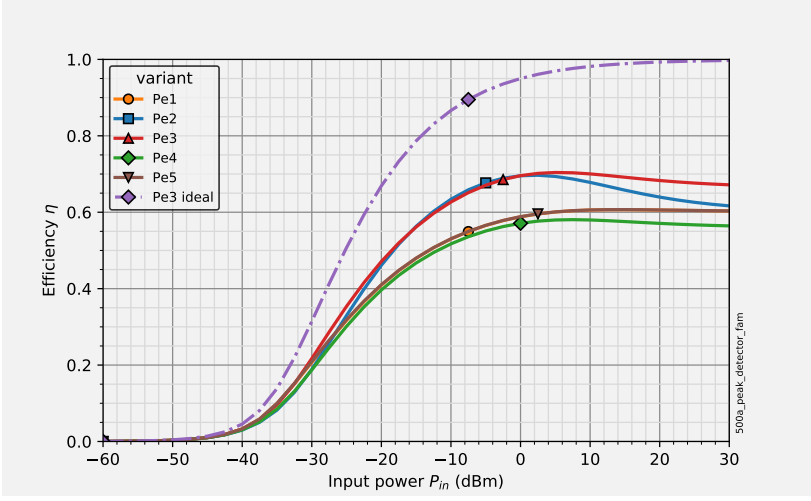


(e) Pe5: passing f_0 and shorting dc to ground, at input.

Figure 5.3 The single diode peak detector rectifier family.

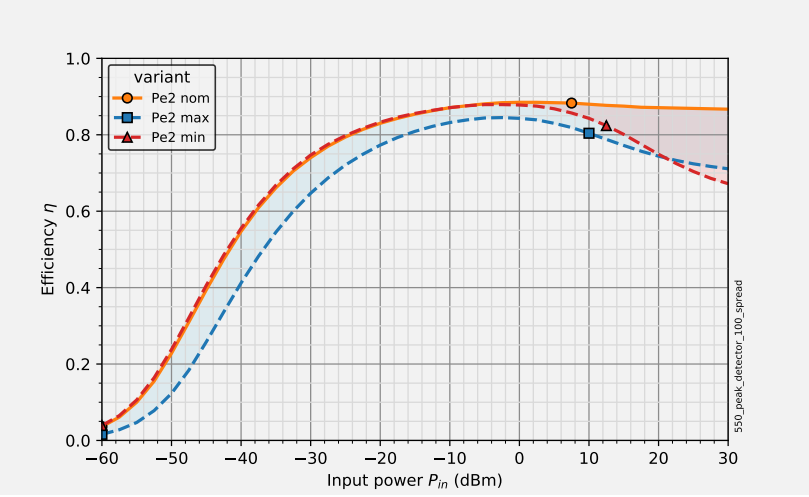


(a) SMS 7621.



(b) HSMS-2852.

Figure 5.4 Peak detector rectifier family efficiency, shown for (a) the SMS 7621 and (b) the HSMS-2852 and (c) the expected efficiency spread using the nominal, minimum and maximum SMS 7621 models (see tables 3.8 and 3.9).



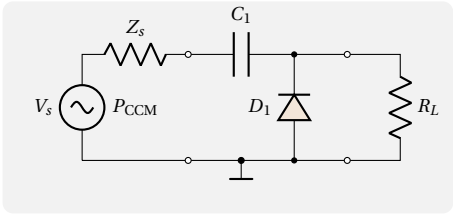
(c) SMS 7621 Pe2 spread.

Figure 5.4 Peak detector rectifier family efficiency, shown for (a) the SMS 7621 and (b) the HSMS-2852 and (c) the expected efficiency spread using the nominal, minimum and maximum SMS 7621 models (see tables 3.8 and 3.9).

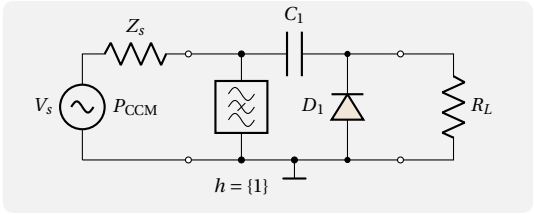
5.3 Villard

The Villard topology looks of similar complexity as the peak detector one, and is shown in Fig. 5.5. An advantage is its build-in dc-block capacitor and no need for an input dc-path to ground, as the diode is connected to ground itself. A drawback of this circuit is the large ac voltage swing on the output. Only the Vi3 and Vi4 types have a flat load voltage characteristic due to the output filter. These variants are also the most efficient ones of the four types, as shown in Fig. 5.6.

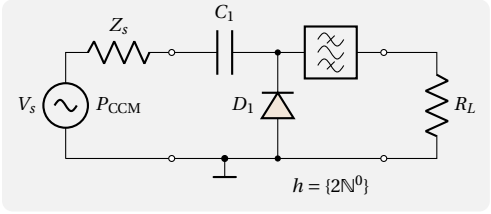
Also for the Villard topology, the SBD SMS 7621 diode with lower I_s value, outperforms the HSMS-2852 one, having a higher I_s value (like for the peak detector type).



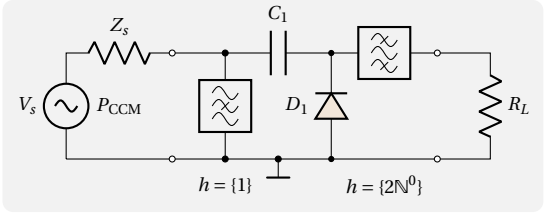
(a) Vi1: capacitor at input, blocking $h = 0$.



(b) Vi2: shorting all but $h = 1$ at input.

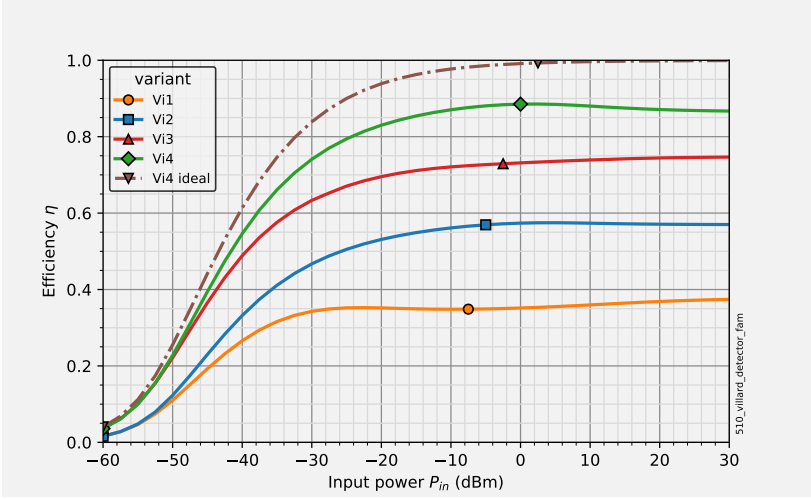


(c) Vi3: passing dc and even h at output.

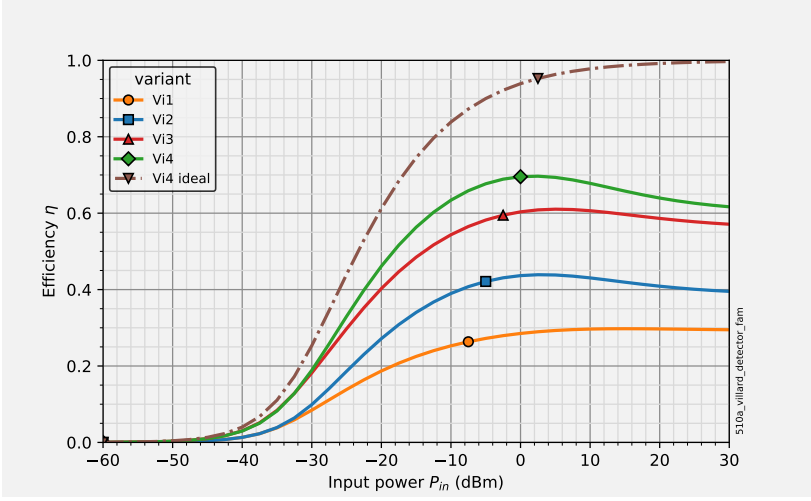


(d) Vi4: shorting all but $h = 1$ at input, passing dc and even h at output.

Figure 5.5 The single diode Villard rectifier family.



(a) SMS 7621.

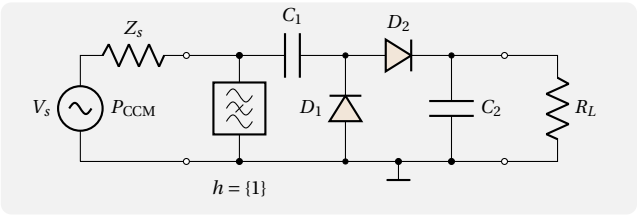


(b) HSMS-2852.

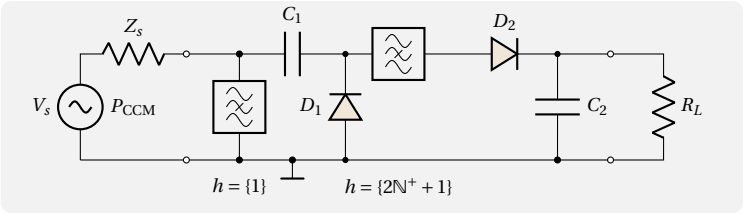
Figure 5.6 Villard detector rectifier family efficiency, shown for two different SBD's.

5.4 Greinacher

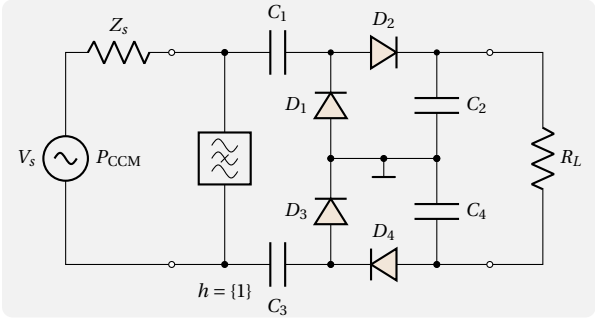
The Greinacher voltage doubler type of rectifier is shown in Fig. 5.7, with the voltage quadrupler variants in (c) and (d).



(a) Gr1: shorting all but $h = 1$ at input.



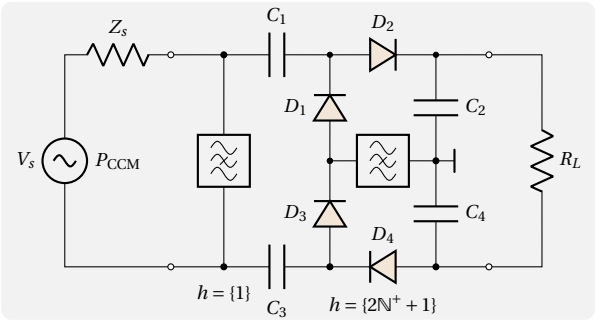
(b) Gr2: shorting all but $h = 1$ at input, blocking odd h to second stage.



(c) Gr3: shorting all but $h = 1$ at input.

Figure 5.7 The voltage doubler Greinacher rectifier family.

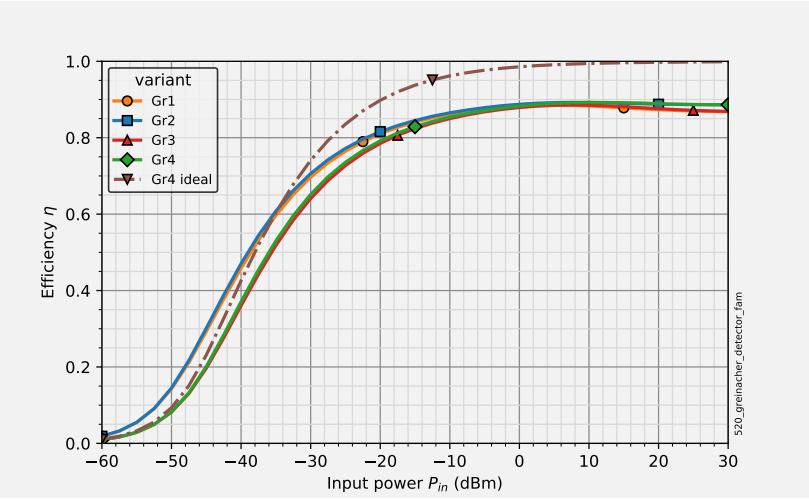
The resulting efficiencies are shown in Fig. 5.8. The Gr1 and Gr2 types perform best at the lower input power levels where Gr2 and Gr4 are the best at the high-end range. Although the output voltage doubling attracts designers to make use of this configuration, we will see later that, from an efficiency point of view, this type is not the best choice. A trade-off should be made, taking high-efficient dc-dc voltage-converters into account as well, when looking at a higher level system design.



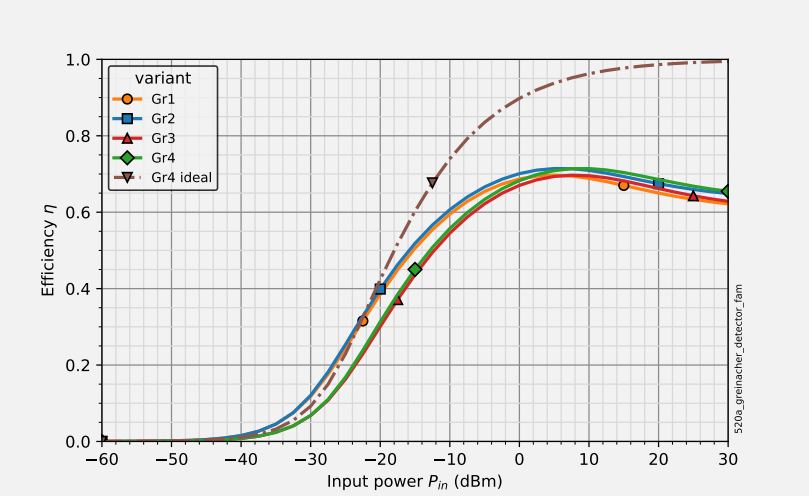
(d) Gr4: shorting all but $h = 1$ at input, blocking odd h to ground in centre.

Figure 5.7 The voltage doubler Greinacher rectifier family.

Like for the peak detector and Villard types, also for the Greinacher topology, the SBD SMS 7621 diode with lower I_s value, outperforms the HSMS-2852 one, having a higher I_s value.



(a) SMS 7621.



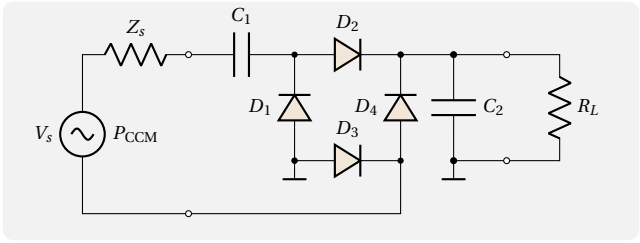
(b) HSMS-2852.

Figure 5.8 Greinacher detector rectifier family efficiency, shown for two different SBD's.

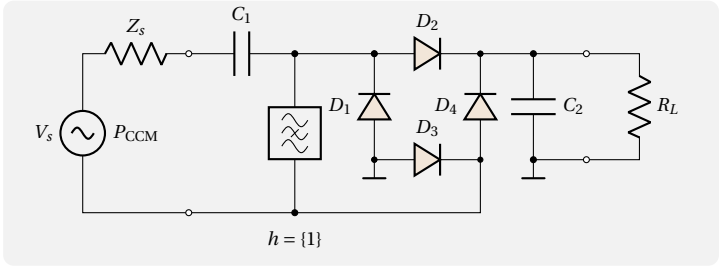
5.5 Graetz

The Graetz-, diode-bridge or full-wave rectifier topology is shown in Fig. 5.9. The resulting efficiencies as a function of input power are shown in Fig. 5.10. This configuration is commonly used in power supply rectification but also serves well in WET applications. The Gz3 variant is the best of the three, performing well both at low and high drive levels.

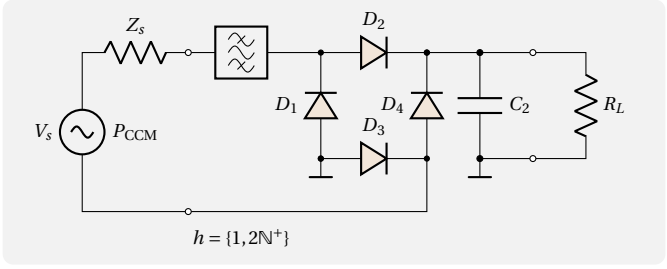
Also for the Graetz topology, the SBD SMS 7621 diode with lower I_s value, outperforms the HSMS-2852 one, having a higher I_s value (like for all three previous types).



(a) Gz1: blocking $h = 0$ capacitors only.

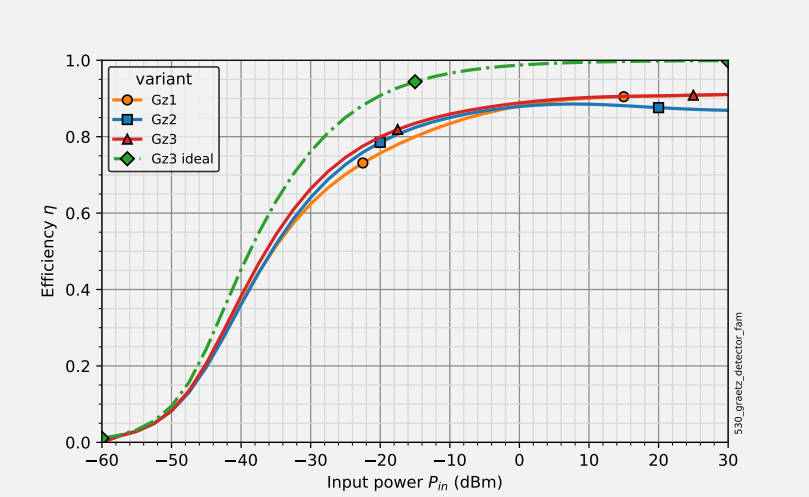


(b) Gz2: shorting all but $h = 1$ at input.

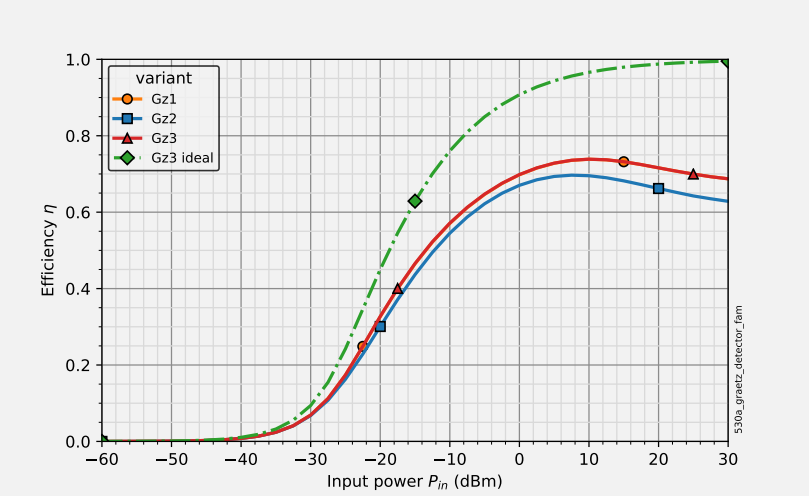


(c) Gz3: blocking dc and odd h at input.

Figure 5.9 The Graetz-bridge full-wave rectifier family.



(a) SMS 7621.



(b) HSMS-2852.

Figure 5.10 Graetz detector rectifier family efficiency, shown for two different SBD's.

5.6 Rectifier Family Comparison

A comparison of the best performing topologies from the different rectifier families is shown in Fig. 5.11, showing efficiency and load voltage as a function of input power[7]. In this comparison only the SMS 7621 diode is taken into account as the HSMS-2852 performs less efficient due to its larger I_s value. Fig. 5.11 (a) shows — for the low drive levels — that Pe2 and Vi4 are performing the best in terms of efficiency (they have an equal curve). For drive levels above 0 dBm, the Gz3 outperforms the rest although the Pe3 variant is equal at 30 dBm.

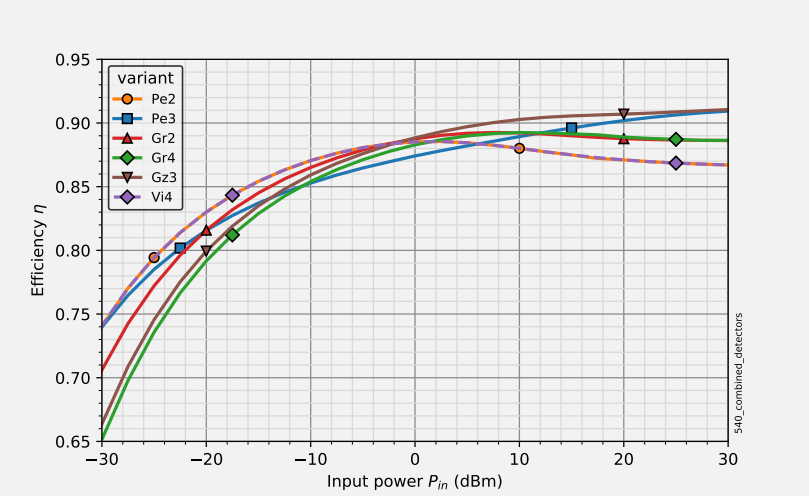
Looking at the load voltage in Fig. 5.11 (b), the Gr4 topology results in the largest voltage values.

Fig. 5.11 (c) shows the load resistance R_L as a function of input power, corresponding to the optimal efficiency η. Note the same order of topologies as for the load voltage graph in (b). The corresponding circuit input resistance versus input power is shown in Fig. 5.11 (d). The imaginary part is negligible at $f_0 = 1$ MHz. The ratio between the two resistances is shown in Fig. 5.11 (e). Note that the different rectifier families have different ratios — the Pe2 and Vi4 topologies correspond to the ideal peak detector curve, shown against junction voltage in Fig. 4.13, with a ratio of 2. The Gr4 topology has a ratio above 20, showing the lowest circuit input resistance. A lower ratio value results in less input impedance matching loss as this requires to bridge a smaller step between source- and circuit impedance by the impedance matching circuit. Therefore a trade-off has to be made between topology efficiency and -input impedance. Also the output voltage is part of the equation, as this plays a role in the power management between rectifier and loading circuit.

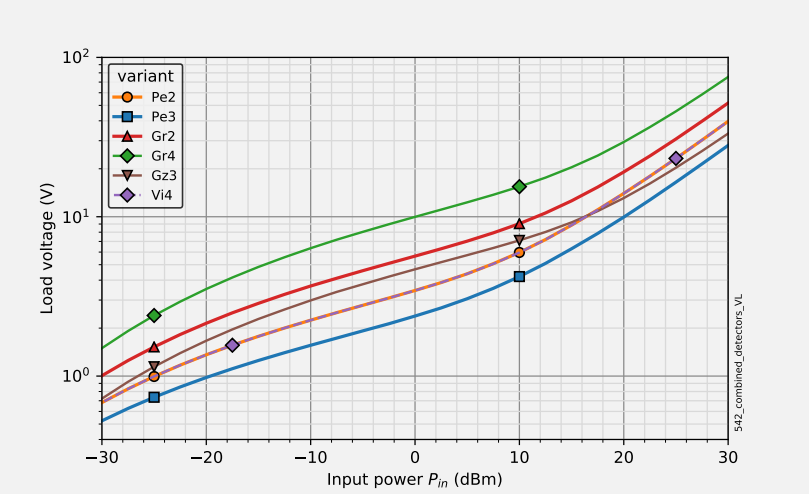
In some applications, different modes of operation are deployed with significant changes in load resistance and therefore rectifier input impedance. For example a rectifier charging a battery can be in normal charge- and trickle charge mode, typically having an order of magnitude difference in charge current and load resistance. This puts an extra challenge on the rectifier input impedance matching circuit. Changing rectifier topology when changing charging mode, can be a solution to obtain less mismatch loss on the rectifier input side.

To specify a topology's efficiency, it is not useful to use a single number, as the efficiency is input power dependent. It would be better to specify the efficiency for a specific input power range. E.g. in chapter 2 a useful WET range is

[7] Rectifier efficiency can also be presented in a graph which shows the breakdown between the contributing different rectifier circuit parts, see e.g. [113]. In this thesis the ideal rectifier is observed, without an input impedance matching network and other dissipating elements. This results in only two contributors for efficiency degradation: the voltage dependency of the diode junction potential and the non-ideal diode reverse bias characteristic. The difference between the two is made clear in Fig. 4.19.

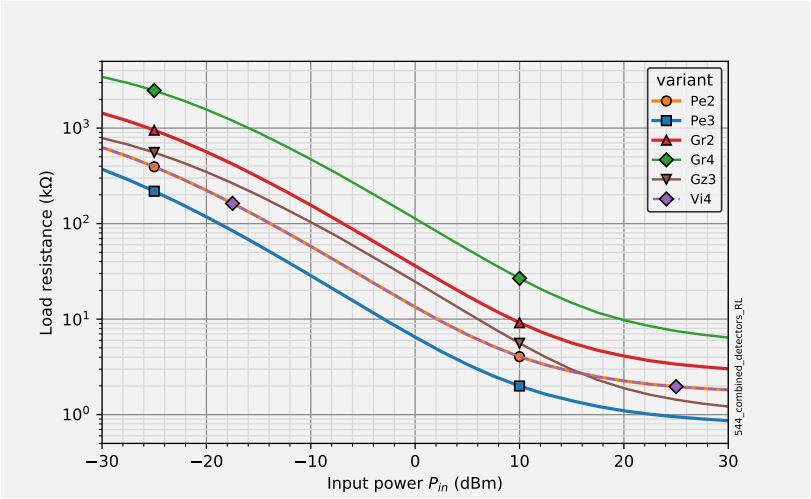


(a) Efficiency.

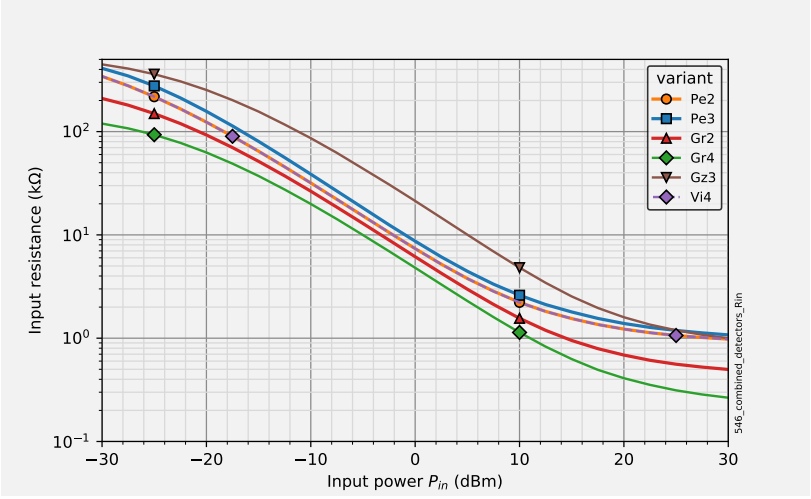


(b) Load voltage accross R_L.

Figure 5.11 A comparision of the different rectifier families, using the SMS 7621 diode for: (a) efficiency, (b) load voltage, (c) optimal load resistance, (d) corresponding circuit input resistance and (e) input- to load resistance ratio.

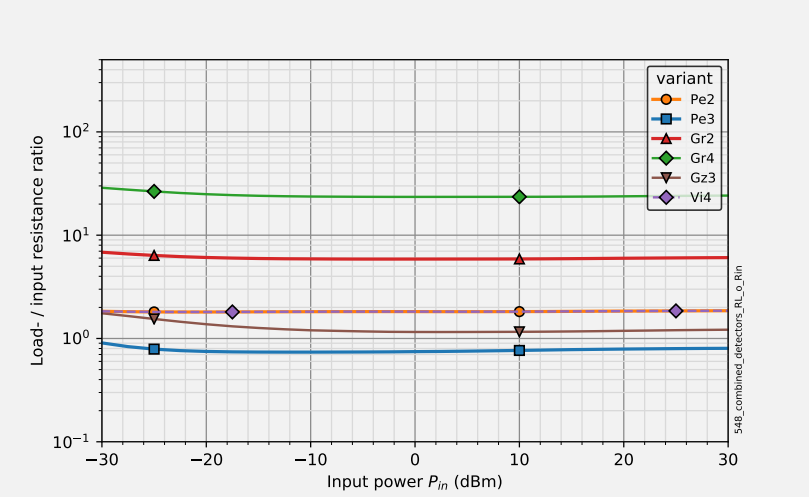


(c) Load resistance R_L.



(d) Circuit input resistance.

Figure 5.11 A comparison of the different rectifier families, using the SMS 7621 diode for: (a) efficiency, (b) load voltage, (c) optimal load resistance, (d) corresponding circuit input resistance and (e) input- to load resistance ratio.



(e) Load resistance to input resistance ratio.

Figure 5.11 A comparision of the different rectifier families, using the SMS 7621 diode for: (a) efficiency, (b) load voltage, (c) optimal load resistance, (d) corresponding circuit input resistance and (e) input- to load resistance ratio.

for input power levels between −15 and −5 dBm for a 915 MHz application. The minimal achievable efficiency over this range is, in that case, useful to specify for a rectifier topology, e.g. as $\eta_{-15\text{dBm}}$.

5.7 Summary

In this chapter different WET rectifier topologies have been discussed and compared. The main findings are:

a) The optimal performing rectifier configuration type is input power dependent, with respect to energy transfer efficiency.

b) The rectifying diode type plays a significant role in the efficiency, and more specifically: the saturation current of the diode.

c) The complexity of a topology plays a role: non-ideal components will add losses and parasitic behaviour. For small size applications the component area is also of importance.

d) The input matching circuit needs to be added, introducing extra loss and frequency dependency. The required impedance transformation factor is not equal for all topologies.

e) Comparing the different rectifier families, the input resistance varies more between the families than the efficiency.

Chapter 6

Far Field Application

This chapter provides a view on typical WET rectifier characterization work: work is shown with WSNs as WET application. A comparison is described between a commercial Powercast harvesting solution [114] and work carried out at imec in 2014 [40]. This shows the typical RF signal levels available at the input of a WET rectifier circuit, the available dc power to drive a connected electronic circuit and the resulting energy conversion efficiency. The topics of the corresponding load resistance and power management circuit are also discussed.

The only available commercial harvester, at that time, from Powercast [114] is compared to a discrete-rectifier from imec [40] (supplemented with a commercial power management circuit by Texas Instruments [115]). For the imec work, a frequency of 868 MHz (European short-range device (SRD) band) is chosen for its relatively high allowable transmit power and which results in favourable antenna dimensions against performance[1]. The Powercast system operates at 915 MHz (USA industrial, scientific and medical (ISM) band).

6.1 RF Harvesting System

Assumptions

As a starting point for the experiments, described in this chapter, the following assumptions are made:

- **protocol** the RF communication protocol, used by the radio system, foreseen to be connected to the RF harvester, will be according to the Institute of Electrical and Electronics Engineers (IEEE) 802.15.4g standard [116].

[1] The regulations have changed over time. In 2021 different restrictions apply, see the European Communication Committee (ECC) Recommendation 70-03 [10].

Table 6.1 Frequency Band Allocations and Transmit Power Restrictions for radio-frequency identification (RFID) Applications.

Frequency band	Power level	Region
865.0 – 865.6 MHz	100 mW ERP	Europe
865.6 – 867.6 MHz	2 W ERP	Europe
867.6 – 868.0 MHz	500 mW ERP	Europe
902.0 – 928.0 MHz	4 W EIRP	USA, Canada
2400.0 – 2483.5 MHz	4 W EIRP	USA, Canada
2400.0 – 2483.5 MHz	10 mW EIRP	Japan, Korea
2446.0 – 2454.0 MHz	4 W EIRP[1]	Europe[2]

[1] effective isotropic radiated power (EIRP) is the transmit power multiplied by the gain of the transmit antenna. EIRP is 1.64 times effective radiated power (ERP).
[2] Power levels above 500 mW are restricted to use inside the boundaries of a building and the duty cycle of all transmissions shall in this case be ≤ 15 % in any 200 ms period.

- **packet** a packet is assumed with 108 bits payload data and 392 bits overhead at 50 kb/s.
- **on-time** this leads to an on-time of 10.0 ms, which is used as pulse duration in the case of a so called dynamic load.
- **energy consumption** the maximum energy consumption is dominated by the transmitter of the radio system, consuming 50 mW of power, although this can be scaled down by lowering the RF output power of the system.

When making use of RF energy transfer, the regulations set in a specific region of the world should be followed. From [39] table 1, the allowed power level restrictions are found as listed in Table 6.1.

For USA/Japan/Europe coverage, the best choice is using 868 and 900 MHz where 2 W respectively 4 W is allowed. For 2.4 GHz this is restricted to 10 mW for Japan and 600 mW for Europe (15 % of 4 W).

Controlled RF environment

Radiative WET used in an indoor environment will be subject to different forms of fading effects.

In order to get an idea of available signal levels at the receiving side in an wireless indoor environment, an available-power measurement is performed in a large office hallway. Two different antennas — a 1.0 dBi ground-plane and a 6.1 dBi patch type (both commercial Powercast antennas [117]) — are used on the receiving side, connected to a power sensor. On the source side, a 3 W EIRP commercial Powercast transmitter with build-in patch antenna is used at a frequency of 915 MHz. The measurement results are provided in Fig. 6.1. We see that even in a large indoor room we will have fading effects. As can be conducted from this experiment, to achieve power transfer over distances between 5 and 10 meter, a system operating at power levels between −15 and −5 dBm on the receiver side will cover most situations. The dashed predicted curves are calculated using Friis' free-space transmission equation [118].

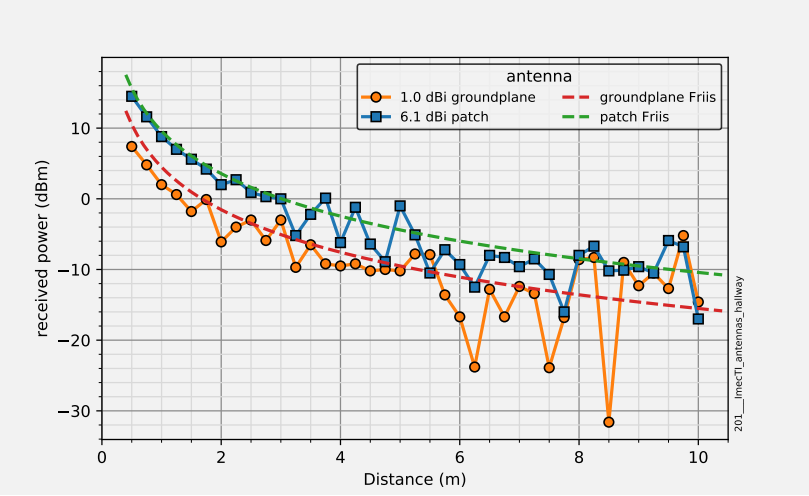


Figure 6.1 Measured indoor (hallway) received power at 915 MHz, using a 1.0 dBi groundplane and 6.1 dBi patch antenna on the receiving side and a 3.0 W effective isotropic radiated power (EIRP) transmitter. The expected received power levels, based on a free-space assumption using the Friis equation [118], are also shown (dashed).

For reproducibility, a controlled RF environment is used in this work, by making use of a wired connection between the source and receiver and controlling the source output power level[2].

[2] Actually the receiver input power is controlled as that is the difficult to control one in a wireless

The following characterization experiments are done in a wired set-up, using a signal source connected to the RF energy receiver by a coaxial transmission line. Fig. 6.2 shows a block-diagram used to characterize a combination of RF matching and rectifier circuit with a voltage boost/buck-converter with energy storage and a dynamic load at the output of this converter. This load is used to emulate a typical wireless sensor node, which will have a specific energy consumption pattern in time.

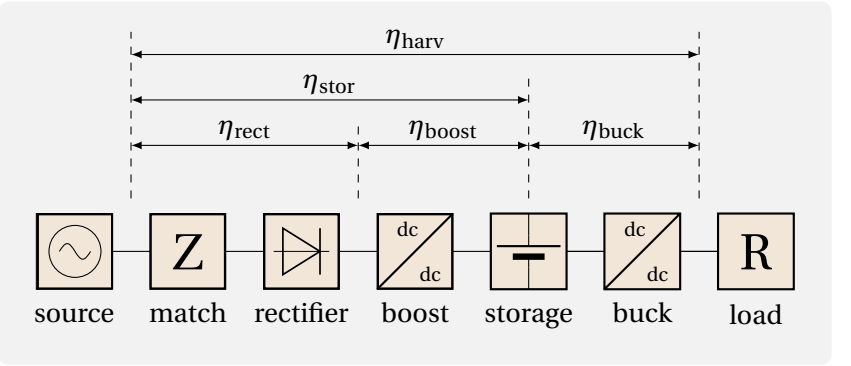


Figure 6.2 Block diagram of a practical WET test-setup. The source represents an RF signal generator (source), connected to the impedance matching network (match). The rectifying circuit (rectifier) is followed by a boost converter to increase to voltage level (boost) for efficient storage in a capacitor or battery (storage). This voltage is brought down by a buck converter (buck). The load is a dynamic load (load), controlled by e.g. an Arduino® microcontroller. The different η's represent power conversion efficiencies and are explained in the next section.

6.2 Rectifier Comparison

In this section, two rectifier designs will be compared: a discrete rectifier, designed at imec in 2014 and a discrete rectifier, made commercially available by Powercast Corporation. Around 2014, the Powercast solution was the only commercial design available on the market. Five years later, they still have the same design and performance available, only some other frequency band versions where added in the mean time. Therefore the comparison is still relevant.

connection. As the source has a wired connection with the receiver input, both are the same in this controlled RF environment.

6.2.1 Powercast discrete rectifier

The COTS RF harvesting product is a Powercast discrete rectifier P2110CSR evaluation board [114] containing an impedance matching circuit, two parallel rectifiers, a voltage boost converter and energy storage capacitors, together with a Powercast Battery Charging Board (BAT-EVAL-01, not available anymore) containing a circuit producing a constant output voltage. The schematics of the matching circuit with rectifiers is shown in Fig. 6.3, the corresponding PCB layout in Fig. 6.4. This product is designed for 915 MHz (USA available license-free ISM frequency band). In the measurements, this frequency is used for the Powercast circuit, where for the imec designs the European license-free ISM frequency of 868 MHz is used.

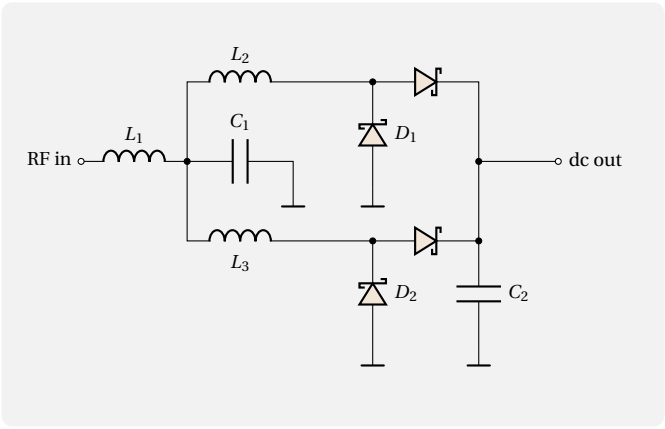


Figure 6.3 Impedance matching and rectifier circuit of Powercast P2110CSR evaluation board, with undisclosed diode type.

6.2.2 Imec discrete rectifier

At imec a discrete RF harvesting rectifier is designed, including an antenna-to-rectifier matching circuit. The circuit consists of an Avago Technologies HSMS-2852 Schottky diode pair and some discrete surface-mounted device (SMD) components. Fig. 6.5 shows a photograph of the fabricated prototype of the matching and rectifier block. The schematic diagram is shown in Fig. 6.6. The left section contains the impedance matching network which is designed to transform the rectifier input impedance towards 50 Ω at the circuit input side at 868 MHz. The right section is a voltage doubler rectifier topology.

The imec rectifier circuit is connected to a COTS Texas Instruments power management circuit BQ25570 [115]. Fig. 6.7 (a) shows the circuit diagram of

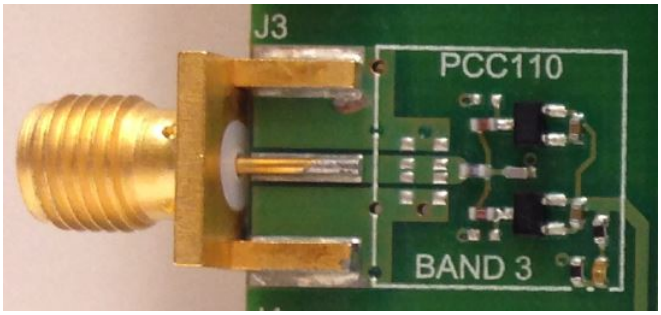


Figure 6.4 Powercast P21XXCSR-EVB evaluation board rectifiers with matching stage, having the same topology and layout as on the P2110CSR evaluation board used in this work.

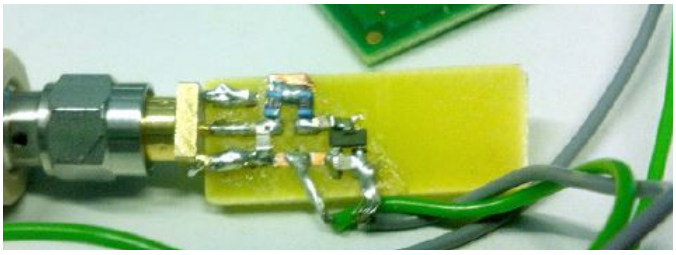


Figure 6.5 Imec matched-rectifier: impedance match and rectifiers in a voltage doubler configuration, prototype on a PCB.

the rectifier circuit connected to the Texas Instruments (TI) BQ25570 power management chip in a circuit diagram and Fig. 6.7 (b) the corresponding PCB application with antenna [12, 119]. The antenna is directly conjugately matched

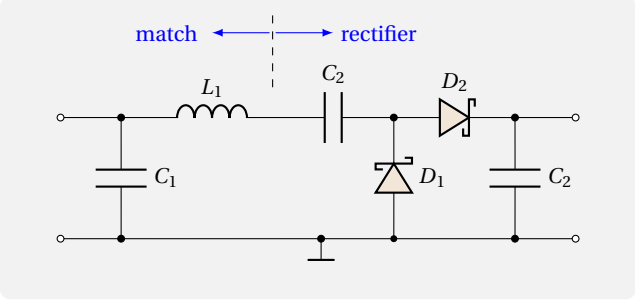
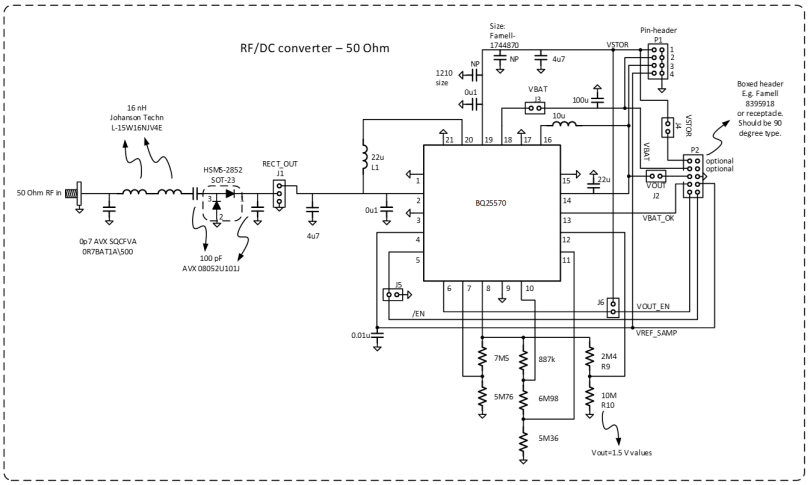
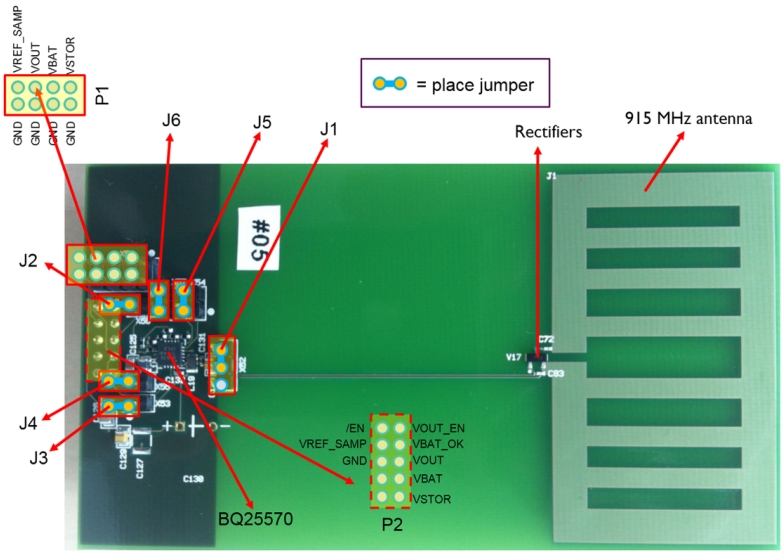


Figure 6.6 Imec matched-rectifier: impedance match and rectifiers in a voltage doubler configuration, circuit diagram with an Avago Technologies HSMS-2852 Schottky diode pair.

to the rectifier. So on the PCB shown in Fig. 6.7 (b) a matching network is not present. Using resistors (R9 and R10), see Fig. 6.7 (a), the output voltage of the TI chip can be determined, on which the load circuitry should run.



(a) Circuit diagram.



(b) PCB application including a 915 MHz antenna.

Figure 6.7 Imec discrete RF energy harvester with TI BQ25570 power management circuit: (a) Circuit diagram, (b) PCB.

TI's BQ25570 is a highly integrated energy harvesting management solution

that is well suited for meeting the special needs of ultra-low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (μW) to milliwatts (mW) of power generated from a variety of dc sources. The BQ25570 is the first device of its kind to implement a highly efficient boost charger with a nano-powered buck converter targeted toward products and systems, such as WSNs which have stringent power and operational demands. The design of the BQ25570 starts with a dc/dc boost converter/charger that requires only microwatts of power to begin operating. Once started, the boost charger can effectively extract power from low voltage output harvesters. The boost charger can be started with V_{in} as low as 330 mV, and once started, can continue to harvest energy down to V_{in} = 100 mV.

The BQ25570 implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the power management circuit. The BQ25570 periodically samples the open circuit input voltage every 16 seconds by disabling the boost converter for 256 ms and stores the programmed maximum power point (MPP) ratio of the connected input voltage to the open circuit (OC) voltage on an external reference capacitor at pin name `VREF_SAMP`, see Fig. 6.7 (a). While the storage element voltage is less than the user programmed maximum voltage (`VBAT_OV`), the boost converter loads the rectifier output capacitor until the regulator input voltage (pin 2, see Fig. 6.7 (a)) reaches the MPP (voltage at `VREF_SAMP`, pin 4). This results in the boost converter regulating the input voltage of the converter until the output reaches `VBAT_OV` (pin 7), thus transferring the maximum amount of power currently available per ambient conditions to the output.

In a practical application, the energy consuming application will not operate in a continuous mode. Duty cycling is a common practice. The corresponding power consumption is drawn in Fig. 6.8. Typically, a limited amount of energy is available, therefore energy storage is in most cases a necessity. In low data rate wireless sensor node applications, the energy can be stored in a capacitor. The amount of energy available from a charged capacitor E_{cap} is equal to

$$E_{\text{cap}} = \int_{Q1}^{Q2} V \, \mathrm{d}q = \int_{Q1}^{Q2} \frac{q}{C} \, \mathrm{d}q = \frac{1}{2C}(Q_2^2 - Q_1^2) = \frac{1}{2}C(V_2^2 - V_1^2), \tag{6.1}$$

where V_1 and V_2 are the capacitor voltage levels after and before the energy is taken out and C is the capacitance value. A higher capacitor voltage corresponds to more available energy. The required capacitance can be calculated using

$$C \geq \frac{P_{\text{dc}} T_{\text{on}}}{0.5(V_2^2 - V_1^2)}, \tag{6.2}$$

with P_{dc} being the foreseen dc-power consumption of the load connected to the energy harvester.

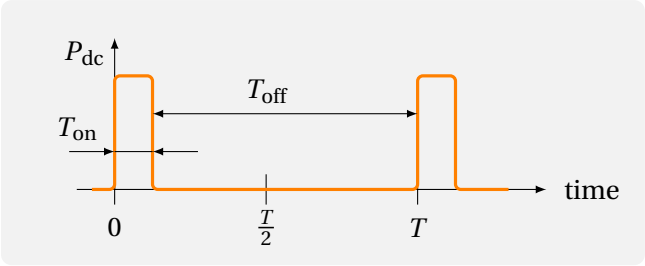


Figure 6.8 Time diagram of dynamic load dc power consumption with period T.

6.3 Dynamic Load

To put the harvesting system in a real state of operation, an energy consuming load should be connected with a non-constant time behaviour, like a wireless sensor node. To be flexible and to provide the ability of loading the system with a specific current profile, a dynamic load is build consisting of seven resistors selectable by BS170 field effect transistors (FETs) as shown in Fig. 6.9. The resistors $R_0, \ldots, R_6$ have decreasing values of 750, 360, 180, 91, 47, 22 and 11 Ω. The load can be controlled using seven lines named $b_0, \ldots, b_6$. This enables binary resistance-FET combining providing 128 different resistance values. The load is controlled using an Atmel® ATmega2560 microcontoller on an Arduino® MEGA board [120]. The lowest bit b_0 is controlling R_0 (750 Ω) and selecting the lowest current amount. Similarly bit b_6 controls R_6 (11 Ω) for the largest current amount. A specific current value can now be programmed in a binary fashion. For example, a binary code of 0000101 will select both R_0 and R_2 in parallel.

Using the Processing based Arduino software, a sequence of different resistor combinations can be repeated in a loop structure, mimicking a wireless sensor node system load [30]. For the RF harvester characterization experiments, the dynamic load is programmed for one specific resistance value only combined with a specific duty cycle, such that the complete system of harvester, power management, energy storage and load are in an energy equilibrium.

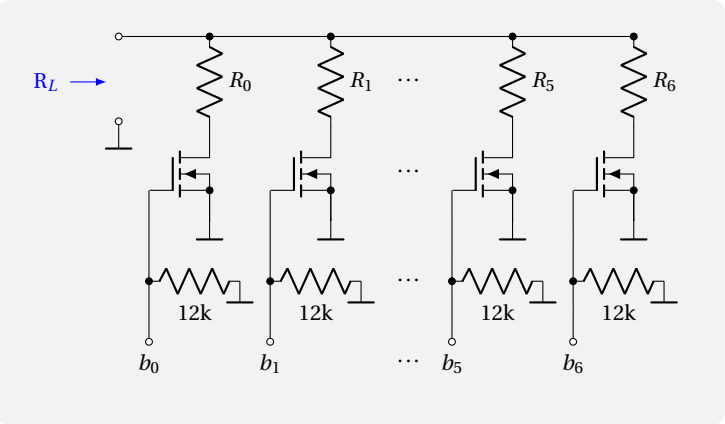


Figure 6.9 Dynamic load consisting of seven BS170 FETs, with 12 kΩ pull-down resistors and resistors $R_0, \ldots, R_6$ ranging from 750 to 11 Ω, selectable by seven (active high) lines named $b_0, \ldots, b_6$.

6.4 Practical WET Application

For practical radiative WET usage, the average available dc output power and with that the system energy transfer efficiency are of most importance. Fig. 6.2 shows how different efficiencies are defined in the practical WET system.

For the efficiency measurement of the first, i.e. the impedance matching and rectifier, stage, the load impedance of this stage is required as a function of input power. The rectifier load impedance is the input impedance of the power management stage. As already mentioned, the BQ25570 makes use of a MPPT mechanism which stores the OC (no boost converter connected) input voltage (`VREF_SAMP`) at a capacitor. By measuring this voltage at different input power levels of the matched rectifier stage, the input power to open circuit output voltage characteristic of this stage is known. The BQ25570 controls the boost-converter input impedance by using a certain percentage of `VREF_SAMP`. In this measurement, a value of 50 % of the OC voltage is used.

As a second step, the matched rectifier stage is measured with a resistive load, of which the value can be controlled. We can determine the corresponding load resistance such, that the same rectifier output voltage is obtained for a specific RF input power level (being 50 % of the OC voltage). Fig. 6.10 presents the result of this measurement using the imec rectifier, showing a decreasing load resistance for the rectifier stage with increasing RF input power. The definition of the matched rectifier stage efficiency is

$$\eta_{\text{rect}} = \frac{P_L}{P_{\text{in}}} = \frac{V_L^2}{R_L P_{\text{in}}} \tag{6.3}$$

with P_L being the rectifier dc output power, V_L the rectifier dc output voltage (equal to half of the OC voltage measured on the MPP voltage storage capacitor) and R_L the load resistance of the rectifier.

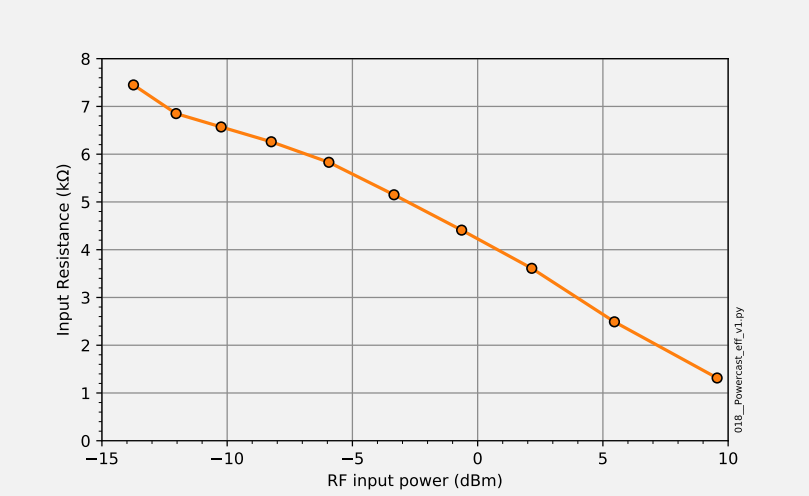


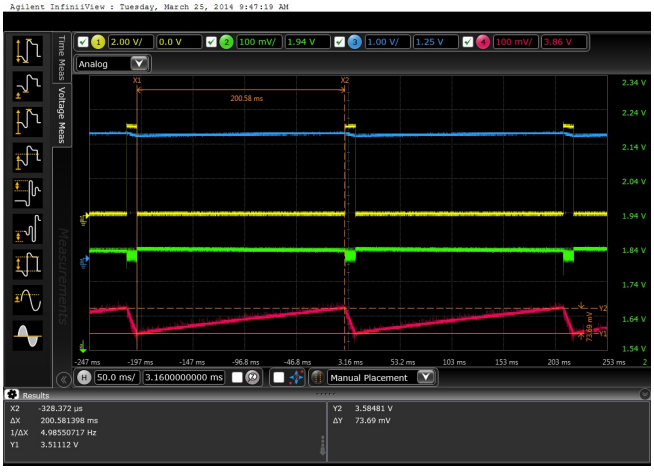
Figure 6.10 Measured BQ25570 power management circuit input resistance at 50 % OC voltage, using the imec rectifier.

By measuring the complete WET setup, the total harvester efficiency η_{harv} can be determined, see Fig. 6.2. For each value of RF input power, the duty cycle of the dynamic load is selected such that the system is in an energy equilibrium. This can be easily determined by monitoring the energy storage capacitor voltage. This voltage will vary between V_1 and V_2, where the larger V_2 should just be reached before the dynamic load starts to draw energy from the capacitor. Fig. 6.11(a) shows the case with more RF input power compared to average dc output power consumption. The energy storage capacitor voltage (magenta line) reaches its maximum well before the dynamic load starts to consume power. In Fig. 6.11(b) the system is in energy equilibrium after lowering the RF input power level. Using Fig. 6.8, the average obtained dc output power is calculated as

$$\overline{P_{\text{out}}} = P_{\text{out}} \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}}. \tag{6.4}$$

From this, the harvester energy transfer efficiency η_{harv} is calculated as

(a) System *not in* energy equilibrium, $P_{\text{in}} = 6.1$ dBm.



(b) System *in* energy equilibrium, $P_{\text{in}} = 4.1$ dBm.

Figure 6.11 Oscilloscope measurement example of RF power transfer system. Dynamic load dc power consumption (yellow, 2nd line from top) with the energy storage capacitor voltage (magenta, bottom line). $T_{\text{off}} = 200$ ms, $T_{\text{on}} = 10$ ms, $P_{\text{out}} = 19.8$ mW.

$$\eta_{\text{harv}} = \frac{\overline{P_{\text{out}}}}{P_{\text{in}}}. \tag{6.5}$$

The energy stored in the energy storage capacitor, see eq.(6.1), during the time period T is used to calculate the efficiency of the matched rectifier stage with the following boost-converter and storage capacitor included as

$$\eta_{\text{stor}} = \frac{0.5C\left(V_2^2 - V_1^2\right)}{TP_{\text{in}}}. \tag{6.6}$$

The efficiency of the boost converter and buck converter are found from the above defined efficiencies as

$$\eta_{\text{boost}} = \frac{\eta_{\text{stor}}}{\eta_{\text{rect}}}, \tag{6.7}$$

$$\eta_{\text{buck}} = \frac{\eta_{\text{harv}}}{\eta_{\text{stor}}}. \tag{6.8}$$

The above mentioned efficiencies are measured and shown as a function of RF input power in Fig. 6.12. In this example, a storage capacitor of 1000 μF is used and an instantaneous power consumption of the load of 55 mW. As an example: $\eta_{\text{harv}} = 22.8\,\%$ for $P_{\text{RF}} = -10$ dBm, which means $\overline{P_{\text{out}}} = 22.8\,\mu$W and with a period $T = 8.7$ s, this provides 19.8 mW available dc output power during 10 ms per period. In the same figure, the measured Powercast efficiency is also indicated. Compared to the imec rectifier, the Powercast circuit performs less efficient over the whole RF input power range.

ADS simulation

The circuit is replicated in ADS using the Sischka SBD model and realistic models (including parasitics) for the lumped elements, based on supplier data. The open circuit load voltage V_{OC} is simulated using a 100 MΩ resistor as load [3]. These values are stored against the source power level (in dBm), with the ADS measurement data interchange format (MDIF) format. Using the file based ADS data access component (DAC), this open circuit voltage data is used in a next simulation to optimize the load resistance to reach a load voltage specified as percentage of the open load output voltage. This is to mimic the situation of using a TI BQ25570 power management circuit as rectifier load.

[3] As this is a simulation of a practical circuit, a normal source type is used: the ADS P_1Tone source.

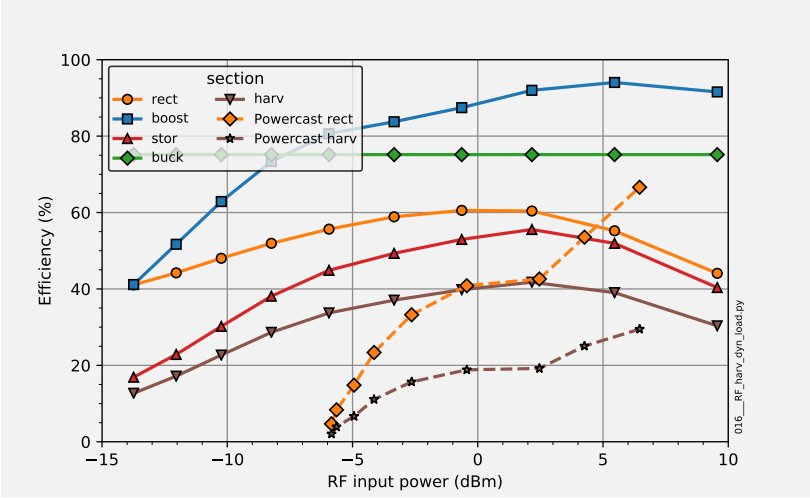


Figure 6.12 Measured efficiency of the different sections of the imec WET setup, at $f_0 = 868$ MHz. 'rect' is the matched receiver section, 'boost' the boost converter and storage capacitor, 'stor' the matched rectifier with boost converter and storage capacitor, 'buck' the buck converter, 'harv' the complete harvester circuit (see Fig. 6.2). The dashed lines are meausured on the Powercast setup at $f_0 = 915$ MHz.

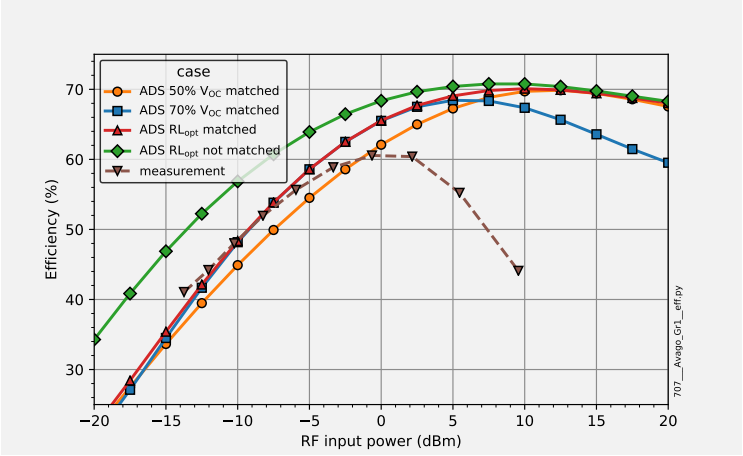
Fig. 6.13 shows in (a) the efficiency and in (b) the load resistance as a function of RF input power for the Gr1-type rectifier. The practical situation is simulated for a range of open circuit voltage values ($40 \cdots 90$ % V_{OC}), of which the 50 % and 70 % cases are shown. Also shown are two cases where the load resistance is optimized for best efficiency. This is done for the matched case[4] and the unmatched case[5]. In the measurement, the TI BQ25570 was set to 50 % open circuit voltage (V_{OC}). Comparing the measurement with the simulation data shows that the 70 % V_{OC} case shows the best match, especially for the load resistance. The efficiency deviation between measurement and the 70 % V_{OC} curve above an input power level of −5 dBm is likely caused by the input voltage limitation of the TI BQ25570 chip. This is not further investigated but plays a role when using such a design in selecting the rectifier topology and setting the open circuit voltage percentage for the maximum power point tracking mechanism.

From the simulation of the optimal efficiency load resistance, the optimal open circuit voltage percentage is calculated. Fig. 6.14 shows the result, both for the matched- and unmatched circuit. As found in chapter 4, the rectifier input impedance is dependent on the load resistance, above a certain input power

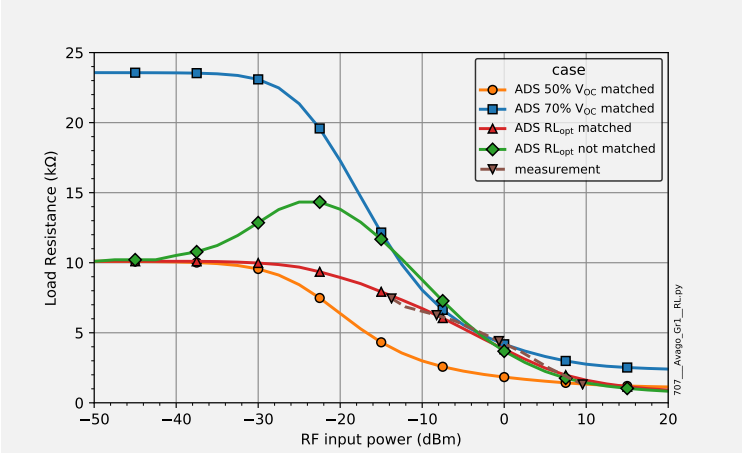
[4] using the capacitor and inductors as shown in Fig. 6.7 (a) as input imedance matching circuit and a normal ADS P_1Tone source.

[5] without input matching circuit and using a complex conjugated matched source

level. This plays a role when the TI BQ25570 chip measures the open circuit voltage: this changes the rectifier input impedance, which results in a impedance mismatch between the source and rectifier. Due to the reduced power flowing into the circuit, the open circuit voltage will be lower. This explains why the matched case shows a larger optimal open circuit voltage percentage.



(a) Efficiency.



(b) Load Resistance.

Figure 6.13 Simulated and measured (dashed) Gr1-rectifier (a) efficiency and (b) load resistance versus input power level, at f_0 = 868 MHz. The simulated results are for different V_L / V_{OC} ratios, for an efficiency optimized case and for the RL_{opt} matched- and unmatched cases. For the unmatched case, a complex conjugately matched source is used. For the matched cases, a normal source is used and an impedance matched section.

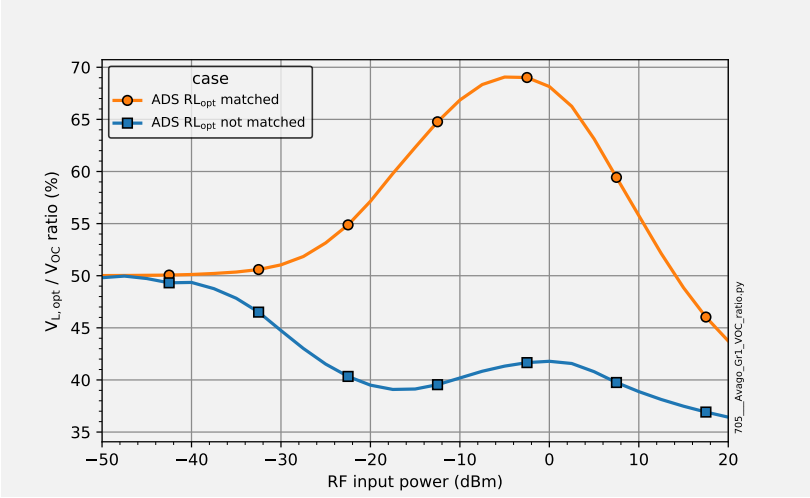
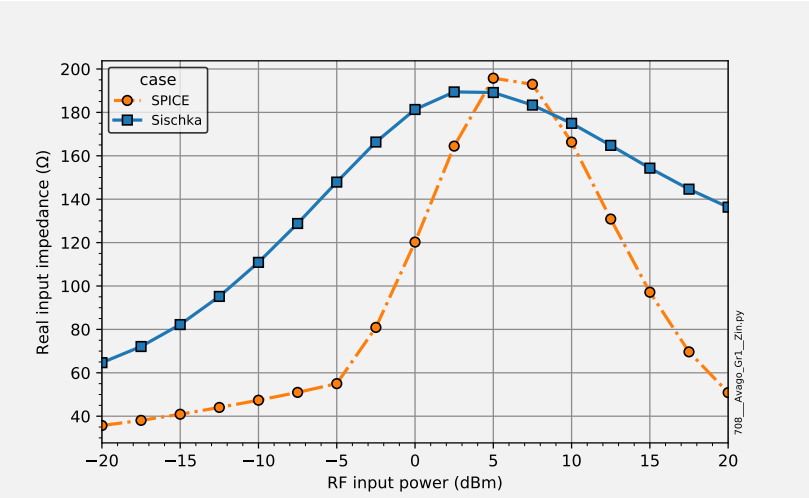


Figure 6.14 Simulated $V_{L,opt}$ / V_{OC} ratio (%) for the unmatched- and matched rectifier case.

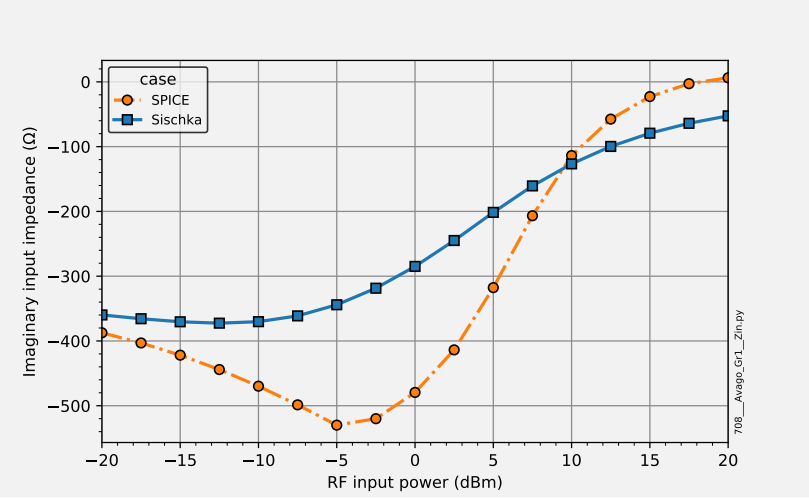
Comparison SPICE – Sischka

In chapter 3 we discussed the difference between the widely used SPICE SBD model and the Sischka macro model. For the practical application circuit as shown in this chapter, a comparison is made between these two models. This is done for the un-matched case, so without using the input impedance matching circuit. Fig. 6.15 shows the difference in rectifier input impedance as a function of RF input power. Fig. 6.16 the difference in rectifier efficiency[6] as a function of RF input power. The significant impedance difference explains why the design of an input matching circuit based on the SPICE model, will not result in a desired circuit input impedance and efficiency. The practical circuit input matching circuit is found by trial-and-error optimization. This was done as the proper Sischka model still had to be made. The measured efficiency is lower compared to the Sischka model efficiency, due to the impedance matching circuit component losses and — for the higher input power levels — also due to the TI BQ25570 input voltage limitation.

[6]Compared to Fig. 4.19 (a), the difference between the models is larger for this Greinacher rectifier at 915 MHz and a non-ideal SBD. The results shown in Fig. 4.19 correspond to a peak detector topology with an ideal SBD at a frequency of 6.78 MHz.



(a) Real part of circuit input impedance.



(b) Imaginary part of circuit input impedance.

Figure 6.15 Simulated Gr1-rectifier (a) real- and (b) imaginary input impedance versus input power level. The simulation is done using a SPICE (dot-dash) and Sischka (straight) diode model for the un-matched topology, at $f_0 = 868$ MHz, including realistic R_s and C_{j0} values and the breakdown effect.

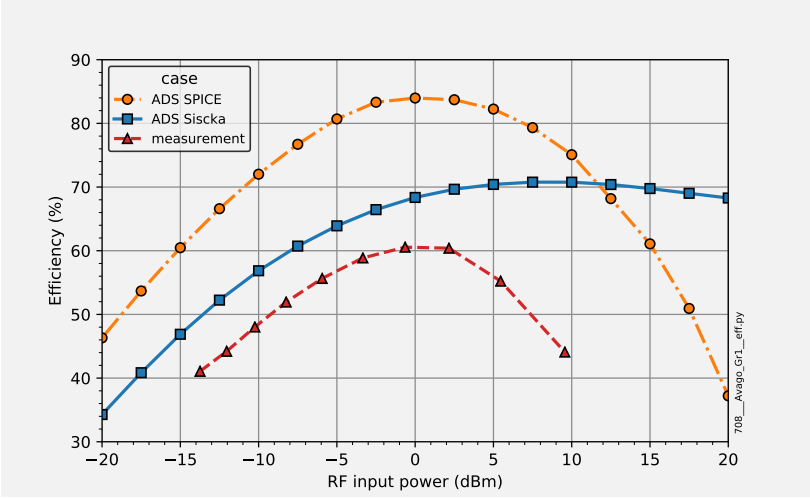


Figure 6.16 Simulated and measured (dashed) Gr1-rectifier efficiency, comparing the SPICE (dot-dash) and the Sischka (straight) diode models. The simulations are for the un-matched topology, including realistic R_s and C_{j0} values and the breakdown effect. The measurement includes the input impedance matching circuit. Measurement and simulations are done at $f_0 = 868$ MHz.

Power and distance prediction

Assuming a free-space, line of sight situation and a transmitter having an EIRP of 3 W at 868 MHz, the average obtained dc output power, $\overline{P_{\text{out}}}$, has been calculated for the imec and Powercast designs, as a function of the distance between transmitter and rectenna. For that, use has been made of the Friis equation and the results shown in Fig. 6.12. The average power levels have been calculated for two assumed receive antennas, one having a gain of 1 dBi and one having a gain of 6.1 dBi. The average obtained dc output power is calculated by eq. (6.4), see also Fig. 6.8.

The results are shown in Fig. 6.17, and are compared to a commercially available radiative WET system, by Powercast, measured and converted to the same EIRP level but for a frequency of 915 MHz [12]. From the figure and eq. (6.4) we see that we can get, using the 6.1 dBi receive antenna, 30 μW of continuous dc power up to a distance of 10 m from the 3 W EIRP source and the imec rectifier circuit. Using the same source and receive antenna we can obtain 60 mW of dc power, during 40 ms, every 2 minutes, also up to a distance of 10 m. The Powercast rectifier circuit is not effective at this distance and will result in a non-working application.

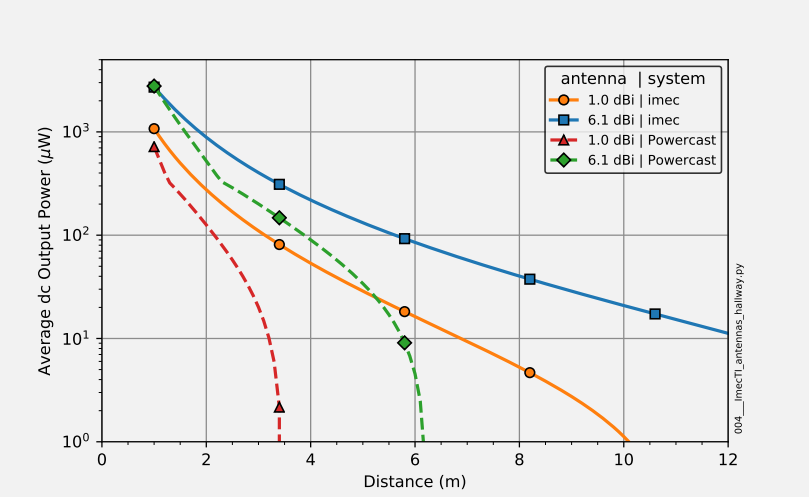


Figure 6.17 Calculated, based on measured data, average obtained dc output power $\overline{P_{\text{out}}}$ as a function of free line of sight distance for two antennas. The solid lines represent the results for the circuit described in this chapter. The dashed lines represent the results for a commercially available radiative WET system, by Powercast, tested for the same EIRP but at a frequency of 915 MHz.

6.5 Summary

In this chapter we have shown a typical radiative WET system and discussed its load, power management and its input power level range and corresponding available dc output power range. A practical example is shown of applying a programmable duty-cycled load. A clear difference in performance is shown between the commercial Powercast solution and the imec design.

In this chapter four items have been presented:

a) A practical WET application in the field of WSNs, including the typical receiver input power levels.

b) An implementation example of a power management system, connected to a rectifier output.

c) The designed practical application example is compared to a COTS product from Powercast.

d) The widely used SPICE diode model is compared in performance with the Sischka model discussed in this work. The superiority of the Sischka model has been demonstrated and we can conclude that the widely used SPICE diode model is not very well suited for (radiative) WET application design.

Chapter 7

Conclusions & Recommendations

In this work we looked at the field of radiative WET, enabling energy transfer bridging a distance of several meters for e.g. WSN applications. With a focus on the energy receiving side, different aspects of the rectifying semiconductor discrete diodes are discussed and their impact on the rectifier itself. The maximization of the rectifier energy transfer efficiency is used as the primary research objective.

7.1 Conclusions

In **Chapter 2** we demonstrated that a rectifier input impedance is showing a time-varying behaviour, depending on the shape of the applied diode voltage. This results in a mismatch loss between a source and rectifier circuit input port even when the rectifier seems perfectly matched for the input impedance. Applying the right filter structure will reduce the mismatch effect, resulting in an increase of energy transfer efficiency. In the rectifier example of Section 2.1 the mismath loss is 0.5 dB at $P_s = 10$ dBm, due to the high pass filter. Shorting the harmonic frequencies to ground at the rectifier input would eliminate this loss.

Having an accurate diode model and insight in the rectifier input impedance does not mean that designing the optimal input impedance matching network is straightforward. A so-called complex conjugately matched source P_{CCM} is presented in **Chapter 2** to ensure an adaptive constant circuit input power level, while optimizing the rectifier load resistance. Using this source results in obtaining the optimal rectifier energy transfer efficiency and corresponding load resistance and rectifier input impedance.

Literature shows that diode-circuit designs are often based on manufacturer

pn-junction diode SPICE model parameters, like e.g. [41–46]. In this work we discussed why this model has shortcomings for usage in the field of WET rectifiers. The reverse bias region plays a significant role for WET rectifiers, which requires an improved model. Two different options were provided in **Chapter 3**: the Sischka macro model, based on two anti-parallel connected *pn*-junction diodes and the equation-based Sze model. The model parameters are fitted on temperature dependent measurements, carried out for two different diode types: the Avago HSMS-2852 and the Skyworks SMS7621. Both models correlate better with measured data on both the reverse bias region and the temperature dependency of the diode current than the classical ones. The measured data also provided insight into component to component parameter spread and deviation from the manufacturer data sheet values. These factors are both significant and should be taken into account in rectifier design work. As an example, Table 3.7 reports a measured SMS7621 saturation current of I_s = 51.6–212 nA with a data-sheet value of I_s = 40 nA. Samewise for the series resistance R_s = 17–40 Ω with a data-sheet value of R_s = 12 Ω.

Chapter 4 described a simple load experiment, which indicates a direct relation between rectifier input impedance and diode type, for extremely low input power levels. It also showed the effect of the load resistance on the rectifier input impedance, for higher input power levels. Next to this, the difference between the SPICE *pn*-junction diode model and the introduced improved models was expressed with this experiment. This resulted in an important insight into the rectifier input impedance, which is — for low input power levels — dependent on the diode type, but for high input power levels on the load resistance. Another result is that the improved models, fitting measured diodes, yield in a significantly lower rectifier input impedance — for the high input power levels — compared to the often used SPICE model.

Education on diodes typically is done in the voltage-current and time domain. **Chapter 4** showed that doing this in the power and frequency domain as well provides important extra insights. The idea that a high diode saturation current and junction temperature lead to more dc current stems from the voltage-current domain. This work shows that this doesn't correspond to a high rectifier efficiency. When looking from the power domain perspective the rectifier efficiency effect is contrary: a low diode saturation current and junction temperature result in a high input impedance and (when converted to energy transfer efficiency) in a high efficiency.

In the comparison of different rectifier topologies, it appears that they do not really distinguish themselves in terms of efficiency, but in terms of output voltage and optimal load and input resistance, as shown in **Chapter 5**. This conclusion helps in making topology choices in a design phase.

Different choices can be made to connect a circuit to a rectifier output port. A few examples are provided in **Chapter 6**. Next to the optimal rectifier load resistance, also the well-chosen fixed load resistance case is shown. The latter might have a benefit, when a large input power level range is applicable.

7.2 Recommendations

Chapter 2 shows the varying rectifier input impedance over time, due to the chosen topology and input signal level. In this situation, the exact point on the impedance time-trajectory used for the input impedance matching circuit might play a role in the obtained efficiency. This topic can be investigated further.

Chapter 3 discussed the improved diode models on the reverse bias characteristic and **Chapter 4** the effect of the improved models on the rectifier input impedance and efficiency. More work on the diode junction capacitance is recommended, as this parasitic element plays a significant role at higher frequencies. Measurements on modern diodes can be verified with the existing models and the model parameter(s) can be adjusted accordingly.

From **Chapter 4** follows that a low diode saturation current results in a higher rectifier energy transfer efficiency. The use of a *pn*-junction diode can be investigated as possible efficient alternative. This might be the case for a specific input power level range and/or frequency of operation range.

WET applications having significant load resistance variation might benefit from switching rectifier topology. **Chapter 5** shows a significant variation between different rectifier topologies for the optimal input impedance and load resistance. E.g. a wireless battery charging case with normal and trickle charge mode, typically has a decade difference in charge current and load resistance.

A thorough comparison of rectifiers, using modern available diodes, is recommended making use of the concepts and insights discussed in **Chapters 2 to 6**. This work can be combined with complex conjugately matched antennas to avoid impedance matching networks, to further enhance the overall efficiency.

Appendix A

Lambert *W* Function

The Lambert W function is defined to be the multivalued function of the converse relation of the function $f(w) = we^w$, where w is any complex number and e^w is the exponential function.

If z and w are any complex number, we can substitute $w = W(z)$ and get the defining equation for the W function:

$$z = W(z)e^{W(z)}. \tag{A.1}$$

If we restrict this to real-valued W, the complex variable z is replaced by the real variable x and the relation is only defined for $x \geq -1/e$. The additional constraint $W \geq -1$ defines a single-valued function $W_0(x)$ which is named the principle or main branch of the W function. The lower branch has $W \leq -1$ and is denoted $W_{-1}(x)$. The Lambert W function cannot be expressed in terms of elementary functions.

Non-linear recurrence relations, as eqn. (3.3), are usually difficult to change into closed-form equations with standard techniques, only for very few cases this works [121]. In this case, we can make use of the main branch of the Lambert W function [76].

Rewriting the equation for the diode current, in a single diode rectifier circuit, as a function of the complete diode voltage V_d (without C_j, so $I_d = I_j$), and using $\Lambda_s = I_s R_s/(nV_T)$ and $\Lambda_d = V_d/nV_T$, the following derivation can be made:

$$I_d = I_s e^{\left(\frac{V_d}{nV_T} - \frac{I_d R_s}{nV_T}\right)} - I_s, \tag{A.2}$$

which can be rewritten as

$$(I_d + I_s)e^{\frac{I_d R_s}{nV_T}} = I_s e^{\Lambda_d}. \tag{A.3}$$

Multiplying both sides with Λ_s/I_s:

$$(I_d + I_s)\frac{\Lambda_s}{I_s}\mathrm{e}^{\frac{I_d R_s}{nV_T}} = I_s\frac{\Lambda_s}{I_s}\mathrm{e}^{\Lambda_d}, \tag{A.4}$$

and separating $\frac{I_d R_s}{nV_T}$ as:

$$\frac{I_d R_s}{nV_T} = (I_d + I_s)\frac{R_s}{nV_T} - \frac{I_s R_s}{nV_T} = (I_d + I_s)\frac{\Lambda_s}{I_s} - \Lambda_s, \tag{A.5}$$

we can write:

$$(I_d + I_s)\frac{\Lambda_s}{I_s}\mathrm{e}^{\left((I_d+I_s)\frac{\Lambda_s}{I_s}-\Lambda_s\right)} = \Lambda_s\mathrm{e}^{\Lambda_d}. \tag{A.6}$$

Bringing the exponential Λ_s term to the right side:

$$(I_d + I_s)\frac{\Lambda_s}{I_s}\mathrm{e}^{\left((I_d+I_s)\frac{\Lambda_s}{I_s}\right)} = \Lambda_s\mathrm{e}^{(\Lambda_d+\Lambda_s)}. \tag{A.7}$$

If we now substitude $(I_d + I_s)\frac{\Lambda_s}{I_s} = x$ we see on the left hand side the function $x\mathrm{e}^x$. Making use of the principle branch of the W function, this leads to

$$x = (I_d + I_s)\frac{\Lambda_s}{I_s} = W_0\left(\Lambda_s\mathrm{e}^{(\Lambda_d+\Lambda_s)}\right). \tag{A.8}$$

Rewriting the equation gives

$$(I_d + I_s) = \frac{W_0\left(\Lambda_s\mathrm{e}^{(\Lambda_d+\Lambda_s)}\right)}{\frac{\Lambda_s}{I_s}}, \tag{A.9}$$

which can be rewritten as

$$I_d = I_s\left(\frac{W_0\left(\Lambda_s\mathrm{e}^{(\Lambda_d+\Lambda_s)}\right)}{\Lambda_s} - 1\right). \tag{A.10}$$

Appendix B

Current Responsivity

To quantify the rectifying energy transfer capabilities of a diode, the current responsivity $\Re_I$ is sometimes used [15]:

$$\Re_I = \frac{\langle i_{\text{sc}} \rangle_0}{P_{\text{in}}^1}, \tag{B.1}$$

in which $\langle i_{\text{sc}} \rangle_0$ represents the dc short circuit current (being the first term in Eq. (4.18)) and P_{in}^1 the power flowing into the diode:

$$P_{\text{in}}^1 = \frac{1}{T} \int_0^T v_j(t) i_j(t) \mathrm{d}t = \frac{1}{2} V_j I_j. \tag{B.2}$$

For an ideal ($R_s = 0\ \Omega$) shorted harmonically terminated rectifier (including a dc-short at the diode's anode), the power dissipated in the junction is only due to the fundamental frequency, as at dc and the $h > 1$ harmonic frequencies the voltage is zero across the junction. For a nonlinear device, at low input power levels, the rectified current varies linearly with the applied RF power - also named the square law regime (see Fig. 4.2: $f_2(x)$ is linear for $x < 0.2$, Fig. 4.4 and Fig. 4.8). This results in a constant $\Re_I$ value, equal to the quadratic current responsivity $\Re_{I_0}$, which can be calculated as following. First the $\langle i_{\text{sc}} \rangle_0$ is obtained by applying Eq. (4.31) in Eq. (4.15). As $\langle V_{\text{j,sc}} \rangle_0 = 0$ we have $\mathrm{e}^{\Lambda_0} = 1$. This results in $\langle i_{\text{sc}} \rangle_0 = \frac{1}{4} {\Lambda_1}^2 I_s$. Next for the P_{in}^1 term we use Eqs (4.35) and (4.8) resulting in: $P_{\text{in}}^1 = \frac{1}{2} V_j \Lambda_1 I_s$. Now $\Re_{I_0}$ is written as:

$$\Re_{I_0} = \frac{\frac{1}{4} {\Lambda_1}^2 I_s}{\frac{1}{2} V_j \Lambda_1 I_s} = \frac{1}{2nV_T} = 19.34 \qquad \text{(A/W)}, \tag{B.3}$$

when using $n = 1$ and $V_T = 25.85$ mV at $T = 300$ K. This means that for every diode, $\Re_{I_0}$ is only dependent on n and temperature T. The deviation from the linear detection can be quantified with factor Δ. This factor is equal to $\Re_I / \Re_{I_0}$.

For $\Re_I$ we take for $\langle i_{sc}\rangle_0$ the large signal term for the dc current using Eq. (4.15). This is divided by the P_{in}^1 term for which Eq. (4.16) with $h = 1$ is used in Eq. (B.2). This results for Δ in:

$$\Delta = \frac{2nV_T \left\{ \sum_{i=0}^{\infty} \frac{1}{h_0!} \frac{1}{2^{h_0}} \binom{h_0}{\frac{h_0}{2}} e^{\Lambda_0} {\Lambda_1}^{h_0} - 1 \right\}}{\frac{1}{2} V_j \sum_{i=0}^{\infty} \frac{1}{h_1!} \frac{2}{2^{h_1}} \binom{h_1}{i} e^{\Lambda_0} {\Lambda_1}^{h_1}} \quad \text{with } (h_0 = 2i,\ h_1 = 2i+1), \tag{B.4}$$

which gives

$$\Re_I = \Re_{I_0} \Delta. \tag{B.5}$$

Fig. B.1 shows the linear detection deviation factor Δ related to the diode junction voltage, for a shorted ideal harmonically terminated diode ($n = 1.0$, $R_s = 0\ \Omega$, $T = 300$ K). This curve shows a decline in dc-current at input voltage levels above 10 mV, which doesn't match the efficiency values seen for these circuits, which typically increase till at least 0 dBm [36, 48].

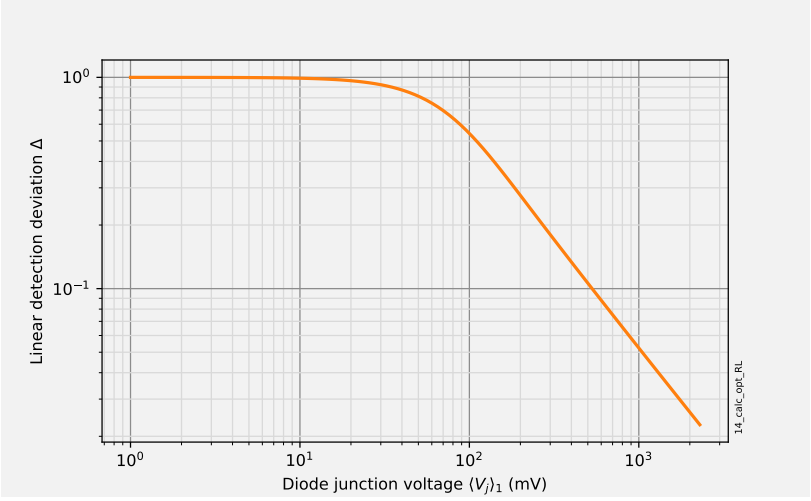


Figure B.1 Deviation from linear detection factor Δ, showing the effect on $\Re_I$. Calculated using eq. (B.4) based on approximation eq. (4.18) with 60 terms.

In the previous equations, a shorted diode is considered. In the practical application, a load resistance is used to obtain a decent level of useful dc-voltage to consume the rectified energy. This dc-voltage introduces a bias-voltage in the

exponential diode equation, causing the average junction-voltage to be negative instead of zero. An equilibrium is reached in steady state, leveling the RF input power with the dissipated power in the rectifying circuit and its load. This results in a change in the above provided equations.

An example is shown to illustrate that the approach of using the current responsivity is not that useful for radiated energy harvesting:

a) The rectifier load resistance has an effect on the single diode detector, with Pin = −30 dBm = 1 μW. Optimal load resistance is R_L = 12 kΩ. The dc-offset (and output voltage) is 57 mV. The peak V_j is only 59 mV instead of the 116 mV available at the anode (no dc-offset at anode). The resulting dc-current into the load equals 4.75 μA, which gives $\Re_I$ = 4.75 A/W and $\eta_{\text{Prf-dc}}$ = 27.1 %. Pdiss,diode = 729 nW, Pload = 271 nW.

b) The same circuit with Pin = 0 dBm = 1 mW. The optimal load resistance is R_L = 37 kΩ. The output voltage is 5.9 V and the dc output current 159.5 μA. This results in $\Re_I$ = 0.159 A/W, a fairly low value, but $\eta_{\text{Prf-dc}}$ = 94.1 %, which shows that this circuit delivers a nice amount of RF to dc conversion. With the corresponding values of Pdiss,diode = 58.9 μW, Pload = 941μW.

The Schottky diode based rectifier is not a current driving source, but instead an RF to dc energy converter.

Authored and co-authored Publications

[a] S. Keyrouz, H. Pflug, and H. Visser, “Input Impedance Calculation of a Multi-Stage Rectifier Circuit,” in *2019 IEEE Wireless Power Transfer Conference (WPTC)*, 2019, pp. 30–35.

[b] H. W. Pflug and H. J. Visser, *Wireless Power Transfer: Discrete Rectifier Modeling and Analysis*. Springer International Publishing, 2016, pp. 111–135.

[c] H. J. Visser, H. W. Pflug, and S. Keyrouz, *Far-Field Wireless Power Transfer for IoT Sensors*. Cham: Springer International Publishing, 2016, pp. 85–110.

[d] ——, “Rectenna Demonstrators at Holst Centre / imec and Eindhoven University of Technology,” in *Antennas and Propagation (EuCAP), 2015 9th EuropeanConference on*, 2015.

[e] H. J. Visser and H. W. Pflug, “ENERGY OUT OF THIN AIR - Theory of radiative, far-field wireless power transfer and applications,” in *International Microwave Symposium IMS2016*, no. IMS Workshop "Theory and Applications of Wireless Power Transfer", San Francisco, CA, USA, 2016.

[f] H. W. Pflug, H. J. Visser, and S. Keyrouz, “Practical Applications of Radiative Wireless Power Transfer,” in *Wireless Power Transfer Conference (WPTC), 2015 IEEE*, 2015, pp. 1–4.

[g] Y. Zhang, H. Pflug, H. J. Visser, and G. Dolmans, “Wirelessly powered energy autonomous sensor networks,” in *Wireless Communications and Networking Conference (WCNC), 2014 IEEE*, apr 2014, pp. 2444–2449.

[h] H. W. Pflug, S. Keyrouz, and H. J. Visser, “Far-Field Energy Harvesting Rectifier Analysis,” in *2016 IEEE Wireless Power Transfer Conference (WPTC)*, 2016, pp. 1–4.

[i] K. van Oosterhout, M. Paulides, H. W. Pflug, S. Beumer, and R. Mestrom, "An Approximate Electromagnetic Model for Optimizing Wireless Charging of Biomedical Implants," *IEEE Transactions on Biomedical Engineering*, vol. 69, no. 6, pp. 1954–1963, 2022.

[j] H. W. Pflug and H. J. Visser, "Time Trajectory Rectifier Impedance Analysis," in *2019 IEEE Wireless Power Transfer Conference (WPTC)*, 2019, pp. 257–262.

[k] H. J. Visser, H. W. Pflug, and S. Keyrouz, *Wireless Power Transfer Algorithms and Applications in Ad hoc Communication Networks.* Springer, 2016, ch. Far-Field.

[l] H. W. Pflug, S. Beumer, K. Weijand, T. B. Ćulibrk, J. Tol, and H. J. Visser, "Parallel Resonant Inductive Wireless Power Transfer," in *2019 IEEE Wireless Power Transfer Conference (WPTC)*, 2019, pp. 182–187.

Bibliography

[1] N. Tesla, "ART OF TRANSMITTING ELECTRICAL ENERGY THROUGH THE NATURAL MEDIUMS," Patent US 787,412, 1905.

[2] ——, "APPARATUS FOR TRANSMITTING ELECTRICAL ENERGY," Patent US 1,119,732, 1914.

[3] B. K. Vancil, "Vacuum electronics - 100 years," in *IVESC 2004. The 5th International Vacuum Electron Sources Conference Proceedings (IEEE Cat. No.04EX839)*, 2004, pp. 23–25.

[4] D. L. Sengupta, T. K. Sarkar, and D. Sen, "Centennial of the Semiconductor Diode Detector," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 235–243, 1998.

[5] S. Marzano, *paste tense, future sense.* BIS publishers, 2005.

[6] J. C. Schuder, "Powering an Artificial Heart: Birth of the Inductively Coupled-Radio Frequency System in 1960," *Artificial Organs TA - TT -* , vol. 26, no. 11, pp. 909–915, 2002.

[7] W. C. Brown, "The History of Power Transmission by Radio Waves," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 32, no. 9, pp. 1230–1242, sep 1984.

[8] A. Kurs, A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, and M. Soljačić, "Wireless Power Transfer via Strongly Coupled Magnetic Resonances," *Science*, vol. 317, no. 5834, pp. 83–86, 2007. [Online]. Available: http://science.sciencemag.org/content/317/5834/83

[9] A. Karalis, A. Kurs, R. Moffatt, J. Joannopoulos, P. Fisher, and M. Soljacic, "WIRELESS ENERGY TRANSFER," Patent US 7825,543 B2, 2010.

[10] ECC, "ERC Recommendation 70-03," 2021. [Online]. Available: http://efis.cept.org/reports/ReportDownloader?reportid=2

[11] ICNIRP, "Guidelines for limiting exposure to electromagnetic fields (100 kHz to 300 GHz)." *Health Phys 118(5)*, pp. 483–524, 2020.

[12] H. J. Visser, H. W. Pflug, and S. Keyrouz, "Rectenna Demonstrators at Holst Centre / imec and Eindhoven University of Technology," in *Antennas and Propagation (EuCAP), 2015 9th EuropeanConference on*, 2015.

[13] H. W. Pflug, S. Beumer, K. Weijand, T. B. Ćulibrk, J. Tol, and H. J. Visser, "Parallel Resonant Inductive Wireless Power Transfer," in *2019 IEEE Wireless Power Transfer Conference (WPTC)*, 2019, pp. 182–187.

[14] P. Kamalinejad, C. Mahapatra, Z. Sheng, S. Mirabbasi, V. C. M. Leung, and Y. L. Guan, "Wireless Energy Harvesting for the Internet of Things," *Communications Magazine, IEEE*, vol. 53, no. 6, pp. 102–108, 2015.

[15] S. Hemour and K. Wu, "Radio-Frequency Rectifier for Electromagnetic Energy Harvesting: Development Path and Future Outlook," *Proceedings of the IEEE*, vol. 102, no. 11, pp. 1667–1691, nov 2014.

[16] J. G. Koomey, S. Berard, M. Sanchez, and H. Wong, "Implications of Historical Trends in the Electrical Efficiency of Computing," *IEEE Annals of the History of Computing*, vol. 33, no. 3, pp. 46–54, 2011.

[17] Y. Sun, T. Tieman, H. Pflug, and W. Velthuis, "A Fully Integrated Dual-Frequency Push-Push VCO for Wideband Wireless Applications," in *Microwave Conference, 2000. 30th European*, 2000, pp. 1–4.

[18] S. D'Amico, A. Baschirotto, K. Philips, J. van der Tang, G. Dolmans, T. Fu, O. Rousseaux, H. Pflug, and B. Gyselinckx, "RF and Base-Band Circuit Blocks for LR-UWB Receivers," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*, sep 2007, pp. 158–161.

[19] H. W. Pflug, "UWB Pulse Shaping for IEEE 802.15.4a," in *Microwave Conference, 2008. EuMC 2008. 38th European*, 2008, pp. 713–716.

[20] S. Bagga, Z. Irahhauten, W. A. Serdijn, J. R. Long, H. Pflug, and J. J. Pekarik, "A Band-Reject ir-UWB LNA with 20 dB WLAN Suppression in 0.13 um CMOS," in *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian*, nov 2008, pp. 449–452.

[21] H. W. Pflug, D. Neirynck, J. Romme, K. Philips, and H. de Groot, "UWB Pulse Amplitude Estimation Method for IEEE 802.15.4a," *Ultra-Wideband (ICUWB), 2010 IEEE International Conference on*, vol. 1, pp. 1–4, 2010.

[22] M. De Nil, B. Busze, A. Young, D. Neirynck, H. Pflug, K. Philips, J. Huisken, J. Stuyt, and H. de Groot, "Low Power IEEE 802.15.4a UWB digital Rx Baseband Architecture," in *Ultra-Wideband (ICUWB), 2010 IEEE International Conference on*, vol. 1, sep 2010, pp. 1–4.

[23] V. Pop, R. de Francisco, H. Pflug, J. Santana, H. Visser, R. Vullers, H. de Groot, and B. Gyselinckx, "Human++: Wireless Autonomous Sensor Technology for Body Area Networks," in *Design Automation Conference (ASP-DAC), 2011 16th Asia and South Pacific*, jan 2011, pp. 561–566.

[24] H. W. Pflug, J. Romme, K. Philips, and H. de Groot, "Method to Estimate Impulse-Radio Ultra-Wideband Peak Power," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 59, no. 4, pp. 1174–1186, apr 2011.

[25] ——, "Impulse Radio Ultra-Wideband DC Power Modeling," in *Ultra-Wideband (ICUWB), 2011 IEEE International Conference on*, sep 2011, pp. 507–511.

[26] K. Ma, R. van Leuken, M. Vidojkovic, J. Romme, S. Rampu, H. Pflug, L. Huang, and G. Dolmans, "A Fast and Accurate SystemC-AMS Model for PLL," in *Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference*, 2011, pp. 411–416.

[27] X. Wang, K. Philips, C. Zhou, B. Busze, H. Pflug, A. Young, J. Romme, P. Harpe, S. Bagga, S. D'Amico, M. De Matteis, A. Baschirotto, and H. de Groot, "A High-Band IR-UWB Chipset for Real-Time Duty-Cycled Communication and Localization Systems," in *Solid State Circuits Conference (A-SSCC), 2011 IEEE Asian*, nov 2011, pp. 381–384.

[28] H. W. Pflug, J. Romme, G. Selimis, J. van den Heuvel, K. Philips, and H. de Groot, "Coupler Based Deterministic Indoor Radio Channel," in *Microwave Conference (EuMC), 2012 42nd European*, 2012, pp. 924–927.

[29] X. Wang, Y. Yu, B. Busze, H. Pflug, A. Young, X. Huang, C. Zhou, M. Konijnenburg, K. Philips, and H. de Groot, "A Meter-Range UWB Transceiver Chipset for Around-the-Head Audio Streaming," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, feb 2012, pp. 450–452.

[30] H. W. Pflug, J. Oudenhoven, N. F. Kiyani, J. H. C. van den Heuvel, K. Philips, and H. de Groot, "Zinc-Air Battery Modeling for Small Form Factor IR-UWB Wireless Sensor Network radios," in *Personal Indoor and Mobile Radio Communications (PIMRC), 2013 IEEE 24th International Symposium on*, sep 2013, pp. 228–232.

[31] J. H. C. van den Heuvel, H. Pflug, A. Ramkumar, A. Young, J. Romme, M. Hijdra, B. Busze, A. Breeschoten, G. J. M. Janssen, G. Dolmans, K. Philips, and H. de Groot, "Real Time Non-Coherent Synchronization Method in 6 -10.6 GHz IR-UWB Demonstrator Chipset," in *Global Communications Conference (GLOBECOM), 2013 IEEE*, dec 2013, pp. 3728–3734.

[32] G. Selimis, J. Romme, H. Pflug, K. Philips, G. Dolmans, and H. de Groot, "Sub-meter UWB localization: Low complexity design and evaluation in a real localization system," in *Personal Indoor and Mobile Radio Communications (PIMRC), 2013 IEEE 24th International Symposium on*, sep 2013, pp. 186–191.

[33] H. W. Pflug, H. J. Visser, N. F. Kiyani, G. Dolmans, K. Philips, K. Kanda, M. Hamaminato, and S. Masui, "Radio Channel Characterization for 400 MHz Implanted Devices," in *Wireless Communications and Networking Conference (WCNC), 2014 IEEE*, apr 2014, pp. 293–298.

[34] S. Gollakota, M. S. Reynolds, J. R. Smith, and D. J. Wetherall, "The Emergence of RF-Powered Computing," *Computer*, vol. 47, no. 1, pp. 32–39, jan 2014.

[35] S. Andreev, O. Galinina, A. Pyattaev, M. Gerasimenko, T. Tirronen, J. Torsner, J. Sachs, M. Dohler, and Y. Koucheryavy, "Understanding the IoT Connectivity Landscape: A Contemporary M2M Radio Technology Roadmap," *Communications Magazine, IEEE*, vol. 53, no. 9, pp. 32–40, sep 2015.

[36] H. W. Pflug, S. Keyrouz, and H. J. Visser, "Far-Field Energy Harvesting Rectifier Analysis," in *2016 IEEE Wireless Power Transfer Conference (WPTC)*, 2016, pp. 1–4.

[37] Y. Zhang, H. Pflug, H. J. Visser, and G. Dolmans, "Wirelessly powered energy autonomous sensor networks," in *Wireless Communications and Networking Conference (WCNC), 2014 IEEE*, apr 2014, pp. 2444–2449.

[38] V. Talla, B. Kellogg, B. Ransford, S. Naderiparizi, S. Gollakota, and J. R. Smith, "Powering the Next Billion Devices with Wi-Fi," *CoRR*, vol. abs/1505.0, 2015. [Online]. Available: http://arxiv.org/abs/1505.06815

[39] H. J. Visser and R. J. M. Vullers, "RF Energy Harvesting and Transport for Wireless Sensor Network Applications: Principles and Requirements," *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1410–1423, 2013.

[40] H. W. Pflug, H. J. Visser, and S. Keyrouz, "Practical Applications of Radiative Wireless Power Transfer," in *Wireless Power Transfer Conference (WPTC), 2015 IEEE*, 2015, pp. 1–4.

[41] M. Roberg, T. Reveyrand, I. Ramos, E. A. Falkenstein, and Z. Popovic, "High-efficiency harmonically terminated diode and transistor rectifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4043–4052, 2012.

[42] S. Hemour, Y. Zhao, C. H. P. Lorenz, D. Houssameddine, Y. Gui, C.-M. Hu, and K. Wu, "Towards Low-Power High-Efficiency RF and Microwave Energy Harvesting," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 62, no. 4, pp. 965–976, apr 2014.

[43] C. Liu, F. Tan, H. Zhang, and Q. He, "A novel single-diode microwave rectifier with a series band-stop structure," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 600–606, feb 2017.

[44] M. D. Wei, Y. T. Chang, D. Wang, C. H. Tseng, and R. Negra, "Balanced RF Rectifier for Energy Recovery with Minimized Input Impedance Variation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 5, pp. 1598–1604, 2017.

[45] J. H. Ou, S. Y. Zheng, A. S. Andrenko, Y. Li, and H. Z. Tan, "Novel Time-Domain Schottky Diode Modeling for Microwave Rectifier Designs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 4, pp. 1234–1244, apr 2018.

[46] X. Wang and A. Mortazawi, "Rectifier Array with Adaptive Power Distribution for Wide Dynamic Range RF-DC Conversion," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 1, pp. 392–401, jan 2019.

[47] H. W. Pflug and H. J. Visser, "Time Trajectory Rectifier Impedance Analysis," in *2019 IEEE Wireless Power Transfer Conference (WPTC)*, 2019, pp. 257–262.

[48] ——, *Wireless Power Transfer: Discrete Rectifier Modeling and Analysis*. Springer International Publishing, 2016, pp. 111–135.

[49] P. Horowitz and W. Hill, *The Art of Electronics*, 3rd ed. Cambridge: Cambridge University Press, 2015.

[50] Keysight Technologies, "Advanced Design System." [Online]. Available: https://www.keysight.com/nl/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html

[51] C. P. Steinmetz, "Complex Quantities and Their Use in Electrical Engineering," in *Proceedings of the International Electrical Congress, Chicago, Illinois conference of the AIEE*, 1893, pp. 33–73.

[52] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, 1st ed. Wiley-Interscience, 1992.

[53] J. Rahola, "Power Waves and Conjugate Matching," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 1, pp. 92–96, jan 2008.

[54] H. Nyquist, "Certain factors affecting telegraph speed," *Bell System Technical Journal, The*, vol. 3, no. 2, pp. 324–346, apr 1924.

[55] C. E. Shannon, "Communication in the Presence of Noise," *Proceedings of the IRE*, vol. 37, no. 1, pp. 10–21, jan 1949.

[56] D. Barataud, F. Blache, A. Mallet, P. P. Bouysse, J.-M. Nebus, J. P. Villotte, J. Obregon, J. Verspecht, and P. Auxemery, "Measurement and Control of Current/Voltage Waveforms of Microwave Transistors Using a Harmonic Load-Pull System for the Optimum Design of High Efficiency Power Amplifiers," *Instrumentation and Measurement, IEEE Transactions on*, vol. 48, no. 4, pp. 835–842, aug 1999.

[57] D. E. Root, J. Verspecht, J. Horn, and M. Marcu, *X-Parameters: Characterization, Modeling and Design of Nonlinear RF and Microwave Components*, S. C. Cripps, Ed. Cambridge University Press, 2013.

[58] B. A. Sexton and J. C. Jones, "Means of Complex Numbers," *Texas College Mathematics Journal*, vol. 1, no. 1, pp. 1–4, 2005.

[59] P. H. Smith, "Transmission Line Calculator," *Electronics*, vol. 12, no. 1, pp. 29–31, 1939.

[60] S. Roberts, "Conjugate-Image Impedances," *Proceedings of the IRE*, vol. 34, no. 4, pp. 198p–204p, apr 1946.

[61] J. Dunsmore, C. Xin, and Z. Yong-Xun, "A Novel Method to Accurately Set Incident Power to DUT with VNA," in *78th ARFTG Microwave Measurement Conference*, 2011, pp. 1–4.

[62] S. A. Maas, *Nonlinear Microwave and RF Circuits, Second Edition*, 2003. [Online]. Available: http://www.docstoc.com/docs/9418303/NonlinearMicrowaveAndRFCircuits2ndEdition

[63] K. S. Kundert and A. Sangiovanni-Vincentelli, "Simulation of Nonlinear Circuits in the Frequency," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 5, no. 4, pp. 521–535, 1986.

[64] L. Nagel and R. Rohrer, "Cancer. Computer Analysis of Nonlinear Circuits Excluding Radiation," *IEEE Journal of Solid-State Circuits*, vol. SC-6, no. 4, pp. 166–182, 1971.

[65] L. W. Nagel and D. O. Pederson, "SPICE (Simulation Program with Integrated Circuit Emphasis)," EECS Department, University of California, Berkeley, Tech. Rep. UCB/ERL M382, apr 1973. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/1973/22871.html

[66] L. W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits," Ph.D. dissertation, EECS Department, University of California, Berkeley, 1975. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/1975/9602.html

[67] T. H. Kuo, H. C. Lin, U. Anandakrishnan, R. C. Potter, and D. Shupe, "Large-signal resonant tunneling diode model for SPICE3 simulation," *Technical Digest - International Electron Devices Meeting*, pp. 567–570, 1989.

[68] T. Quarles, A. Newton, D. Pederson, and A. Sangiovanni-Vincentelli, "SPICE3 Version 3f3 User's Manual," p. 146, 1993. [Online]. Available: http://fides.fe.uni-lj.si/spice/download/spice3{_}manual.pdf

[69] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE*. McGraw-Hill, 1988.

[70] A. Vladimirescu, *The SPICE Book*. John Wiley & Sons, Inc., 1994.

[71] W. Shockley, "The Theory of p-n Junctions in Semiconductor and p-n Junction Transistors," *The Bell System Technical Journal*, vol. 28, pp. 435–489, 1949.

[72] H. H. G. Zirath, S. M. Nilsen, H. Hjelmgren, L. P. Ramberg, and E. L. Kollberg, "Temperature Variable Noise and Electrical Characteristics of Au-GaAs Schottky Barrier Millimeter-Wave Mixer Diodes," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 36, no. 11, pp. 1469–1475, nov 1988.

[73] V. G. Bozhkov and D. J. Kuzyakov, "Low-frequency noise and current-voltage characteristics of Schottky barrier contacts in a wide temperature range," *Journal of Applied Physics*, vol. 92, no. 8, pp. 4502–4512, 2002.

[74] D. K. Schroder, *Semiconductor Material and Device*, 3rd ed. John Wiley & Sons, Inc., 2006.

[75] J. Bardeen, "On the Theory of the A-C. Impedance of a Contact Rectifier," *The Bell System Technical Journal*, vol. 28, pp. 428–434, 1949.

[76] R. M. Corless, G. H. Gonnet, D. E. G. Hare, D. J. Jeffrey, and D. E. Knuth, "On the Lambert W function," *Advances in Computational Mathematics*, vol. 5, no. 1, pp. 329–359, 1996. [Online]. Available: http://dx.doi.org/10.1007/BF02124750

[77] R. T. Tung, "The physics and chemistry of the Schottky barrier height," *Applied Physics Reviews*, vol. 1, no. 1, p. 11304, 2014. [Online]. Available: https://doi.org/10.1063/1.4858400

[78] S. M. Sze, *Physics of Semiconductor Devices*. Wiley, 1969.

[79] H. Torrey and C. Whitmer, *Crystal Rectifiers*, S. A. Goudsmit, Ed. McGraw-Hill, 1948.

[80] W. Schottky, "Vereinfachte und erweiterte Theorie der Randschichtgleichrichter," *Zeitschrift für Physik*, vol. 118, no. 9 - 10, pp. 539–592, 1942.

[81] J. S. Schaffner and R. F. Shea, "The Variation of the Forward Characteristics of Junction Diodes with Temperature," *Proceedings of the IRE*, vol. 43, no. 1, p. 101, 1955.

[82] Agilent Technologies, "Nonlinear Devices," in *ADS documentation*, 2003.

[83] M. Brinson, *Qucs - A Tutorial. Component, compact device and circuit modelling using symbolic equations*, 2007. [Online]. Available: http://qucs.sourceforge.net/docs/tutorial/equations.pdf

[84] M. E. Brinson, S. Jahn, and H. Nabijou, "Qucs, SPICE and Modelica equation-defined modelling techniques for the construction of compact device models based on a common model template structure," in *MOS-AK/GSA Worshop on "Frontiers of Compact Modeling for Advanced Analog/RF Applications", Paris*, apr 2011.

[85] S. M. Sandler, "SPICE subcircuit accurately models zener characteristics," *Personal Engineering*, pp. 45–48, 1998.

[86] L. R. Piotrowski, "An Improved Spice2 Zener Diode Model for Soft-Region Simulation Capability," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 7, no. 12, pp. 1301–1303, dec 1988.

[87] D. A. Fleri and L. D. Cohen, "Nonlinear Analysis of the Schottky-Barrier Mixer Diode," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 21, no. 1, pp. 39–43, jan 1973.

[88] Y. P. Varshni, "Temperature dependence of the energy gap in semiconductors," *Physica*, vol. 34, no. 1, pp. 149–154, 1967. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0031891467900626

[89] V. G. Bozhkov and A. V. Shmargunov, "Influence of the nonlinear bias dependence of the barrier height on measured Schottky-barrier contact parameters," *Journal of Applied Physics*, vol. 109, 2011.

[90] R. T. Tung, "Recent advances in Schottky barrier concepts," *Materials Science and Engineering: R: Reports*, vol. 35, no. 1â€"3, pp. 1–138, 2001. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0927796X01000377

[91] V. Alex, S. Finkbeiner, and J. Weber, "Temperature dependence of the indirect energy gap in crystalline silicon," *Journal of Applied Physics*, vol. 79, no. 9, pp. 6943–6946, 1996.

[92] P. Van Halen, "A new semiconductor junction diode space charge layer capacitance model," in *Bipolar Circuits and Technology Meeting, 1988., Proceedings of the 1988*, sep 1988, pp. 168–171.

[93] B. R. Chawla and H. K. Gummel, "Transition region capacitance of diffused p-n junctions," *Electron Devices, IEEE Transactions on*, vol. 18, no. 3, pp. 178–195, 1971.

[94] H. T. Russell, *The SPICE Diode Model*, aug 1991.

[95] J. Zarebski and J. Dabrowski, "Modelling Power Schottky Diodes," in *Modern Problems of Radio Engineering, Telecommunications, and Computer Science, 2006. TCSET 2006. International Conference*, feb 2006, pp. 90–93.

[96] D. Korucu, T. S. Mammadov, and S. Özçelik, "The Role of Series Restistance on the Forward Bias Current-Voltage (I-V) Characteristicsin Sn/p-InP (MS) Contacts," *Journal of Ovonic Research*, vol. 4, no. 6, pp. 159–164, dec 2008.

[97] A. A. A. L. Hattami, J. R. Rathod, E. A. Kadash, H. S. Patel, K. D. Patel, and V. M. Pathak, "Physical Characteristics of Al/n-CdS Thin-Film Schottky Diode at High Temperatures," *International Journal of Technology*, vol. 4, no. 2, 2013. [Online]. Available: http://www.ijtech.eng.ui.ac.id/index.php/journal/article/view/112

[98] J. Lepkowski. (2006) Zener Macro-Models Provide Accurate SPICE SSimulation. Application Note. [Online]. Available: http://www.onsemi.com/pub{_}link/Collateral/AND8250-D.PDF

[99] F. Sischka, "Diode Modeling Strategy," in *Agilent Technologies Presentation*.

[100] S. Wong and C.-M. Hu, "SPICE Macro Model for the Simulation of Zener Diode I-V Characteristics," *Circuits and Devices Magazine, IEEE*, vol. 7, no. 4, pp. 9–12, 1991.

[101] Hewlett Packard, "Hermetic PIN Diodes for Stripline / Microstrip Switches / Attenuators," in *Technical Data 5965-8882E*.

[102] NXP, "SOT-23 overview," 2006. [Online]. Available: https://www.nxp.com/docs/en/package-information/SOT23.pdf

[103] Avago Technologies, "Low Cost Surface Mount Power Limiters," in *Application Note 1050*, 2010.

[104] ——, "Linear Model for Diode Surface Mount Packages," in *Application Note 1124*, 2010.

[105] Skyworks Solutions, "Circuit Models for Plastic Packaged Microwave Diodes," in *Application Note 1001*, 2005.

[106] L. Zhan, S. Qi, B. Hu, Y. Wu, and C. Chen, "Reflection Coefficient between Complex Impedances," in *IEEE 3rd International Conference on Electronics Technology (ICET)*, 2020, pp. 127–131.

[107] S. Adami, P. Proynov, G. S. Hilton, G. Yang, C. Zhang, D. Zhu, Y. Li, S. P. Beeby, I. J. Craddock, and B. H. Stark, "A Flexible 2.45-GHz Power Harvesting Wristband With Net System Output From -24.3 dBm of RF Power," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 1, pp. 380–395, jan 2018.

[108] P. Villard, "Transformateur à haut voltage. A survolteur cathodique." *Journal de Physique Théorique et Appliquée*, vol. 10, no. 1, pp. 28–32, 1901. [Online]. Available: https://doi.org/10.1051/jphystap:019010010002801

[109] H. Greinacher, "Das Ionometer und seine Verwendung zur Messung von Radium- und Rontgenstrahlen," *Physikalische Zeitschrift*, no. 15, pp. 410–415, 1914.

[110] L. Graetz, "Ein electrochemisches Verfahren, um Wechselströme in Gleichströme zu verwandeln," *Annalen der Physik*, vol. 298, no. 10, pp.

323–327, 1897. [Online]. Available: https://www.onlinelibrary.wiley.com/doi/epdf/10.1002/andp.18972981008

[111] F. H. Raab, "Maximum Efficiency and Output of Class-F Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1162–1166, 2001.

[112] R. A. Beltran, "Class-F and inverse class-F power amplifier loading networks design based upon transmission zeros," *IEEE MTT-S International Microwave Symposium Digest*, pp. 8–11, 2014.

[113] C. H. P. Lorenz, S. Hemour, and K. Wu, "Physical Mechanism and Theoretical Foundation of Ambient RF Power Harvesting Using Zero-Bias Diodes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2146–2158, 2016.

[114] (2021) Powercast P2110CSR Evaluation Board (P2110CSR-EVB), similar to the P2110-EVB board.

[115] "Texas Instruments BQ25570, Ultra Low Power Harvester Power Management IC with Boost Charger, and Nanopower Buck Converter." [Online]. Available: http://www.ti.com/product/bq25570

[116] "IEEE 802.15.4g-2012 - IEEE Standard for Local and metropolitan area networks–Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs) Amendment 3: Physical Layer (PHY) Specifications for Low-Data-Rate, Wireless, Smart Metering Utility Networks," 2012. [Online]. Available: https://standards.ieee.org/standard/802{_}15{_}4g-2012.html

[117] "Powercast Development Tools - Evaluation Board Antennas." [Online]. Available: https://www.powercastco.com/products/development-kits/{#}Antennas

[118] H. T. Friis, "A Note on a Simple Transmission Formula," *Proceedings of the IRE*, vol. 34, no. 5, pp. 254–256, 1946.

[119] H. J. Visser, H. W. Pflug, and S. Keyrouz, *Far-Field Wireless Power Transfer for IoT Sensors*. Cham: Springer International Publishing, 2016, pp. 85–110.

[120] "Arduino Mega microcontroller board." [Online]. Available: https://store.arduino.cc/arduino-mega-2560-rev3

[121] W. W. Chen, *Discrete Mathematics*. Macquarie University, 2008.

Publiekssamenvatting

Het zich nog steeds ontwikkelende gebied van draadloze energie-overdracht kan grofweg in twee categorieën worden verdeeld. In de eerste categorie wordt energie geleverd aan bijvoorbeeld elektronische sensoren met een relatief laag energieverbruik. Hierbij wordt meestal een afstand overbrugd van meerdere meters. De tweede categorie is die van inductieve energie-overdracht — meestal gebruikt op afstanden van minder dan een meter en op verschillende vermogensniveaus; van elektrische tandenborstels tot elektrische voertuigen. De eerste categorie maakt gebruik van antennes en elektromagnetische golven en wordt daarom *stralings* of *verre veld* draadloze-energie overdracht genoemd. De tweede categorie gebruikt meestal spoelen om een magnetisch veld over te dragen en wordt aangeduid als *inductieve* draadloze energie-overdracht. Dit onderzoek richt zich op de eerste *verre veld* categorie, waarbij de kant die energie ontvangt wordt geanalyseerd, zonder rekening te houden met de kant die energie zendt. Dit maakt de analyse eenvoudiger. Alle inzichten in dit werk zijn ook bruikbaar in de inductieve, tweede categorie.

Een essentieel onderdeel in de ontvanger van energie is de gelijkrichter. Deze is nodig om de wisselstroom, die gebruikt wordt voor de energie-overdracht, om te zetten naar gelijkstroom. De nadruk in dit onderzoek ligt op deze gelijkrichter, en dan specifiek het type waarbij gebruik wordt gemaakt van halfgeleider-diodes.

Om een optimale gelijkrichter te kunnen ontwerpen, is inzicht in de fundamentele werking van deze gelijkrichter nodig. De werking is gebaseerd op de niet-lineaire eigenschappen van een diode. Om de diode-werking te modelleren wordt gebruik gemaakt van een simulator. Een belangrijke grootheid in dit onderzoek is de efficiëntie van de energie-overdracht en daarmee de efficiëntie van de gelijkrichter.

Uit dit onderzoek komen de volgende **conclusies**:

- Het kortsluiten van de niet-lineaire harmonische stromen, die in de diode van een gelijkrichter ontstaan, resulteert in een hogere efficiëntie van energie-overdracht en een constante ingangsimpedantie van de gelijkrichter.
- De literatuur laat zien dat de meeste ontwerpen gebaseerd zijn op het SPICE-diodemodel. Dit onderzoek laat de tekortkomingen van dat model zien voor de toepassing van draadloze energie-overdracht. Ook worden er twee alternatieven beschreven, gebaseerd op metingen.
- Het hebben van een accuraat diode-model en inzicht in de gelijkrichter ingangsimpedantie garandeert nog niet dat er een optimaal ingangsimpedantie aanpas-netwerk ontworpen kan worden. Hiervoor blijkt een adaptieve signaalbron nodig te zijn. Hiermee kan de optimale belastingsweerstand bepaald worden en de bijbehorende efficiëntie van energie-overdracht, voor een bepaald ingangsvermogen.
- Een eenvoudig belastingsweerstand-experiment toont aan dat de gelijkrichter ingangsimpedantie voor lage ingangsvermogens afhankelijk is van het diodetype en voor hoge ingangsvermogens van de belastingsweerstand. Ook wordt met dit experiment het verschil duidelijk tussen het veel gebruikte SPICE-model en de op metingen gebaseerde alternatieve Schottky-diodemodellen.
- Het intuïtieve idee dat een hoge temperatuur en een grote diode verzadigingsstroom resulteren in een hoge gelijkrichter efficiëntie blijkt verkeerd. Het is juist andersom en dat wordt bevestigd door het uitwerken van de bijbehorende formules.
- In het vergelijk van verschillende gelijkrichter topologieën blijkt dat deze zich qua efficiëntie niet echt onderscheiden maar wel wat betreft uitgangsspanning en optimale belastingsweerstand.
- Tot slot blijkt dat, bij het ontwerpen van een gelijkrichter, de keuze tussen het gebruik van een optimale belastingsweerstand of een belastingsweerstand met vaste waarde, afhangt van het gekozen bereik aan ingangsvermogen.

Curriculum Vitae

Hans Pflug was born on 31 August 1966 in Eindhoven, the Netherlands. After finishing VWO in 1984 at Myrtus College in Apeldoorn, the Netherlands, he studied Electrical Engineering at the University of Twente and The Enschede Polytechnic, Faculty of Technology both in Enschede, the Netherlands. In 1991 he graduated cum laude on the design and realization of a low noise microwave amplifier and a microwave bandpass filter for a new 'Multi-Frequency Front End' for the Westerbork Synthese Radiotelescoop, Netherlands Foundation for Research in Astronomy Dwingeloo.

He has designed RF and microwave circuits at Ericsson in Emmen (paging), and Enschede (DECT), Lucent Technologies in Nieuwegein (WLAN), and delivered European support on RF and microwave simulation software tools with both Hewlett-Packard and Agilent Technologies in Amstelveen. He was involved with wireless sensor nodes in the Ultra Low Power Wireless Group, Holst Centre/imec in Eindhoven. As a wireless architect at GTX medical, he worked on a transcutaneous wireless charging system for an implantable pulse generator used for spinal cord injury treatment, also in Eindhoven (all in The Netherlands).

In 2016 he started a PhD project at the Eindhoven University of Technology of which the results are presented in this dissertation. Since 2020 he is employed at Philips Electronics in Eindhoven, working on RF and EMC topics.

Index

In the field of wireless energy transfer, a rectifier is used to convert the received alternating current into a direct current. The maximization of the rectifier energy transfer efficiency is not straightforward. This research shows the shortcomings of the SPICE diode model, used in most designs.
The intuitive idea that a high temperature and large diode saturation current result in a high rectifier efficiency appears to be incorrect. It is the other way around. This is confirmed theoretically by introducing topics like the time-varying rectifier impedance and its optimal load resistance.

TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY