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Medium Voltage Solid-State Transformer

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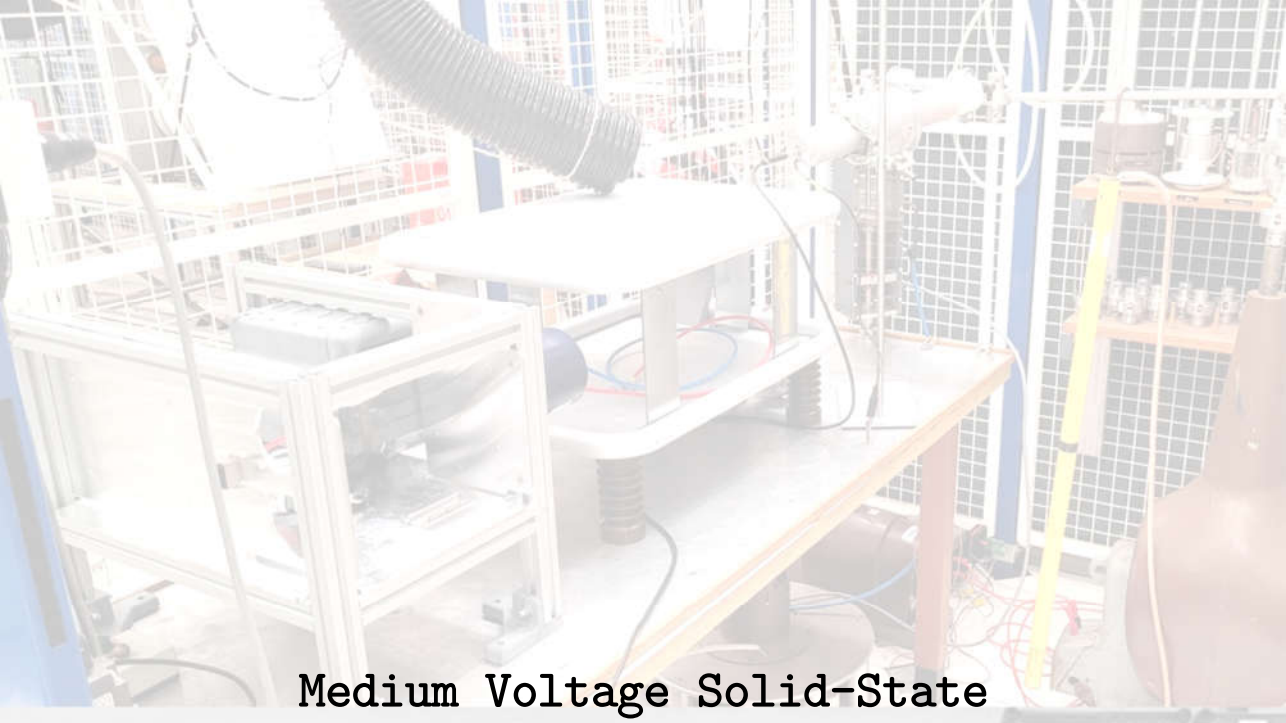

Medium Voltage Solid-State Transformer

An IEC60076-3 based design

Bram van Dam

2023-03-31

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PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op vrijdag 31 maart 2023 om 13:30 uur

door

Bram van Dam

geboren te Eindhoven

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2. Summary

The energy transition strongly impacts medium voltage distribution grids. Among other challenges, the rapid deployment of electric vehicles and the increasing use of renewable energy sources, and their fluctuating nature, give rise to larger voltage fluctuations and increased harmonic distortions at the distribution transformers (10 kV to 400 V). A promising technology to solve these problems is a so-called solid-state transformer (SST). In an SST, a conventional distribution transformer is replaced by a power electronics-based voltage transformer. Literature shows that with such an SST, voltages in networks can be regulated much faster and more dynamically. In addition, other functionalities can be realized with an SST, such as filtering out harmonics, removing imbalance or limiting short-circuit currents.

Literature shows that in the past 16 years, at least 13 prototypes have been built in various countries. However, none of these prototypes addresses the importance of compliance of an SST with relevant standards that must be met to meet all possible conditions that can occur in a grid.

The main contribution of this work is the identification of compliance to the *IEC60076-3: Insulation levels, dielectric tests, and external clearances in air* -standard as a requirement for SSTs. Two sub-contributions are derived.

1. The first sub contribution is that conventional transformers (and by extension, SSTs), are subjected to double the input voltages (compared to normal operation) for 60 seconds. This requires the power electronics to be fully dimensioned for that voltage, as opposed to the existing prototypes, which only limit themselves to the nominal 10 kV_{RMS}.
2. The second sub contribution is that the standard states that the primary and secondary windings of the transformer/SST will be subjected to 40 kV_{PEAK}, 50/60 Hz, for 60 seconds. Along with the transformer core requiring to be connected to earth, this effectively presents a galvanic isolation test for SST power electronics. The consequence of this test is that both the medium voltage side, *and* the low voltage

side, need to be carefully designed with respect to geometry, isolation, creepage, and clearance.

An SST prototype was designed, tested, and built as a research platform. The power architecture was selected, heavily influenced by available switching devices and their losses. The firmware and control loops have been implemented using MATLAB Simulink to soften the learning curve for future researchers. The SST research platform has been tested and is functioning as expected.

The tests identified in the IEC60076-3 standard are determined to be necessary and subsequently will result added high-cost and complexity for SSTs. As failure to comply would likely result in a cascading, catastrophic failure of the SST.

De energietransitie heeft een grote invloed op de middenspanningsnetten. Voorbeelden van uitdagingen die de middenspanningsnetten gaan zien zijn de toename in de uitrol van elektrische voertuigen en de toenemende aantal duurzame energie bronnen. De grote fluctuaties in energie waarmee deze gepaard gaan, gaan ook zorgen voor een toename in spanningsfluctuaties en harmonische vervorming bij distributietransformatoren (10 kV naar 400 V). Een van de veelbelovende technologiën is de zogenaamde Solid-State Transformator (SST). Met een SST word teen conventionele distributie transformator in zijn geheel vervangen door vermogenselektronica. De literatuur wijst uit dat spanningen in elektriciteitsnetten vele malen sneller geregeld kunnen worden met een SST. Daarnaast kan met een SST ook nog andere functionaliteit gerealiseerd worden, zoals het filteren van harmonischen, onbalans compenseren, en / of het begrensen van kortsluitingen. Literatuuronderzoek laat zien dat in de afgelopen 16 jaar tenminste 13 prototypen in verschillende landen zijn gebouwd. Echter, geen van deze prototypen addresseert de noodzaak om aan de relevante standaarden te voldoen die de condities van een elektriciteitsnet nabootst.
De hoofd-bijdrage van dit werk is de identificatie van de standaard "*IEC60076-3: Insulation levels, dielectric tests, and external clearances in air*" als een vereiste voor SSTs. Twee sub-bijdrages komen hieruit voort.

1. De eerste sub-bijdrage is dat conventionele transformatoren (end us ook SSTs), blootgesteld worden aan testspanningen op de ingang die tweemaal zo hoog zijn als de nominale spanning, voor 60 seconden. Deze testspanningen vereisen dat de vermogenselektronica van een SST volledig hiervoor gedimensioneerd worden. Dit is in contrast met bestaande prototypen, deze zijn allemaal gedimensioneerd op 10 kV_{RMS}.
2. De tweede sub-bijdrage is dat de IEC60076-3 vereist dat de primaire en secundaire zijde van een transformator / SST een piek-testspanning van 40 kV kunnen doorstaan (op 50 Hz voor 1 minuut). Met de kern van de transformator verbonden aan aarde, betekent dit effectief een isolatie-test voor de vermogenselektronica. Deze test heeft tevens als gevolg dat *zowel* de middenspannings-kant, als de laagspannings-kant,

zorgvuldig ontworpen moet worden betreft geometrie, isolatie, kruipafstand, en luchtwegen.

Een SST prototype is ontworpen, getest, en gebouwd als een onderzoeks platform. De vermogens elektronica architectuur selectie is in grote mate beïnvloed door de beschikbare halfgeleider-schakelaars en diens verliezen. De firmware en regellussen zijn geïmplementeerd in MATLAB Simulink om de leercurve voor toekomstige onderzoekers te verlagen. Het SST onderzoekplatform is getest en functioneerd naar verwachting.

Deze thesis concludeerd dat het voor SSTs noodzakelijk is om ook te voldoen aan de geïdentificeerde testen van de IEC60076-3 standaard. Het gevolg hiervan is dat SSTs hierdoor duurder en complexer zullen worden. Het niet voldoen aan deze test condities zou hoogstwaarschijnlijk resulteren in het cascaderend, catastrofisch falen van de SST.

3.Contents

4.Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
AV	Applied voltage test
BPF	Band-Pass Filter
BRP	Balancing Responsible Party
CAGR	Compound Annual Growth Rate
COTS	Commercial Off The Shelf
CT	Current Transformer
DAB	Dual Active Bridge
DARPA	Defense Advanced Research Projects Agency
DC	Direct Current
DSO	Distribution System Operator
DUT	Device Under Test
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ePWM	enhanced PWM (Texas Instruments terminology)
EV	Electric Vehicle
HF	High Frequency
HPF	High-Pass Filter
HV	High Voltage
IBE	Isolated Back End
IFE	Isolated Front End
IGBT	Insulated Gate Bi-polar Transistor
IVPD	Induced voltage test with Partial Discharge measurement
IVW	Induced voltage withstand test
LFT	Low Frequency Transformer
LI	Lightning Impulse
LIC	Chopped wave lightning impulse test for the line terminals
LIN	Lightning impulse test for the neutral terminal
LTAC	Line terminal AC withstand voltage test
LPF	Low-Pass Filter
MFIT	Medium-Frequency Isolation Transformer

MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MV	Medium Voltage
NDA	Non-Disclosure Agreement
NPC	Neutral Point Clamped
NRE	Non-Recurring Engineering (costs)
OLTC	On-Load Tap Changer
PD	Partial Discharge
PES	Power Electronics Substation
PFC	Power Factor Correction
PQ	Power Quality
PT	Power Transformer
PU	Polyurethane
PV	Photo Voltaic
RES	Renewable Energy Sources
RR	Reverse Recovery
SDAC	Short Duration Alternating Current
SI	Switching impulse test for the line terminal
Si	Silicon
SiC	Silicon Carbide
SSB	System Sensor Board
SSPS	Solid-State Power Substation
SST	Solid-State Transformer
STATCOM	STATic synchronous COMpensator
SVC	Static VAR Compensator
THD	Total Harmonic Distortion
TI	Texas Instruments
TOCR	Tested According to Customer Requirements
TRL	Technical Readiness Level
TSN	Time Synchronized Networking
TSO	Transmission System Operator
TVS	Transient Voltage Suppressor
VAR	Volt-Ampere Reactive
VCO	Voltage Controlled Oscillator
VT	Voltage Transformer
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Table 1 Abbreviations

5.Definitions

10 kV	The term "10 kV" is used throughout this document and it is however not a straightforward ten thousand volts. Firstly, it is implied that it is an Alternating Voltage (at 50/60 Hz). Secondly, in the Netherlands, when referencing 10 kV, the actual voltage is in fact 10,5 kV plus (or minus) 10\%. This voltage range around 10 kV is taken from the grid code and must be complied with by all parties. Since this voltage range is commonly referred to as "10 kV", the same shall be done in this document. One last thing to keep in mind for the purposes of testing standards, is that grid equipment (transformers, switch gear, and future SSTs) operating at 10 kV, all fall in the 12 kV class (again AC at 50Hz). This 12 kV class is relevant with regards to the IEC60076-3 standard that is referenced throughout this document.
The standard(s)	Throughout this document, there will be references to "the standard". This can nearly always be read as the IEC60076-3 standard (2013 version). In case of any deviation, it will be specifically noted. In the case of "standards" this can be read as the IEC60076 in its entirety with all its sub-parts. Again, in case of any deviation, it will be specifically noted, like for example in paragraph *14.1.2 Protection coordination* where the IEC60071-1 is referenced.
IFE and IBE	The terms Isolated Front End (IFE) and Isolated Back End (IBE) are coined by ETH Zürich and refer to the configuration of the SST power conversion stages.

Conventional transformer	When referring to a "conventional transformer" in this thesis, it refers to a power transformer that has a conventional design with copper (or aluminum) windings around a core, with oil (or epoxy) for insulation. Specifically, this definition will refer to power transformers at MV-to-LV distribution substations. In literature, these transformers are also referred to as a Low Frequency Transformer, or LFT. There are also other types of transformers. Namely current transformers, voltage transformers, instrumentation transformers, etc. These will be mentioned specifically when they are discussed.
System/Module	Throughout this document, the use of the term(s) "Master/Slave" will be avoided wherever possible due to the problematic (to say the least) history of slavery. This terminology has been coined during a time when it was still socially acceptable and is therefore pervasive throughout the digital communication industry. It is also fundamentally part of EtherCAT documentation, so the use of these terms cannot be 100% avoided. Throughout this work, the term(s) System/Module controllers will be used.
DC-bus	There are technically two DC-busses in an SST module (as it's currently designed). One is on the MV side between the CHB and DAB (V_{NOM} 1400V), and the other is between the LV inverter and the DAB (V_{NOM} 700V). Throughout this work, when referring to the DC-bus, it implies the LV side. For the MV side, this voltage/bus will be referred to as the MV capacitors (or MV caps for short).

Two-level vs. three-level & Three-level vs. five-level	There are two main definitions found in literature with respect to voltage levels of H-bridges. The first is related to how many voltage levels an H-bridge has. With only two voltage levels at the DC-side, the first definition states it is a two-level H-bridge. If an H-bridge has a more complex configuration with more switches and a DC-midpoint, then it is referred to as a three-level H-bridge. The other definition that can be found would refer to a normal H-bridge as a three-level H-bridge due to the voltage levels it can create. This second definition would refer to the H-bridge with a DC-midpoint as a five-level H-bridge because it can create five levels. For the purposes of this thesis, the first definition will be used. Meaning a DAB that has two H-bridges with four switches each would be referred to as a two-level two-level DAB, also abbreviated as 2L-2L DAB. Subsequently, a DAB that has eight switches on the primary side with a DC-midpoint and four switches on the secondary side, would be referred to as a three-level two-level DAB (abbreviated 3L-2L DAB)

Table 2 Definitions

6.List of figures

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8. Introduction

8.1 The electricity grid of today

Today's electricity grid is based on a strong hierarchical structure. Large power plants generate power at high voltages for transportation over long distances via the HV-grid. High voltage is effective for transporting a large amount of energy, as the losses are determined by the square of the current. High voltage therefore means low current and subsequently, low losses.

The HV-grid provides energy to the distribution grids which operate at the so-called medium voltage. The purpose of MV-grids is to provide the more local distribution of energy over shorter distances. The MV-grids cover smaller areas and interface to the low voltage grids to which (most) customers are connected. LV-grids are operated at the lowest voltages, typically 400V.

Here it becomes possible to see the aforementioned hierarchy. Energy is generated at the HV level, and distributed down to MV and LV. This is the way the electricity grid has been designed and operated from its inception. The hierarchical design of the grid has several advantages. Energy distribution is handled optimally via the voltage levels. The further the distance the energy needs to travel, the higher the voltage (and inversely, the lower the losses). This distribution model has served society well for many decades. However, the future holds several significant changes that impact the way the electricity grid is operated.

8.2 The future electricity grid

The main driver for changes in the electricity grid, is climate change [1][2]. The effects of climate change at the time of writing are becoming more and more apparent. To reverse the trend of climate change, a dramatic reduction in greenhouse gas (e.g., CO_2) emissions must be achieved. The biggest sources of CO_2 are the combustion of coal, oil, and natural gas. These three sources of energy are the

main "fuel" for the electricity grid (but also nuclear fission & fusion) and all operate on the same principle. The fuel is "burned" to generate heat, and that heat in turn, is used to generate steam by boiling water. The steam is then fed through a turbine to drive a synchronous generator to generate electricity.

Since conventional power generation is fundamentally a thermal process, and electrical processes (such as the electricity grid's power flows at the distribution level) are inherently fast, there is a mismatch in the necessary speed of control. With the future seeing more and more electrification, this mismatch will become greater. This is not to negate the merits of conventional power plants, as they are a large contributor of grid stability and inertia. Their processes simply do not allow them to solve fast fluctuations in the hierarchical parts of the electricity grid.

There are many initiatives to combat climate change, there are however several that affect the electricity the most: Renewable Energy Sources (RES), electrification of households, heat pumps, and electrification transportation via Electric Vehicles (EVs).

8.2.1 The effects of Renewable Energy Sources on the future grid

Electricity grid affecting RES come mainly in a few forms, wind energy in the form of wind turbines, solar energy in the form of Photo Voltaics (PV), electrification of households, and heat pumps. Both wind and PV are stochastic in nature and are generally connected to the bottom of the electricity grid's hierarchy (large scale wind / PV energy can be connected higher in the hierarchy and is a topic out-of-scope for this thesis). Taking PV as an example, a neighborhood or even an entire city that has PV on every roof, would push in very large amounts of energy into the "bottom" (LV-side) of the electricity grid when the sun shines, and would all but cease to produce energy when a cloud rolls in.

It is this large stochastic variance in energy flow, that causes problems on the distribution transformers in MV-to-LV substations.

In the current grid, energy is traded on the day-ahead market and assumed reasonably stable (and predictable) for a given time period of the next day. The resolution of this time period is 1 hour and in order to be more accurate with matching supply to demand, increases in resolution have been proposed [3]. But even an order of magnitude increase in resolution (assuming perfect predictions are even possible), would be vastly slower than the electrical processes occurring with PV systems. So, in the current grid, an estimated amount of energy is generated for a given hour of the day. During that hour, that energy would result in 230V at the customers. PV, however, would cause significant deviation from this estimate within a very short period of time (e.g., <1 minute, seconds even). With energy suddenly being supplied directly on the LV grid, the voltage at the distribution transformer will increase. DSO's can compensate for this increase using the tap changers on the transformer, but with a limited speed (typically only a few times per day), resolution, and limits. This also goes for the BRPs that try to balance load and demand during the day, and the increasing RES / decreasing thermal production/inertia poses an increasing challenge.

In (simplified) conclusion, RES will result in an increase in voltage (and fluctuations) on the MV-to-LV distribution transformers that cannot respond to fast voltage changes right now (neither with tap changers, nor changing coal/oil/gas/fission power plant output, nor with any BRP of mechanisms like gas fired plants or rotating reserve).

8.2.2 The effects of electric vehicles on the future grid

The other significant contributor to the electricity grid's future, are EVs. These are essentially batteries that need charging to keep the cars driving. Charging these batteries will result in a very large swing in energy consumption. The rate of consumption is dependent on the charging rate of the battery. With the population currently being used to 1~2 minutes at the gas station for 1000km of range, will likely lead to a desire for higher charging rates,

rather than lower. While not approaching the "recharging" rates of conventional cars, a common "supercharger" from Tesla is advertised as giving 200km of range in 15 minutes. Taking these Tesla superchargers as a metric, the power consumption of charging a single Tesla car battery can be anywhere from 72kW to 250kW. Future charging stations will likely see higher power levels to cut down on charging times (or increase the amount of simultaneously charging cars). Even on the low end, a future city that only has electric cars, would see massive fluctuations in power consumption. Especially in the periods after rush-hour, when the cars are plugged in to recharge. While an average power consumption can be "reasonably" predicted for the day-ahead market's energy generation, the exact times that the cars will be plugged in for recharging, is currently limited. This will lead to the voltage at the MV-to-LV substation distribution transformers dropping fast.

In (simplified) conclusion, EV will result in a decrease (and fluctuations) in voltage on the MV-to-LV distribution transformers that cannot respond to fast enough to fast voltage variations right now (neither with tap changers, nor changing coal/oil/gas/fission power plant output, nor with any BRP of mechanisms like gas fired plants or rotating reserve).

8.3 Challenges

It is estimated that 5% of the Dutch customers will see their voltage limits (230V ±10%) exceeded by as early as 2025, with this percentage increasing to even 25% over the next 10 years (by 2033) [4][5]. The consequences of theses limit violations are equipment simply failing to operate when voltages are too low, and downright damaging / breaking when voltages become too high.

A considerable challenge for the distribution grid, will be to keep these voltages within their legal limits.

Another factor that could be noted, is the influx of power converters and the harmonic distortion that they bring. The one thing that PV, wind energy, and EVs have in common, is that they

will interface with the electricity grid via a power converter. Each of these power converters will be made up of some form of switched power electronics. This means that each of these power converters will introduce harmonic distortion into the 50Hz/60Hz sine wave. This increase in total harmonic distortion (THD) could be magnetically coupled back to the MV grid through the MV-to-LV distribution transformers, potentially further causing problems in the electricity grid. Harmonic distortion may not be as big of an issue as voltage fluctuation, however, because there are standards (e.g., IEC61000) governing the limits for some of these power converters.

Overcoming the large amounts of THD will be a challenge for the distribution grid, though to a lesser degree, since higher harmonics do not propagate great distances. These converters all have controllers internally that could potentially also be used to solve power quality problems in the grid. As of yet, however, these converters are not interconnected / coordinated to achieve this.

8.4 Overcoming the challenges

The previously described challenges lead to the first research question of this thesis.

1. **Given the challenges the grid faces with increased voltage fluctuations, what solutions exist?**

With the challenges to the electricity grid presented, MV-to-LV distribution transformers are one of the focal points for solutions (other research focusses on harnessing large amounts of inverters to solve power quality issues through interconnection / coordination). This is due to the hierarchical proximity of the distribution transformer to the source of the "problem". Compensating for voltage fluctuations at the HV level is not practical because at this level, the main sources that have control over the grid are large scale power plants that are fundamentally large generators powered by steam turbines. Their inertia (though

offering stability / inertia) makes fast compensations in the hierarchical lower parts of the electricity grid impossible.

When looking at the MV grid, there are several solutions possible.

1) The first solution is more grounded in business as usual. This would see the MV-to-LV substations "reinforced" with additional conventional distribution transformers and cables in parallel. These cables and conventional transformers have long lifetimes and DSO's will have less issues with planning upgrades and/or reinforcements to the grid. The problem is not fully solved, however. Reinforcing the grid means lowering the impedance, which results in a lower voltage swing at the same current levels. This would also slightly reduce the effects of harmonic distortion, as a lower impedance will also lower the amplitudes of the voltages (again, at the same current levels). A significant drawback is that it does not fully solve the problem, even if the electricity grid is completely doubled and its impedance halved (this is without even considering the prohibitive cost). It also only postpones the problems with voltage swings and harmonic distortion.
2) The second solution is the use of mechanical or solid-state on-load tap changers (OLTC). These come in a few forms. The first is a mechanically based tap changer. The second is commonly a thyristor based OLTC that is a direct replacement of the mechanical switches of the past. These are an improvement to the mechanical switches as there are no longer any moving parts requiring maintenance. The main drawback is that the voltage changes happen in discrete steps, causing harmonic distortion and a finite number of voltage steps.
3) The third solution is a full replacement of the distribution transformer. The SST is considered a technology that, in theory, can solve both the voltage fluctuation challenge as well as the harmonic distortion challenge. Its main drawback is the cost of the SST, as well as the reliability. There

isn't any data publicly available on either aspect, yet reasonable assumptions can be made. The high number of components in an SST make the failure rate undoubtedly higher than that of a conventional transformer. The high maturity of the conventional transformer (50 to 100 years) means that an SST can also not compete on cost in the near term future. The biggest advantages of the SST from a power quality perspective lie within its ability to control the voltage, actively filter out harmonic distortion, and potentially enable peak-shaving via electric energy storage. These will initially come at the cost of reliability, efficiency, cost, and potentially power density. Over time, economies of scale can reduce the cost of SST modules and after a learning curve for DSO's, improved standardization and tests will likely reduce these initial costs.

For scientific research, solutions one and two are less interesting due to their maturity level. The most interesting solution is option three, the Solid-State Transformer. This will be the subject of research for this thesis and answering the first research question.

8.4.1 Future SST market share

As a result of the changes that the electricity grid faces in the future, and the SST becoming a key technology for enabling renewables, the future of SST market looks bright. The market value of SST's is expected to grow more than 300% by 2028 at a steady CAGR (Compound Annual Growth Rate) of 16,9% [6]. This increase in the SST market will present a scenario where more manufacturers start to enter, increasing competition, and consequently driving down the cost of SSTs.

8.5 The DSO's business case

Currently, it is difficult for the DSO to make a business case for the future. While the cost of over-dimensioning the grid's capacity are known, they cannot yet be weighed against the costs (and

potential benefits) of an SST. To be able to make a more realistic business case, designing and implementing an SST research platform will provide the needed insights. Insights into cost, functionality, effectiveness, efficiency, and performance.

8.6 Project descope

To aid in reading and interpreting this thesis, it is important to mention that a significant amount of hardware was descoped (approximately a year before the end of the project). In 2021, the design of the full SST prototype consisted of 296 switching devices, distributed over 18 power electronics modules, mounted in five industrial COTS cabinets. The entire prototype would be a 200 kVA, three-phase SST and it would weigh an estimated 2200 kg while being almost 10 meters in length. This turned out to be too ambitious for the remaining project time and as such, it was descoped to a single-phase, 35 kVA prototype research platform, consisting of three SST modules. In this thesis, the reader will find both the original "full" SST design, as well as the implemented SST research prototype. The author of this work posits that the conclusions and contributions in this thesis still hold, despite of this descope.

8.7 Concluding remarks

The electricity grid faces challenges in the future with respect to its voltage levels, fluctuations, and harmonic distortion. An increase and decrease of the distribution transformer voltage levels can be expected due to increased renewables, electrification of households, and EVs. These voltage fluctuations are expected to occur at a faster rate than can be compensated with via power plants or other currently available means.

The first research question was:

1. **Given the challenges the grid faces with increased voltage fluctuations, what solutions exist?**

This chapter concludes that SSTs are the most interesting solution from a research perspective to investigate further.

This leads immediately to the second research question of this thesis:

2. **Given the challenges the grid faces with increased voltage fluctuations, what SSTs have been described in the literature as state-of-the-art?**

The answer to this question will be investigated in the next chapter (9 Literature study).

9.Literature study

The previous chapter describes the challenges the grid is facing and has concluded that the SST is the most interesting technology from a research perspective. With the SST being established as the focus of this thesis, the next research question is investigated in this chapter.

2. **Given the challenges the grid faces with increased voltage fluctuations, what SSTs have been described in the literature as state-of-the-art?**

From this second research question, several sub-questions can be formulated. These sub-questions are listed below. The paragraph numbers in which these research sub-questions are answered are listed on the right side between parentheses.

a. What technologies enable the SST? (9.1)
b. What is an SST and how is it made? (9.2)
c. Have any SSTs been prototyped? (9.3 & 9.4)
d. What gaps exist in the literature? (9.5)

This chapter holds the literature review of this thesis and describes the state of the art. The SST is an emerging technology that is becoming increasingly more feasible due to breakthroughs in wide bandgap switching device technologies. These will be investigated first. This will then be followed up with an overview of the prototypes that have been built throughout the world (most of which have been built during the last decade).
Lastly, this chapter will identify the gap in the state of the art being that SSTs have yet to be designed according to a TRL that allows them to be put in the grid. In particular, according to the IEC60076-3 standard.

9.1 The core technologies to enable the SST

The ambition to build a convertor to replace a conventional transformer has existed for a long time, with early patents already arising in 1968 [7]. The Cascaded H-Bridge topology was already described in a patent 1969 [8]. While the core topologies for SSTs have been theorized, the core technologies to build a practical SST, however, were still far off. In the period since those early patents, prototypes have been designed in simulations [9][10][11][12][13][14] [15]. With some even completing the design stage, but never becoming fully realized [16]. Additionally, SSTs have also been described as a mathematical model only in [17]. SSTs hold significant promise in terms of flexibility, as future DC-based renewables, or other DC applications (e.g., electric cars, trucks, busses) can be connected directly to the DC-bus that is present in almost all SST designs [18]. This flexibility is a significant advantage that SSTs hold over conventional transformers, and it is even further extended with the ability to have multiple inverter stages, one for each outgoing feeder (see Figure 9-1 and Figure 9-2), as well as leveraging the DC-bus for connecting DC technologies directly (such as EVs or PV).

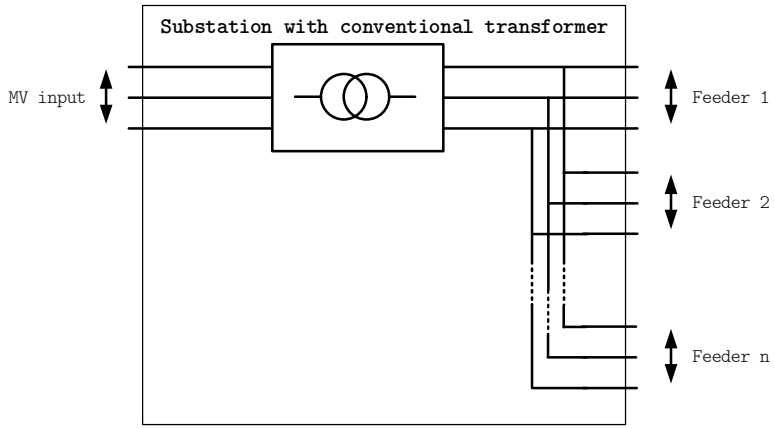


Figure 9-1 Controllable feeders in conventional substation

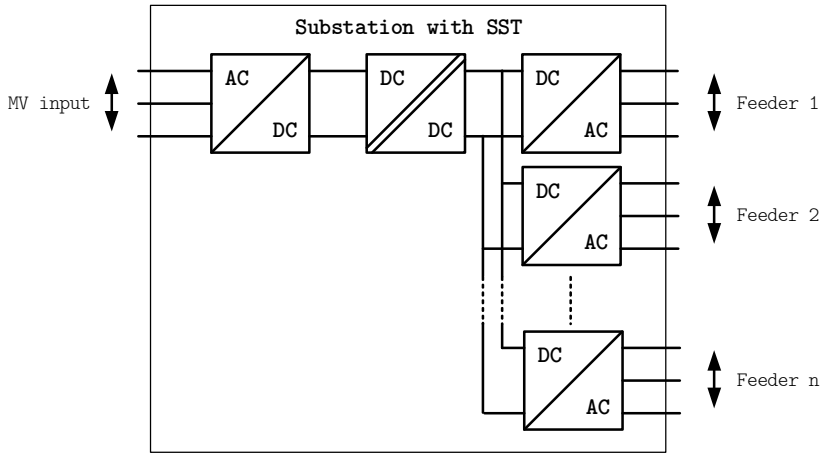


Figure 9-2 Controllable feeders in substation with an SST

A conventional transformer is limited to controlling only the voltage levels of all its feeders simultaneously through its tap-changer. The breakthrough advantage of an SST is that each feeder can have its own voltage setpoint. So in situations where a substation has one feeder has a long street connected with houses that have only PV, and another feeder that has a long street connected with a lot of EV owners, the conventional transformer can only set a single voltage level that "hopefully" covers both extremes of voltage rise & drop respectively (see Figure 9-1). Whereas an SST has the ability to individually set the voltage level for each feeder, ensuring each stay within the limits of the grid code (see Figure 9-2).

9.1.1 Silicon Carbide and Gallium Nitride

Two new switching device technologies have emerged in relatively recent times, and in the last decade or so, have become commercially viable. These are Silicon Carbide (abbreviated SiC) and Gallium Nitride (abbreviated GaN) switching devices. These both represent a significant improvement in the switching characteristics of power electronics switching devices such as IGBTs and MOSFETs.

Both technologies improve specifically the losses of these switching devices by offering 1) lower conducting losses, and 2)

lower switching losses. The technologies are not identical however, and each offer a specialized improvement in their characteristics.

Even though the SST is not specifically looked at as an application, the effectiveness of a selected technology depends on it [19]. This source, however, does look at traction systems, which display very high similarity to SSTs.

1. As is shown in [19], GaN switching devices offer greater switching speeds than SiC, but their blocking voltages are more limited. This actually makes GaN switching devices especially suited for the inverter application/section of SSTs, as proposed in [20]. Additionally, a 1MHz/2kW prototype H-bridge has been built in [21], and showed a very high efficiency of 98% through Zero Voltage Switching (ZVS). Using the proposed topology, however, would not allow for bi-directional power flow (an essential requirement for any grid-placed replacement of the conventional transformer.
2. With regards to SiC switching devices, [19] shows that higher blocking voltages are more common than in GaN. The tradeoff is that the switching speed of SiC is slower, which results in a lower efficiency at higher switching frequencies when comparing to GaN. The SST at its core, requires both high blocking voltages and high efficiency.

As will be posited in chapters 10 and 11.1, the IEC60076-3 standard compliancy requires very high voltage handling capabilities. Commercially available options for both IGBTs and MOSFETs are explored in chapter 11.2. This exploration led to the conclusion that the average blocking voltage capability of GaN and Sic switching devices is limited to around 600V and 1200V respectively. This conclusion is also confirmed in [19], with one SiC switching device of 1700V being commercially available. With IEC60076-3 constraining the SST to very high voltages, SiC devices become the natural choice to limit the amount of switching devices, complexity, and probability of failures when designing an SST. The efficiency gains of utilizing GaN compared SiC, is too little to justify their use.

With switching devices being more readily available at the wafer-level, there is actually very little research into the voltage handling capabilities of the packaging for accommodating SiC switching devices. While there is research into the thermal effects, and finding substrates that have similar thermal expansion coefficients to SiC [22], the only research into the insulation aspects of wide bandgap device packaging has been found in [23]. As will be shown in chapters 10 and 11.1, the insulation of these switching devices is a design aspect that needs to be carefully considered. An example of a package for a high voltage switching device can be seen in Figure 9-3.

Figure 9-3 Wide bandgap device packaging [23]

The key design feature of wide bandgap device packaging is the creepage & clearance distances necessary for handling the high voltages. In SSTs, this affects the design regarding the input voltage at the MV side.

9.2 SST conversion stages

SSTs designs come in many forms, and each contain different (types) of stages. For the purposes of this thesis, a subset of all these design possibilities has been identified and will be explained further in this document. This subset is the Isolated Back End (IBE) configuration of the power electronics (the terminology used

in this thesis follows the terminology proposed by [24]). It should be noted that other configurations have been evaluated during the design phase, see Figure 11-4 in chapter 11.2 for those topologies. The IBE power electronics configuration comes in many forms, but mainly comes in three, basic, energy conversion stages. Each of these will be touched upon in the subsequent paragraphs with their relation towards the state-of-the-art. These three conversion stages are shown in Figure 9-4 and are the:

1) **Active rectifier/inverter** stage (depends on the power flow, the technology is nearly identical)
2) **Isolation** stage (commonly in the form of a Dual Active Bridge (DAB)
3) **Inverter** stage (for making the LV grid voltage)

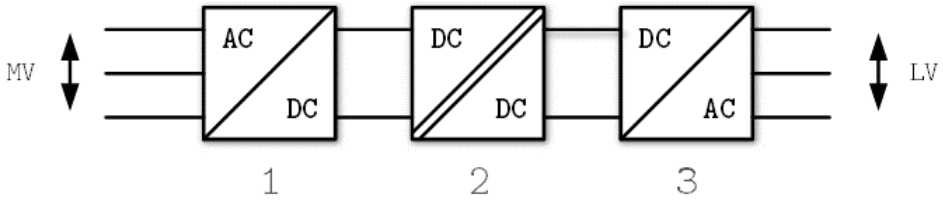


Figure 9-4 Generalized SST power conversion stages

9.2.1 10 kV inverter/rectifier prototypes

The first of the three power conversion stages is the active rectifier. Its purpose is interfacing with the MV grid and ensuring the draw of a sinusoidal current. This is important, because otherwise the SST will introduce PQ (power quality) issues. Which is in essence, the very reason for the SST being conceived. There are examples where this configuration is suggested [25], but it should be noted that those could never be made compliant to the IEC60076-3 (see chapter 11.1 for an explanation why). This is where the first gaps in the state-of-the-art are identified, being the voltage levels for which SST prototypes have been designed. For example, a prototype boost converter has been built in the past that utilizes experimental SiC switching devices that have voltage

withstand capability of 10 kV [26]. Mostly, the investigation focusses on the characteristics of the switching device itself. A more practical implementation has been found in [27]. Their research focused on building an active rectifier prototype using 10 kV SiC MOSFETs. They recognize the challenges that come with working with 10 kV and focus on a lot of the practical aspects such as parasitic effects, switching losses, filter winding techniques, among other things. Their prototype (and their research), however, does not focus on the input conditions that may occur in the MV grid. Specifically, the double input voltage test condition that, as will become apparent in chapter 10, are necessary according to IEC60076-3. This reveals the same gap in the state-of-the-art. Such grid conditions can for example occur when switching capacitor banks.

While not a prototype inverter, a 15 kV gate driver is designed and tested in [28]. Their research identifies the lack of protection mechanisms to protect the MV switching devices and a saturation detection capable driver is developed. The paper states that these new 15 kV SiC switching devices pave the way for non-cascaded topologies, such as suggested in [25].The isolation level used for the driver, is set to max. 20 kV, which is again insufficient to meet the IEC60076-3 standard (as will become apparent in chapter 10).

9.2.2 10 kV Dual Active Bridge converters built

The isolation stage of SSTs is commonly made up of a Dual Active Bridge (DAB). The DAB is more likely to be employed as a conversion stage, rather than forming the SST itself. There are exceptions however, like in [29]. In this research, one side of the DAB is directly interfaced with the MV grid. This configuration is known as the Isolated Front End topology (IFE) The paper describes how a subsection of the SST is prototyped. The main difference between this topology (IFE) and the more commonly used SST topology Isolated Back End (IBE), is the absence of a separate Cascaded H-

Bridge (CHB) on the MV side. See the simplified SST topologies in Figure 9-5 below.

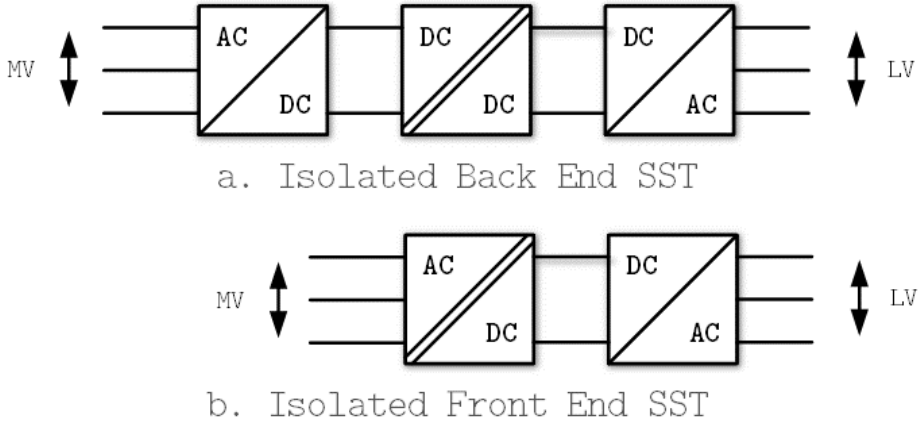


Figure 9-5 Isolated Back End (IBE) vs. Isolated Front End (IFE) SSTs

The most significant advantage of the IFE compared to the IBE is the reduced amount of MV-grid facing switching devices. This is important, because this is the most challenging side of SSTs due to the large voltages. The reduced amount of switching devices also means that there will be less drivers needed, as well as less sensors. The main drawback of the IFE is counterintuitively the increase in complexity. The IFE requires the first / MV grid facing H-bridge to be responsible for two tasks. One, drawing a sinusoidal current from the MV grid, and two, generating an alternating voltage directly for the DAB transformer. This double task for the first H-bridge inherently presents increased control complexity (as well as potentially conflicting optimization problems). **It is for these reasons that the prototype built for this thesis was chosen to be an IBE.** Two 1MW Back-To-Back (BTB) converter designs for the Japanese electricity grid are described in [16]. One for a Si based design, and one for a SiC based design. The paper details a bi-directional DC-DC converter that never made it to a prototype, highlighting the difficulties that come with developing an SST. For example, the paper shows the detailed design problems that come with switching such high voltages in an IFE topology. Specific

issues they encountered were excessive avalanche energies in external diodes, resulting in their destruction when switching at 1,6 kV.

The DAB as a power electronics switching topology contains a transformer in the middle for isolation of the primary and secondary side H-bridges. The DAB topology allows for a lot of flexibility in control. To name a few:

1) As there are two bridges, each can have a different PWM strategy or duty cycle.
2) The switching frequency of both bridges can be changed simultaneously. For example, it can be lowered to lower the switching losses during certain load conditions.
3) The bridges can be phase-shifted with respect to each other. This is commonly used to transfer power.
4) The topology is fully bi-directional when implemented with switches on both sides of the transformer (as opposed to having one side with diodes).

Since an SST will have to ensure isolation between the MV & LV grids, the DAB is an obvious choice with its insulation transformer. In [30], the DAB is recognized as a core circuit for SSTs, and they describe a prototype that they have built. There are two limitations to the presented work, and those are that the designed prototype is for traction systems and that the peak input voltage is "only" 6600 V. It should be noted that this input voltage could be extended (if applied in electricity grids) in three-phase systems to a peak voltage of 6600V $*$ $\sqrt{3}$ by configuring the SST's grid facing converter in wye/star while the MV grid is in delta. The built prototype, however, demonstrates the feasibility of DABs as a core component for SSTs.

Another relevant DAB prototype is described in [31], where a 15 kV SiC based DAB converter prototype is presented. What is remarkable, is that on the MV side, there is a DC bus that is operated at 22 kV, and that the topology of the switching devices uses clamping diodes to effectively series the 15 kV SiC switches. The main

drawback from the presented configuration is that there are only 5 switching levels, with no possibility of interleaving. This results in a much larger MV grid filter being required to comply with the THD limits set forth by the grid code. The current ripple is especially visible with an L-filter of 440uH (see Figure 12 in the paper). This particular prototype, however, would actually be compliant to the IVW & IVPD tests of the IEC60076-3 (see paragraphs 10.2.2.9 and 10.2.2.10 for further details). It would not be compliant to the LTAC or AV tests (see paragraphs 10.2.2.5 & 10.2.2.8 respectively), due to the insulation between the two converters (which is only mentioned in passing along the lines of, DABs having transformers that have isolation).

9.2.2.1 SST isolation transformers for MV to LV

When evaluating existing DAB designs for SSTs, there is one component in particular that requires special consideration, the DAB transformer. The DAB transformer is arguably the most critical component of the SST, as the bulk of the isolation between the MV & LV grids revolves around it. This is because this component is the only feasible technology (at these power levels) for ensuring the isolation of the MV & LV electricity grids when replacing a conventional transformer, and an insulation failure would connect the two grids directly. In the context of the Dutch electricity grid, these two are galvanically isolated in most places, and consequences of that isolation failing, could result in a catastrophic loss of the SST.

While transformer design itself is a mature technology, the design of HF (High Frequency) DAB transformers for SSTs is not. In particular in the context of the IEC60076-3 test voltages of the IVW & IVPD tests (see paragraphs 10.2.2.9 and 10.2.2.10), all designs encountered in literature would not be compliant.

The work presented in [30] references a transformer that needs an insulation level of 35 kV. The referenced work is [32] and in fact,

states a 38kV insulation level. This would still not be compliant as IEC60076-3 states RMS voltages of 28 kV for the IVW & IVPD tests, meaning peak voltages of ≈39,6 kV). The paper does not state where the insulation level was obtained from. It is possible that this was obtained from a standard that was for traction systems. More importantly, the isolation value and test conditions are nearly the same as in the IEC60076-3. The isolation was obtained using MV cabling for the MV-side winding of the DAB transformer. This is a pragmatic approach to the isolation challenge of SSTs, as it avoids having to reinvent an insulation material / strategy for the DAB transformer. Its main downside, however, is the reduced power density / increased volume that comes with every winding being individually insulated. This as opposed to having all MV-side windings encapsulated within a single insulation layer.

Other works have typically designed the insulation level of the DAB transformer to match the MV input voltage. In [33], the main focus of the paper is the insulation of the DAB transformer. It specifically states the risk of partial discharges due to the voltage stresses on the DAB transformer and proposes a novel resistive shielding to counter them. The selected insulation level, however, only insulates up to 30 kV. And this 30 kV is only this high due to a factor 2x margin to account for material deficiencies. The stated requirement is 15 kV, which is also the input voltage of the SST for which the DAB transformer is designed. The same is done in [34], where the input voltage is simply taken as the isolation value. Such designs have no margin for IEC60076-3 test voltages or grid conditions that result in exceeding voltages.

During the search for SST (DAB) transformer designs, no sources were found citing the IEC60076-3. The closest source obtained, is [35]. In the presented work, an adjustable speed driver transformer isolation according to IEC-61800-5-1 is taken for the design. This is a standard for traction systems and does consider a safety factor, but it is not as high as the IEC60076-3. The transformer

itself is designed for a 13,8 kV_{AC} MV system. The SST converts it to 22 kV DC and transformer reduces 22 kV_{DC} to 800V_{DC}.

9.2.3 700V DC/AC inverters built

The last and final stage typically seen in SSTs, is the inverter stage. The input voltages for these inverters range from 1 kV to >350 V, and the output voltage is of course the LV AC grid voltage. This technology is mature and has been developed many times for Renewable Energy Sources (RES) such as PV and wind energy.

The only new aspects to these inverters for SSTs are the likely incorporation of more GaN based switching devices, as these are suitable for the lower voltages, and the increased achievable efficiencies.

For the purposes of this PhD, the inverter stage was only investigated in the form of finding Commercial Off The Shelf (COTS) devices that would be the easiest to integrate. Since the technology is so mature, many inverters were found. The starting requirement was to take a solar inverter. That turned out to be not suitable because solar inverters are grid-following, and not grid-forming.

9.3 Existing SST prototypes

This paragraph lists the prototypes found during the literature study. It provides an overview of the SST status as a technology. The literature study highlights that SSTs are roughly around Technical Readiness Level four (TRL4). During the project, news was shared through the consortium partners that a prototype was built in Korea and placed in an electricity grid [36]. This has raised the TRL to five in 2020.

9.3.1 UNIFLEX 2009)

Uniflex was built by University of Nottingham and industry partners in 2009 and is one of the earliest found SST prototype that was built [18][37][38]. Its configuration is identical in several ways to the developed research platform of this thesis. It consists of

four cascaded H-bridges on the MV side in a floating NPC configuration. There are a few interesting aspects to this prototype.

1) Interleaving on both sides
   The first is that both the MV side, and LV side are utilizing interleaved switching to obtain their waveforms. This ensures a lower harmonic current distortion on both sides.
2) Hybrid centralized control
   An interesting aspect is that the control of the MV side CHB and LV side CHB are centralized. With the DAB switches being controlled by an individual FPGA that only serves to keep the voltage levels on both sides of the DAB equal. All the other 96 switches are connected directly via a fiber optic to a central processing unit consisting of DSPs. This centralized control of the SST's periphery allows for a deterministic behavior of the in- and output powers. The distributed DAB control loops could cause instability when interacting with the centralized control, but the aspect of network delays is eliminated since all other switches are each individually connected to a single fiber optic. The main drawback of this approach is the large amount of fiber optic connections that can each individually fail.
3) MV input voltage capability
   The MV input voltage handling capability is not directly stated. The system as a whole, however, is designed to be modular so that it can be scaled up to input voltages of even 30 kV. In such a configuration the Uniflex could comply with the IVW & IVPD tests of the IEC60076-3 standard (see paragraphs 10.2.2.9 and 10.2.2.10 for details).
4) MV / LV isolation capability
   The isolation level between the primary and secondary sides of the Uniflex is not stated. There is mention of using MV cabling to generate an isolated voltage supply for the gate drivers. This was, however, only in relation to the "highest" switches of the stack, and not for galvanically isolating

the MV & LV grids from each other. As such, the Uniflex is unlikely to be compliant with the AV test of the ICE60076-3 (see paragraph 10.2.2.8 for details).

In summary, this prototype could be compliant with parts of the IEC60076-3 but is unlikely to be compliant in its entirety.

9.3.2 SiC-Enabled Solid State Power Substation (2011)

In 2011, an SST was designed by Huazhong University of Science and Technology for the first time using Silicon-Carbide switching devices [39][40]. The use of SiC is a technological enabler for the SST in the sense that it can increase efficiency and consequently, increase power density. There are not many details on this "SSPS" (Solid-State Power Substation), only these two papers that seemingly relate only to the implemented 10 kV switching devices. The reason for this might be that it is funded by a DARPA program called "*Wide Bandgap Semiconductor - High Power Electronics (WBGS-HPE) Phase II program*". Some key aspects of this prototype are listed below:

1) 10 kV switching devices
   The most novel aspect of this prototype is the used switching devices (and diodes). These are all experimental switching devices that have blocking voltages of 10 kV. These enable the prototype to contend with less cascaded H-bridges to handle the medium voltage.
2) MV input voltage capability
   There is only a mention of the specifications of the SSPS in [41]. The input voltage is listed as 13,8kV and it is unknown how much this design is over-dimensioned.
3) MV / LV isolation capability
   The isolation of the SST is again not listed. There is no way to know what the isolation levels. The best estimate that can be given is that the SSPS is intended for grids on ships. Unless the military electricity grid standards are more stringent than the IEC60076-3, this means it is unlikely to comply with the isolation requirements of the standard.

With so much of the prototype being unknown, it is hard to prove or disprove compliance with IEC60076-3. The designed prototype is 300 kVA with the intent to scale it up to 1 MVA. It is unknown when this was achieved. The first known prototype that reached the 1 MVA level, is described in the next paragraph.

9.3.3 MEGACUBE (2013)

In 2013, ETH Zürich in Switzerland collaborated with ABB to build an SST prototype [42], [43]. The power level of this prototype is 1 MVA and it could be stated that it was the first scientific prototype that reached power levels comparable to conventional power transformers. Some key aspects of this prototype are listed below:

1) DC-DC converter
   The first key aspect is that it is a DC-DC converter. Meaning that there is no MV_{AC} to deal with.
2) IFE switching configuration
   What is very interesting of this prototype is that it is an IFE configuration [44]. This means the researchers have chosen a topology that minimizes the amount of MV "grid" interfacing switching devices. Since there is no input rectification stage, the reduced amount of switching devices does not result in any sinusoidal current needing to be drawn from the "grid". This optimization (of minimizing switching devices, however, does come at the cost of optimization of the DAB's efficiency as the optimal waveforms would normally be generated with a full bridge on both sides. Potentially, it becomes more difficult to achieve ZVS & ZCS (Zero Voltage Switching / Zero Current Switching; methods for reducing switching losses and increase efficiency) over the full load range. Additionally, there is the balancing of the capacitors on the input side to ensure the switching devices do not see their breakdown voltages exceeded.
3) MV input voltage capability

The MEGAcube is dimensioned for 12 kV input voltage on the MV side, distributed over 6 modules that each handle 2 kV. There is no mention of the switching devices used, thus it is difficult to ascertain how much voltage this prototype could actually handle on its input. There are, however, several mentions of the maximum input voltage. Such as the maximum expected MV line-to-line voltage being 20kV, the required isolation level of the MV IGBT drivers needing to be 20kV, and referencing a different prototype that has 19,5kV input handling capability. Despite that, it is not possible to conclusively determine that the prototype is not compliant to the IVW & IVPD tests of the IEC60076-3 standard (see paragraphs 10.2.2.9 and 10.2.2.10 for details). While unlikely, it is not possible to definitively conclude that the standard was not considered for this prototype at all.

4) MV / LV isolation capability

The last aspect to consider of this prototype is: Is this prototype potentially compliant with the IEC60076-3 standard's AV test? The answer is likely "no", as there are no mentions of it in the found literature. From [44], an image of one of the prototype's modules shown below it can be seen that isolation was part of the design considerations. The fiber optic connections are clearly visible on both sides of the dual active bridge. These are connectors for plastic fiber optic connections and are also used in the prototype of this thesis work.

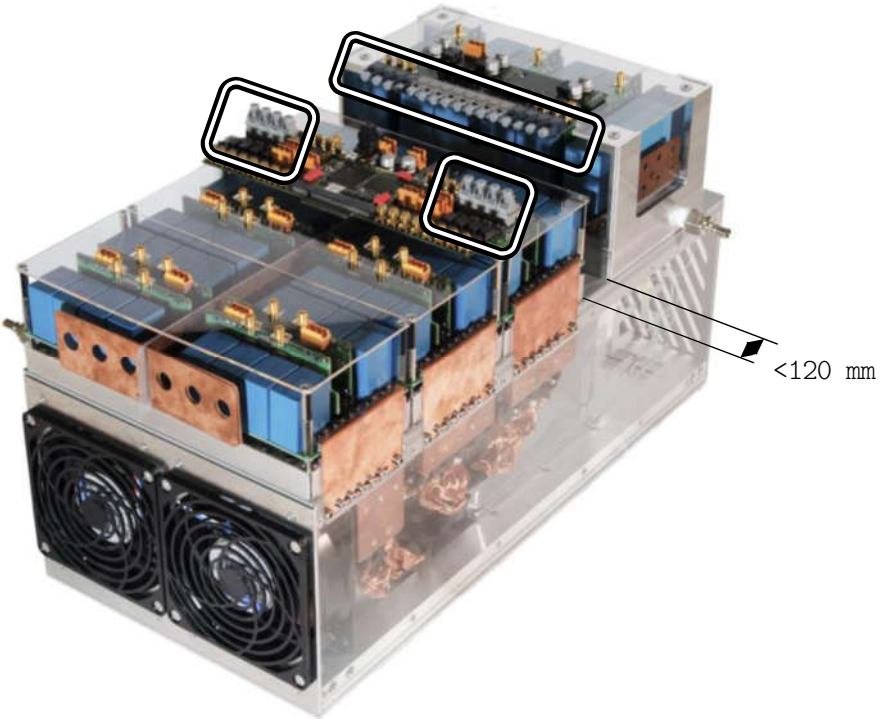


Figure 9-6 One of the MEGAcube prototype modules and its fiber optics [44]

There is information available on the design of the isolation transformer found in [42]. There, in table 1, it is stated that an isolation value between the primary and secondary side should be 100 kV_{DC}. The origins of this value are not stated, and it is unknown if these have been obtained from a standard. When relating this value to the IEC60076-3, this design would be compliant with respect to the isolation of the transformer.

This design is not compliant, however, because what is also visible from the image, is the physical distance between the primary and secondary side of the DAB. While there are no dimensions listed, it is clearly visible that the terminals on the primary and secondary sides are much closer than the 120 mm clearance requirement that is stated by the IEC60076-3.

It can once more be concluded that this prototype has not been designed with compliancy of the IEC60076-3 in mind. As can be deduced, the design is not compliant with regards to the MV input voltage and the clearance requirements of the IEC60076-3.

9.3.4 Electronic Power Transformer (2016)

Huazhong University of Science and Technology in Wuhan, China, published the results of their prototype in [45]. It is a 10 kV to 400 V prototype that has a power capability of 500 kVA. This prototype can also be considered to have a "commercial power level". While smaller transformers exist, a 250 kVA transformer is considered "small" and a 400 kVA, 630 kVA, 800 kVA (or even 1000 kVA) is considered "common" (within the context of the Dutch electricity grid). Highlighted below are key aspects of this SST.

1) IBE configuration
   The prototype uses an IBE switching configuration with modules being made up of the typical power conversion stage configuration (such as seen in Figure 9-4).
2) No bidirectionality
   There is one compromise made with respect to cost, and that this the omission of switches on the secondary side of the DAB. In their place, diodes have been used. This offers significant simplification with respect to control and implementation because there are four switches less to deal with. The drawback of this design choice is that it sacrifices bidirectionality.
3) MV input voltage capability
   The presented prototype has been constructed using IGBTs on the MV input side that have a breakdown voltage of 3,3 kV. With six modules in series, this means that the total handling capability of the medium voltage is 6 * 3,3 kV = 19,8 kV. The prototype this is also configured on the MV side as a floating NPC. This means that at a theoretical maximum breakdown voltage of 34,29 kV, the prototype is theoretically capable of handling the IEC60076-3 input test

voltages ($V_{test\ IVW\&IVPD}$ = 33,94 kV_{PEAK}) with a margin of 1,1%. There is, however, no mention of any (other) standards and / or compliancy.

4) MV / LV isolation capability
   Section 3c of the paper discusses the DAB transformer (the researchers refer to it as the MFIT / Medium-Frequency Isolation Transformer). This section recognizes the voltage stresses across the transformer being determined by the stresses between the MV & LV grids. As such the researchers state that the isolation level should be "considered as a 10-kV device". This recognition, however, does not directly imply a compliance to the IEC60076-3 AV test conditions. It is unfortunate that there is no more detailed number available in literature.

In conclusion, this prototype may, or may not be compliant with IEC60076-3. While the researchers have recognized the need for insulation to be at 10 kV device levels, there is no mention of any detailed testing of the insulation up to the required 28 kV_{RMS} levels. With the MV input over-dimensioned a factor of two, it seems that the thought process was to have a safety margin on the design. For switching devices, a factor of two over-dimensioning of the breakdown voltage is not uncommon. If compliancy with the standard was intended, the designed margin of 1,1% would be insufficient as tolerances in test equipment would already result in a catastrophic destruction of the SST. It can be assumed with reasonable certainty that the designed prototype would not survive compliancy testing of the IEC60076-3 and would therefore not be compliant.

9.3.5 S³T (2016)

2016 also saw the publication of the Swiss Solid-State Transformer (S^3T) prototype results by ETH Zürich [24]. This prototype is built using 1700 V SiC switching devices that have a very low $R_{DS\ on}$ and are thus very efficient. This prototype has been the main focus of ETH Zürich and has been often discussed in their publications.

1) IFE configuration
   This SST is optimized to minimize the MV interfacing switching devices by utilizing the IFE topology. With only 8 switching devices interfacing with the MV, this design has optimized the MV side complexity.
2) MV input voltage capability
   The designed MV input voltage is only 6,6 kV. This immediately makes the design non-compliant with the IEC60073-3 IVW & IVPD tests. What is equally interesting is that the design for 6,6 kV is made up of the blocking voltages of four 1,7 kV switching devices. Meaning that the total blocking voltage of the SST is 4 * 1,7 kV = 6,8 kV. This is only a 3% over-voltage margin on a 6,6 kV grid voltage. In the context of the Dutch Grid code, this SST would not even be compliant as the MV grid voltage is allowed to be ±10% of the nominal voltage.
3) MV / LV isolation capability
   The most striking part of this paper is the way it considers the isolation of the DAB transformer. The paper recognizes the isolation stresses *only* in the form of the dv/dt stress caused by the switching devices. It then proceeds to make the case for an IFE because the capacitors which enable the mid-points of the DAB's MV side are "beneficial for IME". There is no mention of any standards whatsoever and does not give any isolation levels.
   An image published in [44] shows that the transformer would never be compliant based on the dimensions, in combination with the isolation material (Kapton tape).

It can be concluded that the S^{3}T design is not compliant to the IEC60076-3.

9.3.6 150kW SST Demonstration Site (2020)

In 2020, a prototype SST was demonstrated in [36]. This SST is significant in several ways. It is fully bi-directional, and it

focused on the future of DC applications by putting emphasis on an LV DC-bus that generates both +750V, as well as -750V simultaneously. The SST was demonstrated on a separate test-site, housed in its own building. Electrically, the SST was isolated from the grid behind a 200kW conventional transformer. As with the previously discussed SST prototypes, key aspects are listed below.

1) IBE configuration
   The prototype is an IBE configuration with a cascading H-bridge on the MV side. It is followed by a DAB that has a non-conventional topology. A DAB commonly has two full H-bridges at its primary and secondary sides of its (single phase) transformer, this SST uses a different topology. On the MV side of the DAB, it does retain 4 switches, yet these are placed in series-pairs, with a clamped diode mid-point. This is done to accommodate the higher voltage level of the MV DC bus, while still being able to use switching devices of a lower break down voltage. The MV DC-bus operates at a nominal voltage of 2000V, while the break down voltage of the DAB's MV side switching devices is 1700V. By creating a mid-point using capacitors and diodes, a 3-level converter is achieved. This way the switching devices only "see" 1000V. The secondary side of the DAB actually has two outputs, a +750V, and a -750V. These are achieved using two H-bridges on the secondary side, which are each connected to a secondary winding. This means the transformer is a single-phase input (on the MV side) and a two phase-output (on the LV side). Its construction is therefore more complex than that of a common DAB transformer with just two windings.
2) Power supply structure
   Another novel aspect of this transformer is its power supply structure. The MV electronics all derive their power from the MV DC-bus, and all the low voltage switching device drivers acquire their power from the LV DC-bus. This is difficult to achieve as during startup of the SST, these DC-busses are not charged, and their voltage control is

unbalanced. To get around this, the researchers designed a separate 13,2 kV to 220 V transformer to create the low voltage power supplies of the control electronics. Doing so allows them to have a controlled start-up, with most of the electronics being powered locally. See paragraph 15.3 on future research, as this is an important aspect that needs to be solved if an SST is to become a technological and commercial success.

3) MV input voltage capability

The researchers state in table 1 of the paper that the input voltage specification is 13,2 kV. As a first, they also describe the peak input voltage handling specification, which is stated at 18.664 V (which is exactly √2 higher). This means this SST would immediately be non-compliant to IEC60076-3's IVW & IVPD tests. In the test results chapter, however, it becomes apparent that the MV DC-busses of all ten modules in series operated at 2200 V, and that the total rectified voltage reached 22 kV. The researchers used switching devices for the CHB with a breakdown voltage of 3300V. With 10 modules in series, the SST is theoretically capable of handling peak input voltages of 33 kV, meaning that it is compliant with the IVW & IVPD test voltages. This is of course *not* accounting for the higher voltage class that this SST would fall into, as it is technically being deployed in a 17,5 kV class system voltage. Deploying the SST as is into the Dutch electricity grid, however, would mean it is compliant to IEC60076-3.

4) MV / LV isolation capability

The researchers have extensively investigated the isolation barriers necessary to create an SST. Within modules there are isolation barriers between the power stage(s) and the control electronics. Between the MV and LV side, an additional conventional transformer was used to generate the voltages to power the system controller. This partially solves the isolation problem of an SST. The other aspects

will involve the use of fiber optics for control signals, as well as the critical isolation of the DAB transformer. There is unfortunately no mention of either aspect. Since the demonstration site has been isolated by a separate 200kW transformer, the SSTs DAB transformer does not need IEC60076-3 AV test voltage levels of insulation. This greatly simplifies their design, but it does mean that without its external extra conventional transformer, it is not compliant.

In conclusion, this 150 kW prototype that was designed and built in Korea, is partially compliant to the IEC60076-3 if it was designed / implemented for the Dutch electricity grid. The non-compliant aspect, the insulation, is again demonstrated as being very challenging. With the isolation problem overcome, this last SST could be argued to fall into the next category, hybrid SSTs.

9.4 SST hybrids

Up until this point, most research focusses on replacing a conventional transformer in its entirety with power electronics. That is, however, not the only solution. Various hybrid solutions also exist where the conventional transformer is kept but augmented with power electronics to enhance its performance. It should be noted here that there is a distinction between transformers with on-load tap changers (OLTC) and hybrid SSTs (though the difference is very small depending on the topology. Hybrid SSTs generally handle the full voltage range on the LV side (and are very much an addition to a transformers), whereas an OLCT will "only" be connected to the different transformer winding taps. Note that this *is* a simplification, as there are several hybrid SST topologies. There are three main advantages of a hybrid SST with respect to "full" SSTs.

1) The first aspect is cost. With SiC being a relatively expensive technology during the time of writing (2022), the hybrid solutions are much more favorable than a full-fledged

SST from a business perspective. It can be deduced that a hybrid solution is the only viable technology from a business perspective at this time. In this next section, two of hybrid SSTs will be discussed. When compared to an SST, the hybrid distribution transformer offers a significant cost reduction due to the absence of MV side electronics & switching devices.

2) The second aspect is reliability. SSTs have a very high number of components compared to a conventional transformer. This makes the reliability of a conventional transformer far superior. By having a hybrid, that reliability (from a customer-minutes-lost perspective) is retained, with the power electronics being bypassed / disabled in case of a failure. This allows the conventional transformer part of the hybrid to remain in operation while a service engineer is dispatched to fix / replace the power electronics part. This is *not* possible with a full SST.
3) The third and last aspect is the power density. Hybrid SSTs can be built in several forms, but generally the volume that the power electronics take up will be smaller than the volume of a full SST

It should be noted though that hybrid SSTs would still have to comply with the IEC60076-3 standard. Its AV test, however, is no longer an issue because the conventional transformer part of the hybrid takes care of the isolation. With respect to the IVW & IVPD tests, the power electronics part only has to comply with the test levels of a "<1,1 kV system voltage" class (because U_m is 400V). This means the electronics need to withstand test voltages of up to 2x 1,1 $kV_{AC\ RMS}$ (2,2 kV * √2 ≈ 3,1 kV_{PEAK}).

9.4.1 Hybrid distribution transformer 2012

The first hybrid distribution transformer prototype was conceived in the USA in collaboration with ABB [46]. The paper outlines the various ways that electricity grid stresses can be dealt with, with an emphasis on cost effectiveness. It concludes that devices like SVCs, STATCOMs, and passive- and active filters are all *extra*

additions and that an integrated solution might be more cost effective.

The paper evaluates four configurations of hybrid SSTs. The researchers settle on the more integrated hybrid that has power electronics directly interfacing with a separate winding because it has the highest flexibility in control aspects. Since the topology differs so significantly from the generalized topologies of Figure 9-5, the schematic of the designed setup is shown below in Figure 9-7.

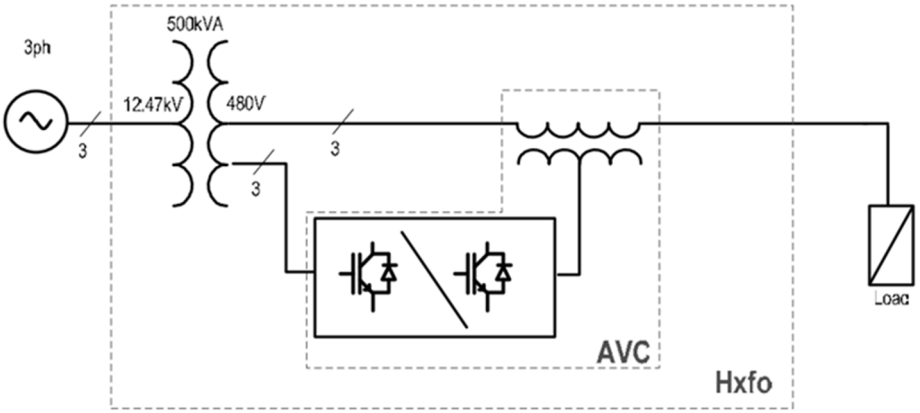


Figure 9-7 Hybrid distribution transformer [46]

By implementing the power electronics on a winding (section) of the conventional transformer, the hybrid SST is capable of PFC, harmonic filtering, flicker control, AC regulation, and phase shifting.

The integration of the power electronics with the LV winding is a concept that, like with SSTs, is not covered by the IEC60076-3. Interpreting the standard would suggest that the MV winding of the transformer would be subjected to the IVW & IVPD test conditions for certification. For the LV side, those tests would also have to be executed for an U_m of 480V. The IEC60076-3 classifies such a voltage as a "system voltage" of U_m<1,1 kV. According to paragraph 7.3.1.3 of the standard, the worst-case testing applied is 2x U_r / √3. With the secondary side of the hybrid SST connected in star

for Dutch electricity grids, this would mean a peak test voltage of 2x 1,1 kV * √2 = 3,1 kV. It needs to be noted that this test voltage *also* applies to the secondary sides of regular SSTs. This is however of secondary importance due to the voltage levels of the MV side taking the bulk of the design effort.

With regards to the AV test voltage, this is not an issue as the conventional transformer will likely be designed using mature conventional transformer technologies, therefore resulting in a relatively easy IEC60076-3 compliance.

9.4.2 400 kVA HT 2015

This second hybrid did not see completion beyond the design stage with no prototype being built [47]. Nevertheless, this hybrid is relevant because of its significant 400 kVA power level.

The arguments the researchers make for designing a hybrid SST over a "full" SST is mostly based on the work of Kolar & Huber in [48]. These arguments are mainly the cost aspect and the efficiency of SSTs being worse than LFTs. The researchers identify as many as eight different hybrid SST topologies (the work described in the previous paragraph only identified four).

Interestingly, this work concludes the exact same topology of the hybrid SST is the most optimal, but via a completely different approach. Whereas [46] concludes that the control flexibility is the best for their chosen topology, [47] reaches the same topology by stating it is optimized for efficiency / power density. Please note that it is *stated*, and not determined analytically. The researchers implicitly choose for the highest degree of flexibility as well and discard four of the eight topologies outright. The remaining four topologies are again halved by focusing on only two topologies which differ only in the aspect of an additional injection transformer. The researchers conclude that the auxiliary winding and the power electronics must be rated to a certain voltage level anyway, therefore the injection transformer is deemed unfavorable. Resulting in the selection of topology C3 from figure

1 of their paper, which, coincidentally is identical to the topology of the previous chapter. Upon further inspection, however, the prototype is designed slightly differently. See Figure 9-8 below.

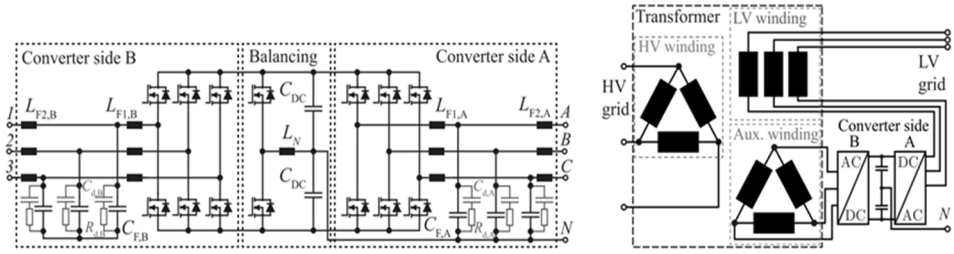


Figure 9-8 Three-phase hybrid transformer [47]

The main difference in the chosen topology is to have the LV side electronics featuring a neutral point. The design allows for a very mature topology, a six-pulse rectifier & inverter, to be used. This simplifies the design process. Two additional switches were necessary to balance the neutral point with respect to the three-phase output of the converter.

As stated in paragraph 9.4, one of the main advantages is that a failure of the power electronics would not result in a failure of the entire hybrid SST. This advantage has been negated because a failed switching device on the LV grid side of this hybrid would result in the hybrid SST no longer being operational (assuming that switching device fails in an "open" state).

With respect to the IEC60076-3 compliancy, two conclusions can be drawn. The first is that the AV test of the IEC60076-3 can be easily complied with as long as the conventional transformer part is implemented using mature conventional technology. With regards to the IVW & IVPD tests, the power electronics would again be subjected to 3,1 kV_{PEAK} because U_m would fall into the 1,1 kV system voltage category (2x 1,1 kV * √2 = 3,1 kV). The IVW & IVPD test can, however, be executed at higher frequencies. This would result in the LV windings taking an increased part of the test voltage

with respect to the electronics. This means that the switching devices do not need to be designed with breakdown voltages that can handle the full 3,1 kV_{PEAK}.

It would be very interesting to see a future version of the standard accommodating SSTs and hybrid SSTs, as it will require careful rethinking of the tests.

9.5 The state of the art

From the literature that was found at the time of writing (2022), three main gaps in the state-of-the-art are identified. Each of these will be discussed in the next paragraphs.

9.5.1 SSTs designed to meet IEC60076-3

All previously mentioned SST prototypes have been designed, to various degrees, for being capable of being placed in the electricity grid. However, none have been designed to comply with two key requirements of an industry standard for testing conventional transformers. An overview of the prototypes and their compliancy have been listed in Table 3 below.

Name	**Year**	**§**	**Max. MV input**	**Isolation level**	**IEC60076-3 Compliancy**
UNIFLEX	2009	9.3.1	Scalable	Unknown	Unlikely
SiC-Enabled SSPS	2011	9.3.2	13,8 kV	Unknown	No
MEGACUBE	2013	9.3.3	20 kV	Unknown	No
Electronic Power Trafo	2016	9.3.4	34,29 kV	Unknown	Unlikely
S^3T	2016	9.3.5	6,6 kV	Insufficient	No
150kW SST demo site	2020	9.3.6	33 kV	Sufficient	No

Table 3 List of SST prototypes & IEC60076-3 compliancy

The first of the two aforementioned key requirements is the Short Duration AC withstand voltage, which requires that conventional transformer windings are tested at 24 kV AC for a duration of 60 seconds. The 28 kV is determined from table 2 of the standard based on an Um of 12 kV (since the SST will work at a nominal voltage of 10,5 kV plus a maximum of +10\%, Um must be chosen as 12 kV). Designing power electronics capable of dealing with 24 kV is an

incredible challenge, as will become apparent in the rest of this document. As can be observed from Table 3, only one SST prototype (the Electronic Power Transformer in Wuhan, China) can withstand the IEC60076-3 IVW & IVPD test conditions (Max. MV input). It can therefore be concluded that most research prototypes have been designed to only meet the input voltage requirements / conditions of a nominally operating MV grid (with no / little margin for over voltages).

The second of the two aforementioned key requirements is the Lightning Impact (LI) withstand voltage. This is a short pulse of 75 kV to simulate a lightning strike and a conventional 10 kV transformer must be able to withstand such an impact. Fortunately, the IEC60076-3 offers some flexibility regarding this requirement and allows (under certain circumstances) the use of surge arrestors. This greatly reduces the complexity of the design of the SST, since 28 kV is already more than sufficiently challenging. It can be observed from Table 3 that particularly in the isolation aspect, existing SST prototypes have not been designed with IEC60076-3 compliancy in mind. The only prototype that is compliant, does so by having a conventional transformer at the MV input to provide the necessary isolation.

At the time of writing (2022), it is foreseen that the design of an SST prototype, capable of handling 28 $kV_{AC\ RMS}$ under continuous operation, will contribute to the state-of-the-art.

By designing an SST prototype that meets the requirements of the *IEC60076-3 2013 - Insulation levels, dielectric tests and external clearances in air*, the prototype can then be considered an *actual* drop-in replacement for a conventional transformer.

9.5.2 SSTs placed in a live electricity grid

Thus far, quite a few SST prototypes have been built. However, at the time of writing, none of these have actually been placed inside an actual electricity grid. Aside from not being designed to comply

with the standards applicable for conventional transformers, the existing prototypes have only been operated in testing facilities and laboratories. Placing an SST prototype in the electricity grid can provide valuable real-world insight into the behavior of the interactions between the LV & MV grids and the converter.

At the time of writing (2022), it is foreseen that placing an SST prototype in the electricity grid and perform actual field measurements, will contribute to the state-of-the-art.

9.5.3 SSTs with large DC battery storage

The SST prototypes mentioned in the previous paragraphs all contain a DC bus in one form or another. From the DC bus an inverter is used to generate the necessary AC at the LV side. If properly dimensioned, this DC bus can be used to interface directly with PV solar cells or EVs without the need for intermediate power converters [32]. The universal power electronics-based distribution transformer, a unified approach. Perhaps the most interesting use of the DC bus will be the addition of battery storage. Adding battery storage can potentially improve power quality by aiding with peak shaving when there is insufficient power available during peak hours. Additionally, battery storage could ensure the operation of the LV grid when any or all phases on the MV side fail. This would greatly improve availability of the electricity grid and is of particular interest to the DSOs. It should be noted however, that current legal regulations prevent DSOs from generating any power and DSO controllable battery storage in the SST would violate these regulations.

At the time of writing (2022), it is foreseen that the design of an SST prototype, utilizing battery storage for improving PQ, will contribute to the state-of-the-art.

9.6 The contribution

This thesis contributes to the state of the art by focusing on the identified gap of paragraph 9.5.1, SST compliancy with IEC60076-3, and designing a prototype research platform to investigate that

compliancy. With research question two answered, the next focus of this work is the IEC60076-3 tests and their applicability to SSTs. The next chapter (10) will focus on the following two key research questions:

3. **Which standards do conventional transformers have to comply with?**

And:

4. **What are the implications of the IEC60076-3 standard when applied to SSTs?**

These questions will be answered in the next chapter which will focus on the standard and its tests.

10. The IEC60076-3

With the state-of-the-art established, there is a clear gap that has been identified in the form of SSTs and their compliancy to standards. This chapter will focus on the two following questions, as well as sub-questions that can be derived from them.

The first is research question nr. 3:

3. **Which standards do conventional transformers have to comply with?**

This research question will be answered in the first paragraph of this chapter (10.1). This paragraph will conclude that there are many that are applicable. As has already been established in the previous Literature study (chapter 9), there is a specific standard of particular interest for SSTs that has not yet been investigated in literature. This is the IEC60076-3 standard, which leads to the research question nr. 4:

4. **What are the implications of the IEC60076-3 standard when applied to SSTs?**

The answer to this research question is only informative and would be limited in scope. It is important to dig deeper and understand the importance of this standard. Hence, the following research sub-questions are derived:

a. What is the standard for?
b. Why is it relevant for SSTs?
c. What tests does the standard describe?
d. What are the tests designed to achieve?

This chapter will first elaborate on the testing that conventional transformers face, and the consequences for the electrical conditions an SST would face as well. This is followed by a description in paragraph 10.2.1 of the test standard that grid components (specifically transformers) need to comply with before

being placed in the grid and why these tests are necessary in the context of the Dutch electricity grid. In paragraph 10.2.2, three tests are elaborated on as the focus of this SST design and this thesis. Lastly, in paragraph 10.3, the additional (non-electrical) requirements of the IEC60076-3 are investigated. Finally, the chapter is concluded in paragraph 10.4.

10.1 The IEC60076 standard for power transformers

The IEC60076 family of standards govern the requirements for power transformers in electricity grids and consists of 26 parts. It should be noted that this number isn't exact because several of these exist of multiple parts (e.g., IEC60076-22 has six sub-parts) and parts 9, 17 and 25 have no release associated with them (part 9 for example apparently showed too much overlap with a competing IEC standard).

It should be noted that part 3 is likely not the only applicable part that is relevant for SSTs. Table 4 below shows all the parts that the IEC60076 is comprised of, as well as which parts the writer of this thesis considers applicable to SSTs. For the purposes of this thesis, however, only part 3 of the standard is evaluated in-depth. It's important to note that parts 5, 10 and 20 of the IEC60076 are likely very important research topics that should be addressed in future research to improve SST adoption in the grid.

IEC60076 part	Part name	Relevant for SST future research?
1	General	Yes
2	Temperature rise for liquid-immersed transformers	No
3	Insulation levels, dielectric tests and external clearances in air	Yes
4	Guide to the lightning impulse and switching impulse testing - Power transformers and reactors	Yes

5	Ability to withstand short circuit	Yes
6	Reactors	No
7	Loading guide for mineral-oil-immersed power transformers	No
8	Application guide	Yes
9	-	
10	Determination of sound levels	Yes
11	Dry-type transformers	Yes
12	Loading guide for dry-type power transformers	No
13	Self-protected liquid-filled transformers	No
14	Liquid-immersed power transformers using high-temperature insulation materials	No
15	Gas-filled power transformers	No
16	Transformers for wind turbine applications	Yes
17	-	
18	Measurement of frequency response	Yes
19	Rules for the determination of uncertainties in the measurement of the losses on power transformers and reactors	No
20	Energy efficiency	Yes
21	Standard requirements, terminology, and test code for step-voltage regulators	Yes
22	Power transformer and reactor fittings	Yes
23	DC magnetic bias suppression devices	Yes
24	Specification of voltage regulating distribution transformers (VRDT)	Yes
25	-	
26	Functional requirements of insulating liquids for use in power transformers	No
57	Liquid immersed phase-shifting transformers	No

Table 4 IEC60076 parts/subsections

It is safe to say that any new power transformer concept will have to comply with a large number of requirements, design guidelines and tests before being placed in the electricity grid. And this is only looking at a subset of the IEC standards, there are many more (IEC and others) standards and even laws that drive further SST requirements. It should be noted that it is possible for any newly introduced component to *not* be compliant to the IEC60076-3 standard, as this partly falls under the discretion of the DSO.

That said, a DSO is generally reluctant to approve such components, as additional testing and justification will be necessary to ensure safety (which is also covered by law). All of which will require significant additional time, and therefore, monetary investment. As such, the DSO is more likely to ask manufacturers of new grid components to simply comply with the applicable standards.

Over the years, there have been occasions where there have been deviations from the standards. In such a case, the DSO agreed with the component's manufacturer on the testing requirements. This is referred to as TOCR (Tested According to Customer Requirements). Such events however are rare due to the aforementioned time and monetary investments needed but are going to be interesting for DSO's and SST manufacturers alike due to the completely different nature of SSTs compared to conventional power transformers.

10.2 The IEC60076-3

As is maybe apparent from Table 4 IEC60076 parts/subsections, the focus of this thesis is the IEC60076-3: insulation levels, dielectric tests and external clearances in air. The main reason for focusing on this part of the IEC60076 is due to the nature of power electronics. Power electronics consists of semiconductor switches (IGBTs, MOSFETs, etc.) that are made up of silicon which has finite breakdown voltage. In fact, there are currently no commercially available semiconductor switches that can sustain the medium voltage level. The exception is one device from Wolfspeed in the U.S.A. that is in the laboratory prototype stage [49]. This SiC MOSFET has a breakdown voltage of up to 15 kV and is as of 2022 still the switching device with the highest voltage capability. Previous demonstrators [37][39][42][43][45][24][46][47] would have sufficed with a single converter stage on the MV-side, made up of these experimental Wolfspeed 15 kV SiC MOSFETs. Such demonstrators, however, would not have been electricity grid-compliant with regards to the IEC60076-3. As will become apparent in paragraph 11.1.

10.2.1 The need for standardization

The Dutch distribution grid of today operates at 10 kV, also referred to as "Medium Voltage / MV" (there are many other voltage levels that are categorized under MV, but the bulk is at 10 kV). This voltage is however not explicit enough as a requirement for designing an SST as it is in fact, an AC, 10 kV RMS value. Meaning that the aforementioned breakdown voltages of switches would have to handle the associated peak voltage of 14,142 kV (equation10-1). Note that this is under the assumption that there is no harmonic distortion.

$$V_{Switch\ breakdown} = V_{peak} = 10kV * \sqrt{2} = 14{,}142kV$$

10-1

This, however, is still unlikely to be a sufficient voltage level. This is because Dutch distribution grid operators may operate at different voltage levels. Throughout the project, consortium partner DSO Alliander for example, mentioned operating parts of its MV network at 10,5 kV. On top of that, there is a margin of ±10% that is allowed by the Dutch grid code. In that case, the power electronics switching devices would need to handle 16,334 kV (see equation 10-2).

$$V_{Switch\ breakdown} = V_{peak} = (10{,}5kV + 10\%) * \sqrt{2} = 16{,}334kV$$

10-2

The IEC has developed the 60076 standard specifically for power transformers to set a common set of rules/requirements for the devices to operate in. Part three of the standard (60076-3) deals with these voltages, as well as the galvanic isolation between the primary- and secondary sides of power transformers.

10.2.2 The tests covered by the IEC60076-3

The IEC60076-3 covers several aspects of conventional power transformers, and it does so in the form of 10 different tests. These are listed in Table 5 below.

Test names as stated in: IEC60076-3 2013 - Insulation levels, dielectric tests and external clearances in air	Abbrev.	In-scope for this thesis
Full wave lightning impulse test for the line terminals	LI	
Chopped wave lightning impulse test for the line terminals	LIC	
Lightning impulse test for the neutral terminal	LIN	
Switching impulse test for the line terminal	SI	
Line terminal AC withstand voltage test	LTAC	
Auxiliary wiring insulation test	AuxW	
Lightning impulses applied to two or more terminals simultaneously	LIMT	
Applied voltage test	AV	Yes
Induced voltage withstand test	IVW	Yes
Induced voltage test with PD measurement	IVPD	Yes

Table 5 IEC60076-3 tests

The main purpose of these tests is to ensure that any newly designed power transformers can handle the grid conditions they will encounter throughout their service life. Each of these tests will be described here briefly, with the ones that are in-scope for this work in higher detail.

10.2.2.1 LI - Full wave lightning impulse test for the line terminals

The LI test is to verify that a conventional power transformer can withstand fast rise time transients. These fast transients simulate the effect of lightning strikes that hit power lines to which a power transformer is connected. Such fast transients may therefore also be experienced by power transformers throughout their service life. This test is performed by applying an impulse to the transformers line terminals. The high frequency components of the test produce non-uniform stresses in the winding (compared to some of the other tests).

This test has been left out-of-scope for the simple reason that lightning strikes, as well as this test, involves voltages that are simply impractical to dimension an SST design to with the given time and budget of the project. For a system voltage of 10 kV, a

peak voltage of 75 kV (minimum) is applied for a duration of 1~3us. Such a test voltage presents less breakdown problems for conventional transformers due to the maturity of their design, as well as some of the fundamental design aspects. For example, copper windings themselves do not really experience any breakdown, and the insulation material (oil) is to a degree even self-repairing in case of a breakdown. Silicon switching devices experience neither of these "luxuries" and will break down, even in such a small time period. For power transformers (and by extension SSTs) that are *not* capable of withstanding these test voltages, alternative protection measures are commonly implemented (such as MOVs & TVS') to protect against lightning strikes. With all these considerations in mind, this test is chosen to be out-of-scope for this project.

10.2.2.2 LIC - Chopped wave lightning impulse test for the line terminals

The LIC test is also to verify that a conventional power transformer can withstand fast rise time transients. The main difference is in the trailing end of the pulse. Compared to the LI test, the LIC test chops the trailing end of the pulse, resulting in even higher voltage transient rates. On top of this, the test voltage for a 10 kV power transformer is even higher at 83 kV (minimum).

With the same considerations of LI test in mind, this test is chosen to be out-of-scope for this research.

10.2.2.3 LIN - Lightning impulse test for the neutral terminal

The LIN test is also to verify that a conventional power transformer can withstand lightning strikes on its neutral terminal. It is similar to the LI and LIC tests. Its biggest difference is that this test also verifies the impact on earthing connections. Once more, with the same considerations of LI test in mind, this test is chosen to be out-of-scope for this research.

10.2.2.4 SI - Switching impulse test for the line terminal

The SI test is to verify that a conventional power transformer can withstand slower voltage rise times as well. This test exposes the power transformer to voltage transients typically associated with any switching operations that it sees in its service life.

The standard states that this test targeted to transformers that operate at 100 kV or more. Thus, this test can be considered out-of-scope for a distribution grid transformer.

10.2.2.5 LTAC - Line Terminal AC withstand voltage test

The LTAC test is intended to verify that the insulation of a conventional power transformer can withstand the alternating voltage. This test checks the withstand strength of each line terminal to earth. This test is very similar to the AV test (which is in-scope for this thesis), in that it tests, in power electronics terms, the galvanic isolation between the primary side and earth. The main difference between this test and the AV test is that this test is intended for transformers with non-uniform winding insulation (the AV test is for uniform winding insulation).

10.2.2.6 AuxW - Auxiliary wiring insulation test

The AuxW test is to verify that the insulation of any auxiliary wiring of a conventional power transformer is sufficient for its operational service life. Since SSTs do not have auxiliary windings, this test could be considered not applicable, simply because the technology does not have any "windings". However, SSTs may be designed such that auxiliary equipment is connected (for example directly on the DC-bus). These parts of the SST architecture (e.g. the DC-bus) could be considered auxiliary windings. The chosen architecture for this project, however, does not have any auxiliary connections for connecting additional auxiliary equipment. It is for this reason that the AuxW test is interesting for future research, and also considered out-of-scope for this project.

10.2.2.7 LIMT - Lightning impulse test for the neutral terminal

The LIMT test is also to verify that any special types of conventional power transformer (like phase shifting transformers with an on-load bypass) can withstand the internal voltage rises that may occur due to lightning strikes on two or more of its terminals simultaneously. This test is also referred to as a "double-ended lightning impulse test". Once more, with the same considerations of LI test in mind, this test is chosen to be out-of-scope for this research.

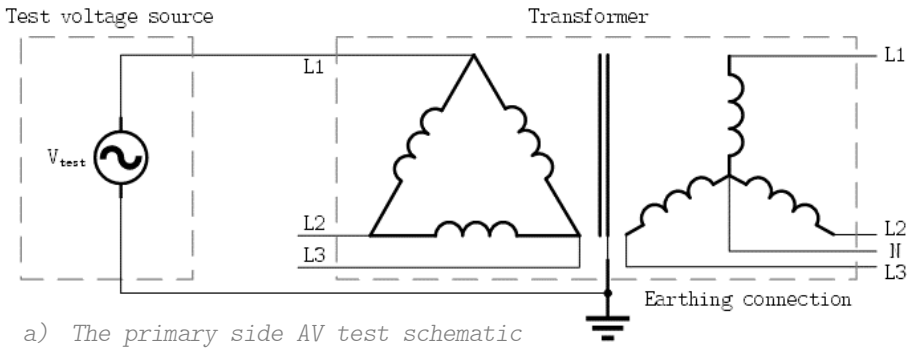
10.2.2.8 AV - Applied voltage test (in-scope of this thesis)

The AV test is also to verify that a conventional power transformer can withstand alternating voltage. Fundamentally, the test is designed to verify the isolation between the primary and secondary windings to transformer's core, which is earthed.

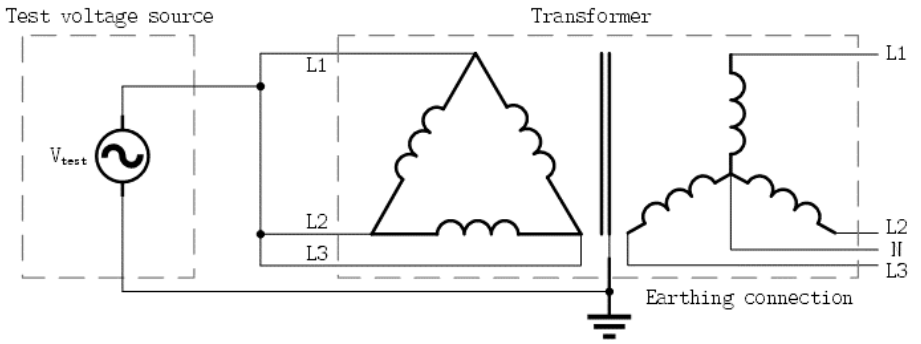
From a power electronics perspective, this test checks the galvanic isolation between the primary and secondary sides of a transformer (and by extension, an SST).

This is important because this test implies a need to *electrically* isolate the MV grid from the LV grid. Any failure to do so connects the local distribution grid of (for example) a city, to a single earthed connection at that transformer.

The IEC60076-3 standard describes the AV test procedure as follows: "*The test is intended to verify the alternating voltage withstand strength of the line and neutral terminals and their connected windings to earth and other windings. The voltage is applied to all the terminals of a winding, including the neutral, simultaneously so there is no turn-to-turn voltage.*". Since the standard is written for conventional power transformers (and the scope of this research is considered the Dutch electricity grid), a schematic view can be derived (see Figure 10-1).



a) The primary side AV test schematic



b) Primary side windings are allowed to be connected together

Figure 10-1 IEC60076-3 Applied voltage test schematic for a conventional PT.

Note 1: The Dutch MV distribution grid is configured in delta, and the LV grid is configured in star / wye.

Note 2: The IEC60076-3 standard defines "system voltage" levels based on the voltage that the PT nominally operates on. This differs for the primary winding compared to the secondary winding.

There are several important things to note here. First thing is the similarity to the LTAC test, with the only difference is the assumed uniformity of the insulation for the AV test (the LTAC tests each winding individually to check non-uniform windings). The second is the typical configuration of the Dutch MV and LV electricity grids. In the Netherlands, the MV distribution grids are typically operated in a delta configuration and in most cases is not earthed. This is, as implied, not universally the case and there are locations that have an earthed / grounded MV. The LV

grids in the Netherlands are universally earthed / grounded at the transformer.

The reason why this is important is because of the impact of the value of V_{test} on the power electronics architecture, as will become apparent in chapter *11.1 IEC60076-3 power electronics architecture impact*. For the primary side, a 10 kV transformer falls into the category of a 12 kV (RMS) "system voltage" (denoted in the standard as U_m). Such a slightly higher number is no issue for conventional transformers, yet for SSTs it will be shown that this has a significant impact.

V_{test} for the primary side is 28 kV (RMS), as found in *table 2 - Test voltage levels* of the IEC60076-3. As mentioned before in this chapter, the peak voltage has the most impact on the power electronics (in this case, the galvanic isolation). As can be seen below in equation 10-3.

$$V_{test\ peak\ primary} = 28kV * \sqrt{2} = 39{,}597kV$$

10-3

This means the galvanic isolation of the SSTs primary side power electronics must withstand almost 40 kV for a duration of 60 seconds.

V_{test} for the secondary side is 28 kV (RMS), as found in *table 2 - Test voltage levels* of the IEC60076-3. As mentioned before in this chapter, the peak voltage has the most impact on the power electronics (in this case, the galvanic isolation). As can be seen below in equation 10-4.

$$V_{test\ peak\ secondary} = 3kV * \sqrt{2} = 4{,}242kV$$

10-4

This means the galvanic isolation of the SSTs secondary side power electronics must withstand a peak voltage of only 4,3 kV (again, for a duration of 60 seconds).

This shows that the impact on designing an SST lies mostly on the primary side as the secondary side could do with 5 kV isolation for most material/component choices (which is a common industry standard voltage level). While the same of course holds for conventional transformers, it has a much greater impact on SSTs. The reasons as to why this has a much greater impact, please see chapter 11.1 IEC60076-3 power electronics architecture impact.

10.2.2.9 IVW - Induced voltage withstand test (in-scope of this thesis)

The IVW test is also to verify that a conventional power transformer can withstand alternating voltage on each line terminal and its connected windings to earth (and other windings).

From a power electronics perspective, this test checks the capability of a transformer (and by extension, an SST) to handle a voltage on its in- and outputs.

This is important because the test voltages applied to the in- and outputs are significantly higher than the nominal voltages. Effectively it checks if the transformer can handle fault conditions in the grid that cause high input voltages.

The IEC60076-3 standard describes the IVW test procedure as follows: "*The test is intended to verify the alternating voltage withstand strength of each line terminal and its connected winding(s) to earth and other windings, along the winding(s) under test and the withstand strength between phases. The test is performed with the transformer connected as for service. During the test, symmetrical voltages appear at all the line terminals and between turns, with no voltage at the neutral. The test is performed with a three-phase voltage on three phase transformers.*". Since the standard is written for conventional power transformers, a schematic can be derived (see Figure 10-2). Important to note in this figure, is that the MV side of the Dutch distribution grid is in delta, and the secondary / LV side is in star / wye.

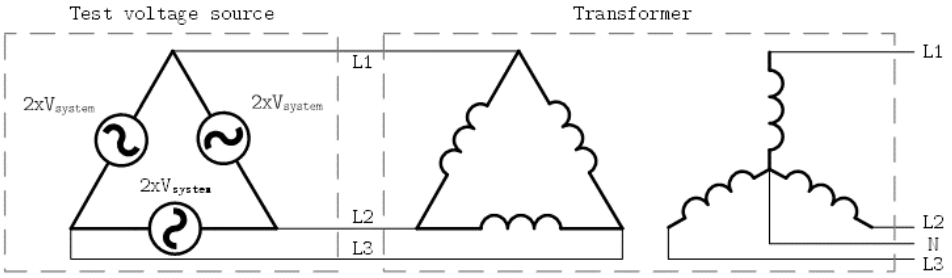


Figure 10-2 Induced Voltage Withstand test for a conventional transformer

As is shown in the derived schematic above, the test is performed with all three windings connected *simultaneously* to the test voltage source. This is important because for an SST, a √3 voltage reduction may be obtained through a floating neutral point configuration of the MV-side electronics. The impact of this is elaborated upon in chapter IEC60076-3 power electronics architecture impact.

The second key takeaway from this test is that the test voltage is a factor two higher than the system voltage, meaning 2*12 kV (RMS). As can be seen from equation 10-5, this amounts to a peak voltage of 34 kV for a duration of 60 seconds.

$$V_{test\ peak} = V_{system} * 2 * \sqrt{2} = 12kV * 2 * \sqrt{2} = \ 33{,}941kV$$

10-5

This means that a 10 kV transformer (and future SSTs) are subjected to an input test voltage of 34 kV for a duration of 60 seconds.

While conventional transformers with paper and oil insulation can relatively easily handle twice the nominal voltages, it is crucial to note that present-day power electronics do not have that capability. As will become apparent in the next chapters, this poses a significant overrating impact on SST designs (which consequently results in a design time and monetary impact). In fact, this test has the highest impact of all tests in the IEC60076-3.

10.2.2.10 IVPD - Induced voltage test with PD measurement (in-scope of this thesis)

The IVPD test is intended to verify that there are no harmful partial discharges in the winding insulation during the operation service life of a conventional power transformer, even if there are over voltages in the grid. The IVPD test is nearly identical to the IVW test with regards to the applied test voltages and test procedures. The main difference is the focus on the measurement of partial discharges in the insulation and no voltage on the neutral.

Partial discharges are a concern because these are caused by small defects in insulation material and each partial discharge degrades the insulation material over time. A partial discharge will usually occur in a single location (as that location likely saw the highest electric field), consecutively worsening local insulation. As will become apparent in chapter 11.1 IEC60076-3 power electronics architecture impact, partial discharges limit the possible insulation materials SSTs can use.

A crucial thing to note is that a conventional power transformer suffers less because its insulation is typically liquid (oil). Meaning that any "defects" in the oil itself tend to be self-repairing. Oil is typically not used in power electronics applications (including SSTs). Conventional transformers do not *only* use oil for insulation, but it is also used in combination with paper. It is this paper part that is not self-repairing, and it suffers degradation over time This happens at a very slow rate though, and conventional transformers are commonly used for several decades without any issues. There are also conventional power transformers that have resin-cast insulation. These are likely to be prone to this degradation mechanism.

10.3 Additional requirements

The IEC60076-3 standard does not only contain testing requirements, it also specifies a direct design constraint for the design of

conventional power transformers. This relates to the second part of the standards' title:

"Insulation levels, dielectric tests and *external clearances in air*"

The standard defines these external clearances as follows: "*Clearance in air is understood as the shortest distance between any metallic part of the bushing terminal and any part of the transformer, taking a line which does not pass through the bushing insulator.*". For a 10 kV conventional power transformer, a system voltage of 12 kV is applicable. In table 4 - minimum clearances in air, a 12 kV system voltage requires 120 mm between line to earth and 120 mm between phase to phase. This too, has a significant impact on the design of an SST (though not as dramatically as the IVW & IVPD tests). It specifically impacts the physical distance any power electronics can be from earthed parts, which impacts the volume of an SST. This is due to the need to enclose any power electronics to prevent access, as well as the physical separation that is needed between the MV side power electronics and the LV side electronics.

10.4 Concluding remarks

The IEC60076-3 is a relevant standard for SSTs as it describes tests which emulate grid conditions that may occur. Out of the 10 tests the standard describes, three have been identified as having the most impact on SST designs and are therefore more closely investigated in this thesis. The Applied Voltage (AV) test, the Induced Voltage Withstand (IVW) test, and the Induced Voltage withstand test with Partial Discharge measurement (IVPD).

From a power electronics perspective, the AV test checks the galvanic isolation between the primary and secondary sides of a transformer (and by extension, an SST). This AV test will subject the galvanic isolation of an SST's primary side power electronics to almost 40 kV_{PEAK} for a duration of 60 seconds.

The IVW and IVPD tests, again from a power electronics perspective, check the capability of a 10 kV/400V SST's capability of handling a test voltage of 34 kV_{PEAK} for a duration of 60 seconds on its input / primary side.

These three tests impose a significant design time and monetary impact on SSTs, as will become apparent in chapter 11.1 IEC60076-3 power electronics architecture impact.

Lastly, the standard requires 120 mm separation of any current carrying element (power electronics in the case of SSTs) to earth, mostly impacting the SST's volume and galvanic isolation components.

With research questions 3 and 4 answered, the applicability of the IEC60076-3 for SSTs is established. This then leads immediately to the next research questions.

5) **How does the standard impact SST design?**
6) **How is an SST designed to be compliant with the standard?**

These will be investigated in the next chapter, Prototype architecture.

11. Prototype architecture

In the previous chapter, the need for compliancy to IEC60076-3 being relevant for SSTs has been established. For the purposes of robustness in the face of possible grid conditions which would subject SSTs to significant stresses, these conditions tested for. From these test conditions and this compliancy, several research questions can be posited. These research questions will be investigated in this chapter. The first research question that comes to mind is:

5) How does the standard impact SST design?

This research question leads to the first part of determining what an SST should look like from a high level perspective, what process steps that need to be followed and what risks are involved when starting such a high-level design. This is discussed in chapter 11.1. In subsequent paragraphs, a more in-depth look will be necessary. This is covered by the following research question:

6) How can an SST be designed to be compliant with the standard?

In paragraphs 11.2 through 11.5, the impact of designing an SST that is compliant with the AV, IVW, and IVPD test conditions is investigated. It will be shown that this will involve a wide range of engineering aspects such as the electronics, mechanics, network infrastructure, isolation strategies, electric field shaping, and more.

The architecture of the SST was established via the risk-based approach. The main driver for the creation of this process was risk-mitigation. And it is a cyclical process in which the design aspect which presented the largest risk to the success of the SST project, was identified first. This would then be followed by a mitigation or solution being created to that risk. After which the next biggest risk would be identified, and solved, and so forth.

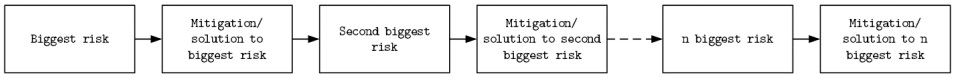


Figure 11-1 Risk based approach

The first risk identified was the lack of knowledge. This is common for every PhD project, but especially for the development of new technologies. The mitigation/solution for a lack of knowledge is the literature study and an investigation into existing technology/knowledge.

As risk by risk was identified and mitigated, the final design flow for the SST ended up being as depicted in Figure 11-2.

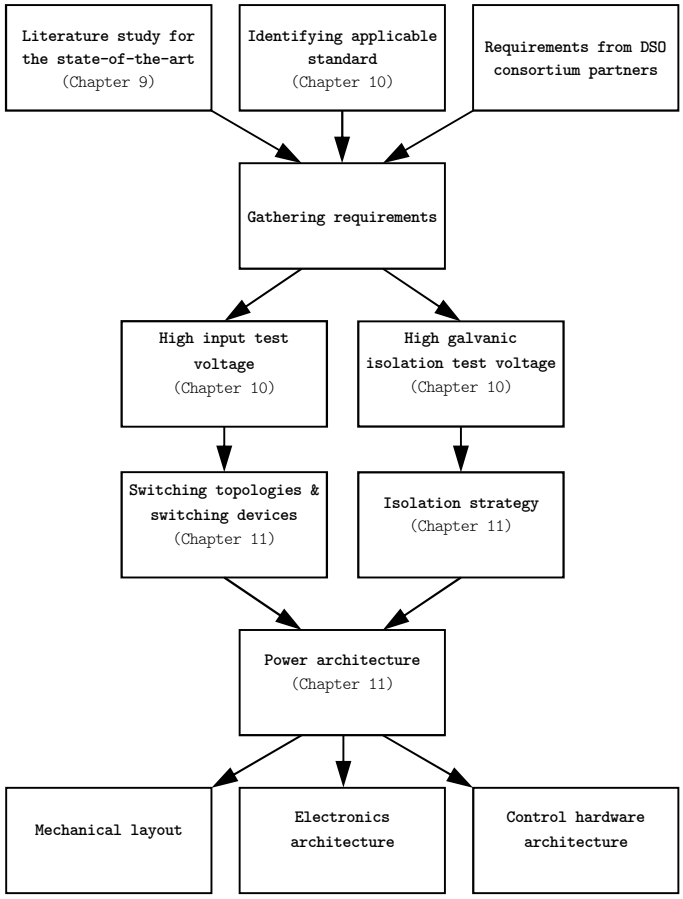


Figure 11-2 Design flow of the SST when looking back in time.

This approach differs from the designed prototypes listed in paragraph 9.3. **With the main difference (and the contribution of this thesis), the identification & application of the IEC60076-3 standard, with regards to the development of the SST prototype.**

As has been argued in the previous chapter, the IEC60076-3 is highly impactful on the design of the SST prototype. Initially, the focus of this chapter will be the impact of the IVW & IVPD tests. This will then be followed up with the impact of the AV test.

11.1 IEC60076-3 power electronics architecture impact

From all the risks that the SST faces, the voltage level at the MV-side presents the highest probability of causing failures. This is since the goal is to replace the conventional power transformer with power electronics, and the *switching devices* of power electronics have hard voltage limits that cannot be exceeded. For example a MOSFET with a rated voltage of 1000 V, is recommended to be operated at a maximum of 60% (and operation at its rated voltage would likely result in an average failure time of 70 hours) [50]. With Medium Voltage (MV) being 10.5 kV in the Netherlands, **the risk of a voltage break down is by far higher than any other engineering risk associated with the SST**.

The search for switching devices focused on availability, since the duration of the project would be very limited. Arguably, the most interesting candidate was a 10 kV / 10 A prototype SiC MOSFET from Wolfspeed (see Figure 11-3 below).

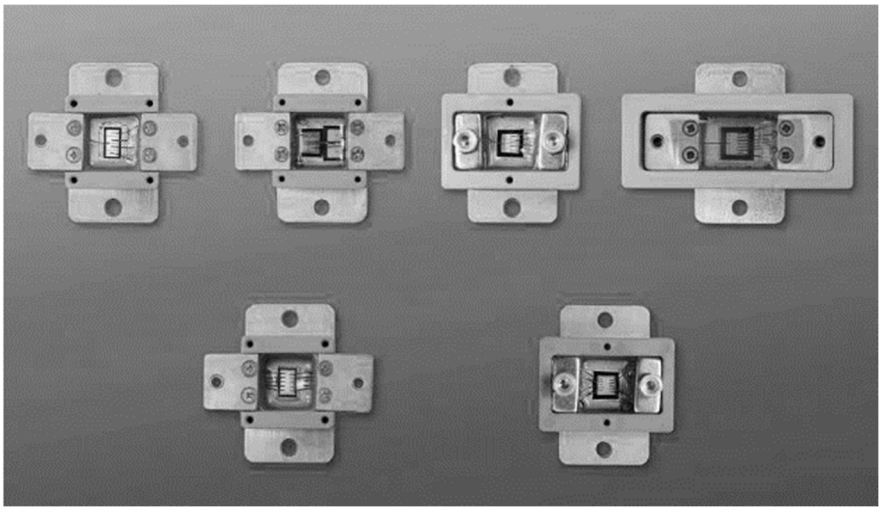


Figure 11-3 Wolfspeed 15 kV SiC MOSFET

This prototype has been the source of several publications since it is still very much in the prototype stage [51]. This switching device can withstand more voltage than any other commercially available IGBT & MOSFET. There were several considerations that lead to not using this switching device for the prototype. The only pro it has, is its high breakdown voltage. There were two main downsides, however. First, switching such devices would result in a very high dv / dt, which would possibly result in issues with EMI. Second, as has been illustrated with the need to comply with the IVW & IVPD tests, the breakdown voltage of these switching devices would *still* be insufficient to convert the MV with a single H-bridge. Effectively, even with the 15 kV Wolfspeed prototype MOSFETs, H-bridges would still have to be cascaded to withstand the IVW & IVPD voltage test levels.

11.2 SST architectures

An SST has several types of architectures. The power architecture is often investigated in literature. A source with a comprehensive overview of the existing power architectures is [52]. In this thesis both the excluded and selected architectures will be discussed. In addition to the power architecture, however, there

is also a real-time network architecture that needs careful consideration, as well as a thermal architecture.

11.2.1 SST power electronics architecture selection

When referring to the power electronics architecture of an SST, this thesis considers the power electronics only. So, the switching devices, bulk- & filtering capacitors, additional inductors, and transformers.

The first step in the selection of a power electronics architecture was a high-level quantitative analysis. Before settling on the Cascaded H-Bridge (CHB) with Dual Active Bridge (DAB) modular topology, several power electronics architectures were considered and excluded for further research.

This next section will illustrate and explain the excluded power electronics architectures, followed by the selected architecture. Additionally, the rationale will be given for excluding these topologies. The first of the excluded power architectures are listed in Figure 11-4 (note that neutrals & earthing connections are not shown). The common theme for discarding these topologies is mainly due to the MV-side. As was established in paragraph 11.1, there is no single switching device available that can withstand the total voltage presented by the MV grid and IEC60076-3. As a result, no single power conversion stage can face the MV grid. With multiple MV grid facing conversion modules in series (to divide the voltage), the only question that remains will be: How many?

Note that this question has already been answered by Huber et al, using a pareto analysis in [53]. The conclusion of their analysis is that an optimum is reached at 1200V~1700V per module. Their pareto analysis, however, only considers 10 kV_{RMS} as the operating voltage of the SST and simplifies (or even omits) practical implementation challenges, such as drivers, heat sinks, fiber optics communications, cabinet enclosures and production complexity. This source will be further discussed in paragraph 11.3.3.

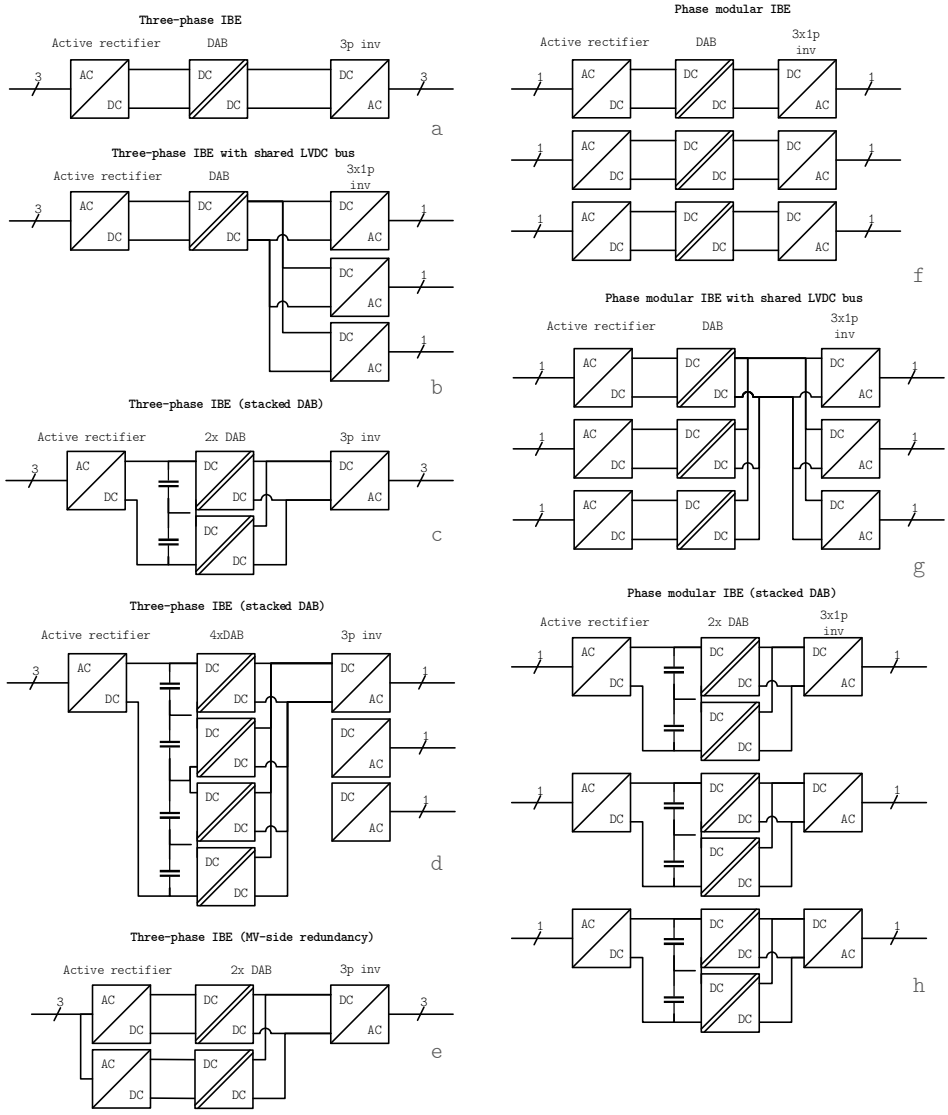


Figure 11-4 SST power architectures discarded for further research

In Figure 11-4a-e, various power architectures are shown with one common theme, and that is each architecture only has a single converter that faces the MV grid. Note, that the neutral, earthing and configuration (delta or wye) are not shown for simplification. Topologies a-e inherently unsuitable for this research. This is because firstly, there are no single switching devices that can

withstand the stated 24 kV_{RMS} of the IEC60076-3 IVW & IVPD tests. Secondly simply placing switches in series would not work because these would be unlikely to all switch simultaneously (resulting in higher voltages across the switch that would switch last). Architectures f, g, & h, suffer from a similar problem, although it is important to recognize their main difference compared through a-e. By having an individual converter per phase, they can be configured to have a floating neutral point, effectively allowing a √3 voltage reduction when the IVW & IVPD tests are executed. This is depicted in Figure 11-5 below.

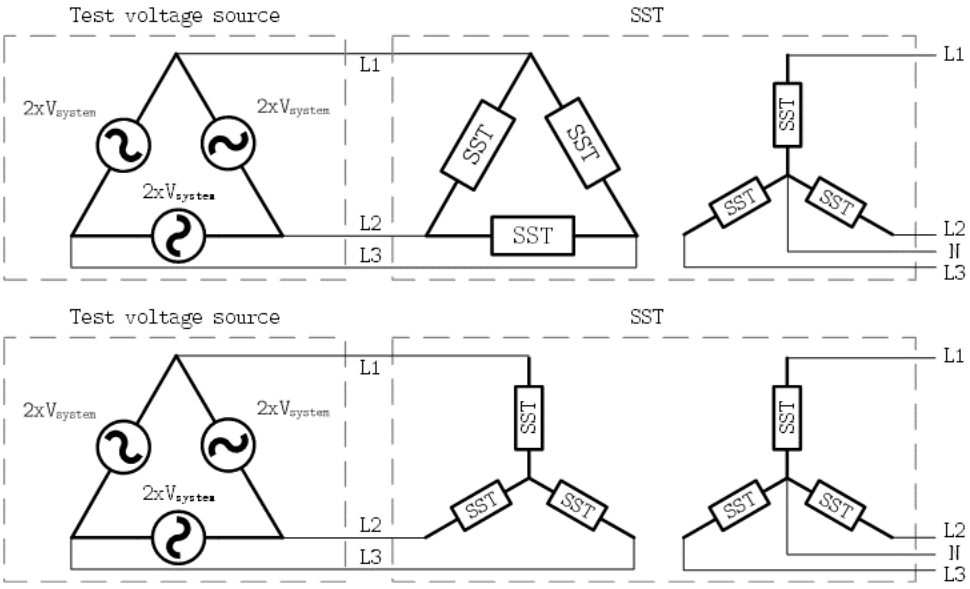


Figure 11-5 √3 voltage reduction through Δ-Y configuration

In the top part of Figure 11-5, the MV side of the SST is facing the same voltage as the grid / test voltage. In the bottom half of Figure 11-5, the power electronics is connected in wye, resulting in a factor √3 reduction of the voltage. Note that active control of the floating neutral point is essential in this case, so the SST must be operational for the IVW & IVPD tests. As depicted, this configuration of a "single module / H-bridge" at the MV side, however, would still not be feasible since the voltage would still

exceed any available (commercial or otherwise) switching device's breakdown limits. As was established in chapter 9, the switching device with the highest voltage handling capability that is available for testing is a laboratory prototype devised by Wolfspeed. This switching device is a SiC MOSFET that has a maximum breakdown voltage of 15 kV (unfortunately, these were not available).

11.2.1.1 Redundancy

Due to the importance of high reliability (see paragraph *14.1.1 Customer-minutes-lost* on the importance of this high reliability), several topologies were evaluated with regards to redundancy. These are shown in Figure 11-6 below, with progressively more redundancy / fault tolerance from left to right.

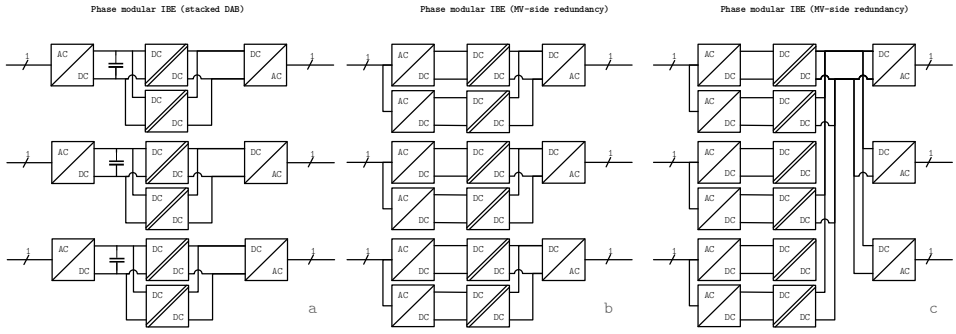


Figure 11-6 Topology redundancy investigation

The first topology in Figure 11-6a shows a partial redundancy of the SST. In this topology, only the DAB has been made redundant. An argument for such a topology would be that the DAB itself is already complex in nature and with a minimum of eight switches (assuming bi-directional power flow capability), many failures can occur. A second argument is that the DAB forms the isolation stage of the SST. The DAB transformer is critical to ensure the isolation of the MV & LV grids and its insulation design is currently still a high-risk aspect (especially with the newly identified 40 kV_{PEAK} test voltage in this thesis). As such, having redundancy of this transformer could be beneficial. However, both arguments are not

very strong. This is because there are many aspects of an SST that are still very critical design-wise, such as the CHB.

A much more logical redundancy scheme is found in Figure 11-6b, where the cascaded H-bridge is also made redundant together with the DAB. This ensures a better chance of having at least one "module" operational in case of a failure in *either* the DAB or the CHB (whereas in the first topology a failure in the CHB would result in a complete failure of the phase). This is also a good point to note that none of these three topologies qualify for the SST due to only having a single conversion stage at the MV side. In the topology of Figure 11-6b, a single failure would imply losing an entire phase at once.

This is where the topology of Figure 11-6c comes in. This topology has all MV modules connected to a single DC-bus, and it ensures that a failure of one of the MV side modules will not result in any failure on the LV side (inverter configurations are ignored for simplicity). This is great for up-time and customer-minutes-lost. The final chosen topology is similar to this one, however, it is important to first address two popular topologies from literature.

11.2.1.2 The Cascaded H-Bridge and Modular Multi-level Converter

There are two topologies that are widely investigated in literature, and both are addressed here. The first is the Cascaded H-Bridge (CHB) depicted in Figure 11-7a and the second is the Modular Multi-level Converter (Figure 11-7b). Both are particularly suited for an SST because the dimensioning of the input voltage is scalable by "simply" adding more modules in series.

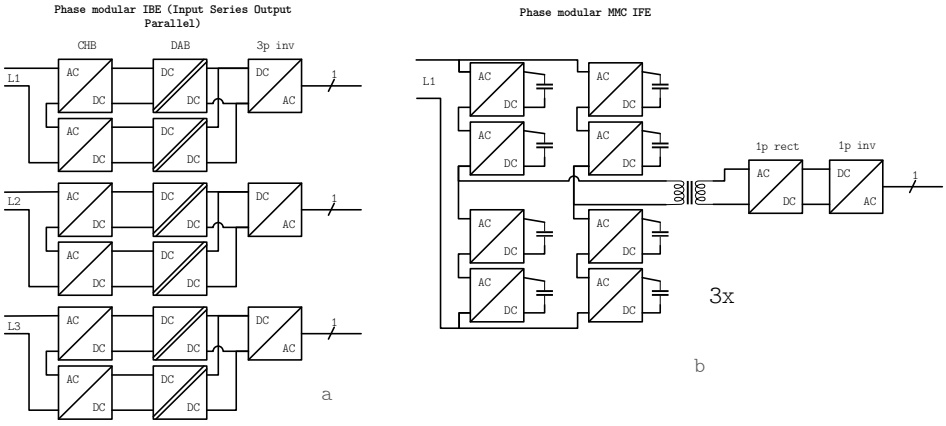


Figure 11-7 Cascaded H-Bridge and Modular Multi-level Converter

Note that the grid connection configuration is left "undefined" as these could be connected in delta or wye (with wye offering the aforementioned advantage of a √3 voltage reduction on the MV side). The MMC has one significant design challenge, and that is its very large DC-bus voltage on the MV-side. From a modularity perspective, a CHB applies a "divide and conquer" on that DC-bus voltage, making it more interesting for industrialization. The CHB also divides the critical isolation stage over multiple modules. Whereas for the MMC, all power is transferred through the single transformer. Lastly, the CHB can be made up of modules in such a way, that the CHB and DAB are combined and over-dimensioned voltage wise. This over-dimensioning would result in a degree of redundancy. Because when a module fails, the MV input voltage and transferred power could be distributed over the other modules (within limits of course).

It is for the arguments presented in this chapter until this point, that the chosen power architecture will be a Cascaded H-Bridge, with each having its own DAB in an ISOP (Input Series Output Parallel) configuration.

11.2.2 The selected SST power architecture

As summarized in the previous paragraph, the chosen SST power architecture will be made up of modules that each have a Cascaded H-Bridge, followed by a DAB. These modules are connected in an ISOP (Input Series Output Parallel) configuration. This leads to the topology that is depicted below in Figure 11-8. This topology sees n modules in series per phase.

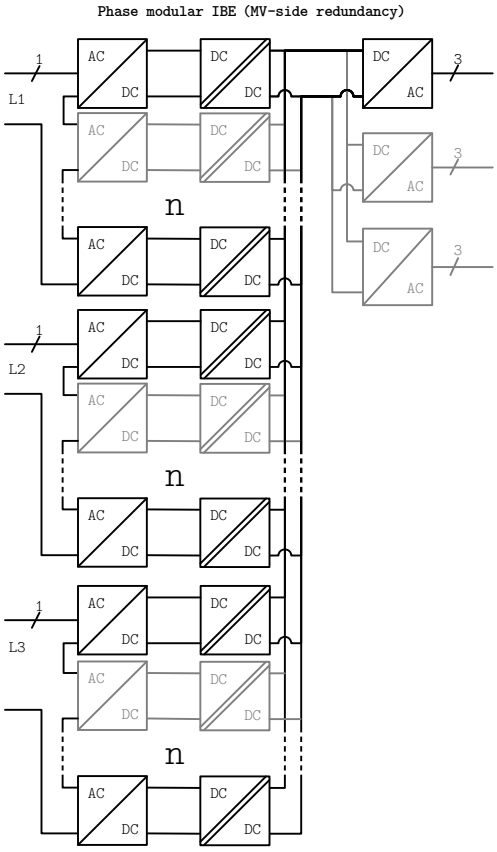


Figure 11-8 The selected SST power architecture

There are four things to note. The first is that the grid connection configuration is left "undefined" as this could be connected in delta or wye (with wye offering the aforementioned advantage of a √3 voltage reduction on the MV side). The second is that the inverter stage can be implemented in multiple ways. It can either

be a single inverter that feeds the LV AC busbar in the substation, or multiple inverters (e.g., one per feeder). The third thing to note is that the number of modules per phase is *highly* dependent on the selected switching devices. This leads to the selection of the switching devices in the next paragraph.

11.2.3 Switching device selection and SST module voltage levels

Having established the overall power architecture, the next step is to select the switching devices, and consequently, the amount of SST modules per phase. Generally, switching devices with a higher breakdown voltage, will result in fewer SST modules. This is because the input voltage on the MV side is max. 24 kV_{RMS} (according to the standard), and this voltage needs to be divided over the number of modules. The higher the voltage handling capability, the fewer SST modules needed. The breakdown voltage of switching devices is however not the only factor that impacts the overall SST power architecture. Each switching device has certain switching characteristics that influence its thermal behavior. Conduction and switching losses generate heat that must be dissipated via heatsinks (with larger heatsinks reducing power density). Additionally, cost has been a major driving force throughout the project.

To investigate the impact of certain switching devices and their characteristics, a tool was developed in Microsoft Excel. The Excel sheet takes several parameters as input, and it will calculate a significant number of outputs. These in- and outputs are listed in Table 6 below. These numbers are given per "converter arm". This "converter arm" is essentially a phase of the SST, but since it could be configured in delta or star, the term "converter arm" was chosen.

Inputs per converter arm	Calculated outputs
$V_{MV\ MAX.\ INPUT}$	Number of modules per phase
$V_{LV\ DC\text{-}bus}$	Voltage per module
$P_{SST\ per\ phase}$	Current through each module
$f_{Switching\ CHB}$	DAB transformer ratio
$f_{Switching\ DAB}$	Estimated THD_V on the MV side
CHB switch type	CHB switching & conduction losses
DAB_{MV} switch type	DAB_{MV} switching & conduction losses
DAB_{LV} switch type	DAB_{LV} switching & conduction losses
	All diode conduction & RR losses
	Total losses of SST
	Losses per module
	Total efficiency of SST over its load range
	Efficiency per module
	Cost estimate (based on available info.)

Table 6 SST topology selection Excel sheet in- and outputs

The Excel tool automates a large number of calculations and provides a fast overview of the impact switching device has on the overall SST. As can be seen from Figure 11-9 below, only few inputs are necessary, and a large amount of information is outputted to the designer. The inputs are the cells marked in grey, all other values are calculated automatically. The section on the left displays the overall SSTs values, and the "blocks / sections" at the top are used to select the switching devices for the CHB, DAB_{MV} and DAB_{LV} switches (from left to right). An estimate is made on the load/efficiency curve, this is displayed at the bottom right with the values for the generation of the graph on the bottom-left.

Note that this is only the front sheet, as there are several other worksheets in this excel file that hold the data of the switching devices that can be selected.

Figure 11-9 Excel tool for calculating switching device impact on SST

These switching device selection worksheets are essentially tables from which the front sheet looks up the necessary values. For the IGBTs, the data table looks like Table 7 (several columns are omitted to avoid clutter).

V_{CES}	Brand	Component ID	$V_{CE\ SAT}$	V_{Fdiode}	I_C	E_{ON}	E_{OFF}	$E_{RRdiode}$	Price
600V	Infineon	FF200R06KE3	1,65V	1,0V	200A	1mJ	3mJ	2mJ	€77
1200V	Infineon	FF400R12KT4P	1,87V	0,9V	400A	6mJ	6mJ	12mJ	€223
1700V	ABB	5SNG 0150Q170300	2,47V	1,2V	150A	20mJ	18mJ	20mJ	-
1700V	Infineon	FF150R17KE4	2,20V	1,2V	150A	23mJ	18mJ	22mJ	€99
2500V	ABB	5SNA 1500E250300	2,25V	0,7V	1500A	100mJ	200mJ	200mJ	-
3300V	Hitachi	MBN1200F33F-C	2,38V	0,9V	1200A	15mJ	50mJ	15mJ	€1300
3300V	SEMIKRON	SKM450GB33F	2,56V	1,2V	760A	601mJ	601mJ	100mJ	€1307
3300V	Powerex	QID3310006	3,28V	1,0V	100A	30mJ	30mJ	30mJ	-
3300V	Dynex	DIM100PHM33-F000	3,20V	1,8V	100A	48mJ	25mJ	40mJ	€50
3300V	Dynex	DIM125PHM33-TL000	2,47V	2,5V	125A	260mJ	340mJ	140mJ	-
3300V	Dynex	DIM125PHM33-TS000	2,67V	2,5V	125A	210mJ	270mJ	140mJ	-
3300V	Dynex	TIM250PHM33-PSA011	2,98V	2,4V	250A	510mJ	380mJ	360mJ	-
3300V	ABB	5SNG 0450X330300	2,98V	1,1V	450A	100mJ	150mJ	150mJ	€207
3300V	ABB	5SNA 0800N330100	3,65V	0,8V	800A	200mJ	375mJ	275mJ	€1382
3300V	Infineon	FZ1000R33HL3	2,93V	0,7V	1000A	250mJ	250mJ	450mJ	€1352
4500V	ABB	5SNA 0650J450300	3,53V	1,4V	650A	350mJ	555mJ	300mJ	-
4500V	Infineon	FZ800R45KL3_B5	3,04V	1,0V	800A	800mJ	400mJ	400mJ	€1493
6500V	ABB	5SNA 0400J650100	5,08V	1,7V	400A	700mJ	300mJ	500mJ	€832
6500V	Infineon	FD250R65KE3-K	3,58V	1,5V	250A	500mJ	300mJ	400mJ	€1859

Table 7 IGBT switching device information

The table is sorted by breakdown voltage, this is a direct result of the IEC60076-3's test voltage being so high, that it becomes the primary evaluation criteria of the SST's design. The table also holds hyperlinks (where available) to show the sources. The prices have been sourced from Farnell, Digikey, Newark, Octopart and other websites.

For IGBT losses, there are two main categories that are important. The first is the $V_{CE\ SAT}$ (collector-emitter saturation voltage), which is used to determine the conduction losses of the switch in combination with the IGBT. The second category are the switching energies. These are used to calculate the switching losses of the IGBT. Lastly, there is the cost associated with each switching

device. Some notable switching devices in Table 7 are 6500V power modules from ABB & Infineon and the 3300V Dynex power modules. The ABB / Infineon modules would result in the least number of H-bridges in the cascade for withstanding the high testing voltage of the standard. These power modules are, however, also quite inefficient due to their high switching energies (resulting in higher losses). Lastly, these modules were prohibitively expensive with respect to the budget. The Dynex 3300 V power modules are very cost effective at only €50 per switch and offer competitive switching energies. Ultimately, the chosen DIM100PHM33-F000 were by far the best available choice.

IGBTs, however, are not the only type of switching device available. For the MOSFETs, another worksheet was made and filled with information from the datasheets. See Table 8 below.

V_{dss}	Brand	Component ID	$R_{DS\ on}$	V_{Fdiode}	I_C	E_{ON}	E_{OFF}	$E_{RRdiode}$	Price
1200V	ROHM	SCT3030KL	38mΩ	-	51A	1,30mJ	0,60mJ	-	€ 47
1200V	ROHM	BSM120C12P2C201	25mΩ	-	134A	1,20mJ	0,70mJ	-	€ 355
1200V	ST	SCTWA50N120	60mΩ	3,5V	50A	0,71mJ	0,43mJ	0,50mJ	€ 25
1200V	SEMIKRON	SKM350MB120SCH15	7mΩ	-	416A	0,65mJ	0,25mJ	-	€ 175
1200V	Infineon	FF23MR12W1M1_B11	28mΩ	-	50A	0,54mJ	0,09mJ	-	€ 85
1700V	CREE	C2M0045170D	85mΩ	-	48A	2,00mJ	0,50mJ	-	€ 91
1700V	CREE	CAS300M17BM2	11mΩ	-	225A	0,40mJ	0,20mJ	-	€ 756
1700V	CREE	C2M0080170P	118mΩ	3,5V	40A	0,07mJ	0,22mJ	0,35mJ	€ 772
1700V	CREE	C2M0045170P	65mΩ	-	72A	0,35mJ	0,10mJ	-	€ 24
1700V	IXYS	IXFN90N170SK	34mΩ	-	90A	3,50mJ	0,70mJ	-	€ 150
3300V	Hitachi	MSM600FS33ALT	3mΩ	4,0V	600A	50,00mJ	9,00mJ	4,00mJ	€ 600
3300V	CREE	XHV-7 Wolfspeed	8mΩ	3,3V	500A	5,00mJ	1,00mJ	1,00mJ	€ 1.631
6500V	-	-	15mΩ	-	250A	19,00mJ	11mJ	-	€ 3.454
10000V	CREE	XHV-6 Wolfspeed	24mΩ	-	50A	20,00mJ	13mJ	-	€ 5.276

Table 8 MOSFET switching device information

Again, just as with the IGBTs, the MOSFETs are sorted by breakdown voltage. And just like with the IGBTs, there are two categories of losses. The conduction losses (determined by $R_{DS\ on}$), and the switching losses (determined by the switching energies. Lastly, there are the prices (these have been sourced from Farnell, Digikey, Newark, Octopart and other websites).

There are several switching devices here that need to be specifically discussed. The last three in the table are switching devices that are not available on the market. These are prototypes that could be procured through Wolfspeed. While high in cost, these are very efficient switching devices due to their low switching energies, while still having a high breakdown voltage. The other switch that needs to be highlighted is the 118mΩ / 1700V switch from CREE. The C2M0080170P was the device chosen due to its availability within Prodrive Technologies. While CREE offers several 1700V switching devices, this is the one with the lowest switching energies. These losses end up outweighing the higher $R_{DS\ on}$ related conduction losses.

With all these switching devices, there is one more optimization to consider, and this is how the topology of the DAB directly relates to the CHB. In Figure 11-10, two DAB configurations are shown with respect to the CHB. Depending on the definition used, this is a two-level two-level DAB, abbreviated by 2L-2L DAB because of the two voltage levels that it *has*. Other definitions exist, where such a DAB is referred to three-level three-level (3L-3L), due to the voltage levels it can *create*. For the purposes of this thesis, the first definition will be used (see chapter 5 Definitions).

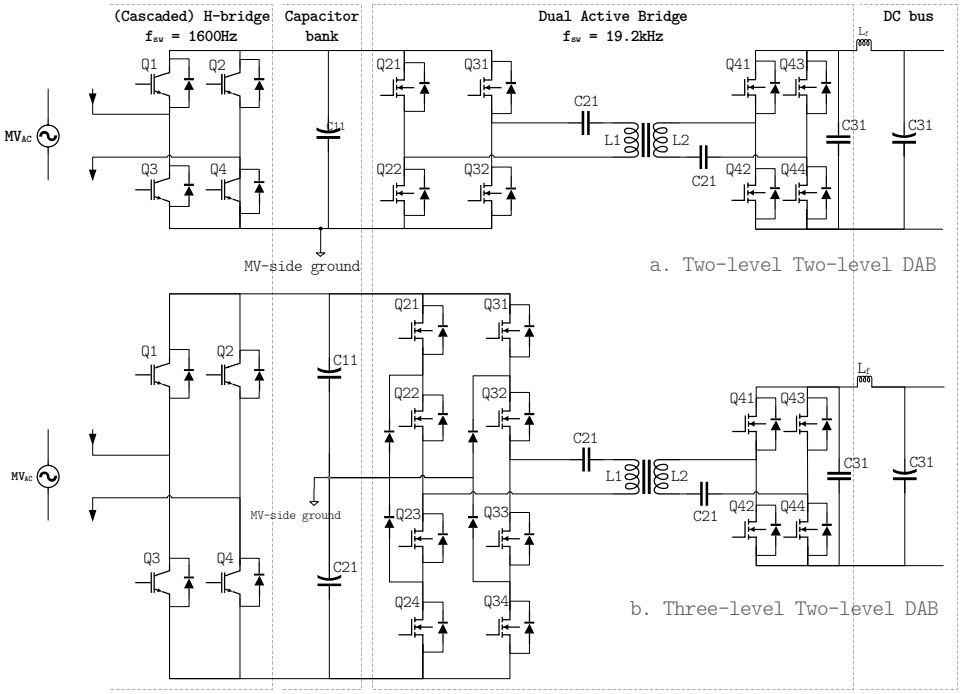


Figure 11-10 A 2L-2L DAB and a 3L-2L DAB

The most commonly found solution in literature is depicted in Figure 11-10a. Here, the DAB and CHB both have two voltage levels and consequently, the breakdown voltage of all the switches can also be selected as being the same. This is a straightforward design, and it offers advantages with respect to economies-of-scale due to higher numbers of identical switches. This is advantageous when considering supply chains and simplicity. In Figure 11-10b, a 3L-2L DAB is shown. This configuration is more complex requires the creation of a midpoint in the MV side DC. Additional complexity comes from the use of eight switches on the MV side. Note that there are more configurations / topologies of DABs that are also 3L-TL, such as a T-type bridge. These were not evaluated due to their even higher complexity.

There are two important advantages to the topology presented in Figure 11-10b. The first is that the CHB can have switching devices with breakdown voltages that are twice as high as the switching

devices of the DAB. **This topology effectively *halves* the amount of SST modules at the "cost" of only four switches more per module.** The second is the increased switching freedom with respect to zero-voltage switching, meaning increased efficiency over a larger load range.

11.2.4 SST isolation architecture

The SST needs to replicate the isolation function of a conventional transformer if it is ever going to replace it. Since the transformers can be placed in MV & LV grids that have neither or only a single side earthed, isolation is indeed important.

In the designed prototype, there are five main aspects with regards to isolation of the MV & LV sides of the power electronics.

1) The DAB transformer (§ 11.2.4.1)
2) Intra-module (internal) fiber optic communication (§ 11.2.4.2)
3) Inter-module fiber optic communication (§ 11.2.4.3)
4) Isolated power supplies (§ 11.2.4.4)
5) Physical isolation of MV & LV mechanical assemblies (§ 11.2.4.5)

In the following subsections, each of these aspects will be dealt with in greater detail, as well as their relevance with respect to IEC60076-3.

11.2.4.1 The DAB transformer

The DAB transformer is arguably the most critical component of the isolation strategy, although all five aspects must be dealt with to avoid a catastrophic failure of an SST.

In literature, existing DAB prototypes recognize the need for isolation, but prototype designs do not do *everything* possible to avoid failure of the isolation function. Specifically, in [30] and [54], both use Litz wire for the MV-winding. Litz wire is inherently riskier with respect to introducing voids (air bubbles) during the isolation potting process (see Figure 11-14). To their credit, [30] uses a transformer design that has an insulation level of 38 kV. While that is still insufficient to meet the IEC60076-3 AV test,

it is the highest isolation value that has been found in literature for such a DAB transformer. The paper specifically mentions that this DAB transformer is intended for traction applications. It also mentions that the 35 kV is taken from a standard mentioned in [32]. Reviewing [32], however, no mention of a standard is made. Though, the presented DAB transformer is designed with particular attention being paid to the insulation between the primary and secondary windings. The insulation level is achieved by using MV cabling as the MV winding. Since the paper is written for high-speed rail / traction applications, it is likely that the standard to which the DAB transformer was designed, was for rail / traction applications as well. Their methodology of using MV cabling for the MV winding of the DAB transformer, however, is also valid for designing an SST for grid applications. The cabling insulation must then be rated for the AV test voltage level.

While [54], contains the following reference to partial discharge levels and "standards", it makes no mention of any standards.

> "*…parallel and distributed winding style can be a good solution for increasing the coupling coefficient. In this case, the voltage difference between windings should be taken into consideration for insulation reasons. Fortunately, new generation Litz wire jackets (such as Teflon) have high electrical insulation levels and they meet the partial discharge level standards.*"

Additionally, the work presented is focused on the efficiency of the transformer, with particular focus on the leakage inductance, there is no other mention of insulation anywhere else in the paper. With the in- and output voltage levels being 1kV, it is reasonable to assume that the transformer's insulation level is taken as the same value. But, that is still an assumption none the less. More revealing is the chosen core structure in figure 4 of their paper. A shell-type construction, which cannot be made IEC60076-3 compliant due to the physical distance of the MV winding to the

core. The IEC60076-3 states a creepage distance of 120 mm is necessary between the SSTs MV & LV sides, which is not possible with the core being (mandatory) grounded to earth. With designing the DAB transformer, special care must be taken with respect to the leakage inductance as well [55].

For the SST prototype of this thesis, the DAB transformer was designed and implemented with several specific parameters in mind. These are listed in Table 9 below.

DAB transformer design parameters	**Value**	**Unit**	**Remark**
$f_{Switching\ DAB}$	20	kHz	
$V_{input\ nom.}$	1400	V	
$V_{input\ max.}$	3000	V	DAB PWM changed to keep same Volt-second
$V_{output\ nom.}$	700	V	
$V_{output\ max.}$	800	V	
$I_{RMS\ prim.}$	7	A	200kW / 10,5kV_{RMS} per converter arm (phase)
$L_{leakage}$	700	uH	
$V_{Isolation\ prim-sec}$	28	kV_{RMS}	@50 Hz for 60 seconds
Creepage distance	120	mm	Between MV and ground (transformer core)

Table 9 DAB transformer design parameters

It should be noted that there are three parameters from Table 9 directly related to the IEC60073-3 standard. The third parameter ($V_{input\ max.}$) is related to the standard because of the IVW & IVPD test voltage on the MV input, and the last two parameters due to the AV test & isolation requirements.

The leakage inductance was determined using a rule of thumb from the "Advanced Power Electronics" classes from the Eindhoven University of Technology (5SWB0 by Jordi Everts). This rule of thumb formula is shown in 11-1 below.

$$L_{leakage} \approx \frac{N \cdot V_{output}}{8 \cdot f_{switching\ DAB} \cdot (1{,}2 \ldots 1{,}3 \cdot I_{peak})}$$

11-1

This leakage inductance requirement was later changed from "only the DAB transformer" to "the DAB transformer plus an external inductor". This allowed for a more optimal magnetic design of the transformer itself. The necessary "leakage" inductance was achieved by adding a specific inductor in series with the DAB transformer. This effectively added the inductances up to the required level.

With these parameters established, the design could be started. There are two aspects to the design. The magnetics design, and the isolation design. The magnetics design was performed by a bachelor student from Fontys hogescholen in Eindhoven for his graduation project (Edon Meda). The isolation design was the scope of the writer of this thesis.

1) Magnetics design

The magnetic design document is too elaborate to fully discuss here. As such, only several aspects will be highlighted. Starting with the final design parameters that have been established, these are listed in below.

Parameter	**Condition**	**Value**	**Unit**
Material		N87	-
μ_r	Relative permeability	2300	-
N_P	Primary number of turns	63	-
N_S	Secondary number of turns	32	-
L_P	Primary inductance	3,91	mH
L_S	Secondary inductance	1,01	mH
$I_{L\ mag\ peak}$	Peak magnetizing current	4,26	A
A_E	Cross sectional area	1680	mm^2
V_E	Effective core volume	1119480	mm^3
B_T	Flux density	0,157	T
l_g	Air gap length	2	mm
F	Fringing flux factor	1,07	-
R_P	MV winding resistance (DC)	15,9	mΩ
R_S	LV winding resistance (DC)	30,5	mΩ
MLT_P	Mean length turn for the MV winding	300	mm

MLT_S	Mean length turn for the LV winding	260	mm
P_C	Core losses	28	W
P_W	Wire losses	9,4	W
P_T	Total losses	37,9	W

Table 10 Final design specifications of the DAB transformer

Note that this table is the result of many calculations and several design iterations. Of all these calculations, equivalent models, core material comparisons, geometry considerations, and many more, only two will be discussed here. The first is to show the extent of the design details that were investigated. Shown in Figure 11-11 below, is a FEM analysis of the flux density in the core of the DAB transformer.

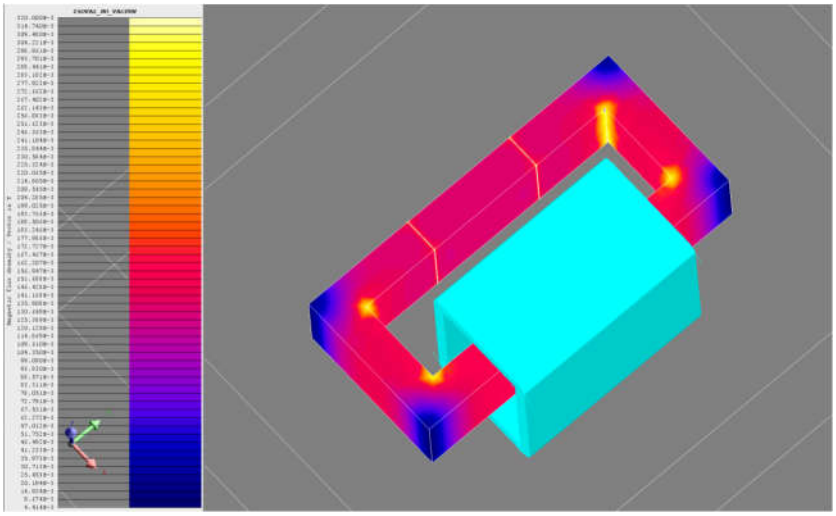


Figure 11-11 FEM analysis of flux density in the core

A more relevant simulation is the isolation evaluation that was performed. In Figure 11-12, the result of the electric field strength simulation is shown. The conclusion of this simulation was that the maximum field strength was 7,1 kV/mm, which is well below the 20kV/mm break down limit of the used epoxy.

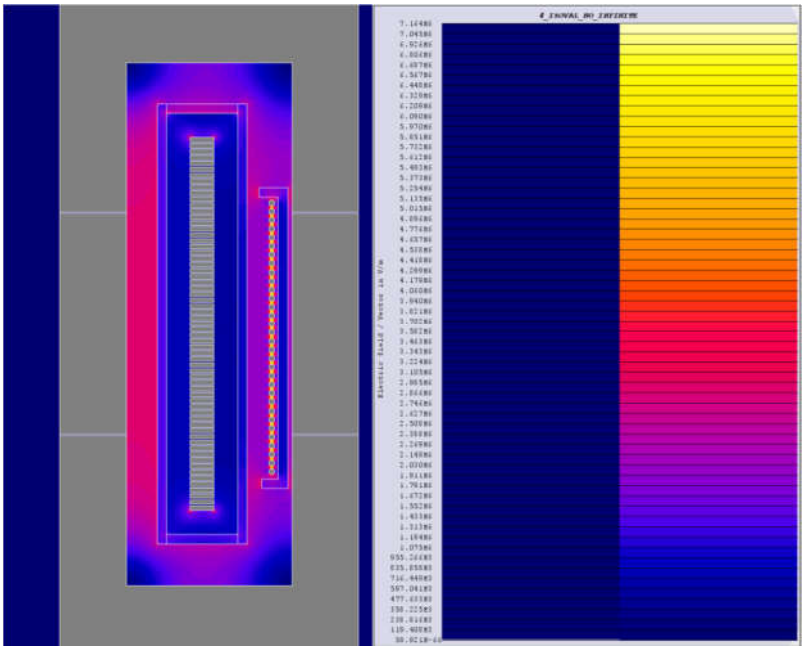


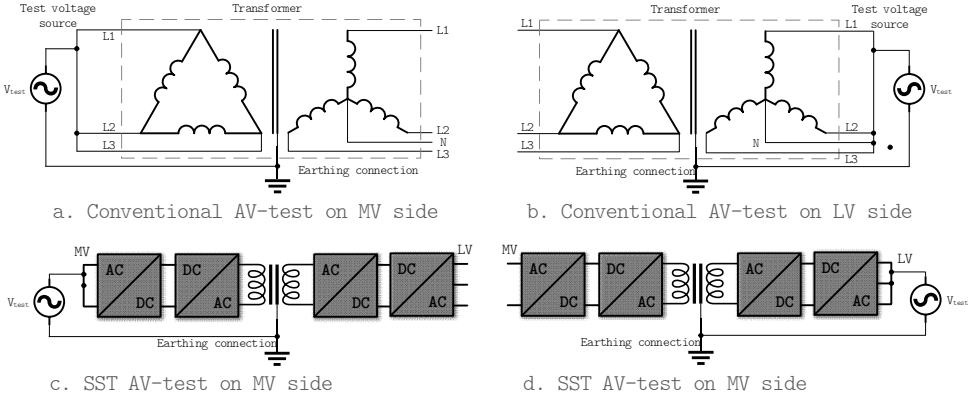
Figure 11-12 Electric field strength of the isolation

With the magnetic design established, it is necessary to look at the design of the DAB transformer's isolation, as well as the considerations & rationales that were found in the process.

2) Isolation design

The isolation design of the DAB transformer is crucial for ensuring galvanic separation of the MV and LV grids. The degree of isolation of the DAB transformer is directly related to the AV test of the IEC60076-3 standard. As described in paragraph 10.2.2.8, the test is performed on conventional transformers by connecting the winding terminals together and applying an alternating voltage with respect to ground. For conventional transformers, this is with respect to the transformer core, as these are required to be grounded. In Figure 11-13a-b below, the AV tests for the MV & LV sides of conventional transformers are shown respectively. The tests are very similar in nature (windings connected and voltage applied with respect to core), yet they are performed at very different voltage

levels. For the MV side, V_{test} is ≈40 kV_{PEAK} at 50Hz for 60 seconds. For the LV side, V_{test} is ≈4,3 kV_{PEAK} at 50Hz for 60 seconds.



a. Conventional AV-test on MV side

b. Conventional AV-test on LV side

c. SST AV-test on MV side

d. SST AV-test on MV side

Figure 11-13 AV isolation test consequences for DAB transformer

When applying these MV & LV AV tests to SSTs, the results look something like Figure 11-13c-d respectively. Note that the figures are very much simplified due to only one SST module being shown! For illustration purposes, however, these figures show the effect of the IEC60076-3 AV test standard clearly. The "winding" terminals of the SST are again connected together, and the test voltage is applied with respect to ground. **The result is that the IEC60076-3 AV (Applied Voltage) test voltage is effectively going to be applied to the DAB transformer.** This means not only careful consideration of the type of insulation material, but also the type of winding material.

For any transformer, there are many choices of insulation material to choose from. Oil and paper are typically used in conventional transformers, and epoxy or silicone is typically used in power electronics. The use of an oil-based insulation for power electronics would be interesting due to the "self-healing" properties of oil. Since any partial discharge would permanently degrade epoxy or silicone-based insulation materials, oil could be interesting to investigate for the purposes of SST longevity. For practical implementation, however, oil is a much more difficult

insulation material to work with due to the necessary sealing of any enclosure. Avoiding leaks and over-pressure due to heating effects are all aspects that need to be covered. Instead, it was opted to go for the more traditional solutions of power electronics (epoxy or silicone).

The insulation material was chosen based on its availability at the consortium partner Prodrive Technologies. There were two materials that were available, PU (Polyurethane) and epoxy. Ultimately "W 342" epoxy was chosen because it had a slightly higher insulation performance at 21~23 kV/mm, and it had lower viscosity compared to PU. The lower viscosity is important, as it will flow better during the potting process, reducing the risk of voids. It is critical to avoid these bubbles/voids in the potting because there is a high probability that with high voltage stresses, a partial discharge would occur within them. Once such a partial discharge occurs, it has permanently degraded the insulation, slightly lowering the insulation level at that void in the process. From that moment on, it is only a matter of time until the entire insulation barrier becomes compromised. Especially when comparing to a conventional transformer, a potting void is more likely than not, to become an issue over the course of a 50-year service life.

To reduce the risk of potting voids, the next consideration must be the winding material of the DAB transformer's MV winding. It is quite common to use Litz wire for transformers in power electronics. Litz wire reduces the skin effect losses at higher frequencies, which is typically where power electronics operates. Litz wire, however, is also more prone to potting voids due to the complex 3D geometry that it has. In Figure 11-14 below a visualization is made of how potting voids can form within or in proximity of Litz wire. Lower viscosity insulation materials will help mitigate the problem, as well as potting under vacuum. A better way to manage this risk is to avoid the use of Litz wire altogether.

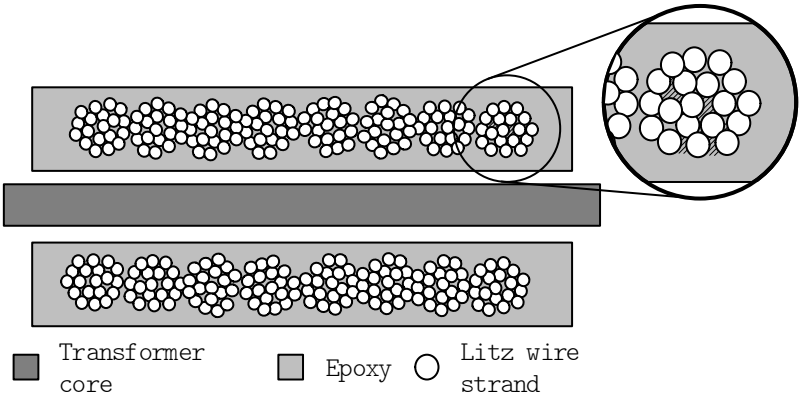


Figure 11-14 Potting voids in Litz-wire based windings

This was recognized by Rothmund in his thesis [56]. There, the choice was made to use normal solid-core copper wire for the MV side, and only use Litz wire for the LV side. For this SST prototype, the same choice is made to reduce the probability of potting voids. The next risk-area for potting voids comes from the bobbin. It is here where [56] uses a 3D-printed bobbin that is quite high in geometric complexity.

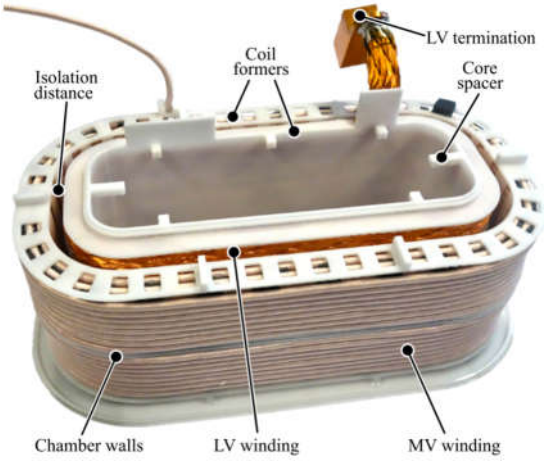


Figure 11-15 DAB transformer prototype from ETH Zurich [56]

It is in this geometric complexity that there is still a high(er) probability of voids between the MV windings and the bobbin. For

this SST prototype, an additional effort was made to eliminate the bobbin from being potted in the isolating epoxy.

The first prototype used an edge-wound rectangular (10x2mm) copper wire for the MV winding. It was thought that this winding would be mechanically stiff enough to hold its shape while being potted. During verification, however, this turned out not to be the case. In Figure 11-16a below, the edge-wound rectangular wire is shown. In Figure 11-16b, a 3D model of the MV winding is illustrated, and the design software (OnShape) determined that the mass was 5,3 kg.

a. Edge-wound copper 10x2mm

b. 3D winding design

Figure 11-16 Rectangular edge-wound copper MV winding

In Figure 11-17, a verification X-ray of the first potting can be seen. The image ghosting effects of the X-ray are due to it being taken on a machine intended for the verification of PCBs. This introduces focus errors and a shifted image. On the bottom left, there is a subtle curve of the windings visible

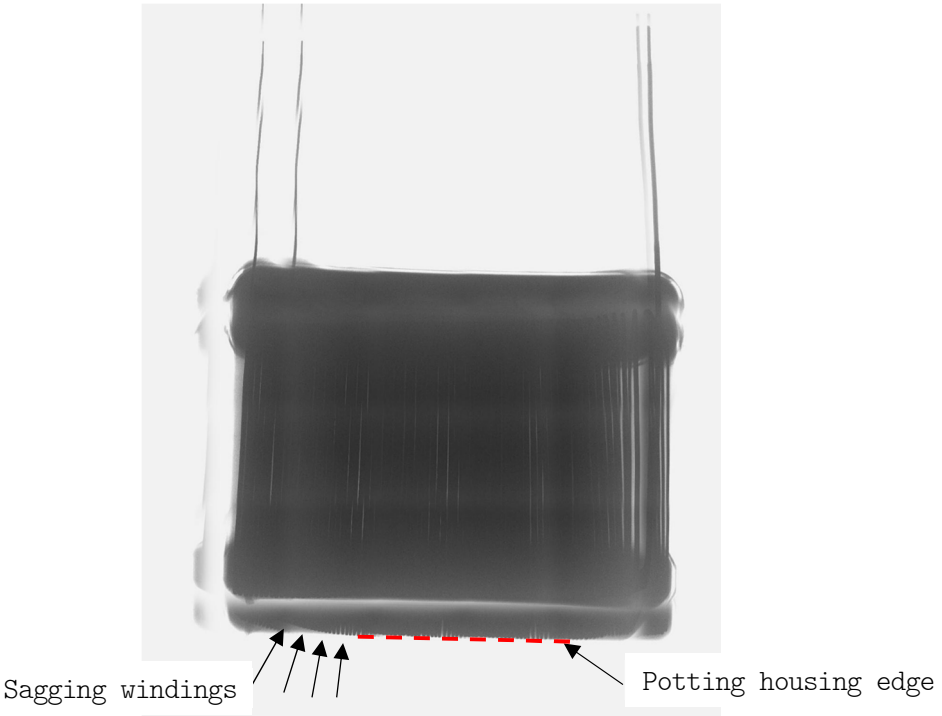


Figure 11-17 X-ray of DAB transformer after epoxy potting

It is this curve that indicates that the winding has buckled and sagged under its own weight during the potting & curing process. For the second iteration, a means was sought to stiffen this MV winding during the potting process. Several solutions were evaluated, such as using (Kapton) tape and a 3D-printed clamp to keep the MV winding in its shape. In the end, these were rejected because they involve potting in an additional object that can introduce potting voids. And while a 3D-printed part is a seemingly attractive solution, it is in fact very problematic. 3D-printed parts have inherent voids within them due to the manufacturing processes involved. This makes 3D-printed parts for any type of high voltage application questionable.

In the end, the choice was made to perform the potting in two stages. The first stage is to pot the winding together to itself, creating a stiff MV winding "assembly". The second stage is potting

that MV winding into a potting enclosure (this is not without risk itself, because adhesion between the first and second pottings may not be perfect). The first stage is illustrated in Figure 11-18a-c. In Figure 11-18a, the MV winding of the DAB transformer is depicted. This MV winding is placed in a small 3D-printed "bucket" that perfectly fits the winding (Figure 11-18b). This bucket is then filled with epoxy under vacuum. After the epoxy has cured, the bucket is removed. The end result is shown in Figure 11-18c, where the MV winding is now glued on the bottom. This results in a winding that is very stiff and can be potted in its entirety in the next stage of the process.

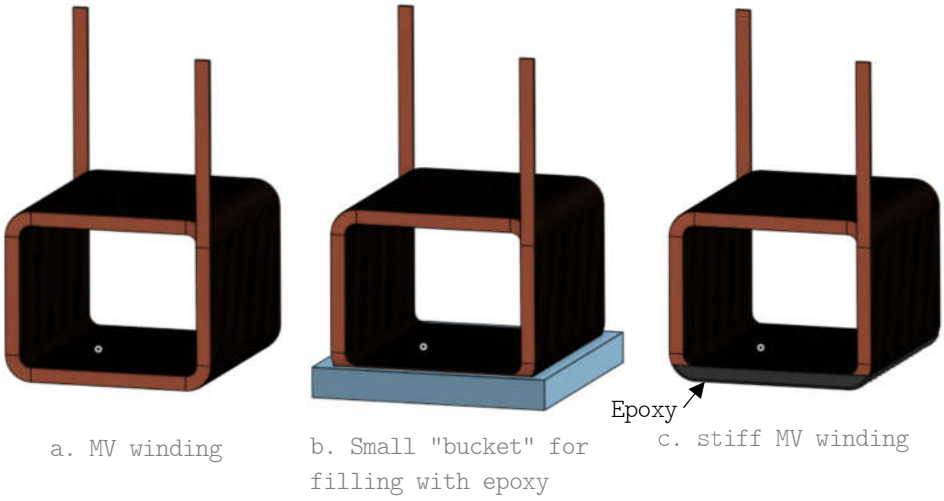
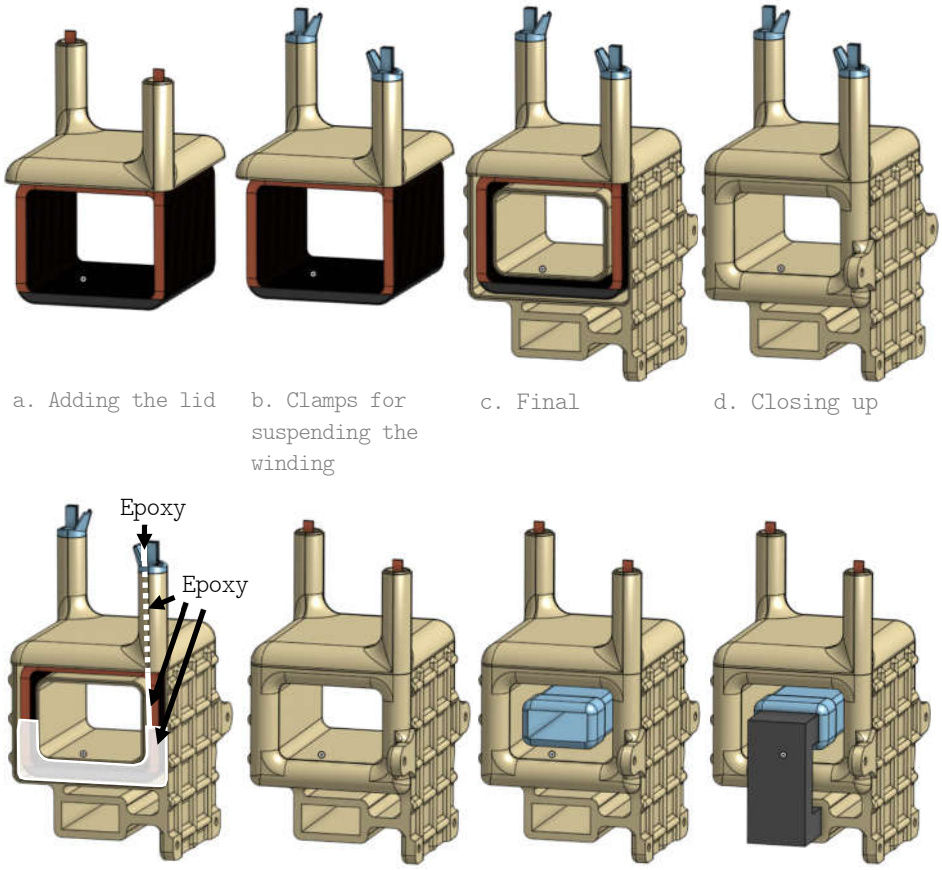


Figure 11-18 First stage of DAB transformer potting

The second stage of the potting process involves encasing the now stiff MV winding into an assembly of 3D printed parts that will be filled with epoxy. Due to the complexity of the DAB transformer's geometry, this second stage requires quite a few steps. These are depicted in Figure 11-19a-h below.



a. Adding the lid b. Clamps for suspending the winding c. Final d. Closing up

e. Adding epoxy f. Clamp removal g. Add LV winding h. Add core

Figure 11-19 Second stage of DAB transformer potting

Steps a through d start with the assembly of the MV winding enclosure around its copper. This volume will be filled with epoxy in the following steps, but before that, it is critical that this winding has at least 2mm clearance on all sides of the enclosure. This 2 mm is derived from the selected potting material ("W 342" epoxy), which has an insulation performance at 21~23 kV/mm. At 2 mm, the isolation level should reach 42-46 kV, which exceeds the AV test voltage of the IEC60076-3 of 39,597 kV_{PEAK} (see equation 10-3). Achieving this 2 mm clearance is achieved in step c, right

before the enclosure is sealed up, by making small adjustments at the clamps that were installed in step b.

Once the enclosure is sealed up, epoxy is poured down under vacuum through a gap in one of the clamps (step e). Note that while not depicted, the epoxy is poured until it reaches all the way up to the clamps at the top. Reaching the top is necessary to create a physical distance of 120 mm, required by the IEC60076-3 (see paragraph 10.3). With the volume filled completely with epoxy, it is set aside in its entirety for 24 hours to let the epoxy cure. Once cured, the clamps are removed from the copper winding part in step f. This is then followed by adding the LV winding inside the MV winding (step g) and inserting the two U-shaped core parts on either side (step h). The two pieces of core material suspend the LV winding equidistant from the MV winding and ensure there is a small gap for cooling through natural convection in between the windings.

A close-up view of the cross section after all the potting steps is illustrated below in Figure 11-20. The first thing it reveals is a minor design deficiency where the top and bottom distance from the copper to the edge of the enclosure are not the same distance.

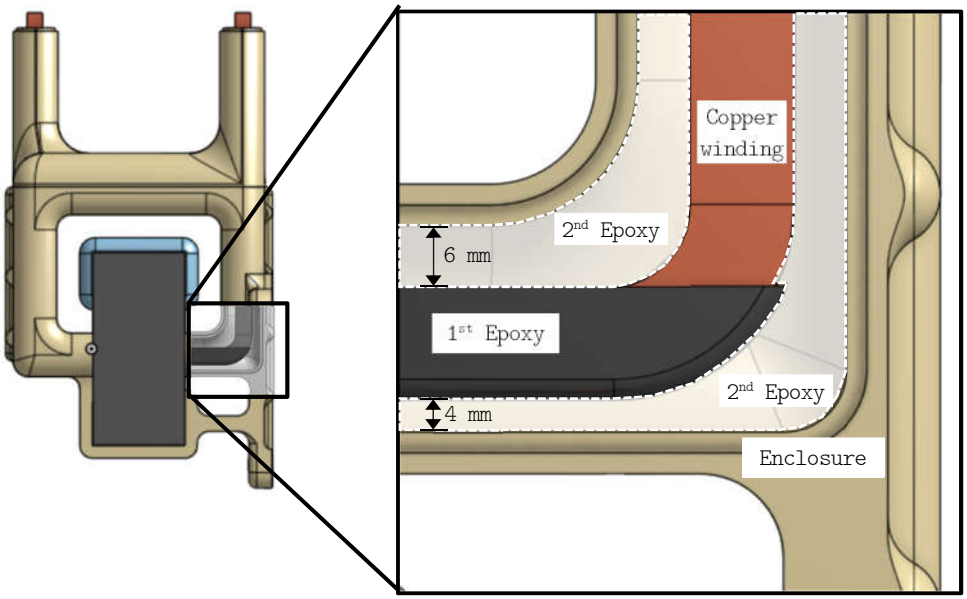


Figure 11-20 Close-up cross section of MV winding after potting

More importantly though, it illustrates that the entire winding (with its first round of epoxy potting) should have enough clearance around all sides to allow a second round of epoxy to flow freely. This close-up also reveals that the weakest point of the isolation, is likely going to be the interface between the first and second round of epoxy potting. Any imperfections on the surface of the first potting (for example the mold release agent of the first "bucket" from Figure 11-18b), might result in isolation defects that can lead to partial discharges. These partial discharges, if they occur, are most likely to happen at that interface.

One interesting problem that impacted the mechanical isolation aspect of the SST module. The DAB transformer was designed with the MV winding being insulated in epoxy for a length that was just over 120 mm from the core. During the potting process however, it was discovered that the epoxy shrinks when potting under vacuum and curing. In the first iteration, the potting shrunk by as much as 50 mm. This required a redesign to lengthen the tubes of the MV winding's terminals to accommodate for this shrinkage. The final

"product" of the DAB transformer is depicted in Figure 11-21 below. Note that isolation sleeves were added to insulate the mechanical interfaces of the DAB transformer's MV winding to its cables. Verification of the insulation is discussed in paragraph *13.1.2 Results MV to LV isolation tests*.

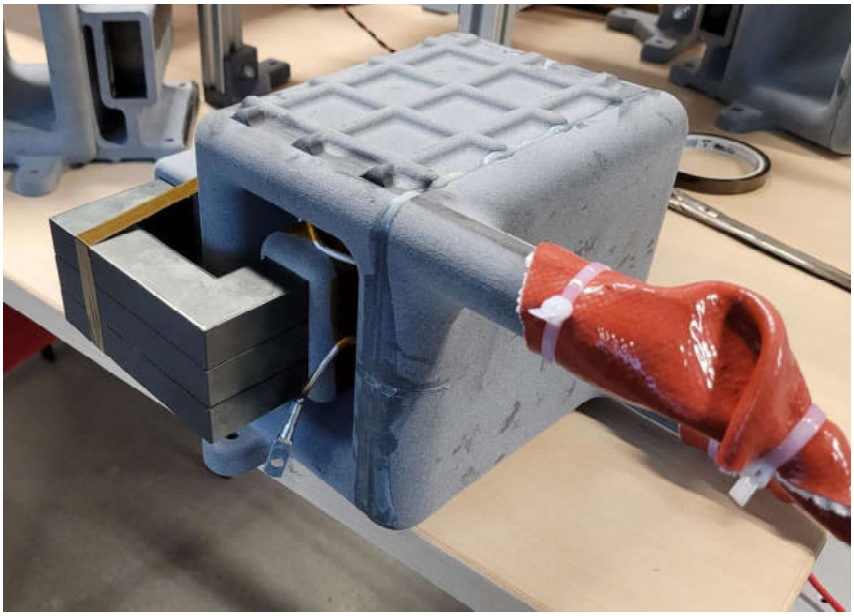


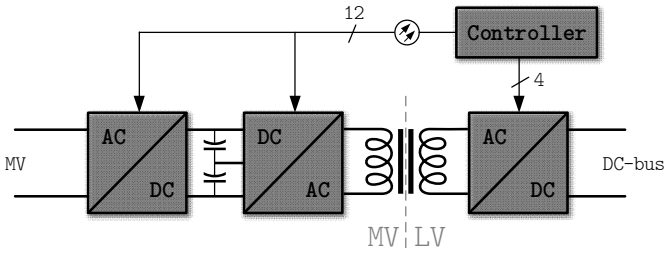
Figure 11-21 The produced DAB transformer

11.2.4.2 Intra-module (internal) fiber optic communication

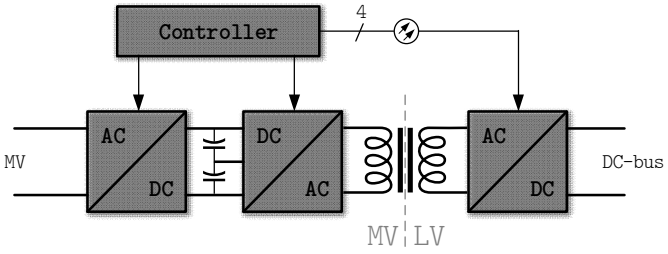
Within the SST module, there is an MV side, and an LV side. These each have electronics, such as driver circuits for switches and sensors for measuring current, voltage, and temperature. The DAB is a power electronics circuit that spans both the MV & LV side and the timing for operating the switches is critical. As such, a single (micro)controller or FPGA should be in control of switches on both sides to ensure this critical timing. This results in the control signals for the switches having to bridge the isolation gap of the SST module, and fiber optics are arguably the easiest way to do this. Especially plastic fiber optics are an affordable solution, and it offers mechanical flexibility for routing a signal (both in circuit board design and in SST module mechanical considerations because of flexible routing). Alternative

configurations with multiple controllers could be devised, but these would then require critical synchronization and would probably still be implemented using plastic fiber optic cables.

With the need for (plastic) fiber optics established, and the choice for a single controller made, the next step is to choose a side for the controller. It can either be placed on the MV side, or on the LV side. With the "other side" controlled via plastic fiber optic cables. The options are shown in Figure 11-22 below.



a. Controller on LV side



B. Controller on MV side

Figure 11-22 Controller on MV or LV side

For the chosen DAB 3L-2L topology, placing the microcontroller on the MV side is logical due to less (fiber optic) connections being necessary. Placing the controller on the LV side would require 12 fiber optic connections for operating the switches on the MV side. By placing the controller on the MV side there are only four fiber optic cables needed to cross the isolation barrier and operate the switches. The only remaining signals are those from the LV sensors. These were all connected to a four-channel / 12-bit ADC chip (Texas Instruments ADS 7950) that has a four-wire SPI communications bus

built in. It is this SPI bus that results in an additional four fiber optics, as well as two additional ones for an enable line and cooling fan PWM control. The final implemented fiber optics connectors in the SST module are shown in Figure 11-23.

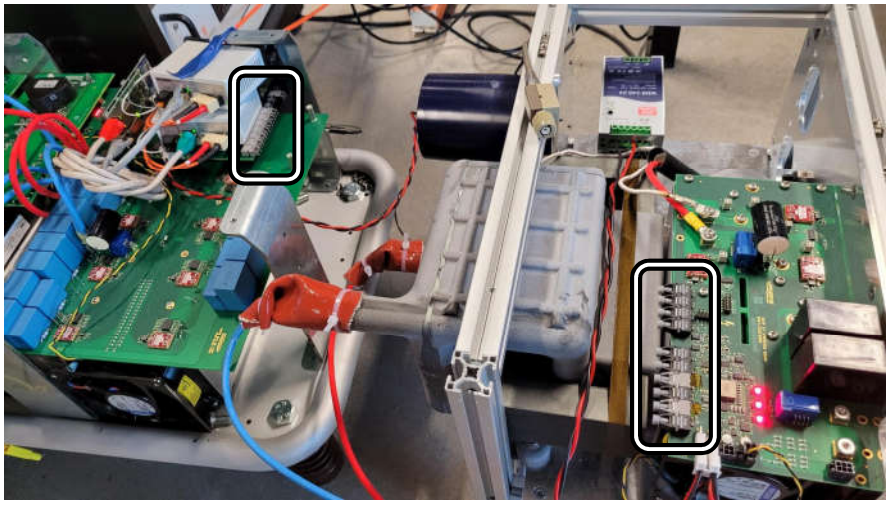


Figure 11-23 Fiber optic connections within the SST module

The communication of signals across the isolation barrier is, however, not only limited to the SST modules themselves. The SST modules also must communicate with the system controller (or perhaps in a future control strategy, amongst themselves). This leads to the inter-module communication, which is discussed in the next paragraph.

11.2.4.3 Inter-module fiber optic communication

To coordinate the power transfer and voltage balancing of the modules with respect to each other, communication with the system controller is necessary. This is achieved, again, using fiber optic cables. These differ from the intra-module fiber optic connection in that they are made of glass and offer a much higher data bandwidth. The system controller is located on the LV side and communicates to each module through an EtherCAT network. This protocol is real-time and is discussed in greater detail in paragraph 11.2.5 SST network architecture.

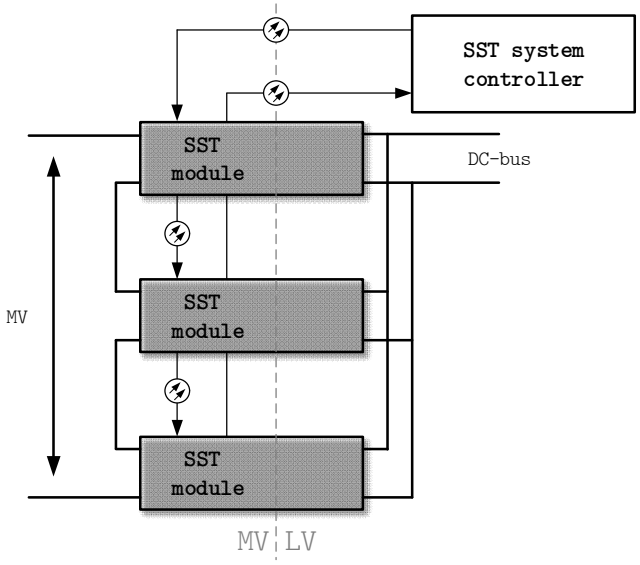


Figure 11-24 Inter-module communication via fiber optics

Because EtherCAT is essentially a type of ring topology, there are two fiber optics connections at each module. One is the EtherCAT input, and the other is the EtherCAT output. It's important to note that it is not possible to "save" on fiber optics connections by having regular network cables on the MV side. This is because each module must be isolated with respect to each other as well. Ignoring this isolation would result in medium voltage levels of stress between the top and bottom module's network ports. These network ports are based on EtherNET and as such do not have the necessary isolation requirements.

The selected fiber is an SC-to-SC Duplex Multi Mode OM2 Fiber Optic Cable from RS PRO. It's 50/125 m and two meters long. The selected media converters are from Beckhoff. These are the CU1521 and take care of the RJ45 EtherNET connection conversion to fiber optic.

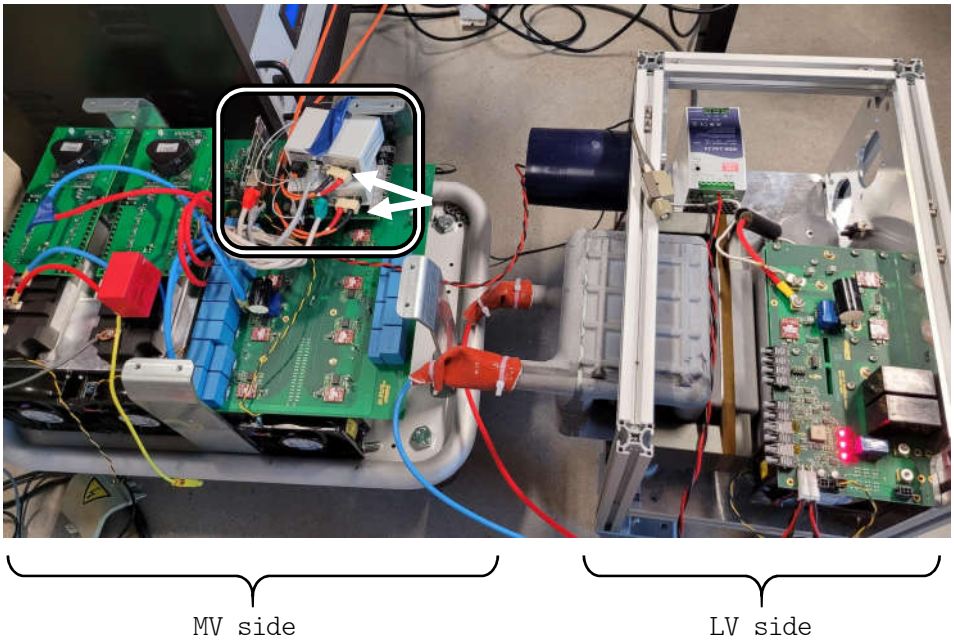


Figure 11-25 Glass fiber optic connections & media converters

In Figure 11-25 above the media converters can be seen in the SST module, the fiber optic connections are marked with the white arrows.

11.2.4.4 Isolated power supplies

With electronics being necessary on the MV side, it is consequentially also necessary to provide these with power. This is a common problem with SST designs, and it has not garnered a lot of attention in literature. Attempts have been made to solve the driver circuit isolation to accommodate a 30kV isolation strategy [41]. Alternatively, in [36] the isolation of powering the SST's MV electronics has been achieved by bypassing the SST entirely using an extra conventional 50Hz transformer.

Figure 11-26 Conventional transformer used for powering MV electronics [36]

In Figure 11-26 above (taken from [36]), the conventional transformer can be seen. The paper describes its purpose is to power the MV electronics. By placing this conventional transformer in parallel, COTS power supply solutions could be used to power the electronics on the MV side.

For this SST project, the choice was made to use an off the shelf solution that does *not* meet the isolation level necessary to withstand the IEC60076-3 AV test voltage. A Siebel SW32 - 24D35U power supply was used to power the MV electronics, it is depicted in Figure 11-27 below [picture was taken from the datasheet].

Figure 11-27 COTS isolated power supply - Siebel SW32-24D35U [datasheet]

It can deliver 80 W of power and offers an isolation level of 32 kV_{PEAK}. It can be seen Figure 11-25 at the top-middle of the image, being the dark cylindrical unit that sits in between the MV & LV sides of the SST module. The 30 kV_{PEAK} is short of the 40 kV_{PEAK} required by the standard. This was, however, the only commercially available solution that could get close to this isolation level.

In the end it was decided to accept the non-compliancy in favor of time and focusing on the other aspects of the SST.

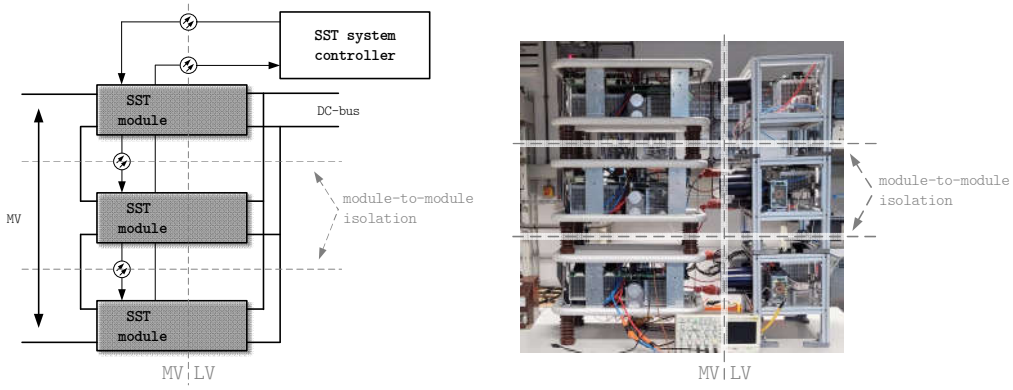
11.2.4.5 Physical isolation of MV & LV mechanical assemblies

The final aspect of the isolation architecture is the physical isolation of the MV & LV sides of the SST modules. The standard states that a minimum distance of 120 mm must be observed between these two sides (see paragraph 10.3 Additional requirements for more information).

The initial design of the SST involved 18 modules and they were going to be designed in such a way that JO 6 - 75 B001 insulators from BINAME ("BINAME" is the name of the manufacturer) would be used to mechanically secure the MV & LV sides together.

Figure 11-28 BINAME JO 6 - 75 B001 insulator (130mm)

These insulators meet the creepage & clearance requirements of the standards. After the descope of the project (see paragraph 8.6), the orientation of the module was changed such, that the insulators would then be used to keep the SST module's MV side physically separated from the floor. Working under the assumption that the floor represents ground.



a. Isolation block diagram

b. Implemented isolation on SST prototype

Figure 11-29 The isolation barriers of the SST

When the modules are stacked, however, these offer much more insulation between the modules than necessary (though, the bottom one that sits on the floor still requires it). This can be seen in Figure 11-29b, where the top two modules are physically separated from each other, at the same distance as the bottom module is separated from the "floor". Using shorter insulators would suffice and result in a significantly more compact SST / increased power density.

11.2.5 SST network architecture

The SST's network architecture is designed to be a **star-topology.** This means that each SST module has a connection to the system controller. The main reason for choosing this topology is the need for redundancy. An SST module faces the MV grid with its CHB. Arguably the most critical failure of the CHB would be exceeding the breakdown limits of the semiconductor. In such an event, the CHB would likely form a short and the MV grid voltage is then presented to the remaining SST modules that have their CHBs still operational. If the sum of the CHB breakdown voltages has been designed with very little over-voltage margin, a failure in one CHB would result in a cascading failure with the next CHB seeing over-voltages as well, and so forth. With the SST power architecture presented in this thesis, the sum of CHB breakdown

voltages exceeds the nominal grid voltage conditions by a factor of two due to the IEC60076-3 IVW & IVPD test condition dimensioning. With this in mind, half of the CHBs could fail before the breakdown limits of the CHBs would cascade out of control. With over-voltage grid conditions being abnormal and rare, one or two CHB failures per phase is acceptable until maintenance / repair since the SST is a factor two over dimensioned to handle the IV & IVW tests of the IEC60076-3. *Voltage-wise* this is not limited to a failure of the CHBs only, any SST module failing could be handled by the other modules by implementing a by-pass mechanism. For example, by bypassing a broken module with a relay that shorts the MV / CHB input of the module. This would then result in approximately 0 V across the broken module's MV / CHB input, requiring a rebalancing of the MV input voltage across the remaining modules. In fact, with that implementation even *two* module failures per phase could be compensated for (again, voltage wise) with other SST modules.

For *power* purposes, a module failure means that the remaining power must be redistributed over the other 17 modules. Since the design is thermally over dimensioned, running the SST at its maximum 200kW power is still possible because the power increase per module becomes 1-17/18 more (around ≈5,5%). More modules failing will result in tripping of overheating protection measures of the SST. Even when applying emergency load shedding techniques as described in [57]. Currently, a possible DSO policy when placing a new transformer in the electricity grid, is to over dimension the power transformer a factor of two for overloading purposes, and another factor of two for futureproofing. If this same policy of large over dimensioning is applied to an SST, then it should never see more than ½x rated power and more modules should be capable of failure without the SST needing to be shut down. With SST cost being so much higher than conventional transformers, as well as a much shorter expected lifetime, this over dimensioned power rating seems unlikely, so only a minimum amount of modules should be allowed to fail, with the total power through the SST never exceeding the maximum rated power of 200kW.

This voltage and power over-dimensioning leads to the selection of the network architecture. After all, if one module is allowed to fail, a ring network is sufficient. This is because any module can still be communicated with "via the other side" when the ring is opened due to a failed module. If more than one module is allowed to fail, (for example, when the power of the SST is well within its maximum power ratings) the star topology is preferred for the network topology.

For the implementation of the research platform SST, however, the star-topology was not feasible due to the system controller's hardware limitations.

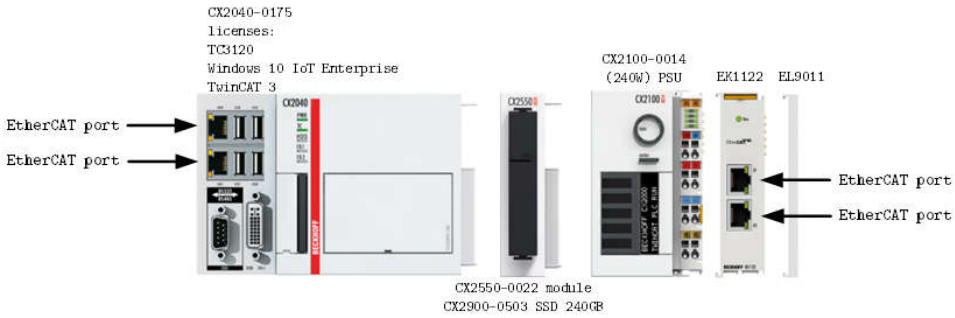


Figure 11-30 System controller hardware

While the system controller has four EtherCAT ports (see Figure 11-30 above), these are considered separate EtherCAT chains from a hardware perspective. The result is that to create the desired star-topology for the network, a separate EtherCAT switch would have to be included. This was not done due to time and budget restrictions.

Ultimately, due to time and budget restrictions, a ring topology has been chosen for the research platform. There is no impact on the functionality due to the research platform only having three modules, and network redundancy experiments would be meaningless.

In Figure 11-31 below, the desired EtherCAT network topology for the total SST is depicted, as well as the final EtherCAT network topology for the research platform.

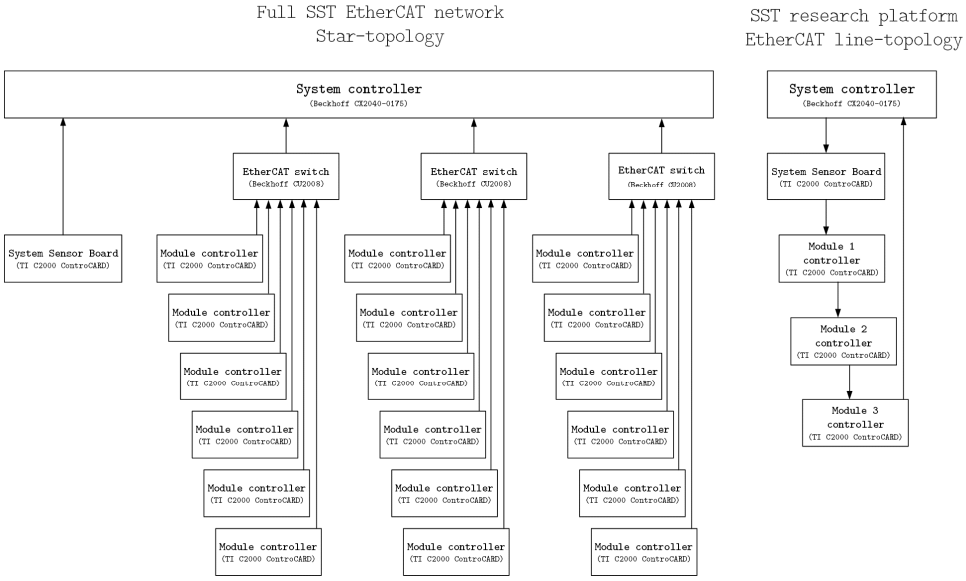


Figure 11-31 The SST EtherCAT network topologies

It should be noted that, while the network connections are depicted with one-directional arrows, the communication is full-duplex capable. For the EtherCAT protocol however, information is sent around in a daisy chain. Even the full SST prototype would send the EtherCAT frame back and forth, looping back to the EtherCAT switch after having "visited" each module. This is due to the fundamental nature of how EtherCAT is implemented by the manufacturer Beckhoff.

The implementation of the network, the sending and receiving of EtherCAT messages was verified on the research prototype using a practical test. The System Sensor Board reads out the ADC, and through a PLL, generates a sinusoidal PWM signal that an SST module can then use to generate its switching outputs. As can be seen in Figure 11-32, three channels are measured. Channel 1 (top / yellow) shows the measured grid voltage at the ADC input of the System

Sensor Board. Channel 2 (middle / blue) shows the MV connections of the CHB at the SST module. Channel 3 (bottom / purple) shows the MV grid current. It is demonstrated that the System Sensor Board generates a synchronized, sinusoidal PWM reference, because the PWM being generated by the SST module's CHB (channel 2), is synchronized with the grid voltage input of the System Sensor Board (channel 1).

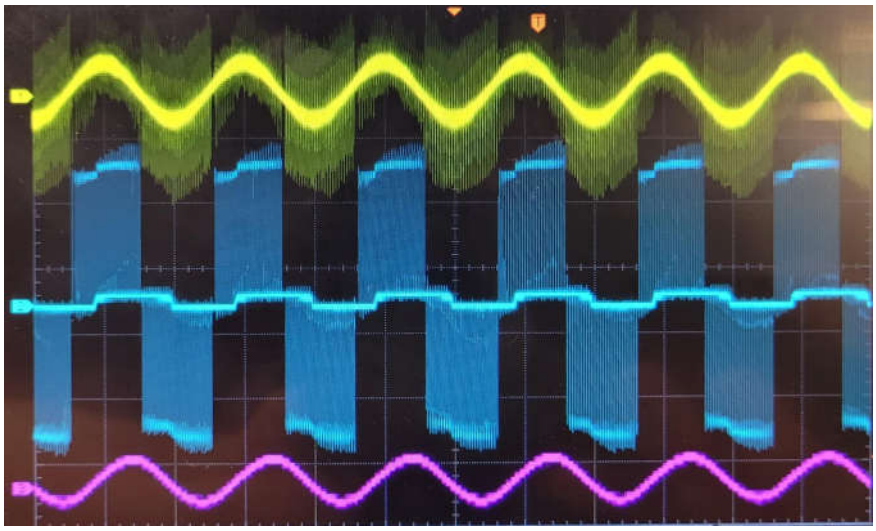


Figure 11-32 CHB PWM generation via network

Network delay

The network delay was measured by generating a reference signal, sending it via the network from the System Sensor board to an SST module. The SST module was programmed such, to receive the message, and then send it back. The signal which was sent back was compared to the sent signal at the System Sensor Board, and the delay was observed using a scope block. The results are displayed in Figure 11-33 below.

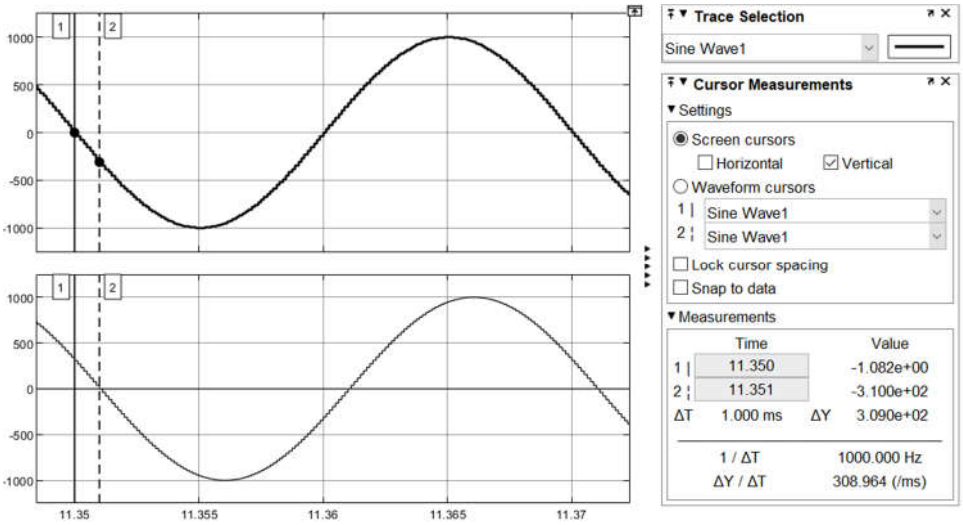


Figure 11-33 Network delay measurement

The measured delay is 1 ms. This is much longer than the anticipated $1/f_{EtherCAT}$ = 1/8000 Hz = 125 us. The explanation for this delay is most likely due to MATLAB Simulink's inability to generate scope plots within models that are both real-time, as well as complex. This is because complex models take too much computation time to complete before the next real-time cycle. As such, rate transition blocks were used for both generating and reading out the signal, which likely results in this high value.

11.3 IEC60076-3 mechanical architecture impact

The IEC60076-3 does not only impact electronics. It also significantly impacts the mechanical architecture as well. The mechanical architecture is affected at both the SST module level, as well as at the system level. An overview of an SST module prototype is shown in Figure 11-34 below.

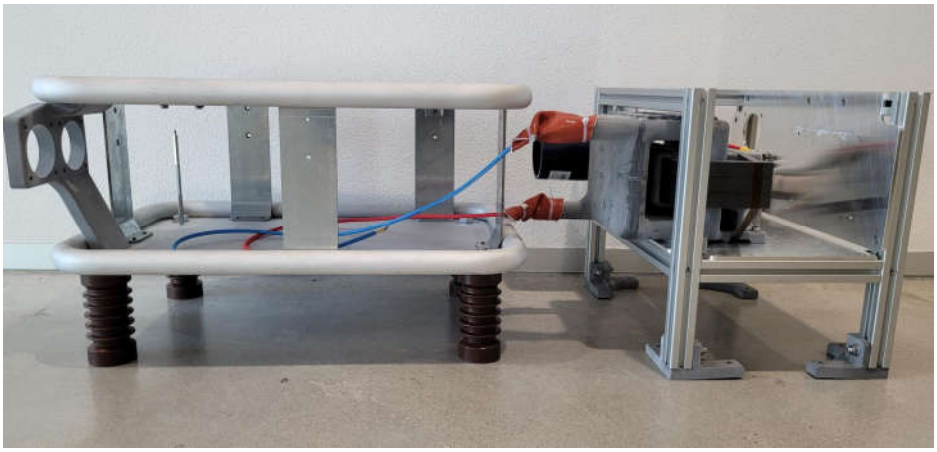


Figure 11-34 Mechanical structure of an SST module

11.3.1 SST module level mechanical impact

The most obvious impact comes from the IEC60076-3's additional requirement of having a physical clearance between the MV & LV sides. For the 10kV prototype, that distance is 120 mm. This can be seen in Figure 11-34 above, with the MV frame depicted on the left, and the LV frame depicted on the right. The DAB transformer, the isolated PSU, and the fiber optic cables (not shown) are the only items that cross this 120 mm physical boundary.

Another aspect that greatly affects the mechanical architecture are the materials used. For the SST module, no conductive parts may cross the MV-LV boundary, meaning that physically connecting the two halves of an SST module would have to be achieved with insulating material. For this module insulator, a COTS component was selected (JO 6 - 75 B001 from BINAME). For the design of the full SST, the physical orientation of the module was envisioned rotated, with the LV frame at the bottom and the MV frame at the top. This original orientation of the SST module is shown in Figure 11-35 below.

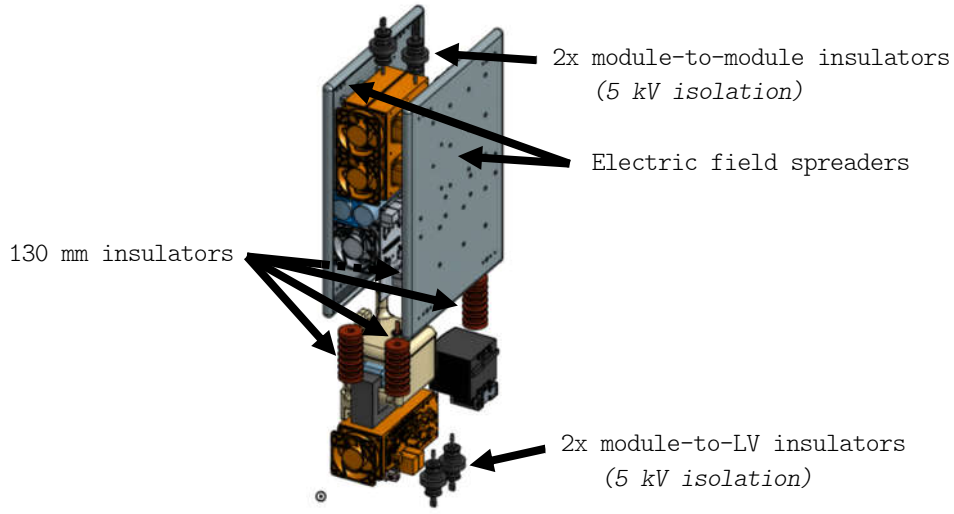


Figure 11-35 Mechanical design of a single module

The BINAME insulators are each 130 mm long and designed for compliancy with the IEC60076-3. These insulators would guarantee the necessary electrical isolation and mechanical strength of the SST modules. With the LV side of the SST module falling in the IEC60076-3 system voltage category of U_m < 1 kV, a 3 kV_{RMS} (or 4,3 kV_{PEAK}) test voltage would be applied during the AV test. For that purpose, the bottom of the LV module was fitted with two 5 kV isolating bushings. To maintain part commonality, these bushings were also reused for the MV module-to-module isolation. With the breakdown voltage of each CHB being determined by 3300 V semiconductor switching devices, the bushings are reasonably over-dimensioned to cope with the maximum module-to-module voltage difference (as in, the CHBs would break down well before the bushings would).

11.3.2 Electric field shaping

While most of this thesis focusses on the isolation between the MV and LV sides of the SST's modules, the SST modules themselves need to be insulated with respect to each other. This was achieved by shaping the electric field between the modules. The level of

module-to-module electric field shaping is determined by the maximum voltage between the modules. With the modules being placed physically next to each other, the maximum voltage between them is determined by the breakdown voltage of the CHB's semiconductor switches within each module. With the selected semiconductor switches having a breakdown voltage of 3300V, the minimum separation in air would have to be at least 1,1 mm (assuming the rule of thumb for the breakdown voltage of air being 30 kV/cm). This is theoretically the closest the modules could be placed next to each other. In practice, however, an SST would be placed in a substation which will likely see atmospheric conditions that will require larger physical distances between modules (e.g. air pollution, higher humidity, etc.). Nevertheless, by having the sides of the SST module fitted with electric field spreaders (see Figure 11-35), sharp edges are avoided, thus allowing the module-to-module distance to be minimized. The radius of the edge of the electric field spreaders is, however, not only driven by the CHB's switch breakdown voltages. Because the MV side of the SST module will also be subjected to the IEC60076-3's AV test. During this test, the MV frame will be subjected to approximately 40 kV_{PEAK} @ 50Hz for one minute, with respect to the LV frame. Requiring the field spreaders of the MV side to be radiused to this higher test voltage. The minimum radius of the edges of these field spreaders are again imposed by the breakdown voltage of air. The worst-case assumption was made by taking the corners of the field spreaders and modeling them as a sphere. In that case, the minimum radius is determined by the following equation.

$$r_{sphere\ min.} > \frac{V_{peak}}{V_{breakdown\ air}}$$

11-2

With the IEC60076-3 AV test voltage being just under 40 kV_{PEAK}, the minimum radius of the field spreader's edges becomes:

$$r_{spreader\ edge\ min.} > \frac{40\ kV_{peak}}{30\ kV} > 1{,}33\ cm$$

11-3

As a safety margin, the radius was rounded up to 1,5 cm. There are more safety margins, as the corners themselves have been given a larger radius, as well as the edges of the field spreader being longitudinal (as opposed to the worst case of them being a sphere). The initial design consisted of a single milled plate of aluminum. An aluminum block with a starting mass of 27 kg, would be milled down to a weight of 5,5 kg. Later, a BSc student redesigned the part using bent tubes that were laser welded to a flat metal sheet. This resulted in a factor 10 (!) cost reduction and a factor 2,5 weight reduction.

11.3.3 SST system level mechanical impact

The mechanical impact is not limited to the SST modules themselves. As a system, the SST is made up of multiple modules and a volume study was performed to see the mechanical impact at the system level. Figure 11-36 below shows this volume study of the full SST.

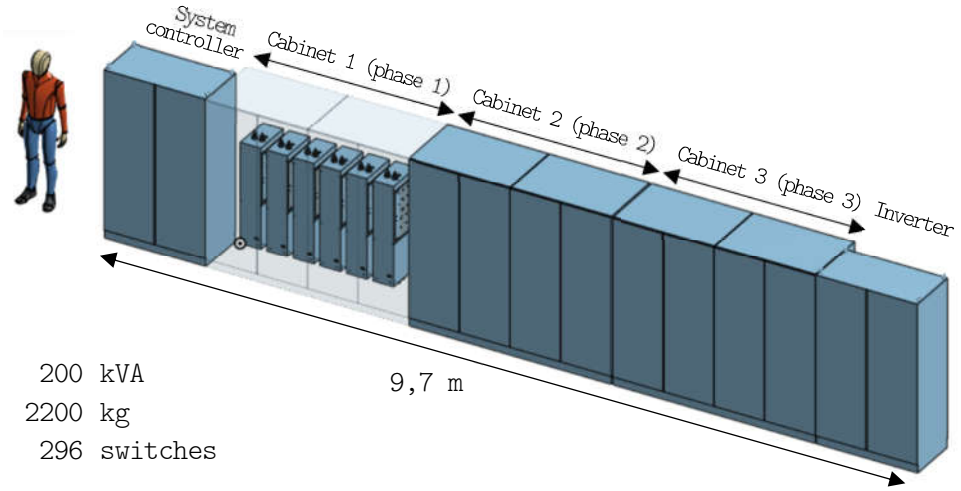


Figure 11-36 Mechanical volume study of full SST

Three COTS (double) cabinets, each housing six modules each, would make up the bulk of the power electronics. An additional cabinet for an inverter would be added, as well as an additional cabinet for the system controller, auxiliary hardware, and the MV grid filter. The full SST was estimated at 9 m long, weighing an estimated 2200 kg.

The main impact on the SST is that at a system level, the SST has many other requirements that are not covered by the IEC60076 family of standards (e.g. IEC61000 for EMC, ISO13849 for safety, etc.). With safety being a concern due to the high voltages involved, the modules would be installed in cabinets which are each connected to earth. Effectively creating a "safety (and) faraday cage" around the SST modules. This final design was descoped (see paragraph 8.6) to a research prototype of three modules.

11.4 SST efficiency

An important aspect of SSTs is their efficiency. There are two aspects to the efficiency of both a conventional transformer and an SST. These are the no-load losses and the load losses. The no-load losses are important because these could be expressed as a monetary loss for the DSO, as these are continuously occurring.

The load losses are of course important because they are dependent on the grid conditions and are limiting the design freedoms due to atmospheric conditions in which a transformer / SST is operated.

11.4.1 SST no-load losses

The no-load losses for each module are taken at 42 W and this was verified via a measurement. For the total no-load losses, a measurement was taken of all the auxiliary power supplies (three powering a module and one powering the system controller & SSB) together, which included the system controller and the system sensor board. These no-load losses were 137 W.

SST element	Consumption [W]	Remark
SST module	30	Cooling fans OFF
SST module	42	Cooling fans ON
System controller	40	Beckhoff CX2040 embedded PC
System Sensor Board	7	

Table 11 No-load losses of SST elements

In the worst case (with the cooling fans turned on, the resulting no-load loss of the full SST results in 18*42 + 40 + 7 = 803 W. With a rated power of 200 kW, the no-load losses represent approximately 0,4%. This is not entirely accurate, as even when no power would be transferred when the SST is in an electricity grid, there would still be switching of the semiconductor switching devices. These switching devices would, however, hardly be conducting any current. Meaning that the no-load switching losses are expected to be very low. A quick evaluation in the Microsoft Excel SST design tool described in paragraph 11.2.3 estimates the no-load switching losses at ≈45 W for the 0% loading case and ≈350 W for a 1% loading case. In practical terms, the no-load switching losses can be said to vary between ≈0,1% and ≈0,2% of the SSTs rated power.

11.4.2 SST load losses & efficiency

The SST's efficiency is estimated by calculating the switching and conduction losses of the switching devices in each SST module

throughout its load profile. These are added to the no-load losses to give the graph depicted below.

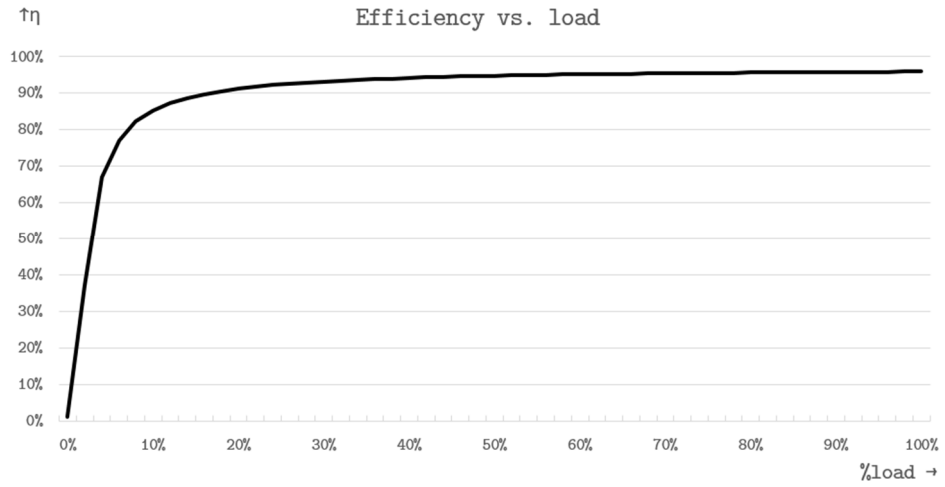


Figure 11-37 Estimated SST efficiency curve

For this efficiency curve the no-load losses, the measurement results were taken. For the SST modules, the load *with* the cooling fans turned on was assumed. It can be observed that the maximum efficiency of the SST is likely to hardly exceed 95%. When comparing this to a conventional transformer, it becomes obvious that SSTs are not competitive efficiency-wise. The figure below shows the approximate efficiency vs. load curve of a conventional transformer. The data was taken from [58] and gaps were approximated through interpolation.

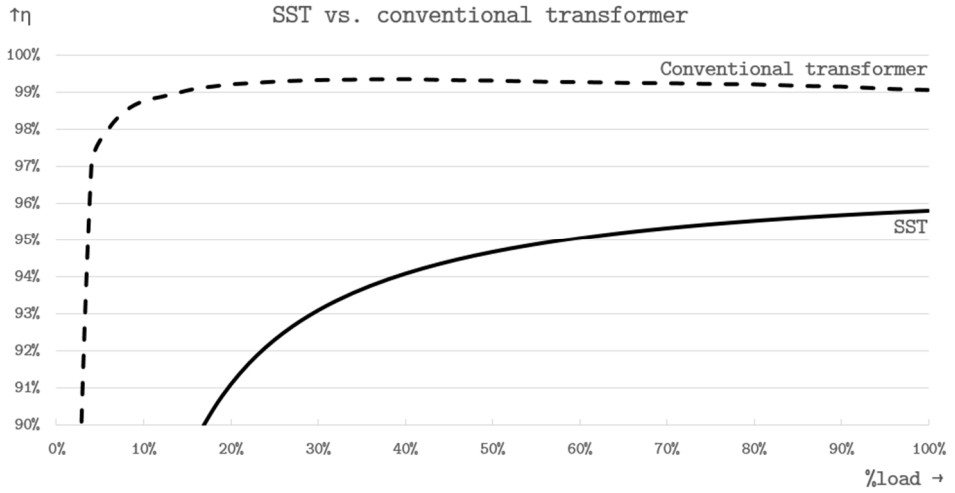


Figure 11-38 SST vs. Conventional transformer efficiency

This is also in line with the average efficiency of distribution transformers throughout Europe, since that efficiency hovers around 98% to 99% [59]. A simplified explanation for the SST's efficiency gap is that conventional transformers enjoy almost a century worth of technological advancement and it is a completely mature technology. A more complex explanation is that SSTs suffer from a lot of "auxiliary electronics" to allow / enable functioning of the main power electronics. While switching devices are becoming very efficient, each switch requires a driver, microcontrollers, power supplies and cooling fans to operate them. These all contribute to a reduced efficiency compared to conventional transformers.

11.5 MV filter

This section will explain the need for having a filter on the MV side of the SST, followed by the different types of filtering solutions. After that, the design of the filter will be described.

11.5.1 The need for a filter

The MV-side of the SST produces a large amount of voltage distortion, and a small (but not insignificant) amount of current distortion. This is due to the nature of the switching converter.

11.5.2 Types of filters

L filter - simply an inductor. Advantage is that its design is simple. Disadvantage is its volume, and level of filtering. The L-filter is, however, the chosen type for this project due to its simplicity.

LC-filter - Consists of an inductor and a capacitor. Essentially it is a compromise between the L- and LCL-filters. It is relatively simple to design and manufacture, as well as reasonable in volume.

LCL filter - Comprised of two inductors and a capacitor. Advantage is that its filtering properties are more favorable and that it will take less volume compared to an L-filter. Disadvantage, much more complex compared to L-filter.

11.5.3 L-filter design

For the purposes of calculating the necessary inductance of the L-filter, it makes sense to use a simplified model of the SST. This filter is based on the three-module research prototype. Displayed below in Figure 11-39 is a block diagram of the SST research prototype and the area marked on the left is investigated for simplification.

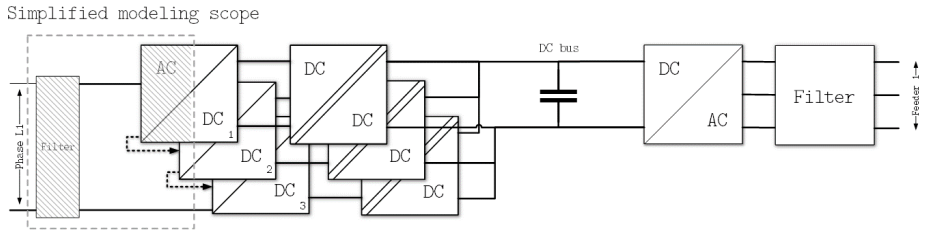


Figure 11-39 Selected SST scope for simplified filter modeling

The simplified model to determine the filter will be based on only a single pair of switches. The complexity of the three modules is then significantly reduced. Figure 11-40 below is the resulting model after the simplification.

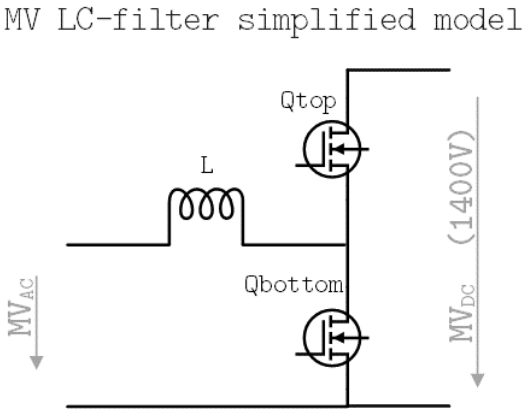


Figure 11-40 The resulting simplified model of the SST converter modules

In this simplified model, the switches present a square-wave switching pattern to the L-filter. It is now possible to start obtaining the relevant parameters to calculate the L value of the filter.

The first parameter is the (effective) switching frequency f_{sw}. To account for the interleaved switching, the switching frequency used for the calculations will be multiplied by three. This is because interleaved switching effectively results in the filter seeing a higher frequency than the base switching frequency of a single module. See the calculation below, and also note an additional factor 2.

$$f_{sw\,eff\,SST} = f_{sw\,module} * n_{modules} * 2 = 1{,}6kHz * 3 * 2 = 9{,}6kHz$$

11-4

The factor 2 in the calculation above is due to the selected switching pattern. Each H-Bridge in the cascade can be switched bipolar or unipolar. Bipolar switching results in a square wave with two switching instances per period. Unipolar switching results in four switching instances per period. The result over a single 50Hz period is 32 switching instances for bipolar and 64 switching instances for unipolar switching. Unipolar switching results in a lower THD [60], and is therefore the chosen switching strategy. A

downside to unipolar switching is that it involves many more switching instances compared to bipolar switching. This could result in more EMI.

The next parameter to be determined is the required maximum ripple current. This is determined by a rule-of-thumb of 10%. To determine the nominal current, the power must be divided by the voltage. The power of the SST is 200kW and is divided over all 18 modules, with 6 modules being in a single converter arm. With the three converter arms connected in wye, and the grid being in delta, the calculation for the nominal current then becomes:

$$I_{RMS\ SST\ converter\ arm} = \frac{P_{SST}\ /\ 3}{V_{MV\ RMS}} = \frac{200kW\ /\ 3}{10.500V/\sqrt{3}} \approx 11A$$

11-5

It is on top of this current that a ripple current will be superimposed due to the converters switching. The maximum ripple, as stated previously should not exceed 10%. Thus, the current ripple amplitude is 1,1A. The ripple current is however always defined in peak-to-peak, to the final ripple current is 2,2A.

With the parameters calculated, it is now possible to determine the inductance of L. This is obtained using the basic inductance formula and rewriting it for L (see calculations 11-6 and 11-7).

$$V_L = L\frac{di}{dt}$$

11-6

$$\Delta i = \frac{V_L}{L} \cdot \Delta t = \frac{\frac{1}{2}V_{MV_{DC}}}{L} \cdot \frac{1}{2} \cdot \frac{1}{f_{sw\ eff\ SST}}$$

11-7

Rewriting for L and filling out the previously obtained parameters, this results in equation 11-8.

$$L = \frac{V_{MV_{DC}}}{4 \cdot f_{sw\,eff\,SST} \cdot \Delta i} = \frac{1400V}{4 \cdot 9{,}6kHz \cdot 2{,}2A} = 16{,}57mH$$

11-8

With the grid filter inductance calculated, it is now possible to design an inductor. To do so, an important aspect must be taken into consideration, and that is the insulation material, as this inductor will be facing the MV grid and its high voltages (and more importantly, the IEC60076-3 test voltage). For the purposes of the prototype, however, an inductor was selected that was already available at the university.

For this purpose, a 50 mH / 10 A inductor (type 195R10 from Hammond manufacturing in Canada) was selected. The inductor is less than ideal for three reasons. The first is the obvious mismatch in inductance, but the second is the core material. This inductor is designed for 50Hz and at higher frequencies it behaves non-linear. These higher frequencies are important because the switching frequency of the CHB is designed at 1,6 kHz which is associated with even higher frequencies due to the square-wave nature of the switching.

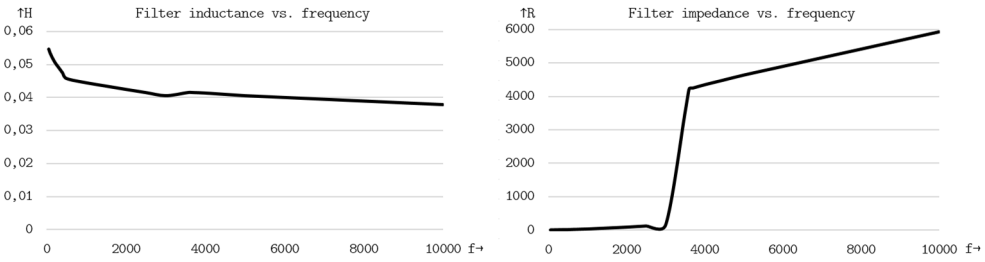


Figure 11-41 MV grid filter non-linearity

This non-linearity was verified using measurements with a programmable LCR bridge, model HM8118 from HAMEG and the results are shown in Figure 11-41.

The last reason why this inductor is not ideal, is because its insulation is made for 230 V_{AC} applications. This will have an impact on the maximum voltage the CHBs can be subjected to.

All these drawbacks were offset by the immediate availability of the inductor, as well as the revised test conditions to which the SST prototype would be subjected to.

11.6 Conclusions - the impact of IEC60076-3

It is safe to conclude that designing an SST that is compliant with IEC60076-3 presents a significant challenge. The first research question posited at the beginning of this chapter was:

5) How does the standard impact SST design?

The answer can be concluded in several aspects. The first is that the IVW & IVPD tests directly impact the amount of SST modules necessary for coping with the test voltage level. The number modules in series is directly correlated to the breakdown voltages of the selected semiconductor switching devices (a higher breakdown voltage results in less CHBs / SST modules in series to cope with the IWV & IVPD test voltages).

The isolation stage of the SST's modules is the DAB, and it is directly impacted by the AV test voltage. Depending on the class of "system voltage" that the SST falls into (in the case of the 10 kV research prototype, this is a 12 kV system voltage class), a significantly higher test voltage is applied between the primary and secondary sides of the SST. This test voltage can be interpreted as being directly applied to the DAB transformer's primary and secondary windings.

It can be concluded that the stated creepage & clearance requirements will require isolated power supplies and the use of fiber optics for any signal transfer between the MV & LV sides.

Additionally, the IEC60076-3 does not only impact the electrical parts of the SST, it also significantly affects the mechanical

construction. Since the mechanical construction is commonly made up of conductive materials, care must be taken with the shapes of the mechanical structures.

6) How is an SST designed to be compliant with the standard?

It is necessary to highlight that designing a full SST requires a team made up of many people, with at least one person for each discipline (power electronics designer, EMC specialist, isolation specialist, mechanics designer, thermal specialist, high voltage specialist, circuit board designer, firmware designer, control specialist). On top of that it is also safe to conclude that some overhead for such a team would be necessary. For this research this discipline gap was covered by talking with a lot of specialists and having master students aiding in the design of various aspects.

In the end, the answer to this research question is effectively a process. That process involves finding all the necessary requirements, which in the case of SSTs come from a large amount of historically established standards. One of those standards is the IEC60076-3, but there are many more, and each discipline will be affected by multiple standards at the same time. An example of this would be the ISO13849 / IEC62061, which are related to safety. Electronics designers would be required to use specific COTS safety-rated electrical components. Mechanical engineers would be required to adhere to specific requirements related to distances and explosions. Software engineers would be required to follow MISRA guidelines for the firmware.

As such, the design of an SST that is ready and compliant for commercial use in an electricity grid, will require a dedicated team of (multi)disciplinary architects, lead designers, etc. to put a focused effort into identifying, evaluating, and applying the necessary standards.

12. Prototype control

This chapter describes the control loops that are implemented in the SST. These are the control loops inside the SST module, as well as the system control loop. With the research questions surrounding SST hardware design answered, the next step is to investigate the following open items

7) **What levels of control are necessary for an SST?**
8) **What impact does the IEC60076-3 have on control loops?**

These research questions are investigated in paragraph 0. It is important to state that there is a difference between the control loops that have been initially designed and the control loops that have actually been implemented. The designed / envisioned control architecture is described in paragraph 0 and describes the control loops only on a high level. This part of the thesis also investigates the impact of the IEC60076-3 on the control architecture of an SST. In paragraph 12.2, the control loops are described that have been implemented on the research prototype and these go into the details of their design.

12.1 Designed control architecture

The control of the SST is envisioned to be of a hybrid control architecture. This means part of the control is distributed over each of the modules, with a system controller that is necessary to balance the modules with respect to each other in terms of voltage and power. To give an overview of all the control loops, the block diagram in Figure 12-2 is shown. The hardware is shown in black (only three modules are shown for simplification purposes), and the control loops are shown in dashed grey.

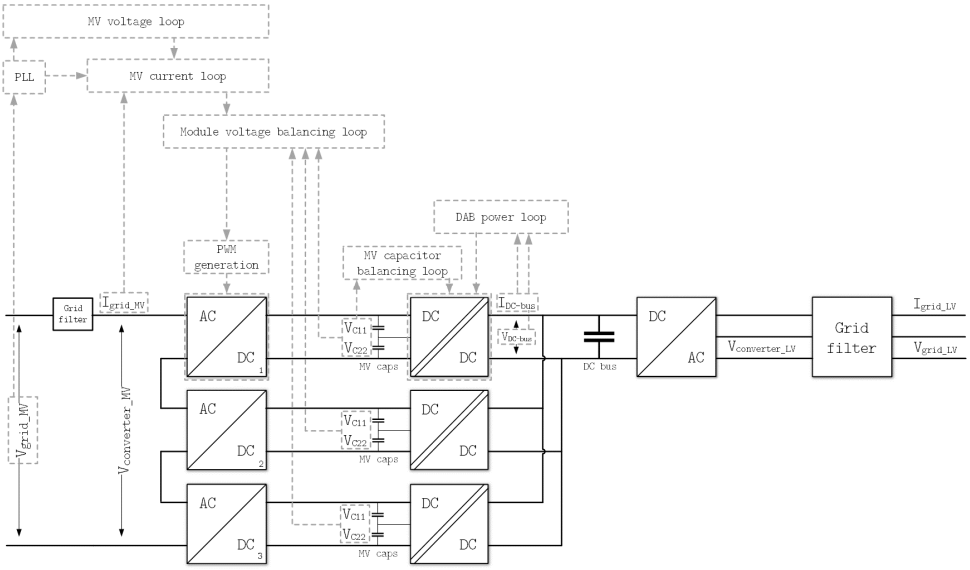


Figure 12-1 The overall block diagram of all the SST's control loops

The system control loops are implemented in the system controller, and they are the:

1. **Module voltage balancing loop**

   The module voltage balancing loop is necessary to ensure the MV capacitors in each of the modules have the same voltage level. A large deviation in voltage level will result in the breakdown voltage limits of one the modules being exceeded, with a catastrophic cascading failure of the module(s) as a result. This control loop is directly affected by the

IEC60076-3 because of the IVW & IVPD tests, where double the input voltage will be applied to the SST's MV side. During this double input voltage, balancing is of course even more critical.

2. **MV voltage loop**
   The MV voltage loop works in conjunction with each module's PWM loop to ensure a sinusoidal voltage is generated, resulting in a sinusoidal current being drawn from the grid, as well as each module generating a voltage that is $1/n^{th}$ of the MV grid voltage (with n being the number of modules in a phase). This control loop is similarly affected by the IEC60076-3 IVW & IVPD tests as the first control loop.

The module control loops are implemented within the modules themselves. These modules control loops are:

3. **MV current loop**
   The MV current loop is there to ensure a PWM voltage is generated such, that it results in a sinusoidal current being drawn from the MV grid. This means this loop results in each module (approximately) generating a sinusoidal voltage $1/n^{th}$ of the MV grid voltage (with n being the number of modules in a phase). This control loop is not directly impacted by the IEC60076-3 standard. It is, however, important from a power quality perspective. Drawing a sinusoidal current without any / minimal harmonic distortion is necessary for achieving a high(er) power quality.
4. **MV capacitor balancing loop**
   Each module has a set of capacitors of which the mid-point serves as that module's neutral point. All the module's electronics are referenced from this neutral point, including the MV DAB switches. If the voltage across the capacitors is not the same, a voltage imbalance occurs. It is in fact unlikely that the voltages will always be identical due to slight mismatches in components (from production), such as capacitor values, microcontroller

timings, cable impedances, etc. A large voltage imbalance will destroy the (400 V) DC-blocking capacitors of the DAB transformer, followed by the MOSFET switches (1700 V).
This voltage imbalance can also cause efficiency problems in the DAB (ZVS may no longer be guaranteed). As such, this balance needs to be actively controlled. This control loop is directly impacted by the IEC60076-3 IVW & IVPD tests in the same way as the first two system controllers are. The capacitors have a maximum voltage rating of 2 kV each and a significant deviation of the DAB's mid / neutral point could result in exceeding this maximum rating. The balancing is most critical during the testing because then each module will have a combined capacitor voltage of 3+ kV, well beyond the limits of a single capacitor.

5. **DAB power loop**
   The DAB power loop controls the power flow through the DAB to control the voltage of the LV DC-bus to a specific level. This loop is similarly affected by the IEC60076-3 IVW & IVPD tests as a large deviation will cause module unbalance. There is, however, also an impact on the DAB power loop that is caused by the AV test. This is because the AV test is effectively an isolation test of the DAB transformer (this is a simplification, because geometry, creepage, and clearance are also heavily affected by the AV test), the DAB transformer's design will involve large creepage & clearance distances, as well as the avoidance of Litz wire. Resulting in a transformer that sees design impact on its leakage inductance. This leakage inductance is one of the key design parameters that greatly affects the control loop of the DAB.

It is safe to conclude that the IEC60076-3 IVW & IVPD tests are highly influential on the control loops of an SST. The third IEC60076-3 test covered in this thesis, the AV test, also affects one of the control loops, but overall, to a much lesser degree than the IVW & IVPD tests.

12.2 Implemented control architecture

The implemented control architecture of the SST also sees its control distributed over all the modules, with a system controller governing the voltages & currents at the SST's extremities. An overview of the implemented control loops is shown in the block diagram (Figure 12-2).

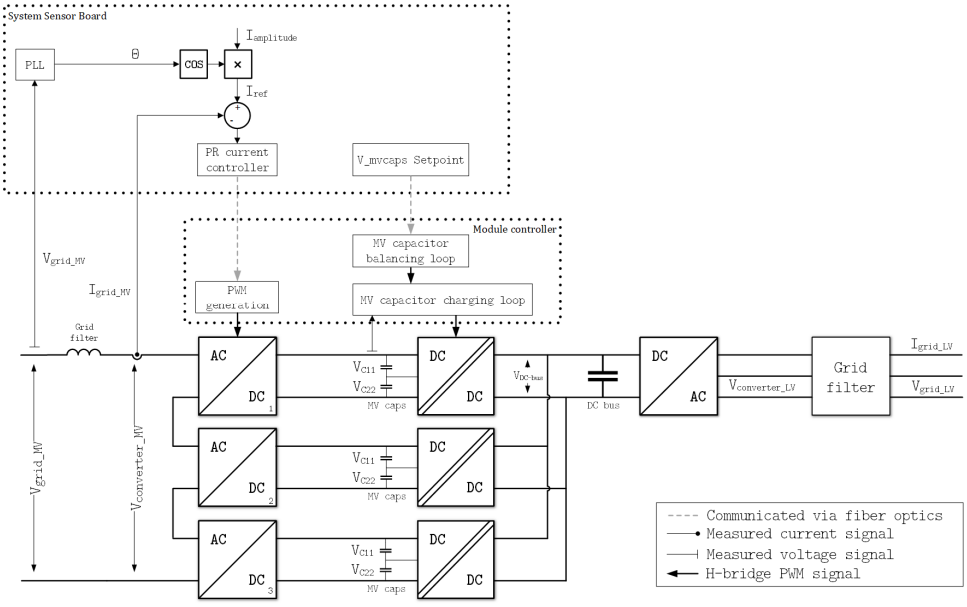


Figure 12-2 The overall block diagram of all SST prototype control loops

The hardware is again shown in black, and the control loops are shown in dashed grey. There are two control "loops" implemented in the system controller, and these are listed below (one is the PLL, the other is a control loop). Please note the paragraph number in which these control loops are described in further detail.

1. **PLL (§ 12.3.1)**
   The PLL is implemented in the system controller and is there to provide a stable grid reference for the MV current loop.
2. **MV voltage loop (§ 12.3.2)**
   The MV voltage loop is there to ensure a voltage is generated that results in a sinusoidal current being drawn from the

MV grid and also to ensure each module generates a sinusoidal voltage $1/n^{th}$ of the MV grid voltage (with n being the number of modules in a phase).

The module control loops are implemented within the modules themselves. These modules control loops are listed below. Please note the paragraph number in which these control loops are described in further detail.

3. **MV capacitor charging loop (§ 12.4.1)**
   This loop uses phase shifting of the DAB to control the power flow through the DAB in such a way that the MV capacitors are charged to a specific voltage level. The voltage level is set by the system controller.
4. **MV capacitor balancing loop (§ 12.4.2)**
   Each module has a set of capacitors of which the mid-point serves as that module's neutral point. All the module's electronics are referenced from this neutral point, including the MV DAB switches. If the voltage across the capacitors is not the same, a voltage imbalance occurs. A large voltage imbalance will destroy the (400 V) DC-blocking capacitors of the DAB transformer, followed by the MOSFET switches (1700 V).
   This voltage imbalance can also cause efficiency problems in the DAB (ZVS may no longer be guaranteed). As such, this balance needs to be actively controlled

There is room to grow for the control loops in both the System Sensor Board and the module controllers. Logical candidates are a module-to-module balancing loop that takes the values of the MV capacitors from each module and balances them with respect to each other. This implementation should be relatively straightforward as the voltages of the MV capacitors are already available via the network.

12.3 System control loops

12.3.1 Phase-Locked Loop

The first part of the system level control is the Phase-Locked Loop (PLL). The PLL is the basis of a stable loop control for both the voltage and current. A PLL is used to accurately detect the phase angle of the fundamental frequency (50Hz in the Dutch electricity grid) of the MV grid voltage. This accurately detected phase angle can then be used to generate an accurate current reference to synchronize with the MV grid voltage. The electricity grid is inherently "polluted" with harmonic distortion. This harmonic distortion affects the performance of an active rectifier (the CHB is an active rectifier that distributes the voltage across its modules). A PLL also functions as a filter for harmonic distortion for the control signals and it is a crucial element in the control of grid-interfacing power electronics.

12.3.1.1 Single-phase PLL model

The block diagram of the proposed single-phase PLL model is shown in Figure 12-3. In a three-phase PLL, there are two voltage references given in the form of V_α and V_β. These are obtained through a mathematical transformation (see later in this paragraph for further explanation). For a single-phase PLL, the V_β is artificially synthesized from V_d.

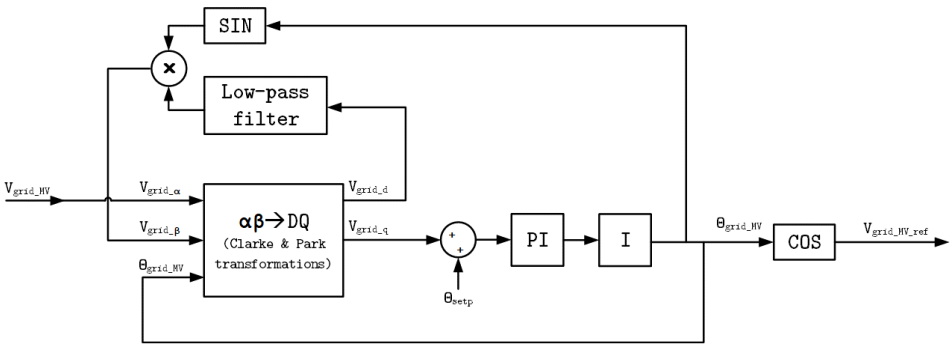


Figure 12-3 PLL block diagram

There are several ways to implement a PLL. Traditionally, with PLLs having their origins in electronics engineering, a phase detector was used, followed by a low-pass filter and a Voltage Controlled Oscillator (VCO) [61]. Even in modern day simulations, that behavior is replicated (e.g., the *Mixed Signal Blockset* of MATLAB Simulink). When working with microcontrollers however, the flexibility of implementing a PLL in software can be achieved more elegantly through a more mathematical approach. By using the Clarke & Park transformations, the rotating grid voltage U_{ABC}, can be represented using a rotating reference frame U_{DQ}. Figure 12-4 illustrates these transformations for a three-phase system. The transformation for a single-phase system is similar and will be discussed later in this paragraph.

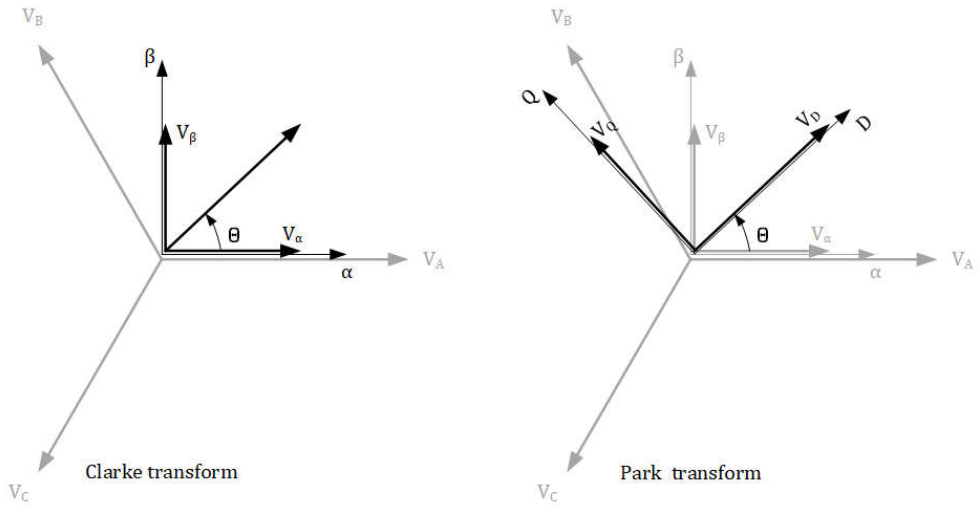


Figure 12-4 Three-phase Clarke & Park transformations for the PLL

The Clarke transformation converts the V_{ABC} to a rotating reference frame called $V_{\alpha\beta\gamma}$. This frame has two axes, called α and β and the voltages are re-projected onto these axes. After the Clarke transformation, a second transformation is performed called the Park transformation. The Park transformation takes this *stationary* reference frame and converts it to a *rotating* reference frame. This results in a two-axis system (D & Q axes) that is rotating

counterclockwise at a continuously increasing angle θ. When this increasing angle is increasing at a rate of 2π50 radians per second (or 50 rotations per second), the DQ frame is synchronized to the grid (assuming the grid frequency is exactly 50Hz).

For a single-phase system, the mathematical transformations are the same, with one difference, V_β is not generated from only having V_A (a single phase). While V_A results directly in V_α, V_β must be obtained taking the sine of V_d with θ. Mathematically, this counter-intuitive because the transformation must first be applied, before V_β can be obtained, which is in itself needed to apply the transformation. In practice, this is not an issue as V_d is rotated with respect to V_β by an amount of sine θ.

The main advantage that comes from using these transformations, is that the control loop for the (re)creation of the grid voltage reference is a "DC" value, instead of a continuously varying sinusoidal value. This is because when implementing a controller (e.g., a PI controller), that controller has a rotating viewpoint. In other words, the controller only needs to control a single, positive value that hovers around the 2π50 mark. Figure 12-5 illustrates two different controllers. Depicted on the left, a conventional controller is continuously lagging the grid voltage input due to its control delay. Even the fastest microcontroller that is commercially available will lag the input. With the Clarke and Park transformations, the controller only needs to control the "DC" value of θ.

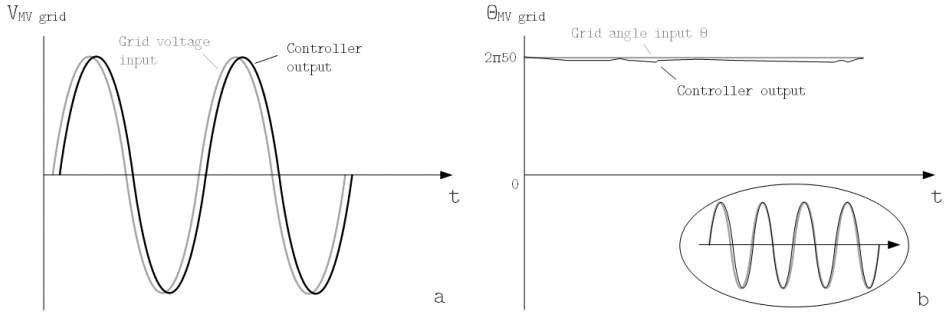


Figure 12-5 a) "Sinusoidal PLL controller". b) "DQ PLL controller".

In Figure 12-5b, the response of a PLL based on a DQ controller can be observed. The angle theta will vary only slightly due to system variances and the resulting effects in the time domain are shown in the bottom-right side of Figure 12-5b.

12.3.1.2 PLL implementation and parameter design

The PLL has been implemented in MATLAB Simulink. The final implementation is depicted below in Figure 12-6 and closely matches the model from paragraph 12.3.1.1.

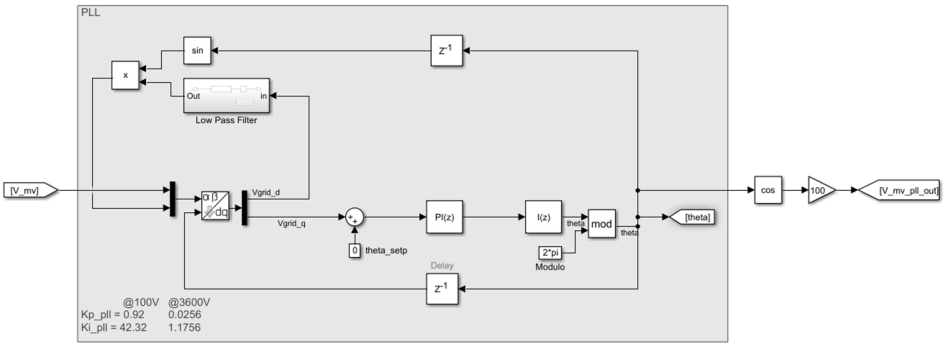


Figure 12-6 PLL implementation in Simulink

The key blocks of this implementation are listed and discussed below.

1) **αβ-to-DQ block**
   This block performs the Clarke and Park transforms on the sinusoidal MV grid input. With V_α being the grid voltage, and V_β being the reprojection V_d (which is necessary because the transformations require two vectors).
2) **Discrete PI controller and integrator blocks**
   It is important to note that a PI controller alone is not sufficient, and two components are necessary. The PI controller, and an additional integrator. The PI controller's function is to track the setpoint value of theta (Θ). The nominal value of the angular frequency (theta) is around 314 (2π50) radians per second. The PI controller outputs a constant value that needs to be "translated" into a continuously increasing angle Θ. The integrator block does exactly this, its function is to form a ramp from a constant input.
   When observing the loop gain, three components can be observed. The first two are the P and I of the PI controller, and the third component is the extra integrator. The loop-gain of the PLL in the S-domain is described in equation 12-1.

$$G_{C-s} = \left(K_{p\_PLL} + K_{i\_PLL}\frac{1}{s}\right) \cdot \frac{1}{s}$$

12-1

   With K_{p_PLL} representing proportional gain, K_{i_PLL}*1/s representing integral gain, and finally 1/s representing the additional integrator.
   The values for K_{p_PLL} and K_{i_PLL} are determined using formulas 12-2 and 12-3.

$$K_{p\_PLL} = 9{,}2 \cdot \frac{1}{t_{settle}} \cdot \frac{1}{V_{d0}}$$

12-2

$$K_{i\_PLL} = 4{,}6 \cdot K_{p\_PLL} \cdot \frac{1}{t_{settle}}$$

12-3

With a settling time t_{settle} of 0.1 seconds and V_{d0} of 3600V (1200V per module for normal operation), the resulting K_{p_PLL} and K_{i_PLL} become 0.0256 and 1.1756 respectively.

The controller's stability is investigated with the help of a bode plot.

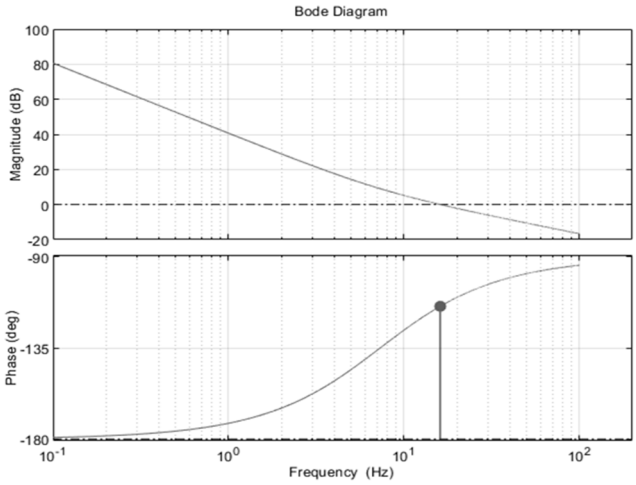


Figure 12-7 PI controller bode plot for PLL

As can be observed in the bode plot, the cross-over frequency is around 10Hz. This means good stability at a 0.1 second settling time.

3) Low-pass Filter (LPF) subsystem

The LPF subsystem is made up of a filter that can be described in the S-domain in the form of a transfer function. Its base form is shown in equation 12-4.

$$G_{LPF-s} = \frac{\omega_{LPF}}{S + \omega_{LPF}}$$

12-4

Where ω_{LPF} represents the corner frequency of the filter. This transfer function is not suitable for direct implementation into a microcontroller, and it needs to be transformed into a discrete format (the Z-domain). The transfer function is discretized through MATLAB's c2d function. The resulting transfer function in the discrete form is shown in equation $G_{LPF-d} = \frac{1+z^{-1}}{1-z^{-1}}$ 12-5.

$$G_{LPF-d} = \frac{1 + z^{-1}}{1 - z^{-1}}$$

12-5

ω_{LPF} is dimensioned at 1Hz. This is because the frequency limit of this filter is designed to be 10 times lower than the bandwidth of the PLL's PI controller. With the PLL's PI controller having a bandwidth of around 10Hz, the filter is dimensioned to 1Hz.

Using MATLAB's c2d function to discretize the S-domain transfer function, the resulting G_{LPF-d} becomes equation 12-6. Note that a sample time of 1/2000. This sample time is derived from the sample rate of the System Sensor Board's ADC. For the testing it was set to 2kHz, but it should be noted that ideally this sampling rate should be equal to the EtherCAT network update rate (normally 8kHz in industrial applications). This is because the firmware of the TI C2000 microcontrollers used in the SSB, and SST modules operates interrupt based. These interrupts are generated upon receiving an EtherCAT message, thus allowing for deterministic operation of the SST.

For the c2d discretization, a trapezoid "Tustin" transformation was used to obtain the equation below.

$$G_{LPF-s} = \frac{0.001568z^{-1} + 0.001568}{z^{-1} - 0.9969}$$

12-6

12.3.1.3 PLL verification

For testing purposes, a low voltage was used to verify the PLL model. At 100V, the resulting K_{p_PLL} and K_{i_PLL} from equations 12-2 & 12-3 become 0.92 and 42.32 respectively. Applying a voltage with a frequency of 50Hz, and peak of 100V, the tracking performance was observed using a scope in MATLAB Simulink.

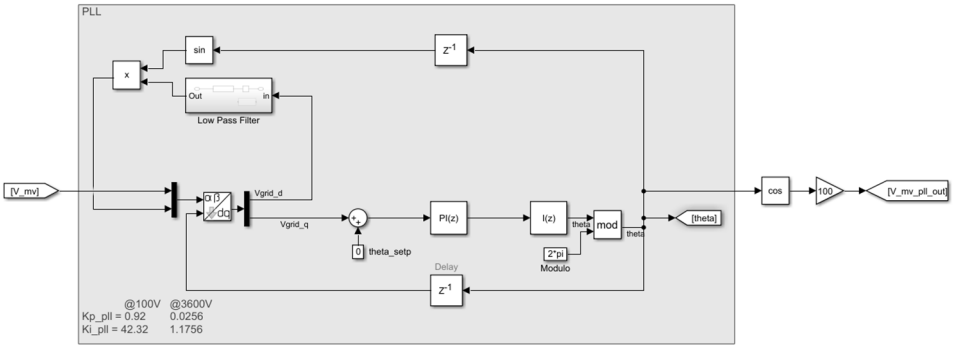


Figure 12-8 PLL behavior test model

Figure 12-8 shows the tested model. V_mv is directly connected to an ADC onboard the TI C2000 microcontroller. The output theta is converted to a cosine and amplified to match the input voltage. This amplification is to scale the output to a comparative level of V_mv (a cosine only varies between 0 and 1).

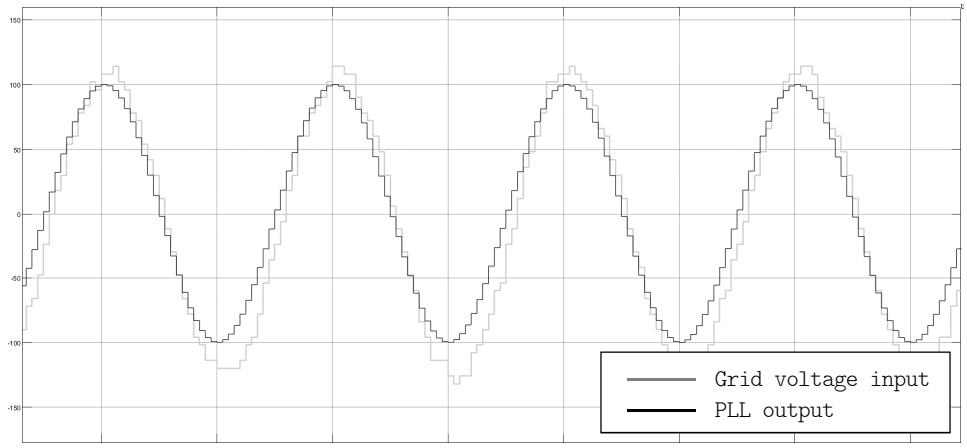


Figure 12-9 PLL behavior test result

As can be seen from Figure 12-9, the tracking performance of the PLL is corresponding to the design.

12.3.2 System MV current loop

There are several choices of controllers for controlling the current that the SST draws on the MV side. Ideally, the SST should always draw a sinusoidal current that does not exhibit any harmonic distortion. While this is not possible from a technical perspective, (for example due to inaccuracies in components, control loops, controller timings, network jitter, etc.) the goal is to get as close as possible.

To achieve a low harmonic distortion, a PIR controller (Proportional Integral Resonant controller) was implemented. This controller has a high gain around the fundamental harmonic (50Hz) and low gain outside of the fundamental harmonic because of its resonant part. Combined with working in the DQ-frame for a future voltage controller, the PIR controller will complement the overall control with eliminating steady state error and suppressing higher harmonic influences that may be present in the MV grid [62].

Design of the PIR controller's response has been achieved using MATLAB's scripting editor, with particular attention being paid to the delays in the system. A typical value for the delay of a

controller is half of the switching period. This is because in a typical control situation, the controller will be able to correct on the next switching instance. For the SST prototype, an additional set of delays must be considered, and these are due to the EtherCAT network delays. Ultimately, an attempt was made to measure the network delay by sending a sinusoidal signal from the System Sensor Board to a module, followed by that module simply sending that value back over the EtherCAT network to the System Sensor Board. This turned out to be 1 ms, which is significantly more than the update rate of the EtherCAT network that runs at 8 kHz (125 us). This is likely incorrect, as MATLAB Simulink only allowed the signal transfer via "rate-change" blocks. These no longer guarantee the timings and as such, the 1 ms network delay has been discarded. The final delay in the system has been modeled according to equation 12-7.

$$T_{delay} = \left(0.5 \cdot T_{switching}\right) + T_{sampling} + T_{network\ delay}$$

12-7

Where:

- T_{delay} is the total delay experienced by the controller
- $T_{switching}$ is the switching period of the CHB (1/1600 Hz = 625 us)
- $T_{sampling}$ the sampling frequency of the controller (equal to EtherCAT network frequency 1/8000 Hz = 125 us)
- $T_{network\ delay}$ being the signal delay between the controller sending a message and the module receiving it (measured at 25 us).

This results in a total delay of ≈463 us. MATLAB was then used to determine values for K_P with a phase margin of 45 degrees and at $\omega_{cross\text{-}over}/L_{grid}$ (the cross-over frequency over the grid inductance). K_I, and K_R is dimensioned at K_P / 20 and K_I another factor two below that. The resulting values for the controller were K_P =113, K_I = 2.5633e+04, and K_R = 7.2094e+03. The PIR controller's response was then investigated with the help of a bode plot.

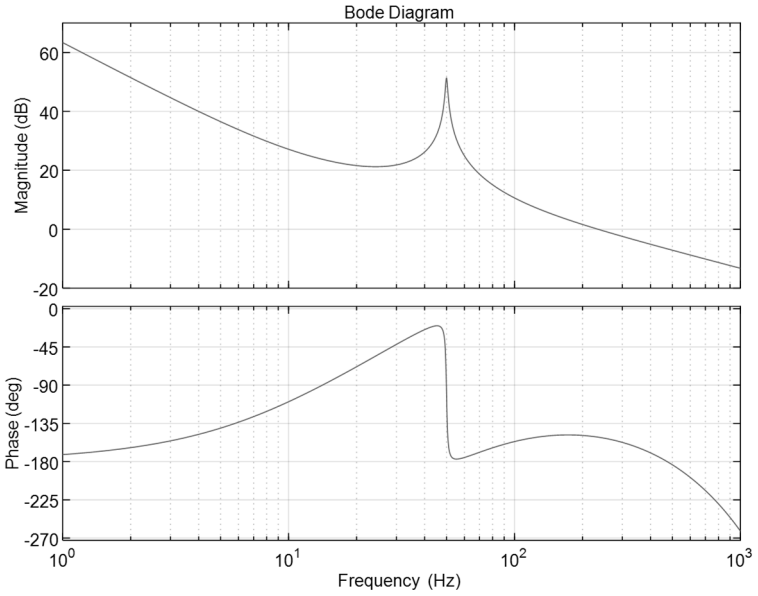


Figure 12-10 PR controller frequency response.

12.3.2.1 System MV current loop verification

To verify the response of the PR current controller, two modules have been connected in series with their MV input sides of their CHBs short circuited via a 50 mH inductor. In Figure 12-11 below, a diagram of the test setup is depicted.

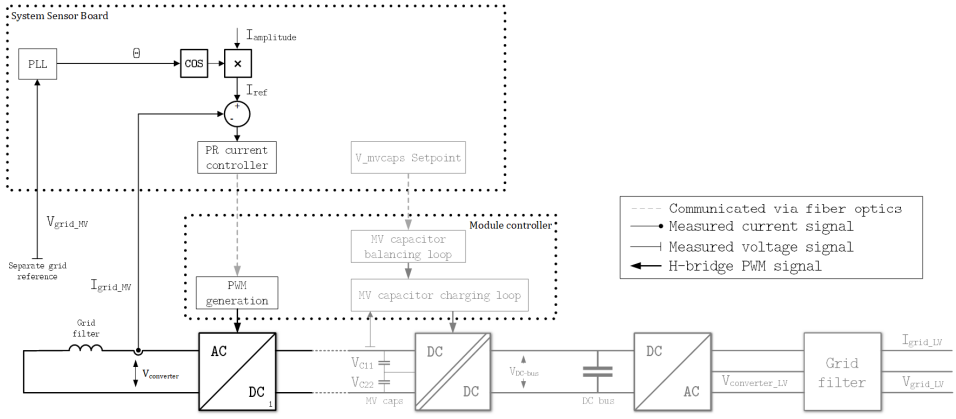


Figure 12-11 The test setup for verification of the PR controller

It is important to note that the CHB was connected separately via an external power supply. The rest of the SST module was not used for the verification measurement. The test was executed successfully with a current amplitude of 0,5 A. As can be observed in Figure 12-12 below.

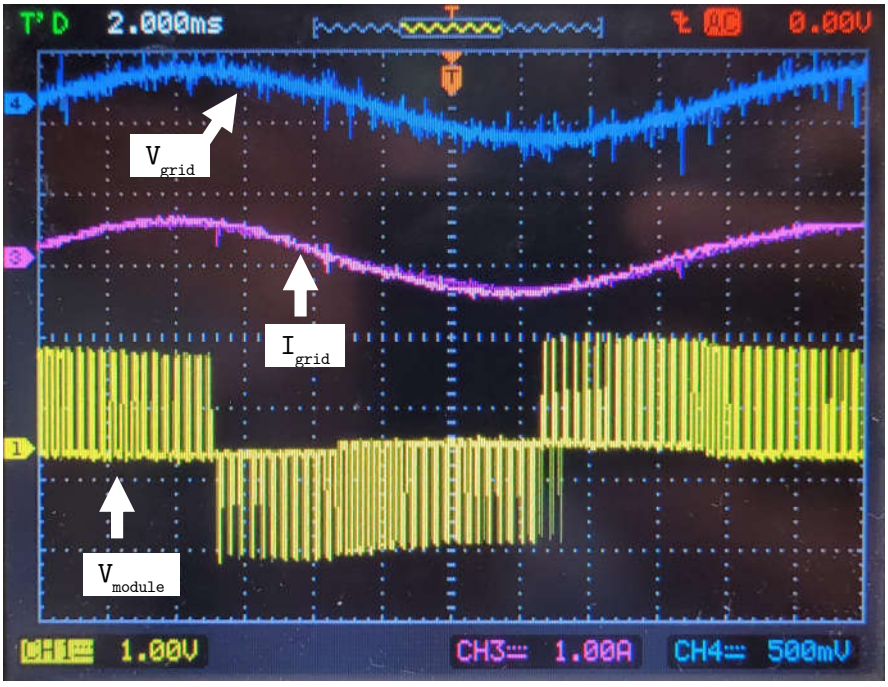


Figure 12-12 MV current loop test results

As can be observed, the generated "grid" current through the inductor is perfectly in phase with the grid voltage. This demonstrates once more the performance of the PLL as well.

12.4 Module control loops

12.4.1 MV capacitor charging loop

The MV capacitor charging loop is for the purposes of this research set up as controlling the MV capacitor voltage level by transferring power from LV to MV. The MV capacitor loop would in the future be operated to charge them via the MV side, but with the laboratory's main power supply breaking down in the final stages of testing, the approach is changed to charging from LV instead. The fundamental operation of the DAB in this particular case is chosen as phase-shifting the two bridges with respect to each other. There are other possible implementations that vary pulse widths and other parameters, but for demonstrating power flow through the SST modules, a phase-shifting control is selected.

12.4.1.1 The DAB model

To design the controller, the DAB must be modeled. For this purposes, an effective model of the DAB is taken from [63]. This model is also operated by phase-shifting the primary and secondary bridges with respect to each other. There are several aspects in which the SST prototype differs from this model. The biggest one is the fact that [63] models the DAB as a 2L-2L, whereas the SST prototype is implemented as a 3L-2L. This deviation can be accommodated for by having the switching times of the three-level side in such a way that it closely resembles a square wave. This approach does not negate the advantages of the 3L-2L implementation, as the rationales that are set forth towards the end of paragraph 11.2.3 still hold.

The model is made up of two parts. The first is the relation of the phase shift Φ (phi) with respect to the DAB's elements is described in equation 12-8 below (taken from [63]).

$$\varphi = \frac{1}{4} - \sqrt{\frac{1}{16} - \frac{f_{sw} \cdot L \cdot I_2}{2 \cdot N \cdot V_1}}$$

12-8 Taken from [63]

Where f_{sw} is the switching frequency, L the DAB transformer's leakage inductance, I_2 the current on the secondary side, N the turns-ratio of the DAB transformer, and V_1 the voltage on the primary side. It is important to note that the DAB's phase shifting power transfer is determined by the leakage inductance L of the DAB transformer [64].

The second aspect of the model is defining the gain of the plant G_P. This is also taken from [63] and shown in equation 12-9 below.

$$G_P = \frac{\hat{v}_2}{\hat{\varphi}} = \frac{N \cdot V_1 \cdot (1 - 4 \cdot \varphi)}{f_{sw} \cdot L} \cdot \frac{R_L}{R_L \cdot C_2 \cdot s + 1}$$

12-9 Taken from [63]

This model was then modified to represent the SST prototype more closely. The main difference is the absence of load resistor R_L. In the case of the SST prototype, this resistor is not there as the "load" is directly represented by the current. This leads to equation 12-10 for G_P below.

$$G_P = \frac{\hat{v}_2}{\hat{\varphi}} = \frac{N \cdot V_1 \cdot (1 - 4 \cdot \varphi)}{f_{sw} \cdot L} \cdot \frac{1}{C_2 \cdot s}$$

12-10

With the model for the DAB established, the next step is to design the controller.

12.4.1.2 The controller design

The first parameter necessary for designing the controller is the cross-over frequency. The DAB is designed to operate at a switching frequency of around 20 kHz. The number is not exact because depending on the implementation, the DAB frequency would have to be multiples of the CHB due to firmware implementation restrictions. These restrictions occur because all SST modules require synchronization, which occurs every 1,6 kHz. 1,6 kHz is also an exact 1:5 frequency difference from the EtherCAT messaging system that issues the synchronization. The logical DAB switching

frequency would be a synchronized multiple of the CHB. At 19,2 kHz, the DAB would complete 12 switching cycles where the CHB would complete only one. Due to the network synchronization, as well as firmware limitations within the Texas Instruments C2000 microcontroller, the switching frequency had to be set to 16 kHz. This being not only a multiple of the CHB, but also of the EtherCAT frequency.

This is important because it leads to the dimensioning of the cross-over frequency of the PI controller for the phase shift. This being 10 times lower than the DAB switching frequency, the cross-over frequency is dimensioned at 1600 Hz. MATLAB is then used to determine K_P and K_I for the controller, resulting in K_P = 0,56 and K_I being manually increased to 5000 for the following resulting bode-plot of the open loop gain.

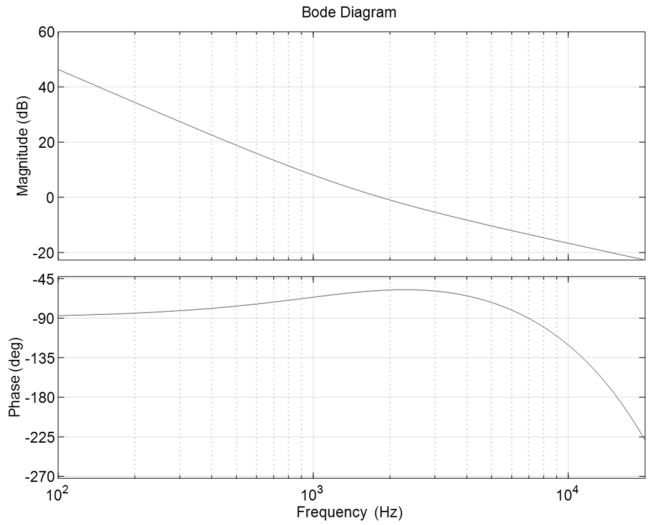


Figure 12-13 MV capacitor charging open loop gain

Good stability margins are observed and the next step will be to verify the control loop on the actual hardware.

12.4.1.3 MV capacitor charging loop verification

For verification of the MV charging loop, one SST module was used. On the LV-side, a power supply was connected to provide 15 V. The test setup is depicted in Figure 12-14 below.

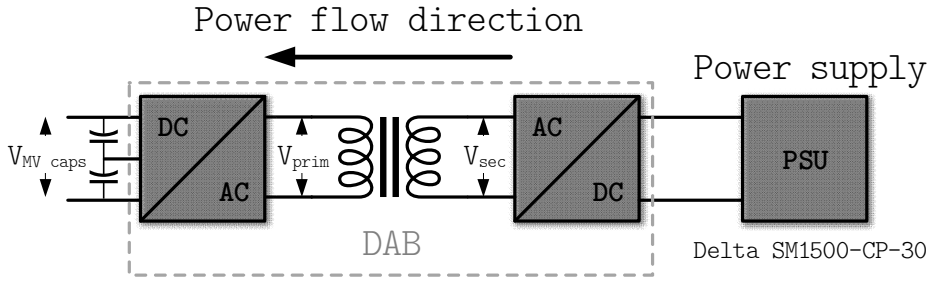


Figure 12-14 MV capacitor charging controller test setup

The "DC-bus" voltage was measured on the output of the power supply unit itself. The LV side voltage of the DAB transformer (V_{sec}), the MV side voltage of the DAB transformer (V_{prim}), and the current through the DAB transformer at the MV side were all monitored on an oscilloscope. Before observing the results, one deviation is expected in advance. The first is the deviation of the MV capacitor voltage from the voltage setpoint. This will be due to the inaccuracy of the ADCs at low voltage. A voltage setpoint of 30 V will likely result in a measured voltage along the lines of 50 V.

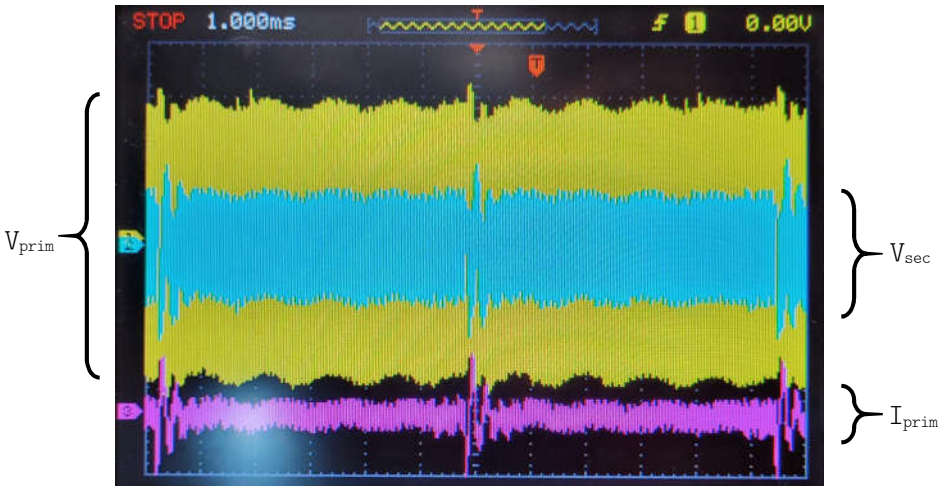


Figure 12-15 MV capacitor charging loop test results

The voltage on the primary side was observed via a multimeter at 46~47 V, this was as anticipated. The control loop is behaving according to the design. There was, however, one phenomenon that was not as designed. As can be seen in Figure 12-15, the current I_{prim} and V_{sec} exhibit transients. In this image, the there are three transients visible, apparently at a fixed frequency apart. This was not a fixed frequency in practice, however. The transients appear random in nature. Taking a close-up by adjusting the timescale & triggering conditions of the oscilloscope reveals Figure 12-16 below.

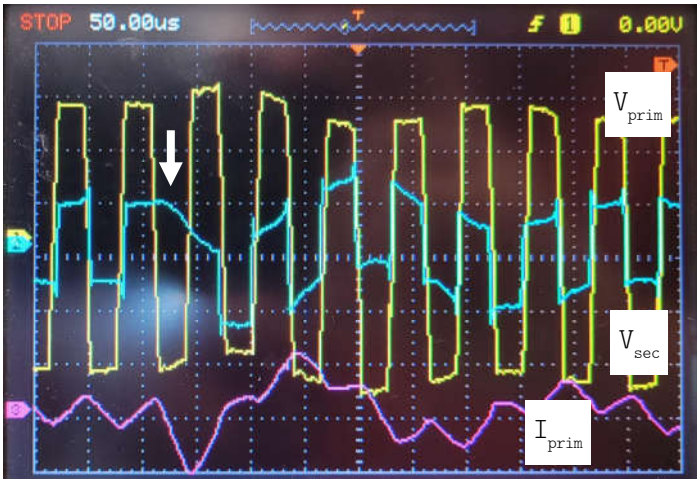


Figure 12-16 Missing switching instance

At certain moments, the secondary bridge will skip exactly one half of a switching cycle. This causes the current to continue ramping down through the DAB transformer. This in turn, causes the power supply's current limiter to trip and its voltage to fluctuate. The voltage fluctuation is transferred to V_{prim} as well. The root cause for this missing switching instance has been thoroughly investigated, but not identified as of yet. The eliminated causes are listed below:

- Improper use of a shadow register (updating PWM counter values in-situ without the use of a shadow register)
- PWM dead-time (a dead-time that prevents a switch from operating)
- Execution order (the order in which ePWM channels are updated and the compiler builds the firmware execution order)

While the transients are unfortunate, the control loop is actually behaving as designed and can be used for charging the MV capacitors to a desired voltage level.

12.4.2 MV capacitor balancing loop

The voltage across the MV capacitors needs to be actively controlled for two reasons. The first is that the mid-point between

the capacitors serves as the reference for the entire module, and that the MV DAB switches are referenced from it. This is important because the MV DAB switches can handle up to 1700V and without actively controlling the capacitor voltage, would be destroyed. It is also important to note that an imbalance of 400V would result in the DC blocking capacitors burning out on *both* sides of the DAB transformer. During testing, there were two instances where on both the primary *and* secondary side of the DAB transformer saw smoke coming of the DC blocking capacitors. This is because an over-voltage will short out the capacitor on one side, which results in a short circuit transient. That short circuit transient is then transformed to the other side of the DAB transformer and causes an over-voltage on that second DC blocking capacitor as well.

The MV capacitor voltage is dependent on the switching waveform that is applied to the DAB's switching legs. In Figure 10-1, the MV capacitors, as well as switching leg A on the MV-side of the DAB has been highlighted.

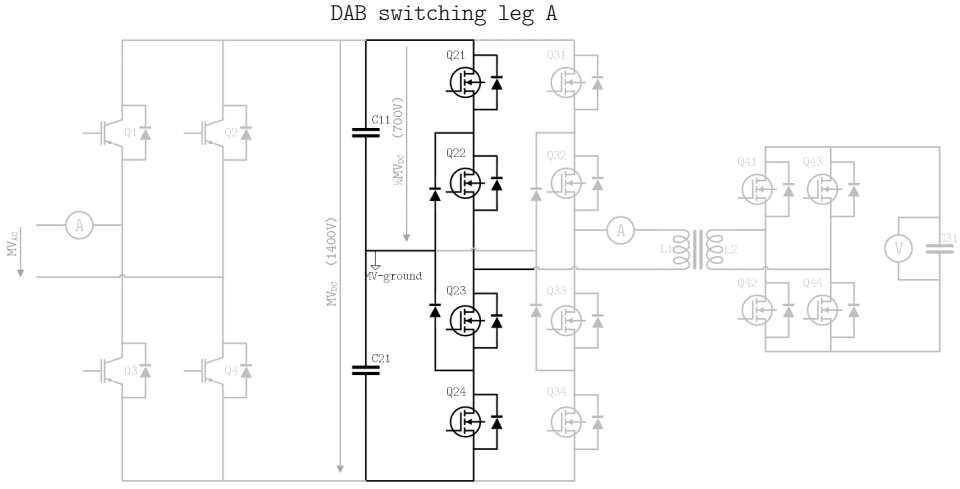


Figure 12-17 Switching leg A of the DAB in the SST module

Switching leg A of the DAB has been controlled in such a way that a trapeziod waveform is achieved.

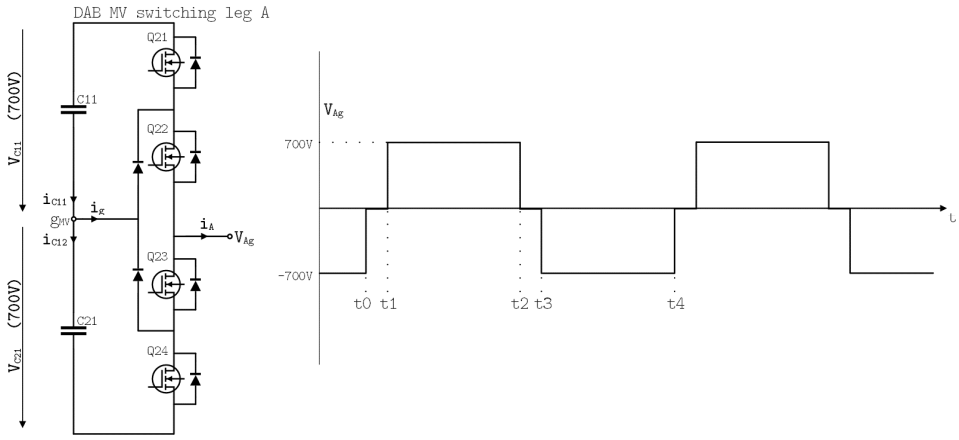


Figure 12-18 Switching waveform generated by leg A

The switching waveform is made up of four switching instances, labeled t0 through t4 (with t0 and t4 representing the same switching moment). Between each two switching instances, an area can be defined that represents a state when the switches are not operated (the switches are either open, or closed, but not switching). During these states, the MV capacitors C11 & C21 are impacted in three ways. They are either being charged, discharged, or held at a constant voltage.

The voltage across these MV capacitors is determined by several factors. The first factor is the CHB, which may charge or discharge both capacitors simultaneously. During a normal power transfer operation (transmitting power from the MV side to the LV side), the CHB charges the MV capacitors. During reverse power transfer operation (from the LV side to the MV side), the DAB charges the MV capacitors and the CHB discharges them.

For the normal power flow direction of MV to LV, the discharging of the MV capacitors occurs because of the DAB. A perfectly symmetrically applied switching pattern of the DAB will discharge capacitors C11 & C21 equally, meaning that their voltages will be

roughly the same. In practice, however, the switching pattern will never be perfectly symmetrical. For example, there are tolerances on the components of each switch's driver, resulting in ever so slightly different on/off moments between switches. Another is the length of the PCB traces from the microcontroller to the drivers, the design of the microcontroller silicon, and perhaps the influences of software. To compensate for these imperfections, the switching pattern of the DAB must be controlled. Specifically, the switches that result in a current through capacitors C11 & C21.

The figure below illustrates the four switching states for leg A.

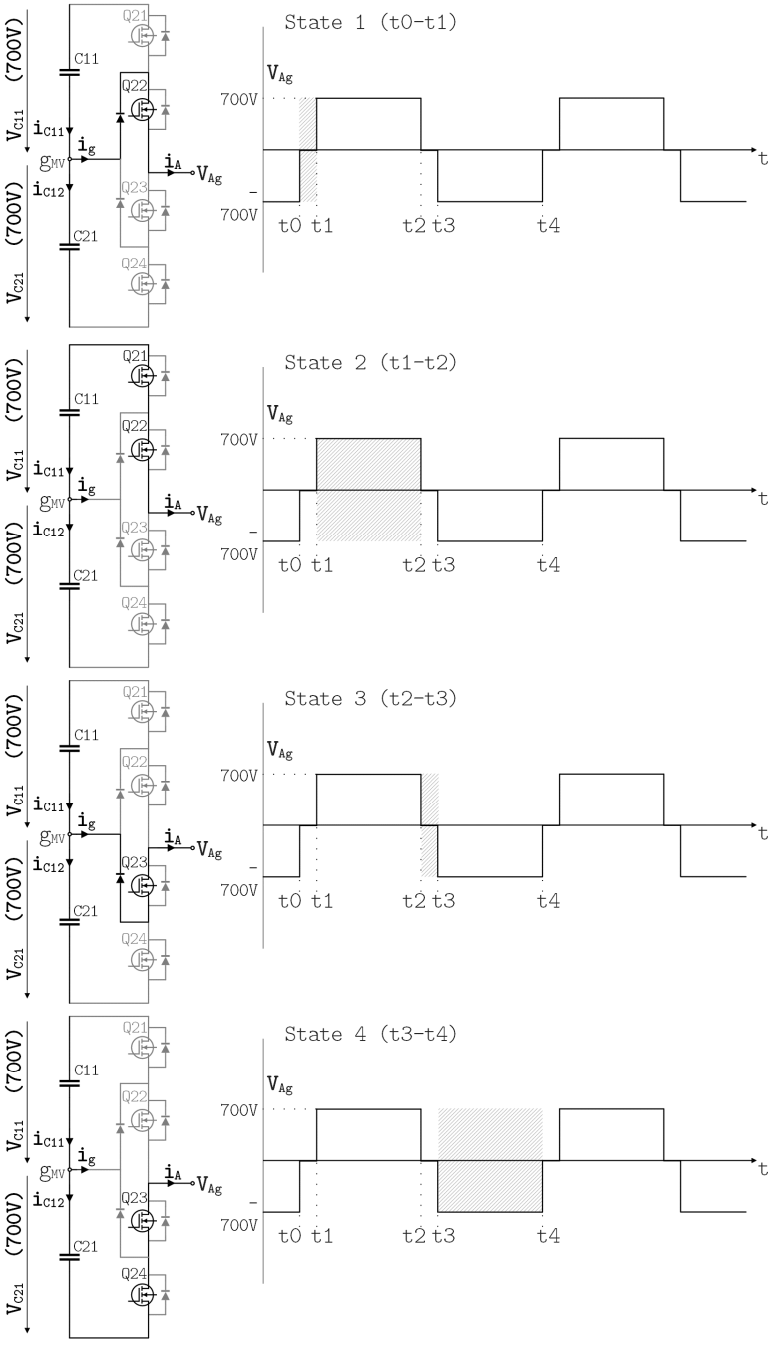


Figure 12-19 The four switching states of leg A

As can be seen in Figure 12-19, there are only two states in which the voltage across C11 & C21 can be controlled. These are state 1 (from t0 to t1) and state 3 (from t2 to t3).

States 1 and 3 correlate with the operation of switches Q22 & Q23. These two switches are the only ones that can affect currents i_{C11} & i_{C21}.

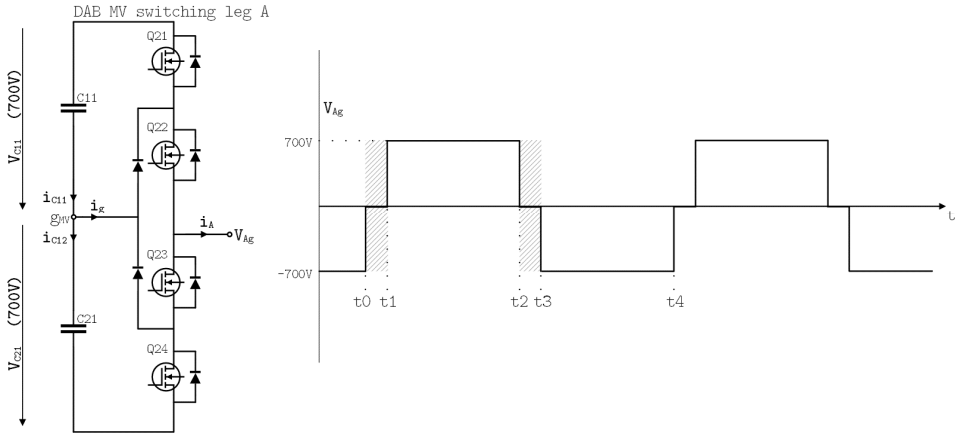


Figure 12-20 Only switching states 1 & 3 can affect C11 & C21

By varying the time these switches are "on", the currents will flow for a proportionally longer (or shorter) time. In turn, this will affect the voltage across the respective MV capacitor.

So, for example, if the voltage across C11 is higher than C21, the SST module's neutral point g_n would be "too low". To correct for this:

- Switch Q22 would be closed longer in State 1 (compared to Q23 in switching State 3).
- This would allow current i_{C11} to flow for a longer duration (compared to i_{C21}).
- Thus, discharging C11 more compared to C21.

Mathematically, this behavior can be described as the voltage difference between V_{C11} & V_{C21} needing to be compensated by adjusting t_{01} & t_{23}.

$$\Delta V = V_{C11} - V_{C21} > 0 \;\rightarrow\; reduce\ t_{01}\ and\ increase\ t_{23}$$

12-11

As these switching patterns occur at ~20kHz it is unlikely a single cycle will suffice to compensate a large voltage difference. The goal, however, is to compensate the voltages across C11 & C21 every switching cycle with a closed control loop. By continuously adjusting the switching times, the capacitor voltages will remain balanced.

The control loop for compensating the MV capacitor voltage difference will be achieved with a basic PI control. The modeled loop is shown in Figure 12-21.

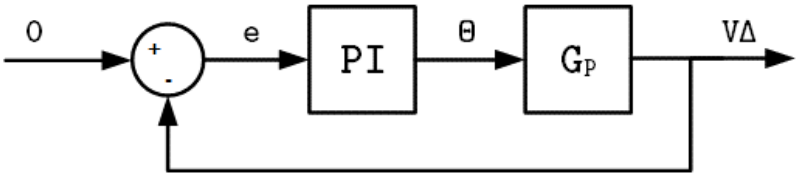


Figure 12-21 MV capacitor voltage balancing control loop

The first step to define this control loop is to determine the transfer function of the plant G_P. The plant in this particular case is the two capacitors whose currents can be described as followed.

$$i_{C11} = C_{11}\frac{dV_{C11}}{dt} \qquad i_{C21} = C_{21}\frac{dV_{C21}}{dt}$$

12-12

Since the goal is to determine the delta between the two voltages and currents, the two equations are combined and rewritten to 12-13. It should be noted that since, both capacitors have the same capacitance value, the variable C_{11}=C_{21} and can simply be written as C.

$$i_g = (i_{C11} - i_{C21}) = C\frac{d(V_{C11} - V_{C21})}{dt}$$

12-13

$$\Delta(V_{C11} - V_{C21}) = \frac{1}{C} \cdot \bar{\iota_g} \cdot \Delta t = \frac{1}{C} \cdot \bar{\iota_g} \cdot 4 \cdot \theta T_s$$

12-14

$$\Delta(V_{C11} - V_{C21}) = \frac{4T_s}{C} \cdot \bar{\iota_g} \cdot \theta$$

12-15

$$With\ plant\ G_P = \frac{4T_s}{C} \cdot \bar{\iota_g}$$

12-16

Now that the plant has been determined, a stability investigation can be done to determine the control variables P and I. This is done via a bode plot.

12.5 Conclusions

This chapter has answered the research questions 10 and 11. The first research question of this chapter was:

7) **What levels of control are necessary for an SST?**

The answer to this research question is that during any sort of operation of the SST, it is necessary to balance CHBs (or their capacitors if you will) with respect to each other. Another important aspect that needs to be controlled are the current / voltage on the MV (and also on the inverter / LV) side, for ensuring power quality. With the focus of this thesis being the IEC60076-3, research question 11 is also answered.

8) **What impact does the IEC60076-3 have on control loops?**

The IEC60076-3 has three tests that are in the scope of this thesis. The AV test is affecting the control of the DAB in the sense that the DAB transformer's leakage inductance is a critical parameter. The leakage inductance affects the power flow of the DAB and the AV test poses a significant impact on the isolation levels required of the DAB transformer. A higher insulation level requirement also

increases that same leakage inductance due to the need for greater insulation thickness, and creepage & clearance distances. Thus, the IEC60076-3 even affects the firmware / control aspects of an SST.

The other two tests are the IVW & IVPD tests and these impact the control of an SST as well. The test voltage levels will result in CHBs / modules operating near their breakdown voltage limits and as such, will need to be balanced with respect to each other. This means that control loops must be implemented to ensure each module has roughly the same voltage on its CHB / capacitors. Failure to control the voltage balance of the SSTs modules would result in a cascading failure.

13. Verification

With an SST design established that is potentially compliant to the IEC60076-3 AV, IVW, and IVPD tests, the following two research questions are quite logical:

9) **How is compliancy verified?**

This research question is investigated in this chapter, and it will be established that the designed SST prototype is in fact, not compliant to the IEC60076-3. This leads to the next two closely related research questions:

10) **What are the results of a compliant SST design?**
11) **What can be improved?**

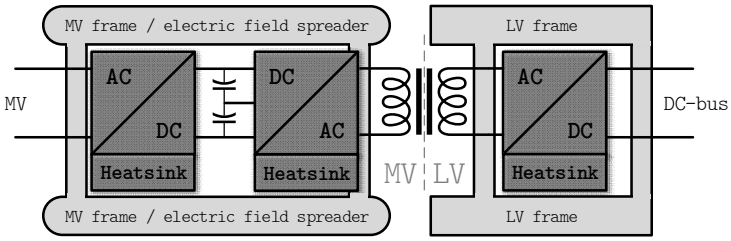
This chapter discusses the laboratory setup for the SST prototype, the devised tests, and the results. There are two main tests that are covered in this chapter. The first is the MV to LV isolation test and the destructive test of the DAB transformer's isolation. The second is the power test where all three modules are transferring power from LV to MV.

13.1 MV to LV isolation test

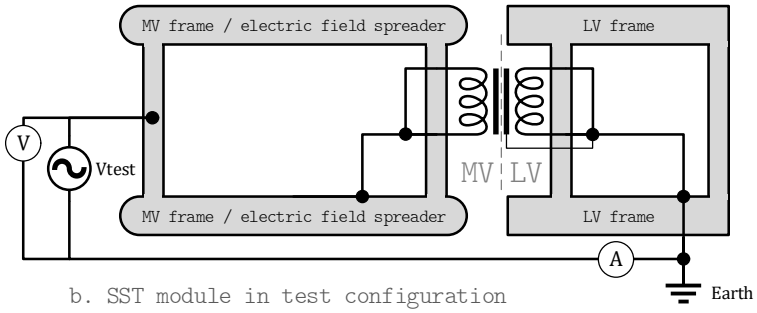
This test consists of two parts and is intended to effectively replicate the conditions of the IEC60076-3's AV test for one module. Measuring on one SST module can be considered a relevant dielectric model of the SST's MV to LV isolation capability.

13.1.1 Equivalent IEC60076-3 Applied Voltage test

The first part of the MV to LV isolation test is to see if an SST module (and more crucially, the DAB transformer) can handle an equivalent voltage to that of the IEC60076-3 AV test. A schematic of the test setup is depicted below in Figure 13-1.



a. SST module in normal configuration



b. SST module in test configuration

Figure 13-1 MV to LV isolation test schematic

The test is executed in the following manner. The 50 Hz alternating voltage source (comprised of two transformers in series) is represented in Figure 13-1b by Vtest. This voltage is measured with a voltage probe close to the test source for monitoring on an oscilloscope. While measuring at the test source is not as optimal as measuring at the DUT, it was necessary to ensure the voltage limits of the test source were not exceeded. It is initially set to zero and slowly increased up to the point where current spikes are detected by the current probe near the earth connection. The detection of current will mean that there is a breakdown, somewhere in the isolation barrier. For this test to represent the equivalent of the AV test, a peak voltage of ≈40 kV should be reached. Figure 13-2 shows the lab setup for the MV to LV isolation test. On the left, the SST module is located on a conductive (and earthed) lab table. The LV frame, DAB transformer core, and the LV winding connections are all earthed with a Litz wire to the lab table.

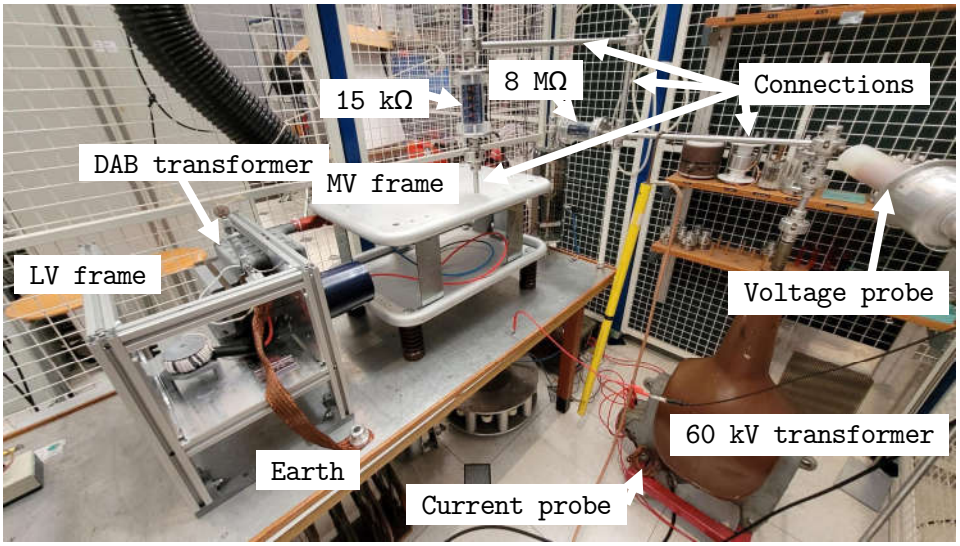


Figure 13-2 Lab setup of SST module MV to LV isolation test

The MV winding connections are attached with a bolt to the MV frame. This MV frame is then connected to the 60 kV_{PEAK} transformer via a 15 kΩ resistor. The 15 kΩ resistor acts as a current limiter in the event of a (partial) discharge. A current probe is added to the bottom of the 60 kV for measuring the partial discharges.

13.1.2 Results MV to LV isolation tests

The tests were executed, yet the results did not correlate with the expectations. Initial testing generated audible electrical discharges at 12 kV_{PEAK} already. Turning down the laboratory's lighting revealed these discharges occurring at the edge of the LV frame (see Figure 13-3 below). These discharges occurred at the edge, over the length of the interface between the LV frame and DAB transformer.

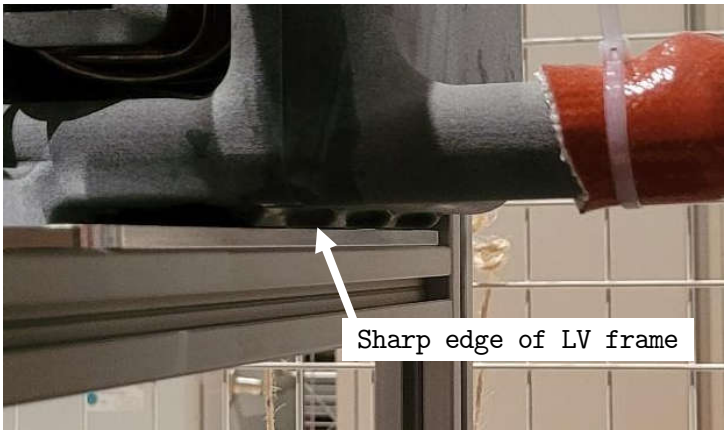


Figure 13-3 Location of observed partial discharges

The cause (but not yet the *root* cause) of the discharges is the sharp 90-degree angle of the LV frame's base plate. An attempt was made to remedy this problem by temporarily applying a curvature to the frame, to distribute the electric field. The temporary solution is depicted below in Figure 13-4.

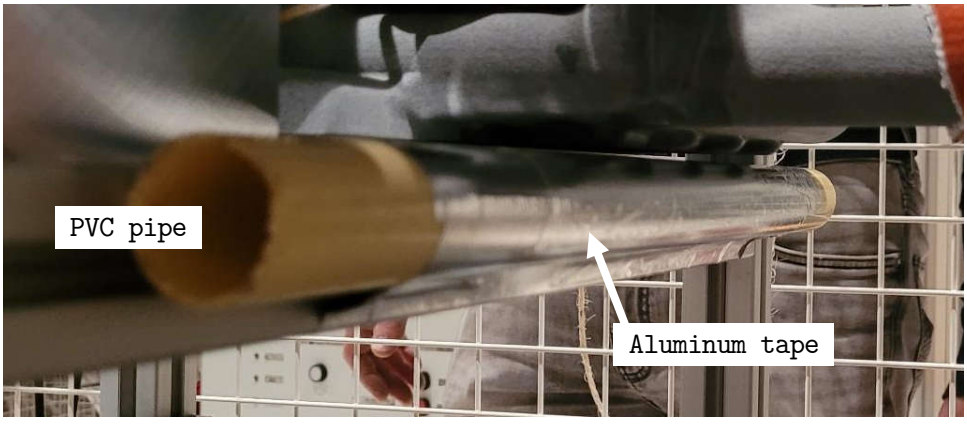


Figure 13-4 Temporary LV frame curvature fix

A PVC pipe was taped to the LV frame using aluminum tape. This ensures a more even distribution of the electric field. The next test (repeated with the same test conditions & procedure) revealed that the electric discharge problem had moved from the bottom of the LV frame to the top of the LV frame. Again, electrical discharges were audible around the 12 kV_{peak} mark.

Figure 13-5 LV frame top side electrical discharges

Fundamentally, it can be concluded that the LV frame was designed incorrectly for coping with the high voltages of the IEC60076-3 AV test conditions. Its proximity to the MV winding is too close and its geometry is too sharp in the direction of the MV winding. The design of the LV frame as-is, should be discarded for the purposes of SST module designs in the future.

With the LV frame being invalid, it is necessary to continue investigating the DAB transformer's isolation capabilities. To verify these, the next test omitted the LV frame entirely. The DAB transformer was placed on top of an empty plastic container. See Figure 13-6 below. This situation reproduces the conditions that the DAB transformer faces, without the LV frame.

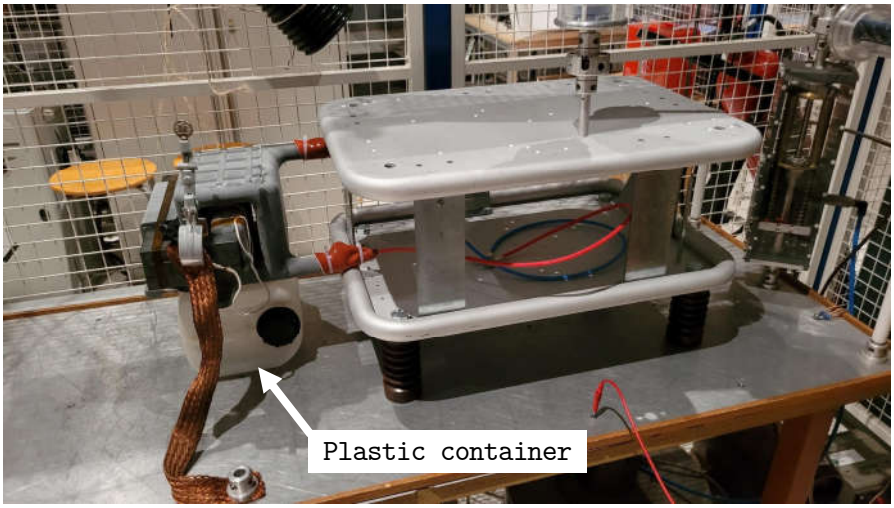


Figure 13-6 MV to LV isolation test without LV frame

The test was executed in the exact same manner as before. Vtest was increased until, again, electrical discharges were audible. Turning the lights of the laboratory down revealed the location of these electrical discharges.

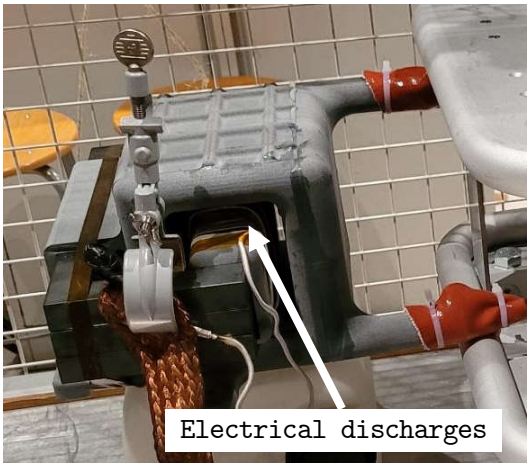


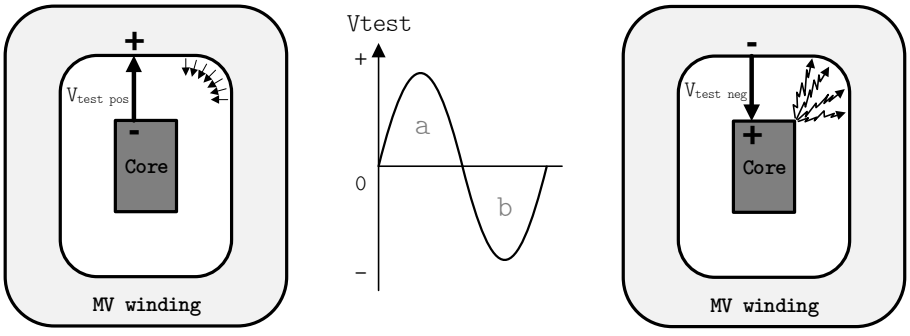
Figure 13-7 MV to LV winding electrical discharges

As indicated in Figure 13-7 above, the discharges were occuring between the MV and LV winding. The test voltage at which these discharges occured, however, had improved significantly from approximately 15 kV_{PEAK}, to around 21 kV_{PEAK}. This voltage, however,

is still insufficient to meet the IEC60076-3 AV test condidtions. **It can be concluded that the DAB transformer design as-is, is flawed with respect to meeting the isolation requirements imposed by te IEC60076-3 AV test conditions.**

The root cause of the discharges in the implemented DAB transformer (and LV frame) is the negative half of the sinusoidal test voltage, in combination with the "sharp" geometry of the core, as well as the MV winding's proximity to the LV frame & core. This root cause will now be explained.

When designing the SST module, careful consideration was taken to design the MV side such, that high voltages are fully managed. The MV frame has carefully designed rounded edges, ensuring an even spreading of the electric field, as well as rated insulators (to ensure insulation from ground or other modules). These design considerations act to mitigate any discharges during the positive half of the sinusoidal test voltage. For the negative half of the sinusoidal test voltage, the LV frame's electrical potential is raised (with respect to the MV side) instead. The problem is illustrated in Figure 13-8 below. In this figure, the LV winding has been omited to more clearly illustrate the problem. Omission of the LV winding also represents a more relevant picture due to the IEC60076-3 AV test being performed between the MV side and the core of a transformer, with the transformer core being grounded.



a. Positive half b. Negative half

Figure 13-8 Positive and negative test voltage effects

During the positive half of the sinewave (Figure 13-8a) the Vtest is applied with the core at earth potential, and the MV winding at a positive potential with respect to the core and earth. Effectively the core is charged with electrons and the electric field is evenly distributed accross the surface of the DAB transformer.

During the negative half of the sinewave (Figure 13-8b) the Vtest is applied with again the core at earth potential, but the MV winding is at a negative potential with respect to the core and earth. It is now that the MV winding is charged with electrons and the electric field is concentrated at the sharp corners of the core. It is here that electrons will discharge from the core (or LV winding) to the MV winding, as this is the closest in proximity. This is because electrons enjoy a diferent level of mobility than a positive charge (the absense of electrons).

This effect is was clearly observable on the oscilloscope. In Figure 13-9, the electrical discharges have been marked with white arrows for channel two, which is the signal from the current probe. On channel one, the sinusoidal voltage of Vtest is shown, with an amplitude of around 26 kV.

Figure 13-9 Oscilloscope plot of LV to MV electrical discharges

It is clear from the oscilloscope plot that these discharges occur only at the negative half of the sinewave, with no discharges being observed during the positive half. **This verifies that the design of the DAB transformer as-is, is insufficient to cope with the high test voltages of the IEC60076-3 AV test conditions.**

The fundamental design flaw is that the LV side of the SST was not designed with the same voltage in mind. With the overview of the state-of-the-art, the writer of this thesis concludes that this represents a significant gap in the field of SST designs. The LV frame / LV side of the SST should be designed such that when the MV winding of the DAB transformer is subjected to a large negative voltage, no discharge will occur towards the MV winding. Solutions can be the absense of "sharp" geometry towards the MV winding, insulation, or increased distances between the LV frame / LV side and the MV winding.

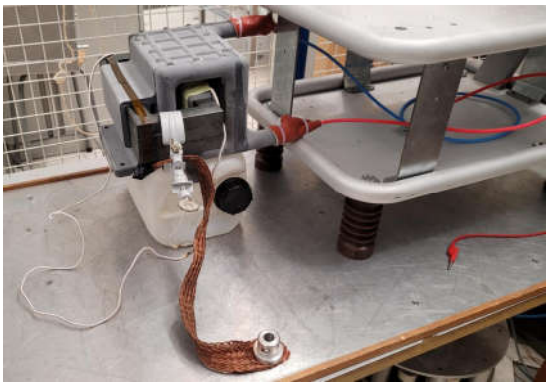
Alternatively, the DAB transformer should be placed in between the MV & LV frames in such a way that no partial discharges can occur. Fundamentally, this would still leave the one physical "interface" of an SST that will remain critical: The DAB transformer's core with respect to the MV winding. There is no foreseeable alternative for transfering power within an SST while still providing galvanic isolation other than the (DAB) transformer. While transformers come in many configurations, it is reasonable to say that physics limits the power transfer through the DAB transformer without a core. Thus, there will most likely always be a core, surrounded by an MV winding in an SST application.

A contribution of this thesis is that the LV side (with respect to the MV side) of an SST needs to be designed with the same design considerations as the MV side. Meaning the careful rounding of geometry for electric field spreading, taking into account creepage & clearance distances, and insulation levels that are all dimensioned for a 40 kV_{PEAK} test voltage.

This is because power density is a driver for SSTs and (DAB) transformers are the only reasonable engineering solution for transfering power, as well as provide galvanic isolation. Thus the MV & LV sides of an SST module are likely always placed in the closest allowable proximity. When this is not done, then the only fundamental galvanic isolation "interface" that remains, is the (DAB) transformer core with respect to an MV winding. These two parts will need to be designed together to cope with the 40 kV_{PEAK} test voltage.

Testing of the DAB transformer continued to gain further knowledge on its designed isolation properties. The first test that followed saw the LV winding covered with an isolation tape. The type of tape used was a "1350-1 19MM" from 3M and this has a rated isolation level of 5500 V. Figure 13-10a below shows the LV winding covered in the isolation tape. It is important to note that the LV winding also was stripped of four turns to ensure that all windings fit on the bobbin. Previously, there were four turns that did not fit on the bobbin, and were wound over the "first layer" of turns. This "second layer" of turns resulted in a deacreased distance between the MV and LV windings. For this next test, the number of turns were reduced.In Figure 13-10b, the winding has been placed in the test setup using the exact same test procedure. The DAB transformer's core and both ends of the LV winding have been clamped to a Litz wire to ground.

a. LV winding insulated with tape



b. Insulated LV winding in test setup

Figure 13-10 LV winding covered in isolation tape

The test voltage was again applied to the MV frame to which the MV winding was connected. Slowly increasing the test voltage's amplitude, discharges were observed at 26,9 kV_{PEAK}. This is a significant increase from the previously measured 21 kV_{PEAK}. The improvements is most likely due to the four turns that were removed from the LV winding, which increased the distance between the MV & LV windings. This is probably a bigger contributor than the application of the isolation tape on the LV winding. In an attempt to further the understanding of the DAB transformer's design limits, the LV windings were removed in their entirety. The bobbin was kept in place to hold the core into position and the test was repeated in the same manner as previously. The DAB transformer is depicted in Figure 13-11 below with the LV winding absent (only the LV bobbin still present to support the transformer's core).

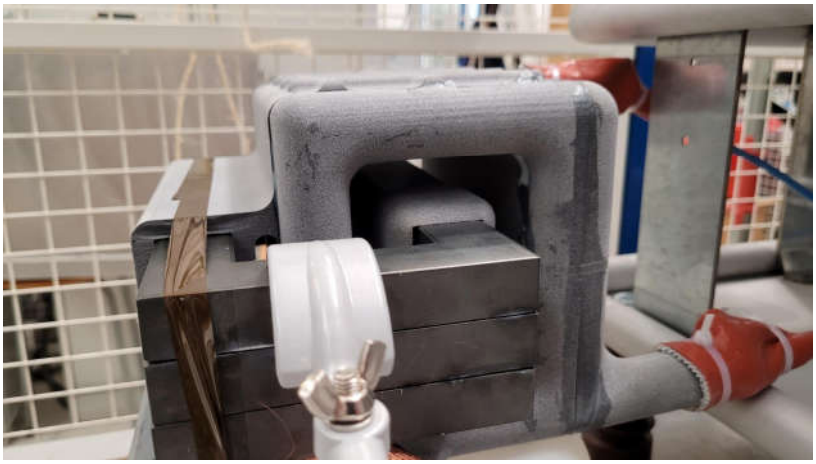


Figure 13-11 Isolation test with LV turns removed from bobbin

The result of this test amounted to a further increase in the test voltage's amplitude before discharges were heard. This time, the discharges were occuring somewhere between 27,9 kV and 29,2 kV. This turned out to represent roughly the limit of the DAB transformer. This is because one last test was performed with the core removed entirely, and discharges occured at 29,2 kV_{PEAK}.

These tests reaffirm the previously drawn conclusion that the DAB transformer requires a redesign in order to be compliant with the IEC60076-3's AV test conditions. This redesign would see the MV winding increase in "diameter" to ensure significant physical distance between it and the core. Additionally, a rounded core could be looked into to improve the electric field distribution.

13.1.3 Destructive isolation test

The second part of the MV to LV isolation test is the destructive isolation test. It is intended to not just see if the DAB transformer design can handle the IEC60076-3 AV test voltage. It is instead intended to find the limit of its isolation capabilities. Two tests were performed, one at 40 kV DC, and one up to 60 kV_{PEAK} AC at 50 Hz. For these tests, the core was first reinserted in the event any inward isolation failure would occur, still leaving room to test any outward isolation failure. Neither

of these two tests caused any breakdown of the insulation. The 60 kV_{PEAK} AC test did, however, produce surface discharges on the DAB transformer. See Figure 13-12 below.

Figure 13-12 Surface discharges on DAB transformer during 60 kV_{PEAK} AC test

These surface discharges started occurring at approximately 29 kV, which is in line with the previous tests. The conclusion is that the surface of the DAB transformer will radiate discharges to its surface or the air before it is able to reach the necessary 40 kV_{PEAK} of the IEC60076-3 standard. This is very likely due to the 3D printed potting "bucket". The 3D printed material is likely suffering from micro voids of air within the 3D print itself. If this is indeed the case, then the use of 3D printed material for such a purpose will present problems in any future SST design.

13.2 Power transfer testing

The second aspect of the prototype that is under close verification is whether it can perform its power transferring functionality. This is done by verifying the power transfer through the DAB from LV to MV, charging the MV capacitors to a specific value, followed by generating an interleaved sinusoidal grid current through an inductor. An overview of the test setup is depicted in Figure 13-13 below.

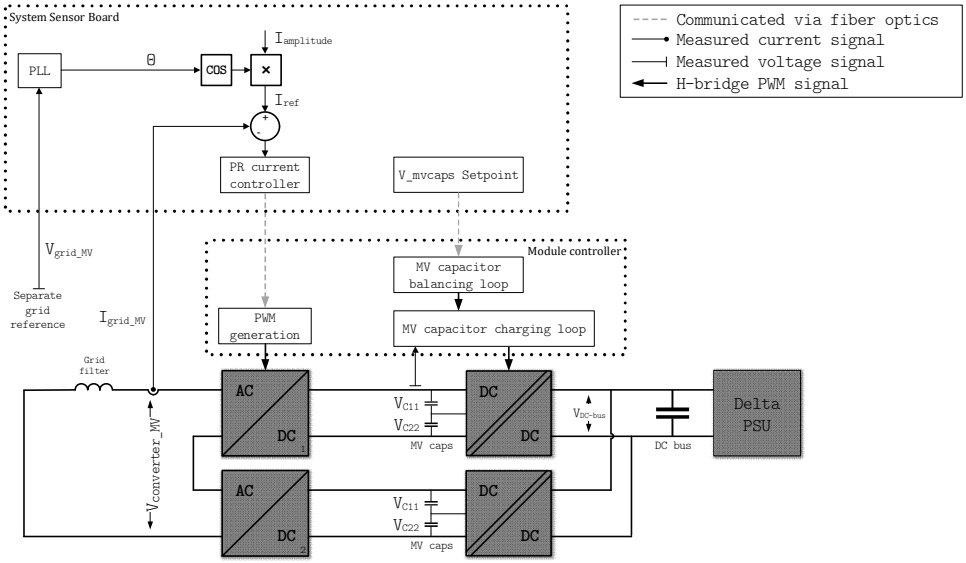


Figure 13-13 LV-to-MV SST power flow measurement test setup

The power supply connected on the LV side is from the brand Delta and was set to 20 V. This PSU forms the DC-bus from which each SST module controller regulated the voltage on its MV capacitors to a setpoint of 30 V. This setpoint was generated at the System Sensor Board (SSB) and sent via the network to the SST modules.

With each SST module's MV capacitors at 30 V, the CHB's received their setpoints via the EtherCAT network from the SSB.

The SSB was fed with a grid reference and the PLL generated a stable reference for the MV current loop. As can be seen from Figure 13-14 below, the loop automatically compensates for the inductive nature of the "grid" by leading the converter voltage. The generated grid current is therefore in phase with the grid voltage.

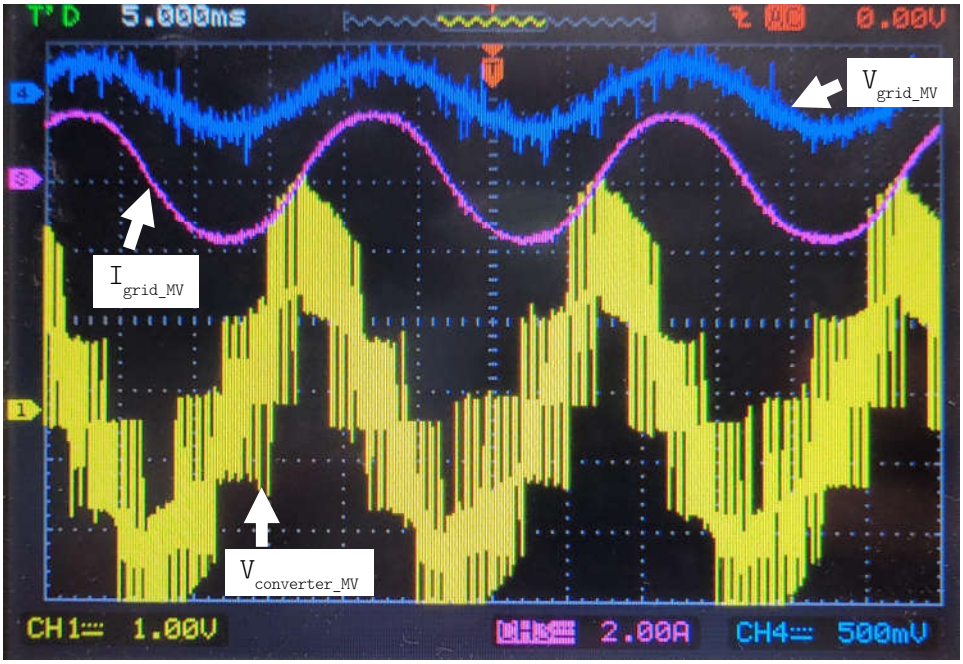


Figure 13-14 Power transfer through two modules with interleaved switching

Also notable is that the converter voltage is interleaved, thus resulting in a "smoother" current. The noise on the grid voltage is due to the probe's proximity to the switching devices, and their generated interference.

13.3 Conclusions

After performing tests to represent the equivalent of an IEC60076-3 AV test, the remaining three research questions have been answered.

9) How is compliancy testing designed for?

Compliancy to the IEC60076-3 AV test is verified by effectively applying a test voltage over the DAB transformer, since this is the main insulating component between the MV & LV sides of SSTs in general. It is, however, critical to include any components that are also affected by the creepage & clearance requirements of the standard. For the SST *prototype* this means that the mechanical frames on both the MV and LV side should be designed with smooth curvatures. Additionally, an increased distance between the DAB transformer's core, or a rounded core should also be employed. It's important to note that the DAB transformer design will most likely always be designed to occupy the smallest volume possible. This is to improve the SSTs overall power density. Even if a DAB transformer design does not have any other volume restrictions imposed, the IEC60076-3 compliancy will always result in volumetric limits. This is because any sort of core material will be running through an MV winding. Thus, a physical / volumetric limit between the core and MV winding will come into effect. The two remaining research questions have also been answered, these were:

10) What are the results of a compliant SST design?
11) What can be improved?

An SST that has a design which is compliant to the IEC60076-3 AV test, will require careful consideration of not only the MV side, but also the LV side with respect to the applied test voltages. Until now, SSTs have been designed with deliberately designed geometry, insulation, and clearances for the MV side, but these same considerations apply to the LV side as well. This is because the AV test applies an alternating voltage, resulting in not only an MV side at a high *positive* voltage of 40 kV_{PEAK}, but also an MV

side with a highly *negative* voltage of minus 40 kV_{PEAK}. It is this negative voltage that requires the LV side of the SST to be designed with all the considerations that come with "high voltage" applications (meaning geometry, insulation, and creepage / clearances).

14. Discussion

14.1 Future SSTs and IEC60076-3 compliancy

Is compliancy with the IEC60076-3 necessary for SSTs in the future? The author of this thesis posits that it *is* necessary because there are grid conditions that merit having a design that is capable with dealing double the MV on its inputs.

14.1.1 Customer-minutes-lost

It is important to note that, protection measures / devices in the electricity grid are not really implemented to protect the transformer (or SST, or any other equipment), but they are there to prevent any problems for the *electricity grid*. The electricity grid in the Netherlands has an extremely high up-time, resulting in a very low number of customer-minutes-lost. This high reliability, with respect to transformers, is currently achieved using a very robust and mature technology in the form of the conventional power transformer. The oil-based variants are in some ways exceptionally fault-proof with their insulation even being self-repairing because it is a liquid. Replacing such robust devices with SSTs will result in a significant amount of customer-minutes-lost if careful design considerations aren't taken.

This thesis argues that there are two design considerations that are of particular importance for achieving a robust SST design. These are the over-dimensioning of the input voltage and the isolation level between the primary & secondary sides. Both design considerations align with the IEC60076-3 standard, specifically the AV, IVW & IVPD tests. The next paragraph will present a discussion on the factor two over-dimensioning of an SST's MV input, how it relates to SST reliability, and what the relevance of the IEC60076-3 standard is.

With regards to over-dimensioning the power rating of the SST, this will have significant impact on the design time (resulting in high

NRE) and final hardware cost. Some mitigation is possible with emergency load shedding to improve the SST's up-time [57]. That, however, is unlikely to achieve the same level of overloading as conventional transformers.

14.1.2 Protection coordination

For HV systems of ≥300kV, the IEC60071-1 standard has provisions that allow protection to be coordinated. Meaning that overvoltage capability of a transformer may be limited if alternative protection mechanisms are installed. Such a provision allows transformer manufacturers to limit the degree of over-dimensioning the transformer voltage handling capability in a way that is "*…generally deemed economically, and obtainable…*", but still be capable of dealing with grid overvoltage events.

Such protection mechanisms are typically MOVs and TVS'. There is however a limiting factor to installing such protection mechanisms, and that is their selectivity. A typical MOV and TVS commonly have a factor 1,5~2 difference between the voltage level at which they *can* start tripping (known as the tripping voltage), and the voltage level at which they are *guaranteed* to trip (known as the clamping voltage). For an MV SST, this means that the clamping level must be equal or less than the sum of the break down voltages of the module's switches. This can be described by formula 14-1, where n is the number of modules in series in a phase.

$$V_{clamp\ MOV/TVS} \leq V_{breakdown\ sw\ mod\ 1} + V_{breakdown\ sw\ mod\ 2} + \cdots + V_{breakdown\ sw\ mod\ n}$$

14-1

It can be concluded that to protect an SST, choosing MOVs and TVS' with their *clamping level* equal to the peak grid voltage, would result in spurious tripping. Similarly, to protect an SST choosing MOVs and TVS' with their *tripping level* equal to the sum of the breakdown voltages would not guarantee clamping of any overvoltage grid events.

An alternative to MOVs or TVS' could be a yet undeveloped technology. For example, a power electronics clamping device could be developed. Again, keeping in mind that the protection device is there to guarantee the up time of the electricity grid, and not *only* to protect the SST. Such a protection device would measure the grid voltage and operate switching devices to conduct current away from the SST to minimize an overvoltage grid event. The IEC60076-3 currently does not have provisions for such a protection device.

14.1.3 Isolation levels

The second design consideration for SSTs that is argued in this thesis, is the necessary isolation level. This isolation level is stated by the IEC60076-3 AV test as better than 40 kV_{PEAK} @ 50 Hz and has not been observed in the state of the art. More importantly, measurements show that such a test not only imposes a high test voltage on the MV side, but also on the LV side due to its alternating nature. To comply with the AV test conditions, the LV side of the SST needs to be designed with same degree of "high voltage care" as the MV side. Meaning that the LV side will require rounded geometry, insulation materials and / or creepage and clearance consideration to the same degree as the MV side.

14.1.4 Out-of-scope parts of IEC60076-3

For this project, several tests of the IEC60076-3 have been considered out-of-scope. That, however, does not mean that these are not applicable to SSTs. For example, the AuxW test is designed to test auxiliary windings of conventional power transformers. Equipment may be connected to these windings and as such, from a safety point of view, these should also be tested. For an SST, a valid discussion point is "What is an auxiliary winding?". Would these be the system controller with its measurement sensors? Or would it only constitute power electronics outputs like additional inverters, or equipment connected to the DC-bus. These are aspects that should be part of a discussion for future revisions of the IEC60076-3. It is the authors recommendation that the architectural

boundary of an SST is carefully chosen. If an SST is considered a black box with only (for example) three MV inputs and three LV outputs, that those could be considered the "windings". If an SST is designed with a DC in/output, then those should probably be considered as (auxiliary) "windings" as any equipment connected to it crosses the boundary of the black box. This would, however, still lead to a gray area. Because it can be foreseen that there are widely different pieces of equipment that can be connected to said DC in/ouput / winding. Something as simple as a voltage monitoring device for the DC in/output can be considered a very different piece of equipment from for example, a field of solar cells or a car charging station. Hence there will be a need to standardize, possibly based on power level, the necessary tests for SST connections.

14.1.5 Recommendations for future revisions of the IEC60076-3

The IEC60076-3 was written to guarantee that conventional transformers for the electricity grid are tested to a level that ensures a high reliability of the electricity grid. It does so by setting test conditions that require a very robust conventional transformer design.

The standard currently makes no distinction between conventional transformers and SSTs. This means that the test conditions for conventional transformers, are also applicable for SSTs. For designing the SSTs power electronics, this presents a challenge. The strict test conditions mean a significant time and monetary impact on the cost of SSTs. The IVW & IVPD tests are beneficial to keep as-is due to inherently necessary over-dimensioning of the input voltage. This is due to the (currently) available protection mechanisms not being selective enough (e.g., MOV & TVS). The AV test is beneficial in the sense that the isolation level of an SST *should* be tested. The degree of isolation level was established when conventional transformer insulation was still mostly made up of oil and paper. It could be beneficial for the next iteration of

the standard to both carefully investigate SST breakdown mechanisms, as well as the grid conditions that could cause them. For the investigation into SST prototypes, the used insulation materials (e.g., epoxy and silicone) can be looked at to establish a test voltage level that good enough to protect SSTs from the simultaneously investigated grid conditions over their lifetime. Taking common power electronics as an example, a lifetime of more than 10 years for an SST module's power electronics is unlikely. This short lifetime is not necessary an issue for an SST, as modules could be replaced individually through a staggered maintenance / replacement schedule.

14.1.6 Other parts of the IEC60076 family of standards

The IEC60076-3 represents only one of the 26 parts of the IEC60076 standard. It is easy to see that many of the other parts of this family of standards are not limited in relevancy to conventional transformers. Many parts are relevant to SSTs as well. Aspects such as lightning impulses, switching impulses, determination of sound levels, energy efficiency, fittings, DC bias suppression and frequency response are all relevant aspects of conventional transformers that are also likely applicable to SSTs. SSTs deal with some of these aspects differently than conventional transformers do and a careful examination of SST design for writing a new version of this family of standards is essential. A specific aspect that should be highlighted separately is an SST's short-circuit behavior. An SST can only generate a fixed amount of current and cannot exceed its limits. This will cause problems for SST adoption as large parts of electricity grids are protected with fuses. Fuses require large currents to trip within specific times and are a mature protection mechanism. For SSTs to accommodate over-current capability for tripping these fuses in similar time frames as conventional transformers would be cost prohibitive. On the other hand, an SST's inherent current limiting capability might suffice for protecting the grid assets. This is again an important aspect that should be thoroughly investigated when creating the next iteration of the IEC60076-5. It will be necessary for the IEC,

the experts they consult, and other bodies to gain a deep understanding of SSTs, their construction, and how that construction should be governed by regulations.

15. Conclusions, recommendations, and future research

15.1 Conclusions

This research draws several conclusions. The first one is that the electricity grid will have a large influx of renewables and EVs which will result in power quality issues (such as voltage drops / rises or harmonic distortion) for which an SST is an interesting solution. SSTs will have many standards that it could comply with, and this work concludes that the IEC60076-3 is a relevant one. This is because the standard describes tests which emulate grid conditions that an SST may face. Out of the 10 tests the standard describes, three have been identified as having the most impact on the design of SSTs. These are the Applied Voltage (AV) test, the Induced Voltage Withstand (IVW) test, and the Induced Voltage withstand test with Partial Discharge measurement (IVPD).

15.1.1 Applied voltage (MV-to-LV isolation) test

From a power electronics perspective, the AV test checks the galvanic isolation between the primary and secondary sides of a transformer (and by extension, an SST). The height of the AV test voltage is dependent on the class of "system voltage" that the SST falls into (the 10 kV research prototype falls into a 12 kV system voltage class). The test voltage that is applied between the primary and secondary sides of the SST is significantly higher than the "system voltage" class. During the AV test the galvanic isolation stage of an SST's power electronics will be subjected to almost 40 kV_{PEAK} (@ 50 Hz) for a duration of 60 seconds. This test voltage can be interpreted as being directly applied to the DAB transformer's primary and secondary windings. Thus, the design of the DAB transformer's geometry, isolation materials, and creepage & clearance must be carefully considered. Careful design consideration is not limited to the DAB transformer only. The same considerations are applicable to any hardware on the MV side of an

SST's module. The MV side requiring careful design consideration is obvious and well accepted in literature. After measurements with the high isolation test voltage, one significant contribution of this thesis is that careful consideration of geometry, insulation, creepage, and clearance is not only applicable for the MV side, but also the LV side. This is because the AV test applies an alternating voltage, resulting in not only an MV side at a high *positive* voltage of 40 kV_{PEAK}, but also an MV side with a highly *negative* voltage of minus 40 kV_{PEAK}. It is this negative voltage that results in discharges from the LV side to the MV side. The MV and LV sides will likely be designed in proximity for future designed SST modules / prototypes (due to a desired power density). Thus, requiring the LV side of the SST to be designed with all the considerations that come with "high voltage" applications (meaning geometry, insulation, and creepage / clearances). Alternatively, when designing the MV and LV sides with lesser proximity, a transformer will likely be the only feasible way to transfer power while providing galvanic isolation. That (DAB) transformer will fundamentally require some sort of core material with an MV winding around it. Thus requiring *it* to be designed with all the considerations that come with "high voltage" applications (meaning geometry, insulation, and creepage / clearances).

15.1.2 IVW & IVPD tests

The IVW and IVPD tests, again from a power electronics perspective, check the capability of a 10 kV/400V SST's capability of handling a test voltage of 34 kV_{PEAK} for a duration of 60 seconds on its input / primary side. These two tests impose a significant design time and monetary impact on SSTs, because the amount of SST modules is effectively doubled compared to only measuring 10 kV_{RMS}. The number of modules in series is directly correlated to the breakdown voltages of the selected semiconductor switching devices for an SST's modules (a higher breakdown voltage results in less CHBs / SST modules in series to cope with the IWV & IVPD test voltages). These two tests impact the control of an SST as well. The test voltage levels will result in CHBs / modules operating near their

breakdown voltage limits and as such, will need to be balanced more closely / precisely. This means that control loops must be implemented to ensure each module has roughly the same voltage on its CHB / capacitors. Failure to control the voltage balance of the SSTs modules would result in a cascading failure. One of the advantages of over-dimensioning an SST to cope with the IVW & IVPD test conditions, is that during normal operation the semiconductor switches are operated at half of their maximum breakdown voltage. This results in increased lifetime of the switches and simultaneously giving enough room for an MOV or TVS to protect the switches from over-voltage grid conditions.

15.1.3 Additional IEC60076-3 impact

Lastly, the IEC60076-3 does not only impact the electrical parts of the SST, it also significantly affects the mechanical construction. Since the mechanical construction is commonly made up of conductive materials, care must be taken with the shapes of the mechanical structures. The standard requires 120 mm separation of any current carrying element (power electronics in the case of SSTs) to earth, mostly impacting the SST's volume, and reducing SST power density.

15.2 Recommendations

It is necessary to highlight that designing a full SST requires a team made up of many people, with at least one person for each discipline (power electronics designer, EMC specialist, isolation specialist, mechanics designer, thermal specialist, high voltage specialist, circuit board designer, firmware designer, control specialist). On top of that it is also safe to conclude that some overhead for such a team would be necessary. For this research this discipline gap was covered by talking with a lot of specialists and having master students aiding in the design of various aspects.

With regards to the IEC60076-3 standard's applicability, it is the author's opinion that SST compliancy to the three tests investigated in this thesis is highly recommended. This is

especially true for the IVW & IVPD tests, as a factor two over-dimensioning of the total breakdown voltage is not only a good design practice. It is also essential because there are no protection mechanisms (like TVS or MOV) that are selective enough to prevent damage if there is not sufficient margin in the overall breakdown voltage of the SST.

For the AV test, the test voltage *level* is debatable, the test's *applicability* is not. For a 10 kV SST, an isolation test voltage of 40 kV_{PEAK} is required. This voltage level requires very careful consideration with respect to geometry, isolation, creepage, and clearance. The level of this test voltage was devised in the time when transformers were mostly comprised of oil and paper insulation. This high test voltage is likely one of the contributors to conventional transformers having such a long lifetime. For SSTs (if other types of power electronics are any sort of indicator) the lifetime is almost certainly shorter. As such, it is important for the next iteration of the IEC60076-3 standard to carefully consider the necessary AV test level. This should be based on the isolation construction (e.g., epoxy), and the expected lifetime of an SST module.

15.3 Future research

There are several aspects that are interesting for future research. Some could even be argued to be critical for the adoption of the SST as a future electricity grid component. The aspects that were identified for future research over the course of this project have been listed in the next paragraphs.

15.3.1 Further IEC60076 compliancy

This thesis has only focused on part 3 of the IEC60076-3. There are however many parts to this overarching standard. Some of these could be considered of critical for the adoption of the SST. Part 5 of the standard deals with the short-circuit capability of a transformer. For SSTs, this is a crucial problem since large parts of the electricity grid are protected using fuses. Fuses require over-current to occur for the thermal breakdown of the fuse. SSTs

are per default built to limit overcurrent. If an SST were to be deployed in the grid, fuses would not trip in the event of an overcurrent. The response of the SST and the effects of the local grid would have to be investigated. In that case, it might be better to design and build an SST that is compliant to IEC60076-5.
Another interesting part of this overarching standard is part 10 that deals with the measurement of the audible noise. Deploying an SST with switching frequencies of 20 kHz would likely lead to hearing issues for dogs and other pets in the neighborhood. As such, the applicability of the IEC60076-10 could be investigated.

15.3.2 MV side power supply

The first design item that should be improved is *powering* the SST from the medium voltage side. Currently, the SST prototype has electronics on the LV- & MV-sides, yet both are powered from the LV-side. The problem is that the SST cannot become a direct replacement for a conventional power transformer if the MV-side electronics still receive their power from the LV-side. As this would always involve a deadlock upon startup. The current design is not suitable for the field because this would require service engineers to apply a startup power via an alternative means (e.g., a battery) in the substation. While this could be ok for commissioning, it is a completely unacceptable situation during a power outage, as the SST would never power itself up after losing power. This is a problem that conventional power transformers do not suffer from and should be fixed before the SST is a mature enough technology for large-scale adoption in the electricity grid.
One solution is to use the inherent passive rectification of the CHBs to charge the MV capacitors. The IGBTs of the CHB have reverse blocking diodes, and these (by the nature of the IGBTs being wired in an H-bridge configuration) will start passively rectifying the voltage of the MV grid. This passive rectification will result in the MV capacitors being charged as soon as the MV grid voltage is present on the SST's module inputs. If each module controller starts up fast enough, then each module controller could draw their power from the MV capacitors, start up, and start controlling the CHB.

There are several things to note here. The first is that the MV grid voltage will NOT be automatically balanced during this start-up behavior. Meaning that any significant deviation in the capacitance of the MV capacitors (e.g., due to production batch differences), could result in the break-down voltage of the CHB IGBTs being exceeded. If the module controllers, AND the system controller can be made to boot up within about one-eight of a 50Hz period, the voltage would likely be low enough to not exceed any of the module's breakdown voltage limits. The selected TI C2000 F28379D controlCARDs should be inherently fast enough to manage this boot time of 2,5ms (one-eight of a 50Hz period). The current system controller (Beckhoff CX2040), is however, not fast enough. It is very likely possible to omit this CX2040 altogether if sufficient effort is put into writing firmware for the System Sensor Board's F28379D controlCARD to turn it into an EtherCAT "master". Thus enabling the ability to start-up the EtherCAT network well within the 2,5ms.

15.3.3 Isolation & LV side geometry

The MV to LV isolation tests revealed that careful design consideration of an SST's LV side is necessary with respect to high voltages. Future research could focus on different (rounded) core geometries, greater physical distances, insulation materials and their impact on SSTs. Specifically, the impact on control bandwidth, efficiency / power density, partial discharges, and cost.

15.3.4 Compliancy to other standards of the IEC60076 family

The IEC60076-3 is only a small part of standards that are applicable to conventional transformers. The IEC60076 family of standards are all developed to ensure conventional transformers are compliant with the grid and its conditions. This compliancy is necessary to ensure that the grid remains operational, and the power delivery is not compromised.

15.3.5 The integration of SSTs into existing grid structures

SSTs present a unique opportunity to solve power quality and other issues in the grid. However, there is not a lot of research

into the integration of SSTs with the grid. Many research questions come to mind:

1) What are the necessary short circuit powers to blow existing fuses?
2) Is it possible to omit fuses from SST substations entirely?
3) What modifications are necessary to existing substations in order to integrate an SST into it?
4) What are the weight, volume and environmental restrictions when integrating an SST into an existing grid?

15.3.6 Cyber security

One aspect that has been placed out-of-scope early in the project, is cyber security. With power electronics being controlled with microcontrollers that are networked to a system controller, the barrier for connecting an SST to the internet is very low. All the hardware pre-requisites are almost inherently part of any design. As such, cyber security for SSTs will become a critical aspect to its adoption. After all, a substation that is remotely shut down by a nefarious actor has great consequences for customers. An early recommendation for future research would be to design SSTs with high levels of diagnostics, but low level of controllability. An in-depth look on hardware implementations, as well as software implementations will be necessary.

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