Photonic flip-chip assembly of InP on TriPleX with laser soldering

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We present a photonic flip-chip assembly for a 4 mm × 4.6 mm InP die with 58 electrical connections on a 16 mm × 8 mm TriPleX die by using laser soldering. Two laser soldering schemes are investigated and show reliable contacts with a 6 N shear force: (1) using a laser wavelength where silicon is highly transmissive (through-silicon laser soldering) and (2) using a laser wavelength where silicon is not transmissive (heat-conduction laser soldering).
Keywords: *Photonic assembly and packaging, Flip-chip bonding, laser soldering.*

INTRODUCTION

Assembly and packaging for photonic integrated circuits (PICs) have been attracting considerable research interests over the years, in particular towards a combination of III-V and Si-based PICs [1]. However, many challenges remain, such as cost-efficient and high-density interconnects. In addition, current packaging for III-V on Si devices is often limited to small component levels, such as semiconductor optical amplifiers or laser diodes. Flip-chip bonding is a well-established technology in the integrated circuits (IC) industry [2] and is favorable for the assembly of die-level PICs with high-density interconnects. Unlike electronic ICs, PICs require more accurate positioning and precise power dissipation. When flip-chip bonding different materials, for example, InP on Si, the difference in thermal expansion results in significant stress when cooling down after soldering, especially for larger dies. Laser soldering is suited for flip-chip bonding of complex PICs assemblies because of non-tactile heating, highly localized thermal energy, good accessibility, and short soldering times allowing a high-throughput process [3].

In this work, we propose a photonic flip-chip assembly concept for an InP (Indium Phosphide) PIC on a TriPleX (silicon oxide-nitride)[4] carrier using passive alignment and laser soldering in an automated fashion. A self-aligned structure is utilized for multiport optical inputs and outputs [5, 6]. Two laser soldering schemes are investigated for flip-chip bonding: through-silicon laser soldering and heat conduction laser soldering. Eutectic gold-tin (AuSn with 80/20 wt-%) solder pads were used which is the state-of-the-art solder metal composition. They are widely used for fluxless flip-chip assembly in optoelectronics packaging [7]. We experimentally demonstrate a 4 mm × 4.6 mm InP die with 58 electrical pads assembled onto a 16 mm × 8 mm TriPleX die based on this concept. Results are promising and provide a high-density, reliable interconnect assembly of InP on TriPleX.

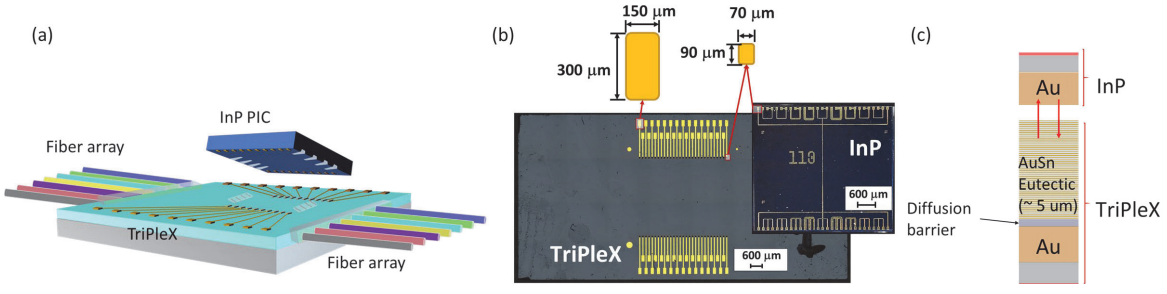

Fig. 1. Concept: (a) Schematic of a flip-chip assembled InP PIC on a TriPleX carrier that connects to fiber arrays; (b) Microscope images of TriPleX and InP test chips, the enlarged view is a schematic of a probing pad (150 µm × 300 µm) and a bonding pad (70 µm × 90 µm); (c) schematic of the metal stack of the bonding pad and solder pad.

CONCEPT

The photonic flip-chip assembly concept for an InP PIC on a TriPleX carrier is shown schematically in Fig.1 (a). Light is coupled from fiber arrays to waveguides on the TriPleX carrier, and vice versa. This is a standard technology on the TriPleX platform that is well-suited for fiber-to-chip coupling [4]. A passive self-alignment method is utilized for

coupling light from the TriPleX chip into the InP chip as reported in [5]. This self-alignment is done simultaneously and as a result of the flip-chip soldering process. This technique has been demonstrated to achieve interconnect density of 40 channels per mm and provides ± 2 µm alignment tolerance within 0.5 dB [6].

Electrical connections are required to drive the InP PIC. They also provide the mechanical connection between InP and TriPleX. A set of test chips are designed and fabricated to investigate the difference between the two soldering methods, as shown in Fig. 1 (b). The InP PIC is positioned and bonded onto the TriPleX carrier through subsequent laser soldering. We standardize chip layouts and interconnects using open standards [8], to use the same soldering scheme for different PIC designs. The InP chips measure 4 mm × 4.6 mm, with a thickness of 200 µm ± 20 µm. On the P-side of the chip, on two opposite sides, there are each 29 electrical pads (bonding pads) with a size of 70 µm × 90 µm at 150 µm pitch. For the test chips, these are electrically interconnected in triplets, as can be seen in Fig. 1 (b). The TriPleX test chip measures 16 mm × 8 mm, with a thickness of 525 µm ± 25 µm. On the TriPleX chip, bonding pads that match the size and location of their InP-chip counterparts are arranged on the top side of the TriPleX chip. Eutectic AuSn solder, about 5 µm thick, is applied on top of each bonding pad on TriPleX during fabrication, as shown schematically in Fig.1 (c). The bonding pads of the TriPleX chip are routed to larger probing pads at the outer edges for electrical testing and driving after assembly.

TECHNOLOGY AND SETUP

Two types of laser soldering schemes were used for reflowing the eutectic AuSn solder pads, as shown schematically in Fig.2 (a, b). The eutectic AuSn-pads have a melting temperature of 278 °C. One laser soldering scheme is through-silicon laser soldering using a 1475 nm central wavelength (CWL) laser source, the other scheme is heat-conduction laser soldering using a 975 nm CWL laser source. Regarding the first scheme, most of the laser power is transmitted through the TriPleX chip, and a smaller part is reflected or scattered, which is mostly determined by the refractive index contrasts between air, silicon, and silica and by the surface roughness. Taking the multiple reflections into account, we calculated that an average of ~60% of the laser power is transmitted through the TriPleX chip, which matches with experiments. As a result, the metal bonding pads directly absorb the thermal energy from the soldering laser. Notably, AuSn solder pads are heated up and melted in a laser-on-time of less than 1 ms. Due to the localized thermal energy, minimal thermal stress is inflicted on the PICs. The second soldering scheme is a standard laser soldering technique that is widely used in industrial applications [3]. Here, most of the laser power is absorbed by the TriPleX chip, and less part is reflected. Up to 70% of laser power is absorbed by the TriPleX chip. Heat is transferred from the thermal energy of the soldering laser, through the TriPleX chip, to the metal bonding interfaces. Multiple solder pads can be melted in a laser-on-time from a few hundred milliseconds to a few seconds.

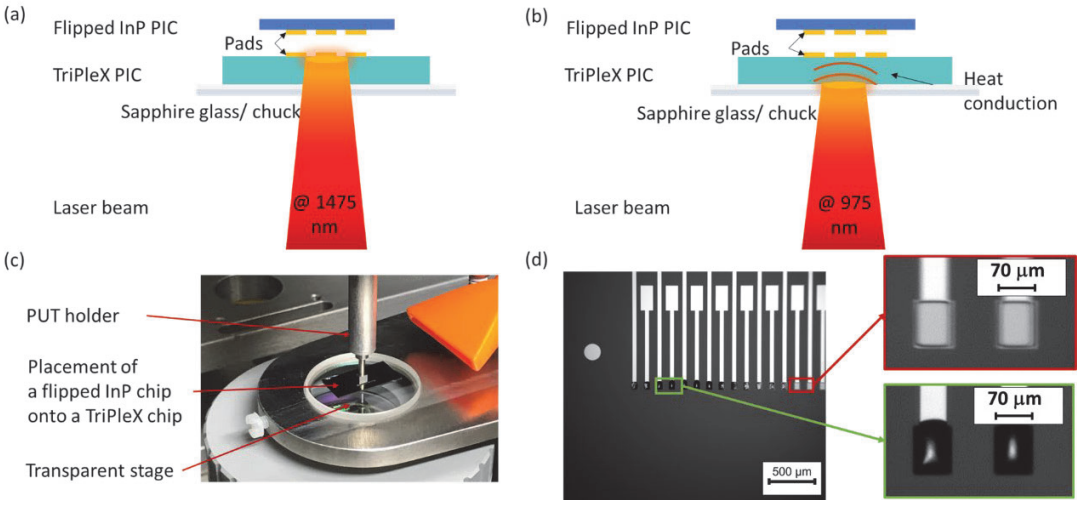

Fig. 2. Technology, setup, and assembly process: (a, b) Schematic of through-silicon laser soldering and heat conduction laser soldering; (c) Image of a flipped InP chip held by a pick-up-tool (PUT) and placed on top of the TriPleX chip on a transparent stage; (d) Microscope image of 16 bonding pads with eutectic AuSn solders on a TriPlex chip; the top enlarged view shows two bonding pads with original solders, the bottom one shows two bonding pads with reflowed solders after laser illumination.

RESULTS AND DISCUSSION

We conducted flip-chip bonding experiments for the test chips shown in Fig. 1 (b) with both types of soldering lasers. Fig. 2 (c) shows the laser-soldering-assisted assembly process based on an automated machine vision[9]. First, the TriPleX carrier is placed on a transparent sapphire glass chuck. Then, an automated pick-and-place tool

picks the flipped InP chip and moves it onto the pre-defined location of the TriPleX carrier. Fig. 2 (d) is a microscope image that shows wetted solders on the bonding pads and an alignment marker on the TriPleX carrier. This research machine integrates the two soldering laser sources to compare the two schemes. The laser beam is guided by a focusing optics system to the bottom side of the chip and melts the AuSn solder pads on the TriPleX chip, joining both chips.

As for the 1475 nm laser source, its spot diameter on the backside surface of the TriPleX chip has a size of ~340 µm. A pad-by-pad reflow scheme requires a laser-on-time of 0.3 ms. Regarding the 975 nm laser source, its spot diameter on the backside surface of the TriPleX chip has a size of ~330 µm. It sufficiently heats an area of about 1 mm at the location of solder pads in a laser-on-time of 3 s. The mechanical strength was checked by shear force testing as shown in Fig. 3. The measured shear force is ~6 N for both schemes, which meets the 2X MIL-STD 883 standards [10].

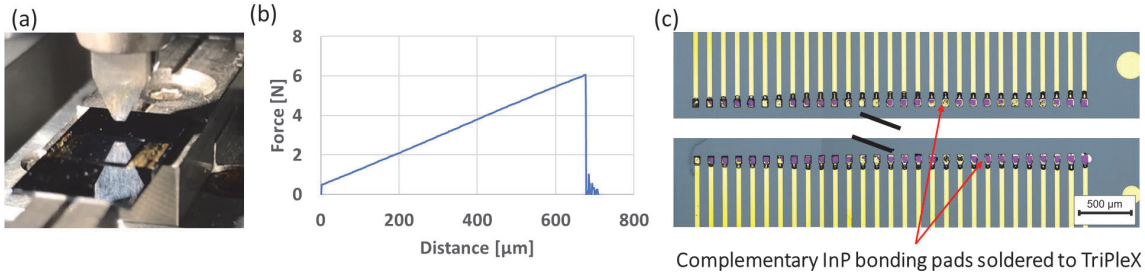

Fig. 3. Experiment results: (a). Image of an assembled InP on TriPleX chip under shear force test; (b). Shear force results; (c). Microscope image of two rows of 29 bonding pads each on TriPleX with complementary InP bonding pads after the shear test.

We presented a photonic flip-chip assembly concept for InP on TriPleX using two laser soldering schemes. The through-silicon soldering shows fast soldering time, lower power for solder reflow, and less thermal impact on PICs which is preferred over heat-conduction soldering, especially for large InP dies. These results indicate a significant step forward towards reliable photonic packaging for complex devices with high-density interconnects.

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References

[1] L. Carroll, J.-S. Lee, C. Scarcella, K. Gradkowski, M. Duperron, H. Lu, Y. Zhao, C. Eason, P. Morrissey, M. Rensing, S. Collins, H. Hwang, and P. O'Brien, "Photonic Packaging: Transforming Silicon Photonic Integrated Circuits into Photonic Devices," *Applied Sciences,* vol. 6, no. 12, 2016.

[2] E. Davis, W. E. Harding, R. S. Schwartz, and J. J. Corning, "Solid logic technology: versatile, high-performance microelectronics," *IBM Journal of Research and Development,* vol. 8, no. 2, pp. 102-114, 1964.

[3] W. Horn, "Welding and Soldering with High Power Diode Lasers," 2009.

[4] K. Wörhoff, R. G. Heideman, A. Leinse, and M. Hoekman, "TriPleX: a versatile dielectric photonic platform," *Advanced Optical Technologies,* vol. 4, no. 2, 2015.

[5] W. Tian, K. Wörhoff, R. Dekker, A. Khachikyan, C. Mittelstädt, J. v. Kerkhof, Y. Ren, R. Santos, K. Williams, and X. J. M. Leijtens, "Self-aligned flexible waveguides for interfacing flip-chip assembled InP photonic integrated circuits on SiN," in IEEE Benelux Chapter Annual Symposium 2021, Mons, Belgium, 2021.

[6] X. Leijtens, R. Santos, and K. Williams, "High Density Multi-Channel Passively Aligned Optical Probe for Testing of Photonic Integrated Circuits," *IEEE Photonics Journal,* vol. 13, no. 1, pp. 1-15, 2021.

[7] M. Hutter, H. Oppermann, G. Engelmann, L. Dietrich, and H. Reichl, "Precise Flip Chip Assembly Using Electroplated AuSn20 and SnAg3.5 Solder," in 56th Electronic Components and Technology Conference 2006, 2006, pp. 1087-1094.

[8] S. Latkowski, D. Pustakhod, M. Chatzimichailidis, W. Yao, and X. J. M. Leijtens, "Open Standards for Automation of Testing of Photonic Integrated Circuits," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 25, no. 5, pp. 1-8, 2019.

[9] "ficonTEC Service GmbH "; https://www.ficontec.com/.

[10] "MIL-STD-883," https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-STD-883/std883.pdf.