Compact 8×8 SOA-Based Optical WDM Space Switch in Generic InP Technology

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Desalegn Wolde Feyisa, *Student Member, IEEE*, Bin Shi, *Member, IEEE*, Rafael Kraemer, *Student Member, IEEE*, Nicola Calabretta, *Member, IEEE*, and Ripalta Stabile, *Member, IEEE*

***Abstract*—As the global internet protocol (IP) traffic volume growth puts more pressure on network connectivity, bandwidth and latency requirements, crucial network elements such as switches need continuous improvement. To this end, we report a monolithically integrated, ultra-compact 8×8 optical space switch based on semiconductor optical amplifier (SOA) gates, utilizing ultra-compact bends and denser SOA placement and demonstrating a strictly non-blocking broadcast and select (B&S) switch architecture on-chip. The switch circuitry comprises 80 SOAs, 112 multimode interference (MMI) splitters, and hundreds of waveguide bends and crossings integrated onto a 4.6×8 mm^2 generic indium phosphide (InP) die with I/O access on the same side. In addition, the SOA waveguide geometry is specifically optimized to improve output saturation power by 2 dB and enable WDM operation. The physical layer characterization shows lossless operation on-chip due to the three SOAs in a path that provides enough gain to compensate for on-chip passive losses. The best-case OSNR is higher than 40 dB. We perform static data signal routing with four-channel wavelength division multiplexed (WDM) data signals at 25 Gb/s and 35 Gb/s, resulting in a worst-case 2 dB power penalty on receiver sensitivity. Additionally, we dynamically switch data signals at bit rates up to 35 Gb/s obtaining a power penalty similar to the static routing. The recorded rising and falling times are 4 and 6.4 ns, respectively, suggesting this chip is suitable for packet-scale fast switching applications.**

***Index Terms*—Broadcast and select, dynamic routing, monolithically integrated, optical space switches, semiconductor optical amplifier.**

I. Introduction

THE steady exponential growth of global internet protocol (IP) traffic has continued for decades. Cisco predicts the worldwide IP traffic will reach 396 Exabytes per month by 2022, almost triple what we had in 2017 [1]. Similarly, global data center traffic is increasing with the demand for data center storage to accommodate big data, the Internet of things (IoT) and the abundance of cloud-based applications and services [2]. Moreover, a large volume of data center traffic is generated within the data center itself [3]. As the number of interconnected nodes and the traffic volume increase, we encounter increased demand for more connectivity per switch and capacity per switch port. Hybrid methods utilizing optical links and electronic switches have been widely used for point-to-point data center interconnects. These methods are facing challenges for two main reasons. First, scalability constraints are an issue as electronic communication bandwidth approaches its physical limits. Second, optical-to-electrical and electrical-to-optical converter circuits increase the footprint, cost and power consumption, posing an additional challenge as data centers scale. A viable solution to these problems is to use architectures that utilize optical switches [4], [5]. Flat data center architectures based on an optical network, instead of electronic switch-based hierarchical networks, have been proposed, offering notable advantages in latency and power consumption [6]. In these scenarios, fast and bit-rate agnostic optical switches that can scale to several port counts play a crucial role.

Table I summarizes optical switch technologies, comparing their key performance indicators (KPIs), such as response time, insertion loss, extinction ratio (ER), footprint, optical signal to noise ratio (OSNR), power consumption, bandwidth, scalability and power penalty [7], [8], [9], [10], [11], [12], [13], [14]. Various optical switching technologies have been proposed so far with significant improvements. However, realizing an optical switch that shines in all metrics has been challenging. Most optical switch (OS) technologies struggle with high insertion loss, latency and power penalty. Switches based on micro-electromechanical systems (MEMS) guarantee low insertion loss, low power consumption and ease of scale-up to large port counts. Several hundred port count switches are easily realized with 3-dimensional (3D) MEMS [8]. Looking into integrated solutions, Silicon has an excellent thermo-optical (TO) coefficient, which helps tune the phase easily and realize low energy switching functionality on a Silicon photonics platform [13]. More recently, a lossless MZI switch in Si_3N_4 has been demonstrated by monolithically integrating an Erbium-doped waveguide amplifier (EDWA) on the Si_3N_4 platform [14]. This work provides a good alternative platform to the optical switching functionality, where amplification is done on a chip with EDWA integrated with the waveguide in order to compensate for passive losses. However, the switching speed of TO- and MEMS-based switches are in order of microseconds. While these technologies are attractive for application in more static

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The authors are with the Institute of Photonic Integration, Eindhoven university of Technology, 5600MB Eindhoven, The Netherlands (e-mail: d.w.feyisa@tue.nl; b.shi1@tue.nl; r.magalhaes.gomes.kraemer@tue.nl; n.calabretta@tue.nl; r.stabile@tue.nl).

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TABLE I
STATE OF THE ART P CANDIDATE SWITCHING TECHNOLOGIES

Ref.	Switch Technology	Port size	Actuation Technology	ER (dB)	OSNR (dB)	Insertion loss (dB)	Circuit size (mm^2)	Penalty (dB) @Bitrate (Gb/s)	Scalability challenges	Speed
[8]	MEMS	512×512	Electrostatic	-	-	6	197×243×140*	-	-	100µs
[7]	Micro ring	4×4	TO	52	-	2.3	1.5 × 2.4	-	Limited bandwidth	10µs
[12]	P/n junction	2×2	EO	-	-	30	-	0.4@40	loss	60 ps
[10]	SOA	16×16	EO	-	35.5	28.2	13.2×4	4.9 @10	ASE noise, loss	5 ns
[13]	MZI	8×8	TO	30	-	10.8	3×8.2	-	ER, loss	-
[14]	MZI	1×4	TO	-	-	Lossless on-chip	-	1.9@4λ×60	EDWA footprint	-
[11]	MZI-SOA	4×4	Hybrid	>50	47	1.3	4×6	<0.5 @10	Number of electrodes	6 ns
[9]	SOA	8×8	EO	>30	>40	lossless	8×8	0.9 @10	ASE	-
This work	SOA based	8×8	EO	37.6**	42.5**	Lossless on best path	4.6×8	2 @ 4×35	Loss, ASE	6 ns

ns-nano second, ms-millisecond, µs-microsecond, ps-pico second *Unit is in mm^3 ** for a representative path

chunks of the network, modern, highly dynamic data center traffic requires faster optical switches.

Electro-optically (EO) actuated switches are attractive due to their fast response speed in a few nanoseconds. While these come at the cost of higher insertion losses when implemented on Silicon via vertical p/n junction [12], their realization on Indium Phosphide (InP) platform is very suitable for high-performance optical switches. In particular, circuits based on semiconductor optical amplifiers (SOAs) offer simultaneously switching and amplification, have broad bandwidth and are suitable for compact and large-scale integration [15]. However, splitting losses and amplified spontaneous emission (ASE) noise building-up from SOA needs consideration for SOA cascades in large radix photonic integrated switches [10]. A hybrid switch implementation that includes Mach-Zehnder Interferometers (MZIs) and SOA-based switches has been demonstrated with good OSNR and lossless operation [11]. It uses the best of SOAs and MZIs features: while using MZIs avoids splitting loss, the SOAs guarantee high ER. However, MZIs result in a more significant form factor and more complicated switch control than operating SOA-only-based photonic integrated switches. In this work, we stick to a purely SOA-based switch design to take advantage of the SOA properties and, at the same time, circumvent intrinsic drawbacks by using a combination of appropriate architecture, optimized component designs and circuit operation.

This paper reports an ultracompact 8×8 port count strictly non-blocking wavelength division multiplexing (WDM) space switch. We realize the circuit with InP generic technology and deflect from standard rules to decrease form factor and preserve signal integrity: A novel SOA waveguide design, densely packed SOAs and ultra-compact routing elements are introduced. Additionally, we use the physical layer characterization and dynamic switching operation to verify that these novel design concepts improve the SOA-based WDM switch compactness and performance despite generic fabrication processes. The organization of the paper is as follows. Section II describes the switch architecture and circuit design, including the novel components and their integration. Then, Section III presents the switch physical layer evaluation, accounting for path-dependent loss, coupling loss, path gain and component loss contribution. Furthermore, we emphasize path losses and identify the pitfalls in the design to propose future improvements. Section IV discusses the experimental setup to measure the data signal routing in both static and dynamic operations to evaluate the switch performance and its suitability for packet switching.

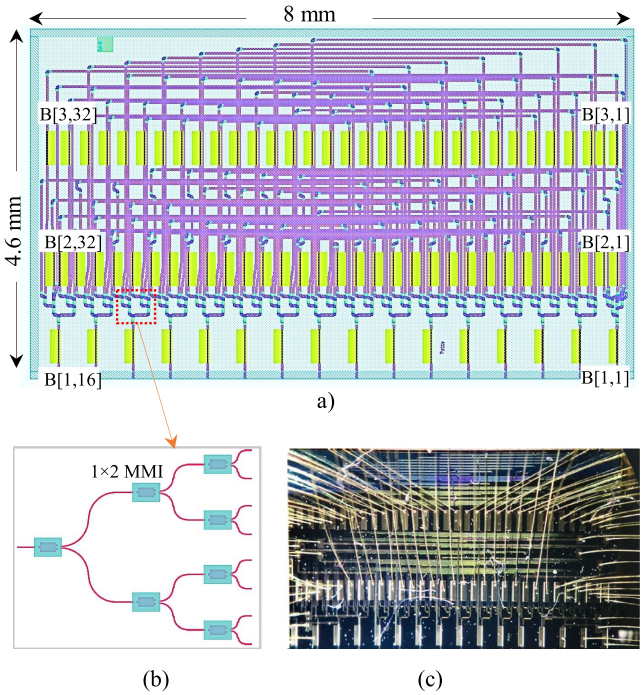

Fig. 1. (a) Switch schematic with SOA blocks of B [1,1] to B [1, 16] at the input/output and B [2,1] to B [2,32] and B [3,1] to B [3,32] representing the path select SOAs b) zoom out diagram for implementation of 1:8 splitter c) Fabricated and wire-bonded chip photograph.

II. CIRCUIT INTEGRATION AND ARCHITECTURE

A. Optical Switch Architecture

Fig. 1(a) illustrates the mask layout of the 8×8 photonic integrated switch, designed to function as a strictly non-blocking

broadcast and select (B&S) switch, with 64 paths to connect any input to any output port independently. One SOA for each path is used as a gate for path selection, while preamplifiers and additional boosters are utilized to compensate for path losses and coupling losses at the inputs and outputs. This architecture requires N^2+2N SOAs for switch radix N, where the first term, N^2, stands for the 64 path selection SOAs and the second term, $2N$, represents 16 SOAs connected at the inputs and outputs when $N=8$. We implement the 1:8 splitter/combiner stage using a three-stage cascaded 1:2 Multimode interference (MMI) splitters/combiners, realizing a tree of 7 MMIs per each, as shown in Fig. 1(b). Indeed, the total number of MMIs on the chip for this architecture is given by $2N(N-1)$, which means we have 112 MMIs integrated into the chip. The number of MMI in a path is $2log_2(N)$, which means that for $N=8$ (this case radix), each path traverses 6 MMIs. Compared to other competitive multistage architectures, such as Banyan and Benes, the proposed architecture provides strictly non-blocking switching functionality. Additionally, as a B&S switch has only one switching stage, the number of SOAs switching simultaneously, even when the switch is fully loaded, is minimal, which leads to reduced energy consumption compared to a multistage architecture. Instead, extra loss from the MMI splitters and combiners in a path is induced; however, this may be overcome by introducing additional booster/preamplifier SOAs in the architecture at input/output at the cost of an increased noise figure. For a radix N $<$ 16, this loss can still be compensated by 3 SOAs in a path, which means that interconnectivity of 8×8 is feasible with this architecture.

The inputs and outputs of this switch are placed on the same side to ease input and output coupling with one fiber array and enable a simplified packaging process. Nevertheless, this also comes at the expense of integrating hundreds of waveguide bends and crossing on-chip, contributing to path loss. With this topology, as in Fig. 1(a), the SOAs are divided into 3 blocks: the first block is the16 preamplifier/boosters SOAs for the 8 input and 8 output, as shown at the bottom, labeled from B[1,1] to B[1,16]; the second and the third blocks at the middle and top are the 64 SOAs for the 8×8 path selection, labeled as from B[2,1] to B[2,32] and from B[3,1] to B[3,32].

B. Circuit Design and Fabrication

Fig. 1(c) shows the photograph of the SOA-based switch circuit realized within the generic InP platform and fabricated by the SMART photonics foundry [16]. The epitaxial growth includes multi-quantum well (MQW)-based SOAs co-integrated with passives onto three rows on-chip. The active region of the SOA used in this circuit is 450 μm long and 3 μm wide. The SOA width is wider than the standard 2 μm device to increase output saturation power and improve the switch performance for a WDM signal input. Carriers in an SOA active gain region become depleted as the optical power increases, causing gain reduction and power saturation. This mechanism hinders WDM operation by limiting the power per channel that can be launched into an SOA-based circuit, resulting in deteriorated OSNR. Specifically, the output saturation power is directly proportional

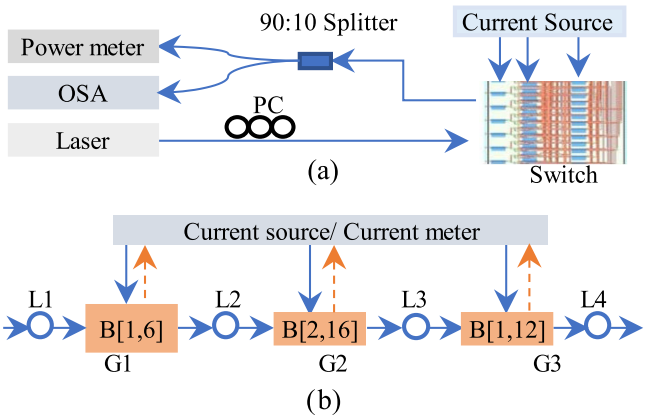

Fig. 2. (a) Experimental setup for loss measurement (b) Typical path operation to measure path loss, coupling loss and path gain.

to the effective mode area A as given in [17]:

$$P_{o,sat} = \left(\frac{G_o \ln 2}{G_o - 2}\right) A \left(\frac{h\nu}{a\tau}\right) \quad (1)$$

where G_o is the unsaturated gain, $h\nu$ is the photon energy, a is the differential gain and τ is the carrier lifetime. The width dependency of saturation is dependent A, which is calculated as $A = wd/\Gamma$, where w and d are the width and thickness of the active region of the SOA, and Γ is the optical confinement factor. An increase in width is expected to increase A, resulting in higher output optical saturation power $P_{o,\,sat}$.

We implement the passive straight waveguides via wide shallow etching. The mode profile size and shape in the 3 μm SOAs are tapered down to 2 μm straight waveguide through adiabatic tapers. The circuit uses deep etching for waveguide micro-bends and multimode interference (MMI) splitters/combiners. In particular, we utilize whispering gallery mode steep bends with a bending radius of 20 μm to allow a very compact design [18]. An antireflection coating is applied to the chip facet to minimize the reflections at the I/Os. Finally, we mount the chip on a copper heat sink and the SOAs are wire-bonded to a printed circuit board (PCB) to facilitate cooling and enable connection to current drivers.

III. Physical Layer Switch Characterization

A. Experimental Setup for Loss Analysis and Methodology

We build a simple setup in Fig. 2(a) for the experimental assessment of the physical performance of the device. A water cooler is used to maintain the chip operating temperature constant at 18 °C throughout the measurement to avoid frequency drift and/or gain perturbation due to the heating effect by biasing multiple SOAs. When fully loaded, the total power dissipation of the SOAs of the switch is about 2.5 W, which a Peltier can manage. Therefore, in a packaged switch, a Peltier can replace the water cooler. We align input and output lensed fibers via two adjacent three-axis stages and use an optical spectrum analyzer (OSA) to monitor the received signal spectra. Intrinsic to MQW, the SOAs are polarization-sensitive; therefore, we use a polarization controller (PC) at the input side to optimize the

input signal state of polarization (SOP) to the SOAs fabricated on the chip. The characterization in this section is carried out with a continuous wave laser source at a wavelength of 1549.32 nm, with 0 dBm peak power. We set the current source to drive the SOA with desired bias current.

Fig. 2(b) shows a typical path from one input to one output. $LC = L1{+}L4$ and $LP = L2{+}L3$ represent the coupling and path losses, respectively, while the gain is the contribution of 3 SOAs (shown in orange boxes) in a line, given as *G1*, *G2,* and *G3*, for the presentative path with SOAs B[1,6], B[2,16] and B[1,2]. When all SOAs are provided with transparency current, the difference between the output and input signal spectrum gives the fiber-to-fiber path loss ($F2F = G{+}LC{+}LP$, with $G = 0$), since the SOAs neither absorb nor amplify the signal at transparency. The transparency currents are estimated to be 14 mA by monitoring the voltage change through a bias-tee [19]. Then we acquire the SOA cascade total gain $G = G1{+}G2{+}G3$ by measuring the difference of the fiber to fiber losses between the case when the SOAs are set at specific operating currents and the case when SOAs are at transparency. The average gain for representative paths is approximately 31 dB when 60 to 70 mA currents drive the SOAs.

We can determine the on-chip component loss by subtracting the fiber-to-chip coupling loss from fiber-to-fiber (F2F) losses. Furthermore, the fiber-to-chip coupling loss is determined by launching optical power p to the input, monitoring the generated current I in the booster/preamplifier SOAs and calculating the coupling loss from $I = \mu RP$ where R is responsivity and μ is coupling efficiency. However, since it is challenging to determine R in a system of cascaded integrated SOAs, we determined the coupling efficiency differently.

Since the fiber-to-fiber signal loss encompasses coupling loss at the chip facets LC and net on-chip gain ($Lnet = G{+}LP$), coupling loss LC can be obtained by subtracting net on chip gain from fiber to fiber transmission F2F ($LC = F2F{-}Lnet$). To determine on-chip component loss, we first connected the laser to the input port and recorded photocurrent I_{in} at the gate of SOA B [1,6]. Then biasing B [1,6] at the transparency current of 14 mA, we measured the generated photocurrent at B [2,16], I_{inm}. After that, photocurrent I_{out} at B [1,12] was recorded with the light signal applied from the output port. Then biasing B [1,12] at the transparency current, a current I_{outm} was measured at the gate of the middle SOA. Finally, we calculate the on-chip loss LP using Eq. (2), assuming the SOAs have a uniform R finding a ratio of currents. It cancels out the effect of R and gives a good approximation of loss between SOAs without even determining the value of R.

$$LP = 10 * \log\left[\left(\frac{I_{inm}}{I_{in}}\right) * \left(\frac{I_{outm}}{I_{out}}\right)\right]. \quad (2)$$

Finally, the average end-to-end coupling loss ($F2F{+}G{+}LP$) was determined as 9 dB.

B. Path Loss, OSNR and Component Losses

The expected path-dependent component loss contributions are estimated from the number of components in a path and component losses in Table II [18], [19], [20]. Determining the measured and expected on-chip loss helps evaluate the chip and component performance to match the measured and expected F2F signal loss, which, as mentioned above, includes the SOA gain, the on-chip component losses and the fibers-to-chip coupling loss.

TABLE II
COMPONENT LOSSES

Component	Loss per component	Reference
Waveguide bends	0.2 dB	[18]
Waveguide crossovers	0.25 dB	[19]
Multi-mode interference (MMI)	3.5 dB	[20]
waveguide	3 dB/cm	[19]

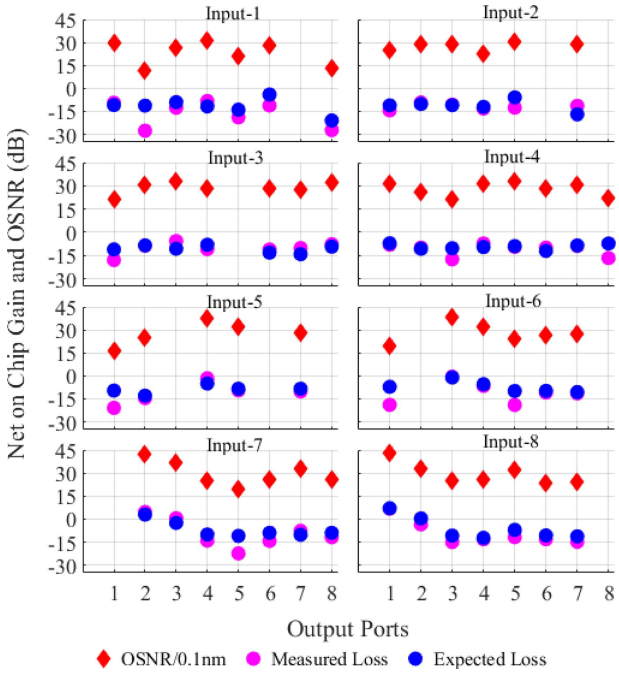

Fig. 3. Expected and measured on chip net loss and optical signal ratio for all working paths with both electrical and optical connections.

Fig. 3 portrays the expected and measured net on-chip gain and the OSNR, with blue circles, magenta circles, and red diamonds, respectively. The paths missing in Fig. 3 are due to missing electrical or optical connections. Paths 1-to-7, 2-to-6, 3-to-5, 5-to-3, 5-to-8, 6-to-2, 7-to-1 and 8-to-8 do not have an optical connection due to localized waveguide damages. Paths 6-to-8 and 8-to-8 have no electrical connection due to a poorly made wire bonding. The variation of net on-chip loss depends on the number of optical components in the path and the performance of each component, which varies from one path to another. The best-case on-chip gain is 8 dB in the shortest path, and the worst-case loss is -12 dB due to path-dependent loss. This does not include the paths with local defects, for which the losses go down to -20 dB.

For paths without defect, the predicted loss compares well to the measured loss, within 4dB variation, confirming the devices work within design expectations. Some other paths present problems, like minor defects created during wire bonding or

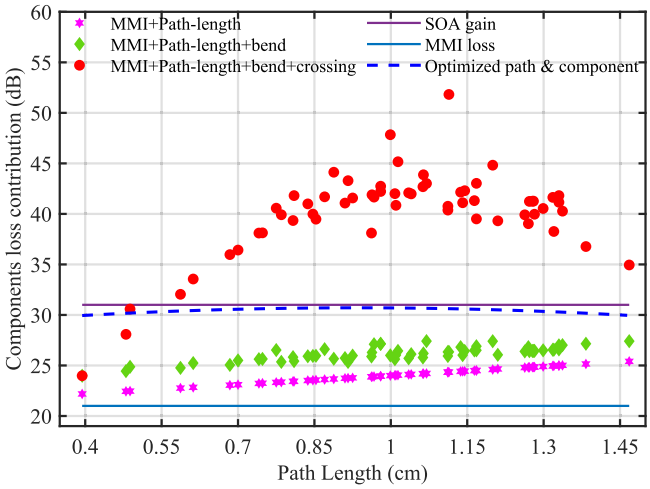

Fig. 4. Loss contribution break down by components and comparison to the case when path routing and component loss is optimized.

fabrication. Other variations may occur for a slight variation in excess losses for the passive components and due to the non-uniformity of the SOAs. A calculation made by excluding paths with identified defects shows that the average measured F2F loss is -18.54 dB, and the expected average is -17.75. The difference between the measured and anticipated F2F losses (measured minus expected) is -0.79. The variation shows a slight underestimation of the expected loss.

The OSNR has also been measured by comparing the optical signal peak at the switch output to the noise floor at the OSA with 0.1 nm resolution bandwidth. It is very notable from Fig. 3 that the OSNR follows the path loss pattern. Paths with higher losses have limited OSNR. Apart from the power budget requirements, it is necessary to reduce the path losses to achieve a better OSNR, which is a critical factor for switching functions without compromising signal integrity.

The optical crosstalk is estimated based on our prior work [10] and applied to the existing on-chip architecture. The linear crosstalk in SOA-based switches comes from the SOA gating and the waveguide crossing leakage. The latter is the most dominant effect [21]. N paths can be operated simultaneously in the fully loaded, strictly non-blocking N×N switch. Given a crosstalk for InP waveguide crossing of -35 dB [22] and for N = 8, up to N-1 = 7 waveguide crossings contribute to the optical crosstalk, which contributes 8.5 dB to the crosstalk and deteriorates the optical crosstalk down to about -26.5 dB.

The component dependency of the path loss is shown in Fig. 4, which is plotted by rearranging the path length from the shortest to the longest, taking different components on each path into account. The loss contribution from the MMI and waveguide path loss (MMI+Path-loss), from MMI, path loss, and bending (MMI+Path-loss+bend), and from MMI, path loss, bending, and crossing (MMI+Path-loss+bend+crossing) are depicted in magenta stars, green diamonds, and red circles, respectively. A constant loss of around 21 dB coming from the 6 MMIs, as shown in the blue line, present in each path is inherent to the architecture and hence unavoidable. And the average gain of the SOAs in one path is about 31 dB, as mentioned in the last section and shown as a solid purple line in Fig. 4. The longest path is around 1.5 cm: for such length, the loss contribution given by the waveguide is less than 4.5 dB considering an average loss per unit length of 3 dB/cm.

Similarly, the average number of waveguide bends in a path is around 10, contributing to approximately 2 dB loss at 0.2 dB per bend. However, from the trend of the loss plot with crossing included (red dots), we can observe that the number of crossings overwhelmingly influences the path-dependent loss. Waveguide crossings contribute up to 24.5 dB loss on the worst path (which contains 98 of them) and 14 dB loss on average, for an average total contribution of up to 73% on the path-dependent losses. Optimization of crossing design to reduce its insertion loss and an optimal path routing in the circuit design could significantly improve the overall switch performance by reducing path losses, which allows the use of shorter SOAs with consequent lower ASE. In the worst case, the utilized architecture requires only N^2-$2N$ crossings (if the path routing is the optimum possible). Notable performance improvements have recently been reported by the foundry [23]. The new enhancements report waveguide loss as low as 1.5 dB/cm and waveguide bend loss as low as 0.1 dB. It is also possible to reduce waveguide crossing loss as low as 0.15 dB using optimized designs such as taper-assisted crossing, MMI-based crossing and inverse-designed crossing [24], [25], [26]. We can already achieve lossless operation for the worst path by assuming optimum path routing and optimized loss components, as highlighted by dashed blue lines in Fig 4: The red quasi-bell circles become flat (blue dashed line) since path-dependent losses are lower and more uniform. As we can see from the dashed blue line in Fig. 4, the projected path loss variation is down to 3 dB, which can be easily equalized by tuning the SOA gain for all paths.

IV. Data Signal Transmission on The Switch

In this section, we demonstrate two sets of data routing experiments to test the effect of the insertion and use of the photonic integrated SOA-based switch on signal integrity. The first experiment is static data signal routing. A WDM signal is loaded to the switch to test the power penalty introduced by the switch on the WDM signal integrity. The second experiment is performed, switching the SOA on and off quickly and periodically to test the dynamic switching effect on the overall performance. For this purpose, we established an experimental setup shown in Fig. 5 that we use for both experiments with minor changes.

A. Experimental Setup for Data Transmission

Fig. 5 schematically depicts the experimental system setup established to verify the proper functionality of data routing operation. For the static routing experiment, four laser outputs (Keysight N7714A) with a channel spacing of 1.6 nm at wavelengths 1549.32 nm, 1550.92 nm, 1552.52 nm, and 1554.13 nm are combined by a 4 to 1 combiner and fed to the optical transmitter (SHF 46210 C) for modulation. The Mach Zehnder modulator (MZM) in the transmitter modulates

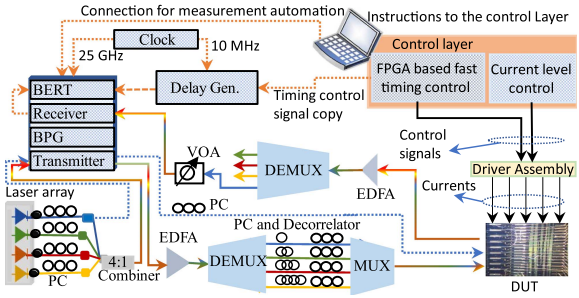

Fig. 5. Schematic of the experimental setup used for static and dynamic data signal routing on the switch. Connections indicated by the dotted blue lines connections are used only for the dynamic experiment. PC-polarization controller, DUT-Device under test, EDFA-Erbium doped fiber amplifier, VOA-Variable optical attenuator, BERT-Bit error rate tester, BPG-Bit pattern generator.

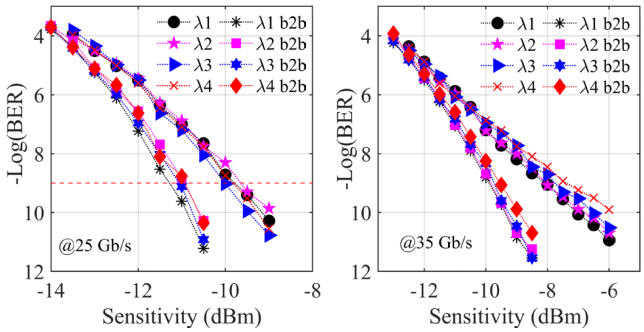

Fig. 6. Static wavelength division multiplexed data signal routing result at bit rates 25 Gb/s and 35 Gb/s for path 6 to 3.

the signal with NRZ-OOK PRBS-31 at 25 Gb/s and 35 Gb/s. Since the MZM is polarization-dependent, we optimize each channel polarization individually via demux and mux. We use an Erbium-doped fiber amplifier (EDFA) to compensate for the insertion loss of the transmitter. The WDM signal is then demultiplexed, decorrelated in time, employing different fiber lengths, polarization controlled, and multiplexed. The alignment to and from the chip is executed via two three-axis stages. The signal suffers power loss due to on-chip loss and coupling loss. In addition, the (de)multiplexing also takes out some power. Hence, an EDFA amplifies the signal to obey the receiver sensitivity power requirement. The dotted connections are only for dynamic routing experiments and ignored for the static measurement. The control layer provides a constant current to the switch chip for this static measurement.

For the dynamic measurement, the most crucial difference from the static experiment is that the control layer and the delay generator are exploited to enable the dynamic switching of the SOAs on-chip. The measurement was realized using a custom-made driver assembly and control system. The control system includes Field programmable gate arrays (FPGAs) (Pulseblater128) based switching control system and a microcontroller (Atmega1280) based current level control. The user sets necessary settings through a Graphical User Interface (GUI)-based control software that sends control signals and current level information to the driver assembly. A driver assembly is built from a series of current drivers (LMH6526) and digital-to-analog converters (AD8804) and generates analog direct current (DC) or on/off current levels varying from 0 to 100 mA based on the digital input to the DAC from the GUI. Therefore, through a high-level control layer software, we can set instructions telling which path to connect, when to connect it, and how much current to provide to each SOA. A copy of the timing signal triggers a delay generator (Stanford Research Systems Model DG645) that synchronously generates a gating signal for the bit error rate tester (BERT) to investigate the switched signal in a synchronized time window in burst mode.

B. Static Routing

For this measurement, we set each laser channel power at 11 dBm. The 4 to 1 combiner and multiplexer add around 9 dB loss. Hence, around 8 dBm signal enters the transmitter. The transmitter introduces 15 dB insertion loss; hence, the output power is -7 dBm after modulation and polarization optimization. The EDFA provides 8 dB gain to overcome the transmitter, polarization controller and decorrelator losses. The final input power from the lensed fiber is -3 dBm. The receiver sensitivity for the receiver (SHF 120100 B) is -14 dBm, and the threshold is 3 dBm. And another EDFA just before the receiver amplifies the signal to match this sensitivity requirement. Fig. 6 designates the channel sensitivity of the back-to-back (B2B) and switched NRZ-OOK WDM signal at 25 Gb/s and 35 Gb/s line rate measured for the representative path from input 6 towards output 3. The path is established by turning on SOAs B[16], B[216] and B[112]. All received channels offer error-free routing at a 10^{-9} bit error ratio (BER) with a worse case 2 dB (for λ4) power penalty at 35 Gb/s. At 25 Gb/s, the power penalty is even smaller, with a worst-case penalty of 1.5 dB. For both 25 Gb/s and 35 Gb/s, the performance from channel to channel at the same bit rate does not show a significant difference: the SOA performance does not vary within the 6.4 nm bandwidth. We expect it is possible to add more channels when the setup power budget allows us to exploit the broadband nature of the SOAs fully. We observe that the BER power penalty is higher at a higher bit rate as the higher bit rate is more susceptible to slow gain recovery effects [27]. In this experiment, the achieved power budget at the input (-3 dBm), which results in -8 dBm at the chip facet, after the coupling loss, has allowed us to operate within a region that gives a good compromise between noise and gain saturation. At this input power we could observe the effect of gain saturation, especially at 35 Gb/s; however, the nonlinear phenomenon is not strong. We have already demonstrated an input power dynamic range (IPDR) of 10 dB within a 1.5 dB power penalty with 4 WDM channels (power varying from -5 dBm to 5 dBm at the lensed fiber inputs) at a 12.5 Gb/s line rate [28], showing that the input power variation can be tolerated by the switch, with application possible also in reconfigurable optical front-haul networks.

C. Dynamic Routing

We study fast reconfigurability and packet switching capability by sending time-slotted current to the SOAs to turn the SOA on-off dynamically. A constant current drives the booster and preamplifier SOAs at the input/output. In contrast, the on-off

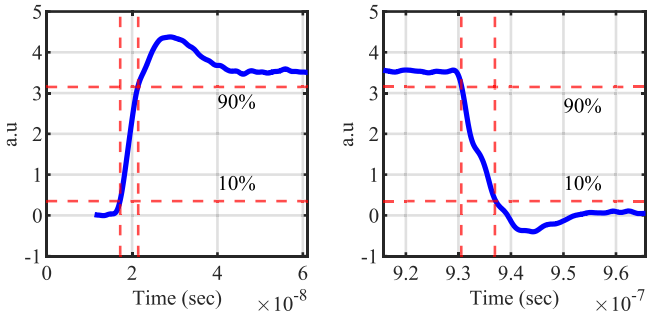

Fig. 7. Rising and falling time of SOA measured as the time it takes to reach from 10% to 90% of the peak and vice versa.

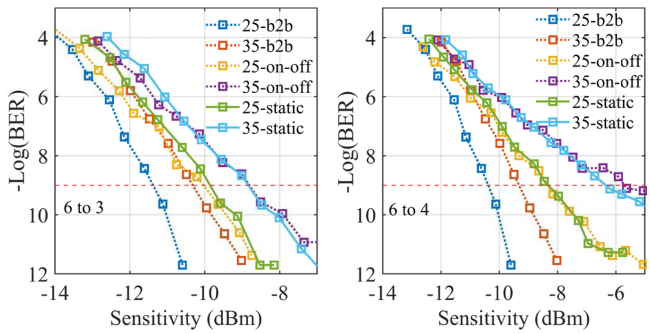

Fig. 8. Static and dynamic routing bit error ratio measurement result comparison at bit rates of 25 Gb/s and 35 Gb/s for paths 6 to 3 and 6 to 4.

current drives the middle SOAs to realize the dynamic switching functionality. Each time slot has an on-time of 950 ns and a guard band of 50 ns. Two periodically repeating time slots are created following Round-Robin scheduling. The optical signal is sent over path 6 to 3 at the first time slot, while during the next time slot, it is sent over path 6 to 4. Fig. 7 shows the rising and falling time of the signal switched on path 6 to 3. The received signal rising and falling time is around 4.2 and 6.4 ns, respectively.

Fig. 8 shows the bit error rate measured for paths 6 to 3 and 6 to 4 under dynamic and static conditions at 25 Gb/s and 35 Gb/s. We detect the signal during its on-time in a time window selected by the delay generator connected to the BERT gating terminal. A copy of the timing signal triggers the delay generator. The delay generator then produces a pulse of 750 ns to trigger the BERT. As can be observed from Section III Fig. 3, compared to paths 6 to 3, paths 6 to 4 has more path loss and experience more degradation in OSNR, explaining the increased power penalty for path 6 to 4 in Fig. 8.

D. Energy Consumption

At 70 mA bias current and a voltage of 1.5 V for each SOA, the switching power consumption per path is 315 mW. The maximum power consumption when all paths are fully connected is 2.52 W. At 35 Gb/s, the switching energy cost is 9 pJ/bit. If we consider the case of 4 WDM channels at 35 Gb/s, the energy cost is lowered to 2.25 pJ/bit. If we use the broadband nature of SOAs and put more channels, the energy cost to switch a bit can even be significantly lower. This energy consumption shows a clear advantage over the hybrid approach. For instance, a typical 4×25 (100G) optical transceiver requires 3.5 W power, and two of them needed for a path require 7 W [29]. Therefore, optical switches based on SOA have the potential of switching with low power consumption.

V. Conclusion and Future Outlook

This paper presents a densely integrated, strictly non-blocking switch design with optimized SOAs enhancing the output saturation power. The bit rate achieved and the low power penalty introduced by the chip show that this architecture, combined with the exploited more resilient SOA design and ultra-compact microbends, can achieve good signal integrity for WDM operation in a very compact footprint. Regardless of the integration density, the components worked following the design expectation. The setup power budget mainly limits the switch scalability investigation. And a higher sensitivity receiver would allow more channels and higher line rates.

Scalability issues of InP optical switches may originate from the built up noise and losses, can be relaxed by minimizing losses. This in fact would in turn minimize the gain required, allowing for the use of shorter SOAs, which generate lower ASE. Newly enhanced component performance has recently been released by the foundry [23]: waveguide loss was reduced down to 1.5 dB/mm, and SOA gain per unit length improved up to 30 dB/mm. Together with component design optimization, improved process technology promises room for further scalability. Additionally, the InP technology provides monolithic integration of active and passive components and enables nanosecond scale fast optical switches, making it attractive for switching technology in highly dynamic emerging data center traffic. Finally, the new InP membrane technologies, like IMOS (InP membrane on Silicon) provide higher integration density and plan to migrate to a generic foundry model [30].

Finally, using on-chip and off-chip spot-size converters, in tandem with packaging, can reduce coupling losses and shorten the time required for testing. From an electrical performance point of view, placing driver electronics near the photonic circuit more intimately with matched impedances and co-packaging can reduce the switching time to sub-ns, as theoretically expected from the MQW-based SOAs.

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Desalegn Wolde Feyisa (Student Member, IEEE) received the B.S. degree in electrical engineering (communication stream) from Adama Science and Technology University, Adama, Ethiopia, in 2013, the joint master's degree in photonic integrated circuits, sensors, and networks from the Sant'Anna School of Advances Studies, Pisa, Italy, and in electrical engineering from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2020. He is currently working toward the Ph.D. degree with the Electro-Optical Communication Group, Eindhoven University of Technology. His research interests include high speed and energy efficient optical switches.

Bin Shi (Member, IEEE) received the B.S. degree in optical information science from the China University of Mining and Technology, Xuzhou, China, in 2014, the M.S. degree in lasers and photonics from Ruhr University Bochum, Bochum, Germany, in 2017, and the Ph.D. degree from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2022. He is currently a Post-doctoral Researcher with Eindhoven Hendrik Casimir Institute (formerly IPI), Eindhoven University of Technology. His research interests include photonic neural networks, photonic integrated circuits, optical switches, and optical signal processing.

Rafael Kraemer (Student Member, IEEE) received the B.S. and M.S degrees in electrical engineering and computer engineering from the Faculty of Engineering, University of Porto, Porto, Portugal. He is currently working toward the Ph.D. degree with the Electro-Optical Communication Group, Eindhoven University of Technology, Eindhoven, The Netherlands. His research interests include multiband optical systems and ultra-wideband optical switching engines.

Nicola Calabretta (Member, IEEE) received the B.S. and M.S. degrees in telecommunications engineering from Politecnico di Torino, Turin, Italy, in 1995 and 1999, respectively, and the Ph.D. degree from the COBRA Research Institute, Eindhoven University of Technology, Eindhoven, The Netherlands, in 2004. From 2004 to 2007, he was a Researcher with Scuola Superiore Sant'Anna University, Pisa, Italy. He is currently an Associate Professor with the Institute of Photonic Integration, Eindhoven University of Technology. He has coauthored more than 490 papers published in international journals and conferences and holds five patents. His research interests include smart optical datacenter and telecom optical networks, optical processing, optical packet switching, semiconductor optical amplifier based optical switching and processing.

Ripalta Stabile (Member, IEEE) received the master's degree in electrical engineering from the Politecnico of Bari, Bari, Italy, in 2004, and the Ph.D. degree in nanoscience from National Nanotechnology Laboratory, Lecce, Italy, in 2008. In 2009, she moved to COBRA Research Institute, Eindhoven University of Technology, Eindhoven, The Netherlands, where she was appointed as a Postdoctoral Researcher. She is currently an Associate Professor with the Institute of Photonic Integration (formerly COBRA), Eindhoven University of Technology. Her research interests include design, simulation, nanofabrication, and characterization of organic and inorganic photonic devices. She is an Expert in Indium Phosphide (InP) large-scale photonic integrated circuits based on semiconductor-optical-amplifiers design for next generation optical networks and on-chip photonic neural networks.