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PO_x/Al_2O_3 stacks for surface passivation of Si and InP

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ABSTRACT

Passivation of semiconductor surfaces is crucial to reduce carrier recombination losses and thereby enhance the device performance of solar cells and other semiconductor devices. Thin-film stacks of phosphorus oxide (PO_x) and aluminum oxide (Al_2O_3) have recently been shown to provide excellent passivation of semiconductor surfaces, including crystalline silicon and indium phosphide, and can also be highly interesting for passivation of other semiconductor materials such as Ge and III-V semiconductors. On silicon, the excellent passivation is attributed to the combination of a high positive fixed charge and a very low interface defect density. On InP nanowires, application of the PO_x/Al_2O_3 stacks improves charge carrier lifetime threefold as compared to unpassivated nanowires. In this work, we review and summarize recent results obtained on PO_x/Al_2O_3 stacks for semiconductor surface passivation. Several topics are discussed, including the passivation performance on various semiconductor surfaces, the processing of the PO_x and Al_2O_3 layers, the role of the capping layer, and aspects related to device integration. The PO_x/Al_2O_3 stacks feature some unique properties, including an unusually high positive fixed charge density, a low interface defect density, and can be prepared over a wide deposition temperature range. These unique properties arise in part from the mixing process that occurs between the PO_x and Al_2O_3 layers, which upon post-deposition annealing leads to the formation of $AlPO_4$. The surface passivation provided by PO_x/Al_2O_3 stacks is highly stable and the stack can be used to conformally coat high-aspect-ratio structures such as nanowires, showing their promise for use in semiconductor devices.

1. Introduction

Semiconductor materials form the basis for many electronic and optoelectronic devices, such as transistors, lasers, photodetectors, power devices, light emitting diodes (LEDs), and solar cells [1]. Silicon has been of great importance in these applications and has been the dominant material for micro-electronics [2] and photovoltaics [3]. However, alternatives to silicon have also been extensively investigated, including germanium and III-V compound semiconductors. Group III-V semiconductors have shown some advantages over silicon, mainly because of their direct bandgap and high electron mobilities [4]. Germanium also has a higher carrier mobility than Si [5], and hexagonal Ge and SiGe alloys were reported to have direct bandgaps [6]. The direct bandgap allows for optoelectronic applications such as LEDs [7,8] and lasers [9,10]. Furthermore, the high carrier mobilities make these semiconductors interesting alternatives to silicon for certain applications, such as field-effect transistors (FETs) [5,11,12]. Germanium specifically is relevant for complementary metal-oxide-semiconductor (CMOS) applications, because it has both a high electron mobility, as well as a high hole mobility [5,13]. These alternative semiconductors are sometimes combined with silicon, which has a very mature processing technology. Examples are Ge on Si [10,14–18] and III-V on Si [8,9,19] technologies, which are used for photonic applications.

Recombination at surfaces of Si, Ge, and III-V semiconductors due to (surface) defect states can significantly limit device performance. For silicon, this is exemplified by silicon solar cells, where initially performance was limited by defects in the silicon bulk. However, as the Si bulk material quality kept improving, recombination processes at the surface

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became dominant [20]. For the use of germanium in field effect transistors, achieving a high quality interface between the Ge and the high-*k* dielectric is a major challenge [13]. For III-V semiconductors, such as GaAs, InP, InGaAs, InSb, and GaN, recombination processes at the surface also significantly reduce device performance [21,22]. Proper surface passivation is therefore critical to reduce the number of defects at the surface, which are generally expressed in terms of the interface defect density (D_{it}). Reduction of the D_{it} leads to a reduction of Shockley–Read–Hall (SRH) recombination enabled by these defects. Proper surface passivation becomes even more crucial with further device downscaling and the emergence of highly structured nanodevices, which typically have higher surface-to-volume ratio. This leads to surface recombination processes becoming even more dominant.

Although Ge and III-V semiconductors exhibit some advantageous properties compared to silicon, in terms of surface passivation these materials face their own specific challenges. The oxide of silicon (SiO_2) is straightforward to obtain and provides excellent surface passivation of silicon surfaces [23], which is mainly enabled by a very low D_{it} of SiO_2 on Si and is one of the reasons why silicon has become the dominant semiconductor in electronic applications. In contrast, passivation of germanium by its oxide (GeO_2) is challenging, because it is unstable at elevated temperatures and soluble in water [24–27]. For III-V semiconductors, passivation by their oxides is also challenging, as they generally result in poor interface quality [28]. Therefore, germanium and III-V semiconductors typically require surface passivation by materials other than their oxides and even for surface passivation of silicon, there is a demand of alternative layers with additional features beside a low D_{it}. For FETs for example, a high-*k* value of the dielectric is desired [29]. For solar cells, a high fixed charge (Q_f) contained within the passivation layer or at the surface of the semiconductor can be desirable [23], or the passivation layer should be able to conduct charge, i.e. act as passivating contact [30]. These requirements have led researchers to consider different materials for surface passivation of Si, Ge, and III-V semiconductors, including a-Si:H, Al_2O_3, SiN_x, SiO_x, TiO_x, Ga_2O_3, HfO_2, AlN, Ta_2O_3, ZrO_2, ZnO, Nb_2O_5, or stacks thereof [23,29,31–44], which have led to varying degrees of surface passivation. Continued research on surface passivation of these semiconductors is key to allow further device scaling, to enable devices based on a wider variety of semiconductor substrate materials, and finally to improve device performance.

Recently, a novel stack of phosphorus oxide and aluminum oxide (PO_x/Al_2O_3) has been shown to provide excellent surface passivation of both Si [45–48] and InP [49] surfaces. On silicon, the PO_x/Al_2O_3 stacks have been shown to achieve a very low D_{it} on the order of 10^{10} eV^{-1} cm^{-2} and a high positive fixed charge density (Q_f) on the order of 10^{12}–10^{13} cm^{-2}. On planar InP and InP nanowires, it has been shown that PO_x/Al_2O_3 stacks improve the charge carrier lifetime and thermal stability of the InP. The PO_x/Al_2O_3 stacks therefore show great promise as passivation scheme for both Si and InP semiconductor devices, and in particular for solar cell devices. It has furthermore been shown that the PO_x/Al_2O_3 stack provides state-of-the-art passivation on textured n^+-doped Si, which is frequently used on the front side of c-Si solar cells [48] and recently InP nanowire solar cells with extremely low material consumption featuring the PO_x/Al_2O_3 stack as passivation scheme have been realized [50]. The PO_x/Al_2O_3 stacks may also prove to be beneficial as passivation layer on other III-V semiconductors or germanium.

Here, we review the recent results obtained on surface passivation by PO_x/Al_2O_3 stacks. First, in Section 2, the passivation of semiconductor surfaces is discussed, specifically for Si and InP, whereon the PO_x/Al_2O_3 stack has been shown to achieve excellent surface passivation. This is followed in Section 3 by a discussion on the processing steps required to obtain PO_x/Al_2O_3 stacks, in particular for two different deposition processes, i.e. plasma-enhanced atomic layer deposition (PE-ALD) and pulsed-flow plasma-enhanced chemical vapor deposition (PF-PECVD). In Section 4, the role of the Al_2O_3 capping layer is discussed, which is shown to have a significant effect on the passivation quality provided by the PO_x/Al_2O_3 stack and to mix with the PO_x layer, leading to structural changes upon annealing. Lastly, in Section 5, aspects pertaining to device integration are discussed, in particular conformality and stability.

2. Passivation of semiconductor surfaces

2.1. Passivation of InP and Si

PO_x/Al_2O_3 stacks for semiconductor passivation have first been reported on InP surfaces [49]. InP surfaces are highly sensitive to heat treatments [51,52]. Desorption of P from the InP can occur at temperatures higher than 200 °C in vacuum [53], which can result in phosphorus-vacancy-related defects. Therefore, low-temperature processes are required for passivation of InP surfaces [54]. Desorption of P from the InP surface might be reduced by using a P-rich passivation layer, which has led to the consideration of a layer of PO_x for passivation of InP surfaces. We note that this PO_x layer is different from the native oxide of InP, which is a mix of indium oxide and phosphorus oxide. However, PO_x is highly hygroscopic [55] and degrades within minutes in air, turning into phosphoric acid. To avoid such degradation, Al_2O_3 has been used as a capping layer to protect the PO_x layer from reactions with the ambient, resulting in the PO_x/Al_2O_3 stack.

On planar InP and InP nanowires (NW), it has been shown that stacks of PO_x/Al_2O_3 deposited at low temperature (25 °C) result in an increase in carrier lifetime and an increase in thermal stability of the InP [49]. The carrier lifetime was increased by a factor of 3 compared to an unpassivated InP NW (where notably the bare InP surface is considered to already be relatively well-passivated) due to the surface passivation provided by the PO_x/Al_2O_3 stacks. On the other hand, deposition of only an Al_2O_3 layer was found to lead to degradation of the InP NW, demonstrating the importance of the PO_x layer and showing the potential of PO_x/Al_2O_3 stacks for InP surface passivation. Following the good results obtained on passivation of InP surfaces, the PO_x/Al_2O_3 stacks were investigated for the passivation of silicon surfaces. On silicon, the PO_x/Al_2O_3 stacks [45] provide surface passivation on the same level as Al_2O_3, which is well-known to be a highly effective passivation layer [31].

The surface passivation provided by PO_x/Al_2O_3 stacks on Si and InP NWs is summarized in Fig. 1, where the carrier lifetime is plotted as a function of the post-deposition annealing temperature. Carrier lifetimes determined on the unpassivated surfaces and surfaces passivated by Al_2O_3 are also plotted for comparison. Annealing is required to activate the surface passivation, which is the case for both Si and InP, although lower annealing temperatures are required for InP. The effect of annealing on PO_x/Al_2O_3 stacks will be discussed further in section 3.1.4 and 4.2.

The carrier lifetimes determined on Si and InP shown in Fig. 1 vary by several orders of magnitude. This is related to a difference in the predominant recombination mechanism [56]. For silicon this is SRH recombination, except at high injection levels, where Auger recombination starts to dominate. For InP and other direct-bandgap materials, assuming high-quality material, the dominant recombination mechanism is radiative recombination. Due to these differences in recombination mechanism, different characterization techniques are used to determine the carrier lifetimes on Si and on III-V materials. For silicon, the carrier lifetimes are often determined by photoconductance decay (PCD) measurements [57], which typically result in carrier lifetimes on the order of microseconds to milliseconds [23]. For III-V materials, time-resolved photoluminescence (TRPL) is frequently used [58], which typically results in carrier lifetimes on the order of picoseconds to nanoseconds [59–61].

2.2. Impact of deposition process on surface passivation quality

After the first report of excellent passivation on c-Si [45], the surface passivation quality of PO_x/Al_2O_3 stacks on c-Si was investigated in more

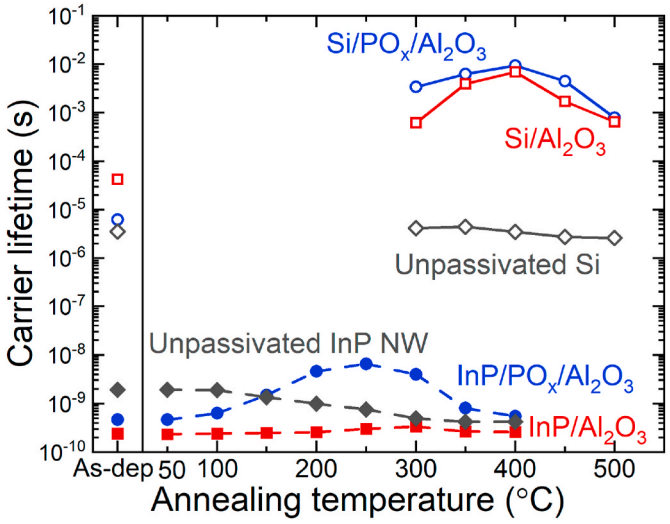

Fig. 1. Carrier lifetimes of Al_2O_3- and PO_x/Al_2O_3-passivated planar 280 μm thick, 1–5 Ωcm, *n*-type FZ Si (100) wafers (data points with solid lines) and wurtzite InP nanowires (data points with dashed lines), as a function of annealing temperature (10 min in N_2), together with unpassivated semiconductor surfaces as reference. The first data points represent the as-deposited or as-received passivation quality. Data on InP nanowires were adapted from Black et al. [49] Note that the reported carrier lifetimes on Si were determined using photoconductance decay, while the carrier lifetimes on InP NWs were determined using time-resolved photoluminescence.

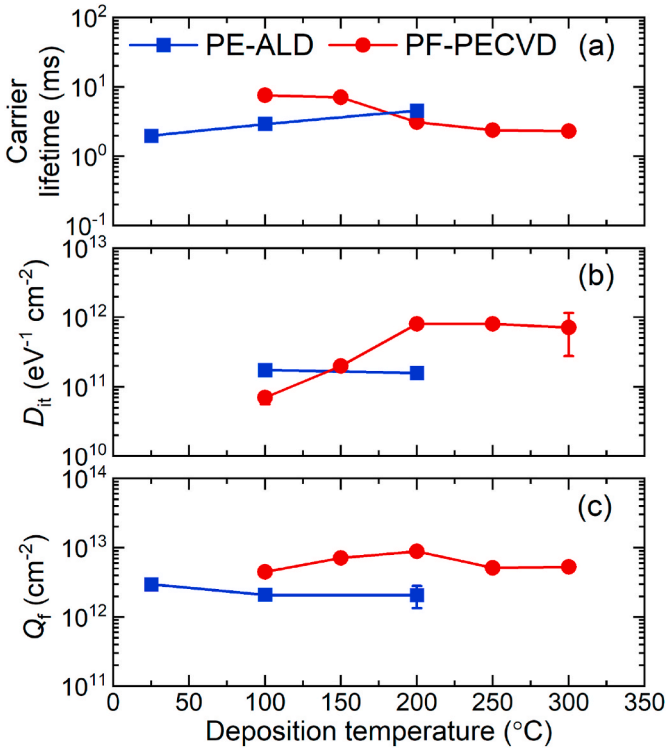

Fig. 2. Passivation properties of PO_x/Al_2O_3 stacks on c-Si, (a) minority carrier lifetime, (b) interface defect density D_{it}, and (c) fixed charge density (Q_f), as function of deposition temperature after post-deposition annealing of the stacks in N_2. Carrier lifetimes were determined using photoconductance decay, while D_{it} and Q_f were determined from combined high-frequency/quasi-static capacitance–voltage measurements. The PO_x layer was deposited using either an PE-ALD process or a PF-PECVD process. Error bars for many data points are small enough not to exceed the size of the markers. Original data is combined with data from Black et al. (25 °C PE-ALD) [46] and Theeuwes et al. (PF-PECVD) [47].

detail. Initial works employed plasma-enhanced atomic layer deposition (PE-ALD) to deposit the PO_x/Al_2O_3 stacks [45,46]. In later works, the PO_x layer was deposited by a pulsed-flow plasma-enhanced chemical vapor deposition (PF-PECVD) process instead [47,48,62]. The details of these deposition processes will be discussed in section 3.1. The passivation provided by the PO_x/Al_2O_3 stacks resulted in high minority carrier lifetimes, i.e. high passivation quality on silicon over a wide range of deposition temperatures, regardless of the deposition process used, as shown in Fig. 2a. These high lifetimes are enabled by the unique combination of a very low interface defect density (D_{it}) and a high positive fixed charge density (Q_f), as shown in Fig. 2b and c, respectively. The interface defect density is a measure for the chemical passivation provided by the passivation layer, where lower is better. On the other hand, fixed charge can aid in surface passivation due to modification of the surface carrier concentrations, which can reduce recombination. This is generally referred to as field-effect passivation [23].

The D_{it} value corresponding to the layer stack fabricated by the PF-PECVD process for the PO_x layer, is influenced by deposition temperature, resulting in an increase in D_{it} at higher deposition temperatures. Interestingly, an increase in deposition temperature for the PE-ALD process from 100 °C to 200 °C did not result in an increase in D_{it}, although the exact mechanism is not known. The Q_f value is not significantly affected by the deposition temperature nor the deposition technique, and a high positive Q_f on the order of 10^{12}–10^{13} cm^{-2} is obtained in all cases. The processing of PO_x/Al_2O_3 stacks appears to be quite robust, as over a wide range of deposition temperatures and using different types of deposition processes, a high passivation quality can be obtained.

2.3. Overview of D_{it} and Q_f

Fig. 3 presents an overview of interface properties of passivation schemes on c-Si, which puts the D_{it} and Q_f values of the PO_x/Al_2O_3 stacks in perspective with other passivation schemes. In Fig. 3a, the defect density is plotted, which generally ranges from 10^{10} to 10^{13} eV^{-1} cm^{-2}. The PO_x/Al_2O_3 stacks reach very low D_{it} values, on a level similar to Al_2O_3 and SiO_x, and lower than SiN_x. Hydrogenated amorphous silicon (a-Si:H) reaches even lower values for D_{it}. Note that the D_{it} values of a-Si:H are not direct experimental measurements but result from modeling of lifetime data under certain assumptions. It is well known that a-Si:H provides excellent chemical passivation of c-Si [30,63,64], which has enabled for example the world-record efficiency of 26.6% for single-junction silicon solar cells [65,66]. However, these a-Si:H layers also result in parasitic optical absorption losses and are not very thermally stable [30].

In c-Si solar cells, Al_2O_3 is commonly used as passivation layer on *p*-type Si surfaces, while SiN_x (or a SiO_x/SiN_x stack) is frequently used on *n*-type surfaces [67], in part due to their high negative and positive fixed charge on silicon, respectively. Fig. 3b depicts the fixed charge of different passivation schemes on silicon. The PO_x/Al_2O_3 stacks show a very high positive fixed charge on silicon, on the order of 10^{12}–10^{13} cm^{-2}. This is higher than the positive fixed charge provided by SiN_x and similar to the magnitude of the negative fixed charge provided by Al_2O_3. Due to this unique combination of high positive fixed charge, combined with the very low D_{it}, PO_x/Al_2O_3 stacks have been shown to be highly effective for the passivation of highly doped *n*-type Si surfaces, which are frequently used in silicon solar cells. It has been found that the passivation provided by PO_x/Al_2O_3 on n^+ -doped silicon rivals state-of-the-art 'alnealed' SiO_2 and $SiO_x/SiN_x/SiO_x$ (ONO) stacks, and results in higher passivation quality than that provided by SiN_x and SiO_x/SiN_x stacks [48].

The origin of the low D_{it} enabled by PO_x/Al_2O_3 on silicon is found to be related to surface passivation provided by hydrogen and the formation of $AlPO_4$ upon annealing, leading to a decrease in D_{it} by almost 3 orders of magnitude from ~10^{13} to ~10^{10} eV^{-1} cm^{-2} [47]. On silicon a

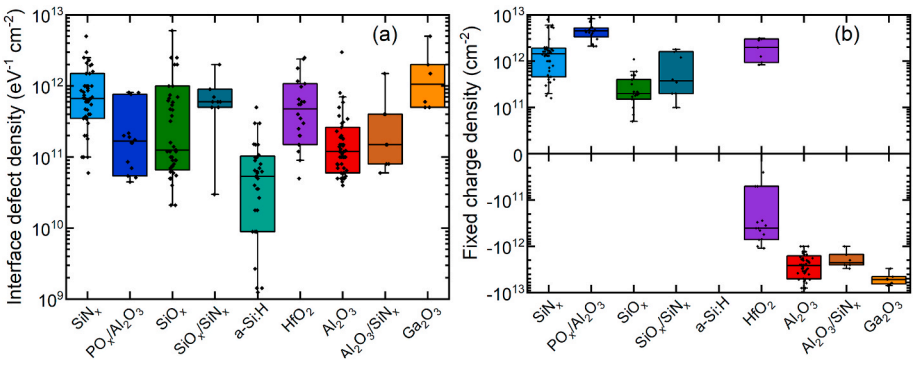

Fig. 3. Overview of interface properties of passivation schemes on c-Si, namely SiN_x [68–72], PO_x/-Al_2O_3 [45–48], SiO_x [71,73–76], SiO_x/SiN_x [77,78], a-Si:H [79–81], HfO_2 [82–84], Al_2O_3 [84–92], Al_2O_3/SiN_x [87], and Ga_2O_3 [93,94]. Interface defect density is shown in (a), while fixed charge density is shown in (b). Note that the fixed charge density can be both positive or negative. Colored bars show ±30% of data points from the median, while the error bars show where ±45% of data points from the median are located.

high positive fixed charge of around 10^{12}–10^{13} cm^{-2} is present, both after deposition and after annealing [47]. On InP NWs, PO_x/Al_2O_3 stacks induce an *n*-type field-effect, which indicates the presence of positive fixed charges [95]. The origin of the high positive fixed charge, however, has not been established. It is suggested that the $[(O\text{-})_4P]^+$ defect (P bonded to four bridging oxygen atoms) can be a likely origin for the positive fixed charge of the PO_x/Al_2O_3 stacks [45]. This defect is structurally analogous to $[(O\text{-})_4Al]^-$, which has been proposed as the origin of negative fixed charge in Al_2O_3 [96]. The high positive fixed charge density is already present in the as-deposited state. Upon annealing, $AlPO_4$ is formed mainly in the PO_x layer (see section 4.2), but the positive fixed charge density does not change [47]. This suggests that the mixing of the Al into the PO_x layer does not significantly affect the fixed charge, possibly because the fixed charges are situated near the silicon interface.

3. PO_x/Al_2O_3 processing

3.1. Process flow

Fig. 4 schematically shows a typical process flow of the fabrication of PO_x/Al_2O_3 stacks. The substrates used so far are Si and InP, but other substrates such as germanium or III-V semiconductors may also be used. First, an optional surface pre-treatment can be used, for example to remove the thin (native) oxide layers from the substrate prior to deposition. Then, the PO_x layer and Al_2O_3 layers are deposited, where it is important that deposition of the Al_2O_3 capping layer is performed *in-situ* to avoid degradation of the PO_x layer upon exposure to the ambient. Finally, a post-deposition annealing treatment is used, which has been found to be required to activate the passivation. In this section, these processing steps will be discussed in more detail.

3.1.1. Pre-treatment

The surface can receive a pre-treatment prior to deposition of the PO_x and Al_2O_3 stacks. A common pre-treatment is the removal of the surface oxides, for example using a short exposure to dilute hydrofluoric acid, also known as an HF dip, as these oxides are usually not grown in a controlled manner or might be detrimental to the surface passivation. In this work, an HF dip has been used for removal of the surface oxides both on Si and InP, prior to the deposition of PO_x/Al_2O_3 stacks. On Si, the effect of several other pre-treatments and their effect on the passivation quality of the PO_x/Al_2O_3 stacks have also been investigated. These pre-treatments include a Radio Corporation of America (RCA) clean [97] without removal of the RCA-formed oxide, an HF dip followed by O_2 plasma treatment, and an HF dip followed by UV/O_3 treatment. Regardless of which pre-treatment was used, high surface passivation quality could be reached with the PO_x/Al_2O_3 stack - which can be seen in the supplementary info Fig. S2 - underlining the robust passivation quality provided by the PO_x/Al_2O_3 stacks.

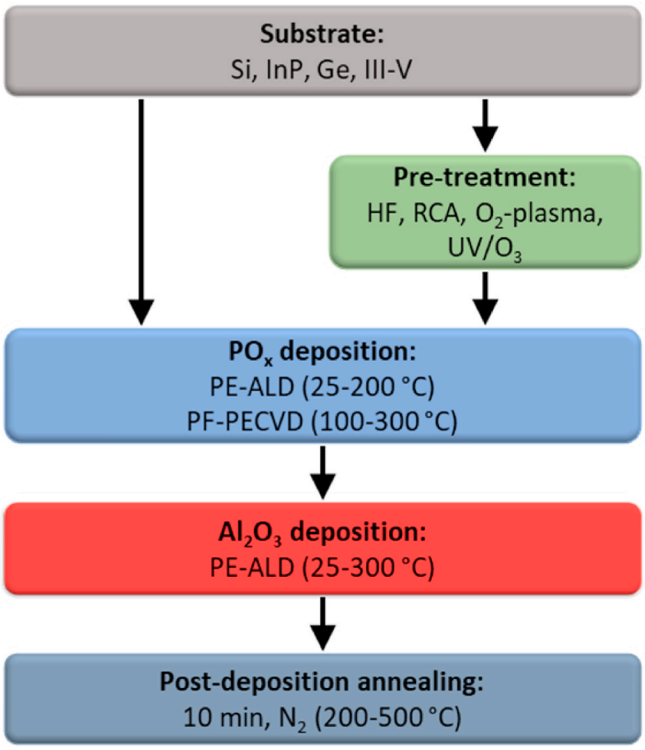

Fig. 4. Schematic process flow for PO_x/Al_2O_3 surface passivation stacks. Pre-treatment is optional and different pre-treatments can be used. The deposition of the PO_x layer should be followed by *in-situ* capping with Al_2O_3. Post-deposition annealing is required to activate passivation. The values indicated in brackets represent the already investigated processing conditions.

3.1.2. PO_x deposition

For the deposition of thin film passivation layers, vapor phase deposition techniques, such as atomic layer deposition (ALD) and chemical vapor deposition (CVD), are frequently used. ALD processes have the merits of atomic layer thickness control, conformality, and uniformity [98], while using a plasma as co-reactant enables a wider variety of precursors and materials, and lower deposition temperatures [99,100]. CVD processes on the other hand typically have higher growth rates (lower processing times) and enable higher throughput and growth of thicker films. PO_x layers have been reported to be obtained using various methods, i.e. CVD using an O_2 plasma and phosphorus vapor [101,102], ALD using tris(dimethylamido)phosphorus and an O_2 plasma [103], oxidation of black phosphorus [104], and O_2 plasma etching of phosphorene [105,106]. However, for investigations of surface passivation by PO_x/Al_2O_3 stacks, two deposition processes for the PO_x layer have been reported so far: a plasma-enhanced ALD process (PE-ALD)

[45,46,49] using trimethyl phosphate (TMPO, $PO(OCH_3)_3$) and an O_2 plasma, and a pulsed-flow plasma-enhanced chemical vapor deposition process (PF-PECVD) [47,48], using TMPO and an O_2 plasma. The main difference between these two processes is whether the precursor (TMPO) and reactant (O_2 plasma) are present in the reactor simultaneously (PF-PECVD) or alternately (PE-ALD). The details of the two PO_x deposition processes are schematically shown in the Supplementary Information Figs. S1a and S1b. Although currently only these two processes have been reported for PO_x passivation layers, other processes for deposition of the PO_x layer are likely also realizable, such as for example continuous CVD.

The *in-situ* characterization of the PE-ALD and PF-PECVD PO_x layer growth is shown in Fig. 5a and b, respectively. Lower deposition temperatures lead to higher growth per cycles (GPC) for both PO_x deposition processes. The thickness of the PO_x layer is typically kept around 5 nm. The PO_x PE-ALD process shows a significant growth delay on Si, as seen in Fig. 5a. The growth mechanisms of the PO_x layer have not been investigated in detail yet, but it is known that the precursor dose does not reach saturation [45]. This may lead to a buildup of precursor molecules inside the reaction chamber, which could explain why the GPC increases with the number of cycles. Eventually, this buildup of precursor appears to reach a steady state, as after the initial growth delay, the PE-ALD PO_x deposition process does reach linear growth, which can take more than 100 ALD cycles. The steady-state GPCs are about 1.05, 1.02, and 0.52 Å/cycle, for deposition temperatures of 25, 100, and 200 °C, respectively. The small jump in thickness in the first 10 ALD cycles is likely related to the formation of a SiO_x layer due to the exposure of the silicon surface to the O_2 plasma of the PE-ALD PO_x process.

The PO_x PF-PECVD process has a significantly higher growth rate and requires fewer cycles to obtain the same PO_x film thickness, as can be seen in Fig. 5b. The PF-PECVD process still shows a slight growth delay, similar to the PE-ALD process. However, there is no jump in film thickness observed in the first cycles, as in this particular case the silicon surface was pre-oxidized using an O_2 plasma prior to the start of the PO_x deposition process. At a deposition temperature of 300 °C, there is growth for the PF-PECVD process albeit with a lower GPC, whereas the PE-ALD process at this deposition temperature barely shows any growth.

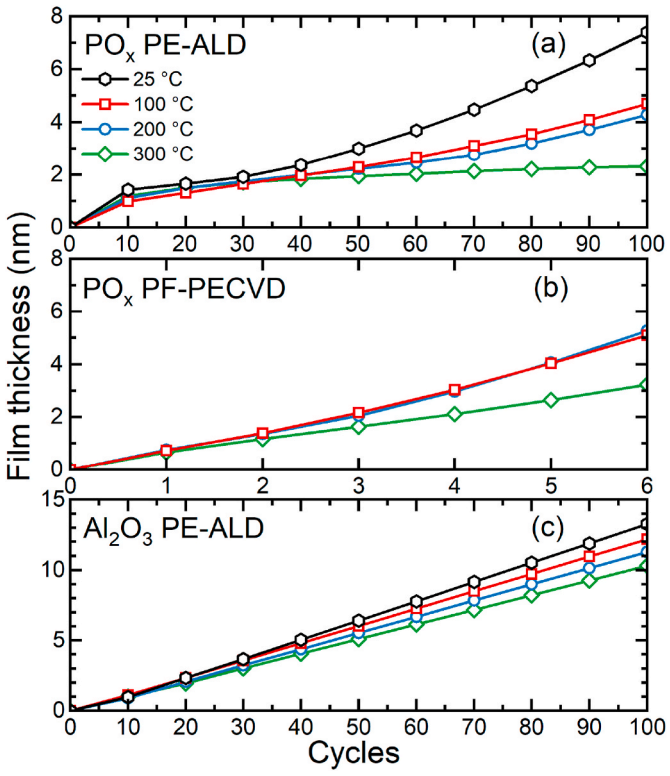

Fig. 5. Film thickness on silicon determined by *in-situ* spectroscopic ellipsometry as function of cycles for (a) PO_x deposited by PE-ALD, (b) PO_x deposited by PF-PECVD, and (c) Al_2O_3 deposited by PE-ALD. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

3.1.3. Al_2O_3 deposition

As exposing the PO_x layer to ambient leads to visible degradation within minutes, it is critical that the PO_x is capped *in-situ* with a layer that protects the PO_x from the ambient. For the PO_x/Al_2O_3 stacks, Al_2O_3 acts as a capping layer and has been deposited by PE-ALD using trimethyl aluminum (TMA, $Al(CH_3)_3$) and an O_2 plasma. The details of the PE-ALD process are shown schematically in the Supplementary Information Fig. S1c. Besides PE-ALD, other deposition methods such as plasma-enhanced CVD or PF-PECVD [107] for deposition of the Al_2O_3 capping might also be used. In principle any *in-situ* deposited capping layer could be used to protect the PO_x layer. However, it is important to note, that the Al_2O_3 layer plays a role in the passivation quality provided by the PO_x/Al_2O_3 stack, which will be discussed in more detail in section 4.1.

The *in-situ* growth of Al_2O_3 on top of the PO_x layer is shown in Fig. 5c. In the first 10 cycles, the GPC of the Al_2O_3 PE-ALD process is slightly reduced as it is growing on the PO_x layer. This slight reduction in growth may be related to mixing of the Al into the PO_x layer, which is known to occur during deposition and will be discussed in section 4.2, and might take place within the first few cycles. However, it could also be related to a slight delay in nucleation which is quite common when growing one layer on top of another. After the first 10 cycles a steady GPC is reached, and linear growth can be observed. The GPC values of the Al_2O_3 PE-ALD process are 1.37, 1,23, 1.15, and 1.04 Å/cycle, for deposition temperatures of 25, 100, 200, and 300 °C, respectively. This decreasing trend in GPC with higher deposition temperature for PE-ALD of Al_2O_3 matches well with reports in the literature for Al_2O_3 grown on silicon, although the reported GPC values at the lower deposition temperatures are slightly higher [108].

3.1.4. Post-deposition annealing

After the deposition of the PO_x/Al_2O_3 stack, a post-deposition annealing treatment is required to activate the passivation, as can also be seen in Fig. 1. The optimal annealing temperature depends on the substrate, where surface passivation of InP requires lower annealing temperatures, in comparison to the surface passivation of Si. On Si, post-deposition annealing leads to passivation of Si dangling bonds by hydrogen originating from the PO_x/Al_2O_3 stack, as well as to the formation of $AlPO_4$ [47]. The latter will be discussed in more detail in section 4.2. The passivation mechanism of PO_x/Al_2O_3 on InP has not been investigated in detail, but hydrogen is known to not only be able to passivate defects at the Si surface, but also to passivate defects at the surfaces of other semiconductor materials, including InP, GaAs, and Ge [109–112]. Annealing may activate such passivation provided by hydrogen, where the hydrogen originates from the PO_x/Al_2O_3 stack. Annealing at high temperatures leads to depassivation of the surface as also seen in Fig. 1, which may be related to breaking of hydrogen bonds and the effusion of hydrogen.

3.2. Influence of layer thickness

The thicknesses of the PO_x and Al_2O_3 layers in the stack play an important role in the obtained surface passivation quality. It has been shown that the PO_x layer thickness should be around 4–6 nm to reach the optimal passivation quality on c-Si, as a lower thickness leads to a decreased passivation quality [46]. For the Al_2O_3 layer, a thickness of 10 or 15 nm results in the same passivation quality, but Al_2O_3 layer thicknesses <10 nm result in a decrease in passivation quality. On InP,

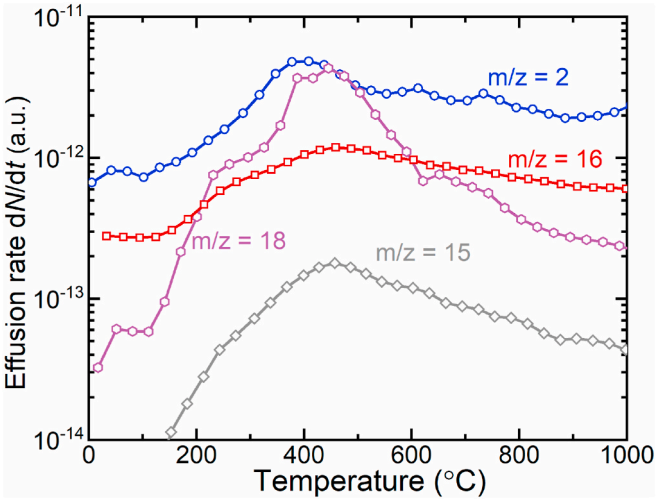

Fig. 6. Effusion rate as function of annealing temperature for a PO_x/Al_2O_3 stack deposited at 100 °C. The measured effusion rate is shown for various mass-over-charge (m/z) ratios. A heating rate of 20 °C min^{-1} was used. The main contributions to the m/z ratios are: H_2 for $m/z = 2$, CH_4 for $m/z = 15$, CH_4, H_2O, and CO for $m/z = 16$, and H_2O for $m/z = 18$.

using a thicker Al_2O_3 capping layer of 16 nm resulted in higher surface passivation than a 3 nm Al_2O_3 capping layer (when using a 1 nm thick PO_x layer), while using 5 nm PO_x instead of 1 nm resulted in even higher surface passivation [49].

Notably, if the PO_x layer becomes thicker than ~7 nm, the PO_x/Al_2O_3 stack can start to show blistering upon annealing, and for thicker (~10 nm) PO_x layers, blistering can even occur without annealing. A microscope image of this blistering can be seen in the Supplementary Information Fig. S3. This sort of blistering of a stack of two layers is similar to Al_2O_3/SiN_x stacks, which can also show blistering upon annealing [113,114]. For the Al_2O_3/SiN_x stacks, it has been shown that blistering is the result of the release of hydrogen and other gaseous species such as H_2O, from the Al_2O_3 layer at elevated temperatures, which initiates the blistering of the layers. It has been shown that the PO_x/Al_2O_3 stacks have a high hydrogen content (~20 at. %) [47] and from effusion measurements, it is evident that H_2 ($m/z = 2$) and H_2O ($m/z = 18$) effuse from the PO_x/Al_2O_3 stacks at temperatures of around 300–400 °C, as shown in Fig. 6. The blistering upon annealing of PO_x/Al_2O_3 stacks with a thick (>7 nm) PO_x layer also occurs at annealing temperatures of around 300–400 °C. Therefore, it is likely that the blistering of the PO_x/Al_2O_3 layers follows a similar mechanism as the blistering of the Al_2O_3/SiN_x layers, i.e. the PO_x layer releases significant amounts of gaseous H_2 upon annealing, which can initiate the formation of blisters.

It has been observed that when using a higher pressure (100 mTorr instead of 15 mTorr) when depositing the PO_x layer, that stacks of 5 nm PO_x with 10 nm Al_2O_3 can also start blistering. It is possible that this is related to a higher hydrogen content of the PO_x layers deposited at higher pressure. For higher deposition temperatures up to 300 °C, no blistering was observed for stacks of 5 nm PO_x and 10 nm Al_2O_3. It has not been investigated whether a PO_x layer thicker than 5 nm results in blistering for these higher deposition temperatures.

3.3. Physical properties

The material properties of PO_x/Al_2O_3 stacks are similar to those of Al_2O_3 films, although the overall mass density and refractive index are lower, which is likely due to the lower mass density and refractive index of the PO_x layer [47]. Note that mixing and structural changes take place in the stack upon annealing. Therefore, the PO_x/Al_2O_3 stacks are treated as single (mixed) layers for determination of the physical properties after annealing. The physical properties of the PO_x/Al_2O_3 stacks are summarized in Table 1, where also the physical properties of Al_2O_3 are added for comparison. While the material properties of Al_2O_3 films can vary quite significantly with deposition temperature [31], the material properties of PO_x/Al_2O_3 do not vary much over the deposition temperature range of 100–300 °C [47]. Note that the phosphorus content in Table 1 is averaged over the entire PO_x/Al_2O_3 stack, whereas the phosphorus content in the PO_x layer is higher, up to around 12 at. %. In the table also the interface properties of PO_x/Al_2O_3 and Al_2O_3 on silicon are listed, namely the interface defect density and the fixed charge density. The values for optical constants ε_1 and ε_2 can be found in the Supplementary Information Fig. S4.

4. Capping layer

4.1. Role of the capping layer on passivation quality

The capping layer of the PO_x/Al_2O_3 stacks, i.e. the Al_2O_3 layer, not only plays the role of protecting the PO_x layer, but it also plays a role in the passivation quality. This is illustrated in Fig. 7a, where the passivation quality of PO_x/Al_2O_3 stacks with an Al_2O_3 capping layer deposited by thermal ALD and PE-ALD is shown in terms of minority carrier lifetime, where a higher lifetime indicates better passivation quality. Clearly, the choice of co-reactant for the ALD Al_2O_3 layer affects the passivation quality, even though both capping layers appear to have very similar composition, as shown in Fig. 7b and c. This shows that the capping layer has an influence on the passivation quality provided by the stack and not every capping layer might work as well without optimization. In this case, the passivation provided by the PE-ALD grown Al_2O_3 layer provided the highest passivation quality, but this is also (so far) the most optimized process for capping of the PO_x layer.

The difference in passivation quality provided by these two capping layers might also be related to a difference in ability of the Al_2O_3 layer to act as a hydrogen source and hydrogen effusion barrier [115], as the passivation quality of the PO_x/Al_2O_3 stacks is found to be related to surface passivation provided by hydrogen [47]. It is also noted that,

Table 1
Physical properties of PO_x/Al_2O_3 stacks (5/10 nm), deposited at 100 and 200 °C after annealing [47] and Al_2O_3 films deposited at 200 °C [31,85,108].

Physical property	PO_x/Al_2O_3 (100 °C)	PO_x/Al_2O_3 (200 °C)	Al_2O_3 (200 °C)
Phase	Amorphous	–	Amorphous
Refractive index	1.57 (at 2.1 eV)	1.56 (at 2.1 eV)	1.64 (at 2.0 eV)
Optical bandgap	>6 eV (E_{04})	>6 eV (E_{04})	6.4 eV
Dielectric constant	6.4	6.4	7–9
Mass density	2.7 g/cm^3	2.3 g/cm^3	3.1 g/cm^3
Hydrogen content	8 at. %	7 at. %	2-4 at. %
Aluminum content	28 at. %	28 at. %	32-33 at. %
Phosphorus content	5 at. %	5 at.%	–
Oxygen content	59 at. %	60 at.%	64-65 at. %
Interface defect density	5 x 10^{10} eV^{-1} cm^{-2}	8 x 10^{11} eV^{-1} cm^{-2}	1 x 10^{11} eV^{-1} cm^{-2}
Fixed charge density	+4 x 10^{12} cm^{-2}	+5 x 10^{12} cm^{-2}	- 6 x 10^{12} cm^{-2}

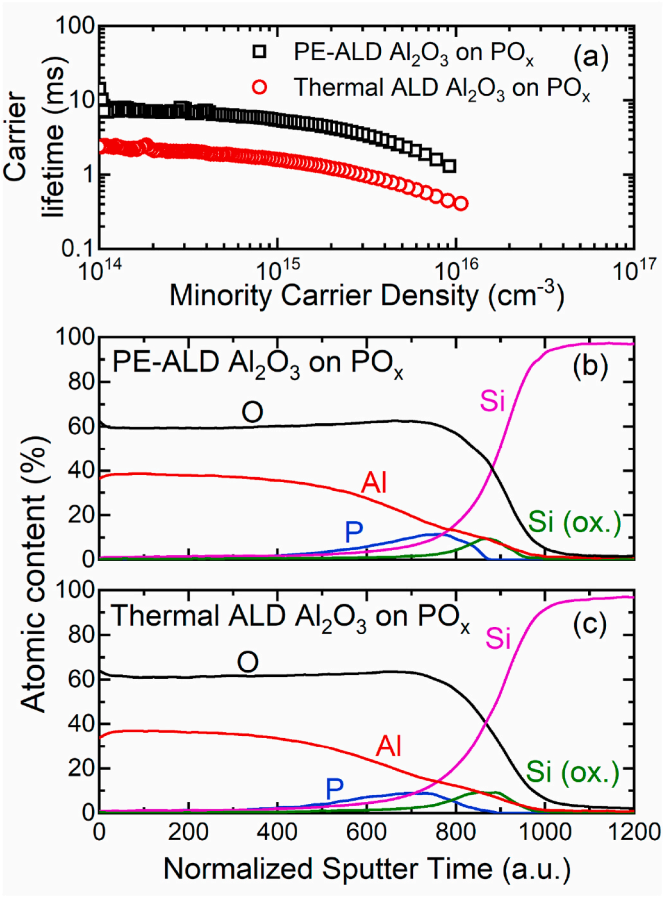

Fig. 7. The effective minority carrier lifetimes of (a) annealed PO_x/Al_2O_3 stacks on Si, where the of Al_2O_3 capping layer is deposited by PE-ALD or thermal ALD. Compositional XPS depth profiles of as-deposited PO_x/Al_2O_3 stacks where (b) Al_2O_3 is deposited by PE-ALD and (c) Al_2O_3 is deposited by thermal ALD. The PO_x layer is deposited by PF-PECVD and is 5 nm thick, while the Al_2O_3 layers are both 10 nm thick. The deposition temperature is 100 °C in both cases. The sputter times are normalized to the start of the Si bulk, which is set to 1000.

because of the hygroscopic nature of the PO_x layer, deposition using a thermal ALD process with H_2O as reactant may result in degradation of the PO_x layer during deposition of the capping layer, which may also lower the passivation quality.

Besides Al_2O_3, other capping layers can also be of interest. TiO_x has been investigated as capping layer on PO_x, resulting in a PO_x/TiO_x stack. A compositional XPS depth profile of this stack can be found in the Supplementary Information Fig. S5. The PO_x/TiO_x stack did not result in any significant surface passivation on silicon, indicating that not all capping layers may result in good passivation. However, this can also be in part related to the blistering observed for this stack. Nevertheless, capping the PO_x layer with alternative layers (or stacks) may provide opportunities to tailor the (passivation) properties of the resulting stack. It has been reported that deposition of a SiN_x layer on top of the PO_x/Al_2O_3 layers can protect the PO_x/Al_2O_3 from degradation during a high temperature firing process. The resulting $PO_x/Al_2O_3/SiN_x$ stack showed improved passivation quality as compared to the fired PO_x/Al_2O_3 stacks without SiN_x [48]. Possibly, a PO_x/SiN_x stack without intermediate Al_2O_3 layer might also lead to good passivation, as SiN_x is also frequently used as a capping layer.

4.2. Mixing of the PO_x and capping layer

It has been reported that aluminum from the Al_2O_3 layer mixes into the PO_x layer [47]. The mixing of the Al_2O_3 and PO_x layers can also be seen in Fig. 7a and b, where the Al signal clearly persists in the PO_x region. This mixing of Al into the PO_x layer can also be seen for PO_x/Al_2O_3 on InP [49]. The mixing of the capping layer with the PO_x layer happens already during deposition, and the mixing of the layers itself is not limited to just Al_2O_3 and PO_x. When using TiO_x as a capping layer, infiltration of Ti in the PO_x layer in the as-deposited state can also be observed, which can be seen in the Supplementary Information Fig. S5. As this mixing happens for these various capping layers, it is likely related to the hygroscopic nature of the PO_x layer and such mixing can be expected to also occur when using other capping layers. The mechanism for the mixing is not yet established, although some explanations have been proposed, including mixing due to a highly porous PO_x layer, a low melting point and glass transition temperature of the PO_x layer (lower than the deposition temperature), and interface reactions occurring between the PO_x layer and the capping layer [47].

Although mixing of the Al_2O_3 and the PO_x layer occurs already during deposition, upon annealing structural changes occur, which lead to the formation of $AlPO_4$ [47]. This can be seen in Fig. 8a, where the infrared spectra of the PO_x/Al_2O_3 stacks are plotted for as-deposited and annealed conditions. The structural changes lead to the formation of a prominent peak at 1100 cm^{-1}, which indicates the formation of $AlPO_4$, and a reduction in signals at 1250 and 950 cm^{-1}. These structural changes start to be visible already when annealing at 250 °C, and are more apparent when annealing at 400 °C. In Fig. 8b, Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) depth profiles for the same as-deposited and annealed PO_x/Al_2O_3 stacks from Fig. 8a are shown. The ToF-SIMS depth profiles show the presence of Al in the PO_x layer in the as-deposited state, showing the mixing of the layers, and upon annealing, the signals of Al^- and P^- change to some degree, consistent with the structural changes seen in infrared spectroscopy in the same annealing temperature range. The changes due to annealing consist of a broadening of the P^- signal into the Al_2O_3 layer and a flattening of the Al^- signal in the PO_x layer. Besides changes in the Al^- and P^- signal upon annealing, also the H^- signal decreases upon annealing at $T > 250$ °C. Specifically, the peak in H^- at the Al_2O_3/PO_x interface disappears upon annealing at 400 °C and the peak in H^- at the PO_x/Si interface is reduced. The coincidence between hydrogen effusion (see Fig. 6) starting near 200°C with a maximum near 400°C, the out-diffusion of hydrogen according to SIMS (between 250 and 400°C, see Fig. 8b) and the formation of $AlPO_4$ according to infrared spectroscopy (mostly between 250 and 400°C, see Fig. 8a) suggest a correlation between the formation of $AlPO_4$ and the effusion of hydrogen predominantly from the PO_x ($AlPO_4$) layer including the interfaces. We note that at the PO_x/Si interface hydrogen can react with silicon dangling bonds and passivate them [116]. These results suggest that the low interface defect density achieved with the Al_2O_3/PO_x stacks is likely not just related to hydrogen diffusion from a passivation layer as frequently observed for single layer passivation schemes [23], but also due hydrogen mobilized by a chemical reaction. Furthermore, the formation of $AlPO_4$, which is structurally analogous to SiO_2 [117], may also lead to some surface passivation.

For deposition temperatures of 200 °C and 300 °C, the comparison between infrared spectra and ToF-SIMS can be found in the Supplementary Information Fig. S6, where it is shown that at higher deposition temperatures, less structural and compositional changes in the PO_x/Al_2O_3 stacks take place. This corresponds to a lower passivation quality provided by these (PF-PECVD) PO_x/Al_2O_3 stacks, as shown in Fig. 2. The P^- signals at the surfaces of the PO_x/Al_2O_3 stacks are likely due to backside deposition of PO_x (wraparound), because these samples received a deposition on both sides. This is explained in more detail in section 6 of the supplementary information.

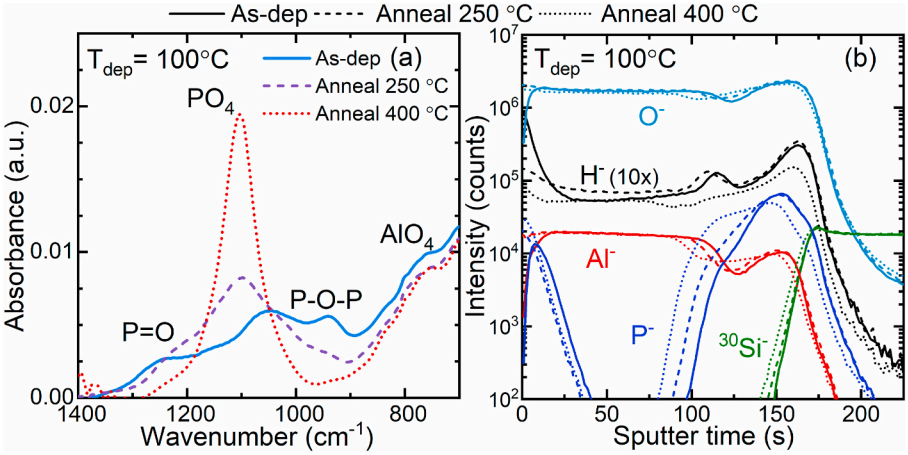

Fig. 8. Changes in PO_x/Al_2O_3 stacks due to annealing determined by (a) infrared spectroscopy spectra for PO_x/Al_2O_3 deposited at 100 °C from Theeuwes et al. [47] and (b) Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) depth profiles of the same PO_x/Al_2O_3 stacks. The layer thicknesses were 5 nm for the PO_x layer and 10 nm for the Al_2O_3 layer. Note the depth profiles were shifted to overlap the $^{30}Si^-$ signal and the intensities of H^- signals were multiplied by 10x to improve readability of the figure.

5. Towards device integration

5.1. Conformality

As device dimensions continue to scale down and high-aspect-ratio and complex 3D shaped device structures become more common, the conformality of thin film deposition processes becomes more critical. Flux controlled deposition techniques, such as CVD and physical vapor deposition (PVD), can have limited conformality, because for example, the flux of reactant molecules can be orders of magnitude higher at the entrance of a trench than inside the trench, leading to higher growth rates at the entrance [118]. For ALD, the surface-controlled nature of the deposition process allows for reactant molecules to diffuse deep into a trench and a higher probability to coat the entire structure conformally through the self-limiting surface reactions. For integration of PO_x/Al_2O_3 in devices, the choice between ALD or CVD most likely depends on aspect ratio, complex 3D structures, processing throughput, and the desired thickness control.

In Fig. 9, TEM images of three different types of structures coated with PO_x/Al_2O_3 stacks are shown, namely flat silicon, textured silicon, and an InP nanowire. Both an overview image of the structure itself, as well as a close-up of the interface between the PO_x/Al_2O_3 and the semiconductor are shown. In all cases, the structures are coated conformally by the PO_x/Al_2O_3 stacks. For the flat and textured silicon, the PO_x/Al_2O_3 stacks were deposited by PF-PECVD. On the InP nanowire, the PO_x/Al_2O_3 stack was deposited by PE-ALD. Energy-dispersive X-ray

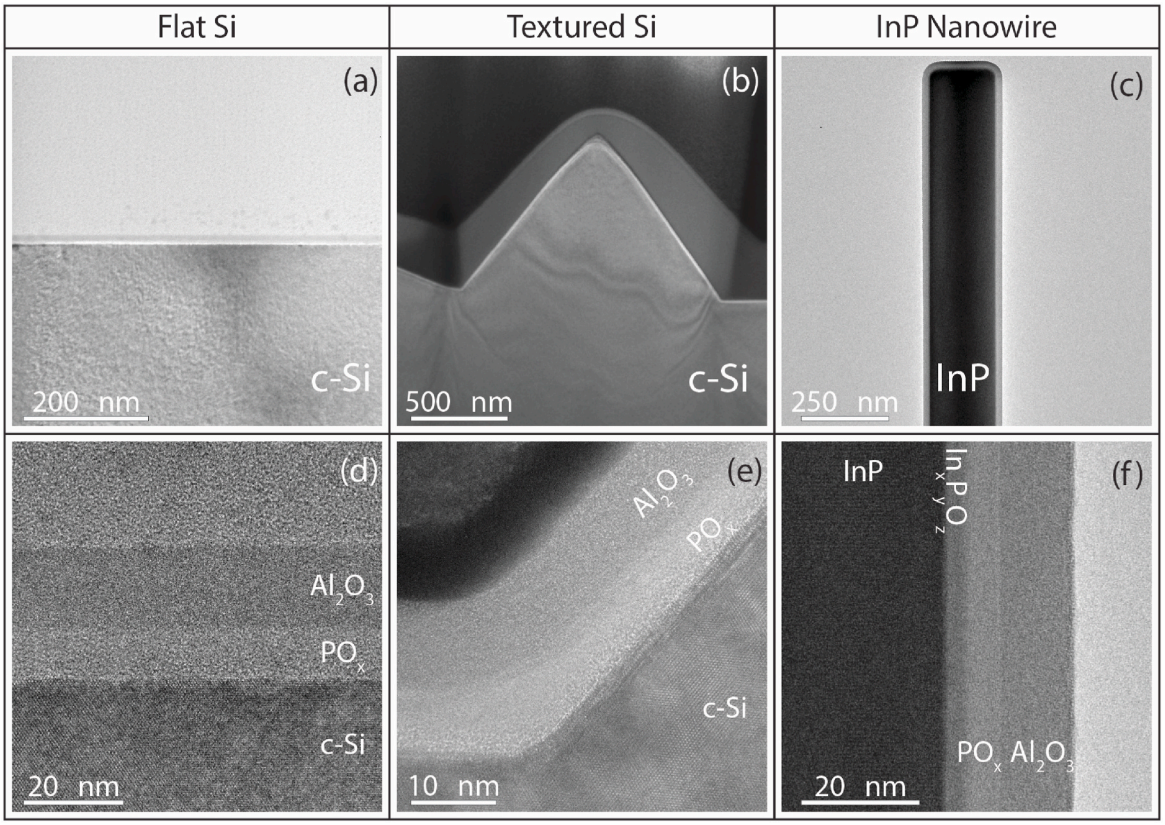

Fig. 9. Bright field TEM images of different types of structures coated with PO_x/Al_2O_3 stacks, namely a) flat silicon, b) textured silicon, and c) an InP nanowire. A close-up of the interface between PO_x/Al_2O_3 and the semiconductor for d) flat silicon, e) the bottom of textured silicon, and f) the bottom of an InP nanowire. The PO_x/Al_2O_3 stacks are deposited using the PF-PECVD process on flat and textured silicon, and the PE-ALD process on InP NWs.

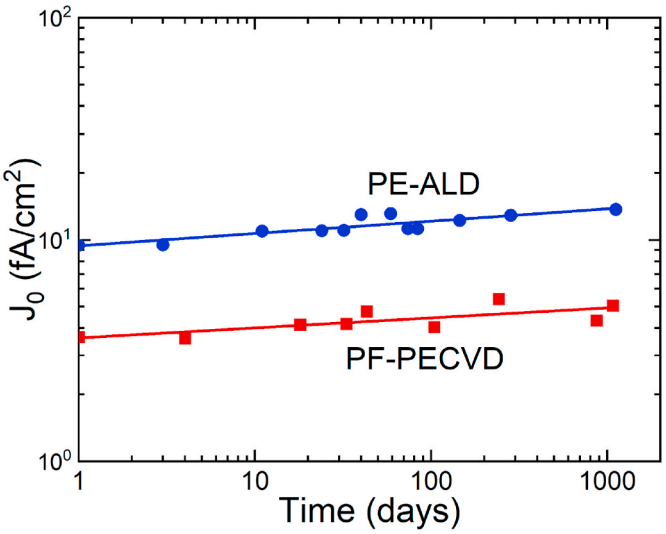

Fig. 10. Recombination parameter J_0 values as function of time for PO_x/Al_2O_3 stacks, where the PO_x layer was deposited either by PE-ALD or PF-PECVD, representing the stability of the passivation quality over time. Samples were kept in ambient conditions. The solid lines represent a least-square fit of the data.

spectroscopy (EDX) maps of the PO_x/Al_2O_3 stacks on textured silicon and InP nanowire are shown in the Supplementary Information Figs. S7 and S8, respectively.

5.2. Stability

For device applications, it is important that layers remain stable over an extended period of time, such that the device performance does not degrade significantly over time. Fig. 10 shows how the passivation quality of the PE-ALD and PF-PECVD PO_x/Al_2O_3 layers on silicon changes over time for samples kept in ambient conditions. The passivation quality here is presented in terms of the recombination parameter J_0 [119], which represents a measure for the amount of charge carrier recombination, where a lower value indicates better passivation quality. The solid lines represent a least-square fit through the data, which show that on average there is only a very slight increase in J_0 over time, indicating a very slight decrease in passivation quality. The degradation is similar for both the PE-ALD and PF-PECVD processes, as indicated by the similar slope of the straight-line fits. Such gradual degradation may simply be due to sample handling damage (like scratches) commonly observed to accumulate over multiple such measurements.

6. Conclusion

In this review, the latest insights of the PO_x/Al_2O_3 stacks for semiconductor surface passivation were summarized and elaborated upon. PO_x/Al_2O_3 stacks provide excellent surface passivation of Si and InP, which is enabled by the unique properties of the PO_x/Al_2O_3 stacks, including a high positive fixed charge density, a low interface defect density, and a wide deposition temperature range.

PO_x/Al_2O_3 stacks can be deposited using various deposition processes, which include PE-ALD and PF-PECVD processes, and several different pre-treatments may be used in prior to deposition of the PO_x/Al_2O_3 stack, without significantly impacting the surface passivation. Post-deposition annealing plays an important role for the surface passivation, as it activates the chemical passivation, which is related to passivation provided by hydrogen and the formation of $AlPO_4$.

The Al_2O_3 capping layer is required to protect the hygroscopic PO_x layer from reacting with ambient. However, the Al_2O_3 layer also plays a role in the passivation provided by the PO_x/Al_2O_3, likely due to its role as hydrogen source and hydrogen effusion barrier. Furthermore, the Al_2O_3 capping layer mixes into the PO_x layer during deposition, which upon annealing leads to the formation of $AlPO_4$. Instead of capping by Al_2O_3, capping the PO_x layer by other thin films may provide opportunities to tailor the properties of the resulting stack.

The surface passivation provided by the PO_x/Al_2O_3 stacks on silicon is stable for over 1000 days and high-aspect-ratio structures, such as nanowires can be conformally coated. Therefore, PO_x/Al_2O_3 stacks may be used in devices featuring complex 3D structures.

The understanding gained on the PO_x/Al_2O_3 stacks can enable the adoption of PO_x/Al_2O_3 stacks as a passivation scheme in Si and InP devices, including solar cells, FETs, LEDs, and lasers. Moreover, the unique properties of the PO_x/Al_2O_3 may enable opportunities for surface passivation of alternative semiconductor materials, including germanium and III-V semiconductors.

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CRediT authorship contribution statement

Roel J. Theeuwes: Writing – original draft, Visualization, Investigation, Conceptualization. **Jimmy Melskens:** Writing – review & editing, Supervision, Investigation, Funding acquisition. **Wolfhard Beyer:** Writing – review & editing, Investigation. **Uwe Breuer:** Writing – review & editing, Investigation. **Lachlan E. Black:** Writing – review & editing, Investigation. **Wilhelmus J.H. Berghuis:** Writing – review & editing, Investigation. **Bart Macco:** Writing – review & editing, Supervision, Investigation, Funding acquisition. **Wilhelmus M.M. Kessels:** Writing – review & editing, Supervision, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

W.M.M. Kessels has patent pending to Eindhoven Technical University.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.solmat.2022.111911.

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