Hybrid Integration of VCSEL and 3-μm Silicon Waveguide Based on a Monolithic Lens System

Letters

Hybrid Integration of VCSEL and 3-μm Silicon Waveguide Based on a Monolithic Lens System

Chenhui Li, Srivathsa Bhat, Ripalta Stabile, Yuchen Song, Christian Neumeyr, and Oded Raz

***Abstract*— We design an optical interface system for vertical coupling between vertical-cavity surface-emitting lasers (VCSELs) and 3-μm silicon waveguides. The system includes a photoresist lens and a total internal reflection mirror, which allows for passive alignment and flip-chip bonding (FCB) of VCSELs. The simulated coupling loss is 0.7 dB, in optimal conditions, which increases to 1 dB when 3- and 20-μm alignment tolerances are considered in lateral and longitudinal directions, respectively. The system is built by post-processing lens and metallic wiring on the backside of a 3-μm silicon photonic platform. After FCB and embedding of the VCSELs, the system performance is characterized, and VCSEL-to-waveguide coupling efficiency of −7.5 dB is obtained.**

***Index Terms*— Flip-chip bonding (FCB), microlens, silicon photonic waveguide, vertical-cavity surface-emitting laser (VCSEL).**

I. Introduction

SILICON photonics research has been conducted for several decades and has become a mature technology for optical interconnect applications because of well-developed semiconductor processing technologies and large wafer sizes [1]. However, the diamond-cubic silicon crystal has an indirect bandgap, and, as a result, the silicon photonic integration platform is still limited by a lack of an efficient light source. Hybrid integration is a solution to complete the system, which combines the III–V material or semiconductor lasers with silicon photonic circuits [2]. In order to maximize the advantages of silicon photonic platforms, a low-cost and highly efficient coupling method is required.

Similar to the light coupling between fiber and silicon photonic chips, light from a semiconductor laser source can be integrated from the chip edges or surface. In the edge coupling scheme, a spot size converter (SSC) is required due to the modal mismatch between lasers and silicon waveguides. Both distributed feedback (DFB) lasers [3] and vertical cavity surface-emitting lasers (VCSELs) [4] have been assembled using the edge coupling method. To integrate the DFB, SSCs are designed on both waveguides, and a particular cavity is also fabricated on a silicon photonic chip to accommodate the laser die. These occupy a large area on the chip. VCSELs are attractive for optical interconnects due to their low power dissipation, low cost, and suitability for dense integration. Recently developed single-mode VCSELs are working in the *C*-band (1530–1560 nm), which can extend the applications of the VCSELs [5]. However, to assemble the VCSELs with waveguides from the edges, one of the dies must be vertically placed, which leads to complex packaging processes [4]. As an alternative, surface coupling may offer a better solution since VCSELs can be integrated on top of the silicon photonic dies using grating couplers. However, grating couplers operate in narrow bands and require light to arrive at an angle. To allow for such assembly, tilting VCSELs [6] or gratings couplers [7] have been proposed. Polymer prisms have also been used to tilt the incidence beam [8]. The difficulty in achieving the exact degree of assembly, as well as the inherent modal mismatch between VCSEL and grating couplers, has resulted in high coupling losses and small displacement tolerance in previous demonstrations.

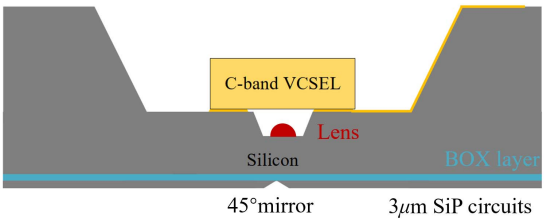

Fig. 1. Design of hybrid integration of VCSELs with the 3-μm silicon photonic platform.

Previously, we demonstrated, the 2.5-D and 3-D packaging of VCSELs on silicon interposers [9], [10], where the VCSELs can be embedded, and high-speed transmission lines can be patterned on the interposer surface, allowing for flip-chip bonding (FCB) of VCSEL and driving CMOS electronics. This letter proposes a novel integration approach for VCSELs based on a 3-μm-thick silicon-on-insulator (SOI) photonic platform [11]. The light coupling system is fabricated on the SOI wafers, including 45° downward mirrors on the photonic circuit side, as well as cavities and lenses on the substrate side. In this approach, the Gaussian beam from a VCSEL can be modified to match the mode in silicon photonic waveguide to achieve minimum coupling losses over a wide wavelength range (e.g., 1.2–4 μm). Furthermore, multiple inputs and outputs can be placed arbitrarily in the 2-D plane for sophisticated WDM system designs. Simulations have been conducted to define the parameters of the coupling system yielding an optimal coupling efficiency of −0.7 dB and alignment tolerance of $\pm$ 1.5 μm in the lateral and $\pm$ 10 μm in the longitudinal directions for −1-dB coupling efficiency. The assembly concept, working in the broadband and polarization independence, is then demonstrated by processing an SOI PIC sample. Finally, the optical performance of the system is measured by FCB VCSELs from the bottom side of the wafer and measuring the light output through the silicon waveguides.

II. Design and Simulation

The proposed integration scheme is shown in Fig. 1. The photonic circuits are patterned on the 3-μm-thick silicon layer with 45° mirrors at the ends of the waveguides. On the same SOI wafer, two cavities are formed from the substrate side to embed a VCSEL and a photoresist lens, respectively. Due to the layout of the VCSEL, the opening size of the lens cavity is limited to 70 μm × 70 μm square, which further limits the lens design, and the two cavities are

Manuscript received October 4, 2021; revised December 15, 2021, February 11, 2022, and March 12, 2022; accepted March 13, 2022. Date of publication March 16, 2022; date of current version May 25, 2022. This work was supported by the European Union's Horizon 2020 Research and Innovation Program under Grant Agreement PASSION 780326. Recommended for publication by Associate Editor C. Zhang upon evaluation of reviewers' comments. *(Corresponding author: Chenhui Li.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCPMT.2022.3160149.

Digital Object Identifier 10.1109/TCPMT.2022.3160149

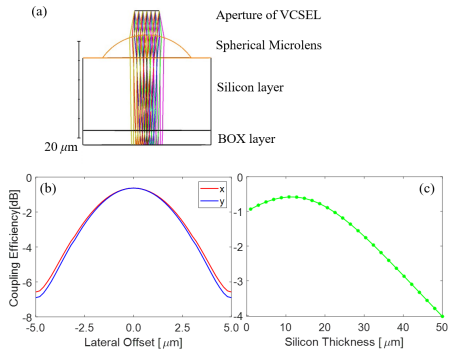

Fig. 2. (a) Zemax simulation model and the tolerance calculation results in x-, y- directions (b), and z- direction (c). The optimal coupling loss is 0.7 dB.

combined to accommodate the microlens system. The microlens is fabricated in the cavity on a wafer level. Silicon nitride, as the anti-reflection coating for the C-band laser, is deposited between the lens and VCSEL. After fabrication, FCB is used to integrate the VCSEL.

The refractive index of the baked photoresist is tested. First, a thin layer of positive photoresist (AZ®4562) is spun on a bare silicon wafer with 4000 rpm and baked in the same condition with the lens fabrication, at 300 °C. We fabricate the lens at such a high temperature to make the lens compatible with the following FCB process, which is processed at 280 °C. Then, an ellipsometer (M-2000, J. A. Woollam) is used to obtain the refractive index, which is 1.62 over the C-band range.

The micro-optical system is designed in Zemax OpticStudio with the Gaussian beam propagation method. The calculation model is shown in Fig. 2, including the VCSEL aperture, an air gap, a spherical photoresist lens, a silicon layer, and a buried oxide (BOX) layer.

In the lens model, the Gaussian beam (5.5-μm beam diameter, 10.2° beam divergence) from the VCSEL is collimated by a spherical photoresist lens, with the optimum radius of curvature (ROC) of 7.5 μm. The optimal image distance is defined by 3-μm BOX layer and remaining silicon layer is calculated to be 15 μm.

The mode fields in 3-μm SOI waveguides are tightly confined in the waveguide (3 μm × 3 μm), and the field distributions are almost the same for both TE and TM polarizations. The beam waists are 1.34 and 1.26 μm in x- and y-directions, respectively. With this layer arrangement, the best coupling loss is calculated to be −0.7 dB. In addition, we also simulate the placement tolerances. An extra −1-dB coupling loss is recorded for ± 1.5-μm displacement in the x- and y-directions [see Fig. 2(b)] and ± 10-μm variation in the thickness of silicon between the lens and the SOI waveguide [see Fig. 2(c)].

III. Fabrication

With the aiming parameters, the fabrication starts on a 6-in- and 3-μm-thick SOI wafer. First, the waveguides are defined, and then, the slot openings with 20 μm in length are patterned at the ends of the waveguides to form the wide mirrors. The tetramethylammonium hydroxide (TMAH) solution is used as the etchant for wet etching of total internal reflection (TIR) mirrors till the BOX layer. The schematic drawing and fabrication results are shown in Fig. 3. The SEM photograph demonstrates a smooth mirror that is formed by etching along a silicon crystal plane (110).

After the fabrication of photonic circuits, the wafer is diced into 40 mm × 40 mm samples for the process on the bottom side of the wafer. The cavities for VCSELs and lens embedding are patterned and formed by wet etching of silicon as well. A photoresist cylinder is patterned, inside the small cavity, by double-side lithography to achieve the best alignment accuracy. The lens is formed by reflowing the photoresist at 300 °C. Electronic circuits and bumps are patterned and plated along the etched facets. The process results

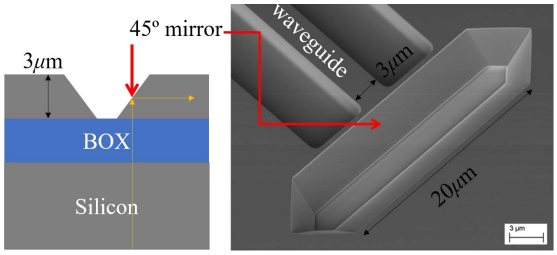

Fig. 3. Schematic drawing (left) and SEM photograph of the waveguide and the TIR mirror (right). The yellow arrows indicate the light path.

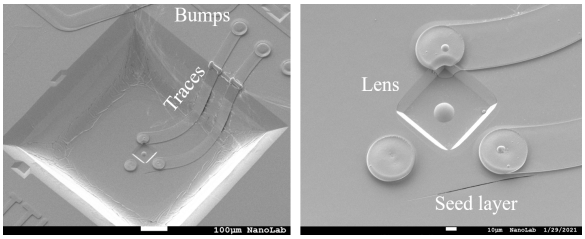

Fig. 4. SEM photographs before removing the plating seed layer: fabricated cavities for the single VCSEL (left). Zoom-in photograph of small cavity and lens and pads for VCSELs (right).

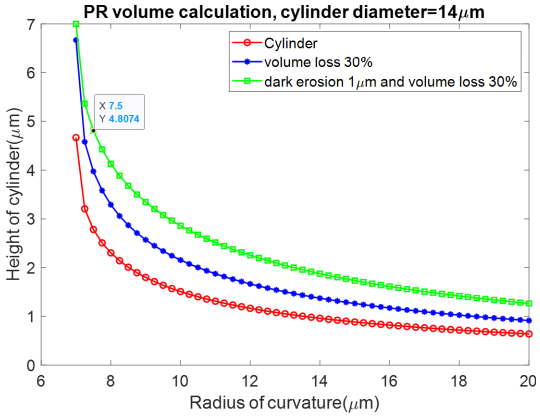

Fig. 5. Calculated cylinder height for the aimed ROC.

are shown in the photographs of the scanning electron microscope (SEM) with the plating seed layer, as shown in Fig. 4.

We creatively fabricate the microlens in etched cavities with standard lithography processes. During the reflow of the photoresist, the cylinder transforms to the spherical lens [12], and the height of the cylinder (thickness of the photoresist T) can be calculated from aimed ROC(R), lens height (h), and radius (r)

$$T = \frac{h^2}{3r^2}(3R - h).$$

In our process, the volume loss and dark erosion need to be considered. The volume loss of the photoresist during the reflow process (300 °C) is tested to be 30%. Dark erosion due to the gap between the lithographic mask and the photoresist in contact lithography is optimized to be 1 μm. After considering all effects that impact the volume of the patterned cylinder, the relation between the height of the cylinder and ROC is plotted in Fig. 5. From the calculation, 7.5-μm ROC after reflow can be achieved when the PR cylinder's thickness and diameter are 4.8 and 14 μm, respectively. To control the thickness of the photoresist, we use the small etched cavity, which works on a wafer level. The variation of the photoresist thickness in the small cavity is within 1 μm.

Three-dimensional mapping of the small cavity and microlens is obtained with a profilometer (DektakXT) with a scanning step of 1.0 μm and height resolution of 8.0 nm. The measurement results are shown in Fig. 6. We see that the small cavity is 11.9-μm deep and that the height of the microlens is measured to be 4.5 μm in both

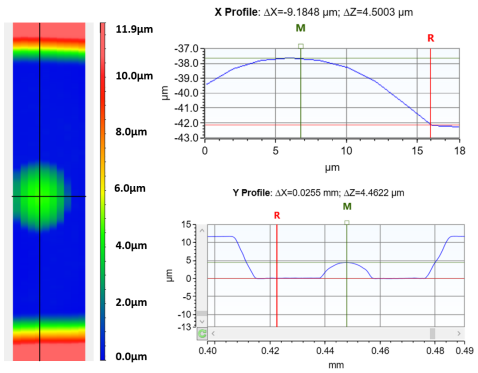

Fig. 6. Measured 3-D map for the lens in the small cavity, both x- and y-profiles indicate that the height of the microlens is 4.5 μm and the radius of curvature is 11.3 μm.

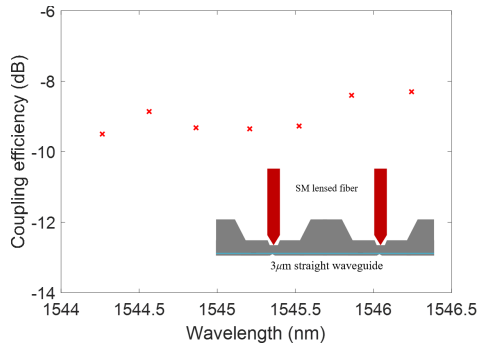

Fig. 7. Calibration measurement in the VCSEL tuning range by using two lensed fibers. Inset: test scheme shows two vertically aligned lensed fibers and mirrors on both sides of the straight waveguide.

the x- and y-directions, which are indicated in the 3-D map. The ROC of the lens can be calculated to be 11.3 μm, which is 3.8 μm larger than the design. The fabricated lens has a larger radius than the design due to the large gap between the mask and the photoresist in the lithography step. More photoresist has been developed away. Therefore, a defocusing compensation needs to be considered in the following process, and the volume can be increased by a thicker photoresist layer in the small cavity. We calculate the coupling loss to be −2.1 dB by building the model with the fabricated cavity and lens dimensions.

IV. Characterization

The 45° TIR mirrors are fabricated at both the input and output of a straight 3-μm waveguide to characterize the photonic circuit design. Two lensed fibers, with a 2-μm mode field diameter (MFD) at a focus distance of 12 μm, are placed vertically on top of the etched cavities, which are the locations of the 45° TIR mirrors. However, because of the thin layer of silicon (kept in place to ensure the correct imaging distance between the VCSEL and mirror), the fiber cannot be placed at the optimal distance from the TIR mirror, leading to high coupling loss shown in Fig. 7 (inset). The coupling loss is wavelength-dependent, and the lowest coupling loss of fiber to mirror is −8.2 dB. Here, we assume there is no loss on the 3-mm-long waveguide [11]. In future designs, the input and output will be patterned separately, such that the silicon layer at the output mirror will be further etched. Alternatively, a lens can also be designed and fabricated in the same reflow for the fiber coupling.

After characterizing the straight waveguides and mirrors, the single-mode VCSEL, working in the C-band, is passively aligned between the VCSEL apertures and photoresist lens and then flip-chip bonded with thermal compression bonding. The current–voltage curves of the VCSEL are compared in Fig. 8, before and after the

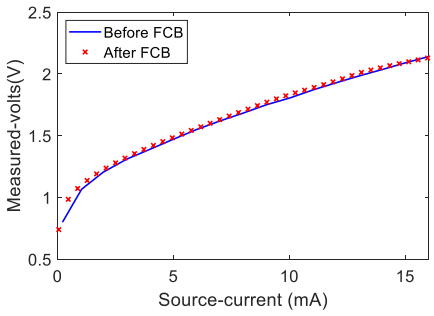

Fig. 8. IV curve of the VCSEL before and after bonding.

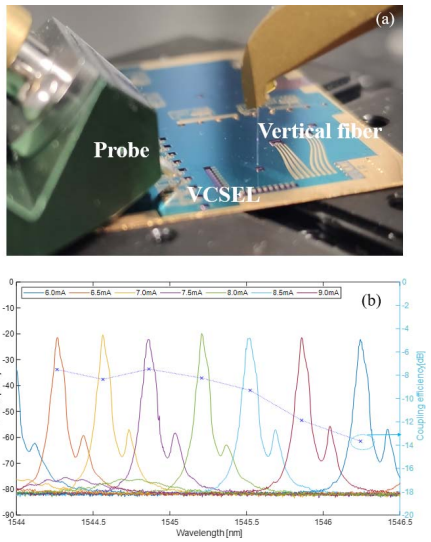

Fig. 9. (a) Testing setup with electronic probes at the VCSEL side and vertically aligned fiber at the output side. (b) Spectra measurement results after VCSEL bonding and the calculated power loss of the lens system.

FCB. The measurement result indicates that the VCSEL is well connected with the electronic circuits.

Finally, the coupling performance is tested, and the test setup is shown in Fig. 9(a). First, the spectra of the VCSEL are measured with changing current to identify the laser wavelength [13]. As shown in Fig. 9, from 6 to 9 mA, the wavelength shifts from 1544.26 to 1546.24 nm, and power increases from 1 to 3.3 dBm. By deducting the insertion loss of the fiber, the calculated lens system loss is shown in Fig. 9. The highest coupling efficiency is −7.5 dB. The reason for the extra losses is the alignment shift in the high-temperature bonding process. We use the updated lens model to determine the shift to be 3.5 μm. Therefore, low-temperature bonding or local heating techniques will be employed in the future.

V. Conclusion

In this letter, we have designed and demonstrated an integrated lens system capable of allowing the integration of VCSELs with silicon waveguides on one SOI wafer. The system is designed to have a high coupling efficiency (−0.7 dB) with improved bonding tolerance and can be utilized over a broadband wavelength range. The 45° TIR mirrors and photoresist microlens can be fabricated at any location on a wafer level to combine with any photonic circuits. The bottom side of the SOI wafer is utilized to make the high-speed electronic connections and the microlens.

In the future, the coupling efficiency (−7.5 dB) will be further improved by a better bonding technique. This platform and the integrated laser system will be used for many applications, including creating dense wavelength-division multiplexing (DWDM) transceivers and Lidar systems.

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