Co-design of the high-speed photonic and electronic integrated circuits

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Co-design of the high-speed photonic and electronic integrated circuits

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PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op dinsdag 14 December 2021 om 17:00 uur

door

Arezou Meighan

geboren te Teheran, Iran

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Het onderzoek of ontwerp dat in dit thesis wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

To my mother, my two sisters, my brother, and my two nieces.

Summary

The information age has been powered by electronic and photonic integrated circuits. The resulting digital revolution has made computers and mobile technology accessible to almost everyone. This creates a large amount of data that needs to be processed and transferred around the globe. Optical fibers and photonic circuits provided the required technology for doing that at high capacity and speed. So far, the increase in data capacity has been exponential, but we now see major technology challenges in terms of bandwidth and energy efficiency.

At the heart of these information processing and transport technologies, optical transceivers convert data from the electrical to the optical domain and are made from photonic and electronic integrated circuits. Electronic integrated circuits (EICs) and photonic integrated circuits (PICs) are usually made in different technology and are connected afterward to form a module. The connection between these technologies is now becoming a major performance bottleneck. To increase the transmission speed, the speed of both EICs and PICs and that of the interface has to be re-invented. Moreover, compact co-integrated transceivers with a small footprint that minimizes interface losses is crucial to allow increased bandwidth and reduced energy use.

This work's central question is: **Can close co-integration of the electronic and photonic circuits increase high-speed performance?**

To answer this work's research question, first, the modulator's building blocks' physical limits are studied. The scope of the thesis includes coplanar stripline (CPS) and hybrid coplanar waveguide (HCPW) designs. After getting knowledge of the critical parameters affecting the modulator's high-speed performance, a co-design environment that can involve the electronic, photonic, and interconnects circuits between them is developed. A compact, very high-speed CPS modulator with a small footprint that can minimize the interface losses between the co-integrated electronic to photonic circuits is proposed. A high-speed packaging technique is then developed to interconnect the two devices. Finally, co-design photonic cells for evaluating the methods are designed. In the following, the details of this research are described.

Co-integrated transceivers usually contain electronic drivers and photonic modulators. In this work, a high-speed Mach Zehnder Modulator (MZM) does the electro-optical modulation. Starting with studying the effects of the physical and mask parameters on the electri-

cal characteristics of the hybrid coplanar waveguide (HCPW) modulator's building block, such as line impedance, microwave index, and electrical bandwidth, a compact model consisting a full field 3D tool and analytical equations is introduced to calculate the modulator's electro-optical response. Then, the cross-sectional and mask parameters' effect on the modulator's 3dB electro-optical bandwidth is discussed and validated by comparing it to a fabricated reference device. The critical cross-sectional parameters that have a high impact on the electro-optical performance are identified. This optimization leads to a parameter set, enabling an electro-optical bandwidth of 120 GHz, which is more than four times the reference device's bandwidth. However, this design requires epitaxial changes and can not be realized in the available generic technology, preventing direct validation.

A co-design environment is then developed for studying the modulator's high-speed small and large signal performance when intimately interconnected with the driver and termination circuits. For that, first, a non-iterative spatially resolved electrical circuit model for the modulator building block is introduced and validated. Importantly this circuit model is non-iterative, so it enables the co-design environment to study the co-optimized EICs and interconnect circuits on the performance of the MZMs. This enables explicitly quick large-signal calculations, which usually take long-computation-time in the other methods such as full-field calculations. To demonstrate the power of the co-design environment, an equalization circuit is designed and co-simulated. This interconnection circuit doubles the 3dB bandwidth and increases the eye quality.

Validation of new design concepts is most readily demonstrated with the generic foundry technology, which is commercially available at SMART Photonics. The high-speed performance of the HCPW-MZM was not achievable with the current technology, and these devices have a large footprint. To increase the electro-optical bandwidth of the MZMs using the generic foundry technology, the coplanar stripline (CPS) electrode design is studied. This electrode design has smaller dimensions than the conventional capacitively-loaded or coplanar waveguide MZMs. It has a higher line impedance and has a lower refractive index than coplanar waveguide MZMs; therefore, it has a lower electrical reflection in the interfaces between the EICs and PICs and closer electro-optical velocity matching. The effect of the substrate and the three main mask parameters and substrate on these modulators' performance is studied. A high-density, 27 μm wide, CPS Mach-Zehnder modulator with velocity and impedance matching, increasing the 3dB electro-optical bandwidth to 27.3 GHz, 3.6 times higher than a more conventional HCPW-MZM with similar length, substrate and waveguide parameters is assessed. This design was bandwidth limited by the n-doped substrate. The design is adapted to a semi-insulating substrate, and an active-passive process has been implemented. High-density and high-speed CPS modulators with a 1.4 dB electro-optic modulation bandwidth of 67 GHz are demonstrated on a generic foundry platform with the semi-insulating substrate. The modulator electrode design is miniaturized to allow a high packaging density with a Mach-Zehnder pitch of below 25 microns. Moreover, to increase the modulators' co-design flexibility to the electrical interfaces, a high-density and high-speed tapered CPS-MZM with different input and output impedances is introduced and experimentally assessed.

Wafer bonding enables the physically-close co-integration of the electronic to photonic devices on wafers with different technologies. Distances between bond pads can be reduced to microns, and bond-wires can be removed from the assembly. The concept studied in this thesis is compatible with wafer and die bonding of electronic and photonic circuits to each other. Adhesive wafer bonding requires a layer to bond the two wafers. In this research, methods for metal interconnection are developed for the polymer bonding layer. The mechanical reliability of these through polymer vias in the presence of the temperature cycle is tested. The electrical performance is assessed from scattering parameters of vias. These short vias show a very high-speed performance with less than 1 dB electrical loss in the measurement range of 67 GHz.

The effect of the interconnects between the electronic to photonic integrated circuits is studied. Co-design photonic cells for comparison of these techniques have been designed. Using the co-design environment, the modulator's high-speed performance, packaged by the high speed through polymer vias, was theoretically compared to the state of art stud bonding and wire bonding packaging techniques. This comparison confirms that the close co-integration of the electronic to photonic circuits enhances high-speed performance.

For increasing the high speed MZMs performance, modulators often have to be terminated to a proper termination circuit. An ideal termination has an infinite capacitance while in practice capacitance value is limited. The effect of the termination capacitance is studied. Then the measurement data of an on-chip termination fabricated in a generic InP platform with semi-insulating substrate is combined with the spatially resolved circuit model of the HCPW-MZM and EO-frequency response of the MZM is simulated. This termination is suitable for K-band applications with a frequency range of 18-27 GHz.

The high-speed modulator design and high-speed through-polymer-via technology research presented in this thesis identifies performance increases in terms of energy, bandwidth and density, which are achievable through the close integration and co-design of electrical and photonic circuits. Using the co-design environment introduced in this work and anticipating the increasing manufacturing processing accuracy, new possibilities are emerging for much faster and denser co-integrated photonic to electronic devices.

List of acronyms

AC	Alternating Current
ADS	Advanced Design System
ALD	Atomic layer deposition
BB	Building Block
BCB	Benzo-Cyclo-Butene
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BW	Bandwidth
CEO	Compact Electro Optical
CMOS	Complementary Metal–Oxide–Semiconductor
CPS	Co-Planar Stripline
CPW	Co-Planar Waveguide
DC	Direct Current
DFB	Distributed FeedBack
DHBT	Double Heterojunction Bipolar Transistor
DLM	Directly Modulation Laser
E	Electrical
EAM	Electro-Absorption Modulator
EDFA	Erbium Doped Fiber Amplifier
EIC	Electronic Integrated Circuit
EM	Electro-Magnetic
EML	Electro-Absorption Modulated Laser
EO	Electro-Optical
FEM	Finite Element Method
GSG	Ground Signal Ground
HCPW	Hybrid Co-Planar Waveguide
HCSEL	Horizontal-Cavity Surface-Emitting Lasers
IC	Integrated Circuit
IL	Insertion Loss
IMOS	InP-Membrane-On-Silicon
InGaAs	Indium Gallium Arsenide
InP	Indium Phosphide
JePPiX	Joint European Platform for InP-based Photonic Integrated Components & Circuits

LaMP	Laser Micro Printing
LED	Light-Emitting Diode
MEMS	Micro-Electro-Mechanical Systems
MMI	Multi Mode Interference
MPW	Multi-Project Wafer
MQW	Multi quantum-well
MZM	Mach-Zehnder modulator
NRZ	Non-Return-To-Zero
OCT	On-Chip Termination
OOK	On-Off-Keying
PC	Polarization Controller
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PIC	Photonic Integrated Circuit
PM	Phase modulator
PRBS	Pseudo-Random Bit Sequence
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SI	Semi-Insulating
Si	Silicon
SMF	Single Mode Fiber
SNR	Signal-to-Noise Ratio
SOLT	Short-Open-Load-Thru
TCPS	Tapered Co-Planar Stripline
TEM	Transverse electromagnetic
TML	Transmission Line
TPV	Through Polymer Vias
TRL	Thru-Reflect-Line
TSV	Through Silicon Via
TWE	Traveling-Wave Electrode
VNA	Vector Network Analyzer

Contents

Chapter 1

Introduction

1.1 Abstract

State-of-the-art optical transceiver technologies are introduced in the context of ever-growing demands on data services. New integration concepts are required to sustain increases in bandwidth within the same chip area and with sustainable energy use. The latest concepts in optical and electronic interconnection technologies are reviewed. Research questions concerning density and speed are identified. Then the research question is explained, followed by the outline of each chapter.

1.2 Optical transceivers

In our daily life, from using social media to do bank transactions, we use data communication. As a result, more traffic will be created in 2022 than in the 32 years since the Internet started, and the number of devices connected to IP networks will be more than three times the global population by 2023 [1]. Photonic integration is a solution for the high demand for data communication. Photonic Integrated Circuit (PIC) concept is the same as Electronic Integrated Circuit (EICs). The main difference is that an EIC includes electrical building blocks to generate electrical data, while a PIC includes optical building blocks to manipulate light.

In order to transfer information through optical fibers, in optical communication systems, electrical information has to be converted to light. Optical transmitters generate optical carriers and modulate those carriers with broadband, and high-speed electrical signals [2]. Optical transceivers include both electronic integrated circuits (EIC) and photonic integrated circuits (PIC). Electrical components such as driver amplifiers and biasing circuits can be implemented into a single electronic integrated chip and are commonly fabricated with silicon technology. PICs are commonly made in III-V platforms such as InP or silicon photonic platforms.

Silicon photonics can leverage CMOS processes and provides a route to cost-effective volume manufacturing. However, silicon photonics can not produce lasers and optical amplifiers that are fundamental components for generating and amplifying light, respectively [3].

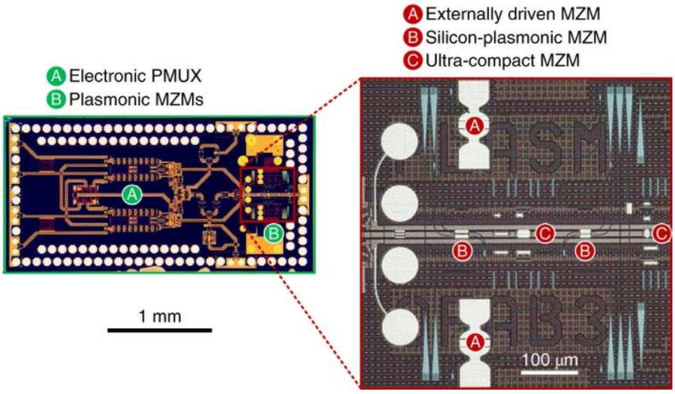
InP photonic platform includes photonic components such as modulators, photo-detectors, and waveguides monolithically integrated with the laser source in a single photonic chip. InP-based monolithic integration offers the most comprehensive range of photonic functionality with high-energy-efficiency quantum well lasers and modulators, as well as optical amplifiers, detectors, and a range of passive components for creating interferometers, combiners, and modulators [4].
In high-speed optical transceivers, modulator components convert information from the electrical domain into the optical domain. Modulators are in any optical transmitter and significantly influence the specifications and the performance of the transceivers, such as speed, power consumption, output power, and extinction ratio. Therefore, advancements in modulators are crucial for achieving high-speed transmitters.

1.3 Broadband high-speed modulators

Optical modulation can directly or indirectly modulate the optical signal generated by the laser source. There are three main methods to achieve optical intensity modulation as follows.

- Directly modulation lasers (DMLs) are the first generation of optical modulators. An applied electrical signal directly modulates the power and switches the laser intensity between high and low power states. The advantage of direct modulation is simplicity. However, broadband modulation is limited by complex dynamics. Additionally wavelength changes during modulation limit transmission distances.
- Electro-absorption modulators (EAMs) modulate light by voltage tuning the absorption edge in a reverse biased waveguide light with a relatively low voltage. The EAMs drawback is also optical chirp inside the component that can be minimized by careful design. Other disadvantages of EAMs are operation wavelength dependency and power handling capacity. However, these optical modulators are attractive due to the small size and integration capacity with the lasers (electro-absorption modulated lasers).
- In a Mach Zehnder modulator (MZM), a light splitter splits the input optical signal into two signals. Then, optical signals propagate through two waveguides. While propagating, the optical phase of the two optical signals can be modulated by the voltages applied to one or two waveguides. Then an optical combiner component combines the optical signals of the two waveguides and superimposes them at the output. The output light intensity depends on the constructive or destructive interference between the optical phase delay incurred by the two waveguides of the MZM. MZM can be designed for zero, or negative chirp [5]. The chirp of the MZM output optical signal can be controlled by the propagation constants in the two waveguides of the MZM. By designing the two waveguides with equal propagation constant magnitudes and different signs, zero chirp can be achieved [6]. Therefore, in long-haul applications, where zero chirp is required, MZMs are preferred over EAMs. One drawback of the MZMs is the commonly long length of these modulators, which results in a large footprint. Moreover, for high-speed applications, careful electrode designs are needed to minimize capacitance.

For high-speed modulation, MZMs with high-density electrode size, extensive bandwidth, high efficiency, compatible with $50\,\Omega$ impedance and compact are required. In this chapter, we look at MZMs in the various integration platforms and specifically address the compromises made when integrating optical and electrical components.



a) b)

Figure 1.1: a) Top view of the monolithically integrated electronic and photonic circuit. b) Plasmonic MZM on top of the electrical driver [7]

MZMs with modulation speed above 50 GHz have been realized in silicon photonics [8]. High-speed carrier depletion MZMs with co-planar stripline traveling wave electrode in combination with horizontal p-i-n junctions for silicon photonics have been fabricated in silicon photonics [9–12]. This resulted in 50 Gb/s on-off-keying (OOK) for modulator with 2 mm phase-shifter and about 180 μm width [11] and 64 Gb/s quadrature phase shift keying (QPSK) for a modulator with 3.5 mm phase-shifter [9]. Silicon photonics can include the monolithic integration of the electrical circuit and MZM made in a silicon platform. For example, bipolar complementary metal-oxide-semiconductor (BiCMOS) electronics and silicon plasmonics are used to produce the plasmonic MZMs monolithically integrated with the electrical driver. Figure 1.1 shows a) top view of the monolithically integrated electronic and photonic circuits and b) plasmonic MZM on top of the electrical driver [7]. High-speed SiGe BiCMOS electronic layers with a top plasmonic layer monolithically integrated on a common substrate and connected through electrical vias. Plasmonic MZMs on the top optical layer converts the electrical signals onto intensity-modulated optical signals [7]. These ultra-compact plasmonic MZMs with footprints smaller than 100 μm are monolithically integrated into an electrical driver with V_{rms}=1.55 V. These plasmonic MZMs show a high symbol rate of 100 Gbd with a signal quality of 16 dB signal-to-noise ratio (SNR). However, the insertion loss of these modulators is in the range of 27-30 dB, which is significantly high. Moreover, since the silicon platform can not include active optical components, off-chip laser sources have to be optically packaged for using these modulators in the optical transceivers.

InP platform has the potential for the monolithic integration of the laser source to the modulator. MZM components have been studied in the generic InP platform [15]. The bandwidth is constrained by high electrical loss in these hybrid coplanar waveguide (HCPW) electrode designs, and the line impedance is limited to 25 Ω [16] at high frequencies [17], leading to undesired electrical reflections. Also, these modulators have microwave indexes

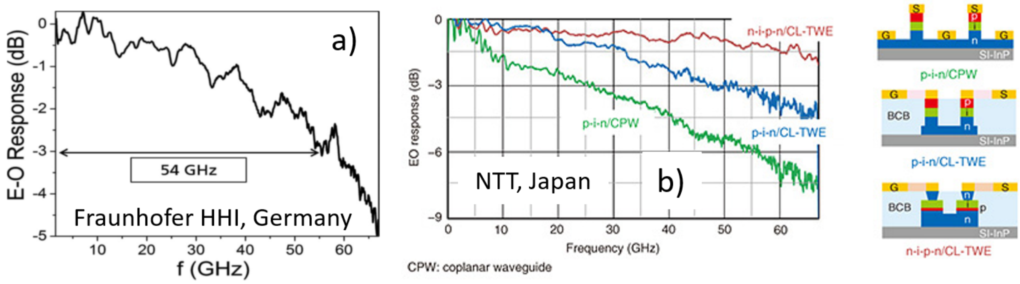


Figure 1.2: State of art a) Capacitively-loaded electrode MZM fabricated by HHI [13] and b) NNT [14]

of about 1.5 times the optical index, which results in the walk-off between the electrical and optical signals. Capacitively-loaded Mach-Zehnder modulators are widely used in transmission systems due to their fast modulation speed, and large optical extinction [18]. Figure 1.2 shows state of art a) 54 GHz capacitively-loaded electrode MZM fabricated in HHI [13] with the footprint of $10 \times 0.5\ mm^2$ and b) n-i-p-n capacitively-loaded MZMs designed and fabricated by NTT [14] and in III-V material platforms. However, these are physically large with over 50 μm modulator width.

1.4 State of the art interconnection technologies

In the optical transceivers, the individual PICs and EICs have to be properly interconnected to make a single module. Optical and electrical interconnections are the two main interconnect categories used. Silicon Photonics can potentially be monolithically integrated into the EICs; on the other hand, in InP photonics, the laser source can be monolithically integrated into the rest of the photonic circuit in a single chip. However, high-speed electrical connections have to be later done to the EICs. Here, we review the current state-of-the-art technologies for photonic and electronic interconnections and their potential challenges.

1.4.1 Optical interconnection

Transfer printing, Laser Micro Printing (LaMP), and photonic wire-bonding are three state-of-the-art technologies for interconnecting the off-chip light source to silicon photonic circuits.

Figure 1.3 shows the schematic of the transfer printing method [19]. A transfer stamp, a source substrate printable chips, and a non-native target substrate are required for the transfer printing. In this method, first, the printable chips are transferred onto the stamp. Then chips on the stamp are printed to the non-native target substrate. In Figure 1.4 we see an example of using the transfer printing method. In this figure, the InP laser is transfer printed to the passive silicon photonics [20].

LaMP optical packaging technology is shown in figure 1.5 [21]. Perspective view of hermetic silicon LaMP is showed on the left, and a section of LaMP showing beam path is showed on the right. The LaMP technique is used for the commercial packaging of the

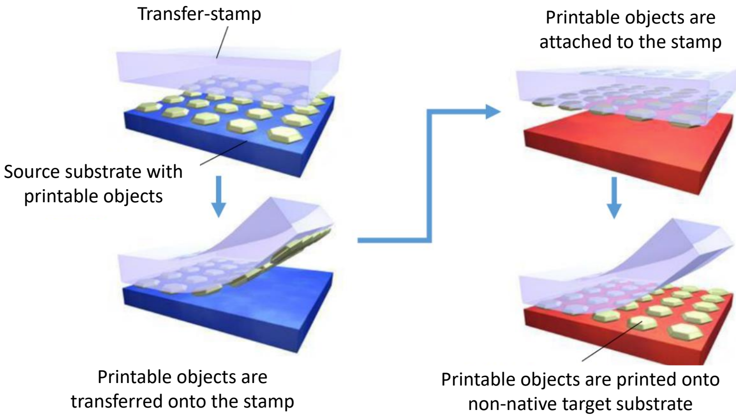


Figure 1.3: Schematic of the transfer printing method [19]

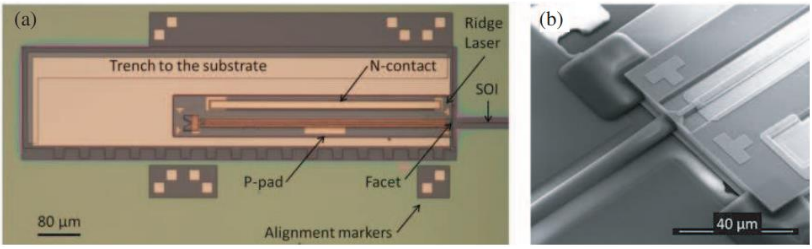


Figure 1.4: Transfer-printing of the InP laser to the silicon photonics [20].

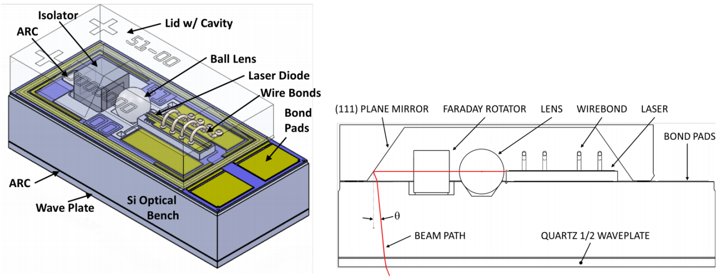


Figure 1.5: (Left) Perspective view of hermetic silicon LaMP, (right) section of LaMP showing beam path [21].

distributed feedback (DFB) laser chip. In the LaMP method, a ball lens and a Faraday rotatory are placed after the laser diode's optical output, focusing the light on the mirror and reflecting light to the silicon photonics optical circuit below.

Photonic wire-bonding technology is used by the Institute of Integrated Photonics (IPH) for photonic interconnection of the off-chip light source to the silicon photonic chip [22]. Figure 1.6 shows the concept of the photonic wire-bond, which optically connects the InP chips, silicon photonic p-n modulators, and single-mode fibers (SMF), all with photonic wire-bonds (PWBs). (1) Micrograph of one out of eight fabricated PWBs connecting the InP laser arrays to silicon photonic chip. (2) Micrograph of two PWBs out of eight connecting the SOI chip to SMF.

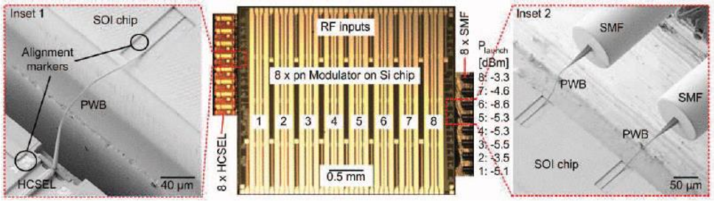


Figure 1.6: The concept of the photonic wire-bond optically connects the InP chips, silicon photonic p-n modulators, and single-mode fibers (SMF), all with photonic wire-bonds (PWBs). (1) Micrograph of one out of eight fabricated PWBs connecting the InP laser arrays to silicon photonic chip. (2) Micrograph of two PWBs out of eight connecting the SOI chip to SMF [22].

In figure 1.6 a silicon photonic die includes 8 travelling-wave carrier-depletion MZMs. Horizontal-cavity surface-emitting lasers (HCSEL) that contain InGaAsP distributed feedback (DFB) that have 45° mirrors for deflecting the light to a direction normal to the substrate plane [22]. The HCSEL is placed next to the photonic chip and has a wavelength around 1550 nm. The optical output of the MZMs is coupled to an array of 8 single-mode fibers. This module transmits 28 GBd PAM-4 signals at a total data rate of 448 Gbit/s.
Optical interconnection of the off-chip light source often suffers from relatively significant coupling losses between the off-chip light source and the silicon photonic chip [23]. Moreover, packaging expenses are usually high. This motivates the use of a generic active passive integration platform to remove the complexity of photonic connections inside the circuit and allow miniaturisation

1.4.2 Electrical interconnection

Electrical wire-bonds or flip-chip technologies are widely used for the electrical interconnection of the PICs to the EICs. Here we review examples of these two techniques and their potential advantages and disadvantages for electrical interconnections.
Wire-bonding is still the most flexible and cost-effective electrical interconnect technology packaging the micro-systems [24, 25]. Wire-bonding is also used for electrical connection of the high-speed InP PICs and BiCMOS EICs [26]. Figure 1.7 shows the realization of the wire-bonded BiCMOS driver and the EAM sub-assembly. In this figure, both BiCMOS driver EIC and the InP EAM PIC are mounted on a CuW carrier. The driver output pads are directly interconnected to the signal pad of the EAM by wire-bonds, and ribbon bond wires are used for interconnection of the EAM to the EAM submount. In figure 1.7 we see that the dimensions of the EAM are much smaller than the electrical submount and the rest of the package. One of the main disadvantages of the wire-bonding technique is the bandwidth limitation due to the electrical parasitics of the bond wires. Also, physically big counterpart bond-pads on the ICs and side-by-side placement of the ICs results in a big footprint of the bonded EICs and PICs. Moreover, this interconnection technique can not be used for wafer-scale co-integration of the EICs and PICs.

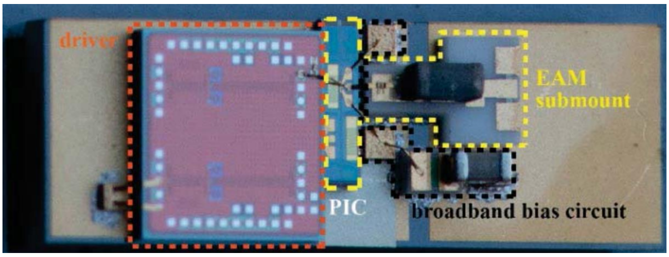


Figure 1.7: Realization of the wire-bonded BiCMOS driver and the EAM sub-assembly [26].

Flip-chip provides excellent performance and allows a cost-effective interconnect technique for dice with a high number of electrical inputs/outputs [25]. In flip-chip mounting, contact bumps electrically, mechanically, and thermally connect the pads on a die to the counterpart pads on a second die, a carrier, or a substrate wafer. An example of a reliable high count on wafer-level assembly using flip-chip bonding is the assembly of the 576 high brightness LED dice on a 4-in substrate wafer [27]. Another example of flip-chip assembly is shown in figure 1.8 [28], where the EICs and PICs are electrically interconnected. The photonic chip includes the photonic components such as phase modulators splitter and balanced UTC photo-diode. The schematic of the PIC and EICs and counterpart electrical pads designed for flip-chip bonding are showed in figure 1.8, a) and the PIC layout is depicted in figure 1.8, b) which shows big pad sizes compared to the electrodes.

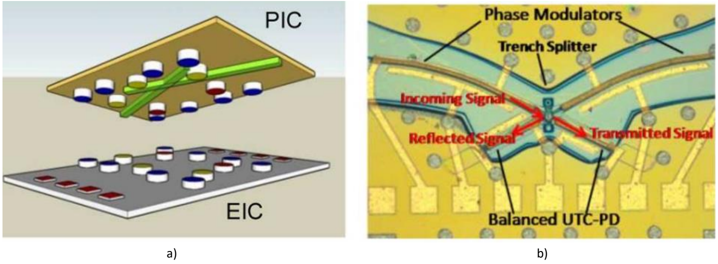


Figure 1.8: a) Schematic of flip-chipping of electronic and photonic ICs. b) Layout of the PIC [28].

Flip-chip technology can efficiently make metal interconnects on the die level. In flip-chip bonding, the electrodes of the ICs are usually not directly bonded, and pads/tapers are often needed. This can reduce the electrical bandwidth and minimize the density of the co-designed devices. The challenge of flip-chip is variability in assembly, and therefore we look at lithographically defined schemes to remove variability.

1.4.3 Wafer-scale electronic photonic co-integration

Here we show a concept for co-integration of the high-speed photonic to electronic ICs at the wafer-scale. Wafer-scale adhesive bonding co-integration of the InP EICs to the SiGe BiCMOS EICs is successfully done [29]. High-speed through polymer interconnects between the InP double heterojunction bipolar transistor (DHBT), and SiGe BiCMOS electronic ICs are done to combine the advantages of both high bandwidth BiCMOS analog and digital circuits and high output power of InP DHBT amplification and mixing stages. Signal sources operating at up to 330 GHz were demonstrated [29].

A wafer level integration of the InP wafer adhesivly bonded with a silicon wafer has been done in the InP membrane on silicon (IMOS) platform [30, 31]. IMOS uses the high refractive index contrast with the underlying adhesive polymer to form an environment for fabrication of full high-density InP photonic. In the IMOS platform, the silicon wafer is used only as a carrier, but this platform has the potential of integration with a CMOS wafer for realization of the photonic electronic co-integration.

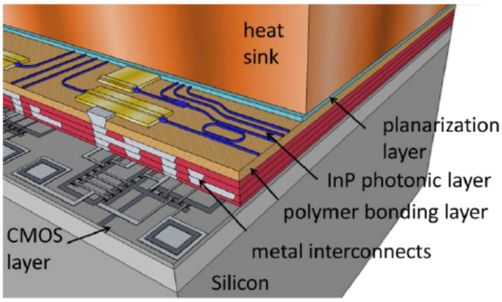


Figure 1.9: Schematic diagram of the InP PICs co-integrated to the CMOS EICs with wafer to wafer bonding.

Figure 1.9 shows a schematic diagram for the chosen concept of electronic-photonic co-integration. The lower CMOS layer is shown with electronic driver circuits and a fully processed high-performance InP photonic layer that is aligned and attached with a polymer bonding layer. The main difference of this concept with IMOS is that the PIC and EIC are made independently and had been bonded later. The substrate of the photonic circuit is removed, leaving a thin PIC structure with optical inputs and outputs. The electrical connection relies on the creation of metal vias through the polymer bonding layer between the silicon and InP. A polymer adhesion layer thickness of 2-30 μm is required to obtain a mechanically strong structure that provides appropriate electrical isolation.

This wafer-scale co-integration technique can potentially make direct metal connections between the high-speed PICs and EICs, and extra bond pads/tapers are not needed.

1.5 Aim of the thesis

This thesis aims to answer the following central question.

Can close co-integration of the electronic and photonic circuits increase high-speed performance?

To answer this question, this thesis includes the following four sub-questions.

- Which cross-sectional parameters in the MZM building block have a high impact on the electro-optical performance of the modulator?
- What are the density and speed limits of the generic InP platform?

- Can we build a co-design environment to explore the benefit of electronic to photonic co-integration?

- What is limiting the 3D-integration of the photonic and electronic ICs?

1.6 Thesis outline

The outline of the thesis is given as follows:

- **Chapter 2** explores the effects of the physical and mask parameters on the electrical characteristics of the HCPW modulator's building block. A simple combined model is introduced to calculate the electro-optical small-signal response of the modulator building block. The critical cross-sectional parameters that have a high impact on the electro-optical performance are identified. This optimization leads to a parameter set, enabling an electro-optical bandwidth of 120 GHz.

- **Chapter 3** introduces a co-design environment for studying the modulator's high-speed small and large signal performance when intimately interconnected with the driver and termination circuits. A non-iterative spatially resolved electrical circuit model for the modulator building block is introduced and validated. This circuit model enables the co-design environment to study the co-optimized EICs and interconnect circuits on the small and large signal responses of the MZMs. To demonstrate the capabilities of the co-design environment, an equalization circuit is designed and co-simulated. This interconnection circuit is predicted to double the large-signal modulation bandwidth of the previously reported MZM to 80 Gbit/s for on-off-keyed modulation.

- In **Chapter 4**, in order to increase the density and electro-optical bandwidth of the MZMs using the generic foundry technology, the coplanar stripline (CPS) electrode design is studied. This novel electrode design has smaller dimensions than the conventional capacitively-loaded or coplanar waveguide MZMs. It has a higher line impedance and has a lower refractive index than coplanar waveguide MZMs; therefore, it has a lower electrical reflection in the interfaces between the EICs and PICs and closer electro-optical velocity matching. The effect of the three main design-critical parameters on these modulators' performance is studied. A high-density CPS Mach-Zehnder modulator fabricated in the n+ substrate is experimentally compared to a more conventional HCPW-MZM in the same platform in terms of velocity and impedance matching. Since the n-doped substrate limited the bandwidth of the CPS-MZM, the design is adapted to a semi-insulating substrate, and a best-in-class high-density 100 GHz class CPS modulator is demonstrated.

- **Chapter 5** develops methods for metal interconnection of the electronic to photonic integrated circuits through the polymer bonding layer. The mechanical reliability of these through polymer vias in the presence of temperature cycling is tested. The electrical performance is assessed from scattering parameters of vias. For smaller, more compact structures with lower parasitic, atomic layer deposition is introduced to create a seed layer for a steep sidewall through polymer vias.

- **Chapter 6** studies the co-integration of the high-speed modulator PICs to the driver EICs. First, the effect of state-of-the-art interconnect technologies between the electronic to photonic integrated circuits is studied. Then, using the co-design environment, the modulator's high-speed performance, interconnected by the high-speed through polymer vias, was theoretically compared to the state of art flip-chip bonding and wire-bonding interconnect techniques. Then, a co-design photonic cell for comparison of these techniques has been designed. Since, for achieving high bandwidth, high-speed MZMs have to be terminated to a proper termination circuit, the effect of the termination capacitance on the EO-responses of the HCPW-MZM is studied. Moreover, for increasing the modulators' co-design flexibility to the electrical interfaces, a high-density and high-speed tapered CPS-MZM with different input and output impedances is introduced and experimentally assessed.

- Finally, **Chapter 7** summarizes the main achievements of this thesis and gives an outlook on possible directions for future research. This thesis has a pathway to multi-Terabit picoJoule/bit systems.

Chapter 2

Geometrical analysis of the phase-modulator building block

2.1 Abstract

The growth in bandwidth-demanding applications such as cloud computing and online information exchange requires high-speed communication through the optical fiber system. At the same time, the fraction of energy used for handling information has risen to an environmentally significant level [32]. In fiber-optic networks, high-speed electro-optical modulators are crucial components of the transceivers. Mach–Zehnder modulators (MZMs) have high-speed modulation, and low power consumption compared to electro-absorption modulators [33], which leads to their widespread use in high-speed transceivers. In the phase-shifter section of the MZMs, a high-speed electrical signal is sent via an electrical traveling wave electrode along with an optical waveguide that modulates the modulator's light. Coplanar waveguide (CPW) traveling wave electrodes are widely used to carry high-speed radio frequency electrical signals.

In this work, we focus on the power consumption and speed of the CPW-MZMs building block in the indium phosphide (InP) platform, and we addressed the following question:

How can we reduce the power consumption and increase the electro-optical bandwidth of the MZMs by engineering only the phase-shifter building block cross-section?

Answering this question requires fast physical modeling approaches. We propose an analytical model and use that in combination with a 3D simulation tool. The electrical model is validated by comparing it with the experimental results of a reference modulator. For evaluating the electrical performance limits of the MZMs, wide-sweep variable analyses are performed. Starting from the premise that higher impedance systems enable reduced power loss because V^2/R losses are reduced, we study methods to engineer the characteristic impedance of the MZM. We then explore ways to achieve velocity matching, since the optical efficiency is greatest when the electrical and optical indexes are matched. As high-speed modulators require traveling wave electrodes with high electrical bandwidth, we study methods to increase the electrical bandwidth. To identify what limits the elec-

trical bandwidths, we also see where the electrical loss is dominant along the modulator's transmission traveling wave electrode.

To see the modulator's small-signal electro-optical-response, we introduce a compact electro-optical model that analytically calculates the electro-optical frequency response of the modulator. Inputs of this model are simply the mask and cross-sectional parameters of the modulator, and no fitting or calibration was applied. We validate this model by comparing it with the measurement data of the reference modulator. The reference modulator has electro-optical bandwidth of 30 GHz, which is measured in the 50 Ω source and termination conditions. Using this model, we show the effect of the wide range of parameters on the optical 3 dB electro-optical bandwidth of the MZM.

Finally, we propose a parameter set that results in a modulator design, with 3 dB electro-optical bandwidth of 120 GHz in the matched termination source condition and 87 GHz when termination and termination are 50 Ω. This is significantly higher than the electro-optical bandwidth of the reference modulator (30 GHz).

2.2 Introduction

To properly design Mach–Zehnder modulators (MZMs) for high-speed applications, accurate modeling, and simulation tools are needed that capture both the microwave signal propagation and the electro-optic interactions. Modeling approaches exist that are based on large iterative EM simulation [34] or the method of lines [35], which can become very complex in nature. In this work, by using a fast 3D electromagnetic simulation (CST Microwave Studio [36]), we create an electrical model and study the frequency-dependent electrical characteristics of the MZM in a wide range of physical and dimensional parameters. Then, by using the characteristic impedance and propagation constant derived from the electrical model, we introduce a compact electro-optical model that analytically calculates the small signal electro-optical frequency response of the MZM. Afterward, we study the effect of the mask and cross-sectional parameters on the 3 dB electro-optical bandwidth of the MZM. To accomplish this study, the focus of this chapter is divided into the following order.

In section 2.3, we define a model to calculate the frequency-dependent electrical characteristics. We validate our approach by comparing the simulation results with experimental results of a reference design, and we show that our simple model can yield accurate predictions.

Section 2.4 describes how higher characteristic impedance results in lower resistive power consumption. It also shows the importance of impedance matching for reducing the electrical reflection and increasing the electrical transmission. Then it introduces two mechanisms for enhancing the characteristic impedance of the MZMs.

Since matching the velocity of the electrical and optical signal of the MZMs results in higher electro-optical bandwidth, in section 2.5 we study how to engineer the microwave index of the MZMs. We also introduce two mechanisms of reducing the microwave index toward the optical index.

In section 2.6 we look at the radio frequency (RF) loss in both semiconductor and metal regions of the modulator's building block to gain insight into the source of the RF loss. We also show the changes in the 3 dB electrical bandwidth of the MZMs in the sweep of a wide range of parameters.

In section 2.7, we develop insight and map wide parameter spaces on the MZM's EO-response by using the simple, compact electro-optical model described in 2.3. Understanding the effect of cross-sectional parameters on the MZM's electrical and electro-optical frequency-dependent characteristics, led us to propose a parameter set for a high-speed MZM design in section 2.8, which result in the 3 dBo electro-optical bandwidth of 120 GHz.

2.3 Model

In this section, an electrical model (E-model) for studying the frequency-dependent electrical characteristics and a compact electro-optical model (CEO-model) for analytically calculating the MZM's electro-optical frequency response is proposed. Design parameters of a modulator fabricated in the semi-insulating substrate are used as a reference for the validation of the models. No fitting or calibration has been applied to E-model or CEO-model.

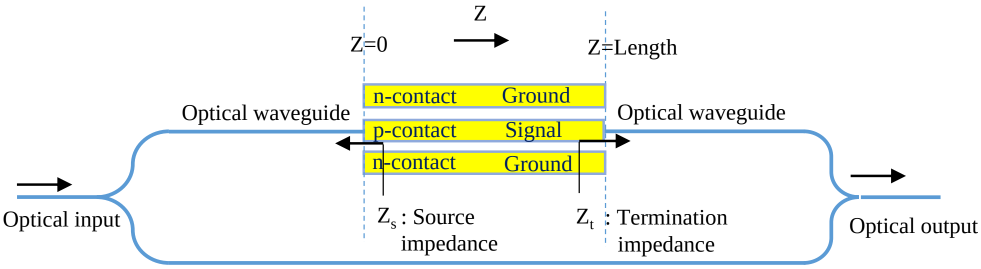


Figure 2.1: Schematic of the CPW-MZM for the single-drive applications, which includes the phase-modulator building-block (PM-BB)

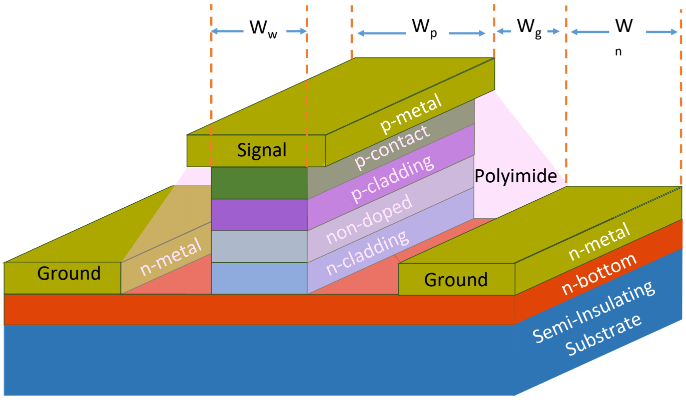


Figure 2.2: Cross-section of the HCPW-PM.

Figure 2.1 is the schematic of the high-speed CPW-MZM for the single-drive application.

In a single-drive CPW-MZMs, a high-speed CPW phase-modulator (CPW-PM) modulates the light enters to one of the optical arms of the MZM. The CPW-PM connects from one side to an electrical source and from the other side to a termination. In figure 2.1, the CPW-PM building block (BB) is on the top arm of the CPW-MZM and is extended from z=0 to Z=Length in the z-direction. CPW-PM-BB includes a central (signal) of the CPW traveling wave electrode placed on the optical waveguide. The two ground lines are on the sides of the signal electrode. Thus, Z_s and Z_t are the source impedance of the electrical driver and the termination impedance seen by the CPW phase-modulator BB, respectively.

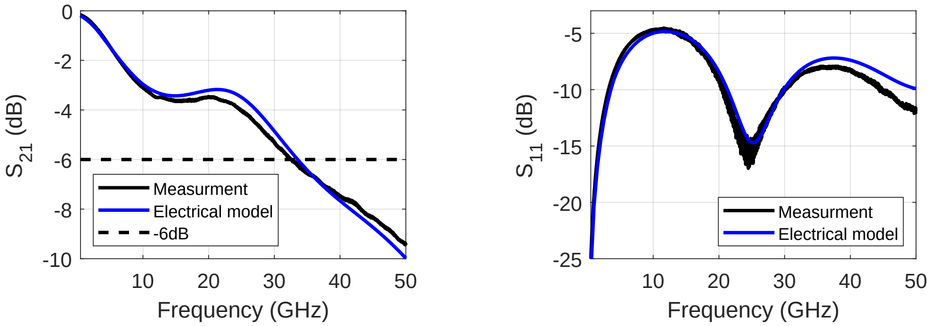
Design Parameters		
Variable	Symbol	Value
Thickness of the p-cladding layer	d_{pclad}	1.5 μm
Thickness of the p-contact layer	d_{pc}	0.28 μm
Thickness of the n-cladding layer	d_{nclad}	0.31 μm
Thickness of the intrinsic layer	d_{i}	0.5 μm
Thickness of the signal metal layer	d_{pm}	2 μm
Thickness of the n-bottom layer	d_{nb}	1.5 μm
Conductivity of the p-cladding layer	σ_{pclad}	1000 S/m
Conductivity of the p-contact layer	σ_{pc}	23000 S/m
Conductivity of the n-contact layer	σ_{nclad}	16400 S/m
Conductivity of the non-doped layer	σ_{i}	100 S/m
Conductivity of the n-bottom layer	σ_{nb}	27600 S/m
Conductivity of metal layer	σ_{m}	4.11×10^7 S/m
Permittivity of the p-cladding layer	$\varepsilon_{\mathrm{pclad}}$	89.385 pF/m
Permittivity of the vacuum	ε_0	8.85 pF/m
Permittivity of the polyimide	$\varepsilon_{\mathrm{poly}}$	20.01 pF/m
Permittivity of the p-contact layer	$\varepsilon_{\mathrm{cp}}$	124.01 pF/m
Permittivity of the n-cladding layer	$\varepsilon_{\mathrm{nclad}}$	100.12 pF/m
Permittivity of the SI substrate	$\varepsilon_{\mathrm{sub}}$	88.76 pF/m
Permittivity of the non-doped layer	ε_{i}	100.14 pF/m
Permittivity of the n-bottom layer	$\varepsilon_{\mathrm{nb}}$	88.79 pF/m
Permeability of vacuum	μ_0	1.25 μH/m
Light wavelength in vacuum	λ_0	1550 nm
Light speed in vacuum	c_0	299,792 km/s
Waveguide width	W_{w}	1.5 μm
Signal line width	W_{p}	9 μm
Ground line width	W_{n}	20 μm
Ground to signal gap	W_{g}	11 μm
Length of the phase shifter	L_{ps}	1 mm

Table 2.1: Design parameters of the reference HCPW-MZM

2.3.1 Electrical model

Figure 2.2 shows the cross-section of the CPW-PM-BB in the InP platform. To show all the critical layers and electrodes, this picture is not in scale. Since this platform's ground and signal electrodes are in two different planes above and below the p-i-n junction, we use the term hybrid co-planar waveguide (HCPW) instead of co-planar waveguide. The optical waveguide of the HCPW-MZM includes an intrinsic core layer with n-cladding and p-cladding layers above and below it, respectively. A highly doped InGaAs ternary-layer (p-contact) is between the p-metal and p-cladding to minimize the loss. The signal p-metal line is located on the optical waveguide, and the two n-metal ground lines are next to the waveguide on the n-bottom layer. A reference HCPW-MZM, fabricated in the semi-insulating (SI) substrate by SMART Photonics, has the cross-sectional parameters shown in table 2.1 which are taken from [37]. These parameters were used for validating both the electrical and the compact electro-optical models. In these models, the following assumptions are made for the cross-section:

- The polyimide region is sloped, while, in this work for simplicity, a flat polyimide region is assumed. As this region is a dielectric material, this assumption is not expected to affect the bandwidth, but because signal metal will get closer to the n-bottom part in the sloped polyimide, microwave index and characteristic impedance will be slightly different.
- The core region is represented by a non-intentionally-doped bulk layer.



(a) Electrical S_{21}

(b) Electrical S_{11}

Figure 2.3: Comparing the simulation and measurement electrical a) S_{21} and b) S_{11} of the phase modulator in the reference HCPW-MZM when source and termination impedances are $50\,\Omega$.

We use a 3D EM simulation environment (CST microwave studio [36]) for the high-speed RF electrical simulation. The CST frequency-domain solver divides the 3D structure into tetrahedral meshes and calculates the electrical s-parameters of the entire structure. It also calculates the frequency-dependent characteristic impedance, microwave index, and propagation constant.

In the frequency-domain solver of CST, there is a trade-off between the number of meshes and the simulation accuracy. In the RF simulation of the PM BB of this work, to achieve converged results, the minimum mesh size of $0.2\,\mu$m is set for the core, n-cladding, and InGaAs layers of the optical waveguide. The minimum mesh size of the p-cladding and n-bottom layers are 0.3 and $0.5\,\mu$m, respectively. The other mesh dimensions are calculated automatically by the software. The automatic mesh calculation is by setting the smallest mesh dimension, ten times smaller than the smallest waveguide length, which corresponds to the highest frequency of the simulation.

To validate the electrical model, we simulate the electrical scattering parameters of the phase-modulator BB with the cross-sectional parameters listed in table 2.1. In figure 2.3 the 3D-simulated electrical scattering parameters of the reference design are compared for model and measurement data of the reference device in a $50\,\Omega$ measurement system. The measured and simulated electrical S_{21} transfer function in figure 2.3a and S_{11} reflection function in figure 2.3b are presented with good agreement.

2.3.2 Compact electro-optical model

A compact electro-optical (CEO) model to calculate the small-signal electro-optical frequency response of the MZM is introduced in this part. The calculation and measurement data of the reference HCPW-MZM design with cross-sectional and mask parameters are listed in table 2.1, which is compared to validate the model.

In the Mach–Zehnder interferometer, the output optical intensity follows a cosine dependence on the optical phase change. At quadrature bias and under small-signal approximation, the intensity variation is linearly proportional to the optical phase change. In this work, we assume that the optical refractive index's change and the associated change in the optical phase depend linearly on the modulating voltage applied to the PM. Therefore for calculation of the frequency response of the reference single-drive HCPW-MZM, we calculate the frequency-response of the phase-modulator.

When an alternating current (AC) voltage source is applied to the HCPW traveling wave electrode, the phase modulator's voltage (V_m) can be expressed as a superposition of forward and backward (reflected) waves at time t and distance z along with the HCPW-PM [33]:

$$V_m(z,t) = V^+ e^{j\omega\left(t-\frac{z}{v_{\mathrm{RF}}}\right)-\alpha_{\mathrm{RF}}z} + V^- e^{j\omega\left(t+\frac{z}{v_{\mathrm{RF}}}\right)+\alpha_{\mathrm{RF}}z} \tag{2.1}$$

Where complex voltages V^+ and V^- will be determined from the source and termination conditions. The normalized modulation index $M(\omega)$ which calculates the small signal electro-optical frequency response can then be expressed in the form of the modulating phase change as:

$$M(\omega) = \left|\frac{\triangle\phi(\omega)}{\triangle\phi(0)}\right| = \frac{R_t+R_s}{R_t}\left|\frac{Z_{in}}{Z_{in}+Z_S}\right|\left|\frac{(Z_t+Z_m)F(u_+)+(Z_t-Z_m)F(u_-)}{(Z_t+Z_m)e^{\gamma_m L_{\mathrm{ps}}}-(Z_t-Z_m)e^{-\gamma_m L_{\mathrm{ps}}}}\right| \tag{2.2}$$

$\triangle\phi(\omega)$ is cumulative phase modulation over the interaction length L_{ps}, and

$$\begin{aligned} F(u) &= \frac{1-exp(u)}{u}, \quad u_{\pm} = \pm\alpha_m L_{\mathrm{ps}} + j\frac{\omega}{c_0}(\pm n_\mu - n_{\mathrm{opt}})L_{\mathrm{ps}} \\ \gamma_m &= \alpha_m + j\frac{\omega n_\mu}{c_0} \\ Z_{in} &= Z_0\frac{Z_t + Z_m tanh(\gamma_m L_{\mathrm{ps}})}{Z_m + Z_{\mathrm{t}} tanh(\gamma_m L_{\mathrm{ps}})} \end{aligned} \tag{2.3}$$

n_{opt}=3.7 is the optical index of the reference design which is the effective group index of the fundamental optical mode. c_0 is the speed of light in the vacuum and n_μ is microwave index (the phase refractive index) of the electrical signal. γ_m and Z_m are the frequency-dependent electrical complex propagation constant and the characteristic impedance of

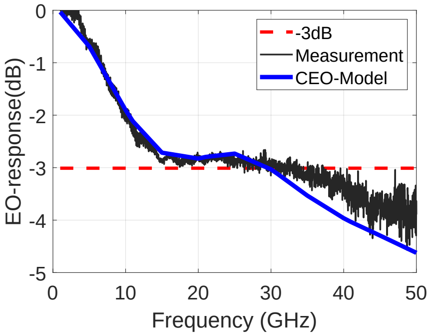


Figure 2.4: Comparison between measured and analytically calculated electro-optical frequency response of the reference HCPW-MZM. Data shown for a 50 Ω source and termination.

the HCPW-MZM, respectively.

$M(\omega)$ includes walk-off for the difference in the microwave and optical propagation constants $\beta_e = (n_\mu \omega)/c_0$ and $\beta_0 = (n_0 \omega)/c_0$. $M(\omega)$ also includes the effect of single back-reflections from the source impedance Z_s and the termination impedance, Z_t. R_t and R_s are the real part of termination and source impedances. The modulation index can make reference to the signal optical output power (optical definition) or to the electrical power originated by detecting the signal output power through a photodetector, proportional to the square of the optical power (electrical definition). In this thesis we consider the "optical" definition and for calculating the electro-optical response, we calculate is $(10\log_{10}|M(\omega)|)$ [33].

To analytically calculate the electro-optical frequency response of the reference HCPW-MZM, using the cross-sectional data in table 2.1, CST software calculated frequency dependent γ_m and Z_m needed in equation 2.3. Since these values are per meter, it is not needed to simulated the whole length of the MZM. This makes much shorter calculation time. Here we simulated 10 μm instead of total length of 1 mm. In figure 2.4, we compare the measured electro-optical-frequency response with the calculated electro-optical response ($M(\omega)$) of the reference HCPW-MZM when both source and termination impedances are 50 Ω. Figure 2.4 shows the agreement for measurement and calculation and a -3 dB EO-bandwidth at 30 GHz. Higher EO-frequency of the measurement result compared to the simulation response is because the measured high frequency response is close to the noise level.

In this section, by using the CST software, an electrical model for calculating the electrical frequency-dependent characteristics of the MZM is introduced. Then, by combining the modulator's propagation constant and characteristic impedances from the EM simulation tool (CST) with analytical equations, a compact electro-optical model for calculating the small signal electro-optical frequency response of the MZM is proposed. These simple and accurate models just include the cross-sectional parameters, have validated its output with experimental data and have shown they can effectively predict device performance without applying any fitting or calibration.

2.4 Characteristic impedance

This section investigates the effect of the source and termination matching on electrical bandwidth. It also describes the relationship between the power consumption of the MZMs to their characteristic impedance. Furthermore, it describes mechanisms that increase the characteristic impedance of the HCPW modulators. The simulated magnitude of the frequency-dependent characteristic impedance of the reference modulator is shown in figure 2.5. This characteristic impedance is between 23 and 27 Ω in the simulated frequency range, indicating a significant mismatch between modulator, source, and termination of the standard 50 Ω system.

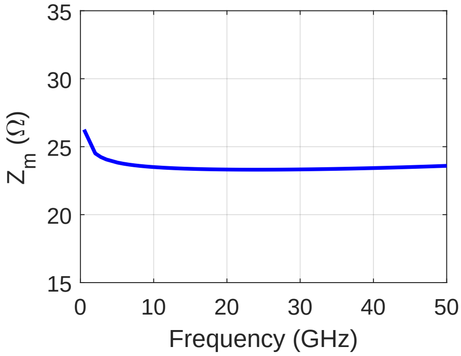


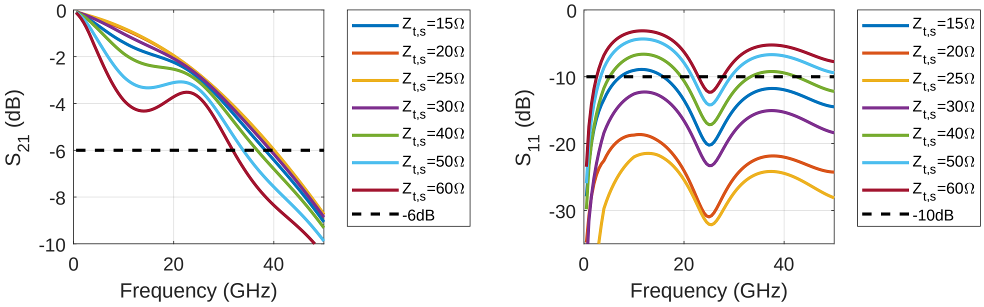
Figure 2.5: Characteristic impedance of the reference HCPW-MZM

2.4.1 Impedance matching

An increased characteristic impedance for the transmission line is expected to reduce resistive losses. However, increasing the impedance without careful matching to source and termination leads to a rapid degradation in the electrical performance, as can be seen in the scattering matrices. Figure 2.6 shows a) the transmission (S_{21}) and b) the reflection (S_{11}) of the electrical signal traveling the reference design connected to a sweep of source and termination impedances $Z_{\mathrm{t,s}}$. This Figure shows that by changing $Z_{\mathrm{t,s}}$ respect to the characteristic impedance of the reference HCPW traveling wave electrode, which is between $23 - 27\Omega$; the -6 dB electrical bandwidth is reduced while reflection is increased. Therefore to minimize the reflection and increase the -6 dB electrical bandwidth, characteristic impedance needs to be matched to the source and termination impedances. Typical design values for the power input reflection are below -10 dB [33]. Source and termination impedances between 20 and 30 Ω provide this requirement for the reference HCPW-MZM.

2.4.2 Power consumption

Termination resistors connected to the output of the traveling wave electrode leads to resistive losses. In the single-ended circuit of the HCPW-MZM (Figure 2.1), most of the



(a) Electrical transmission S_{11} (b) Electrical reflection S_{11}

Figure 2.6: a) The normalized transmission (S_{21}) and b) reflection (S_{11}) of the electrical signal traveling the reference HCPW connected to the sweep of source and termination impedances ($Z_{\mathrm{t,s}}$).

transmitted electrical power through the PM BB is consumed in the termination as follows:

$$P = V^2/R_t \tag{2.4}$$

In the above equation, P is the consumed power by the real part (R_t) of the termination Z_t at the voltage V. This equation shows that, for a particular voltage and by increasing the termination resistance, the resistive electrical power consumption of the MZMs can be reduced.

HCPW traveling wave electrodes have inductive and capacitive behaviors. The following equation shows the relationship between characteristic impedance Z , inductance L and capacitance C of the traveling wave electrodes [38]:

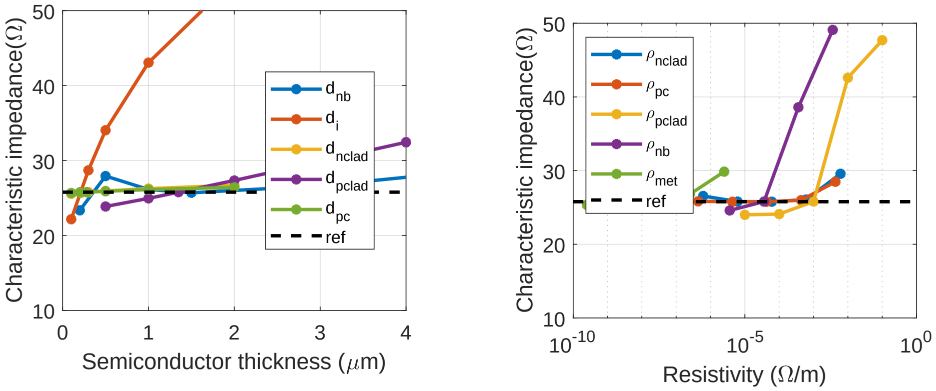
$$Z = \sqrt{L/C} \tag{2.5}$$

Equation 2.5 shows that by increasing the characteristic impedance and reducing the termination's resistive loss, inductance L and capacitance C of the traveling wave electrode have to be increased and decreased, respectively.

Figure 2.7 presents the characteristic impedances of the HCPW transmission line at the frequency of 100 GHz, calculated by the electrical model for a broad range of primary parameters, including dimensions and material properties. These are independently swept to identify the most important design variables. The values include the reference design. In these plots, while sweeping a parameter, the other parameters are kept constant and equal to the reference design in table 2.1. The dashed line shows the reference numbers, and the crossing of each curve with the dashed lines shows the reference value for that parameter.

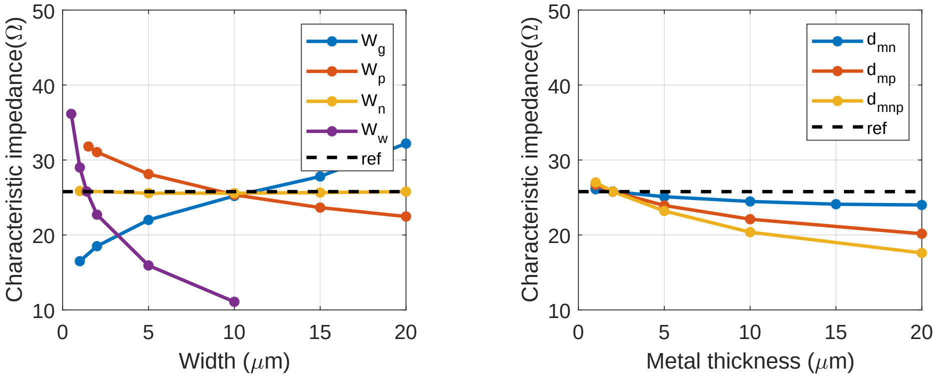
In figure 2.7a, thickness of the semiconductor layers is changed in a wide range. This plot shows that by increasing the thickness of the intrinsic layer (d_{i}), the characteristic impedance increases significantly. The reason is that by increasing the thickness of this layer, the parallel plate capacitor in this region decreases as follows:

$$C = \frac{\epsilon A}{d}, A = W_{\mathrm{w}} \times L_{\mathrm{ps}} \tag{2.6}$$



(a) characteristic impedance vs. semiconductor thicknesses

(b) characteristic impedance vs. resistivity



(c) characteristic impedance vs. widths

(d) characteristic impedance vs. metal thicknesses

Figure 2.7: Plots of characteristic impedance for different a) semiconductor thicknesses, b) resistivities c) widths and d) metal thicknesses. The subscripts nb, i, nclad pclad and pc are denote the n-bottom, intrinsic, n-cladding, p-cladding and p-contact, layers, respectively. The variables d_{mn} and d_{mp} are the n-contact and p-contact metal thicknesses. d_{mnp} means increasing the n and p-contact metals simultaneously.

Figure 2.7b, depicts the characteristic impedance vs. changes of the material resistivities. It shows that, increasing the resistivity of the p-cladding layer makes a significant change in the characteristic impedance. As this layer is above the intrinsic layer, by making it resistive, it acts like an insulator and makes the thickness of the dielectric region of parallel plate capacitance higher and as a result, the capacitance decreases and impedance increases. Another resistivity that makes the characteristic impedance higher is the resistivity of the n-bottom layer (ρ_{nb}). As this layer is below the intrinsic layer, making it resistive, it has the same influence as the p-cladding layer. Figure 2.7c shows that by decreasing the optical waveguide width (W_{w}) the characteristic impedance increases. Equation 2.6 explains how reducing this parameter reduces the capacitance of the traveling wave electrode and increases characteristic impedance. Increasing the gap between the ground and signal line (W_{g}) enhances the inductance of the traveling wave electrode and increases the characteristic impedance (equation 2.6). Reducing the width of the signal line (W_{p}) also increases the inductance and characteristic impedance. Metal thicknesses are addressed in figure 2.7d. Changing d_{mn} and d_{mp} mean changing the thickness of the n and p metals separately, while d_{mnp} means changing their thickness simultaneously. Changing these metal thicknesses slightly increases the parallel capacitance between metal lines. This change also decreases the inductance of the traveling wave electrode. Due to the ground and signal configuration of the HCPW transmission line, increasing the signal line thickness has about double the effect on inductance reduction while the two grounds make parallel inductance and make lower inductance reduction. From this explanation, we see that increasing both thicknesses has the highest impact in reducing the inductance and decreasing the impedance of the traveling wave electrode.

Mechanism	**Design change**	**Side effects**
Decreasing capacitance	Increasing the thickness of the intrinsic layer (d_{i} in figure 2.7a) from 0.21 to 0.8 μm.	It will reduce the electric field for the same input electrical power.
	Decreasing the width of the waveguide (W_{w} in figure 2.7c) from 1.5 to 0.5 μm.	This induces optical loss in the waveguide [39].
	Five times increasing the resistivity of the p-cladding layer (ρ_{pclad} in figure 2.7b).	It may increase the optical loss and reduce the electric field for the same input electrical power.
	10 times increasing resistivity of the n-bottom layer (ρ_{nb} in figure 2.7b).	It minimizes the field distribution across the waveguide. Therefore, electro-optical modulation reduces.
Increasing inductance	Increasing the gap between ground and signal (W_{g} in figure 2.7c) from 11 μm to 25 μm.	By increasing the electrical loss in the n-bottom layer, it reduces the electrical bandwidth.
	Decreasing the signal width (W_{p} in figure 2.7c) to smaller than 1 μm.	-

Table 2.2: Mechanisms for enhancing the characteristic impedance of the reference HCPW-MZM and required design changes to have a 40-50% increase in the characteristic impedance.

In this section, we showed how the characteristic impedance of a HCPW traveling wave electrode is related to the material properties of the layers below the metal lines, as well as the geometry of traveling wave electrodes. We also discussed how to increase the characteristic of the reference design. To summarize this section, in table 2.2 we explain mechanisms for enhancing the characteristic impedance of the reference HCPW-MZM and required design changes to have a 40-50% increase in the characteristic impedance.

Decreasing capacitance can be achieved by increasing the thickness of the intrinsic layer (d_{i}), decreasing the width of the waveguide (W_{w}), or increasing the resistivity of the p-cladding layer (ρ_{pclad}). Increasing the thickness of the intrinsic layer from 0.21 to 0.8 μm increases the characteristic impedance of the reference device by 50%. However, this change will reduce the electric field for the same electrical power input. Decreasing the width of the waveguide from 1.5 to 0.5 μm increases the impedance by about 40% but induces optical loss in the waveguide [39]. Increasing resistivity of the n-bottom layer by ten times results in 40% increase; however, it minimizes the electric field distribution across the optical waveguide, and electro-optical modulation reduces. Increasing inductance is the second mechanism for increasing the characteristic impedance of the traveling wave electrode. A larger gap between ground and signal electrodes (W_g) and, narrower signal width (W_p) increases the inductance of the reference HCPW-MZM. Changing the former from 11 to 25 μm increases the characteristic impedance of the reference device by 40%. However, by increasing the electrical loss in the n-bottom layer, it reduces the electrical bandwidth. Decreasing the signal width to smaller than 1 μm also increases the characteristic impedance of the reference device. This design change increases the modulator's performance without affecting the optical transmission. Also, Decreasing the signal width to smaller than 1 μm also does not need any changes on the cross-section of the PM BB. Therefore, we propose to increase the impedance of the HCPW-MZM, by decreasing the signal width.

2.5 Velocity matching

For high-speed modulation, the electrical and optical signals of the MZM have to be velocities matched. In this section, we show the impact of velocity mismatch on the electro-optical response of the reference modulator. Then we explain mechanisms to match the electrical and optical velocities.

To have a velocity match between light and electric fields, microwave index (n_μ) needs to be in the same order of value of the optical index. This is expected to be more important in high frequencies when the electrical wavelength is short and optical and electrical waves will not sufficiently overlap. The relation between wavelength (λ) to frequency (f) and microwave index is as follows:

$$\lambda = \frac{c_0}{f n_\mu} \tag{2.7}$$

c_0 is the speed of light in vacuum. This equation explains how increasing the microwave index (n_μ) and frequency (f) decreases the electrical wavelength (λ). At the frequency of 60 GHz, for a device with the microwave index of 5, the electrical wavelength is equal to the length of the reference device (1 mm). Higher frequencies and microwave indexes makes the electrical wavelength shorter than the reference length.

When we assume ideal conditions, f_{3dB} which is the 3 dB-electro-optical bandwidth of the MZM, in the presence of velocity mismatching, is calculated as shown below [18].

$$f_{3dB} = \frac{1.4c_0}{\pi |n_\mu - n_\mathrm{opt}| L_\mathrm{ps}} \tag{2.8}$$

n_μ is the microwave index, n_opt is optical index, c_0 is velocity of light in vacuum, and, L_ps is the length of the MZM's phase shifter. Examining equation 2.8, in figure 2.8, the 3 dB-electro-optical frequency response for microwave indexes that are larger (red curve) or smaller (blue curve) than the reference optical index (3.7) of a MZM with the phase modulator length of 1 mm are depicted. This shows that an ideal modulator with 1 mm length and optical index of 3.7, at frequencies higher than 100 GHz and when the microwave index is lower than 2.5 or higher than 5, has more than a 3 dB reduction in the

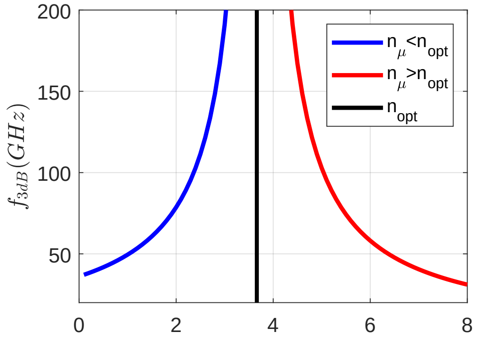


Figure 2.8: Velocity-mismatch limited 3 dB electro-optical bandwidth of the MZM vs. microwave index (n_μ). n_{opt} is the optical group refractive index.

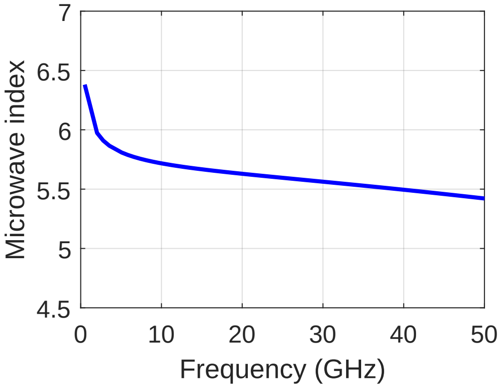
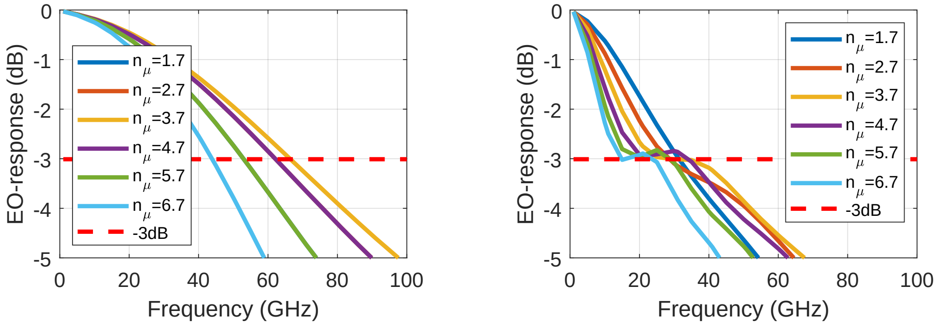


Figure 2.9: Frequency dependent microwave index of the reference HCPW-MZM simulated by the electrical model described in section 2.3.

electro-optical frequency response.

In figure 2.9, by using the electrical model, the microwave index of the reference HCPW transmission is calculated. The microwave index of this device in the 50 GHz frequency range, is between 5.4 and 6.4. This is higher and the optical index of the reference modulator (3.7) in the whole range of 50 GHz frequency.

By using the CEO-model described in section 2.3, we calculated the EO-frequency response of the reference HCPW-MZM, and in figure 2.10 we show the role of the velocity mismatch when the microwave index changes from 1.7 to 6.7. In figure 2.10a, the source and termination impedance perfectly matched the modulator's characteristic impedance. It showed that the 3 dB electro-optical bandwidth is maximum (66.5 GHz) when the modulator's microwave index (n_μ) was equal to the optical index (3.7) and was at the minimum (44 GHz) when the difference between the two is highest (n_μ= 1.7, 6.7). When n_μ = 1.7, the EO frequency response overlaps with n_μ= 5.7 because in both cases, the microwave index had



(a) Matched termination and source impedances (b) Termination and source impedances are 50 Ω

Figure 2.10: Role of the velocity mismatch on the EO-frequency response of the reference HCPW-MZM for a) source and termination impedances perfectly matched to the modulator's characteristic impedance and b) 50 Ω source and termination impedances. Optical index of the reference device is 3.7.

the same absolute difference from the optical index. For the same reason, the $n_\mu = 2.7$ plot overlaps with $n_\mu = 4.7$.

In figure 2.10b source and termination impedance are 50 Ω. Therefore, as shown in figure 2.3b, the reference modulator experiences a high electrical reflection. This figure shows that bandwidth is at the maximum (33 GHz) when microwave index is at the minimum ($n_\mu = 1.7$) 1.7), and bandwidth is at the minimum (15 GHz) when microwave index is at the maximum ($n_\mu = 6.7$). In 2.10b, when source and termination impedance is 50 Ω, the EO- bandwidth of the reference device is higher for microwave indexes smaller than the optical index. This is because the destructive interference of the reflected signal for microwave indexes smaller than the optical index is less than when the microwave index is larger than the optical index.

In both cases of matched and unmatched termination and source impedances, to have higher electro-optical bandwidth, the microwave index of the reference device must be reduced.

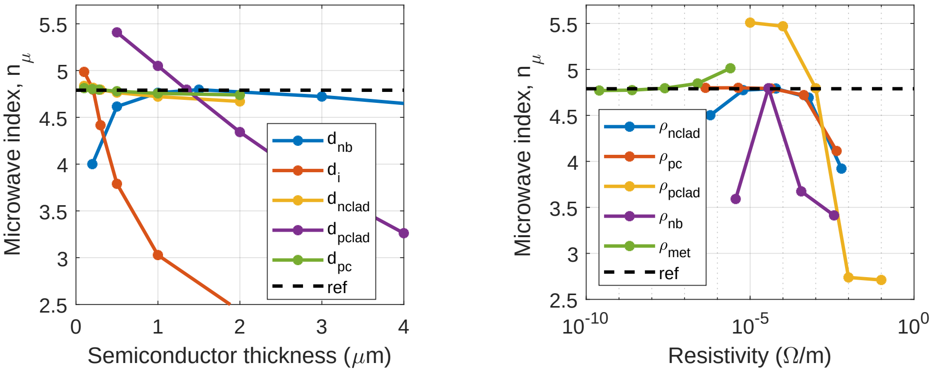
Bandwidth is limited by about 20% due to velocity mismatch in a 1mm impedance matched phase modulator. Increasing the phase modulator length increases the bandwidth limit due to the velocity mismatch. For instance, doubling the length of the impedance-matched phase-modulator results in a 30% bandwidth reduction compared to a velocity-matched phase-modulator with a 2mm length.

2.5.1 Reducing the microwave index

To have velocity matching between the light and electrical signals, the microwave index of the reference HCPW-MZM needs to be decreased. The following equation explains how lower inductance or capacitance reduces the microwave index [38].

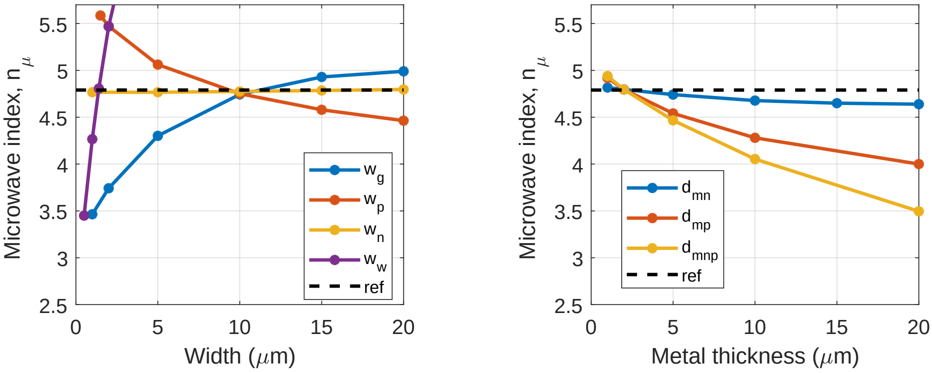
$$n_\mu = c_0\sqrt{L \times C} \tag{2.9}$$

c_0 is the speed of light in the vacuum, C is the characteristic capacitance, and L is the characteristic inductance of the traveling wave electrode. The inductance of the HCPW traveling wave electrode can be increased by narrowing the width of the signal electrode (W_p), decreasing the metal thicknesses ($d_\mathrm{mp}, d_\mathrm{mn}$), or increasing the gap between signal and ground electrodes (W_g). The primary capacitance of the traveling wave electrode is due to the parallel plate capacitance of the optical waveguide layers between the signal metal and n-bottom layer.



(a) Microwave index (n_μ) vs. semiconductor thicknesses

(b) Microwave index (n_μ) vs. resistivity



(c) Microwave index (n_μ) vs. widths

(d) Microwave index (n_μ) vs. metal thicknesses

Figure 2.11: Plots of microwave index (n_μ) for different a) semiconductor thicknesses, b) resistivities c) widths and d) metal thicknesses. The subscripts nb, i, nclad pclad and pc denote the n-bottom, intrinsic, n-cladding, p-cladding, and p-contact layers, respectively. The variables d_mn and d_mp are the n-contact and p-contact metal thicknesses. d_mnp means increasing the n and p-contact metals simultaneously.

Figure 2.11 presents the microwave index of the reference HCPW traveling wave electrode measured at 100 GHz frequency for a broad range of primary parameters, including dimensions and material properties. Again, the reference design values are used. In these plots, while sweeping a parameter, the other parameters are kept constant. The dashed line shows the reference numbers, and the cross of each curve with the dashed lines shows the calibration value for that parameter.

Thicknesses of the semiconductor layers impact the impedance, as shown in figure 2.11a. The reference design has a microwave index of 4.7, which is not influenced by the dimensions of n-cladding or pc thicknesses. This can be understood because these two layers behave like a good conductor and do not present excess capacitance to the line. As the p-cladding layer is not highly doped, it acts like a poor dielectric and weak conductor layer. Therefore, decreasing the thickness of this layer decreases the parallel capacitor of the line, and as a result, the microwave index decreases. The thickness of the intrinsic layer has the strongest impact, achieving 3.7 for a thickness of $0.5\mu m$. Methods to accomplish this will include a low electric field for the same input electrical power.

Resistivity is addressed in figure 2.11b. It shows that by increasing the resistivity of p-cladding and n-bottom layers, we can achieve a microwave index of 3.7. Making these layers more resistive decreases the parallel capacitance and, as a result, microwave index decreases. However, increasing the resistivity of the p-cladding increases the electrical loss. Also, since increasing the resistivity of the n-bottom layer causes electrical resistivity between the ground and signal electrodes, the electric field in the optical waveguide reduces significantly.

Widths are shown in figure 2.11c. By decreasing the gap between ground and signal (W_g), inductance decreases and microwave index of 3.7 is achievable when the gap is four microns. Figure 2.11c also shows that reducing the waveguide width (W_w) decreases the microwave index by reducing the capacitance (equation 2.6). A microwave index of 3.7 needs a W_w of 0.5 micron.

Metal thicknesses are addressed in figure 2.11d. Figure 2.11d shows that, by reducing inductances, thicker metal reduces the microwave index. A microwave index of 3.7 can be achieved when both the n- and p-metal thicknesses (d_mn , d_mp) are increased to $15\mu m$. In this section, we studied the importance of velocity matching in the MZMs. First, we looked

Mechanism	**Design change**	**Side effects**
Decreasing capacitance	Increasing the thickness of the intrinsic layer (d_i in figure 2.11a) from 0.21 to 0.5 μm.	It will reduce the electric field for the same input electrical power.
	Decreasing the width of the waveguide (W_w in figure 2.11c) from 1.5 to 0.65 μm	This induces optical loss in the waveguide.
	Increasing the resistivity of the p-cladding layer by two times (ρ_pclad in figure 2.11b).	It will increase the electrical loss and reduce the electric field for the same input electrical power.
	Increasing resistivity of the n-bottom layer by eight times (ρ_nb in figure 2.11b).	By minimizing field distribution across the waveguide, electro-optical modulation reduces.
Decreasing inductance	Reducing the gap between ground and signal (W_g in figure 2.11c) from 11 to 2 μm	It reduces the characteristic impedance (from 25.7 to 16.5 Ω).
	Increasing metal thicknesses (d_mnp in figure 2.11d) to 15 μm.	It reduces the characteristic impedance (from 25.7 to 19.5 Ω).

Table 2.3: Mechanisms for matching the electrical and optical velocities of the reference modulator.

at the effect of velocity mismatching on the electro-optical frequency response of the reference HCPW-MZM. Since the optical index is lower than the electrical index (microwave index), we found that the optical signal is faster than the electrical. Therefore to speed up the electrical signal, we studied mechanisms for reducing the microwave index. Table 2.3 summarizes the study on how to decrease the microwave index of the reference HCPW-MZM by changing the physical and dimensional parameters of the modulator. Table 2.3 shows two mechanisms for decreasing the microwave index: decreasing the capacitance and decreasing the inductance. It also describes the required design changes required for the electrical and optical velocity matching, as well as the potential side effects of each mechanism.

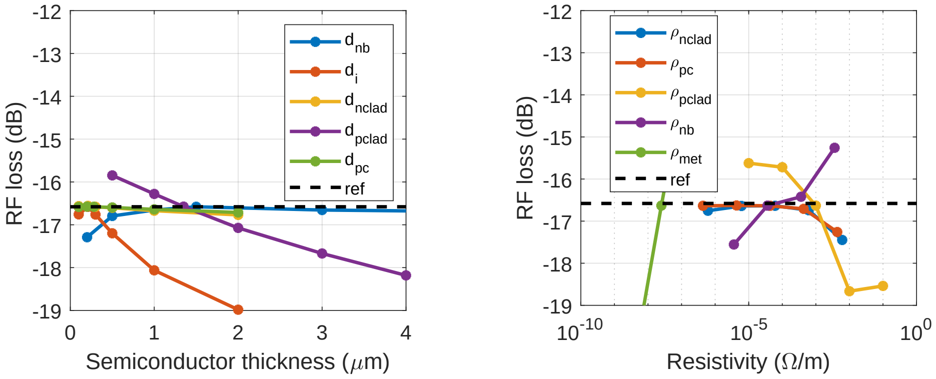
Decreasing capacitance of the traveling wave electrode reduces the microwave index and can match the optical and electrical velocities. This can be achieved by increasing the thickness of the intrinsic layer (d_i in figure 2.11a) from 0.21 to 0.5 μm; however, it reduces the electric field for the same electrical power input. Decreasing the width of the waveguide (W_w in figure 2.11c) from 1.5 to 0.65 μm also matches the velocities, but it costs extra optical loss in the waveguide [39]. Increasing resistivity of the n-bottom layer by eight times (ρ_nb in figure 2.11b) makes the velocity match by reducing the capacitance. However, by minimizing field distribution across the waveguide, electro-optical efficiency reduces. Increasing the resistivity of the p-cladding layer by two times (ρ_pclad in figure 2.11b) matches the optical and electrical velocities by capacitance reduction; however, it increases the electrical loss and reduces the electric field for the same input electrical power.

Decreasing inductance also reduces the microwave index, and as a result, matches the optical and electrical velocities of the reference device. It can be achieved by reducing the gap between ground and signal (W_g in figure 2.11c) from 11 to 2 μm or increasing metal thicknesses (d_mnp in figure 2.11d) to 15 μm. However, these costs reduce the characteristic impedance of the reference device from 25.7 to 16.5 and 19.5 Ω, respectively.

2.6 Radio frequency loss

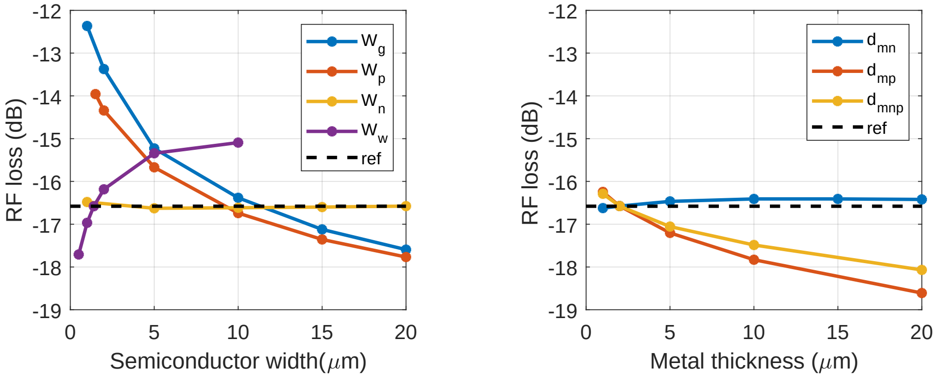
To have an insight into the origin of lost electrical power inside the modulator's building block when a radio frequency (RF) signal is applied, in this section, we look at the RF loss (radio frequency electrical power lost) caused by the cross-sectional and dimensional parameters of the HCPW-MZM. The electrical model described in section 2.3, also simulates the total RF loss of the reference HCPW traveling wave electrode at 100 GHz frequency. For calculating the total electrical loss of the phase modulator, the whole length of the modulator has to be simulated. However, to shorten the simulation time, instead of 1 mm HCPW phase modulator of the reference MZM, a 100-micron long HCPW phase modulator is simulated. Then, we sweep the cross-sectional parameters over a wide range to see the modulator's sensitivity to the RF losses. While sweeping a parameter, the other parameters are kept constant as in table 2.1. Moreover, we show the electrical 3 dB bandwidth of the modulator when these parameters are changed, and we list the key parameters that improve the electrical bandwidth by reducing the RF loss.

The HCPW-MZM cross-section shown in figure 2.2 consists of general types of two primary materials: metal and semiconductor. Since gold metal used in this cross-section is not a perfect conductor, it has metal losses, especially at the higher frequency when the skin effect plays a higher role [38]. The semiconductor region also has RF loss, usually higher



(a) RF loss in metal vs. semiconductor thickness

(b) RF loss in metal vs. resistivity



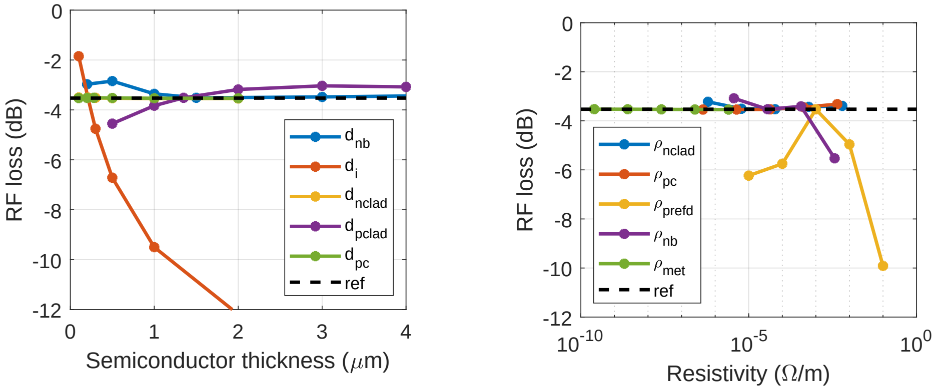
(c) RF loss in metal vs. widths

(d) RF loss in metal vs. metal thicknesses

Figure 2.12: Plots of the total electrical RF loss at 100 GHz in metal region of the of the $100\,\mu$m phase modulator for different a) semiconductor thicknesses, b) resistivities c) widths and d) metal thicknesses. The subscripts nb, i, nclad pclad and pc denote the n-bottom, intrinsic, n-cladding, p-cladding, and p-contact layers, respectively. The variables d_{mn} and d_{mp} are the n-contact and p-contact metal thicknesses. d_{mnp} means increasing the n and p-contact metals simultaneously.

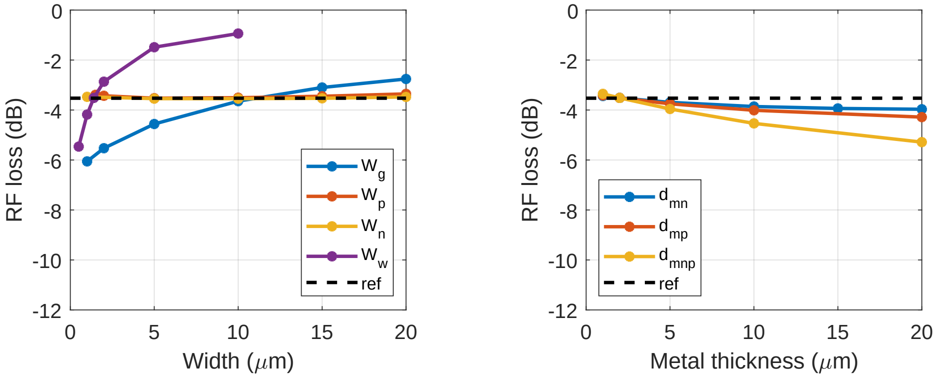
than the metal loss.

In figures 2.13 and 2.12, total RF loss over the $100\,\mu$m length of the HCPW traveling wave electrode in the semiconductor and metal regions for different a) semiconductor thicknesses, b) resistivities, c) widths, and d) metal thicknesses are depicted. The input power of this simulation is 0.5 W, and we normalized the RF loss to this input power; therefore, RF loss of 0 dB is when the total power is lost. By comparing Figures 2.13 and 2.12 plots for a sweep of parameters, it is seen that the total RF loss in the metal is from -19 to -12 dB, while in the semiconductor, it is much higher (-12 to -2 dB) for the same range of



(a) RF loss in semiconductors vs. semiconductor thicknesses

(b) RF loss in semiconductors vs. resistivity



(c) RF loss in semiconductors vs. widths

(d) RF loss in semiconductors vs. metal thicknesses

Figure 2.13: Plots of the total electrical RF loss at 100 GHz in semiconductor region of the of the 100 μm phase modulator for different a) semiconductor thicknesses, b) resistivities c) widths and d) metal thicknesses. The subscripts nb, i, nclad pclad and pc denote the n-bottom, intrinsic, n-cladding, p-cladding, and p-contact layers, respectively. The variables d_{mn} and d_{mp} are the n-contact and p-contact metal thicknesses. d_{mnp} means increasing the n and p-contact metals simultaneously.

parameter sweep. This means that most electrical power is lost in the semiconductor region.

Figures 2.12a and 2.13a show the RF loss vs. changes of the semiconductor thicknesses for semiconductor and metal regions, respectively. Increasing the thickness of the core layer reduces the RF loss in both regions. This is due to reducing the electric field intensity over the waveguide layer and minimizing the electric field's overlap with the lossy material. Decreasing the thickness of the p-cladding layer also decreases the loss in this lossy layer significantly. However, reducing this thickness increases the field's overlap to the signal electrode, and metal loss slightly increases. Thus, the role of reducing this thickness on the total RF loss in the semiconductor region is more significant. Changing the other thicknesses does not significantly impact the electrical RF loss distribution in semiconductors or metal regions.

Figure 2.12b and 2.13b depict the effect of the resistivities on the total RF loss of the semiconductor and metal regions. Decreasing the resistivity of the lossy p-cladding region makes this layer a better conductor and reduces the loss. Likewise, reducing the resistivity of the n-bottom layer decreases the RF loss in the lossy n-bottom semiconductor region. However, a high reduction of this resistivity results in the short circuit between the two ground electrodes, and the hybrid coplanar waveguide configuration changes to microstrip traveling wave electrode.

Figures 2.12c and 2.13c show that reducing the waveguide gap (W_g) and waveguide width (W_w) reduces the total RF loss of the semiconductor region in the waveguide and n-bottom layer, respectively. However, these changes increase the electric field's overlap with the signal electrode, and therefore the metal RF loss increases. Nevertheless, as mentioned before, metal loss compared to the loss in the semiconductor is smaller.

In figure 2.12d and 2.13d, the effect of the metal thicknesses on the total RF loss at 100 GHz for 100 μm length of the reference design for a wide sweep of parameters in both semiconductor and metal regions is depicted. This Figure shows that increasing the thickness of the ground metal (d_mn) and signal metal (d_mp), and increasing these both at the same time in (d_mnp), results in a lower loss in both regions. We also see that the effect of this reduction is more significant in the signal electrode. The reason is that the two ground electrodes are in the parallel electrical configuration, and they show a lower impact on the electrical loss. We also see that increasing the thickness of the two electrodes simultaneously to 20 μm results in a significant reduction in the overall electrical RF loss.

2.6.1 Electrical bandwidth of the HCPW line

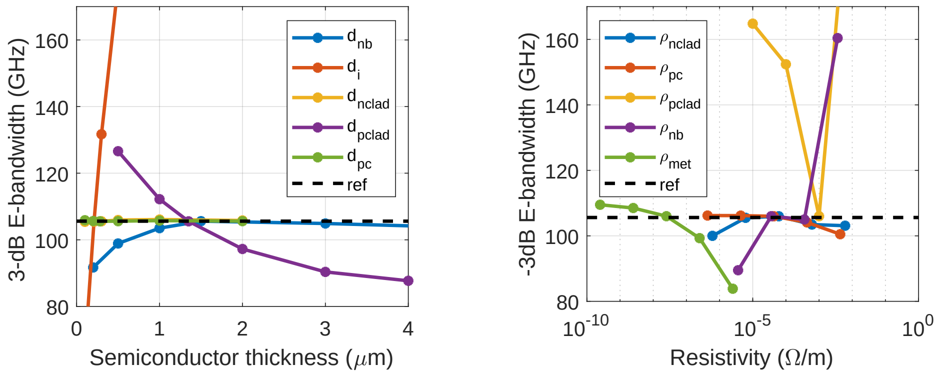
To see the impact of cross-sectional and dimensional parameters of the HCPW-MZM on the transmission line's electrical bandwidth, we use the electrical model in section 2.3, and we sweep the parameters of a 100-micron length of the reference HCPW traveling wave electrode and simulate the electrical-bandwidth. When a parameter is swept, the other parameters are kept constant and equal to the reference modulator in table 2.1.

Figure 2.14 shows the 3 dB electrical bandwidth of the HCPW traveling wave electrode for different a) semiconductor thicknesses, b) resistivities, c) widths, and d) metal thicknesses. The dashed line shows the reference numbers, and the cross of each curve with the dashed lines shows the calibration number for that parameter. In this simulation, to study only the influences of the parameters in the MZM's building block on the electrical bandwidth, source and termination impedances are matched to the modulator's impedance.

Figure 2.14a shows that thicker intrinsic layer results in higher electrical bandwidth. Since a thicker intrinsic layer has a lower electric field for the same electrical power, this causes less electrical RF loss when the electrical signal travels along the electrode.

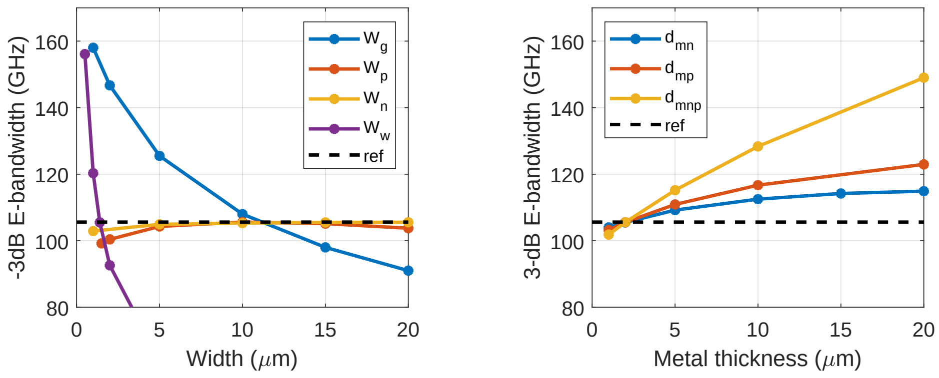
In figure 2.14b, it is apparent that, by increasing the resistivity of n-bottom and p-cladding layers, the thickness of the low loss insulating layer increases, and the electrical bandwidth increases. By decreasing the p-cladding layer's resistivity, this layer acts like a lossless metal and significantly increases the electrical bandwidth.

Figure 2.14c shows that, decreasing the waveguide width (W_w) and the gap between signal



(a) -3 dB E-bandwidth vs. semiconductor thicknesses

(b) -3 dB E-bandwidth vs. resistivities



(c) -3 dB E-bandwidth vs. widths

(d) -3 dB E-bandwidth vs. metal thicknesses

Figure 2.14: Plots of the electrical -3 dB bandwidth of the 100 μm phase modulator for different a) semiconductor thicknesses, b) resistivities c) widths and d) metal thicknesses. The subscripts nb, i, nclad pclad and pc denote the n-bottom, intrinsic, n-cladding, p-cladding, and p-contact layers, respectively. The variables d_{mn} and d_{mp} are the n-contact and p-contact metal thicknesses. d_{mnp} means increasing the n and p-contact metals simultaneously.

and ground (W_{g}) increases the E-bandwidth. The former reduces the electrical loss in the semiconductor material (mainly in the p-cladding layer), and the latter decreases the RF loss in the n-bottom layer. By increasing the metal thicknesses (figure 2.14d), and since the perimeter of the traveling wave ground and signal electrodes increases, the skin depth effect at high frequency is weaker; therefore, electrical bandwidth is higher.

In this section, we studied the origins of the RF loss in the modulator's building block. By sweeping the cross-sectional and dimensional parameters of the modulator, we showed how to reduce RF loss of the reference HCPW-MZM. We also simulated the E-bandwidth for the same parameter range. We showed that electrical bandwidth is significantly related to RF loss in the semiconductor region of the modulator. To summarize this study, we listed the design changes that can increase the E-bandwidth of the reference modulator:

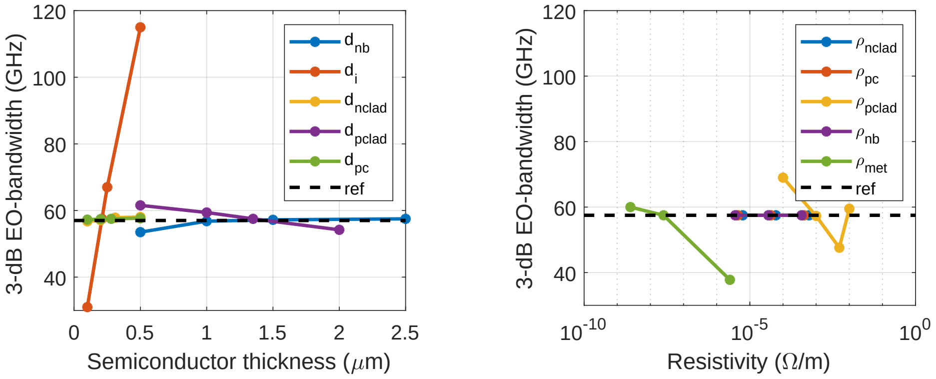
- Increasing the thickness of the intrinsic layer in figure 2.2 (by reducing the E-field overlap with the lossy regions).
- Decreasing the width of the waveguide (by reducing the width of the lossy semiconductor region and decreasing the RF loss).
- Making the p-cladding layer more conductive (changes the lossiest layer to the lossless conductive layer). Increasing the conductivity of the p-cladding layer in figure 2.2 requires increasing the doping level of this layer. However, this change might influence the doping near the optical layer.
- Making the n-bottom layer in figure 2.2 more resistive (by making this layer more insulating, reduces RF loss). This reduces the electrical connection between the electrical ground and signal, which results in a low electric field in the optical core layer.
- Decreasing the gap between ground and signal (reduces the loss in the n-bottom layer).

2.7 Electro-optical bandwidth

The high-speed EO-bandwidth of the MZM is defined by the frequency in which the modulator's optical power drops by half of the power at the low-frequency [33]. By small-signal assumption and using the equation 2.2 in this section, the effect of the cross-sectional physical and dimensional parameters of the HCPW-MZM on the EO bandwidth is studied.

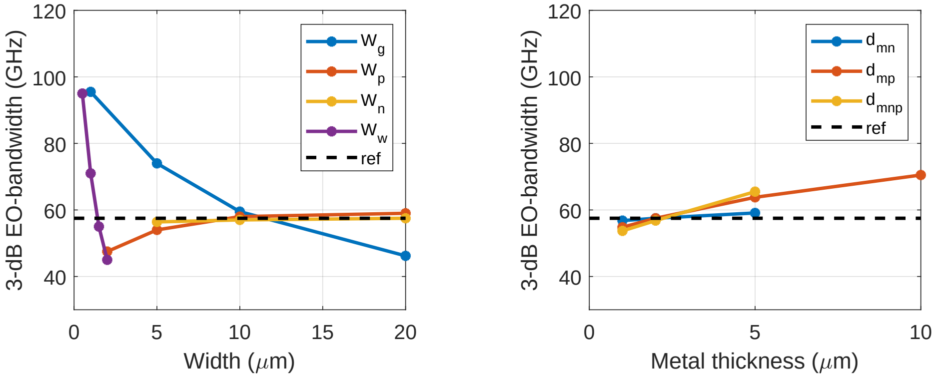
Figure 2.15 depicts the 3 dB EO-bandwidth of the HCPW-MZM for different a) semiconductor thicknesses, b) resistivities, c) widths and d) metal thicknesses. In figure 2.15a, the effect of the thickness of the semiconductor layers on the EO-bandwidth is studied. Increasing the thickness of the optical core layer (d_i) from 0.21 to 0.5-micron doubles the EO-bandwidth of the reference modulator. However, this decreases the electric field intensity of the optical core layer for the same input voltage. Decreasing the thickness of the p-cladding layer reduces the electrical loss in this layer and enhances the EO-bandwidth. Since as in figure 2.11a this change increases the microwave index, and as a result, the velocity mismatch increases, the overall effect of reducing the thickness of the p-cladding layer on the EO-bandwidth is not significant compared to the thickness of the optical core layer (d_i). Changing the thickness of the other layers does not have a significant effect on the EO bandwidth. In figure 2.15b, by decreasing the p-cladding layer's resistivity, this layer acts like a lossless metal and exponentially increases the electrical bandwidth. However, this will induce optical loss. Decreasing the resistivity of the metal layer also increases the bandwidth slightly. In figure 2.15b, by decreasing the p-cladding layer's resistivity, this layer acts like a lossless metal and exponentially increases the electrical bandwidth. However, this will induce optical loss. Decreasing the resistivity of the metal layer also increases the bandwidth slightly.

By increasing the metal thickness in figure 2.15d, and since the skin depth in high frequency plays a lesser role, electrical RF loss decreases, and EO-bandwidth increases. By



(a) 3 dB EO-bandwidth vs. Semiconductor thickness

(b) 3 dB EO-bandwidth vs. resistivity



(c) 3 dB EO-bandwidth vs. widths

(d) 3 dB EO-bandwidth vs. metal thicknesses

Figure 2.15: Plots of dependence of the -3 dB EO-bandwidth of the 100 μm phase modulator on critical design parameter for different a) semiconductor thicknesses, b) resistivities c) widths and d) metal thicknesses. The subscripts nb, i, nclad pclad and pc denote the n-bottom, intrinsic, n-cladding, p-cladding, and p-contact layers, respectively. The variables d_{mn} and d_{mp} are the n-contact and p-contact metal thicknesses. d_{mnp} means increasing the n and p-contact metals simultaneously.

comparing the electrical and electro-optical bandwidths in figure 2.14 and figure 2.15 respectively, we see that increasing the electrical bandwidth does not necessarily increase the EO-bandwidth of the MZM. To summarize the study on the EO-bandwidth of the HCPW-MZM, we list the parameters with a significant effect on the EO-bandwidth enhancement:

- Decreasing the waveguide width (W_{w}) reduces the RF loss in the semiconductor layers of the optical waveguide. (This change will increase optical loss.)
- Decreasing the gap between signal and ground (W_{g}), reduces the RF loss in the n-

bottom layer (This reduces the characteristic impedance, and therefore as described in section 2.4 the resistive power consumption increases.)

- Decreasing the resistivity of the p-cladding layer and reducing the electrical loss in this layer. (This change will induce optical loss.)
- Increasing the thickness of the optical core layer (d_i) by improving the velocity matching and reducing the intensity of the electric field reduces the RF loss (This decreases the electric field strength for the same input voltage.)

2.8 Design of a high-speed HCPW-MZM

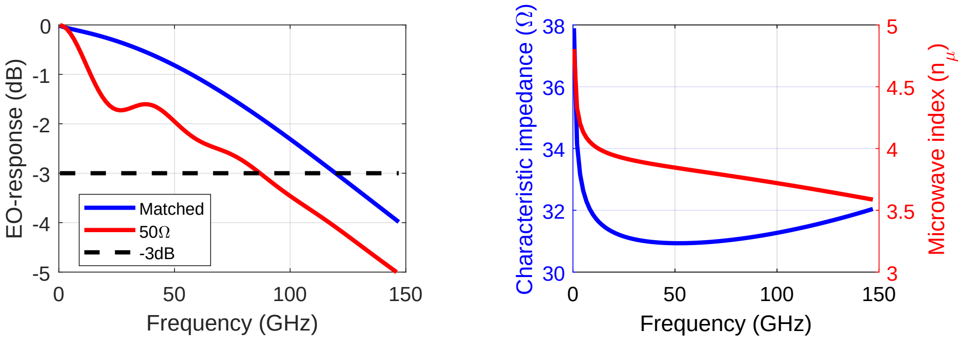
In the previous sections of this chapter, the effect of the material and dimensional parameters on HCPW-MZM frequency-dependent characteristics was discussed. When a parameter was studied, the values of other parameters were kept constant and equal to the reference value listed in table 2.1. To have an example of the effect of the combination of physical and mask parameters on the electrical and EO-responses, in Table 2.4 a parameter set is proposed.

Parameter	**Reference value**	**New value**	**Effect**
d_i	0.21 μm	0.31 μm	RF loss in both metal and semiconductor regions decreases. Also improves characteristic impedance and velocity matching.
W_g	11 μm	5 μm	RF loss in n-bottom layer decreases.
W_w	1.5 μm	1 μm	RF loss in waveguide decreases.
W_p	9 μm	5 μm	Increases the characteristic impedance and reduces RF loss in n-bottom layer.
ρ_pclad	$10^{-3}\Omega/m$	$0.8 \times 10^{-3}\Omega/m$	RF loss in p-cladding layer decreases

Table 2.4: Parameter set for a high-speed design.

The thickness of the optical core layer (d_i) is proposed to be increased from 0.21 to 0.31 μm. As depicted in figure 2.13a, this reduces the RF loss, and as shown in figure 2.15a it results in higher EO-bandwidth. This change also improves the characteristic impedance and velocity matching which are depicted in figure 2.7a and figure 2.11a, respectively. Reducing the gap between the signal and ground electrodes, W_g from 11 μm to 5 μm reduces the n-bottom layer's RF loss (figure 2.13b). This results in higher EO-bandwidth (2.15c). Since in figure 2.13c, the thinner waveguide width (W_w) has lower electrical loss, we reduced W_w from 1.5 to 1 μm. This change also improves the characteristic impedance and velocity matching, which are depicted in figure 2.7c and Figure 2.11c, respectively. To reduce the RF loss in the p-cladding layer (figure 2.13b), we decreased the resistivity of this layer $10^{-3}\Omega/m$ to $0.8 \times 10^{-3}\Omega/m$.

Figure 2.16 depicts a) EO-response in the 50Ω and b) microwave index and characteristic impedance of the proposed high-speed HCPW-MZM design. In figure 2.16a, in the 50Ω termination and source condition, the 3 dB EO-bandwidth is 87 GHz, which is about triple the bandwidth of the reference design (30 GHz). When termination and source are matched to the characteristic impedance, the 3 dB EO-bandwidth of the proposed design increases to 120 GHz, about two times the impedance matched reference design. Figure 2.16b shows the frequency-dependent microwave index (n_μ) and the characteristic impedance of the



(a) EO-frequency-response

(b) Microwave index and characteristic impedance

Figure 2.16: a) EO-frequency-response in the 50Ω and matched termination and source conditions and b) microwave index and characteristic impedance of the proposed high-speed HCPW-MZM design.

proposed high-speed HCPW-MZM. This design's microwave index is between 3.6 and 4.8, which is lower than the microwave index of the reference design (4.7–6.5) depicted in figure 2.11. In figure 2.16b we see that the microwave index of the proposed device for frequencies over 50 GHz is in the range of 3.6 to 3.7. Since the high-frequency microwave index of the proposed high-speed HCPW-MZM design is very close to the optical index of 3.7, this design has high-velocity matching between the optical and electrical signals.

Figure 2.16b also shows a higher impedance for the proposed design. This design's impedance is 31–38 Ω, while the characteristic impedance of the reference design is 23-26 Ω.

In the proposed high-speed HCPW-MZM design, changing a combination of parameters increased the EO-bandwidth of the modulator to about triple the reference design. In addition, it has higher electro-optical velocity matching. Because of higher characteristic impedance, this device can consume lower resistive electrical power. This is just one example of the effect of the combination of parameters. Due to the time limits, a rigourous multi-parameter optimization is not studied in this work. The model presented in this work can be used to calculate the optimized HCPW MZM design and for that model calibration for 100 GHz is recommended. Additionally, this work assume optical losses as not adversely affected for widths down to 1 μm.

2.9 Summary

The trade-off between geometrical parameters on the electro-optical bandwidth and power consumption of HCPW-MZMs was studied in this chapter. An electrical model was proposed to simulate the critical parameters' effects on the frequency-dependent electrical characteristics of the modulator. A compact electro-optical model was introduced to analytically calculate the effect of the cross-sectional and mask parameters on the EO-responses of the modulator.

As power consumption in termination of the traveling wave electrode decreases with increasing characteristic impedance, we introduced parameter changes for increasing the characteristic impedance. Increasing the thickness of the intrinsic layer from 0.21 to 0.8 μm increases the characteristic impedance of the reference device by 50%. However, this change will reduce the electric field of the optical core layer for the same electrical power input. Decreasing the width of the waveguide from 1.5 to 0.5 μm increases the impedance by about 40% but induces optical loss in the waveguide [39]. Increasing resistivity of the n-bottom layer by ten times results in 40% increase of the characteristic impedance; however, it minimizes the electric field distribution across the optical waveguide, and electro-optical modulation reduces. A larger gap between ground and signal electrodes (W_g) and, narrower signal width (W_p) increases the characteristic impedance of the reference HCPW-MZM, by increasing the inductance. Changing the former from 11 to 25 μm increases the characteristic impedance of the reference device by 40%. However, by increasing the electrical loss in the n-bottom layer, it reduces the electrical bandwidth. Decreasing the signal width to smaller than 1 μm also increases the characteristic impedance of the reference device. This design change increases the modulator's performance without affecting the optical transmission. Also, Decreasing the signal width to smaller than 1 μm also does not need any changes on the cross-section of the PM BB. Therefore, we propose to increase the impedance of the HCPW-MZM, by decreasing the signal width.

The microwave index should be reduced to match the effective optical index from the other side to obtain velocity matching between electric and optical fields. We showed how to achieve the velocity matching by changing the cross-sectional parameters of the HCPW phase modulator. Increasing the thickness of the intrinsic layer (d_i in figure 2.11a) from 0.21 to 0.5 μm matches the velocities by decreasing capacitance of the traveling wave electrode; however, it reduces the electric field for the same electrical power input. Decreasing the width of the waveguide (W_w in figure 2.11c) from 1.5 to 0.65 μm also matches the velocities, but it costs extra optical loss in the waveguide [39]. Increasing resistivity of the n-bottom layer by eight times (ρ_{nb} in figure 2.11b) makes the velocity match by reducing the capacitance. However, by minimizing field distribution across the waveguide, electro-optical efficiency reduces. Increasing the resistivity of the p-cladding layer by two times (ρ_{pclad} in figure 2.11b) matches the optical and electrical velocities by capacitance reduction; however, it increases the electrical loss and reduces the electric field for the same input electrical power. Reducing the gap between ground and signal (W_g in figure 2.11c) from 11 to 2 μm or increasing metal thicknesses (d_{mnp} in figure 2.11d) to 15 μm makes the velocity match by decreasing the inductance of the traveling wave electrode. However, these costs reduce the characteristic impedance of the reference device from 25.7 to 16.5 and 19.5 Ω, respectively.

By using the electrical model introduced in this work, we simulated the total electrical RF loss in the semiconductor and metal regions. We showed that RF loss in the semiconductor region at 100 GHz frequency is over 10 dB higher than the metal region. Then we presented how to increase the E-bandwidth by reducing the RF loss, achieved by minimizing the size or resistivity of the lossy semiconductor layers or by changing the electrical field distribution to keep it away from such layers. Increasing the thickness of the intrinsic layer in figure 2.2 (by reducing the E-field overlap with the lossy regions). Decreasing the width of the waveguide increases the electrical bandwidth by reducing the width of lossy semiconductor region and decreasing the RF loss. Making the p-cladding layer more conductive increases the electrical bandwidth by changing the most lossy layer if the phase modulator cross-section to the lossless conductive layer. However, because increasing the conductivity of the p-cladding layer requires increasing the doping level, it might influence the doping near the optical layer. Making the n-bottom layer in figure 2.2 more resistive can increase the electrical bandwidth by making this layer more insulating and reducing the RF loss. However this change reduces the electrical connection between the electrical ground and signal which results in low electric field in the optical core layer. Decreasing the gap between ground and signal increases the electrical bandwidth by reducing the loss in the n-bottom layer. However, this change decreases the characteristic impedance of the modulator.

After understanding the effects of cross-sectional parameters on the electrical characteristics, we studied the electro-optical bandwidth of the HCPW-MZM. By comparing the electrical and electro-optical bandwidths, we showed that increasing the electrical bandwidth does not necessarily increase the EO-bandwidth of the MZM. During this study, each time one parameter was studied, the other parameters' default values were kept constant. A parameter set as an example was proposed to show the effect of combining the effective parameters on the modulator's performance. This modulator has an 87 GHz EO-bandwidth in the $50\,\Omega$ and 120 GHz in the matched source and termination condition, makes it a promising candidate for high-speed HCPW-MZMs. However, these modulators can not be fabricated in the current generic technology due to the epitaxy changes.

Moreover, we discussed that the highest electrical loss is from the p-cladding layer of the phase modulator's p-i-n junction. NTT reduced this loss by changing to the n-i-p-n junction [14]. Applying this change also can improve the speed of the HCPW-MZMs significantly.

In this work, we proposed design modifications of the phase modulator BB for optimizing electrical and electro-optical characteristics of the HCPW-MZM. However, some of these design changes require epitaxial changes and can not be realized in the available generic technology, preventing direct validation. Moreover, both the electrical and the electro-optical models proposed in this work calculate frequency-dependent characteristics of the phase modulator BB. However, these models do not include the effect of electrical connections on the electrical and electro-optical frequency-dependent characteristics of the MZM. Also, since the CEO model assumes a small signal assumption, this model can not calculate the large-signal electro-optical response of the MZM.

Chapter 3

Electronic to photonic co-design

3.1 Abstract

In this chapter, we propose a co-design methodology for the optimization of high-speed characteristics in Mach-Zehnder modulator based transmitters. The approach uses a parametric, non-iterative, traveling-wave model for the phase modulators which is readily incorporated with the optical circuit and driver networks. The model uses only measurable design parameters such as layer thicknesses, materials properties, and mask feature dimensions. The model is embedded within an electrical device simulation environment and compared with both a full-3D, electromagnetic simulation, and experimental data. A foundry-produced indium phosphide InP Mach Zehnder Modulator (MZM) with a hybrid coplanar-waveguide electrode design is used as a reference design for verifying model accuracy. The electronic-photonic co-design is validated with both small and large-signal modeling of the electrically connected device. The model is used to study impedance matching and passive electrical pre-compensation to predict a doubling the large-signal modulation bandwidth of the previously reported MZM to 80Gbit/s for on-off-keyed modulation with 7.5 dB extinction ratio. Further bandwidth increases may be anticipated with driver and phase modulator optimizations. In this chapter, we answer the following question:

- **Can a non-iterative, design-variable-driven InP MZM model be built and efficiently embedded in an electrical circuit simulator?**
- **Can we quantify the benefits of electronic photonic codesign?**

3.2 Introduction

Wider bandwidth, more energy-efficient modulators are required to meet ever-increasing performance requirements in fiber-optic communications. Mach-Zehnder modulators have now been demonstrated to offer modulation signal rates of 100 GBaud [40]. High-order modulation formats have enabled increased spectral efficiency [41–43] , and increased data rates [44], but the electrical frequency response of the complete transmitter circuit is critical to determining the ultimate data capacity [33]. The bandwidth of the transmitter is increasingly limited by the connection between the driver and the modulator [45–47].

The design tools required for optimizing the connection between electrical and photonic ICs are currently fragmented, and the most accurate methods are computationally intensive. This limits opportunities for design space exploration, co-designed electrical and photonic circuits, and large-signal modeling.

Electrical equivalent circuit models can describe the optical phase modulator at the heart of a photonic transmitter, and parameters may be derived from the measured electrical scattering parameters [17, 48]. However these approaches use fitting of electrical and electro-optical transfer functions and provide a means for local optimizations. When the model uses experimental electrical scattering parameters rather than design variables, this limits opportunities for more wide-ranging, structural design optimizations. This can be a particular concern with complex, out-of-plane electrode architectures and advanced waveguide geometries such as co-planar waveguides and capacitively-loaded electrodes.

Numerical techniques such as the semi-analytical method of lines [35], and the iterative finite-element and finite difference methods [34, 49–51] have been extensively studied. These methods come with high computational overhead and are not conveniently integrated with the electronic design flow to enable multi-variable analysis. Realistic physical design parameters can lead to 3D structures with intractably large simulation volumes and the computation time is too high for modeling the large-signal operation. Spatially-resolved, equivalent-circuit models using structural design inputs have been proposed and can reduce the computational overhead. Such approaches have been proposed for silicon photonic modulators with lateral p-i-n junctions [52] and traveling wave InP photodetectors [53], using a separate tool for inductance calculations in the latter case [54]. A computationally efficient, compact, analytical approach to embed InP modulators in the electronic design flow has not yet been proposed.

In this work, we propose a non-iterative, spatially-resolved, equivalent-circuit model for traveling-wave electrode (TWE) phase modulators, resolving the propagation along the electrode using only the design parameters of the MZM. We implement the model within the Advanced Design System (ADS) environment to facilitate co-design with electrical interconnects and loads. We present the modulator design, described in terms of material and geometrical properties. A compact electrical model is then constructed around the unit-length, cross-sectional representation for the phase modulator. We calculate the small-signal, electro-optic frequency response, and the large-signal modulation response with time-domain modeling, and verify the model with experimental comparison. The co-design methodology is finally validated with a bandwidth-equalizing, passive interconnection network.

3.3 Modulator compact model

The Mach-Zehnder transmitter model comprises an idealized driver, the connection between driver and input electrodes to the modulator, a traveling wave electrode design on top of a p-i-n phase modulator, and the connections to the resistive termination load to reduce back-reflected power. The elements of the model are shown in figure 3.1 as a block diagram description. This builds out from a spatially resolved phase modulation model, incorporates velocity mismatch, intensity modulation within the optical interferometer and finally electrical reflections between the interfaces for the driver, interconnection, modulator and termination. Both small and large signal transmitter analysis are studied.

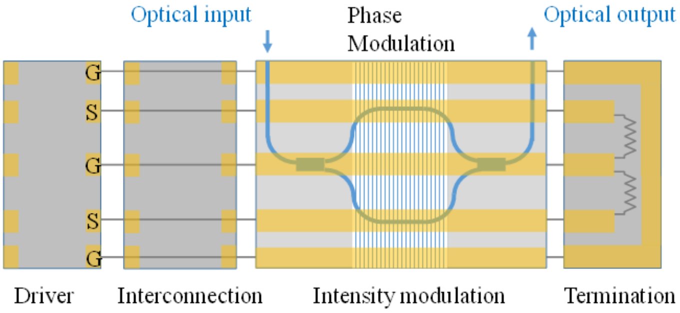


Figure 3.1: Block diagram for the modeling of an HCPW-MZM

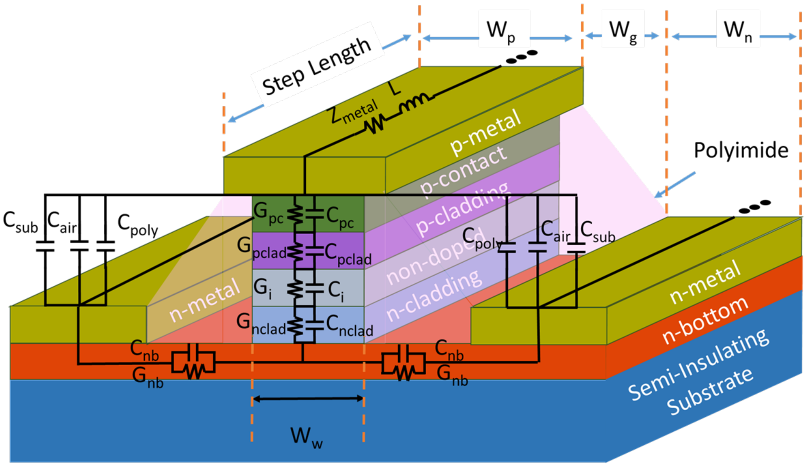


Figure 3.2: The cross-section of the studied phase modulator element showing dimensions, materials and electrical equivalent circuit.

3.3.1 Electro-optic circuit modulation

The hybrid co-planar waveguide design studied in this work is analysed for the case of single phase-modulator modulation: the high-speed voltage source is applied to the CPW line on one branch of the MZM. As the electrode design and epitaxial design are invariant along the length of the phase modulator, this is represented by a unit-length cross-section as shown in figure 3.2. The non-intentionally-doped, optical waveguide layer sandwiched between the p-cladding and n-cladding layers forms the p-i-n junction optical phase-shifter. The p-contact metal is placed on a thin InGaAs p-contact layer. The n-contact metal is placed on the n-doped layer labeled n-bottom which is below the n-cladding layer. Figure 3.2 shows the constituent layers, materials, and dimensions.

The physical parameters used in this work for calculating the phase modulator are listed in in Table 2.1. The material parameters are taken from [37]. Dimensional data is specific to the reference design presented in this paper which is used to verify the model. No curve fitting is performed.

In figure 3.3, a schematic of the non-iterative simulation method of the high-speed HCPW

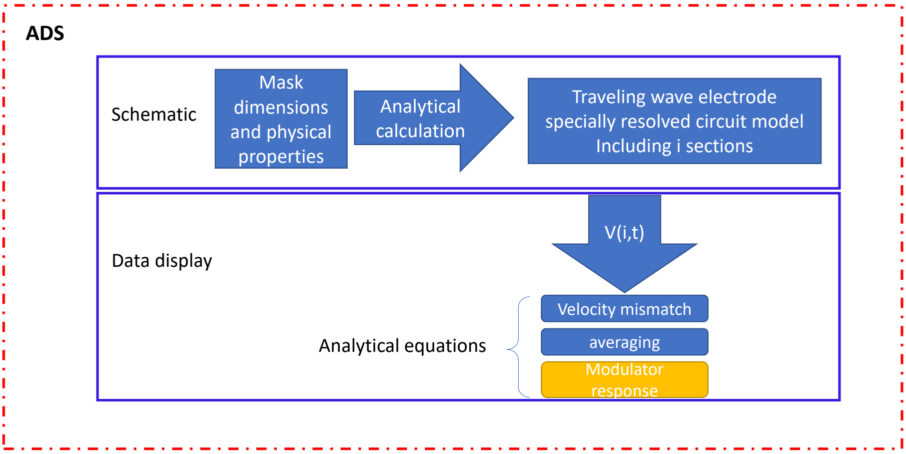


Figure 3.3: Schematic of the non-iterative simulation method of the high-speed HCPW modulator in ADS software

modulator in ADS software is depicted. In the schematic window of the ADS software, mask and dimensional parameters of the HCPW-MZM listed in Table 2.1 are the input parameters. Closed-form analytic solutions use the cross-sectional and mask parameters to calculate the longitudinally-resolved phase response for the HCPW traveling wave modulator (in figure 3.2). C_i is the capacitance of the n-doped layer of the optical waveguide core. V_1, V_i and V_N are voltages across the C_{i1}, C_{ii} and C_{iN} respectively. As shown in figure 3.4 the circuit model of the HCPW traveling wave electrode is divided to N sections. When input voltage (Vin(V), AC+DC) is applied to the section 1 of the the circuit model of the HCPW traveling wave electrode, the N_{th} section is terminated by a load such as a $50\,\Omega$ load, and ADS simulations is run in the data display window of ADS, V(t, i) that is voltage across the section i (figure 3.3), will be generated. In the display window of ADS, to include velocity matching and averaging needed for calculating the modulator's small and large signal responses, another set of analytical equations will be applied to V(t,i).
The methods to calculate the equivalent circuit elements shown in figures 3.2, 3.4 and using values listed in Table 2.1 are described in the following text. These relationships have been proposed in earlier work, but they have not been presented together in the context of a phase modulator model, and an overview is accordingly provided here. The equivalent circuit is defined in terms of:

- Metal-air impedance Z_{metal}
- Line inductance L
- p-i-n stack impedance C_{pc}, G_{pc},C_{pclad}, G_{pclad}, C_{nclad}, C_i, G_{pc}
- polyimide capacitance C_{poly}
- air capacitance C_{air}
- substrate capacitance C_{sub}

Metal-air impedance Z_{metal} represents the transverse impedance of the signal electrode and is defined as the ratio of metal-air transverse wave impedance η_m and width

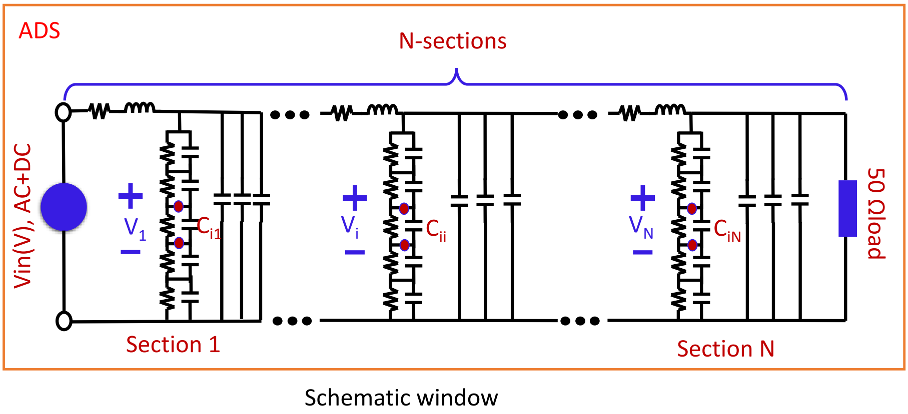


Figure 3.4: Specially resolved circuit model of the HCPW phase modulator divided into N sections. V_1, V_i and V_N are voltages across the C_{i1}, C_{ii} and C_{iN} capacitances respectively.

of the electrode W_p and is scaled by the skin depth δ_m and the conductivity of the gold σ_m [55, 56]

$$Z_{metal} = \frac{\eta_m}{W_p}, \quad \eta_m = \sqrt{\frac{j\omega\mu_0}{\sigma_m}} coth[(1+j)\frac{d_{pm}}{\delta_m}]; \quad \delta_m = \sqrt{\frac{2}{\omega\mu_0\sigma_m}} \tag{3.1}$$

The electrical field is applied between the signal and ground electrodes and includes the full layer stack. The p-i-n stack impedance represents the individual layer impedance contributions orthogonal to the electrode and. The parallel capacitance and conductance values of each layer x are calculated [53].

$$\begin{aligned} C_x &= \frac{W_w \varepsilon_x}{d_x}; \qquad G_x = \frac{W_w \sigma_x}{d_x} \\ C_{nb} &= \frac{d_{nb}\varepsilon_{nb}}{W_w + W_p + 2W_g}; \qquad G_{nb} = \frac{d_{nb}\sigma_{nb}}{W_w + W_p + 2W_g} \end{aligned} \tag{3.2}$$

Polyimide capacitance C_{poly} results from the p-electrode lying on top of a polyimide passivation layer. The equivalent thickness is taken from the total layer thickness of the ridge waveguide.

$$C_{poly} = \frac{(W_p - W_w)\varepsilon_{poly}}{d_{pc} + d_{pclad} + d_i + d_{nclad} + d_{nb}} \tag{3.3}$$

Air capacitance C_{air} is the capacitance of the line where there is an absence of the dielectric materials and is calculated by using the conformal mapping technique. The validity of conformal mapping in transmission-line analysis assumes that the propagation mode in the transmission lines is a quasi-TEM mode and this approximation is usually considered valid up to a frequency of 100 GHz [57]. The capacitance is calculated from the complete elliptical integral of the first kind K_{0r}.

$$
\begin{aligned}
&C_{air} = 4\varepsilon_0 \frac{K_{0r}(K_0')}{K_{0r}(K_0)} \\
&K_0 = \frac{W_a}{W_b}\sqrt{\frac{W_b^2 - W_a^2}{W_c^2 - W_a^2}}, \quad K_0' = \sqrt{1 - K_0^2} \\
&W_a = 0.5W_p; \quad W_b = 0.5W_p + W_g; \quad W_c = 0.5W_p + W_g + W_n
\end{aligned}
\tag{3.4}
$$

Substrate capacitance is calculated using the same technique as for C_{air}. Here K_{sr} is the complete elliptical integral of the first kind and $K' = K(k')$. The ratio of the complete elliptical integral of the first kind is calculated following [58], to give:

$$
\begin{aligned}
&C_{sub} = 2(\varepsilon_{sub} - \varepsilon_0)\frac{K_{sr}(K_s')}{K_{sr}(K_s)}, \quad K_s' = \sqrt{1 - K_s^2} \\
&K_s = \frac{sinh(\frac{\pi W_b}{2d_{sub}})}{sinh(\frac{\pi W_c}{2d_{sub}})}\sqrt{\frac{sinh^2(\frac{\pi W_b}{2d_{sub}} - sinh^2(\frac{\pi W_a}{2d_{sub}})}{sinh^2(\frac{\pi W_c}{2d_{sub}} - sinh^2(\frac{\pi W_a}{2d_{sub}})}} \\
&\frac{K}{K'} = \frac{1}{\pi}ln(2\frac{1+\sqrt{k}}{1-\sqrt{k}}) \qquad 0.7 \le k \le 1 \\
&\frac{K}{K'} = [\frac{1}{\pi}ln(2\frac{1+\sqrt{k}}{1-\sqrt{k}})]^{-1} \qquad 0 \le k \le 0.7
\end{aligned}
\tag{3.5}
$$

Inductance L for the hybrid CPW electrodes is calculated from the equivalent parallel rectangular planar lines with the width of the n-electrode W_n and the half-width of the p-electrode $0.5W_p$ .Two parallel sets of rectangular planar lines are assumed and the mutual inductance between the ground and signal electrodes is neglected [59].

$$
\begin{aligned}
&L = 0.5\left(\frac{120\pi^2}{c_0 ln\left[2\left(1+\sqrt{k_l'}\right)/\left(1-\sqrt{k_l'}\right)\right]}\right), \quad 0 \le k_l \le \frac{1}{\sqrt{2}} \\
&L = 0.5\frac{120}{c_0}ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right), \qquad \frac{1}{\sqrt{2}} \le k_l \le 1 \\
&k_l = \frac{W_g}{W_g + 0.5W_p + W_n}, \quad k_l' = \sqrt{1 - k_l^2}
\end{aligned}
\tag{3.6}
$$

The microwave phase velocity v_{RF} and optical group velocity v_{opt} are estimated from the refractive indices to be $60 \times 10^6 \frac{m}{s}$ and $81 \times 10^6 \frac{m}{s}$ at 50GHz respectively. This corresponds to a 4.6 ps difference in transmission time for a 1mm long electrode. This walk-off in signals [33] leads to reduced modulation efficiency and is therefore modeled by spatially resolving phase modulation along the length. The RF signal is fed at the left side of the phase modulator in figure 3.1 and propagates to the right, inducing an electric field that travels with the optical field. This two-media nature of the top and bottom of the traveling-wave electrode leads to a dominant hybrid – quasi-TEM mode [60] and the phase velocity and characteristic impedance in the phase modulator become mildly frequency-dependent [61]. The RF signal voltage undergoes attenuation α_{RF} and is partially reflected at mismatches in impedance in the RF circuit. This may be described in terms of the forward and back-reflected complex voltages V^+ and V^- [33]. This includes multiple reflections from the source and load circuits. The electric field across the core layer with thickness di is subsequently calculated:

$$\begin{aligned} V_{TWE}(z,t) &= V^+ e^{j\omega\left(t-\frac{z}{v_{RF}}\right)-\alpha_{RF}z} + V^- e^{j\omega\left(t+\frac{z}{v_{RF}}\right)+\alpha_{RF}z} \\ E(z,t) &= \frac{V_{TWE}}{d_i} \end{aligned} \tag{3.7}$$

The refractive index of the optical wave in the absence of the external electric field is $n = n_r - jn_i$. While traveling along the line, the optical wave experiences an additional following local variation of the refractive index $\triangle n = \triangle n_r - j\triangle n_i$

$$\triangle n_r(z,t) = \frac{1}{2}n_g^3 r_{pockels}E + \frac{1}{2}n_g^3 r_{kerr}E^2 \tag{3.8}$$

Where n_g is the background optical group index. $\triangle n_r$ is the local perturbation to the real part of the refractive index. The group index is assumed to depend on the field-dependent Pockels effect, the nonlinear Kerr effect. The refractive index perturbation includes the linear (Pockels effect) and the quadratic (Kerr effect) dependency on the applied electric field and the role of the plasma effect and the band filling are neglected in this work [62]. $E(z,t)$ is the RF electric field at the core of the optical waveguide, which has a band-edge corresponding to $1.25\mu m$. The corresponding coefficients are assumed to be $r_{pockels} = 1.2\times10^{-12}m/V$ for the Pockels effect [63, 64] , $r_{kerr} = 0.8\times10^{-20}m^2/V^2$ [63] for the Kerr effect. No optical nonlinearities are included in the model. The electric field of the optical plane wave propagating in the z-direction in the absence of the applied electric field is defined in terms of optical refractive index $n = n_r - jn_i$ [33].

$$E_0(t) = E_0 e^{-jkz} = E_0 e^{-j\frac{2\pi}{\lambda_0}(n)z} \tag{3.9}$$

By defining $\alpha_{opt} = \frac{2\pi}{\lambda_0}n_i$, as the field attenuation and $\beta_{opt} = \frac{2\pi}{\lambda_0}n_r$ as the propagation constant:

$$\begin{aligned} -j\frac{2\pi}{\lambda_0}(n)z &= -jk_0(n)z = -z(j\beta_{opt}+\alpha_{opt}) \\ E_0(t) &= E_0 e^{-z\alpha_{opt}}\left(e^{-jz\beta_{opt}}\right) \end{aligned} \tag{3.10}$$

The traveling optical wave enters at the left side of the phase modulator as shown in figure 3.1 at z=0 at time t_0 and leaves the phase modulator of length L at time t_2. Since the optical intensity of the modulated light in the MZM will be measured when it has passed the entire L, the optical time coordinate of the calculation is be changed to t_2.

$$\begin{aligned} t(z) &= t_0 + \frac{z}{v_{opt}} = t_2 - \frac{L}{vopt} + \frac{z}{v_{opy}} \\ t_2 &= t - \frac{L}{v_{opy}} + \frac{z}{v_{opt}} \end{aligned} \tag{3.11}$$

Where v_{opt} is optical velocity. The net amplitude and phase change in the optical field after propagation along the phase modulator can be recovered by integrating the spatially resolved refractive index change $\triangle n(z)$ as seen by the optical field where:

$$\begin{aligned} E_{opt}(t) &= E_0(t)exp\left[-jk_0 \int_0^L \triangle n\left(z,t-\frac{L}{v_{opy}}+\frac{z}{v_{opt}}\right)dz\right] \\ &= E_0(t)exp\left[-jk_0 \int_0^L \triangle n_r\left(z,t-\frac{L}{v_{opy}}+\frac{z}{v_{opt}}\right)dz\right] \\ &- E_0(t)exp\left[\int_0^L \triangle \alpha_{opt}\left(z,t-\frac{L}{v_{opy}}+\frac{z}{v_{opt}}\right)dz\right] \end{aligned} \tag{3.12}$$

The cumulative phase modulation and cumulative amplitude modulation are described in the first and second integrals respectively. Propagation is discretized into N sections with index i so that $z = \frac{iL}{N}$ to describe the walk-off between electrical and optical signals. Loss perturbation, $\triangle\alpha_{opt}$ is neglected, the net phase perturbation is described at the time t in terms of integration along the phase modulator which may be discretized:

$$\begin{aligned} \triangle\phi &= k_0 \int_0^L \triangle n_r\left(z,t-\frac{L}{v_{opy}}+\frac{z}{v_{opt}}\right)dz \\ \triangle\phi &= k_0 \sum_{i=1}^{N} \triangle n_r\left(iL,t-\frac{L}{v_{opy}}+\frac{iL}{v_{opt}N}\right) \times \frac{L}{N} \\ &= k_0 \frac{L}{N} \sum_{i=1}^{N} \triangle n_r\left(iL,t-\frac{L}{v_{opy}}+\frac{iL}{v_{opt}N}\right) \end{aligned} \tag{3.13}$$

3.3.2 Mach-Zehnder interferometer

Intensity modulation is achieved using the Mach-Zehnder configuration in figure 3.1. The optical field propagation is modeled in the z-direction accounting for both optical loss and the optical phase shift. The input optical field splits at a symmetric splitter to allow the simulation of optical field transmission from the two input ports T_{10} and T_{20} of the two phase modulators arms, with phase shift $j\phi_s$ from the symmetric splitter, leading to an output optical field from the single-ended phase-shifted modulator:

$$\begin{aligned} [T_{10} \quad T_{20}] &= \left[\frac{1}{\sqrt{2}}E_0 e^{j\phi_s} \quad \frac{1}{\sqrt{2}}E_0 e^{j\phi_s}\right] \\ [T_{1L} \quad T_{2L}] &= \frac{1}{\sqrt{2}}e^{-\alpha_{opt}L}E_0\left[e^{j\phi_s}e^{-j\beta_{opt}L}e^{-j\triangle\phi} \quad e^{j\phi_s}e^{-j\beta_{opt}L}\right] \end{aligned} \tag{3.14}$$

E_0 is the optical input field. T_{10} and T_{20} are optical fields of the two splitted light transmitting the phase modulators arms. In the single-ended drive scheme used in this work, the refractive index of the first arm locally changes by $\triangle\phi$ as the RF signal travels through the electrode in the same direction of the light. The combiner at the output allows interference and the optical wave after the combiner is defined in terms of the sum of the fields, and the optical power at the output port P_{out} is the product of the field with its complex conjugate:

$$\begin{aligned}
a_{out} &= [T_{1L} \quad T_{2L}] \times \begin{bmatrix} \frac{1}{\sqrt{2}} e^{j\phi_s} \\ \frac{1}{\sqrt{2}} e^{j\phi_s} \end{bmatrix} \\
&= \frac{E_0}{\sqrt{2}} e^{-\alpha_{opt}L} e^{j2\phi_s} e^{-j\beta_{opt}L} (e^{-j\triangle\phi} + 1) \\
P_{out} &= \frac{E_0^2}{2} e^{-2\alpha_{opt}L} |e^{-j\triangle\phi} + 1|^2 = \frac{E_0^2}{2} \chi \left(1 + cos(\triangle\phi)\right) = \frac{|a_{in}|^2}{2} \chi \left(1 + cos(\triangle\phi)\right) \\
\chi &= e^{-2\alpha_{opt}L}
\end{aligned} \tag{3.15}$$

The modulation index is calculated from the ratio of the input and output optical powers. The phase response in equation 3.13 is calculated for a range of modulation frequencies to give the small-signal response.

$$\begin{aligned}
m(\omega) &= \frac{|P_{out}|}{|P_{in}|} = \frac{\left|\frac{|a_{in}|^2}{2} \chi \left(1 + cos(\triangle\phi(\omega))\right)\right|}{|a_{in}|^2} \\
m(\omega) &= \frac{1}{2} \left|\chi \left(1 + cos(\triangle\phi(\omega))\right)\right|
\end{aligned} \tag{3.16}$$

The small-signal electro-optical frequency response of the modulator is therefore calculated by $10 \times log_{10} m(\omega)$.

3.4 Model verification

To predict the electro-optic frequency response and modulation efficiency, the spatially resolved model described above is implemented within an electrical simulation tool. Figure 3.4 shows the equivalent circuit described in preceding parts of this section as they are used in the electrical simulation environment ADS. The per unit length electrical components are described in figure 3.2. For the small-signal analysis, a frequency-swept electrical source is applied as an input. For large signal eye diagram calculations, time and frequency domain simulations are performed. A reference design using the generic foundry process from Smart Photonics is used to verify the model [65]. A hybrid co-planar waveguide HCPW-MZM with 1 mm electrode length, 1.5 μm optical waveguide width, 9 μm signal electrode width, 11 μm signal to metal gap and the vertical p-i-n junction phase shifter is used. A photograph of the experimentally assessed device is shown in figure 3.5. The optical fibers are shown at the left and right of the circuit. The electrical probes at the RF input and output are withdrawn for clarity. The phase modulators have a bulk active region and exhibit $V\pi L$ values of 7.4 Vmm. The calculated $V\pi L$ value is 7.15 Vmm. A convergence test has been performed to determine the minimum required discretization, prior to small signal and large signal simulation and comparison. This is described further in section 3.4.1. No parameter fitting is performed, as the purpose is to verify model accuracy with input design variables. The model predictions are compared with the 3D EM simulation CST Microwave Studio [36] and experimental measurements for the reference PIC design.

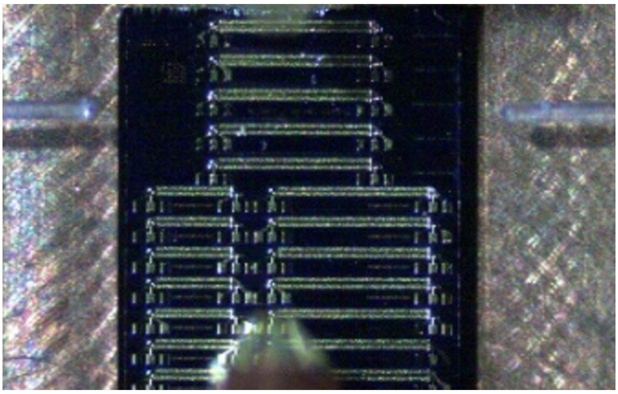


Figure 3.5: Photograph of the reference PIC

3.4.1 Convergence analysis for transmission line

The phase modulator circuit is discretized into N-sections where N varies from one – equivalent to a lumped element equivalent circuit model – to 30 sections. The phase modulator is driven from a 50 Ω source impedance and terminated with a 50 Ω load. Figure 3.6 shows the convergence of the calculated electrical transmission (S21) of the electrical transmission line of the phase modulator when the number of sections (N) is increased from 1 to 30. In figure 3.6 we also see that electrical S21 when N=20 (number of sections) overlaps with electrical S21 when N=30 therefore for the rest of the calculations of this work N=20 is used.

The calculated and measured electrical scattering from the input to the output port (S21) of the electrical transmission line is simulated and compared with experimental data in figure 3.6. The figure shows very good agreement between the measurement data and the circuit model transmission responses in the range of the measurement. It also shows that electrical S21 of the compact model agrees closely with CST Microwave Studio [36]. In contrast to the FEM solver, the compact model takes two seconds to compute the full frequency response. The full 3D calculation for the 1 mm long device takes two hours using the same computer.

3.4.2 Small signal electro-optic response

The electro-optical frequency response is calculated for a normalized input light intensity. In the experimental measurements, the polarization state is aligned and an on-chip power of –2.9 dBm is estimated before the first splitter. A swept RF signal is applied with power –15.0 dBm over the range of 10 MHz to 67 GHz. The RF electrical signal is applied to the input of the modulator electrode from the 50 Ω network analyzer system. The output connection is made via an RF ground-signal-ground probe and a coaxial cable to the network analyzer [1]. The electro-optic small-signal modulation response is shown in figure 3.7. The calculated electro-optical frequency response of the modulator overlaps with the measurement result. The initial drop and plateau observed in the frequency response are

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[1] Weiming Yao did the small and large-signal measurements and the picture of the modulator.

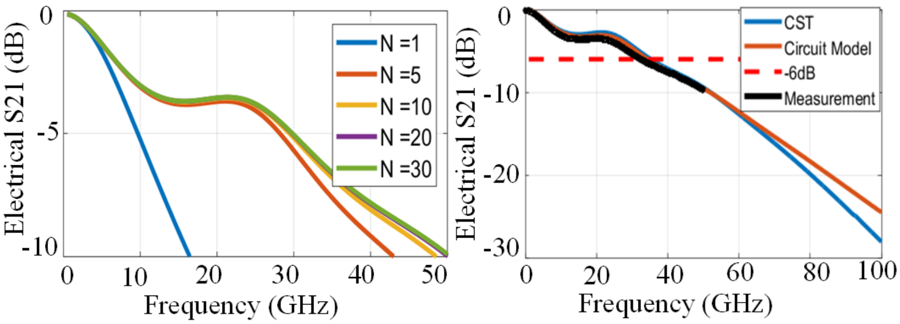


Figure 3.6: Frequency response of the traveling wave electrode: Left: Convergence for increasing discretization. Right: Comparison between the compact model, 3D FEM simulation and the measured reference PIC.

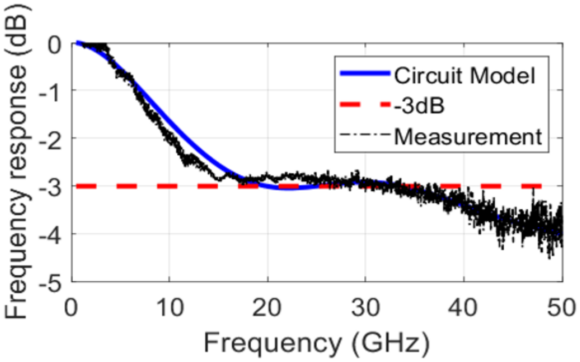


Figure 3.7: Measured and simulated electro-optic frequency response for a 50 Ω source and 50 Ω load.

attributed to electrical reflections at the input and output of the phase modulator electrodes. The impedance of the phase modulator transmission line is observed to vary from 20 to 25 Ω over the range 10 MHz to 67 GHz, while the electronic components are fixed at 50 Ω.

3.4.3 Large electro-optic response

The large-signal response is assessed with the output-eye-diagram for 20 Gbps and 30 Gbps on-off-keyed data. A pseudorandom bit sequence with $2^8 - 1$ pattern length is used in the modeling leading to time sequence durations of order 12.6ns at 20 Gbps. Experimentally measured eye diagrams are performed with an experimentally limited peak to peak modulator voltage of 5.5 V. Eye diagrams in figure 3.8 show good agreement between the measured data and the predictions using the compact model. Comparable rise and fall times are observed for the experimental and simulated eye diagrams for 20 Gbps and 30 Gbps. A broadening of the ones and zeros rails is evident at 30 Gbps, indicating increased bit pattern dependence. The eye-opening is quantified in terms of a quality factor derived from

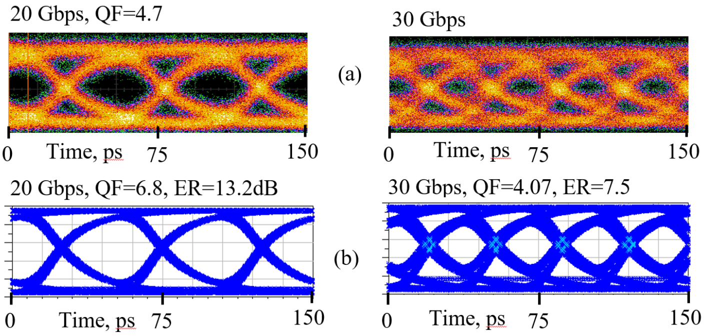


Figure 3.8: Measured (a) and simulated (b) optical-eye-diagrams of the reference design at 20 Gbps and 30 Gbps.

ADS software. The simulated Q-factor values degrade from 6.8 to 4.1. This eye-pattern degradation is attributed to RF reflections, motivating the co-design of the electrical and photonic elements in the circuit.

3.5 Electrical-optical co-design

Two co-design approaches are taken to remedy the bandwidth limitations observed in section 3.4. The first approach is impedance matching through electronic component replacement, and the second approach is a passive interconnection network for a 50 Ω electronic driver and load combination with the electrically unoptimized MZM.

3.5.1 Electrical impedance matching

The impedance of the electronic source and termination load is varied to study the relative dependence on matching the phase modulator impedance. The small-signal electro-optical response of the transmitter circuit is simulated for both 50 Ω and of 20 Ω source impedances. The former is equivalent to the experimental measurement conditions, and the latter corresponds to near-optimal impedance matching with the phase modulator. As it may be more practical to vary only the termination load, this is varied from 20 Ωto 55 Ω for both cases. The modulation responses are normalized to the 50 Ω source and 50 Ω termination load condition. The electro-optic frequency response is shown to flatten markedly in figure 3.9 when the termination resistance is matched to the real part of the transmission line impedance, even if no measures are taken to improve the source to transmission line matching. The 3 dB optical modulation bandwidth is observed to increase from 30 GHz to 57 GHz, representing a two-fold increase relative to the 50 Ω termination condition.
Figure 3.9 shows that matching the source impedance to the transmission line impedance (20 Ω) results in 0.8-1.2 dB increase in the frequency response.

3.5.2 Passive interconnection network

An alternative approach enabling the connection of available 50 Ω driver and 50 Ω termination load is investigated with the inclusion of a bandwidth equalizing passive inter-

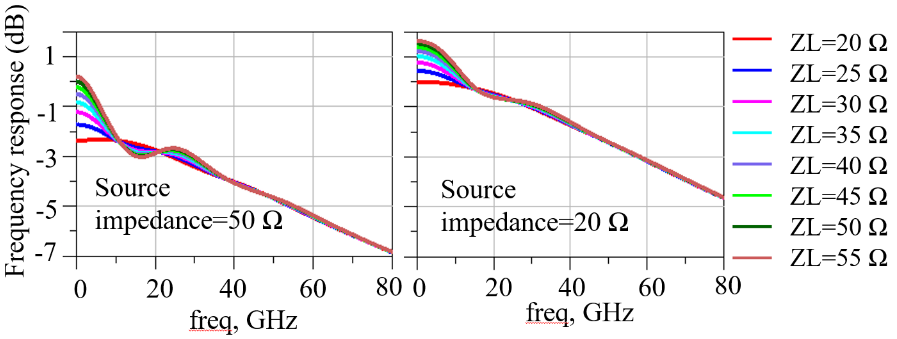


Figure 3.9: Electro-optic frequency response for varied termination load. Left: Source impedance at 50 Ω. Right: source impedance at 20 Ω.

connection network. A co-designed passive interconnection network is proposed between the 50 Ω driver and the 20 Ω phase modulator to increase the electro-optic bandwidth of the MZM and improve the eye-opening for on-off-keyed data. The co-design environment enables the combined chips to be optimally interconnected within the same simulation environment. The interconnect network proposed in figure 3.10 is designed as a passive filter with a high pass transfer function to suppress the low-frequency response in figure 3.6 to the level of the plateau. This equalizes the frequency responses to extend the modulation bandwidth. Component values have been selected to ensure that the network can also be designed on a BiCMOS platform using standard lumped elements with a half-millimeter square size. The approach leads to a trade-off between modulation efficiency and bandwidth, as the applied voltage on the phase modulator is reduced for frequencies below 20GHz. The network is subsequently implemented in ADS to predict the small and large signal performance of the modulator. Bandwidth flattening is observed in both the response of the transmission line and also the MZM. Figure 3.11 shows that the passive interconnection network increases the -3 dB electro-optic modulation bandwidth of the reference HCPW-MZM from 30 GHz to 63 GHz by flattening the frequency response. The large signal performance is also simulated. The condition with direct wideband connection is compared with the customised interconnection network. In both cases, a 50 Ω driver and a 50 Ω resistive termination is used. Figure 3.12 shows the effect of the co-designed passive interconnection network on the optical-eye-diagram of the reference design when the

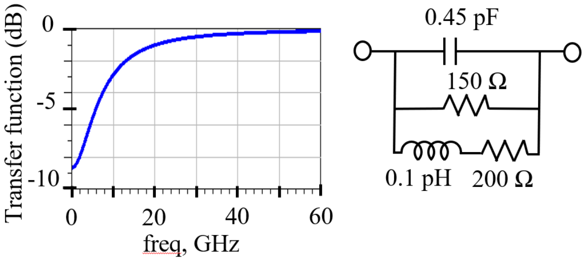


Figure 3.10: Proposed interconnect network and the associated transfer function

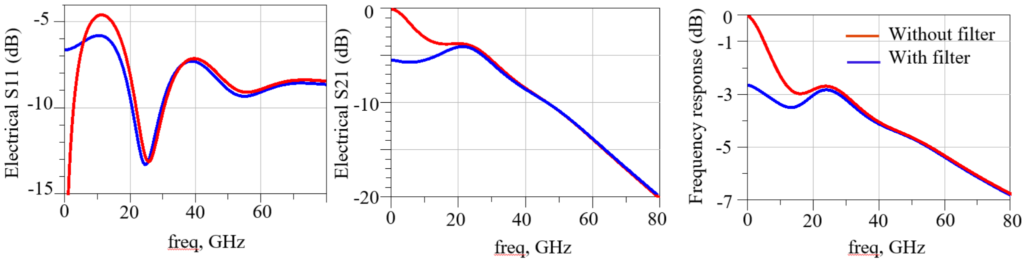


Figure 3.11: Bandwidth enhancement with interconnection network. Left: Electrical reflection and Middle: Electrical transmission for the phase modulator transmission line. Right: electro-optic frequency response of the MZM

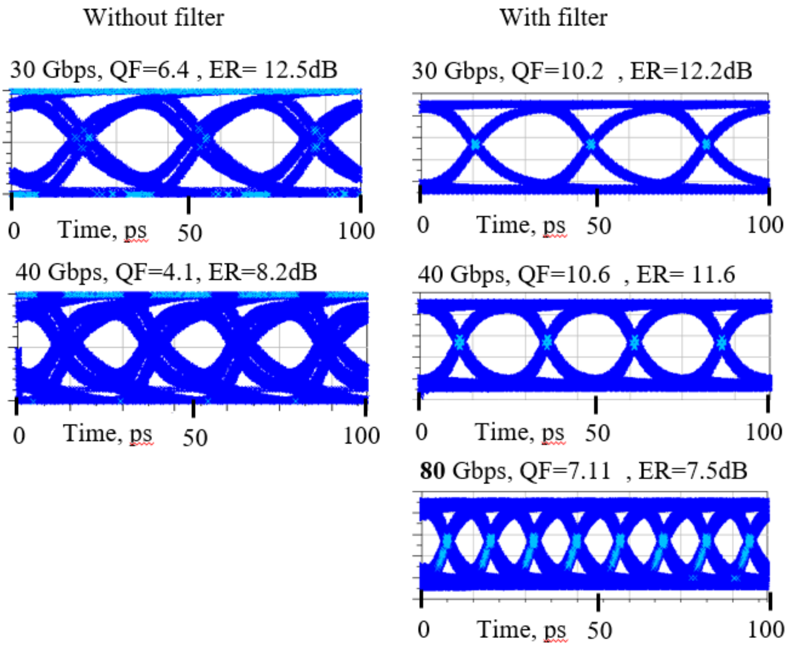


Figure 3.12: Large signal performance without (left) and with (right) a passive interconnection network using a 50 Ω driver and termination. From top left down, a broadband connection with 30 Gbps and 40 Gbps signals. From top right down, the passive interconnection network is included for with 30 Gbps, 40 Gbps and 80 Gbps modulation signals.

simulated applied voltage is $7.5Vp-p$. The eye quality and extinction ratio of the modulator is assessed by applying the full V_π. The role of the filter is quantified in terms of eye diagram quality factor and the extinction ratio.

The quality factor of the simulated eye diagram improves from 6.4 to 10.2 at 30 Gbps and from 8.2 to 11.6 at 40 Gbps. The interconnection network enables 80 Gbps modulation with 7.5 dB extinction ratio and a quality factor for the optical eye-diagram of 7.11 dB.

3.6 Summary

In this chapter, we proposed a co-design methodology for the optimization of high-speed characteristics in Mach-Zehnder modulator-based transmitters. The approach uses a parametric, non-iterative, traveling-wave model for the phase modulators, which is readily incorporated with the optical circuit and driver networks. The model uses only measurable design parameters such as layer thicknesses, materials properties, and mask feature dimensions. We validated the model accuracy by comparing to the measurement data of a reference foundry-produced indium phosphide HCPW-MZM. The electronic-photonic co-design is validated with both small and large-signal modeling of the electrically connected device.

The co-designed model is used to study impedance matching. By matching the load termination impedance to the transmission line impedance of the MZM, the 3 dB optical modulation bandwidth is observed to increase from 30 GHz to 57 GHz, representing a two-fold increase relative to the 50 Ω termination condition. Moreover, a co-designed passive interconnection network is proposed between the 50 Ω driver and the 20 Ω phase modulator to increase the electro-optic bandwidth of the MZM and improve the eye-opening for on-off-keyed data. The passive electrical pre-compensation predicted a 3 dB optical modulation bandwidth to increase from 30 GHz to 57 GHz and double the large-signal modulation bandwidth of the reference HCPW-MZM to 80 Gbit/s for on-off-keyed modulation with a 7.5 dB extinction ratio. Further bandwidth increases may be anticipated with driver and phase modulator optimizations.

In this chapter, we showed that matching the source impedance to the characteristic impedance of the MZM increases the simulated electro-optical response. However, the characteristic impedance of the HCPW-MZM studied in this work is 20 Ω, which is much smaller than the standard 50 Ω electrical circuit. Moreover, we showed that matching the termination impedance increases the simulated electro-optical bandwidth. Termination resistors (R) connected to the output of the transmission line lead to resistive losses. In the single-ended HCPW-MZM, most of the transmitted electrical power through MZM is consumed in the termination at the voltage V as V^2/R. To decrease this power consumption, a MZM with higher impedance is desired.

Chapter 4

High-density and high-speed Mach-Zehnder modulators

4.1 Abstract

This chapter proposes a high-density and high-speed Mach-Zehnder Modulator (MZM) with a new coplanar strip-line (CPS) electrode design. The width of the proposed CPS-MZM is much smaller than the conventional capacitively-loaded or coplanar waveguide MZMs. The CPS electrode design allows new electrode geometries which can be much narrower and more closely spaced, allowing a pathway to impedance engineering and high density. We investigate the limitations to the matching of optical and electrical velocity and impedance of the phase modulators for improved bandwidth and modulation efficiency, and we answer the following question:

What are the density and speed limits of the generic InP platform?

To address this question, in this chapter, we first study the effect of the substrate on the electrical loss of the CPS-MZM. We simulate the radio-frequency (RF) electrical loss of the CPS-MZM in the semi-insulating (SI) substrate, and we show that it has 1.5 times lower loss compared to the same modulator with a n-doped substrate. Then three main critical-to-performance mask parameters are identified and optimized for the coplanar stripline MZM. The theoretical study is performed for the semi-insulating generic process, which supports the highest speed operation. The designs are taped out on a dedicated semi-insulating (SI) process and additionally on an n+ multi-project wafer process.

The measurement results of the CPS-MZM in a n-doped substrate with the conventional CPW-MZM produced in the same platform are compared. We show that the high-density, 27 μm wide, Mach-Zehnder modulator with CPS electrode enables velocity and impedance matching, increasing the 3dB electro-optical bandwidth of 27.3 GHz, 3.6 times higher than a more conventional coplanar waveguide design with similar length and waveguide parameters is achieved.

Then the CPS-electrode design is adapted to a semi-insulating substrate, and fabrication is performed with an active-passive integration process. Modulators with a 67 GHz electro-optic bandwidth at -1.4 dB are demonstrated on a generic foundry platform, supporting

monolithic integration with lasers, detectors, and passive waveguides. The modulator electrode design is miniaturized to allow a high packaging density with a Mach-Zehnder pitch of below 25 μm.

4.2 Introduction

MZM components have been studied in the generic InP platform [15]. However, the bandwidth is constrained by high electrical loss in these HCPW electrode designs, and the line impedance is limited to 25 Ω [16, 17] at high frequencies, leading to undesired electrical reflections. Also, these modulators have high microwave indexes, which results in the walk-off between the electrical and optical signals.

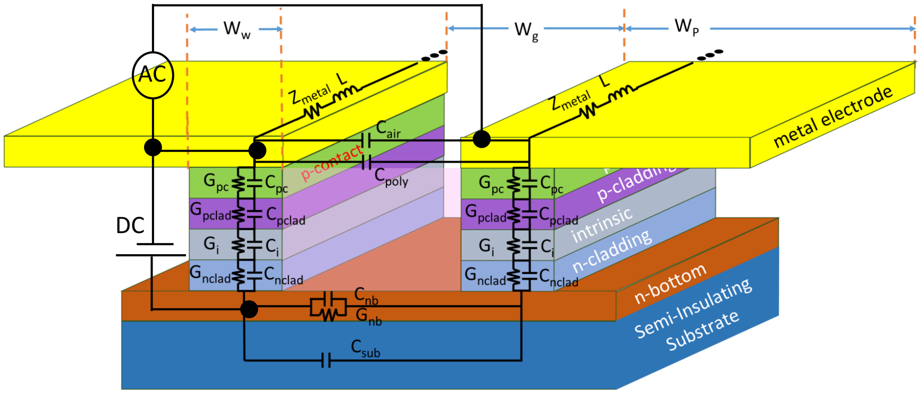


Figure 4.1: Cross section of the CPS-MZM in the generic InP platform, perunit length circuit elements and electrical connections

Coplanar stripline modulators have been widely modeled [66] and studied [9–12] in combination with horizontal p-i-n junctions for silicon photonics. It has also been used with vertical p-i-n junctions in GaAs modulators with a customized layer stack [67], but they place the two electrodes out of the plane at different heights on the chip.

In push-pull configuration, by placing the two electrodes in-plane at the same height, on top of the two waveguides, the capacitors in two MZM arms are in series, and the capacitance of the complete Mach Zehnder modulator is half of that for one phase modulator. This has been successfully used in CPS capacitively-loaded modulators and is one factor that leads to a speed increase [18].

Capacitively loaded Mach-Zehnder modulators are widely used in transmission systems due to their fast modulation speed and large optical extinction. In III-V material platforms, HHI fabricated 54GHz capacitively-loaded electrode MZM with the footprint of $10 \times 0.5mm^2$ [13] and NTT designed and fabricated n-i-p-n capacitively-loaded MZM [14]. However, having an additional transmission line next to the segmented electrodes increases the width of the MZM, limiting the achievable densities, while, the unloaded sections also lead to longer phase modulators. Moreover, the MZM designed by NTT is based on specifically tailored epitaxial layers [14].

In this work, we present a design for high-density, high-speed MZM, which just includes in-plane ultra-narrow CPS electrode on the two optical waveguides. Also, it is compatible with generic InP platform [15]. We propose design parameters for a short 1 mm long velocity-matched 50Ω CPS-MZM with a 3 dB EO-bandwidth of 95 GHz with the same VπL efficiency of 8 Vmm. Moreover, to prove the concept of velocity matching and impedance matching enabled by the CPS electrode design, we tape out the CPS-MZM in a multi-project wafer in a InP generic platform with n-doped substrate. To accomplish this study, the focus of this chapter is divided in following order.

In section 4.3, to study the impact of the substrate on the electrical loss of the CPS-MZM, we simulate the electrical radio-frequency attenuation constant of the CPS-MZM in both n-doped and SI substrate. Then we study the impact of the three mask parameters (waveguide width, electrode gap and electrode width) on the electrical and electro-optical responses of the CPS-MZM.

In section 4.4, to show the improvement of the electrical characteristics such as velocity and impedance matching results from the CPS electrode design, we directly compare the high-density CPS electrode design that has only 27 μm width with the more conventional CPW approach in the same platform. The substrate of both CPS and CPW modulators is n-doped. We study the impedance and velocity matching before addressing radio-frequency (RF) electrical losses and experimental performance.

Finally in section 4.5, since the n+ substrate limits the bandwidth of the CPS-MZM, we design the CPS-MZM in a generic InP platform with SI substrate. We measure the electrical and electro-optical responses of the very high-density CPS-MZM with 17 μm width. We show that this modulator has 67 GHz electro-optic bandwidth at -1.4 dB.

4.3 Simulation

Figure 4.1 shows the cross-section of a 1 mm long push-pull CPS-MZM electrode in the generic InP platform with SI substrate and how it is connected to the DC and AC sources. The two metal electrodes on top of the optical waveguides are driven by an AC signal and terminated with a load. Figure 4.1 also shows the cross-sectional equivalent circuit elements of the MZM, which have per unit length (PUL) values. Calculation of the PULs is described in detail in chapter 3 of this thesis. The cross-sectional equivalent circuit has been implemented in the Advanced Design System (ADS), which facilitates its embedding within electrical interconnect, 50 Ω load, and source networks. In this circuit, Z_{metal} is the metal-air impedance of the electrodes [53], L is the inductance of the CPS line [59], $C_{\text{pc,i,ncald,pclad,nb}}$ are the capacitances of the semiconductor layers below the metal lines under parallel plate approximation. C_{air} and C_{sub} are partial capacitances in the absence of all non-metal material and substrate, respectively [57]. $G_{\text{pc,i,ncald,pclad,nb}}$ are the conductance of each semiconductor material of the optical waveguide [53]. The electrical losses of the SI substrate are neglected. Cross-sectional parameters shown in table 2.1 (chapter 2) which are taken from [37] are used.

To see the impact of the n-doped substrate on the high-speed electrical loss, we use the electrical model described in the section 2.3.1 of this thesis for comparing the radio-frequency (RF) attenuation of the CPS-MZM in both SI and n-doped substrate.

Then we use the spatially resolved circuit model described in the section 3 of this thesis, and we study the impact of the three mask parameters (waveguide width, electrode gap and electrode width) on the electrical and electro-optical responses of the CPS-MZM. We simulated the effect of the waveguide width; we also studied the gap and widths of the electrodes. Assuming the small-signal approximation [33], the model is able to yield the

EO-frequency response of the modulator. As it is described in of chapter 3 of this thesis (section 3.3.1), the spatially resolved circuit model can also perform time-domain large-signal simulations. We performed a time-domain large-signal simulation and obtained the optical eye diagram response of the CPS modulator in the SI substrate.

4.3.1 Effect of the substrate

To see the impact of the substrate on the high-speed electrical loss, we compare the radio-frequency attenuation of the CPS-MZM in both SI and n-doped substrate. We use the electrical model described in section 2.3.1 of this thesis, and we simulate the CPS-MZMs with n-doped and SI substrate. In the simulation, waveguide width (W_w) is 1.5 μm, electrode gap (W_g) is 7 μm and electrode width (W_p) is 10 μm. Cross-sectional parameters are as in 2.1. The conductivity of the n-doped substrate is 57600 (S/m) [37].

Figure 4.2 depicts the comparison between the electrical radio frequency attenuation of the CPS-MZM with n-doped and SI substrates. This figure shows that the electrical loss in the CPS-MZM with a SI substrate is about 1.5 times lower than the same MZM with an n-doped substrate. This lower electrical loss in the cross-section of the CPS-MZMs in the SI substrate is estimated to result in the higher electro-optical bandwidth compared to the same CPS-MZM with an n-doped substrate.

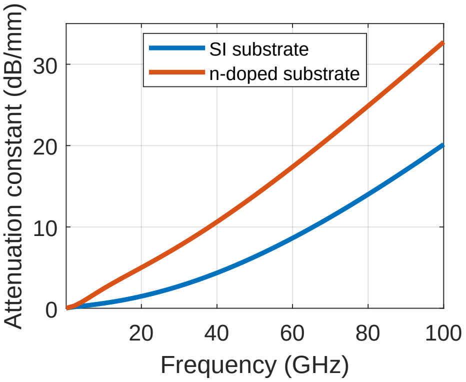
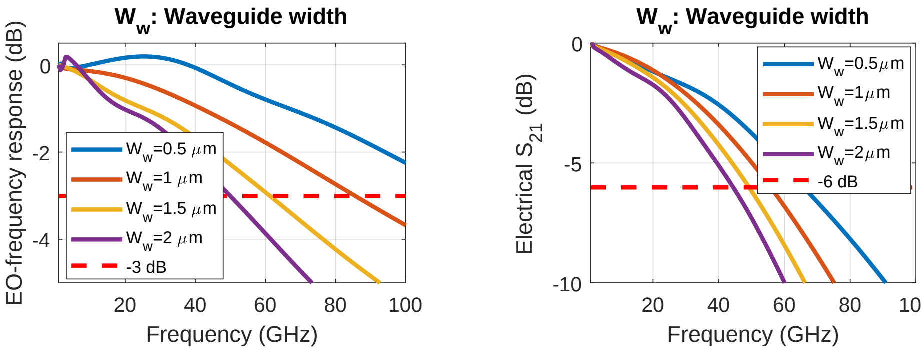


Figure 4.2: Comparison between the electrical radio frequency attenuation of the CPS-MZM with n-doped and SI substrates.

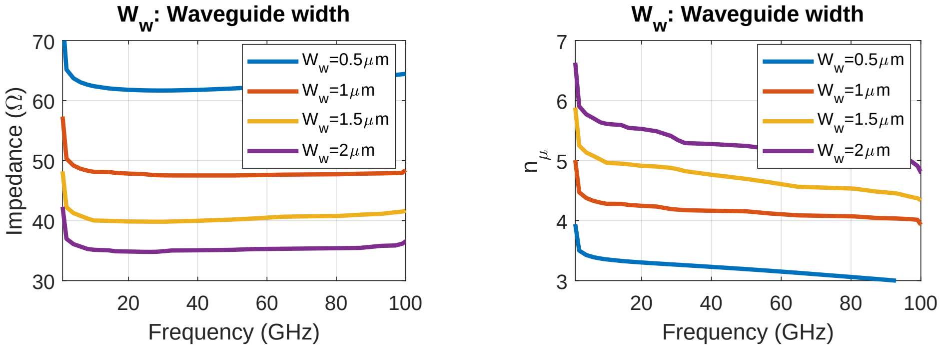
4.3.2 Effect of the waveguide width

We study the effect of the waveguide width on the characteristics of the CPS-MZM with SI-substrate. Figure 4.3 shows that reducing the waveguide width is beneficial in all aspects. By reducing the waveguide width, W_w, and keeping the electrode gap and width at 10 μm, the cross-sectional electrical loss of the semiconductor reduces significantly. As shown in figure 4.3b narrower waveguide has higher -6 dB Electrical bandwidth. Reducing the waveguide width from 2 μm to 0.5 μm increases the -6 dB electrical bandwidth of the CPS-MZM from 45 GHz to 69 GHz.



(a) EO-frequency response

(b) Electrical S21 (dB)



(c) Frequency dependent characteristic impedance (Ω)

(d) Frequency dependent microwave index, n_{μ}

Figure 4.3: Effect of waveguide width on a) EO-frequency response of the CPS-MZM, b) electrical S21, c) frequency-dependent line impedance and d) microwave index.

To increase the line impedance, as in equation 2.5 [38], the capacitance of the traveling wave electrode has to be decreased. Reducing the waveguide width also reduces the parallel plate capacitance of the semiconductor waveguide region, which is the dominant capacitance of the traveling wave electrode. As it is shown in figure 4.3c, since the narrower waveguide has smaller capacitance, it shows higher line impedance. Waveguide width of 0.5 μm results in the line impedance of 62 Ω at 50 GHz while at the same frequency, 2 μm waveguide width has a line impedance of 35 Ω.

The group index of light in the InP waveguide is 3.7. The microwave index has a direct relation to the square root of the line capacitance [38]. Reducing the microwave index results in a better velocity match. Figure 4.3d shows that waveguide width of 0.5 μm results in the microwave index of 3.0 at 100 GHz while at the same frequency, 2 μm waveguide width has a microwave index of 4.9.

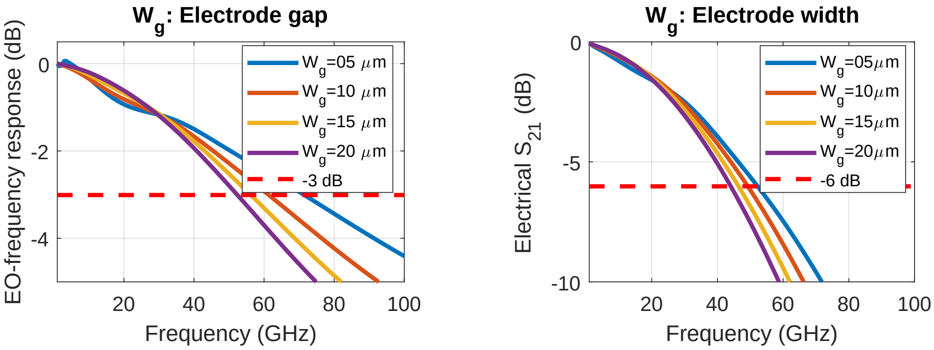
A narrow waveguide provides a wider EO-bandwidth by closer impedance matching between electrodes and electrical circuit, velocity matching, and low microwave loss. In figure 4.3a the electro-optical response is depicted. It shows that by reducing the waveguide width from 2 μm to 0.5 μm, the EO-bandwidth of the CPS-MZM increases from 50 GHz to over 100 GHz.

4.3.3 Effect of the electrode gap

We study the effect of the electrode gap on the characteristics of the CPS-MZM with SI-substrate. As in equation 2.5 [38], line impedance has a direct relation to the square root of the line inductance, therefore, decreasing the gap from 20 μm to 5 μm when W_w=1.5 μm and W_p= 10 μm reduces the line impedance at 100 GHz from 48 to 34 Ω. The microwave index has a direct relation to the square root of the line inductance. Reducing the waveguide gap reduces the microwave index, and it results in a better velocity match. Decreasing the gap from 20 μm to 5 μm when W_w=1.5 μm and W_p=10 μm decreases the microwave index at 100 GHz from 5.0 to 3.8.

Figure 4.4 shows the effect of electrode gap on a) EO-frequency response and b) electrical S21 of the CPS-MZM with SI substrate. Figure 4.4b shows the effect of the electrode gap on the electrical transmission (S21) of the CPS-MZM. The lower n-doped semiconductor layer (n-bottom layer in figure 4.1) has the electrical conductivity of 27600 S/m [37]. Since narrower gap W_g results in a smaller dimension of this layer in the cross-section of the CPS-MZM, reducing the electrode gap reduces the electrical loss of this layer and by that the electrical bandwidth increases (more information in section 2.6 of this thesis). In figure 4.4b, decreasing the electrode gap from 20 μm to 5 μm (when W_w=1.5 μm and W_p= 10 μm) increases the -6 dB electrical bandwidth from 45 GHz to 62 GHz.

In figure 4.4a, decreasing the gap from 20 μm to 5 μm when W_w=1.5 μm and W_p=10 μm by increasing the electrical bandwidth and matching the microwave and optical indexes, increases the EO-bandwidth from 55 GHz to 70 GHz.



(a) EO-frequency response

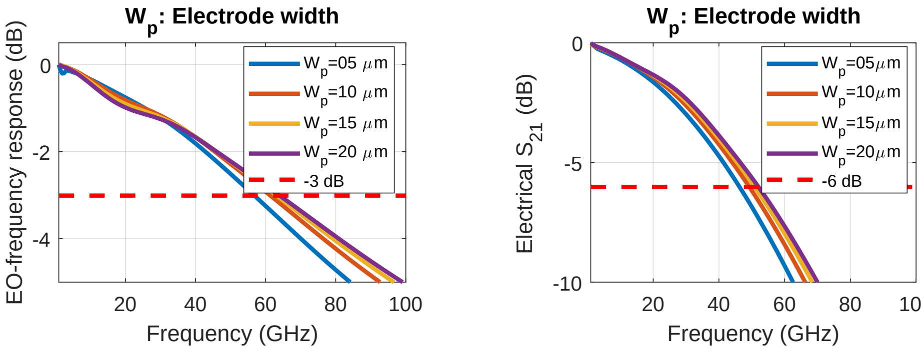
(b) Electrical S21 (dB)

Figure 4.4: Effect of electrode gap on a) EO-frequency response and b) electrical S21 of the CPS-MZM with SI substrate

4.3.4 Effect of the electrode width

We study the effect of the electrode width on the characteristics of the CPS-MZM with SI-substrate. Increasing the W_p also reduces the inductance, and by that line impedance reduces from 45 to 38 Ohm, and the microwave index increases from 4 to 5 at 100 GHz. But these changes are minimal comparing to the effect of the waveguide width and waveguide gap.

In figure 4.5 we show the effect of electrode gap on a) EO-frequency response and b) electrical S21 of the CPS-MZM with SI substrate. Figure 4.5 shows that the effect of the electrode width W_p is minimum comparing to the waveguide width and electrode gap. In figure 4.5b when W_g= 10 μm, W_w=1.5 μm, and W_p increases from 5 μm to 20 μm the electrical bandwidth increases from 55 GHz to 65 GHz. Figure 4.5a shows that changing the electrode width only increases the EO-bandwidth by about 10 GHz when W_g=10 μm, W_w=1.5 μm, and W_p increases from 5 μm to 20 μm.



(a) EO-frequency response

(b) Electrical S21 (dB)

Figure 4.5: Effect of electrode width on a) EO-frequency response and b) electrical S21 of the CPS-MZM with SI substrate

4.4 CPS-MZM in a n-doped substrate

To show the improvement of the electrical characteristics such as velocity and impedance matching results from the CPS electrode design, we directly compare the fabricated high-density CPS electrode design that has only 27 μm width with the more conventional CPW approach in the same platform. The substrate of both CPS and CPW-MZMs is n-doped. We study the impedance and velocity matching before addressing radio-frequency (RF) electrical losses and experimental performance.

Figure 4.6 shows the photonic integrated circuit (PIC) cell assessed in this work. The cell has dimensions of $4 \times 4.6\,(mm^2)$; and is produced on a multi-project wafer with the JePPIX [65] InP generic platform[1]. An n-doped substrate is used, enabling direct comparison with a previously produced CPW design [37]. Because of the electrical loss, the use of an n-doped substrate will limit the bandwidth, but the design is portable to a higher speed

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[1] Chip fabrication is done with the JePPIX multi-project wafer service by SMART Photonics

Figure 4.6: Photonic integrated circuit cell including 22 modulators under electro-optical measurement

in a semi-insulating platform. The cell includes twenty-two CPS modulators: half have 1 mm length phase modulators, and the other half have 2 mm length. The width of the CPS modulator is 27 μm. This compares to a width of 110 μm for the CPW modulator design. The difference in cross-sections for the CPW and CPS designs is shown in figure

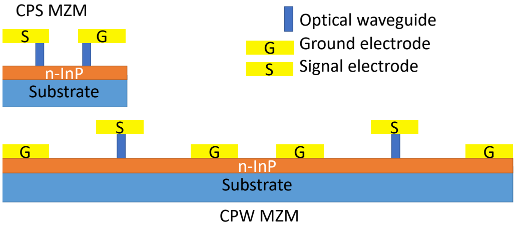


Figure 4.7: Cross section of the traveling wave electrodes for the phase modulator sections in the CPS and CPW designs.

4.7. Waveguide width and other waveguide parameters are the same as for the previous CPW design. The width of all ground and signal electrodes is 10 μm, and the gap between the ground and signal is 10 μm and 7 μm in the CPW and CPS, respectively. In the CPS modulator, two signal electrodes are in-plane and placed on the optical waveguides. In the CPW modulator, there are six traveling wave traces: both the signal electrodes on the optical waveguides and pairs of ground electrodes on the top of the n-doped layer. There are three times as many electrodes for the CPW design. There is also an additional gap of 10 μm between the two CPW traveling wave electrodes. By reducing the number of electrodes and the gap between them in the CPW-MZM, the width of the design is reduced from 110 μm to 27 μm.

4.4.1 Impedance matching

The difference in cross-section is expected to directly impact the electrical impedance and, therefore, the impedance matching to the 50 Ω measurement equipment. The modulators are probed on-chip and measured with a 67 GHz bandwidth vector network analyzer. Figure 4.8 shows the electrical reflection at the input port (S11) of the 1 mm CPS and 1.25 mm

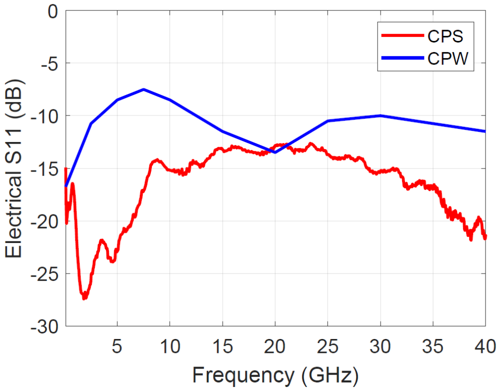


Figure 4.8: Electrical reflection (S11)

CPW [37] modulators at -3.8 V DC. The peak reflection for the CPW is -7.5 dB, while the CPS design has a reflection peak of less than -13 dB. The 5.5 dB reduction of the electrical reflection in the CPS modulators is attributed to the improved impedance matching. The extracted impedance values at 0 V DC and 40 GHz are 41.5 Ω and 17.5 Ω for the CPS and CPW designs, respectively.

4.4.2 Reducing the radio-frequency loss

The smaller width of the CPS-MZM in this work has the advantage of including fewer n-InP and n-substrate regions in the cross-section of the high-speed phase shifter of the MZM. Since there is reduced overlap between metal traces and lossy semiconductor regions, the CPS electrode of this work is expected to have a much lower electrical loss than CPW. The radio-frequency attenuation constant, defined as the real part of the electrical propagation constant, is calculated by de-embedding the measured electrical scattering parameters of the CPW and CPS electrode designs with two different length designs at 0V DC. In Figure 4.9, we compare the RF electrical attenuation constant of the CPS and

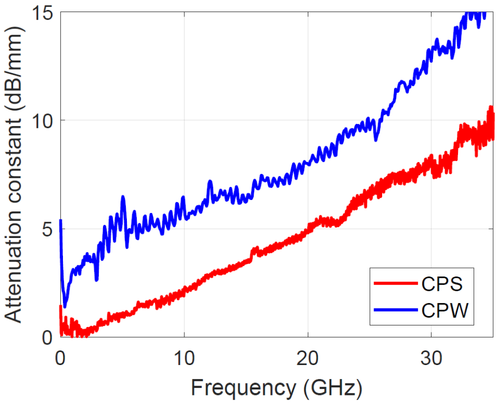


Figure 4.9: RF electrical attenuation constant of the CPS and CPW electrodes

CPW electrodes. We see that the CPS electrode has a much lower electrical attenuation constant in the whole range of the depicted frequency.

4.4.3 Velocity matching

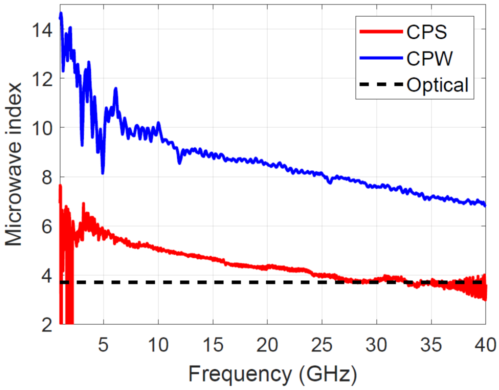


Figure 4.10: Frequency-dependent microwave index of the CPS-MZM

The CPS design enables the matching of optical and microwave impedances for improved electro-optic bandwidth. The electrical refractive index (also known as the microwave index) of both CPW and CPS modulators is determined by de-embedding the measured electrical scattering parameters of the CPW and CPS electrodes with two different length designs when 0 V DC voltage is applied. The group index of the optical waveguide is 3.7.
Figure 4.10 compares the frequency-dependent microwave index of the modulators. This figure shows that the microwave index of the CPS modulator is much smaller than the CPW modulator. We also see that at the higher frequency ranges, when the electrical signal is shorter and velocity matching is more important, the microwave index of the new CPS modulator design is in very close agreement with the optical index. This means that the new design is velocity matched at the higher frequencies.

4.4.4 Electro-optical performance

Figure 4.11 shows the schematic of the setup for measuring the EO-frequency response. The electro-optic performance is measured by connecting a 1550 nm, +14 dBm optical signal to a single-mode optical fiber which couples light to the facet of the chip. The output fiber transfers light passed through the MZM to the optical amplifier, optical bandpass filter, and then the optical port of the lightwave component analyzer. An electrical probe is used for applying the high-speed electrical signal from the lightwave component analyzer to the CPS traveling wave electrode. The electrical output of the traveling wave electrodes is connected to 50 Ω termination by a second electrical probe. A DC voltage referenced to the ground of the RF signal generator is applied to the n-substrate to ensure appropriate biasing across each phase modulator for single-ended modulation. Figure 4.11 shows the normalized EO-frequency response of the 1 mm CPS modulator and the CPW modulator

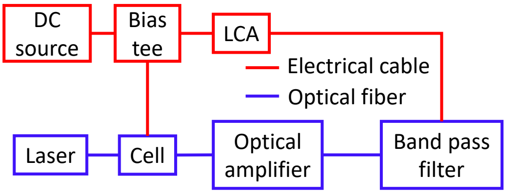


Figure 4.11: Setup for EO-frequency response

with 1.25 mm length [37]. The 3 dB EO-bandwidth of the CPS modulator for 1 mm length is 30 GHz, and the CPW is 7.5 GHz. DC bias of both modulators is -3.8 V. The longer length of the CPW design will lead to a small bandwidth reduction. The bandwidth of the 2 mm CPS modulator is 18 GHz. From the de-embedding of EO-bandwidth of the CPS-MZM with 1 and 2 mm lengths, the 3 dB EO-bandwidth of a 1.25 mm CPS modulator is estimated to be 27.3 GHz. This is 3.6 times the bandwidth of the CPW modulator of the same length.

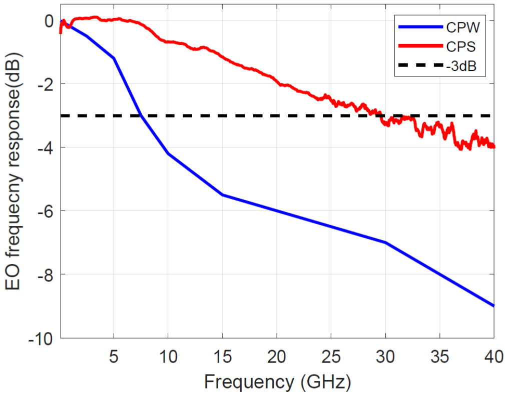


Figure 4.12: Comparison between the normalized EO-frequency responses of the 1 mm CPS-MZM and 1.25mm CPW-MZM

VπL of the CPS modulator is 0.8 Vcm, and optical insertion loss of the Mach-Zehnder modulator is estimated to be 9.8 dB, which is similar to the CPW design with an insertion loss of around 10 dB [37].

4.5 CPS-MZM in a semi-insulating substrate

A 27 μm wide, CPS Mach-Zehnder modulator with n-doped substrate enables velocity and impedance matching, increasing the 3 dB electro-optical bandwidth to 30 GHz for modulator length of 1 mm. This design was bandwidth limited by the n-doped substrate. Therefore, in this section, the design is adapted to a semi-insulating substrate, and an active-passive process has been implemented. The performance of the produced modulators is assessed for small signal electrical and electro-optical operation, highlighting the close agreement with the design intent.

4.5.1 Modulator design

The generic foundry process enabling this work has been previously reported [15]. In this work, the multi-quantum-well modulator layer stack has been designed [2] to enable the butt-join regrowth integration with the lasers and detectors. Electrode designs have been re-engineered to enable top-side n-contacts for the n-layers, which are grown on a semi-insulating substrate. The electrode configuration to enable high density and high speed has been optimized with an advanced, spatially resolved circuit model.

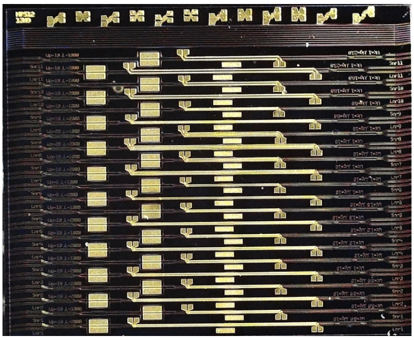
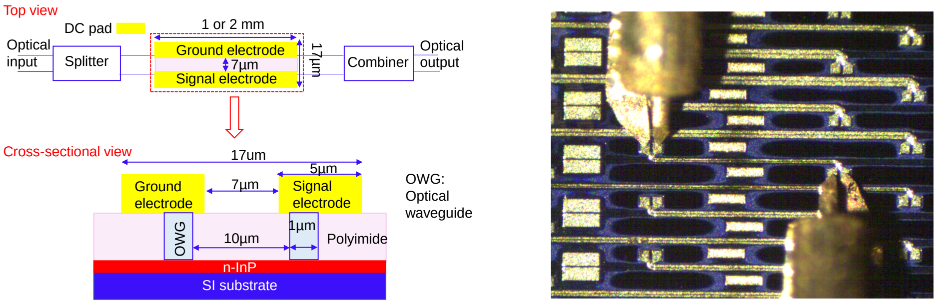


Figure 4.13: High-density modulators: A microscope image of a 4.6 mm x 4.0 mm cell containing 22 Mach-Zehnder modulators. Devices 11 and 12 from the bottom are assessed

The measurements reported for a range of Mach-Zehnder modulators with CPS designs in a InP Generic Foundry Platform with semi-insulating substrate, as shown in figure 4.13. Modulators have been fabricated in a dedicated run with an additional multi-quantum-well into the layer stack. The image shows the input and output optical waveguides on the left and right. The electrical connections are probed.



(a) Mask level detail

(b) Device 12 under test

Figure 4.14: Co-planar waveguide modulators: a) Mask level detail with design intent. Aspect ratio adjusted to emphasize design features. b) Image of device 12 under test with RF probes applied. Phase modulators are 1 and 2 mm in length.

The assessed devices with the top and cross-sectional view, as depicted in figure 4.14, have

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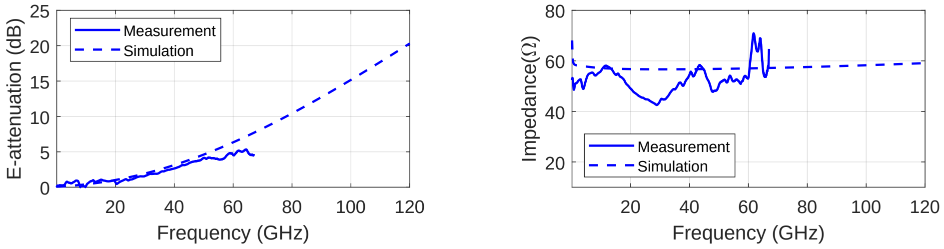
[2] Multi-quantum-well layers are designed by Weiming Yao

a designed waveguide width of 1 μm, and signal electrode widths of 5 μm. [3] The separation between the electrodes is 7 μm, leading to a modulator width of 17 μm and the possibility to integrate devices on a pitch of order 25 μm with the current technology. The design intent is to maximize bandwidth through impedance matching to the source and load of the 50-Ohm measurement system for the minimization of reflections and also to maximise efficiency at higher frequency through reduced velocity mismatch due to reactance of the electrodes.

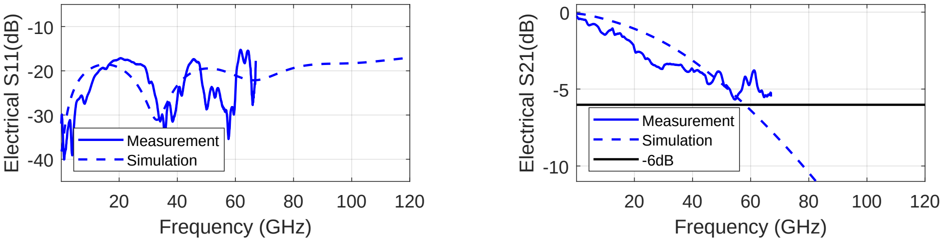
4.5.2 Electrical performance

The RF electrical design is first analyzed at zero DC bias using a vector network analyzer. The calibration procedure is done by probing an on-wafer calibration kit. The electrical attenuation, defined as the real part of the electrical propagation constant, is determined by de-embedding the measured electrical scattering parameters of the CPS modulators with two different length designs. The S11 reflections are determined with the second port terminated to 50 Ohm. Impedance is verified to be within the range 40-60Ohm over the measurement range available.



(a) Electrical loss

(b) Impedance



(c) Electrical S11

(d) Electrical S21

Figure 4.15: Small-signal electrical characteristics at 0V DC bias for the 1 mm device. Solid lines for measurement, dashed lines for the design intent. a) Electrical losses from input probe to output probe b) Impedance of the electrodes c) Reflections from modulator to input d) Transmission from input to output of the modulator

Simulation data is included in figure 4.15 to show excellent agreement over the ranges

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[3] Chip fabrication is done by SMART Photonics

which can be measured, and to indicate the design limited performance, which may be anticipated.

4.5.3 Electro-optical performance

The DC electro-optic modulation response is analyzed at the wavelength 1550 nm has VπL of 7.5 Vmm with an extinction ratio of about 30 dB. The optical insertion losses for the full device are 8.6-9.1 dB and are within the range of the previous works with an insertion loss of 9-10 dB. These insertion losses exclude the fiber coupling losses. In figure 4.16 large-signal performance is simulated for 7.5 and 3.8 Vp-p electrical signals applied to 1 mm and 2 mm long MZMs, respectively. The eye diagram has been calculated for a non-return-to-zero (NRZ) data sequence of 2^8 bits. 1 mm long MZM potentially facilitating 200 Gbit/s modulation with the quality factor (QF) of 9.5 with appropriate electronic input signal and connections. The longer 2 mm design requires lower input voltage, still facilitating 100 Gbit/second modulation with a high QF of 16.7. The RF electro-optic (EO) modulation responses are performed with Agilent's lightwave component analyzer model N4373C for the 1 mm and 2 mm long designs depicted in figure 4.17. An optical amplifier

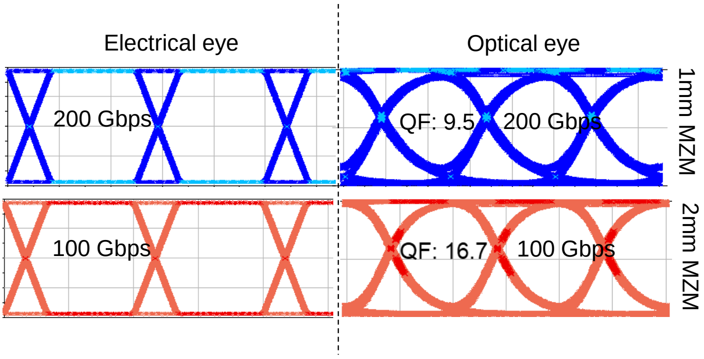

Figure 4.16: Eye diagram: electrical input and optical output eye simulations for devices with 1 mm (blue) and 2 mm (red) phase modulators.

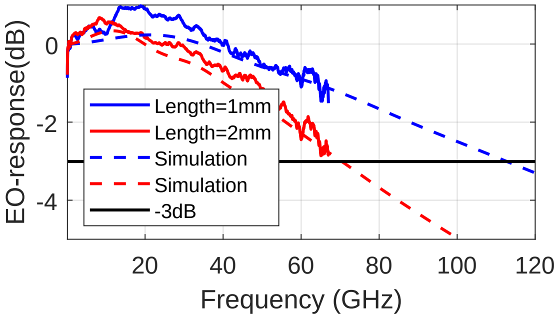

Figure 4.17: Eye diagram: electrical input and optical output eye simulations for devices with 1 mm (blue) and 2 mm (red) phase modulators.

and a passive optical bandpass filter have been used in the S21 measurements. The InP platform would, of course, enable placement of SOAs at arbitrary locations and at high density.

The close match between experiment and simulation is observed for both device lengths. With currently available equipment, the electro-optic bandwidth is measurable only to 67 GHz, where a 1.4 dB drop in the frequency response is observed for the 1 mm long device. Simulations preduct that the inherent device bandwidth extends to beyond 110 GHz. The longer 2 mm design will enable a reduced drive voltage for large-signal modulation but leads to a compromise in electro-optic bandwidth, measured here to be slightly above 67 GHz.

Reducing this modulator's electrode width and gap to 2 μm is predicted to have a 3 dB bandwidth of 114 GHz and an even higher density with total 6 μm width. However, electrode width below 5 μm and electrode gaps smaller than 7 μm are not manufacturable with the current technology.

4.6 Summary

A new CPS electrode design for the high-density, high-speed InP Mach-Zehnder modulator is presented. This CPS electrode design enables velocity, and impedance matching also increases the density of the MZMs. The effect of the substrate on the RF performance of the CPS-MZM was studied and showed that SI substrate has about 1.5 times lower loss than the n-doped substrate. We then studied the effect of the three mask parameters on the frequency-dependent microwave index, line impedance, and electrical and electro-optical responses of the CPS-MZM with the SI substrate was simulated.

The CPS-MZMs are taped out on a dedicated semi-insulating (SI) process and additionally on an n+ multi-project wafer process. The n+ circuits were available for measurements. We compare the CPS-MZM in a n-doped substrate with the conventional CPW-MZM produced in the same platform. Measurement results prove the velocity and impedance matching enabled by CPS electrode design. The design of the CPS electrode allows a width reduction from 110 μm in the CPW electrode to 27 μm in the CPS electrode, allowing a fourfold increase in density. A length-normalized bandwidth increase of 19.8 GHz is also observed, providing a path to order of magnitude bandwidth density improvements.

An ultra-high-density, 100 GHz class InP CPS Mach-Zehnder modulator integrated with an InP generic foundry platform with a semi-insulating substrate is presented. This modulator has a 1.4 dB electro-optic bandwidth of 67 GHz, and a predicted 3 dB bandwidth of over 110 GHz is potentially capable of facilitating 200 Gbit/s modulation. In addition, a modulator width of 17 μm allows a high packaging density with a Mach-Zehnder pitch of below 25 μm. Therefore, the CPS modulator of this work has a pathway to multi-Terabit picoJoule/bit systems.

Chapter 5

Through polymer vias

5.1 Abstract

The need for higher bandwidth optical links with lower power consumption is driving increasing levels of integration. Transmitters with multiple wavelength channels have been demonstrated on generic integration platforms [68] and with high data rates per wavelength on customized integration platforms [69, 70]. However, this leads to higher numbers of electrical connections per chip, motivating tighter integration between electronics and photonics [71]. Therefore, in this chapter we describe a key enabling step towards ultra-tight 3D integration of electronic and photonic circuits at wafer scale.

3D integration provides flexibility for physically-close co-integration of the electronic and photonic integrated circuits which are made with different technologies. Distances between bond pads can be reduced to microns, and bond wires can be removed from the assembly. This is important for high-speed applications when parasitics reduce the bandwidth of the co-packaged devices. This chapter's central question is:

How do we build a scalable co-designed 3D integration technique, suitable for close connection of electronic to photonic integrated circuits?

To answer this question, methods for metal interconnection through the adhesive polymer bond layer between the two wafers are developed. Evaporated seed layer is used for making through-polymer vias with sloped sidewalls. The electrical performance is assessed from scattering parameters of these vias. They show a very high-speed performance with less than 0.5 dB electrical loss in the measurement range of up to 67 GHz. Furthermore, to check the strength of these vias, the mechanical reliability of vias is tested with temperature cycling.

Then the via density limits are studied and for more compact structures with lower parasitics, atomic layer deposition is introduced to create seed layer for steep sidewall through polymer vias. Couple of these vias show high-speed performance, with less than 0.4 dB loss up to 67 GHz frequency, making them promising candidates for wafer scale co-integration of photonic-electronic devices.

5.2 Introduction

Increasing demand in data traffic brings a need for technologies with higher capacity, faster speed, and better power efficiency. To meet these requirements, increased application of photonic interconnects and high-speed co-integrated photonic-electronic devices is expected [3]. In high-speed photonic-electronic devices, electronic integrated circuits (EICs) and photonic integrated circuits (PICs) are usually created separately using different technologies and are connected afterward to form a module. The connection between these technologies is now becoming a major performance bottleneck.

3D integration can provide the physically close co-integration of electronic and photonic devices on dice/wafers. Wafer (or die) bonding is a 3D co-integration technique whereby two or more wafers of similar or dissimilar materials are often permanently attached or bonded together. The individual wafers might have already been through previous fabrication steps, providing them with various features, or they might just be plain wafers [72]. Wafer bonding is an important, well-established technology, used in making and packaging sensors, actuators, and microsystems [73–80]. It is also used in the fabrication of integrated circuits, and the production of the composite materials and wafers needed in advanced circuit technologies [81]. Also, because the close connection of wafer-bonded devices has the advantage of low electrical parasitics, this technique was used for packaging RF Micro-electromechanical systems (MEMS) [82, 83]. Since wafer (or die) bonding has the advantage of connecting wafers with different technologies. This technique has been used for the hybrid connections of electronic devices [29, 84], hybrid photonic devices for the connection of photonic sources to silicon photonics [85–98] and the hybrid connection of electronic and photonic integrated circuits [99–101].

In this work, we study the wafer (or die) adhesive polymer bonding approach for to reducing the electrical parasitics in the hybrid connection of high-speed electronic and photonic integrated circuits, which are produced separately and with different technologies in BiCMOS and InP platforms respectively. The study is further explained in the following chapter, and the content of the chapter is divided into the following sections.

In section 5.3, we develop a method for close connection of the wafer-bonded devices. We create through polymer vias (TPVs) with sloped sidewalls, which can be simply created using an evaporated seed layer. In section 1.2, we simulate the mechanical stress of the TPVs with different polymer thicknesses when the temperature changes from -40 to 80 °C. Then, to prove the mechanical reliability of the TPVs, by the 4-point electrical resistivity measurement method, we measure whether the resistivity of the developed sloped sidewall TPVs before and after a series of temperature cycles was applied, is changing. Then we measure the radio frequency scattering parameters of the transmission lines, designed separately in BiCMOS and InP, which TPVs connect after wafer bonding. We de-embed the high-speed scattering parameters of the TPVs, and we compare them with the simulation data.

To obtain TPVs with smaller footprints, we studied how to create steep sidewall TPVs. Section 5.4 describes how, we used atomic layer deposition of the Ruthenium seed layer to make steep sidewall TPVs [1]. We show how to reduce the number of process steps by utilizing InP and metal patterns as a mask for etching the polymer. Furthermore, in this section, we measure the transmission lines on the InP, which are connected to the top surface of the bare silicon wafer by the TPVs. We de-embed the scattering parameters of the

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[1] This work is done with the collaboration of the PMP group at TU/e

TPVs, and we compare them with the simulation data.
In section 5.5, we summarize the two methods that have been studied for high-speed metal connections between the electrical and photonic integrated circuit.

5.3 Bonding and sloped sidewall TPV

In this section, we study methods to create 3D vias realized through a polymer bonding layer. We first describe the overview of the steps required for making metal connections between InP and silicon wafers through the BCB bonding layer. Then we focus on the masking techniques for creating holes through thick layers of BCB and validate the most promising approach by creating gold-plated vias. We simulate the mechanical stress of the sloped sidewall TPVs in -50 to +300 °C temperature range, and by measuring the resistivities of the TPVs before and after the temperature cycling, we check the mechanical reliability of these vias. Also, for properly designing the co-designed mask for creating the sloped sidewall TPVs, in this section, we first use a 3D high-speed software that calculates the radio frequency (RF) scattering parameters of the TPVs. Then we measure the RF scattering parameters of the fabricated sloped sidewall TPVs created between the gold metal pads on the InP and aluminum metal pads on the BiCMOS silicon wafer [2]. Then from the measurement data, we de-embed the radio frequency scattering parameters of the TPVs. The details of this section are described as follows.
For creating the through polymer vias between the wafer-bonded devices, first, the InP and silicon wafers must be separately fabricated. These wafers can include metal pads and tracks. In the InP wafer fabrication, it is essential to have a thin layer of etch stop layer between the InP stack and InP substrate. This layer stops the etching of the InP stack when later we etch the InP substrate. For aligning the two wafers/dice, a set of co-designed alignment marks on the back or front of both wafers is necessary. Figure 5.1 shows the steps for making through polymer vias between the metals on two wafers/dice. We list the main steps for creating TPVs in follows, and since in different experiments of this work, the parameters of each step can be different, the details of the steps will be described later where the experiments are described.

1. To improve adhesion of the polymer on InP and silicon wafers, a thin layer of silicon oxide is deposited on both.
2. BCB polymer is spun on both wafers (or one wafer).
3. Wafers are aligned and then bonded under certain pressure and temperature.
4. The substrate of the InP wafer has to be thoroughly wet etched. Etching of the substrate stops on the etch stop layer. After this step, on the InP side, just the thin layer of the stack remains. Then the etch-stop layer also has to be removed.
5. To access the metal layers on the InP, windows are etched through the layer stack.
6. To reach the metal layer on the silicon wafer, BCB polymer is etched.
7. A seed layer is deposited on the wafer. This layer has to cover the whole surface, as well as the sidewalls of the etched polymer openings.
8. A patterned mask defines the contact section of the metal connections.
9. With electroplating, metal connection between the metal on the InP to the metal on the silicon is made.
10. Finally, the patterned mask and the seed layer can be removed.

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[2] This work is done within the European WIPE project [102]

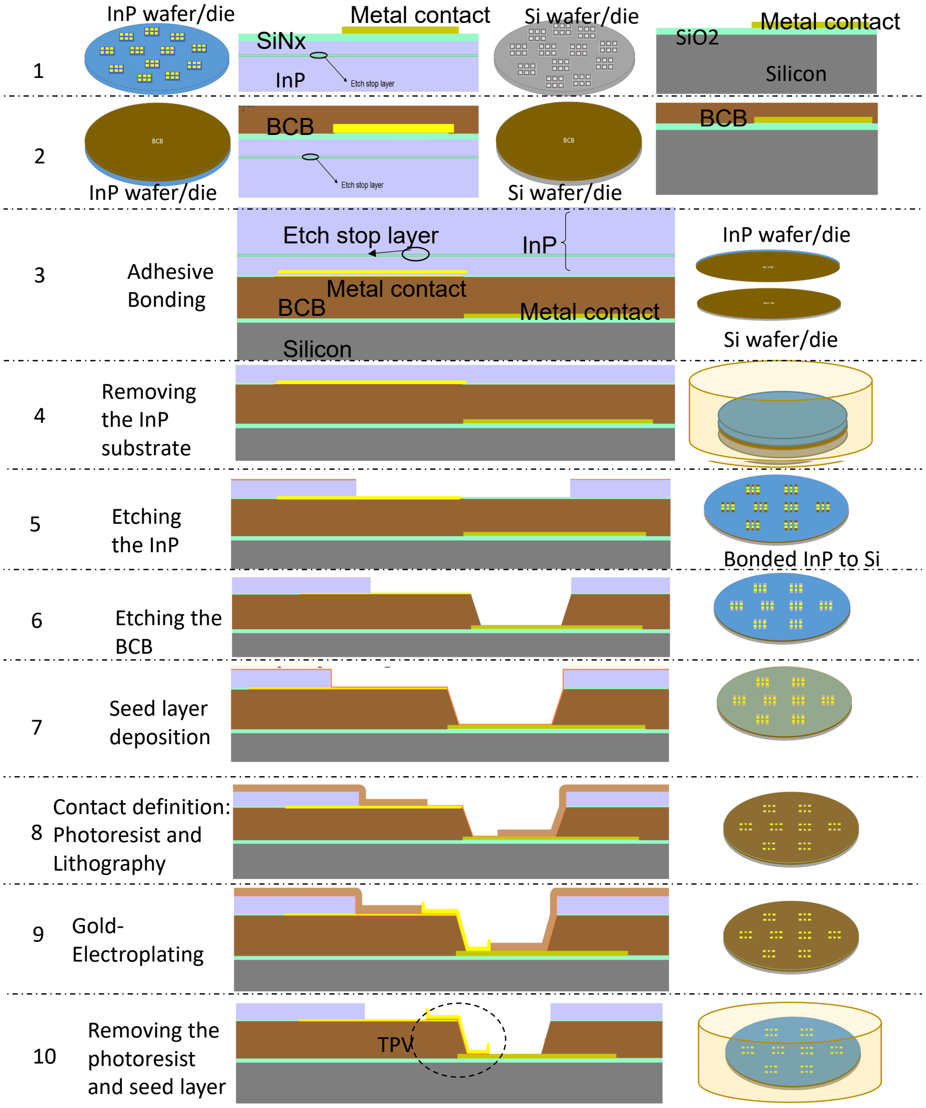


Figure 5.1: General process steps for making metal connection between silicon to InP die/wafer

The experimental samples of this chapter are listed in appendix A.

5.3.1 Masking and etching

One of the challenging steps in the process of making TPVs is to etch the thick polymer layer (step 6 in figure 5.1). In this part, we study masking techniques for etching the BCB polymer. For achieving a good planarization, the thickness of the BCB bonding layer has to be more than 1.5 times the topology height. Depending on the typologies of the silicon and InP wafers, its thickness can be between 4 and 20 μm. To develop a technique for etching BCB, samples of cured polymer were prepared on top of three 2 inch silicon wafers. By Plasma-enhanced chemical vapor deposition (PECVD) thin 50 nm SiO_2 layers are deposited before spinning 27 μm thick layers of BCB, which were then cured at 270 °C for two hours. We tried to find how deep and smooth we could etch the BCB with three different hard mask techniques. A mask with a range of openings from 116 to 1250 μm and a range of pitches with a minimum opening separation of 25 μm was used. For pattering the BCB, the hard mask was created with three different methods is performed with the following three approaches:

1. Silicon nitride mask: A 360 nm silicon nitride layer was deposited on top of the BCB with PECVD. A pattern of holes was etched on the silicon nitride layer by photolithography and plasma etching using combining CHF_4 (50 sccm) and oxygen (5 sccm) with a power of 100 W during 4 minutes.
2. Chromium mask: 100 nm of chromium (Cr) was evaporated on top of the BCB and patterning is performed with litho. Unwanted material is removed by lift-off.
3. AZ 9260 photoresist: 10 μm of the thick positive photoresist was used as a mask and patterned during a lithography step. Post baking of the photoresist for 20 minutes at 110 °C resulted in sloping sidewalls in the photoresist, and these slopes are subsequently transferred from the photoresist to the BCB.

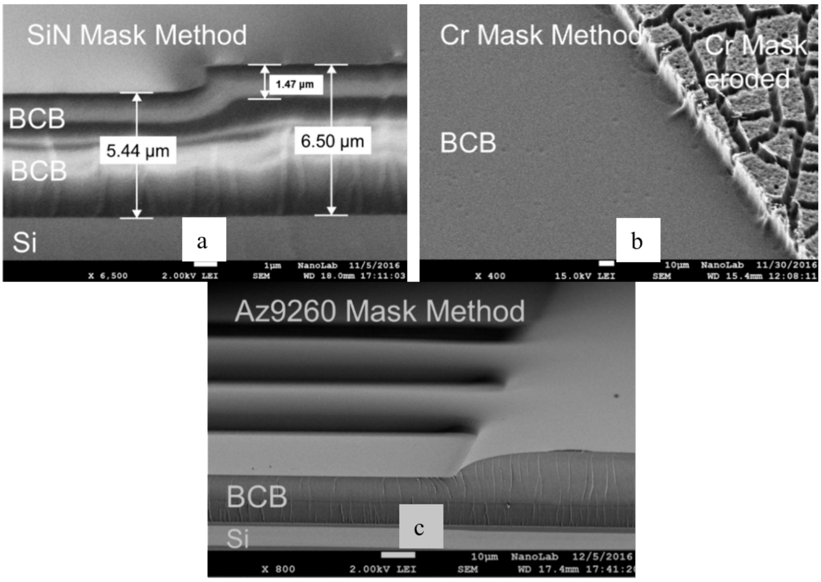


Figure 5.2: SEM images for three masking methods: a) Silicon nitride mask, b) chromium mask and c) AZ 9260 photoresist

Via holes are created with reactive ion etching with the gas combination of SF_6 (6 sccm) and O_2 (40 sccm) and forward power of 200 W to achieve a high etch rate of 0.6 μm/min. We continued etching until the mask was consumed completely, and the step height of the etched BCB is measured (with a Tencor Profilometer) to check how deep BCB can be etched with each mask. Scanning electron microscope images of the results for the various masking techniques are shown in figure 5.2. The silicon nitride mask is completely consumed for 1.2 μm BCB, as shown in figure 5.2 (a). Figure 5.2 2(b) shows that the chromium mask was consumed after etching 21 μm of BCB, showing a higher selectivity of chromium against oxygen and SF_6 plasmas, but there are cracks in the hard mask. The resilience of the AZ9260 resist was sufficient to allow etching of up to 8 μm of BCB (step height was measured after 20 minutes of etching) with a single layer of resist mask (figure 5.2 (c)). For etching higher BCB thicknesses, multiple layers of AZ9260 resist can be used. The sloped sidewalls obtained with the AZ9260 mask would facilitate full coverage in the seed layer for plating when using the evaporation technique for metal deposition, and AZ9260 resist was accordingly chosen for the subsequent work of making sloped sidewall through polymer vias.

5.3.2 Metallization

Three samples with 4, 7, and 8 μm thickness of cured BCB are prepared on quarters of 2 silicon wafers with a 50 nm SiO_2 layer to enhance adhesion. AZ9260 was used to define mask patterns for etching the BCB, resulting in sloping side walls. A thin seed layer of Ti/Au (50/100 nm) was then evaporated on the samples. In order to maximize coverage on the sidewalls, the carrier was angled by 45 °C and rotated during deposition. The same mask as the via opening mask mask is used for vias. For that, the via opening mask was offset by 50 μm to define vias on the sidewall. This results in the creation of metal tracks, including vias in the end part. AZ4533 photoresist was used to define the areas for electro-plating. The gold plating bath had 30 °C. After plating, the resist was removed with acetone, and the seed layer is etched with a potassium cyanide (KCN) solution.

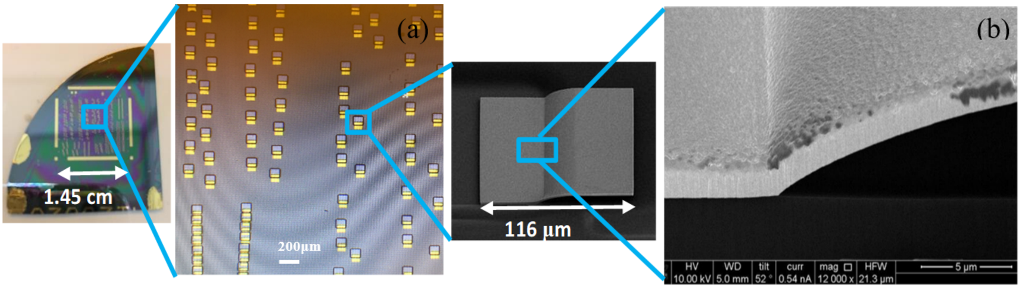


Figure 5.3: Metallization of 116×116 μm^2 through polymer vias on a quarter of a two-inch silicon wafer

Referring to figure 5.3, the closest vias are 25 μm apart with examples at 116 μm shown in the figure. This is a route to high-density integration. The cross-section image taken after focused ion beam (FIB) etching shows a break-free connection. A constant metal thickness of 1.2 μm is observed in the image over the full slope. There is variation in plating thickness varies across the samples from 0.7 to 3.7 microns which is attributable to different numbers of potential cycles used per sample in the plating bath.

5.3.3 Mechanical reliability

Metal electroplating of the TPVs of this work is done at 30 °C. Therefore the gold metal of the TPVs is mechanically relaxed at this temperature. The significant mismatch in the coefficients of thermal expansion (CTE) of gold (13 ppm) [103], and BCB (42 ppm/C) [104] can causes stresses in the gold when changing the temperature to lower or higher than 30. To see the mechanical reliability of the vias, mechanical stress of the gold TPVs is simulated with COMSOL multi-physics software [105] in a temperature range of -50 °C to 300 °C.

Yield strength is the material property defined as the stress at which a material begins to deform plastically. Prior to the yield strength, the material will deform elastically and will return to its original shape when the applied stress is removed [106]. Once the yield strength is passed, some fraction of the deformation will be permanent, and non-reversible [107]. The yield strength of the bulk gold is 205 MPa, but it can be higher for thin films. For instance, gold tracks with a width of 2.5 to 20 μm and a thickness of 0.3 μm to 0.5 μm can have yield strength of 250 to 300 MPa [108].

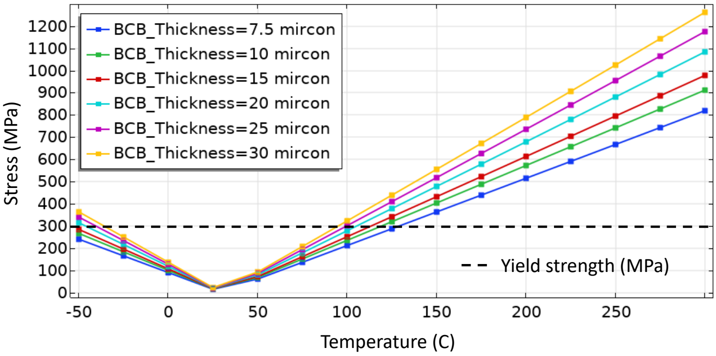
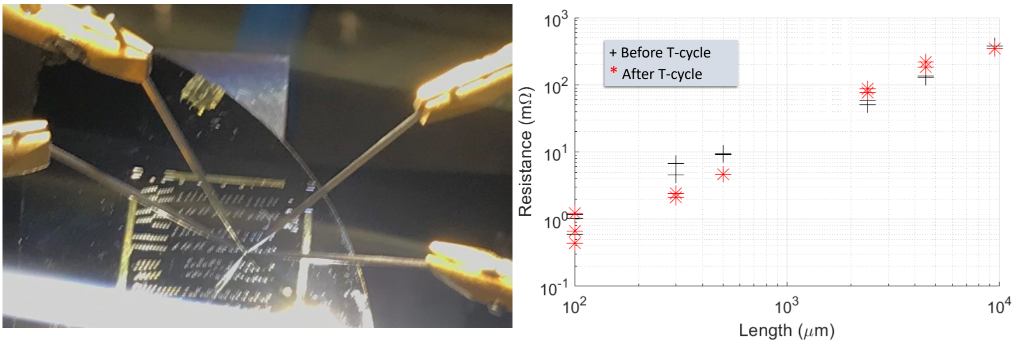


Figure 5.4: Mechanical stress of the gold TPVs vs. temperature for different BCB thicknesses.

By using the MEMS module of the COMSOL multi-physics simulation tool [105] the mechanical stress of the sloped sidewall TPVs, which connects a metal pad on the InP to a metal pad on the silicon, is simulated. The mechanical and thermal parameters of BCB, gold, InP and silicon are from references [104], [103], [109] and [110] respectively. The thickness of the gold TPVs is 2 μm, and the thickness of the BCB is changed from 7.5 to 30 μm. The plot of the maximum stress in the gold vias vs. temperature for a range of BCB thicknesses (7.5 μm to 30 μm) is depicted in figure 5.4. In this figure, at 30 °C (electroplating temperature), the stress of the gold via is zero, while with increasing/decreasing temperature from this point, stress increases. The stress of the TPV with BCB thickness of 7.5 μm reaches 300 MPa at the temperature of 125 °C and below -50 °Cwhile 15 μm BCB reaches this stress level at 100 and -50 °C.

To check the reliability of the fabricated sloped sidewall TPVs, DC measurements before and after the temperature cycle have been done. Since the standard operating temperature of the telecommunication systems is -40 °C to 85 °C, 400 cycles with 15 min dwell time are made for this temperature range.

Figure 5.5 shows a) TPVs under four probe measurement and b) four-probe resistance measurement for different lengths of metal tracks, with vias before and after tempera-



(a) Four probe measurement setup

(b) Resistance

Figure 5.5: a) TPVs under four probe measurement. b) Four-probe resistance measurement for different lengths of metal tracks, with vias before and after temperature cycle

ture cycle [3]. Figure 5.5b shows the resistance as measured versus separation between the probes before and after the T-cycling. In this figure, the resistance of the metal tracks, including one TPV in each track before and after the T-cycling, is within the same range, proving that the metal vias are not broken, thus the mechanical reliability of the created TPVs in the range of T-cycling. Since, in the four-probe resistance measurement, probes are manually placed on the sample, the probing resolutions can explain the observed difference in the resistances.

In this part, the DC measurement and the mechanical reliability of the vias is studied. However, to see the high-speed performance of these TPVs, radio frequency (RF) characteristics of these vias has to be defined.

5.3.4 Radio frequency characteristics

In this section, we first, use a fast 3D EM simulation (CST microwave studio [36]) to simulate the scattering parameters of the through polymer vias with slope sidewalls.

Figure 5.6 shows a) the 3D perspective view of the simulated sloped sidewall TPVs that connect GSG pads on the InP to the counterpart GSG pads on the silicon and b) electrical scattering parameters (S21 and S11) of TPVs. Width and gap sizes are in μm. In figure 5.6b, three gold sloped sidewall TPVs connect three ground-signal-ground (GSG) aluminum pads on the silicon to the gold GSG pads on the InP. Since in figure 5.6 InP is flipped to the silicon, metal patterns on the InP face down towards the silicon. There is a 50 nm silicon oxide layer and silicon nitride on the silicon and the InP respectively. The BCB thickness of this simulation is 20 μm. The width of the simulated gold TPVs is 2 μm. Scattering parameter simulation is with 50 Ω ports at the two GSG pads (aluminum and gold pads in figure 5.6a). In figure 5.6, the simulated electrical scattering parameters of the eight TPVs (1-8) with different gap and width are depicted. Figure 5.6b shows the simulated scattering electrical S11 and S21 of the TPVs. In figure 5.6b, the electrical S21 of the TPVs in the range of up to 100 GHz is higher than -0.4 dB, and electrical reflection is lower than -10 dB. TPV3 with 25 μm width and 20 μm gap has the maximum electrical

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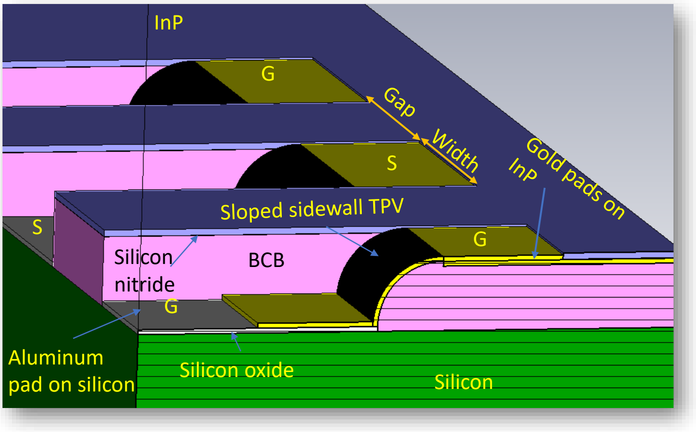
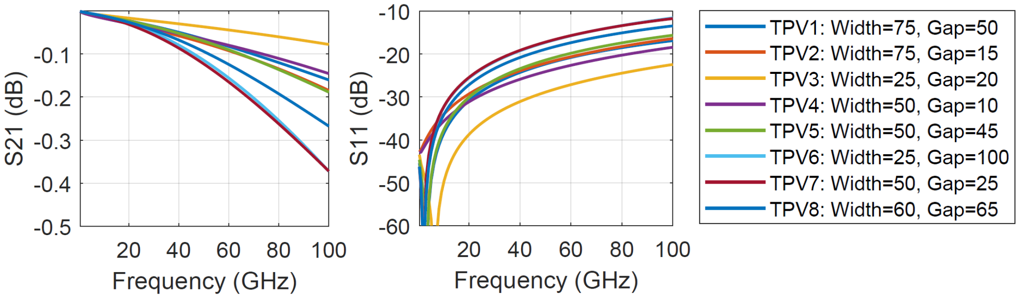
[3] The temperature cycling experiment is done by Tim Durrant from Effect Photonics



(a) The 3D perspective view of the simulated TPVs



(b) Electrical S21 and S11)

Figure 5.6: a) a) the 3D perspective view of the simulated sloped sidewall TPVs that connect GSG gold pads on the InP to the counterpart aluminum GSG pads on the silicon and b) electrical scattering parameters (S21 and S11) of TPVs. Width and gap sizes are in μm.

transmission (S21) and minimum electrical reflection (S11) while TPV6 (Width= 25 μm, Gap=100 μm) and TPV7 (Width= 50 μm, Gap=25 μm) is vise versa. Therefore, for connecting the high-speed 50 Ω devices on the InP to silicon, simulations show that TPV3 with 25 μm width and 20 μm gap is a good candidate with less than 0.1 dB loss at 100 GHz.

5.3.5 RF measurement

For experimentally assessing the RF performance of the TPVs, a cell that includes metal tracks and pads on both the silicon and InP wafers is co-designed. This is transferred to masks for making the TPVs. Figure 5.7 shows the co-designed cell with the metal patterns for RF measurement of TPVs. The co-designed cell contains three parts: co-designed InP cell to be fabricated by HHI, co-designed silicon cell [4] to be fabricated in the BiCMOS [5] [111] and masks for TPVs. The co-designed cell showed in figure 5.7 includes input GSG

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[4] Co-designed silicon structures are designed by Xi Zhang

[5] NXP fabricated the BiCMOS silicon wafer

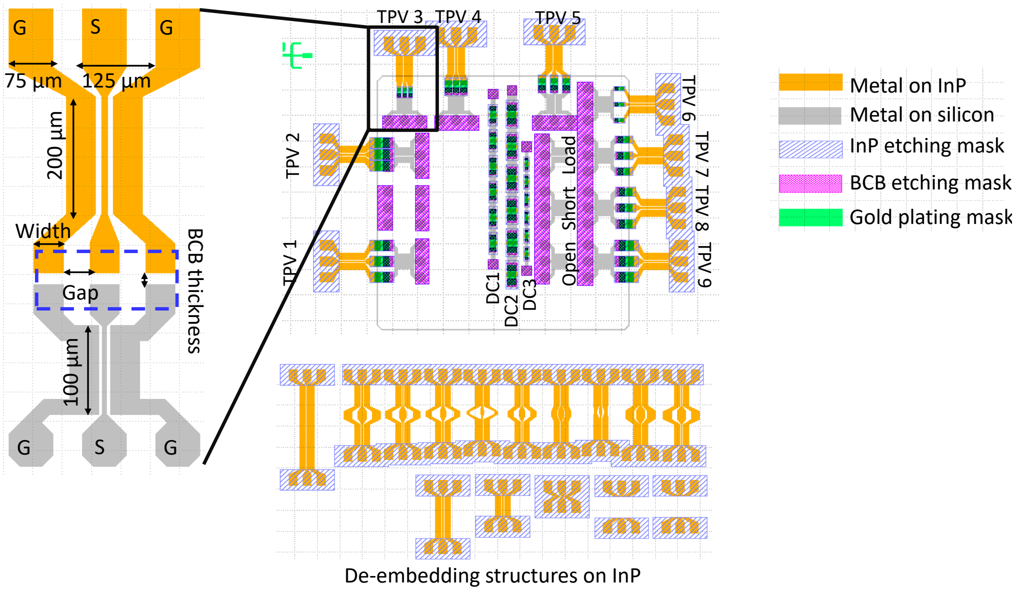


Figure 5.7: Figure of co-design cell including the metal patterns on InP and silicon for RF measurement of nine TPVs (TPV1-9), RF de-embedding (open, short, load) structures on silicon, three daisy-chains (DC1-3) for DC characterizations, masks for creating the TPVs, and the RF de-embedding structures on the InP

pads and tapers for probing, 100 μm and 200 μm CPW transmission lines on silicon and InP, respectively, and output GSG pads and taper for creation of TPVs. GSG probing pads on silicon and InP have 75 μm width and 125 μm pitch. TPV1-9 in figure 5.7 are designed for RF measurement of the TPVs. TPV1 to 8 have different widths and gaps (equal to the TPVs in figure 5.6a) for the TPVs while TPV9 has similar dimensions as TPV1. There are structures (open, short, and 50 Ω load) for de-embedding the RF scattering parameters of the metal patterns on the silicon. Three daisy chain structures in the center of the cell in figure 5.7 are co-designed for measuring the DC characteristics of the metal connections with different widths of 25, 50, and 75 μm.

In the left side of the figure 5.7, the zoomed look of the metal patterns on InP and silicon designed for RF measurement of the TPVs is depicted. TPVs will be processed inside the dashed blue line. Metal patterns on both silicon and InP include GSG pads with 75 μm width and 125 μm pitch, transmission lines, and tapers to connect the TPV GSG pads to the transmission lines. Since the TPVs have 45° sloped sidewalls, a distance equal to the thickness of the BCB between metal patterns on InP and silicon is considered.

In figure 5.7 there are structures for de-embedding the RF scattering parameters of the metals on InP. Since 50 Ω load is not available in the InP platform, for de-embedding the metals on InP, thru-reflect-line (TRL) method [112] is used instead. De-embedding structures on InP include high-speed transmission lines with 10 μm width and 10 μm gap. These transmission lines have different lengths needed for the TRL de-embeding. Tapers connect the both ends of these transmission line to the measurement GSG pads. In the center of some of the transmission lines, there are tapers that connect the transmission lines to the GSG pads with gaps and widths equal to the TPV1-8.

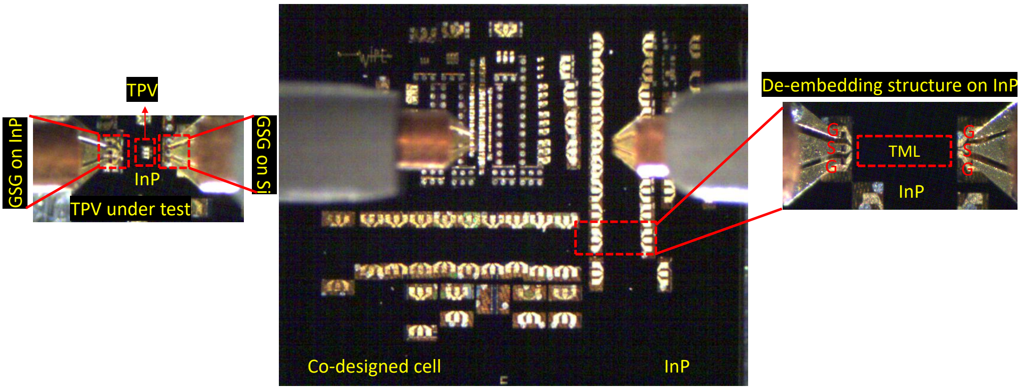
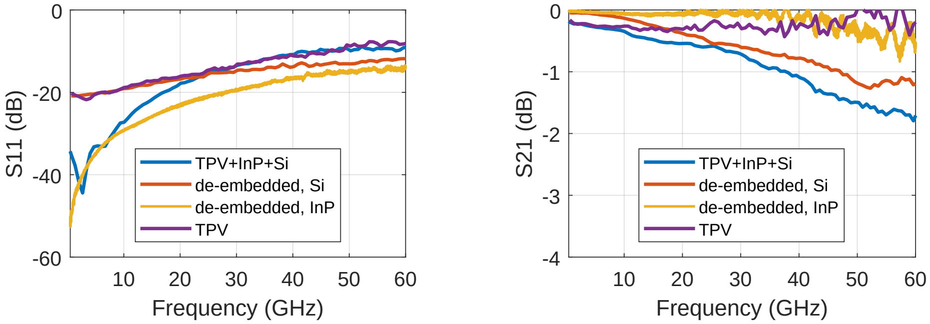


Figure 5.8: Co-designed fabricated cell under test including the TPVs and de-embedding structures on both Si and InP

Figure 5.8 depicts the co-designed fabricated[6] cell under test, including the TPVs and de-embedding structures on both Si and InP. Two GSG probes with 125 µm pitches are used for probing the input pads and output pads of the TPV. A vector network analyzer (VNA) is used for 50 Ω RF measurement of the TPVs and de-embedding structures on InP and silicon. An input signal from port one of the VNA is applied to the GSG pads via a GSG probe and a second GSG probe takes the transmitted electrical signal from the GSG pads back to the VNA.



(a) Electrical S11

(b) Electrical S21

Figure 5.9: Measurement data of the electrical scattering parameter a) S11 and b) S21 of the transmission line on the InP that are connected to the transmission lines on silicon by TPVs , de-embedding structures on Si and InP, and a TPV (Width=75 μm, Gap=50 μm)

Figure 5.9 shows the measurement data of the electrical scattering parameter a) S11 and b) S21 of the transmission line on the InP that are connected to the transmission lines on silicon by TPVs , de-embedding structures on silicon and InP, and a TPV (Width=75 μm,

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[6] Bonding process of the InP wafer to the silicon wafer is done by Marc Spiegelberg [113]

Gap=50 μm). In the bonding process, a misalignment of 40 μm between the InP wafer and the silicon wafer occurred. In order to compensate for this misalignment, an additional 40 μm long gold plated transmission line was used to connect the TPV pads on the InP wafer and the circuit. The misalignment caused open or short circuit in some of the TPVs. Therefore we couldn't measure the scattering parameters of those CPW TPVs. Also, while probing, some of them have been lifted off. Because of these issues, only the TPV with 75 μm width and 50 μm gap is measured.

In figure 5.9b and figure 5.9a, electrical transmission (S21) and reflection (S11) in of the measured transmission line on InP, which is connected by a TPV of 75 μm width and 125 μm pitch to the transmission line on silicon, is depicted in blue. This blue line has 1.8 dB loss and -10 dB reflection at 67 GHz.

The blue curve in figure 5.9 includes TPVs and transmission lines on InP and silicon. To get the scattering parameters of just the TPV, both the transmission lines on the InP and silicon have to be extracted from the measurement data. For extracting the transmission lines on the silicon, short-open-load method [114] is used and thru-reflect-line (TRL) method [112] is used for de-embedding the transmission line on the InP. S21 and S11 of the de-embedded transmission lines on InP and silicon are depicted in figure 5.9. S21 of the de-embedded transmission line on silicon is -1.2 dB at 60 GHz, and the de-embedded transmission line on InP has about 0.5 dB loss at 60 GHz. Reflection parameters of the de-embedded transmission line on silicon and InP are -15 dB and -13 dB, respectively.

The extracted de-embedded scattering parameters of the transmission lines on the silicon and InP are then used for extracting the RF scattering parameters of the TPV by using the de-embedding technique for interconnects described in reference [115]. In figure 5.9 we see that de-embedded TPV has less than 0.4 dB loss up to the 60 GHz frequency range and has a reflection of equal or less than -10 dB.

These through polymer vias show very high speed RF performance, however the 45° sloped sidewall, increases the footprint of these vias by $2 \times cos(45) \times$BCB-thickness.

5.4 Method for steep sidewall TPVs

To have a process suitable for TPVs with a small footprint, in this section, a method for creating vias with steep sidewalls is introduced. Figure 5.10 shows the experimental objective of developing a process for steep sidewall TPVs. Sloped sidewall TPVs have a wide footprint, while steep sidewall TPVs can have a smaller footprint. These larger dimensions

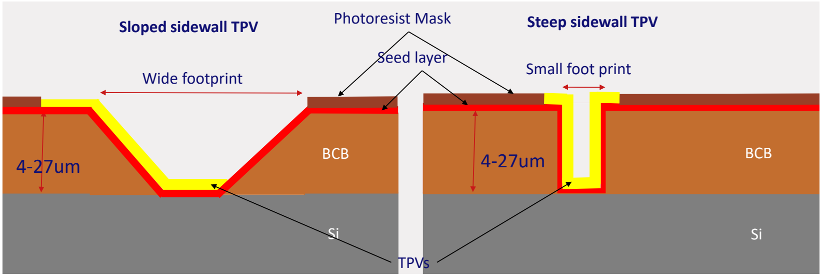

Figure 5.10: Experimental objective of developing a process for steep sidewall TPVs. Sloped sidewall TPVs have wide footprint while steep sidewall TPVs can have smaller footprint

increase the footprint and, by inducing more parasitic, reduce the high-speed performance of the TPVs.

To have vias with steep sidewalls, one of the main challenges is how to cover the sidewalls with a conformal seed layer. In the silicon industry, atomic layer deposition is widely used for creating through-silicon vias [116]. Precise thickness control and conformality of ALD enables steep sidewall vias with a high aspect ratio.

Ruthenium is one of the most attractive noble metals with respect to cost and physical properties. Ruthenium has low bulk resistivity of 7.5 $\mu\Omega$cm. In the silicon platform, copper-plated TSVs on Ruthenium ALD with a high aspect ratio (2 μm width and 30 μm depth) have been reported [117]. In this work, we study how to use the Ru-ALD seed layer for creating gold-plated TPVs.

To develop the process for making TPVs with steep sidewalls, first the compatibility of the Ru ALD with the materials are experimentally checked [7]. Since the ALD seed layer has to cover the whole InP surface, the etched BCB polymer, and gold metal on the InP, we first prepared separate samples of these materials. Because pads of the NXP BiCMOS platform are aluminum, we also prepared a sample with evaporated aluminum. Atomic layer deposition of ruthenium is done as described in [118]. Ru films are deposited at 225 °C. X-ray photoelectron spectroscopy proved the deposition of Ru on all of the mentioned materials. Ru films have a low oxygen impurity level and resistivity of 26 ± 2 $\mu\Omega$cm.

For making steep sidewall TPVs with ruthenium seed-layer, three experiments have been done. We first experimentally checked the sidewall coverage of the etched BCB polymer and the capability of plating the Ruthenium seed layer with gold. 5 μm BCB was spun on a bare silicon wafer covered with 50 nm of silicon oxide. For etching the BCB with steep sidewall, simply the InP and gold patterns are used and as a result the process steps for creating the steep-sidewall TPVs is reduced. Then a 32 nm ALD Ruthenium seed layer was deposited on the whole wafer. The sample was in ambient for three weeks. After that, contact definition is done with photo-resist, and gold is plated on the Ruthenium seed layer.

In figure 5.11. a, cross-section of the TPVs of the first experiment is depicted on the left side of. The right side of this figure 5.11. a shows the microscopic picture of the metal tracks, including gold-plated TPVs. This shows a complete detachment of the plated gold. The reason of this detachment is that, in the electro-plating process, nucleation and growth kinetics are often strongly dependent on surface chemistry. Ruthenium exhibits a thin oxide layer under ambient conditions [119]. In the silicon platform, when Ru is used for copper-plating, the surface oxide layer on Ru, although extremely thin, is reported decreasing the ability of Cu to wet the Ru surface during electrodeposition [120].

To reduce the Ruthenium oxide in the second and third experiments, the delay between the ALD and plating is reduced to 3 hours and 1 hour, respectively. In the third experiment, the whole surface of the ruthenium seed-layer is encapsulated by 100 nm of the evaporated gold to enhance the plating quality. Figure 5.11.b , c shows the cross-section and microscopic pictures of the TPVs when b) Ru-ALD seed layer is plated after three hours delay and c) when Ru-ALD after an hour is covered by 100 nm evaporated gold and then plated. Gold has been plated on both experiments. In experiment three (figure 5.11. c), the encapsulated gold was wet etched with potassium cyanide (KCN) for 3.5 minutes. Then, in both experiments 2,3 (figure 5.11. b, c), Ru seed-layer was removed with diluted sodium hypochlorite for 3.5 minutes. On the right side of figure 5.11.b, c, the successfully

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[7] The ruthenium ALD experiments were done by Martijn F.J. Vos from the PMP group

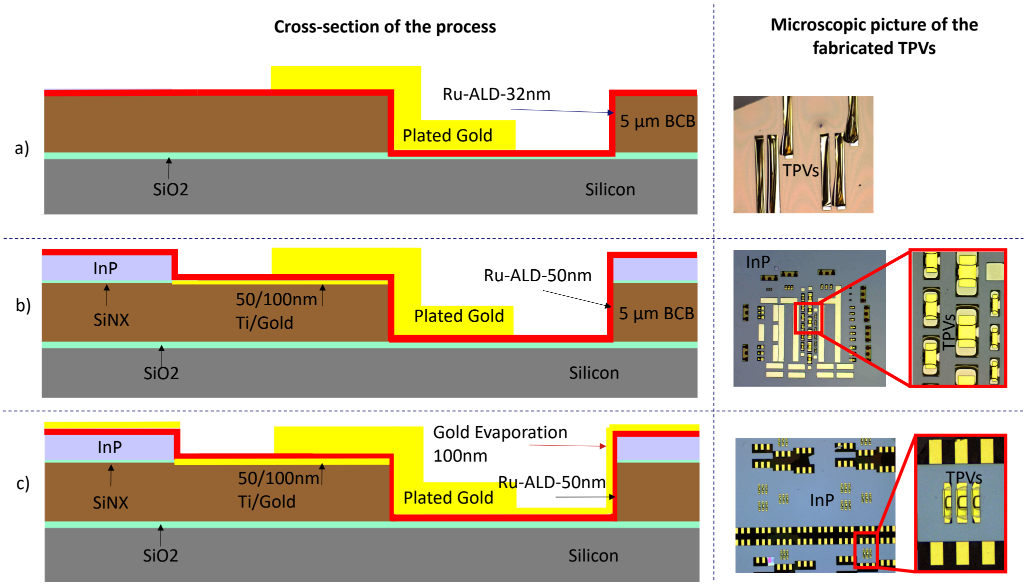


Figure 5.11: Cross-section and microscopic pictures of the TPVs when a) Ru-ALD seed-layer is plated after three weeks in ambient, b) Ru-ALD seed layer is plated after three hours delay and c) when Ru-ALD seed-layer is covered by 100 nm evaporated gold after an hour delay and then is plated

fabricated TPVs without detachment is depicted. The three experiments for creation of the steep sidewall TPVs are summarized in table 5.1.

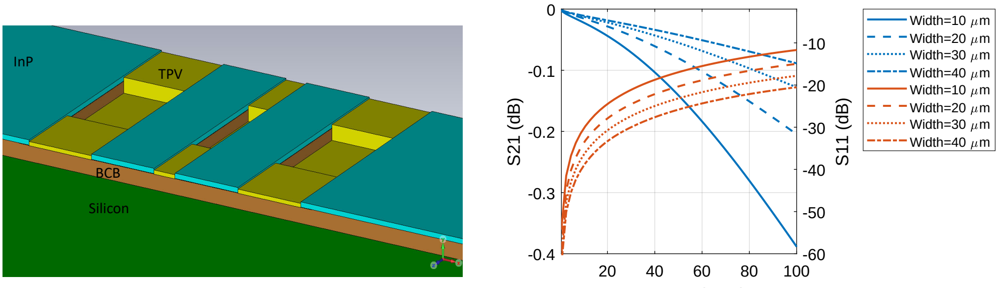
Experiment	**1**	**2**	**3**
Preparation of etched BCB	4 μm BCB on Si	1 μm InP bonded to Si by 5 μm BCB	1 μm InP bonded to Si by 5 μm BCB
ALD of Ruthenium	32 nm	50 nm	50 nm
	3 weeks in ambient	Delay of about 3 hours	Delay of about one hour and encapsulation with Au
Lithography	AZ3345 photo-resist	AZ3345 photo-resist	AZ3345 photo-resist
Gold plating	NB Semiplate solution, Au 100 bath with 9.5 pH at T=30 °C	NB Semiplate solution, Au 100 bath with 9.5 pH at T=30 °C	NB Semiplate solution, Au 100 bath with 9.5 pH at T=30 °C
Seed-layer removal	Not done	Wet etched	Wet etched
Top view inspection	Complete detachment of Au	No detachment	No detachment

Table 5.1: Summary of experiment

By using Ru seed-layer, a method for creating steep-side wall TPVs without detachment is introduced. However for high-speed application of these vias, the radio frequency characteristics of these vias has to be studied.

5.4.1 Radio frequency characteristics

RF scattering parameters of the steep sidewall TPVs are determined with a fast 3D simulation. Figure 5.12a shows the perspective of the steep-sidewall TPVs with BCB thickness of 5 μm in the CST 3D simulation tool [36]. For this simulation, semi-insulating silicon and non-intentionally doped InP correspond with the cross-sectional view of TPVs in figure 5.11.b is used. In figure 5.12b electrical scattering parameters of the TPVs simulated with two 50 Ω RF ports are shown. In this simulation, signal line width is swept from 10 to 40 μm. Ground width is 40 μm and gap between ground and signal is 10 μm. In figure 5.12b, increasing the signal width reduces the electrical loss at 100 GHz frequency from 0.4 to 0.1 dB, because by increasing the width of the gold layer, electrical loss in this layer reduces. Also, a 40 μm width has a better impedance match with 50 Ω ports. The characteristic impedance of the transmission lines with signal width of 10 μm is about 90 Ω, while when the width is 40 μm this impedance reduces to about 60 Ω. Therefore, as in figure 5.12b, increasing the width from 10 to 40 μm reduces the electrical reflection (S11) from -11 dB to -20 dB.



(a) Perspective picture

(b) Scattering parameters

Figure 5.12: a) Perspective picture and b) electrical scattering parameters of the simulated steep sidewall TPVs with different signal width in CST

On the realized structures, InP with metal patterns is bonded by 5 μm BCB to a bare semi-insulating silicon wafer. The transmission line on the InP with and without TPVs are connected (with two tapers) to two GSG pads designed for RF measurement. Two GSG probes with 100 μm pitches are used for probing the input and output GSG pads on the InP. A VNA is used for 50 Ω RF measurement of the TPVs and de-embedding structures on InP. An input signal from the VNA is applied to the GSG pads via a GSG probe and a second GSG probe takes the transmitted electrical signal from the GSG pads to port 2 of the VNA.

To extract the scattering parameters of the two series TPVs that connected the TML on the InP to silicon and back to the InP, the scattering parameters of the two TMLs on the two sides of these series TPVs is de-embedded. To extract the transmission lines on InP, the thru-reflect-line (TRL) de-embedding method [112] is used. Then the de-embedding technique for interconnects described in reference [115] is used for de-embedding the scattering parameters from the measurement data.

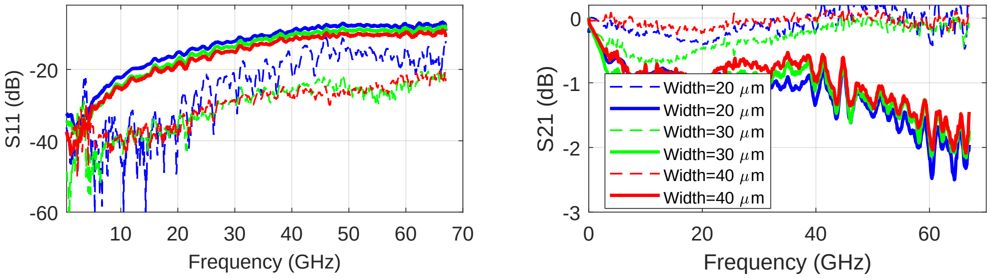


Figure 5.13: Scattering parameters of measured (solid lines) and de-embedded (dashed lines) TPVs with the width of 20 to 40 μm.

Figure 5.13 depicts scattering parameters of the de-embedded TPVs with the width of 20 to 40 μm. Ground width is 40 μm and gap is 10 μm. A TPV with 10 μm signal width was also fabricated. However, because of the misalignment of the plating mask for creating the TPVs, the ground and signal parts of the TPV was short circuited. Except for the TPVs with 10 μm width, in figure 5.13 we show that all of the other TPVs have de-embedded S11 of less than -8 dB and S21 of -0.1 to -0.6 dB.

5.5 Summary

Since parasitics reduce the bandwidth of the co-packaged devices and close co-integration is important for high-speed applications, therefore in this section, we focused on two fabrication methods for short wafer-scale metal connections can be used for 3D integration of the InP and silicon wafers.

Using the evaporated seed layer, sloped sidewall TPVs are created. The electrical performance is assessed from scattering parameters of vias. These short vias show a very high-speed performance with less than 0.4 dB electrical loss in the measurement range up to 67 GHz. Furthermore, to check the strength of these vias, the mechanical reliability of vias in the temperature cycle's presence is tested. Four-probe measurement is performed for metal tracks, with vias. The resistance of the metal tracks, including TPVs before and after the T-cycle, is within the same range (figure 5.5), proving the mechanical reliability of the created TPVs in the range of T-cycling.

For smaller, more compact structures with lower parasitic, atomic layer deposition is used to create a seed layer for the steep sidewall through polymer vias. A series connection of a couple of high-density TPVs with 40 and 10 μm signal width and gap, respectively, show high-speed performance with 0.2 dB loss over the 67 GHz making them promising candidates for wafer scale co-integration of high-speed photonic-electronic devices.

Chapter 6

Co-integration of the photonic and electronic circuits

6.1 Abstract

The scope of this chapter is the co-integration of the high-speed Mach-Zehnder modulator (MZM) photonic integrated circuits to the driver electronic integrated circuits.

The effect of the interconnects between the electronic to photonic integrated circuits is discussed. Using the co-design environment, the modulator's high-speed performance, interconnected by the high-speed through polymer vias, was theoretically compared to the state of art flip-chip bonding and wire bonding interconnect techniques. This comparison confirms that the close co-integration of the electronic to photonic circuits enhances high-speed performance. Moreover, co-design photonic cells for comparison of these techniques have been designed.

Because high-speed MZMs have to be terminated to a proper termination circuit, the effect of the termination capacitance is studied. Then the measurement data of an on-chip termination (OCT) fabricated in a generic InP platform with semi-insulating (SI) substrate is combined with the spatially resolved circuit model of the HCPW-MZM EO-frequency response of the MZM is simulated.

Moreover, To increase the modulators' co-design flexibility to the electrical interfaces, a high-density and high-speed tapered-CPS-MZM with different input and output impedances is introduced and experimentally assessed.

6.2 Introduction

At the heart of the information processing and transport technologies, optical transceivers convert data from the electrical to the optical domain and are made from photonic and electronic integrated circuits. Electronic integrated circuits (EICs) and photonic integrated circuits (PICs) are usually made in different technology and are packaged afterward to form a module. In packaging the high-speed integrated circuits, besides the protection of separately assembled devices, electrical performance optimization plays a vital role. In the range of radio-frequency (RF), minimizing the electrical parasitic of the package is crucial [83]. This is now becoming a major performance bottleneck of the high-speed optical transceivers.

In the optical transceivers, to increase the transmission speed,the interface between the EICs and PICs has to be re-invented. Wire-bonding, flip-chip bonding, and 3D bonding are the three state-of-the-art interconnect technologies for high-speed electrical connection of the PICs and EICs.

Wire bonding is still considered the most flexible and cost-effective method of making interconnects in microsystem packaging [24,25]. In this technique, a wire or ribbon connects the metal pad of an IC to the counterpart pad on the other IC. The diameter of the wire bonds for high-speed applications can as thin as 15 μm, and it can also be several hundred micrometers for high-powered applications. Wire bonding is widely used in the silicon industry for the high-speed electrical connection of the EICs, also used for electrical connection of the high-speed PICs and EICs [26].

Flip-chip interconnect technology is another standard process to connect ICs to the substrate. This is a face down assembly technique originally developed by IBM [121]. Stud bumping is a modified form of the flip-chip process. It is suitable for the single-chip to substrate bonding [122], where Au, Ag, Pt, Pd, and Cu can be used as materials. One of the advantages of flip-chip assembly is its self-alignment function. As a result, flip-chip provides excellent performance and allows a cost-effective interconnect technique for dice with high input/output counts [25]. Flip-chip interconnect technology is used in both electronic and photonic industries [122].

Demands for increased performance, smaller size, reduced power, and reduced cost cannot be met with conventional wire-bond and flip-chip bonding technologies. There are limitations in interconnect density, thermal management, bandwidth, and signal integrity that cannot be addressed with those conventional technologies [25]. Therefore, 3-D bonding such as through silicon and polymer via approaches can provide the shortest and most plentiful vertical connections.

In this work, the effect of the three wire-bond, stud-bump, and through polymer vias (TPV) interconnect technologies on the two types of high-speed MZMs in the generic InP technology is studied. To accomplish this study, the focus of this chapter is divided into the following order.

In section 6.3, the electrical scattering parameters of the stud-bump and TPV interconnects are simulated and compared with the wire-bond interconnect available in the advanced design system (ADS) simulation software. Then, the co-design environment achieved by the spatially resolved circuit model introduced in chapter 3 of this thesis is used to study the effect of the interconnects on the small and large signal responses of high-speed hybrid coplanar waveguide (HCPW) and coplanar stripline (CPS) modulators in subsections 6.3.1 and 6.3.1, respectively. Then, we show that wire-bond interconnects severely compromises the EO-bandwidth and optical eye quality of both CPW and CPS modulators while stud-bump and impact the responses of those modulators are small.

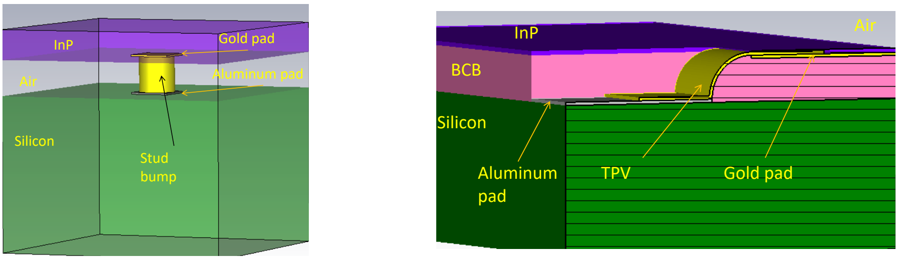
For achieving a high-speed EO-bandwidth, the traveling wave electrode of the high-speed MZMs has to be terminated to a proper termination circuit. Small and large-signal frequency responses of the high-speed HCPW and CPS-MZMs in section 6.3 are simulated by a perfect termination with infinite capacitance. However, the termination capacitance is not infinite in practice. In section 6.4 the impact of the termination capacitance on the broadband electro-optical frequency response of the HCPW-MZM is studied. The measurement data of an on-chip termination (OCT) fabricated in a generic InP platform with semi-insulating (SI) substrate is combined with the spatially resolved circuit model of the HCPW-MZM. Then the electro-optical frequency response of the HCPW-MZM terminated with the OCT is simulated.

To compare the effect of state-of-the-art interconnect technologies on the large signal response of the MZM, in section 6.5 a single PIC including the laser sources and high-speed CPS modulators is designed. Furthermore, the co-designed single PIC is compatible with wire-bond and stud bump interconnections to BiCMOS driver and termination EICs enables the comparison between these two technologies' effects on the optical eye diagram. The co-designed PICs are taped out on a dedicated semi-insulating process. The co-designed PICs are additionally taped out on a multi-project wafer process with an n-doped substrate. The n-doped substrate PIC was available for interconnection to the BiCMOS driver and terminations.

Electronic systems are commonly made with 50 Ω impedance. To minimize the reflections at the interface between the electrical high-speed modulators and drivers, the modulators are also usually designed with 50 Ω characteristic impedance. For the co-design approach and increasing the flexibility of the modulator's impedance at the input and termination interfaces, in section 6.6 a tapered-CPS (TCPS) Mach-Zehnder modulator with different input and output mask parameters is introduced. By tapering the waveguide width, electrode width, and electrode gaps from the front to the end side of the phase modulation section of the CPS modulator, in the TCPS-MZMs different impedances at the two sides are realized. Then small-signal electrical and electro-optical responses of the TCPS modulators are assessed.

6.3 Interconnect effect on the high-speed modulators

This section focuses on the effect of the three wire-bond, stud-bump and through polymer vias (TPV) interconnect technologies on the small and large signal responses of the high-speed CPS and HCPW Mach-Zehnder modulators. To accomplish this, first, the electrical scattering parameters of single stud-bump and TPV interconnects are simulated.

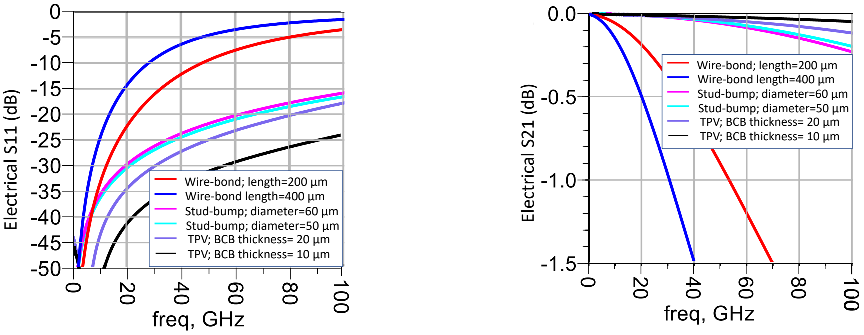


(a) Stud bump

(b) TPV

Figure 6.1: 3D-perspective of the simulated a) stud-bump and b) sloped sidewall TPV interconnects, connecting the gold pads on the InP to the aluminum pads on the silicon through a metal-connection

Figure 6.1 shows the 3D-perspective of the simulated a) stud-bump and b) sloped sidewall TPV interconnects, connecting the gold pads on the InP to the aluminum pads on the silicon through a gold metal connection. CST microwave studio software [36] is used for two-port scattering parameter simulations when one port is on the gold pad, and the other is on the aluminum pad. In the simulation of both stud bump (figure 6.1a) and TPV (figure 6.1b), the silicon substrate thickness is 260 μm, aluminum pads on the silicon have 65 μm width and 3 μm thickness, gold pads have the same dimensions as the aluminum pads. The thickness of the InP is 20 μm and 4 μm in figure 6.1a) and figure 6.1b respectively. The stud-bump interconnect in figure 6.1a is a cylinder with equal diameter and height. The sloped sidewall TPV in figure 6.1b has 3 μm thickness. The mediums around the TPV are BCB polymer and air, while air is around the stud-bump.



(a) Electrical S11

(b) Electrical S21

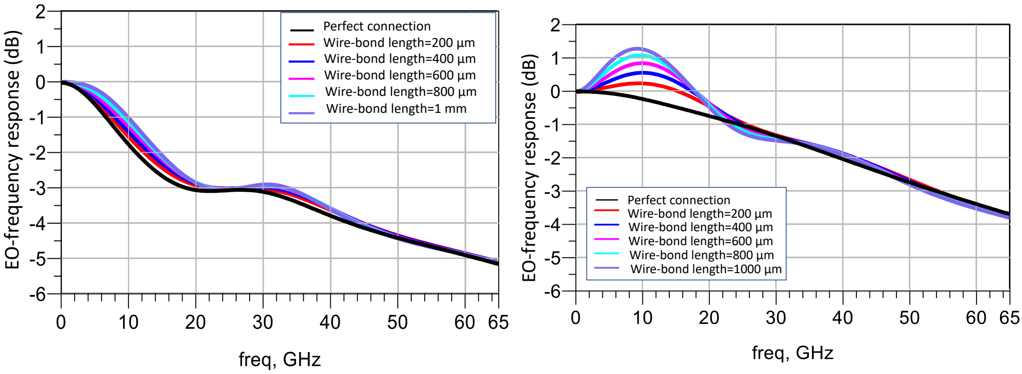
Figure 6.2: Electrical a) reflection (S11) and b) transmission (S21) of the wire-bond, stud-bump, and TPV interconnects.

In figure 6.2, the simulated electrical a) reflection (S11) and b) transmission (S21) of the stud-bump and TPV interconnects are compared with the wire-bond interconnect with 25 μm diameter available in the advanced design system (ADS) simulation software. For comparison, in figure 6.2, scattering parameters of the wire-bonds with 200 and 400 μm lengths and circle cross-sections, stud-bumps with 50 and 60 μm diameters, and TPVs with 10 and 20 μm BCB thickness are depicted. Figure 6.2a shows that the electrical reflection of the wire bond is much higher than stud-bump and TPV. 200 μm wire-bond has -4.5 dB reflection at 100 GHz frequency, and the reflection of the 400 μm wire-bond is -2 dB at 100 GHz. Reflection of the stud-bump is higher than TPV but much lower than the wire-bond. Reflection of the stud-bumps with 50 and 60 μm diameters are -16 dB and -17 dB at 100 GHz, respectively. S11 of the TPVs with 10 and 20 μm BCB is -16.5 and -24 dB, respectively. In figure 6.2a, electrical transmission (S21) of the interconnects are compared. Wire-bond has the lowest transmission at high frequencies, and stud-bump has higher high-speed transmission than wire-bond but lower than TPV. S21 of the 200 and 400 μm wire-bonds at 100 GHz are below -1.5 dB, while the two stud bumps and both TPVs have transmissions above -0.35 dB at 100 GHz.

For 50 Ω systems to tolerate reflections below -10 dB, short wire-bonds with 200 μm length are suitable for frequencies up to 50 GHz; however, for frequency ranges above 50 GHz, reflections from wire-bonds are higher than -10 dB; therefore, for frequencies above 50 GH and reflection below -10 dB stud-bump or TPVs interconnection techniques can be used.

6.3.1 Interconnect effect on the coplanar waveguide modulators

The co-design environment achieved by the spatially resolved circuit model introduced in chapter 3 of this thesis is used for simulating the interconnect effect on the high-speed small and large signal responses of the hybrid coplanar waveguide (HCPW) modulator. The interconnect between the HCPW-MZM to perfect source and termination is studied. The parameters and the circuit of the HCPW-MZM are explained in detail in chapter 3. The phase shifter building block of the HCPW-MZM has a 1 mm length, optical waveguide width of 1.5 μm, signal electrode width of 9 μm, and gap of 11 μm between ground and signal electrodes. The substrate of the HCPW-MZM is semi-insulating (SI).

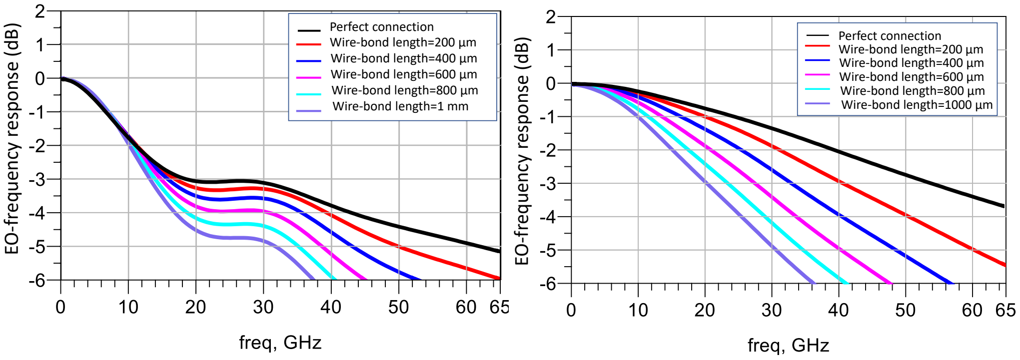


(a) Zs=Zt=50 Ω

(b) Zs=Zt=22 Ω

Figure 6.3: The effect of the 200 μm to 1mm wire-bond interconnections between the termination and HCPW-MZM on the normalized EO-frequency response of the modulator. The source and termination impedances a) are 50 Ω and b) are matched to the characteristic impedance of the phase modulator of the HCPW-MZM (Zs=Zt=22 Ω).

In figure 6.3, the effect of the 200 μm to 1 mm wire-bond interconnection between the termination and modulator on the normalized EO-frequency response of the HCPW-MZM is simulated. In figure 6.3a source and termination impedances are 50 Ω and and in figure 6.3b, Zs= Zt= 22 Ω, is depicted. Zs is the source impedance, and Zt is the termination impedance. In figure 6.3a, the wire-bond has a small positive effect on the EO-bandwidth of the HCPW-MZM. The small peaks in the normalized EO-frequency responses at around 30 GHz increases the bandwidth of 3 dB bandwidth of the HCPW-MZM from 30 GHz to 34 GHz when wire-bond length increases from 200 μm to 1 mm. This slightly higher bandwidth is estimated to be from the constructive interference of the electrical signal along with the modulator and the reflected signal caused by the mismatch between the wire-bond to termination and modulator impedances. Figure 6.3b shows the effect of the 200 μm to 1 mm wire-bond interconnections between the termination and HCPW-MZM when Zs= Zt= 22 Ω. Figure 6.3b shows that when impedances of the source and termination is matched with the modulator, the flat response of the modulator with the perfect interconnections changes to the non-flat curves with a peak at around 10 GHz and another peak at around 30 GHz when MZM is connected to the termination with 200 μm to 1 mm wire-bonds. These peaks are estimated to be from the reflection caused by the impedance mismatches between the wire-bond and both termination and modulator.



(a) Zs=Zt=50 Ω

(b) Zs=Zt=22 Ω

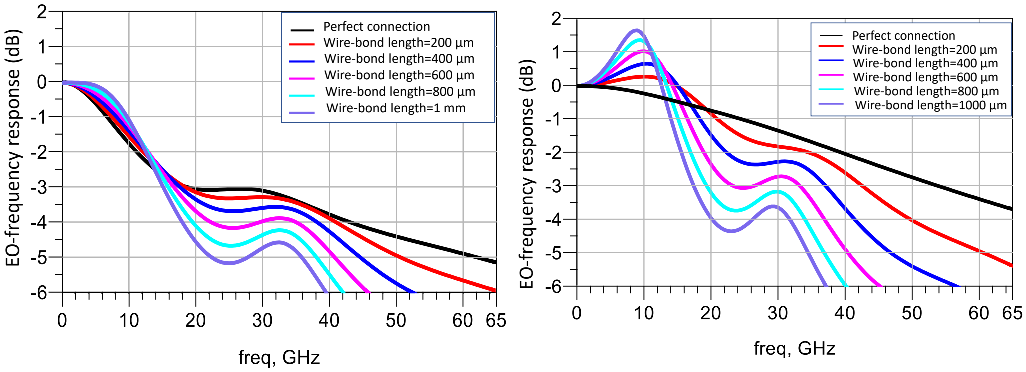
Figure 6.4: The effect of the wire-bond interconnection between the source and HCPW-MZM on the normalized EO-frequency response of the modulator when the source and termination impedances a) are 50 Ω and b) are matched to the characteristic impedance of the phase modulator of the HCPW-MZM (Zs=Zt=22 Ω).

The effect of the 200 μm to 1 mm wire-bond interconnection between the source and termination side of the HCPW-MZM on the normalized EO-frequency response when the source and termination impedances a) are 50 Ω and b) are matched to the characteristic impedance of the modulator (Zs=Zt=22 Ω), is depicted in figure 6.4. In figure 6.4a and 6.4b we see a significant reduction in the normalized EO-frequency response of the modulator wire-bonded to the source, when source and termination impedances are 50 or 22 Ω. This is because the impedance mismatch between the wire-bond and the electrical source reduces the electrical bandwidth of the ideal source signal that passes the wire-bond and goes to the modulator (as shown in figure 6.2b). In figure 6.4a, when source and termination impedances are 50 Ω, 3 dB EO-bandwidth of the HCPW-MZM perfectly interconnected to the termination, reduces from 30 GHz to 16 GHz with 400 μm wire-bond and to 13 GHz with 1 mm wire-bond. figure 6.4b shows that, when source and termination impedances are matched to the modulator impedance, 3 dB EO-bandwidth of the HCPW-MZM perfectly interconnected to the source, reduces from 55 GHz to 34 GHz with 400 μm wire-bond and to 20 GHz with 1 mm wire-bond.

In figure 6.5, the combined effect of the wire-bond interconnection between the modulator and both termination and source, when the source and termination impedances a) are 50 Ω and b) are matched to the characteristic impedance of the phase modulator of the HCPW-MZM, is depicted. 1 mm wire-bond on both termination and source reduces the 3 dB EO-bandwidth of the modulator from 30 GHz to 14 GHz when Zs=Zt= 50 Ω (figure 6.5a) and from 65 GHz to 18 GHz when Zs=Zt= 22 Ω (figure 6.5b).

Figure 6.6 shows the effect of the wire-bond interconnection between the source and modulator on the large signal response of the HCPW-MZM, when source and termination impedances are a) 50 Ω and b) 22 Ω. Optical eye is simulated for a non-return to zero (NRZ) data sequence of 2^8 bits at 40 Gbps and 100 Gbps in figure 6.6a and 6.6b, respectively.

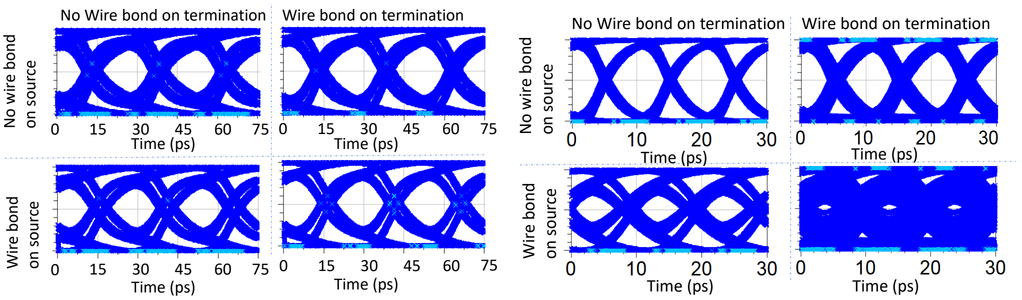
Comparing four eye-diagrams in figure 6.6a shows that for the same reason as the effect of the wire-bond on the EO-response of the modulator, at 40 Gbps when source and termi-



(a) Zs=Zt=50 Ω

(b) Zs=Zt=22 Ω

Figure 6.5: Effect of the wire-bond interconnection between both termination and source to the HCPW-MZM on the normalized EO-frequency response of the modulator when the source and termination impedances a) are 50 Ω and b) are matched to the characteristic impedance of the phase modulator of the HCPW-MZM.



(a) Zs=Zt=50 Ω, bit rate=40 Gbps

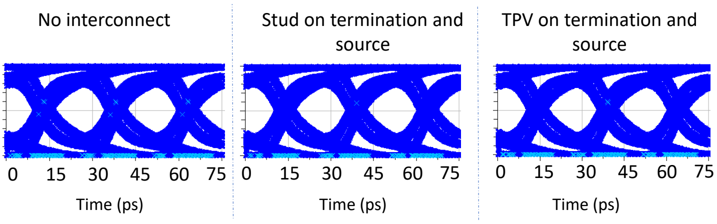
(b) Zs=Zt=22 Ω, bit rate=100 Gbps

Figure 6.6: Effect of the wire-bond interconnection between the source and HCPW-MZM on the large signal response of the modulator when source and termination impedances are a) 50 Ω and b) 22 Ω.

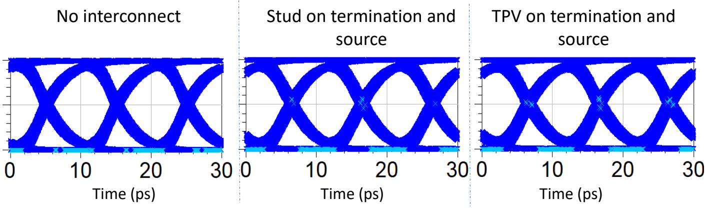
nation impedances are 50 Ω, wire-bond on source reduces the eye-quality while wire-bond on termination slightly improves the eye-quality.

In Figure 6.6b, at 100 Gbps, when source and termination impedances are 22 Ω, wire-bond on both termination and source reduces the eye-quality. However, the effect of wire-bond on the source is stronger than on termination. The effect is negligible when impedance matching is achieved. As depicted in figure 6.6b, for this the combined effect of wire-bond (with the parameters described in section 6.3) on both termination and source is significant, and it closes the eye at 100 Gbps.

Figure 6.7 shows the effect of the TPV and stud-bump interconnects on the eye-diagram of the HCPW-MZM when the source and termination impedances are a) 50 Ω and b) 22 Ω. Optical eye is simulated for a non-return to zero (NRZ) data sequence of 2^8 bits at 40 Gbps and 100 Gbps in figure 6.7a and 6.7b respectively. Figures 6.7a and 6.7b show that TPV and stud bump do not have significant impacts on the quality of the eye.



(a) Zs=Zt=50 Ω, bit rate=40 Gbps



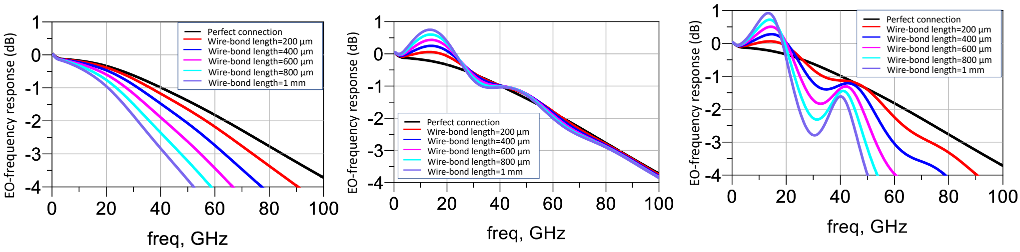
(b) Zs=Zt=22 Ω, bit rate=100 Gbps

Figure 6.7: Effect of the TPV and stud-bump interconnects on the eye-diagram of the HCPW-MZM when source and termination impedances are a) 50 Ω and b) 22 Ω

By studying the effect of the three wire-bond, stud bond, and TPV on the small and large signal responses of HCPW-MZM, we saw that wire-bond interconnects do not have a high impact on the responses of the HCPW-MZM with 50 Ω source and termination. However, when source and termination impedances are matched to the modulator impedance and the 3 dB EO-bandwidth of the MZM is high (64 GHz), wire-bond significantly reduces the EO-bandwidth and eye quality of the modulator. This study also showed that stud-bump and TPV do not show a visible impact on the small and large signal responses of the HCPW-MZM modulator.

6.3.2 Interconnect effect on the coplanar stripline modulators

Interconnect effect on the small and large signal responses of the coplanar stripline MZM is discussed in this subsection. The co-design environment described in chapter 3 of this thesis is used for simulating the interconnect effect on the high-speed small and large signal responses of the CPS-MZM. The interconnect between the modulator to perfect source and termination is studied. The cross-sectional parameters and the circuit of the CPS-MZM are explained in detail in chapter 4. CPS-MZM of this work has 1 mm length, 1 μm optical waveguide width, 10 μm electrode width, 10 μm electrode gap, and a SI substrate.
Figure 6.8 shows the 200 μm-1 mm long wire-bonds effect on the electro-optical frequency response of the CPS-MZM when wire-bond is on a) source, b) termination and c) both termination and source. Source and termination impedances are 50 Ω. The characteristic impedance of the CPS-modulator at frequency ranges from 1 to 100 GHz is 55-57 Ω from the simulations. In figure 6.8a, since wire-bond reduces the high-speed transmission of the signal that passes through it, the wire-bond on source reduces the EO-bandwidth of the CPS-MZM significantly. The 3 dB EO-bandwidth of the transmitter reduces from 84 GHz to 42 GHz when a 1 mm wire-bond is applied to the source. In figure 6.8b, effect of



(a) Wire-bond on source

(b) Wire-bond on termination

(c) Wire-bonds on termination and source

Figure 6.8: Effect of the 200 μm-1 mm wire-bonds on the electro-optical frequency response of the CPS-MZM when wire-bond is on a) source, b) termination, and c) both termination and source. Source and termination impedances are 50 Ω.

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the wire-bond on termination is studied. The smooth response of the CPS modulator connected perfectly to the source and termination gets distorted when wire-bond is applied on termination but does not strongly affect the EO-bandwidth. The distortion on normalized frequency response is estimated from the impedance mismatches between the wire bond to both modulator and 50 Ω termination. 1 mm wire-bond reduces the 3 dB EO-bandwidth of the CPS modulator from 84 GHz to 80 GHz. The combined effect of the wire-bond on both termination and source is showed in figure 6.8c. Distortion from the wire-bond on termination and lower input electrical signal strength from the wire-bond on source, changes the smooth EO-response curve of the CPS-MZM to a non-smooth response with 3 dB EO-bandwidth of 48GH when wire-bond length is 1 mm.

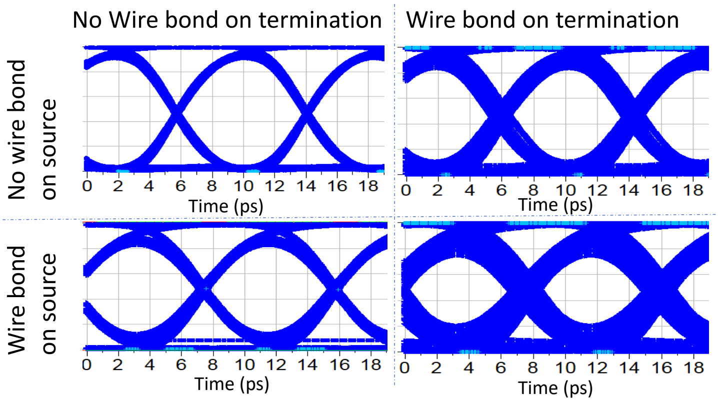


Figure 6.9: Wire-bond effect on the eye diagram of the CPS-MZM when 400 μm wire-bond is applied on the source, termination, or both. Zs=Zt=50 Ω, bit rate= 120 Gbps.

Wire-bond effect on the eye-diagram of the CPS-MZM when 400 μm wire-bond is applied on the source, termination, or both showed in figure 6.9 when Zs=Zt=50 Ω. The optical eye is simulated for a non-return to zero (NRZ) data sequence of 2^8 bits at 120 Gbps. Distortion from wire-bond applied between termination and modulator on the EO-response of the CPS-MZM (figure 6.8b) reduces the quality of the eye. The EO-bandwidth reduction

caused by wire-bond on the source (figure 6.8a) also reduces the quality of the eye. The combined effect of the 400 μm wire-bond on both source and termination reduces the quality of the simulated eye diagram of the CPS-MZM significantly.
TPV and stud-bump effect on the normalized electro-optical frequency response of the CPS-MZM when source and termination impedances are 50 Ω is depicted in figure 6.10. This figure shows that applying TPV or stud-bump on both termination and source does not have any visible effect on the EO-response of the CPS-MZM.

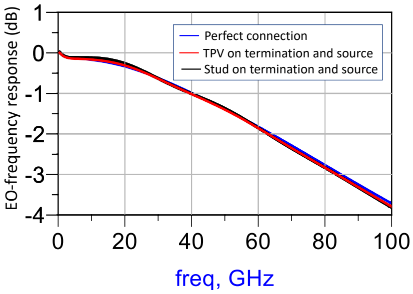


Figure 6.10: TPV and stud-bump effect on the optical eye diagram of the CPS-MZM when source and termination impedances are 50 Ω, and bit rate is 120 Gbps.

Figure 6.11 depicts the TPV and stud-bump effect on the optical eye-diagram of the CPS-MZM when source and termination impedances are 50 Ω, and bit rate is 120 Gbps. Comparing the three eye-diagrams in figure 6.11 shows that TPV and stud bump does not have any visible effect on the simulated optical eye diagram of the CPS-MZM at 120 Gbps.

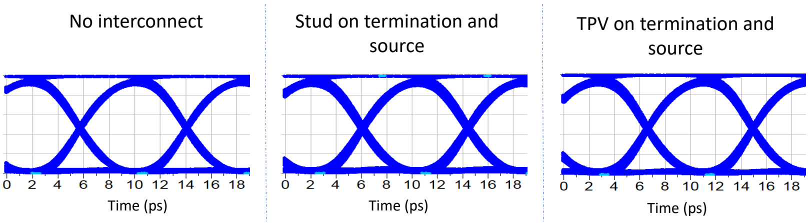


Figure 6.11: Effect of the TPV and stud-bump on the eye-diagram of the CPS-MZM when the source and termination impedances are 50 Ω, and bit rate is 120 Gbps.

6.4 On-chip termination

In the previous section of this chapter, for studying the effect of the interconnect circuits on the small and large signal responses of the high-speed modulators, a perfect broadband termination was used. For DC decoupling and reducing the low frequency reflections, an ideal broadband termination usually requires an infinite capacitance in series connection with the desired resistance. However, in practice, terminations are not perfect, and capacitance is not infinite. Therefore, in this section, we look at the effect of the termination capacitance on the electro-optical frequency response of the high-speed MZM. We study the required capacitance value for broadband and high-speed response of the HCPW-MZM.

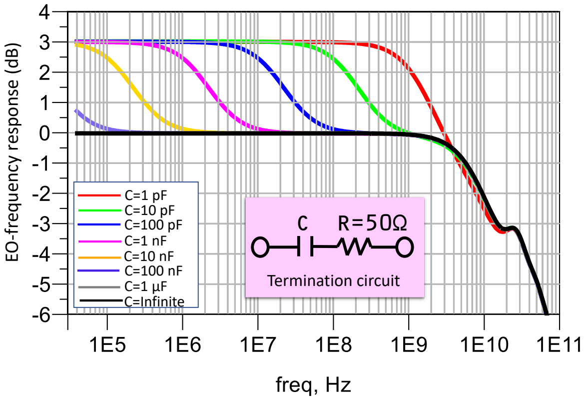


Figure 6.12: Effect of the termination capacitance on the electro-optical frequency response of the 1 mm HCPW-MZM terminated by termination with 50 Ω resistance (R) and a sweep of capacitance (C)

Figure 6.12 shows the effect of the termination capacitance on the normalized electro-optical frequency response of the HCPW-MZM terminated by termination with 50 Ω resistance (R) and a sweep of capacitance (C). In this plot, the EO-frequency response is compared with a modulator, terminated with a perfect termination that has an infinite capacitance. All of the plots are normalized to the EO response of the HCPW-MZM terminated by a perfect 50 Ω termination at 40 kHz. Figure 6.12 shows that increasing the capacitance from 1 pF to 0.1 μF reduces the low-frequency cut-off from more than 3 GHz to around 100 kHz. The 3 dB steps on the EO-responses are because when capacitance is low, and the imaginary part of the termination is very high, it is like the open circuit (infinite impedance), and the signal can not see the termination resistance.

Comparing the plots in figure 6.12 shows that for a broadband MZM with a low cut-off frequency of 40 KHz, the modulator has to be terminated with a termination with capacitance higher than 1 μF.

6.4.1 Design

To study the effect of the OCT on the EO-response of the HCPW-MZM, an on-chip termination is designed.

Figure 6.13 shows an on-chip termination (OCT) that is previously made in the generic InP platform with SI substrate [123]. The layer stack of this OCT is similar to the layer stack of the phase-modulator BB in chapter 2, which is listed in table 2.1. Resistance of the n-doped InP is used to make the resistance, and depletion layer capacitance is used to make the OCT's capacitance.

We taped-out an OCT with similar cross-section as reference [123] on a generic InP process with SI substrate. The OCT dimensions are: W1=W2= 75 μm G=85 μm, L=75 μm (figure 6.13).

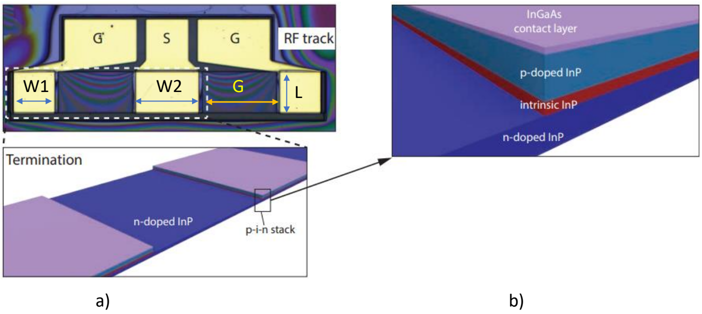
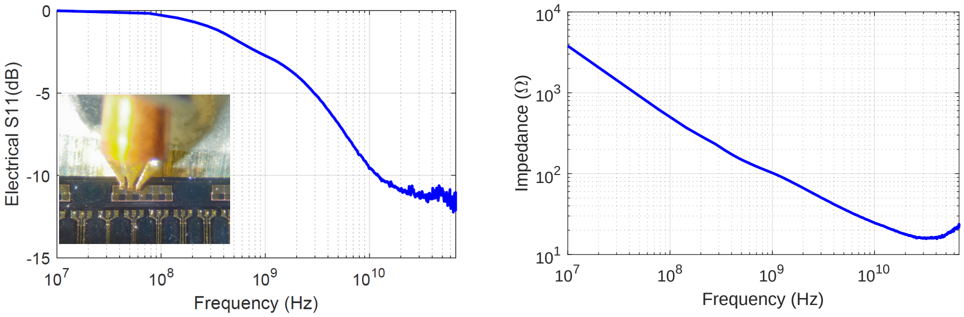


Figure 6.13: a) Microscope image the OCT and structure of the layers used. b) Detailed view of p-i-n layers [123].

6.4.2 Experiment

Figure 6.14 shows a) Electrical S11 (normalized to 22 Ω) and b) impedance of the on-chip termination under test, which is produced in the generic InP platform with SI substrate. Scattering parameter measurement is done by a GSG probe that was connected to the vector network analyzer with 50 Ω impedance via a coaxial cable. Figure 6.14a depicts the electrical S11 of the OCT which is normalized to 22 Ω. In figure 6.14a, for frequencies higher than 11.6 GHz, the normalized (to 22 Ω) electrical reflection of the OCT is below -10 dB, and at 64 GHz, reflection is the minimum of -12.5 dB. Reducing the frequency from 11.6 GHz to 10 MHz increases the reflection from -10 dB to -9 mdB, which is very high.



(a) Electrical S11

(b) Impedance, Ω

Figure 6.14: a) Electrical S11 (normalized to 22Ω) and b) impedance Ω of the on-chip termination produced in the generic InP platform with SI substrate.

Measured electrical reflection (S11) is used for calculating the characteristic impedance of the OCT as follows [38]:

$$Z_{OCT} = Z_0 \frac{1+S11}{1-S11} \tag{6.1}$$

Z_0 is the reference measurement impedance which is 50 Ω. In figure 6.14b, the calculated impedance of the fabricated OCT (Z_{OCT}) is showed. The impedance of the OCT is 24 Ω at 67 GHz. Reducing the frequency from 67 GHz reduces the impedance to the minimum of

18.2 Ω at 35 GHz and then increases the impedance to 3.8 MΩ at 10 MHz.
We used the co-design environment achieved by the spatially resolved circuit model introduced in chapter 3 of this thesis for simulating the effect of this OCT on the EO-frequency responses of the HCPW-MZM with the same parameters as the modulator that was studied in subsection 6.3.1 of this chapter. The frequency dependent characteristic impedance of this modulator is between 20-26 Ω. The measured scattering parameter of the OCT is used for terminating the HCPW-MZM.
Figure 6.15 compares the simulated electro-optical frequency response of the HCPW-MZM terminated by a perfect 22 Ω and by the OCT. Both simulations are normalized to the EO-response of the HCPW-MZM terminated with a perfect termination at 10 MHz. The simulated EO-response of the modulator terminated by OCT has a 3 dB step at lower frequencies compared to the modulator terminated with a perfect 22 Ω termination. This is because the OCT's capacitance is much smaller than what is required for a broadband termination (more than 1 μF).
Figure 6.15 shows that the EO-frequency response of the HCPW modulator terminated by OCT at the frequency range of 12-67 GHz overlaps the EO-response of the terminated modulator with a perfect 22 Ω termination. This makes the OCT a good candidate for the K-band applications with 18-27 GHz frequency ranges.

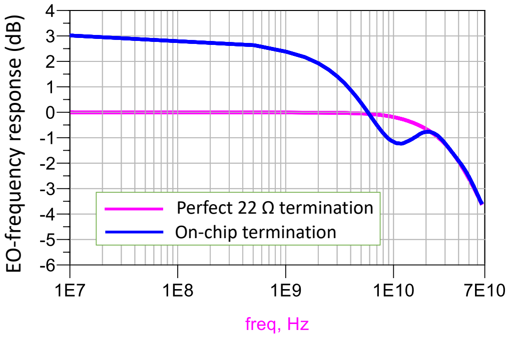


Figure 6.15: Electro-optical frequency response of the 1 mm HCPW-MZM terminated by a perfect 22 Ω and by on-chip terminations.

6.5 Co-designed photonic integrated circuit

A single co-designed photonic cell for comparison of the wire-bond and stud-bump interconnect techniques has been designed. The photonic cell is taped out on a dedicated semi-insulating (SI) process and additionally on an n+ multi-project wafer process [65]. The n+ circuits were available for assembly to the electrical driver and termination. Figure 6.16 shows the picture of a single photonic cell co-designed for comparison of the wire-bond and stud-bump interconnect techniques. This includes two CPS-MZMs, two on-chip lasers, metal pads for DC, and metal pads for RF and is capable of two sets of assemblies (1 and 2 in the picture) to the driver and termination.
In figures 6.17 and 6.18 layouts of the co-designed photonic cell in a) wire-bond assembly and b) stud-bump assembly to the BiCMOS drivers are depicted. In this picture, the

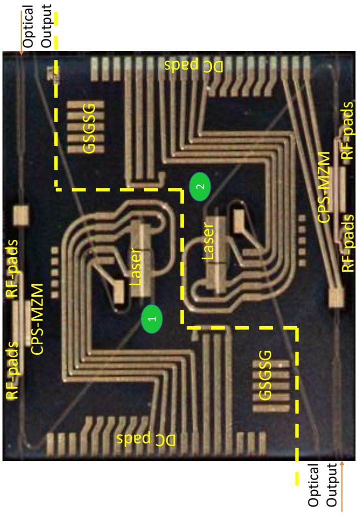


Figure 6.16: Co-designed photonic integrated circuit including two CPS-MZMs, two on-chip lasers, metal pads for DC, metal pads for RF, etc.

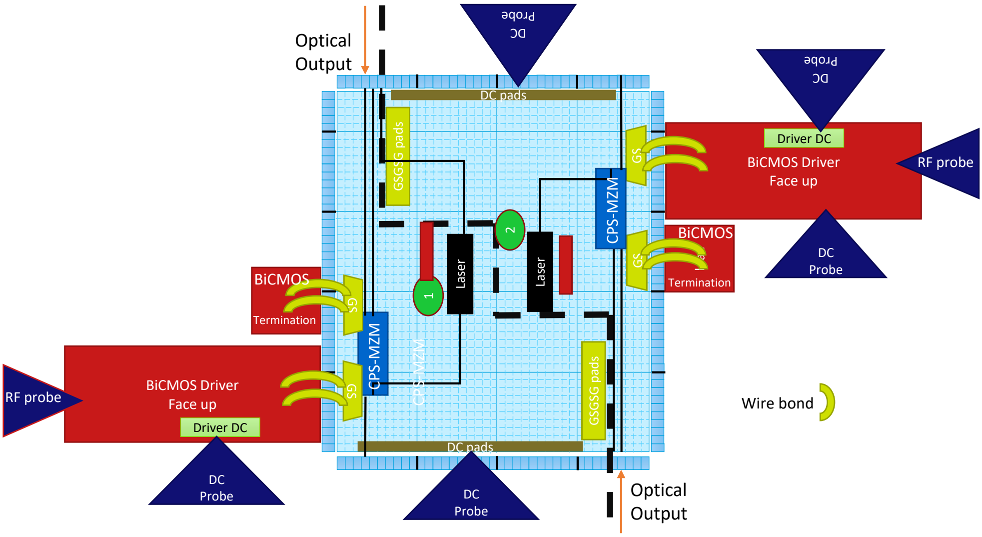


Figure 6.17: The layout of the co-designed photonic cell in wire-bond amenably to the BiCMOS drivers and terminations.

photonic cell is blue, and BiCOMS drivers and terminations are red. DC and RF probing scheme is also depicted. In figure 6.17 photonic cell is in the center, and two sets of BiCMOS drivers and termination on the sides are wire-bonded to the two CPS-MZMs. On-chip coupled-cavity lasers [124] are designed to generate the light source. Optical outputs are on the top and bottom sides of the photonic cell. For minimizing the wire-bond length,

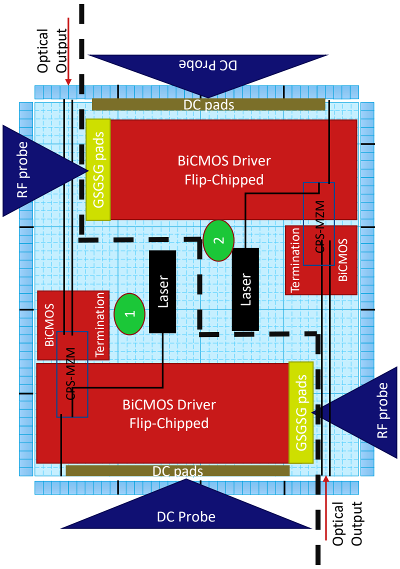


Figure 6.18: The layout of the co-designed photonic cell in stud-bump assembly to the BiCMOS drivers and terminations.

CPS-MZMs are designed close to the edges of the photonic chip. In figure 6.18 for stud-bonding, two sets of BiCMOS driver and termination are flipped-chip on the photonic cell, which includes two CPS-MZMs. GSGSG metal tracks are designed on the photonic chip for RF probing the flipped-chip BiCMOS drivers from the top. DC pads on the top and bottom sides are designed for DC probing the drivers and lasers.

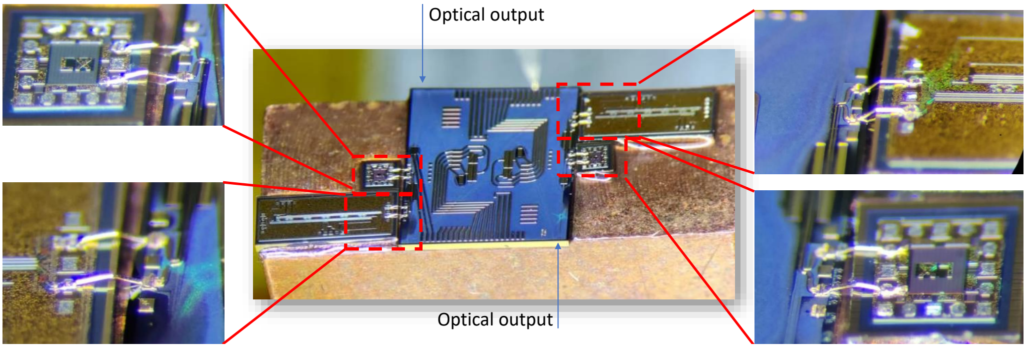


Figure 6.19: Co-designed photonic integrated circuit including CPS-MZMs, on-chip laser, wire-bonded to the BiCMOS drivers and terminations.

Figure 6.19 shows the wire-bond assembly of the two sets of BiCMOS drivers and termination to the co-designed PIC [1]. The photonic cell and four BiCMOS cells are die bonded to a copper chuck. Manual tweezers and the K&S 4526 wedge bonder are used for die bonding. To have electrical isolation of the photonic and electronic PICs, the adhesive bonding was

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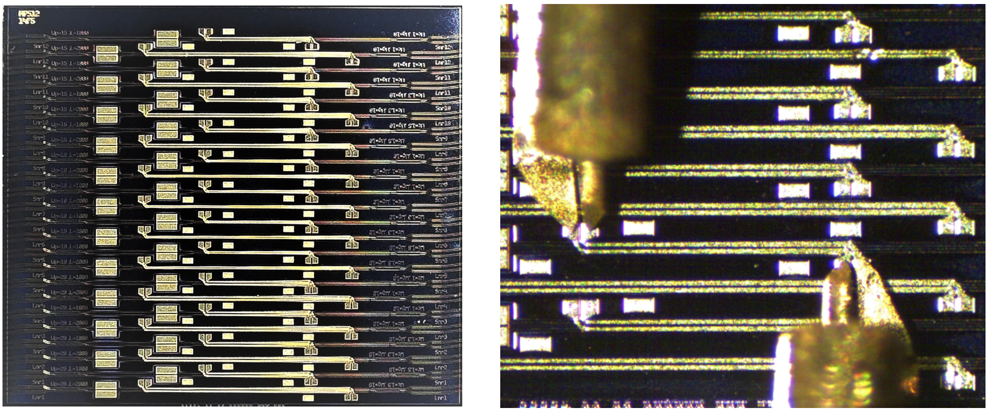
[1] Wire-bonding and pictures of the assembly are done by Michail Chatzimichailidis

done by using a non-conductive epoxy [125]. Wire-bonds with 25 μm diameter are used for electrical connection of the electrical input of each CPS-MZM to a BiCMOS driver and the electrical output of each CPS-MZM to a BiCMOS termination.
On-chip measurement of the coupled-cavity laser with 315 μm and 268 μm cavity lengths is done. 40 mA current is applied to each cavity and the voltage of 1.8-1.9V was measured. The output of the laser was -58 dBm which was not enough for measuring the EO-response of the CPS-MZM assembled to the driver and termination. Th measurement is repeated to the second laser on the same chip and any output power from the lasers has been detected. The visual inspection does not show any defect on the laser and optical input/outputs. The design has to be studied.
The chip includes a second optical waveguide to each MZMs for external laser input. However, because the insertion loss of the MZMs was in the range 25-30 dB was high for the large-signal modulation experiment.

6.6 Tapered coplanar strip-line modulator

Electronic systems are commonly made with 50 Ohm impedances. For minimizing the reflections from the interface between the modulator and electronic drivers, in chapter 4 of this thesis we focused on the design of the high speed CPS modulators with 50 Ω characteristic impedance. For the co-design approach and increasing the flexibility of the modulator's impedance at the input and termination interfaces, in this section we realize a high density and high-speed, tapered-CPS-MZM with different input and output impedances. The high-density co-planar stripline electrodes in the phase modulator provides better integration of the device into the electrical system. Moreover, the tapered configuration has a new degree of design freedom for managing reflections, flattening the response and extending the bandwidth.



(a) Photonic integrated cell

(b) Device 4 under test

Figure 6.20: a) A microscope image of a 4.6 mm x 4.0 mm cell containing 24 TCPS Mach-Zehnder modulators with different front and end parameters. b) Image of device 4 from the bottom under test with RF probes applied.

Figure 6.20 shows a) a microscope image of a 4.6 mm x 4.0 mm cell containing 24 tapered

Mach-Zehnder modulators with different front and back parameters, b) an image of device four from the bottom under test with RF probes applied. Devices 3 and 4 from the bottom are assessed in this work. Phase modulators of devices 3 and 4 are 1 and 2 mm in length, respectively.

6.6.1 Modulator design

The assessed devices with the top and cross-sectional view, as depicted in figure 6.20, are designed with different mask parameters at the front (side A) and end (side B) sides of the phase modulation section that results in a tapered shape. The aspect ratio is adjusted to emphasize design features. Side A has a waveguide width of 1 micron, electrodes width of 10 μm, and electrodes gap of 20 μm, while side B has a waveguide width of 1.3 μm, electrodes width of 20 μm, and electrodes gap of 10 μm. The design intent is to have 35 Ω and 55 Ω characteristic impedances at the two A and B sides of the CPS modulator respectively.

As discussed in section 4.3 of this thesis, increasing the waveguide and electrode widths and reducing the electrodes gaps reduces the characteristic impedance of the CPS line; therefore, side A is estimated to have a higher impedance than side B. Using the electrical model introduced in section 2.3.1 of this thesis, the impedance at sides A and B are calculated to be 35 Ω and 55 Ω, respectively.

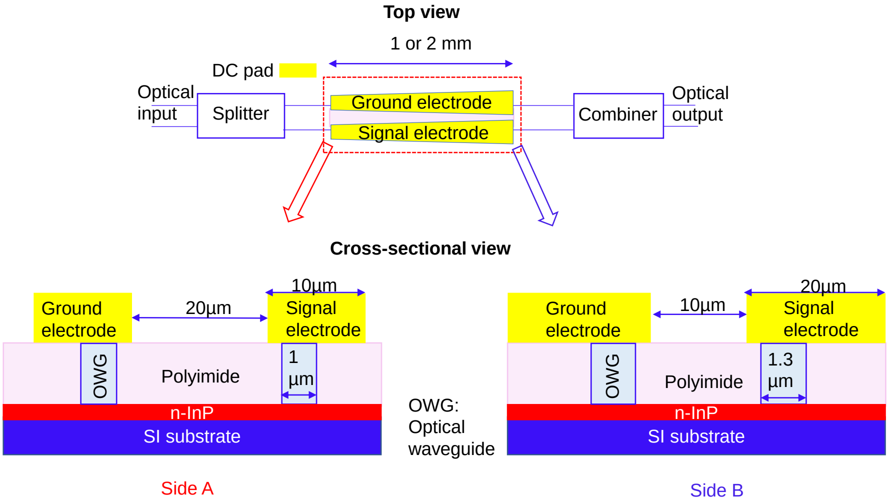
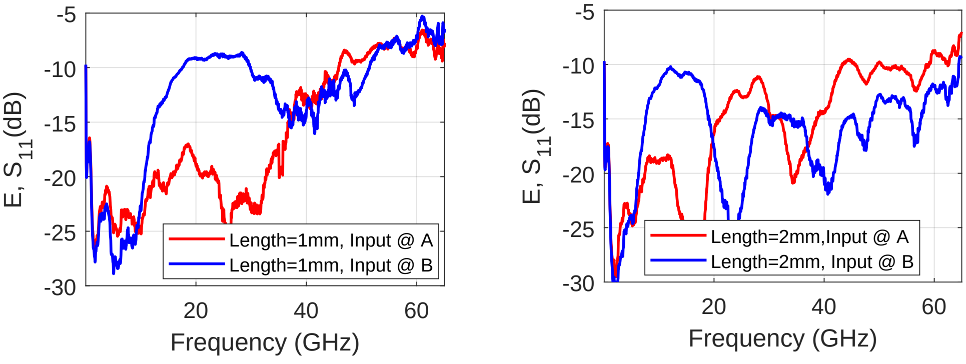


Figure 6.21: Top and cross-sectional views of the tapered-CPS modulator and the mask level detail with the design intent.

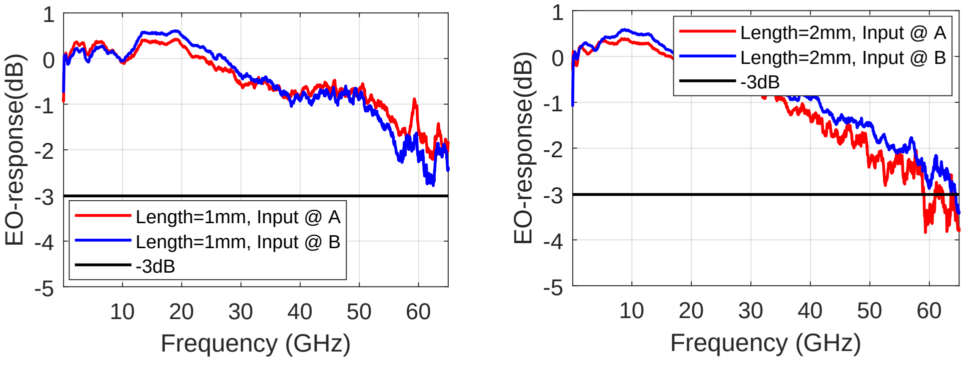
6.6.2 Small-signal performance

The RF electrical design is first analyzed at zero DC bias using a vector network analyzer. The calibration procedure is done by probing an on-wafer calibration kit which includes open, short, load and through structures for one port electrical calibration. The S11 reflections are determined with the second port terminated to 50 Ω. Figure 6.22 shows the S11 reflections of the tapered-CPS modulators with a) 1 mm and b) 2 mm lengths when the input probe is at side A for the red curves and at side B for the blue curves. Comparing the blue and red reflections curves shows that the reflection from the 50 Ω termination is different. This difference is because of the different characteristic impedances of the side A and B. For example, in figure 6.22a when the modulator length is 1 mm, the difference of the electrical reflection to the 50 Ω termination is significant at the frequencies 17-35 GHz for input at A and B sides. Increasing the length to 2 mm in figure 6.22b increases the frequency range with different reflections to the 50 Ω load from A and B sides to 10-67 GHz. Agilent's lightwave component analyzer model N4373 is used for measuring the small signal electro-optic (EO) modulation responses. The EO-frequency responses of the a) 1 mm



(a) 1 mm length (b) 2 mm length

Figure 6.22: Electrical reflections of the tapered-CPS modulators with a) 1 mm and b) 2 mm lengths when the input probe is at side A for the red curves and at side B for the blue curves.



(a) 1 mm length (b) 2 mm length

Figure 6.23: Small-signal electro-optical frequency-response of the tapered-CPS modulators with a) 1 mm and b) 2 mm lengths when the input probe is at side A for the red curves and side B for the blue curves.

and b) 2 mm long tapered-CPS modulator designs depicted in figure 6.23. In the S21 measurements, an optical amplifier and a passive optical band-pass filter have been used after the optical output of the devices. In both figures 6.23a and 6.23a, at the lower frequency ranges when input is at side A (blue curves), higher reflections to the 50 Ω load result in a peak at the EO-response of the modulators. These peaks appear at around 18 GHz and 10 GHz for 1mm and 2mm length modulators. However, at a frequency around 60 GHz, when input is at the side A, EO-response is lower in the modulator with 1 mm length and higher in the 2 mm modulator. This is because 1 mm modulator has a higher reflection to the 50 Ω load at 60 GHz when input is at A (figure 6.22a), while at the same frequency, electrical reflection is lower in the 2 mm device (figure 6.22b).

6.7 Summary

Co-integration of the high-speed modulator PICs to the driver EICs is studied. The effect of the interconnects between the electronic to photonic integrated circuits is researched. The electrical scattering parameters of the stud-bump and TPV interconnects are simulated and compared with the wire-bond interconnect available in the advanced design system (ADS) simulation software. We showed that wire-bond with the lowest transmission and stud-bump has higher high-speed transmission than wire-bond but lower than TPV at high frequencies. S21 of the 200 and 400 μm wire-bonds at 100 GHz are below -1.5 dB, while the two stud bumps and TPVs have transmissions above -0.35 dB at 100 GHz.

The co-design environment is used to study the effect of the interconnects on the small and large signal responses of high-speed CPW and CPS modulators connected to the perfect termination and source. Small and large-signal simulation results show that wire-bond interconnects introduce significant reductions on the EO-bandwidth and optical eye quality of both CPW and CPS modulators while stud-bump and TPV impact the responses those modulators is minimal.

For achieving a high-speed EO-bandwidth, high-speed MZMs have to be terminated to a proper termination circuit. A perfect termination has infinite capacitance. However, the capacitance of a termination is not infinite in practice. We studied the impact of the termination capacitance on the broadband electro-optical frequency response of the HCPW-MZM. We showed that for a broadband HCPW-MZM, the capacitance of the termination has to be higher than 1 μF. Then, in the co-design environment, the measurement data of an on-chip termination (OCT) fabricated in a generic InP platform with semi-insulating (SI) substrate is combined with the spatially resolved circuit model of the HCPW-MZM, and the EO-frequency response of the MZM was simulated. For frequencies higher than 12 GHz, the simulated EO-frequency response of the HCPW-MZM terminated with the OCT overlapped with the modulator terminated with perfect matched termination. Simulations showed that at lower frequency ranges up to 10 GHz, the OCT that is studied in this work has more than -10 dB reflection to the load. Therefore, this OCT is suitable for K-band applications with a frequency range of 18-27 GHz.

To compare the effect of state-of-the-art interconnect technologies on the large signal response of the MZM, a single PIC including the laser sources and high-speed CPS modulators is co-designed to the BiCMOS drivers and terminations. The co-designed single PIC layout is compatible with wire-bond and stud-bump assemblies to BiCMOS driver and termination EICs enable comparing these two technologies' effects on the optical eye diagram. Coupled cavity lasers of the PIC were measured. However, the optical output of the lasers was not enough for measuring the EO-response of the CPS-MZM assembled to the driver and termination.

For the co-design approach and increasing the flexibility of the modulator's impedance at the input and termination interfaces, a tapered-CPS-MZM with different input and output waveguides, electrode width, and gaps is introduced. Simulations predicted 35 and 55 Ω impedances at the front and end sides of the modulator. Different electrical reflection from the 50 Ω load to the two sides of this modulator showed that this modulator has different input and output impedances. The tapered-CPS-MZM of this work is a good candidate for co-design approaches when different input and output impedances are desired. For instance a TCPS-MZM with matched input impedance to the electrical circuit and higher output impedance (more details in section 2.4.2) matched with a termination impedance can reduce the power consumption of the modulation circuit without back reflection to the electrical circuits.

Chapter 7

Conclusions and outlook

7.1 Abstract

In this chapter, first, the work is summarized in section 7.2. Then the research questions are addressed in section 7.3, and finally, the outlook is proposed in section 7.4.

7.2 Summary

At the heart of the optical links, optical transceivers convert data from the electrical to the optical domain and are made from photonic and electronic integrated circuits. To increase the speed and reduce the power consumption of the transceivers, both electronic and photonic building blocks and the interconnections between them have to be properly co-designed.

This thesis looked into the co-design and co-integration of the high-speed photonic to electronic integrated circuits. Special attention was paid to the Mach-Zehnder modulator's building block, a co-design environment to study the co-integrated photonic to electronic ICs, and technology developments for high-speed electrical connection of the PICs and EICs. Moreover, a particular focus is placed on realizing a Mach-Zehnder modulator with best-in-class bandwidth and density, which is expected to enable very advanced applications in high-speed optical communication systems.

7.3 Research questions

We first studied the phase modulator's building block and answered the following question.

Which cross-sectional and mask parameters in the MZM building block have a high impact on the high-speed performance of the modulator?

To answer this question, we started with developing a compact electrical model in a 3D simulation tool [36]. The inputs of this model are just the material and dimensional parameters of the MZM building block. We validated the model [126] by comparing it to a reference device in a generic InP platform fabricated by SMART Photonics. Next, we performed simulations for exploring the parameter space of the hybrid coplanar waveguide (HCPW) modulator's building block. Then we analytically combined the electrical model and built an electro-optical model. Finally, we validated the model [126] and used it for discussing the cross-sectional and mask parameters' effect on the modulator's 3dB electro-optical bandwidth.

Since increasing the inductance and reducing the capacitance of the reference HCPW-MZMs improves the velocity and impedance matching, we studied the mechanisms for doing those changes. Then we identified that reducing the waveguide width, increasing the thickness of the waveguide core, and reducing the signal electrode width have the highest impact on the high-speed specifications of the HCPW-MZM. These parameter changes improve the velocity and impedance matching of the modulator and reduce the cross-sectional electrical loss. Moreover, we proposed a parameter set enabling an electro-optical bandwidth of 120 GHz, more than four times the reference device bandwidth with 30 GHz bandwidth. Since this design requires epitaxial and technology changes that can not be realized in the available generic technology, we were unable to validate these results directly.

Getting knowledge of the modulator building block enabled us to introduce a new electrode design for a compact, velocity, and impedance-matched, high-speed co-planar stripline (CPS) modulator with a very small footprint in the InP platform. Then we addressed the second question of this thesis as follows.

What are the density and speed limits of the generic InP platform?

For answering this question, we first simulated the effect of the substrate on the RF performance of the CPS-MZM and showed that for a unique CPS modulator design, the n-doped substrate has about 1.5 times higher electrical loss than the SI substrate. We also studied the effect of the three mask parameters on the frequency-dependent microwave index and line impedance. Moreover, RF electrical and electro-optical responses of the CPS-MZM with the SI-substrate were simulated.

Then, we compared the CPS-MZM in an n-doped substrate with the conventional HCPW-MZM produced in the same platform and proved the velocity and impedance matching enabled by CPS electrode design. The total width was reduced from 110 μm in the CPW electrode to 27 μm in the CPS electrode. The bandwidth of the modulator bandwidth is improved from 7.5 GHz in the CPW to 27.5 GHz in the CPS modulator.

Since this CPS-MZM was bandwidth limited by the n-doped substrate, we adapted the design to a semi-insulating substrate, and we demonstrated a high-density and high-speed CPS modulators with a 1.4 dB electro-optic modulation bandwidth of 67 GHz, and we predicted the 3dB bandwidth of over 110 GHz. The total width of this fabricated CPS electrode is 17 μm, which is the smallest reported width. Reducing this modulator's electrode width and gap to 2 μm is predicted to have a 3 dB bandwidth of 114 GHz and an even higher density with a total 6 μm width. However, electrode width below 5 μm and electrode gaps smaller than 7 μm are not manufacturable with the current technology.

Since the new CPS building block designs do not need any epitaxial changes to the generic platform, integrating these modulators does not impact the performance of the other active or passive building blocks of the platform. Therefore, these MZMs are ready for use in co-designed, high density, and high-speed applications and can be implemented in a

publicly available generic InP platform [65].
The limits to the density are ultimately the signal line width with values of order 5-10 μm in this work, and the separation of the lines - so far 5-10 μm. Further reductions will require process engineering.

High-speed and high-density co-integration of the photonic and electronic integrated circuits requires high-speed and high-density interconnections. In this thesis, we described a key enabling step towards ultra-tight 3D integration of electronic and photonic circuits at wafer-scale, and we addressed the following question.

What is limiting the 3D integration of the photonic and electronic ICs?

3D integration provides flexibility for physically-close co-integration of the electronic and photonic integrated circuits made with different technologies. For example, distances between bond pads can be reduced to microns, and bond wires can be removed from the assembly. This is important for high-speed applications when parasitics reduce the bandwidth of the co-packaged devices.
We focused on two fabrication methods for short wafer-scale metal connections that can be used for 3D integration of the InP and silicon wafers:

1. Using the evaporated seed layer, sloped sidewall TPVs are created. The electrical performance is assessed from scattering parameters of vias. These short vias show a very high-speed performance with less than 0.4 dB electrical loss in the measurement range up to 67 GHz. Furthermore, to check the strength of these vias, the mechanical reliability of vias in the temperature cycle's presence is tested. Four-probe measurement is performed for metal tracks, with vias. The resistance of the metal tracks, including TPVs before and after the T-cycle, is within the same range, proving the mechanical reliability of the created TPVs in the range of T-cycling.
2. For smaller, more compact structures with lower parasitic, atomic layer deposition is used to create a seed layer for the steep sidewall through-polymer vias. Two in series high-density TPVs with 40 and 10 μm signal width and gap, respectively, showed high-speed performance with 0.2 dB loss over the 67 GHz, making them promising candidates for wafer-scale co-integration high-speed photonic-electronic devices.

Technological developments have been done, and two routes have been demonstrated. Densities of 20-microns have been shown for TPVs. The challenge becomes more commercial, understanding at which component density and performance makes sense to implement flip-chip, die to wafer bonding, and even wafer to wafer bonding. Wafer to wafer bonding was demonstrated in the previous work [113], but questions are raised about whether this is viable at this time due to the mismatch in wafer size. Designs are realized for die to wafer in this thesis and are the subject for future study.

The high-speed performance of the realized CPS-MZM building block can improve the speed of the photonic modulation circuit, and the small footprint of this CPS-MZM can minimize the interface losses between the co-integrated electronic to photonic circuits. However, the overall electro-optical performance of the co-integrated photonic to electronic ICs is dependent on the co-design of the individual building blocks and the interconnections between them. For this reason we addressed the final question of this thesis as follows:

Can we build a co-design environment to explore the benefit of electronic to photonic co-integration?

We started by proposing a co-design methodology for the optimization of high-speed characteristics in Mach-Zehnder modulator-based transmitters. The co-design environment of this thesis just uses a parametric, non-iterative, traveling-wave model for the phase modulators, which is readily incorporated with the optical circuit and driver networks. The introduced model uses only measurable design parameters such as layer thicknesses, materials properties, and mask feature dimensions. We validated the model accuracy by comparing it to the measurement data of the high-speed foundry-produced indium phosphide HCPW and CPS modulators. The co-design environment introduced in this thesis can calculate both small and large signal electro-optical responses of the whole electro-optical circuit.
A co-design environment is the only route to accurate modeling of the high-density co-integrated photonic-electronic ICs beyond 50 GHz.

By studying the modulator building block, demonstration of the high-speed and density CPS-MZM, 3D interconnection technology developments, and co-design environment, we answered the above four main questions of this thesis. This enables us to address the central question of this thesis as follows.

Can close co-integration of the electronic and photonic circuits increase high-speed performance?

To answer this question, we first used the co-designed model to study impedance matching. By matching the termination impedance to the transmission line impedance of the HCPW-MZM, the 3 dB optical modulation bandwidth is observed to increase from 30 GHz to 57 GHz, representing a two-fold increase relative to the 50 Ω termination condition. Then a co-designed passive interconnection network is proposed between the 50 Ω driver and the 20 Ω phase modulator to increase the electro-optic bandwidth of the MZM and improve the eye-opening for on-off-keyed data. The passive electrical pre-compensation predicted a 3 dB optical modulation bandwidth to increase from 30 GHz to 57 GHz and double the large-signal modulation bandwidth of the reference HCPW-MZM to 80 Gbit/s for on-off-keyed modulation with a 7.5 dB extinction ratio. For achieving a high-speed EO-bandwidth, high-speed MZMs have to be terminated to a proper termination circuit. A perfect termination has infinite capacitance. However, infinite capacitance can not be realized in practice. We showed that for a broadband HCPW-MZM, the capacitance of the termination has to be higher than 1 μF. Then, in the co-design environment, the measurement data of an on-chip termination (OCT) fabricated in a generic InP platform with semi-insulating (SI) substrate is combined with the spatially resolved circuit model of the HCPW-MZM, and the EO-frequency response of the MZM was simulated. For frequencies higher than 12 GHz, the simulated EO-frequency response of the HCPW-MZM terminated with the OCT overlapped with the modulator terminated with perfect matched termination; this makes it a good candidate for K-band applications with a frequency range of 18-27 GHz. For the co-design approach and increasing the flexibility of the modulator's impedance at the input and termination interfaces, a tapered-CPS-MZM (TCPS) with different input and output waveguides, electrode width, and gaps is introduced. Simulations predicted 35 and 55 Ohm impedances at the front and end sides of the modulator. Furthermore, the measured electrical reflection of this modulator to the 50 Ohm load proved that this modulator has different input and output impedances. Thus, the TCPS-MZM of this work is a good candidate for co-design approaches when different input and output impedances are desired.

Then, we studied the building block of the three state-of-the-art electrical interconnect technologies. The electrical scattering parameters of the stud-bump and TPV interconnects are simulated and compared with the wire-bond interconnect available in the advanced design system (ADS) simulation software. We showed that wire-bond with the lowest transmission and stud-bump has higher high-speed transmission than wire-bond but lower than TPV at high frequencies. For example, S21 of the 200 and 400 μm wire-bonds at 100 GHz are below -1.5 dB, while the two stud bumps and TPVs have transmissions above -0.35 dB at 100 GHz. Finally, we studied the effect of the electrical interconnects on the small and large signal responses of high-speed CPW and CPS modulators connected to the perfect termination and source. Small and large-signal simulation results show that wire-bond interconnects significantly reduce the EO-bandwidth and optical eye quality of both CPW and CPS modulators. In contrast, stud-bump and TPV impact on the responses of those modulators is minimal. Since stud-bump has dimensions in the order of a few 10-microns, for interconnecting the high-density devices with stud-bump, pads and tapers are required; therefore, they can not be used for wafer-scale co-integration of the high-density photonic modulators discussed in this thesis to the electronic ICs. Thus in this thesis, we conclude that for the high-density and high-speed wafer-scale co-integration of the co-designed PICs and EICs in the applications such as transceivers of the optical data centers, TPVs studied in this work can be a promising solution.

7.4 Outlook

In this thesis, we have reported a design study for the high-speed modulator building block, an environment for co-designing the high-speed photonic and electronic ICs, a device demonstration for high density and high-speed CPS-MZM modulators and technology developments for 3D high-density co-integration of photonic and electronic ICs. There is possible future work to be done to benefit more from the proposed concepts and methods. We discussed them in the previous chapters and can be summarized as follows.

1. Several improvements can be made to this work's two HCPW and CPS modulators to obtain higher performance. As we discussed in chapter 2 of this thesis, reducing the waveguide width, increasing the waveguide intrinsic layer thickness, and reducing the electrode width can significantly improve both impedance and velocity matching, reduce the electrical loss and increase the 3 dB electro-optical bandwidth of the HCPW-MZM. We proposed a parameter set for increasing the bandwidth of this modulator from 30 GHz to 120 GHz however, we could not make it with the current technology. Here we have the following suggestions.
    - Increasing the intrinsic layer thickness of phase modulators.
    - Reducing the signal electrode width to 2 μm, which requires technology development to make long and narrow metal electrodes.

    The proposed CPS modulator of this work has a high-density with a total width of 17 μm. The gap between the two electrodes of the reported modulator is 7 μm. Our simulation showed that reducing the electrode width and gap to 2 μm can increase

the density to even further with 6 μm. A short circuit between the two electrodes happened when we reduced the gap to 5 μm. Therefore, to increase the density of the CPS-MZM of this work, we propose technology developments for making long and narrow metal tracks with gaps smaller than 7 μm.
Moreover, in chapter 2 of this thesis, we discussed that the highest electrical loss is from the p-cladding layer of the phase modulator's p-i-n junction. NTT reduced this loss by changing to the n-i-p-n junction [14]. Applying this change can improve the performance of both HCPW and CPS modulator building blocks.

2. The wafer-bonding technology reported in a previous work [113] used the sloped sidewall gold connections between the electrical pads of the high-speed photonic and electronic devices. The pads' dimensions are in the order of 50-60 microns. To increase the density and speed, pads and taper connections to the photonic and electronic devices must be removed, and direct connections between the device electrodes must be made. For this reason, using the high-density and high-speed through polymer vias with steep side walls of this work will be an interesting research topic for the future.
3. Developments of the CPS modulators presented in chapter 4, which have leading-edge performance and characterization at higher frequencies (above 67 GHz).
4. High-density CPS-MZMs with less than 25 µm width are a promising candidate for designing a transmitter chip with more than 8×100 Gbaud.
5. The modulators presented in this thesis are intensity modulators and can be detected using NRZ-OOK modulation format. The co-design environment presented in this work can be used for utilizing higher-order modulation formats such as IQ and QPSK modulations.
6. High-density and high-speed on-chip terminations directly connected to the MZMs can reduce the packaging complexity, improve the bandwidth and increase the design flexibility of the transmitter circuits. We discussed that a broadband termination suitable for our modulators requires a capacitance higher than one micro-Farad. In the current InP generic platform, making a micro-Farad capacitance by the p-i-n junction requires a large 2000 $(mm)^2$ space. Here post-processing steps for adding high capacitors to the current generic platform are recommended. Creating envisage 3-D integrated capacitors by atomic layer deposition techniques can be a good direction for producing the required capacitance suitable for broadband and high-speed terminations.
7. To reduce the power consumption of the electro-optical modulation circuit as discussed in chapter 2, one way is to increase the termination impedance. The TCPS modulators introduce flexibility in the choice of termination impedance. Therefore, a TCPS-MZM with matched input impedance to the electrical circuit and higher output impedance matched with a termination impedance can be an excellent topic for future work. This can reduce the power consumption without back reflection to the electrical circuits.

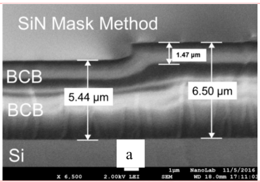
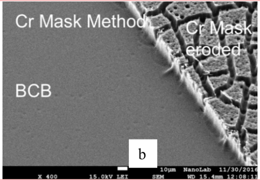
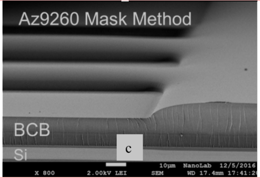
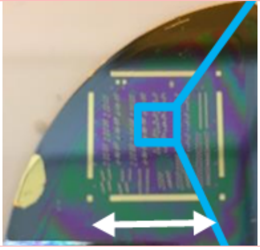
Many possible 3D-integration routes and important advances in performance shown in the simulations and prototypes, but now we need to look at the cost-benefit analysis and the yield aspects of 3D-integration to identify the methods best suited to manufacture.

"This book has ended, but the story is to be continued."

Appendix A

List of samples

The list of the samples in chapter 5 of this thesis is in table A.1.

Sample	**Description**	**Picture**
#1	Masking methods: Silicon nitride mask for etching BCB	
#2	Masking methods: Chromium mask nitride mask for etching BCB	
#3	Masking methods: AZ 9260 photoresist mask for etching BCB	
#4	Plated sloped TPV with sloped sidewall (1)	

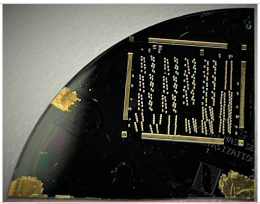
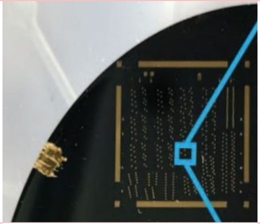
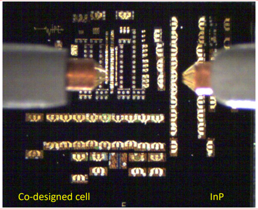
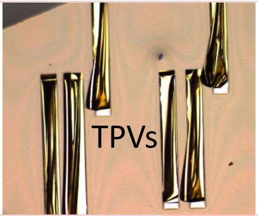
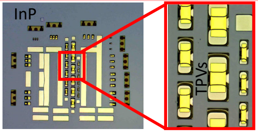
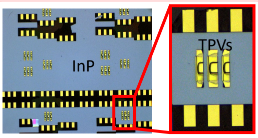
#5	Plated sloped TPV with sloped sidewall (2)	
#6	Plated sloped TPV with sloped sidewall (3)	
#7	Co-designed bonded InP and silicon cell with sloped sidewall TPVs	
#8	Steep sidewall TPVs: Ru-ALD seed-layer is plated after three weeks in ambient	
#9	Steep sidewall TPVs: Ru-ALD seed-layer is plated after three hours delay	
#10	Steep sidewall TPVs: Ru-ALD seed-layer is covered by 100 nm evaporated gold after an hour delay and then is plated	

Table A.1: Experimental samples of chapter 5

Bibliography

[1] "Cisco." [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html (Cited on page 1.)

[2] W. Ciciora, J. Farmer, D. Large, and M. Adams, "Chapter 12 - linear fiber-optic signal transportation," in *Modern Cable Television Technology*, 2nd ed., ser. The Morgan Kaufmann Series in Networking, W. Ciciora, J. Farmer, D. Large, and M. Adams, Eds. San Francisco: Morgan Kaufmann, 2004, pp. 509–557. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B978155860828350014X (Cited on page 1.)

[3] "IPSR photonic roadmap," 2020. [Online]. Available: https://photonicsmanufacturing.org/2020_iprs-i_roadmap_chapters (Cited on pages 1 and 72.)

[4] M. Smit, K. Williams, and J. van der Tol, "Past, present, and future of InP-based photonic integration," *APL Photonics*, vol. 4, no. 5, p. 050901, 2019. [Online]. Available: https://doi.org/10.1063/1.5087862 (Cited on page 2.)

[5] P. Bravetti, G. Ghislotti, and S. Balsamo, "Chirp-inducing mechanisms in Mach-Zehnder modulators and their effect on 10 Gb/s NRZ transmission studied using tunable-chirp single drive devices," *Journal of Lightwave Technology*, vol. 22, no. 2, pp. 605–611, 2004. (Cited on page 2.)

[6] F. Koyama and K. Iga, "Frequency chirping in external modulators," *Journal of Lightwave Technology*, vol. 6, no. 1, pp. 87–93, 1988. (Cited on page 2.)

[7] U. Koch, C. Uhl, H. Hettrich, Y. Fedoryshyn, C. Hoessbacher, W. Heni, B. Baeuerle, B. I. Bitachon, A. Josten, M. Ayata, H. Xu, D. L. Elder, L. R. Dalton, E. Mentovich, P. Bakopoulos, S. Lischke, A. Krüger, L. Zimmermann, D. Tsiokos, N. Pleros, M. Möller, and J. Leuthold, "A monolithic bipolar CMOS electronic–plasmonic high-speed transmitter," *Nature Electronics*, vol. 3, no. 6, pp. 338–345, 2020. (Cited on page 3.)

[8] J. Witzens, "High-Speed Silicon Photonics Modulators," *Proceedings of the IEEE*, vol. 106, no. 12, pp. 2158–2182, 2018. (Cited on page 3.)

[9] H. Zhu, L. Zhou, T. Wang, L. Liu, C. Wong, Y. Zhou, R. Yang, X. Li, and J. Chen, “Optimized silicon QPSK modulator with 64-Gb/s modulation speed,” *IEEE Photonics Journal*, vol. 7, no. 3, pp. 1–6, 2015. (Cited on pages 3 and 56.)

[10] J. Wang, L. Zhou, H. Zhu, R. Yang, Y. Zhou, L. Liu, T. Wang, and J. Chen, “Silicon high-speed binary phase-shift keying modulator with a single-drive push-pull high-speed traveling wave electrode,” *Photon. Res.*, vol. 3, no. 3, pp. 58–62, January 2015. [Online]. Available: http://www.osapublishing.org/prj/abstract.cfm?URI=prj-3-3-58 (Cited on pages 3 and 56.)

[11] P. Dong, L. Chen, and Y. kai Chen, “High-speed low-voltage single-drive push-pull silicon Mach-Zehnder modulators,” *Opt. Express*, vol. 20, no. 6, pp. 6163–6169, March 2012. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-20-6-6163 (Cited on pages 3 and 56.)

[12] H. Zhu, L. Zhou, L. Liu, T. Wang, Y. Zhou, J. Wang, Q. Wu, A. Xie, R. Yang, Z. Li, X. Li, and J. Chen, “Single-drive push-pull silicon Mach-Zehnder modulator for OOK and BPSK modulation,” in *2014 OptoElectronics and Communication Conference and Australian Conference on Optical Fibre Technology*, 2014, pp. 174–175. (Cited on pages 3 and 56.)

[13] S. Lange, S. Wolf, J. Lutz, L. Altenhain, R. Schmid, R. Kaiser, M. Schell, C. Koos, and S. Randel, “100 GBd intensity modulation and direct detection with an InP-based monolithic DFB laser Mach-Zehnder modulator,” *J. Lightwave Technol.*, vol. 36, no. 1, pp. 97–102, January 2018. [Online]. Available: p://jlt.osa.org/abstract.cfm?URI=jlt-36-1-97 (Cited on pages 4 and 56.)

[14] J. Ozaki, Y. Ogiso, and S. Nakano, “High-speed modulator for next-generation large-capacity coherent optical networks,” *NTT Technical Review*, vol. 16, no. 4, pp. 1–8, 2018. (Cited on pages 4, 37, 56, and 112.)

[15] M. Smit *et al.*, “An introduction to InP-based generic integration technology,” *Semiconductor Science and Technology*, vol. 29, no. 8, p. 083001, June 2014. (Cited on pages 3, 56, 57, and 66.)

[16] W. Yao, M. Smit, and M. Wale, “Design and simulation of a series push-pull Mach-Zehnder modulator in a generic photonic integration platform.” Proceedings of the 19th Annual Symposium of the IEEE Photonics Benelux Chapter, 3-4 November 2014, Enschede, The Netherlands, November 2014. (Cited on pages 3 and 56.)

[17] W. Yao, G. Gilardi, M. Smit, and M. Wale, “Equivalent circuit modelling of integrated travelingwave optical modulator in InP foundry platform.” Warsaw: European Conference On Integrated Optics, May 2016. (Cited on pages 3, 40, and 56.)

[18] R. Walker, “High-speed III-V semiconductor intensity modulators,” *IEEE Journal of Quantum Electronics*, vol. 27, no. 3, pp. 654–667, 1991. (Cited on pages 4, 22, and 56.)

[19] M. A. Meitl, Z. Zhu, V. Kumar, K. J. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, and J. A. Rogers, “Transfer printing by kinetic control of adhesion to an elastomeric stamp,” *Nature Materials*, vol. 5, no. 1, pp. 33–38, 2006. (Cited on pages 4 and 5.)

[20] R. Loi, J. O'Callaghan, B. Roycroft, A. J. Trindade, A. Fecioru, A. Farrell, S. Kelleher, R. F. Gul, S. Iadanza, L. O'Faolain, E. Pelucchi, B. Corbett, and D. Gomez, "Micro-transfer-printing of InP photonic devices to silicon photonics," in *2019 PhotonIcs Electromagnetics Research Symposium - Spring (PIERS-Spring)*, 2019, pp. 242–248. (Cited on pages 4 and 5.)

[21] M. Mack, A. Ayazi, Y. Chi, A. Dahl, P. D. Dobbelaere, S. Denton, S. Gloeckner, H. Kam-Yan, S. Hovey, Y. Liang, G. Masini, A. Mekis, M. Peterson, T. Pinguet, S. Sahni, J. Schramm, M. Sharp, C. Sohn, K. Stechschulte, P. Sun, G. Vastola, L. Verslegers, and R. Zhou, "Luxtera's silicon photonics platform for transceiver manufacturing." International Conference on Solid State Devices and Materials, 2014. (Cited on pages 4 and 5.)

[22] M. R. Billah, M. Blaicher, J. N. Kemal, T. Hoose, H. Zwickel, P.-I. Dietrich, U. Troppenz, M. Moehrle, F. Merget, A. Hofmann, J. Witzens, S. Randel, W. Freude, and C. Koos, "8-channel 448 gbit/s silicon photonic transmitter enabled by photonic wire bonding," in *2017 Optical Fiber Communications Conference and Exhibition (OFC)*, 2017, pp. 1–3. (Cited on pages 5 and 6.)

[23] Z. Zhou, B. Yin, and J. Michel, "On-chip light sources for silicon photonics," *Light: Science & Applications*, vol. 4, no. 11, pp. e358–e358, 2015. (Cited on page 6.)

[24] H. Reichl, "Technologien der mikrosysteme II." Research Center of Microperipheric Technologies, Technical University of Berlin, 2005. (Cited on pages 6 and 88.)

[25] T. Tekin, "Review of packaging of optoelectronic, photonic, and mems components," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 3, pp. 704–719, 2011. (Cited on pages 6, 7, and 88.)

[26] M. Trajkovic, "36 Gb/s operation of a BiCMOS driver and InP EAM using foundry platforms," *IET Conference Proceedings*, pp. 347 (3 pp.)–347 (3 pp.)(1), January 2019. [Online]. Available: https://digital-library.theiet.org/content/conferences/10.1049/cp.2019.1081 (Cited on pages 6, 7, and 88.)

[27] H. Oppermann, *Montage optisch-elektrischer Bauelemente*. Germany, Templin, 2002, p. 207. (Cited on page 7.)

[28] L. A. Coldren, S. C. Nicholes, L. Johansson, S. Ristic, R. S. Guzzon, E. J. Norberg, and U. Krishnamachari, "High performance InP-based photonic ICs—A tutorial," *Journal of Lightwave Technology*, vol. 29, no. 4, pp. 554–570, 2011. (Cited on page 7.)

[29] "Scifab: Joint lab InP devices," February 2008-2021. [Online]. Available: https://www.fbh-berlin.de/en/research/iii-v-electronics/inp-devices (Cited on pages 7, 8, and 72.)

[30] J. J. G. M. van der Tol, Y. Jiao, L. Shen, A. Millan-Mejia, V. Pogoretskii, J. P. van Engelen, and M. K. Smit, "Indium phosphide integrated photonics in membranes," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 1, pp. 1–9, 2018. (Cited on page 8.)

[31] J. J. G. M. van der Tol, Y. Jiao, J. P. Van Engelen, V. Pogoretskiy, A. A. Kashi, and K. Williams, “InP membrane on silicon (IMOS) photonics,” *IEEE Journal of Quantum Electronics*, vol. 56, no. 1, pp. 1–7, 2020. (Cited on page 8.)

[32] D. A. B. Miller, “Attojoule optoelectronics for low-energy information processing and communications,” *J. Lightwave Technol.*, vol. 35, no. 3, pp. 346–396, February 2017. (Cited on page 11.)

[33] G. Ghione, *Semiconductor Devices for High-Speed Optoelectronicss*. Cambridge, UK: Cambridge University Press, 2009. (Cited on pages 11, 16, 17, 18, 32, 39, 44, 45, and 57.)

[34] M. U. Sadiq, B. Roycroft, J. O’Callaghan, P. Morrissey, W. Han, F. H. Peters, and B. Corbett, “Efficient modelling approach for an InP based Mach-Zehnder modulator,” in *25th IET Irish Signals Systems Conference 2014 and 2014 China-Ireland International Conference on Information and Communications Technologies (ISSC 2014/CIICT 2014)*, 2014, pp. 123–128. (Cited on pages 12 and 40.)

[35] U. Rogge and R. Pregla, “Method of lines for the analysis of strip-loaded optical waveguides,” *J. Opt. Soc. Am. B*, vol. 8, no. 2, pp. 459–463, February 1991. (Cited on pages 12 and 40.)

[36] “CST Studio Suite, Dassault Systèmes.” [Online]. Available: https://www.3ds.com/products-services/simulia/products/cst-studio-suite/ (Cited on pages 12, 15, 47, 48, 78, 85, 89, and 107.)

[37] W. Yao, “Towards a high-capacity multi-channel transmitter in generic photonic integration technology.” Ph.D. dissertation, Eindhoven University of Technology, The Netherlands, 2016. (Cited on pages 15, 41, 57, 58, 60, 61, 63, and 65.)

[38] D. Pozar, *Microwave Engineering*, 4th ed. The Atrium-United Kingdom: John Wiley & Sons, 2012. (Cited on pages 19, 24, 27, 59, 60, and 98.)

[39] J. Besten, den, “Integration of multiwavelength lasers with fast electro-optical modulators,” Ph.D. dissertation, Electrical Engineering, 2004. (Cited on pages 21, 22, 27, and 36.)

[40] Y. Ogiso and J. Ozaki, “80-GHz bandwidth and 1.5-V Vπ InP-based IQ modulator,” *J. Lightwave Technol.*, vol. 38, no. 2, pp. 249–255, January 2020. [Online]. Available: http://jlt.osa.org/abstract.cfm?URI=jlt-38-2-249 (Cited on page 39.)

[41] R. A. Griffin, N. D. Whitbread, S. K. Jones, S. C. Heck, P. Firth, D. Govan, and T. Goodall, “InP coherent optical modulator with integrated amplification for high capacity transmission,” in *Optical Fiber Communication Conference*. Optical Society of America, 2015, p. Th4E.2. [Online]. Available: http://www.osapublishing.org/abstract.cfm?URI=OFC-2015-Th4E.2 (Cited on page 39.)

[42] G. E. Hoefler, Y. Zhou, M. Anagnosti, A. Bhardwaj, P. Abolghasem, A. James, S. Luna, P. Debackere, A. Dentai, T. Vallaitis, P. Liu, M. Missey, S. Corzine, P. Evans, V. Lal, M. Ziari, D. Welch, F. Kish, J. S. Suelzer, P. S. Devgan, and N. G. Usechak, “Foundry development of system-on-chip InP-based photonic integrated circuits,”

IEEE Journal of Selected Topics in Quantum Electronics, vol. 25, no. 5, pp. 1–17, 2019. (Cited on page 39.)

[43] R. A. Griffin, "InP-based high-speed transponder," in *Optical Fiber Communication Conference*. Optical Society of America, 2014, p. W3B.7. [Online]. Available: http://www.osapublishing.org/abstract.cfm?URI=OFC-2014-W3B.7 (Cited on page 39.)

[44] Y. Ogiso, J. Ozaki, Y. Ueda, H. Wakita, M. Nagatani, H. Yamazaki, M. Nakamura, T. Kobayashi, S. Kanazawa, T. Fujii, Y. Hashizume, H. Tanobe, N. Nunoya, M. Ida, Y. Miyamoto, and M. Ishikawa, "Ultra-high bandwidth InP IQ modulator for beyond 100-GBd transmission," in *2019 Optical Fiber Communications Conference and Exhibition (OFC)*, 2019, pp. 1–3. (Cited on page 39.)

[45] Y. Ma, C. Williams, M. Ahmed, A. Elmoznine, D. Lim, Y. Liu, R. Shi, T. Huynh, J. Roman, A. Ahmed, L. Vera, Y. Chen, A. Horth, H. Guan, K. Padmaraju, M. Streshinsky, A. Novack, R. Sukkar, R. Younce, A. Rylyakov, D. Scordo, and M. Hochberg, "An all-silicon transmitter with co-designed modulator and dc-coupled driver," in *2019 Optical Fiber Communications Conference and Exhibition (OFC)*, 2019, pp. 1–3. (Cited on page 39.)

[46] M. Smit, K. Williams, and J. v. d. Tol, "Integration of photonics and electronics," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2019, pp. 29–34. (Cited on page 39.)

[47] G. K. Gopalakrishnan, W. K. Burns, R. W. McElhanon, C. H. Bulmer, and A. S. Greenblatt, "Performance and modeling of broadband LiNbO/sub 3/ traveling wave optical intensity modulators," *Journal of Lightwave Technology*, vol. 12, no. 10, pp. 1807–1819, 1994.

[48] G. L. Li, C. K. Sun, S. A. Pappert, W. X. Chen, and P. K. L. Yu, "Ultrahigh-speed traveling-wave electroabsorption modulator-design and analysis," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 7, pp. 1177–1183, 1999. (Cited on page 40.)

[49] W. Pascher, J. Besten, den, D. Caprioli, X. Leijtens, M. Smit, and R. Dijk, van, "Modelling and design of a travelling-wave electro-optic modulator on InP," *Optical and Quantum Electronics*, vol. 35, no. 4-5, pp. 453–464, 2003. (Cited on page 40.)

[50] J. Witzens, T. Baehr-Jones, and M. Hochberg, "Design of transmission line driven slot waveguide Mach-Zehnder interferometers and application to analog optical links," *Opt. Express*, vol. 18, no. 16, pp. 16 902–16 928, August 2010. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-18-16-16902 (Cited on page 40.)

[51] H. Bahrami, H. Sepehrian, C. S. Park, L. A. Rusch, and W. Shi, "Time-domain large-signal modeling of traveling-wave modulators on SOI," *Journal of Lightwave Technology*, vol. 34, no. 11, pp. 2812–2823, 2016. (Cited on page 40.)

[52] H. Yu and W. Bogaerts, "An equivalent circuit model of the traveling wave electrode for carrier-depletion-based silicon optical modulators," *Journal of Lightwave Technology*, vol. 30, no. 11, pp. 1602–1609, 2012. (Cited on page 40.)

[53] K. S. Giboney, M. J. W. Rodwell, and J. E. Bowers, “Traveling-wave photodetector design and measurements,” *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 2, no. 3, pp. 622–629, 1996. (Cited on pages 40, 43, and 57.)

[54] “Keysight technology,2009.” [Online]. Available: https://edadocs.software.keysight.com/display/ads2009/Using+LineCalc. (Cited on page 40.)

[55] D. Jager, “Slow-wave propagation along variable Schottky-contact microstrip line,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 24, no. 9, pp. 566–573, 1976. (Cited on page 43.)

[56] K. S. Giboney, “Travelling-wave photodetectors,” Ph.D. dissertation, University of California, Santa Barbara, USA, 1995. (Cited on page 43.)

[57] E. Chen and S. Y. Chou, “Characteristics of coplanar transmission lines on multilayer substrates: modeling and experiments,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 6, pp. 939–945, 1997. (Cited on pages 43 and 57.)

[58] R. Collin, *Foundations for microwave engineering*. Wiley India Pvt. Limited, 2007. [Online]. Available: https://books.google.nl/books?id=coBpP2SLiZQC (Cited on page 44.)

[59] O. Paul and L. Paul, *Loop and Partial Inductance*, 1st ed. Hoboken, New Jersey: A John Wiley & Sons, 2010. (Cited on pages 44 and 57.)

[60] A. Das and S. K. Das, *Microwave engineering*. New Delhi: Tata McGraw-Hill Pub, 2000. (Cited on page 44.)

[61] T. K. Sarkar, R. Mailloux, A. A. Oliner, M. Salazar-Palma, and D. L. Sengupta, *The Evolution of Electromagnetic Waveguides: From Hollow Metallic Guides to Microwave Integrated Circuits*, 2006, pp. 543–566. (Cited on page 44.)

[62] J.-F. Vinchant, J. Cavailles, M. Erman, P. Jarry, and M. Renaud, “InP/GaInAsP guided-wave phase modulators based on carrier-induced effects: theory and experiment,” *Journal of Lightwave Technology*, vol. 10, no. 1, pp. 63–70, 1992. (Cited on page 45.)

[63] S. Adachi, *Properties of Semiconductor Alloys:Group-IV, III–V and II–VI Semiconductors*, 1st ed. The Atrium-United Kingdom: John Wiley & Sons, 2009. (Cited on page 45.)

[64] L. Keldysh, “The effect of a strong electric field on the optical properties of insulating crystals,” *Journal of Experimental and Theoretical Physicss*, vol. 7, no. 5, pp. 788–790, 1957. (Cited on page 45.)

[65] “JePPIX.” [Online]. Available: https://www.jeppix.eu (Cited on pages 47, 61, 99, and 109.)

[66] Y. Zhou, L. Zhou, H. Zhu, C. Wong, Y. Wen, L. Liu, X. Li, and J. Chen, “Modeling and optimization of a single-drive push-pull silicon Mach-Zehnder modulator,” *Photon. Res.*, vol. 4, no. 4, pp. 153–161, August 2016. [Online]. Available: http://www.osapublishing.org/prj/abstract.cfm?URI=prj-4-4-153 (Cited on page 56.)

[67] S. Y. Wang, S. H. Lin, and Y. M. Houng, "GaAs traveling-wave polarization electro-optic waveguide modulator with bandwidth in excess of 20 GHz at 1.3 μm," *Appl. Phys. Lett*, vol. 51, no. 83, pp. 83–85, 1998. (Cited on page 56.)

[68] W. Yao, M. K. Smit, and M. J. Wale, "Monolithic 300 Gb/s parallel transmitter in InP-based generic photonic integration technology," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 1, pp. 1–11, 2018. (Cited on page 71.)

[69] R. Maher, K. Croussore, M. Lauermann, R. Going, X. Xu, and J. Rahn, "Constellation shaped 66 GBd DP-1024 QAM transceiver with 400 km transmission over standard SMF," in *2017 European Conference on Optical Communication (ECOC)*, 2017, pp. 1–3. (Cited on page 71.)

[70] R. A. Griffin, S. K. Jones, N. Whitbread, S. C. Heck, and L. N. Langley, "InP Mach–Zehnder modulator platform for 10/40/100/200-Gb/s operation," *IEEE Journal of Selected Topics in Quantum Electronics*. (Cited on page 71.)

[71] R. Going, M. Lauermann, R. Maher, H. Tsai, M. Lu, N. Kim, S. Corzine, P. Studenkov, J. Summers, A. Hosseini, J. Zhang, B. Behnia, J. Tang, S. Buggaveeti, T. Vallaitis, J. Osenbach, M. Kuntz, X. Xu, K. Croussore, V. Lal, P. Evans, J. Rahn, T. Butrie, A. Karanicolas, K.-T. Wu, M. Mitchell, M. Ziari, D. Welch, and F. Kish, "Multi-channel InP-based coherent PICs with hybrid integrated SiGe electronics operating up to 100 GBd, 32QAM," in *2017 European Conference on Optical Communication (ECOC)*, 2017, pp. 1–3. (Cited on page 71.)

[72] K. Najafi, T. J. Harpster, H. Kim, J. S. Mitchell, W. C. Welch, and S. M. Karazi, "Wafer bonding," in *Reference Module in Materials Science and Materials Engineering*. Elsevier, 2016. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128035818005270 (Cited on page 72.)

[73] L. H. V. Vlack, *Wafer Bonding: Applications and Technology*, 1st ed. Springer, Berlin, Heidelberg, 2004. [Online]. Available: https://doi.org/10.1007/978-3-662-10827-7 (Cited on page 72.)

[74] M. Esashi, "Packaged sensors, microactuators and three-dimensional microfabrication," *Journal of Robotics and Mechatronics*, vol. 7, no. 3, pp. 200–203, 1995. (Cited on page 72.)

[75] U. Gösele, Q.-Y. Tong, A. Schumacher, G. Kräuter, M. Reiche, A. Plößl, P. Kopperschmidt, T.-H. Lee, and W.-J. Kim, "Wafer bonding for microsystems technologies," *Sensors and Actuators A: Physical*, vol. 74, no. 1, pp. 161–168, 1999. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0924424798003100 (Cited on page 72.)

[76] S. S. Iyer and A. A. J, *Silicon Wafer Bonding Technology: For VLSI and MEMS Applications*, 1st ed. Institution of Electrical Engineers, 2002. (Cited on page 72.)

[77] W. Ko, J. Suminto, and G. Yeh, *"Bonding techniques for microsensors," Micromachining and Micropackaging for Transducers*, 4th ed. The Atrium-United Kingdom: Elsevier Science Publishing Company Inc, 1985. (Cited on page 72.)

[78] K. Najafi, “Micropackaging technologies for integrated microsystems: applications to MEMS and MOEMS,” in *Micromachining and Microfabrication Process Technology VIII*, J. A. Yasaitis, M. A. Perez-Maher, and J. M. Karam, Eds., vol. 4979, International Society for Optics and Photonics. SPIE, 2003, pp. 1 – 19. [Online]. Available: https://doi.org/10.1117/12.484953 (Cited on page 72.)

[79] U. Biermann, A. van Gorkum, and J. Pals, “Direct bonding: From an optical technology to a broad research topic,” *Philips Journal of Research*, vol. 49, no. 1, pp. 1–10, 1995. [Online]. Available: https://www.sciencedirect.com/science/article/pii/0165581795820000 (Cited on page 72.)

[80] Q. Tong and U. Gösele, *SemiConductor Wafer Bonding: Science and Technology*, 1st ed. John Wiley Sons Inc., New York, 2002. (Cited on page 72.)

[81] M. Alexe, I. Radu, and I. Szafraniak, *Wafer Bonding of Ferroelectric Materials*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2004, pp. 451–471. [Online]. Available: https://doi.org/10.1007/978-3-662-10827-7_13 (Cited on page 72.)

[82] K. Kim, J. Kim, J. Kim, G. Hwang, C. Baek, and Y. Kim, “Packaging for RF MEMS devices using LTCC substrate and BCB adhesive layer,” *Journal of Micromechanics and Microengineering*, vol. 16, no. 1, pp. 150–156, December 2005. [Online]. Available: https://doi.org/10.1088/0960-1317/16/1/020 (Cited on page 72.)

[83] J. Iannacci, J. Tian, S. Sinaga, R. Gaddi, A. Gnudi, and M. Bartek, “Parasitic effects reduction for wafer-level packaging of RF-MEMS,” 2007. (Cited on pages 72 and 88.)

[84] M. Yokoyama, S. Kim, R. Zhang, N. Taoka, Y. Urabe, T. Maeda, H. Takagi, T. Yasuda, H. Yamada, O. Ichikawa, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, “III–V/Ge high mobility channel integration of InGaAs n-channel and Ge p-channel metal-oxide-semiconductor field-effect transistors with self-aligned Ni-based metal source/drain using direct wafer bonding,” *Applied Physics Express*, vol. 5, no. 7, p. 076501, 2012. (Cited on page 72.)

[85] X. Luo, Y. Cao, J. Song, X. Hu, Y. Cheng, C. Li, C. Liu, T. Liow, M. Yu, H. Wang, Q. J. Wang, and G. P. Lo, “High-throughput multiple dies-to-wafer bonding technology and III/V-on-Si hybrid lasers for heterogeneous integration of optoelectronic integrated circuits,” *Frontiers in Materials*, vol. 2, p. 28, 2015. [Online]. Available: https://www.frontiersin.org/article/10.3389/fmats.2015.00028 (Cited on page 72.)

[86] B. B. Bakir, A. Descos, N. Olivier, D. Bordel, P. Grosse, E. Augendre, L. Fulbert, and J. M. Fedeli, “Electrically driven hybrid Si/III-V Fabry-Pérot lasers based on adiabatic mode transformers,” *Opt. Express*, vol. 19, no. 11, pp. 10 317–10 325, May 2011. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-19-11-10317 (Cited on page 72.)

[87] P. Dong, T.-C. Hu, T.-Y. Liow, Y.-K. Chen, C. Xie, X. Luo, G.-Q. Lo, R. Kopf, and A. Tate, “Novel integration technique for silicon/III-V hybrid laser,” *Opt. Express*, vol. 22, no. 22, pp. 26 854–26 861, November 2014. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-22-22-26854 (Cited on page 72.)

[88] A. W. Fang, H. Park, Y. hao Kuo, R. Jones, O. Cohen, D. Liang, O. Raday, M. N. Sysak, M. J. Paniccia, and J. E. Bowers, “Hybrid silicon evanescent devices,” *Materials Today*, vol. 10, no. 7, pp. 28–35, 2007. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1369702107701773 (Cited on page 72.)

[89] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, “Electrically pumped hybrid AlGaInAs-silicon evanescent laser,” *Opt. Express*, vol. 14, no. 20, pp. 9203–9210, October 2006. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-14-20-9203 (Cited on page 72.)

[90] G. Kurczveil, M. J. R. Heck, J. D. Peters, J. M. Garcia, D. Spencer, and J. E. Bowers, “An integrated hybrid silicon multiwavelength AWG laser,” *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 6, pp. 1521–1527, 2011. (Cited on page 72.)

[91] G. Levaufre, A. Le Liepvre, C. Jany, A. Accard, P. Kaspar, R. Brenot, D. Make, F. Lelarge, G. H. Duan, S. Olivier, S. Malhouitre, C. Kopp, G. Simon, F. Saliou, and P. Chanclou, “Hybrid III-V/silicon tunable laser directly modulated at 10Gbit/s for short reach/access networks,” in *2014 The European Conference on Optical Communication (ECOC)*, 2014, pp. 1–3. (Cited on page 72.)

[92] D. Liang, A. W. Fang, C. Hui-Wen, M. N. Sysak, B. R. Koch, E. Lively, O. Raday, K. Ying-Hao, R. Jones, and J. E. Bowers, “Hybrid silicon evanescent approach to optical interconnects,” *Applied Physics A*, vol. 95, no. 4, pp. 1045–1057, 2009. (Cited on page 72.)

[93] D. Liang, M. Fiorentino, T. Okumura, H.-H. Chang, D. T. Spencer, Y.-H. Kuo, A. W. Fang, D. Dai, R. G. Beausoleil, and J. E. Bowers, “Electrically-pumped compact hybrid silicon microring lasers for optical interconnects,” *Opt. Express*, vol. 17, no. 22, pp. 20 355–20 364, Oct 2009. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-17-22-20355 (Cited on page 72.)

[94] D. Liang, G. Roelkens, R. Baets, and J. E. Bowers, “Hybrid integrated platforms for silicon photonics,” *Materials*, vol. 3, no. 3, pp. 1782–1802, 2010. [Online]. Available: https://www.mdpi.com/1996-1944/3/3/1782 (Cited on page 72.)

[95] D. Liang, S. Srinivasan, M. Fiorentino, G. Kurczveil, J. E. Bowers, and R. G. Beausoleil, “A metal thermal shunt design for hybrid silicon microring laser,” in *2012 Optical Interconnects Conference*, 2012, pp. 50–51. (Cited on page 72.)

[96] S. Stankovic, R. Jones, M. N. Sysak, J. M. Heck, G. Roelkens, and D. Van Thourhout, “1310-nm hybrid III–V/Si Fabry–Pérot laser based on adhesive bonding,” *IEEE Photonics Technology Letters*, vol. 23, no. 23, pp. 1781–1783, 2011. (Cited on page 72.)

[97] M. N. Sysak, D. Liang, R. Jones, G. Kurczveil, M. Piels, M. Fiorentino, R. G. Beausoleil, and J. E. Bowers, “Hybrid silicon laser technology: A thermal perspective,” *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 6, pp. 1490–1498, 2011. (Cited on page 72.)

[98] Y. hao Kuo, H. W. Chen, and J. E. Bowers, “High speed hybrid silicon evanescent electroabsorption modulator,” *Opt. Express*, vol. 16, no. 13, pp. 9936–9941,

June 2008. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-16-13-9936 (Cited on page 72.)

[99] L. Grenouillet, T. Dupont, P. Philippe, J. Harduin, N. Olivier, D. Bordel, E. Augendre, K. Gilbert, P. Grosse, A. Chelnokov, and J. M. Fedeli, "Hybrid integration for silicon photonics applications," *Optical and Quantum Electronics*, vol. 44, no. 12, pp. 527–534, 2012. (Cited on page 72.)

[100] J. K. Park, S. Takagi, and M. Takenaka, "InGaAsP Mach-Zehnder interferometer optical modulator monolithically integrated with InGaAs driver MOSFET on a III-V CMOS photonics platform," *Opt. Express*, vol. 26, no. 4, pp. 4842–4852, February 2018. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-26-4-4842 (Cited on page 72.)

[101] R. Jones, P. Doussiere, J. B. Driscoll, W. Lin, H. Yu, Y. Akulova, T. Komljenovic, and J. E. Bowers, "Heterogeneously integrated InP Silicon photonics: Fabricating fully functional transceivers," *IEEE Nanotechnology Magazine*, vol. 13, no. 2, pp. 17–26, 2019. (Cited on page 72.)

[102] "Waferscale integration of photonics and electronics (WIPE)," http://www.wipe.jeppix.eu/, May 2020. (Cited on page 73.)

[103] A. E. Mag-isa, B. Jang, J.-H. Kim, H.-J. Lee, and C.-S. Oh, "Coefficient of thermal expansion measurements for freestanding nanocrystalline ultra-thin gold films," *International Journal of Precision Engineering and Manufacturing*, vol. 15, no. 1, pp. 105–110, 2014. (Cited on page 77.)

[104] "Cyclotene 3000 series advanced electronic resins – processing procedures for cyclotene 3000 series dry etch resins," https://www.dupont.com/products/dryetch.html, 2021. (Cited on page 77.)

[105] "COMSOL Multiphysics reference manual, version 5.3." [Online]. Available: https://www.comsol.com/ (Cited on page 77.)

[106] E. F. Abdewi, "Mechanical properties of reinforcing steel rods produced by zliten steel factory," in *Reference Module in Materials Science and Materials Engineering*. Elsevier, 2017. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128035818103625 (Cited on page 77.)

[107] L. H. V. Vlack, *Materials for engineering : concepts and applications*, 1st ed. Addison-Wesley, 1982. (Cited on page 77.)

[108] B. C. P. H. D. Espinosa, "Size effects on the mechanical behavior of gold thin films. journal of materials," *Science*, vol. 38, no. 1, p. 4125–4128, 2003. [Online]. Available: https://doi.org/10.1023/A:1026321404286 (Cited on page 77.)

[109] ioffe.ru, "InP thermal properties," 2021. [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/InP/thermal.html (Cited on page 77.)

[110] ioffe.ru, "Silicon thermal properties," 2021. [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/Si/thermal.html (Cited on page 77.)

[111] X. Zhang, "Broadband driver amplifiers for electronic-photonic co-integration," Ph.D. dissertation, Electrical Engineering, 2019, proefschrift. (Cited on page 79.)

[112] B. Chen, X. Ye, B. Samaras, and J. Fan, "A novel de-embedding method suitable for transmission-line measurement," in *2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC)*, 2015, pp. 1–4. (Cited on pages 80, 82, and 85.)

[113] M. Spiegelberg, "3D-Integration on wafer level of photonic and electronic circuits," Ph.D. dissertation, Electrical Engineering, 2021, technische Universiteit Eindhoven. (Cited on pages 81, 109, and 112.)

[114] H. Cho and D. Burk, "A three-step method for the de-embedding of high-frequency s-parameter measurements," *IEEE Transactions on Electron Devices*, vol. 38, no. 6, pp. 1371–1375, 1991. (Cited on page 82.)

[115] J. Song, F. Ling, G. Flynn, W. Blood, and E. Demircan, "A de-embedding technique for interconnects," in *IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging (Cat. No. 01TH8565)*, 2001, pp. 129–132. (Cited on pages 82 and 85.)

[116] M. Knaut, M. Junige, V. Neumann, H. Wojcik, T. Henke, C. Hossbach, A. Hiess, M. Albert, and J. W. Bartha, "Atomic layer deposition for high aspect ratio through silicon vias," *Microelectronic Engineering*, vol. 107, pp. 80–83, 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0167931713000592 (Cited on page 83.)

[117] F. Inoue, H. Philipsen, A. Radisic, S. Armini, Y. Civale, P. Leunissen, M. Kondo, E. Webb, and S. Shingubara, "Electroless Cu deposition on deposited Ru as novel seed formation process in through-Si vias," *Electrochimica Acta*, vol. 100, pp. 203–211, 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0013468613005185 (Cited on page 83.)

[118] S. N. Chopra, M. F. J. Vos, M. A. Verheijen, J. G. Ekerdt, W. M. M. Kessels, and A. J. M. Mackus, "Atomic layer deposition of ruthenium using an ABC-type process: Role of oxygen exposure during nucleation," *Journal of Vacuum Science & Technology A*, vol. 38, no. 6, p. 062402, 2020. [Online]. Available: https://doi.org/10.1116/6.0000434 (Cited on page 83.)

[119] L. Guo, A. Radisic, and P. C. Searson, "Electrodeposition of Copper on Oxidized Ruthenium," *Journal of The Electrochemical Society*, vol. 153, no. 12, p. C840, 2006. [Online]. Available: https://doi.org/10.1149/1.2354454 (Cited on page 83.)

[120] P. Shi and J. Wu, "High density copper nucleation on ruthenium and its application to direct plating of advanced interconnects," *ECS Transactions*, vol. 52, no. 1, pp. 437–442, March 2013. [Online]. Available: https://doi.org/10.1149/05201.0437ecst (Cited on page 83.)

[121] L. F. Miller, "Controlled collapse reflow chip joining," *IBM Journal of Research and Development*, vol. 13, no. 3, pp. 239–250, 1969. (Cited on page 88.)

[122] M. Klein, H. Oppermann, R. Kalicki, R. Aschenbrenner, and H. Reichl, “Single chip bumping and reliability for flip chip processes,” *Microelectronics Reliability*, vol. 39, no. 9, pp. 1389–1397, 1999. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271499000670 (Cited on page 88.)

[123] W. Yao, G. Gilardi, M. Smit, and M. Wale, “Design and characterization of a broadband termination resistance integrated in a generic photonic foundry platform,” in *Proceedings of the 20th Annual Symposium of the IEEE Photonics Benelux Chapter, 26-27 November 2015, Brussels, Belgium*, 2015, pp. 63–66, due to safety threats in Brussels on November 26-27, 2015, the symposium was rescheduled on February 8-9, 2016; 20th Annual Symposium of the IEEE Photonics Benelux Chapter, November 26-27, 2015, Brussels, Belgium ; Conference date: 08-02-2016 Through 09-02-2016. [Online]. Available: http://www.photonics-benelux.org/symp15/ (Cited on pages 97 and 98.)

[124] W. Yao, G. Gilardi, D. D’Agostino, M. K. Smit, and M. J. Wale, *IEEE Photonics Technology Letters*. (Cited on page 100.)

[125] “EPO-TEK 301,” February 2021. [Online]. Available: https://www.epotek.com/docs/en/Datasheet/301.pdf (Cited on page 102.)

[126] A. Meighan, W. Yao, M. Wale, and K. A. Williams, “Microwave model for optimizing electro-optical modulation response of the Mach-Zehnder modulator.” Online: European Conference On Integrated Optics, June 2020. (Cited on pages 107 and 108.)

Acknowledgments

In the spring of 2016, I traveled to Eindhoven for a face-to-face interview. By observing the advanced laboratories and meeting people of different nationalities, I made an important decision. The decision was that if I am offered the Ph.D., to remain unbiased by my original opinion and knowledge and be open to learning as much as possible. By starting my Ph.D. in July 2016, I began the journey of implementing my decision. During my Ph.D. period, I learned a lot of professional techniques from experts, learned life skills from diverse cultures, and learned humanity lessons from different personalities. I tried to focus on the behaviors and conversations. If I had any doubts about a situation, I studied, read books, or consulted with colleagues or experts to confirm the information, and if I observed something wrong or inappropriate, I taught myself to avoid it. And now that I am writing this part of my doctoral dissertation in November 2021, I can say that I am significantly different from Arezou's version 2016. Here I would like to acknowledge a selection of people, moments, or places who taught me lessons, created valuable memories, and contributed to my 2021 version.

I came out of the cleanroom one day, excited to share my news. Although what I did was very small, maybe I was as excited as Galileo when he discovered gravity and Kepler when he discovered planetary motion. I went to his office to share with him that my experiment for creating vias was successful. "It's brilliant," he said. "Would you like to test them electrically?" Then we both went to the Nanolab to measure the IV curve of the vias. At the time of the measurement, all eyes were on us. Colleagues wondered what the group leader of PhI was doing in the lab. And this is just one example of hundreds of ways he supported me during my research. During approximately 300 hours of meetings with him, I learned the importance of discipline, order, patience, and documentation. Kevin, thank you so much for supporting my research and teaching me valuable skills.

I vividly remember the first day I officially started my Ph.D. It was a Friday, and I was very excited; an official man with a British accent introduced himself to me with a warm smile and offered me a cup of coffee. He is one of the most experienced scientists in my research field. During frequent meetings with him, I learned a lot; the most important was accuracy in research. Mike, thank you for teaching me to be precise in researching and presenting.

A critical point caught my attention as I was finalizing the writing of my thesis. On one of the first pages of the dissertation, a list of people had to be written right after the title and publisher information pages. Writing their names at the beginning of the thesis shows their great importance. Then I acknowledge my promoter (Kevin), my co-promoter (Mike) and the other members of my doctorate committee for evaluating the results of my research. Bart, I met you a few times at the coffee machine; your behavior is always very professional; thanks for accepting my doctorate defense chairman. Eugenio, I met you digitally at the last Photronics UC meeting; thanks for evaluating my Ph.D. thesis; I hope

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After my master's study, I was unsure about my Ph.D. interest topic, so I started teaching at the university and working for industrial companies. While researching fiber optic communication for the high-speed railway industry, I found an article about photonic integrated circuits. I said to myself, "Aha, this is a field I love to research." The author of that article was Meint Smith, who introduced the Photonic Integrated Circuits (PICs). Although Meint was very popular and busy and on the verge of retirement, he always made time for students interested in discussing the topic. The most important thing I learned from Meint is to look at the big picture of the research and, more importantly, be humble. Thanks, Meint, for teaching me life and technical lessons and opening my eyes to the photonics world.

At the beginning of my Ph.D., I was informed of a European project called WIPE, which was very similar in technology to my Ph.D. project, and I was asked to collaborate on it. An experienced and professional Dutchman was the leader of the WIPE project. He always listened patiently to discussions, was insightful, and was very experienced in the fabrication of PICs. Working with him was very heartwarming and instructive. I learned a lot from him, the most important of which was trust and respect for the opinions of less experienced researchers. Thank you, Jos, for all the valuable things you have taught me.

During my childhood, I was interested in teaching and transferring my knowledge to others. I first tried teaching when I was about four years old. I placed my dolls in a classroom and taught them how to dress. Although my first students did not react to my ordinary tutorials, I did not give up. I later insisted on teaching things to my younger sister. One day, during my Ph.D., I expressed my interest in teaching. A friendly Dutchman and one of the experienced teachers of our group proposed to me to teach lab measurements to his students. Xaveer, thank you so much for giving me the opportunity to experience teaching during my Ph.D.

About six months after starting my Ph.D., my first measurement proved that technology development for making through polymer vias (TPVs) was successful. However, I wanted to measure the resistance of the TPVs. The measurement setup looked very complicated. My colleagues suggested I discuss this with one of the most technical people in our group. He, a professional, punctual, Dutch gentleman, kindly described the measurement setup step by step and asked me to repeat the steps. Then he gave me some files for more details and asked me about my measurement plan. Later, I was in the middle of the measurement when he surprisingly came to check if everything was fine and if I had any questions. Erwin, thank you so much for showing me so many lab skills and, on top of that, teaching me step-by-step support.

Many colleagues already knew him because he had received his doctorate degree in our group. After experiencing research in two other countries during the lock-down period, he returned to our group with extensive experience. When the university was opened with limited access, we had to have a buddy for working. Unlike most Dutch people, he worked late. Therefore, the days he was at the university, I was able to measure until late. In addition, when I was writing my thesis, he often gave me very friendly advice on writing. Martijn, thank you so much for constructive discussions and for sharing your writing experience.

The first time we met was during the peer discussion on my interview date; she kindly answered my questions. We became close friends right after I started my Ph.D., attending dance classes together, traveling, and talking for hours. We became so close that our friends called us "BFFs" (best friends forever). My beautiful and intelligent Chinese BFF, Dan, thank you for all the support you have given me during our deep friendship. Delicious Chinese food for the second chapter of my thesis, a weekend trip to the brewery for the third chapter, the beautiful dress you gave me in Ibiza for chapter four, etc., made me think I could have more chapters in my thesis. Dandan, if someone asks me what the criteria of a BFF are, I just need to list your characteristics. I hope that our friendship will be as long and beautiful as the silk road that connects our home countries.

Unfortunately, the last months of my Ph.D. coincided with the coronavirus pandemic, when my Photonic ICs were ready to be measured. That is why my experienced colleagues were not at the university most of the time when I was measuring. One day when I had a lot of errors in the measurement, I called one of my experienced colleagues. He was working from home and tried to solve the problems remotely but failed. After half an hour had passed, I heard the voice of a humble Belarusian colleague, who had cycled for about 20 minutes to come and solve the issue. Dima, thank you very much for your humble help in coding and solving complex measurement problems. You have been my angel of salvation many times.

One of the most expensive measurement setups in our laboratory is the RF setup. Working with it requires experience and confidence. Breaking any part of the measuring setup can lead to substantial financial and time costs. The first time I wanted to measure my high-speed coplanar strip-line modulators, I had a lot of stress and excitement and needed step-by-step approval from an expert to avoid making a mistake. For this purpose, who was better than the designer of the high-speed electro-absorption modulators in our group? She is a talented, confident, and strong Serbian girl. She often advised me online or in-person while I was measuring. My beautiful friend, Marija, thank you for being by my side in the hardships of life and work.

I have been interested in traveling since I was a child. Sometimes I traveled to the thoughts of different authors by reading books, and sometimes I traveled far and near with my family or relatives and later alone. When I came to Eindhoven, I continued traveling. Geographic location and Eindhoven Airport are great for long weekend trips. For instance, I traveled to France five times. France offered tasty foods, fresh Champagne, and, more importantly, a French friend. My friend, Florian, thank you so much for frequently helping me during our five-year friendship. I will never forget when you realized that my productivity at home was low during the lock-down and generously shared your home desk with me.

The first party that I joined in Eindhoven was the birthday party of a very warmhearted colleague. There I ate homemade guacamole for the first time, and I danced and drank sangria with friends. Although he graduated a year later, we kept our friendship and became colleagues again ten months ago. During the coronavirus quarantine, when we were allowed limited contact with people, he and his girlfriend suggested that we have dinner together on Wednesdays so that I would not feel alone. Their offer was precious. My dear Mexican friend, Alonso, thank you and your beautiful Belgian girlfriend Barbara for reminding me of humanity. I look forward to the birth and embrace of your son.

I like and enjoy eating quality foods. While her boyfriend was working in Germany, my kind and beautiful friend invited me to a girl party and cooked Enchilada. The taste was unbelievable. Later, when I went to Mexico to attend their wonderful wedding, I became increasingly interested in Mexican food, culture, and, more importantly, Mexican people.

My dear friends, Aura and Victor, thank you for inviting me to your beautiful country.

One of the best scientific trips during my Ph.D. was traveling to Japan for the CSW conference. I went there with Yuqing, Jorn, and Vadim from our group. While drinking Japanese sake, we enjoyed a lot of scientific discussions! Jorn had the experience of living in Japan during his master's internship. He kindly showed me the best places in Kyoto and suggested lovely cities to visit for the rest of my trip. Thanks, Jorn, Yuqing, and Vadim, for making incredible memories during our trip to Japan. By the way, I am a fan of your cute daughter, Yuqing; I wish her health and happiness together with you and your beautiful wife.

I am usually curious about the experimental results of the theories. Therefore, one of the best experiences in my Ph.D. program was working in the cleanroom. I still remember the excitement I had for my first experiment in the Nanolab. Many thanks, Barry, Eric Jan, Huub, Robert, and Jeroen, for teaching me processing. Your advice helped me to have successful results. Tjibbe, you helped and encouraged me so many times in processing 3D vias; thank you so much. I also enjoy testing the experiments. Thanks, Sylwester, for helping me with my measurement setup during the lockdown. Rui, thanks for your tips in the lab. Michalis, thank you for making nice and quick wire-bond assemblies.

Scientific work is challenging and energy-consuming. Therefore, it is good to have breaks from time to time to distract the mind. Our group's social, beautiful, and professional secretary was a master of organizing social events; even during the lock-down, she often organized online activities. I always enjoyed discussing with her. Thank you so much, Jolande, for the nice chats and for organizing great social activities.

One of the opportunities I had in my Ph.D. research was working with researchers from other groups or departments in our university. For example, in the Photronics and WIPE projects, I worked with Marion, Xi, and Xiao in the IC group; I also worked with Erwin Kessel and Martijn from the PMP group. Thank you so much for your constructive collaborations. I thank our neighbor colleagues in the ECO group, such as Nickola, Hung, and Chigo, for their nice chats during the coffee breaks and for generously loaning their lab tools. I thank Chenhui for helping me with plating. I also thank the PSN group for sharing their COMSOL license with me.

I would like to thank Valeria, Longfei, Marc, and Perry, who are the previous Ph.D. students of our group, for sharing their experience and knowledge with me. I wish David, Tasfia, Salim, Vikram, Lukas, Jasper, Bernat, Ekaterina, Kolsoom, Rui, and Yi luck finishing your Ph.D. Rachel, we discussed a lot of movies during lunchtime; maybe it is a good idea to watch a movie together one of these days. Sander, Wenjing, and Joel, it was nice measuring in the lab when you have been around. Manuel, we started our Ph.D. on the same day; I hope you can finish soon. Marco, my avocado plants are almost dying, but yours are growing; you have green hands. Ozan, I like your research for coherent quantum communication; good luck with Alice and Bob. Rastko, you drive very smoothly even in the Mexican detours; good luck with the last steps of your Ph.D. Katia, thanks for the nice discussions about your MBA program. I hope you enjoy watching and feeling the happiness and health of your handsome son. Stacey, Akanksha, Daan, Tim, I always enjoyed conversations with you during the coffee and lunch breaks. Irene, I wish you good luck with your new job position in PhI. I would also like to thank the facility service and reception of the Flux building, which supported my research by maintaining a clean and pleasant environment.

At the defense dinner party of a friend, he was sitting at the dinner table, almost in front of me. He offered me to join their company after finishing my Ph.D. Suddenly, one of the people at the dinner table said: "But Arezou cannot travel to many countries with her Iranian passport." Everyone was silent for a moment; then he broke the silence and said, "Her passport is sufficient for traveling from her home to our company and cleanroom." His name is Luc, the CTO of SMART Photonics. Luc, thank you so much for supporting me, especially in writing my thesis while working at SMART. I also thank my other colleagues at SMART. Thanks, Ruud, for straightforward and smooth communication and for giving me the flexibility of working time and location while I was writing my thesis. Peter Thijs, it was my pleasure to discuss all of your brilliant discoveries in lasers behavior in the presence and absence of strain. Govert, thanks for taking care of the fabrication of my tiny modulators. Steven, it was nice to discuss the challenges of MQWs with you. Erik, thanks for your nice tips on designing chips during my Ph.D. at TU/e and for the helpful measurement discussions during my work period at SMART. Madeleine, I admire your cleanroom skills, and I wish you many more successful results. Stefanos, it is nice that we are working in the same place again. Daniel, thank you so much for secretly sending my modulator work to the "Inspiring Fifty Deep Tech Benelux+ Award"; I am nominated. Angel, it was great discussing the processing steps with you. I enjoyed my solo adventure trip to your beautiful country. John, thanks for the generous tour that you offered me in our cleanroom. Paul, I hope you find and buy a nice house soon. Frank, I admire your early-rising habit and your smiling face even at 7:30 a.m. Yichen, I wish you success at ASML. Alessia, I hope you have a smooth baby delivery. Pim and Andrea, good luck with your Ph.D. John McGurk, good luck with finding a flat in Eindhoven. Andrej, I wish you good luck with your career at SMART. Thanks, Yvonne, for constantly improving the quality of HR services. Thanks, Peter Top, for the quick and efficient IT support.

I was about nine and a half years old, and it was a beautiful spring day. I was his princess, and he was my king, and we lived in our small castle. My two younger sisters were playing, and I was helping my mother, who had inadvertently become pregnant again. He kissed us, said goodbye, left, and never came back. Although we only spent a few years together, I learned a lot from him. Dad, thanks for creating fantastic memories and for teaching me problem-solving tricks in your small lab. Your voice came to my mind so many times these years saying, "My little princess, first try to find the best solution. The best solution is not always the first one; neither is the easiest one. If you could not find a solution, move on and create your own solution, your unique solution that involves your mind's fingerprint," I confess that still, I rush to find my own solutions. Dad, I am working on getting a Ph.D. as I promised.

Losing my father in the car accident destroyed our castle, and all the colors turned to gray. My father called her "the Desert Queen," and she was our castle's brave, open-minded, and beautiful queen. She said, "I need your help, Arie[1]. Let's bring happiness back to our family and live in a way that makes your father proud of us." From that day on, I became her assistant. To mention what I learned from her during my assistantship, I would have to write several books. So, here I am referring to only one of the most important teachings she taught me. She frequently told me, "Respect your gender, listen to the signs coming from your nature, and turn your tough professional life into a beautiful feminine utopia." While I have high heels on and my nails are polished in autumn colors, I thank my mother for all the motivation and support she has given me throughout my life, especially during my Ph.D. Mom, I enjoyed reading and discussing together the books you suggested during the lock-down; let's start reading the second book of Yuval Noah Harari right after my Ph.D. defense.

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[1] Arezou is my official name, Arie is my nickname, and my family and friends call me Arie. So, dear reader of my thesis, please feel free to call me Arie.

One of the pleasures of my childhood was her laughing so that I could watch her dimpled cheeks. At the beginning of her master's program in agriculture engineering, she married her dimpled cheeks husband, and now they have two dimpled cheeks daughters. Dear Narges, thank you so much for all your support and kindness. And most importantly, thank you for giving me two beautiful nieces, Benita and Nila. Beni, I'm so glad you could manage to get the blue Taekwondo belt during the lock-down, and I hope you get your black belt soon. Nili, I can't wait to hug and kiss you for the first time. I wish you to shine and blossom.

With her birth, she expanded the range of colors in our family. Later she became an industrial designer. Her name is written on the second page of my thesis as a cover designer. My beautiful sister, Negar, thank you for all your excellent advice and for designing my dissertation cover during your busy schedule.

He is the phoenix of our family. Although he has not seen our father, many of his behaviors are similar to our father. When he was five years old, he asked me to bring him something from his drawer. Everything was sorted so nicely and precisely that it made me stare at it for a few seconds. From that day on, I often asked for his advice in sorting my objects and, more importantly, my thoughts. Thank you very much, my dear brother, for supporting me during my Ph.D. I wish you all the best in studying electrical engineering.

I was born and raised in the metropolis of Tehran. A beautiful, sunny city with four seasons, but very busy. For this reason, we often went to the northern cities along the Caspian Sea for short vacations. The climate of the northern cities was usually cold, cloudy, and rainy, with a hint of dew. And it's so much like the climate of the country where I did my Ph.D. It is a beautiful and flat country with kind, open-minded and punctual people. The Netherlands, thank you for being a good host for more than five years. I am also very grateful to the Dutch people who answered my questions openly and respected my thoughts and opinions. And thanks to my Dutch neighbors asking me to join their Christmas parties and encouraging me by calling me "smart" and "hard worker" when seeing me come home late from the university.

It is beautiful, vast, and historical, where the first seeds of knowledge were sown in me. Many of the first ones, such as the first animation and beer, are found in it. Its Damavand mountain faces the sky, and its Persian Gulf is the color of the sky. Its people are as warm as the summer days of its deserts, and its ethnicities are as diverse as its forests. There, knowledge is appreciated, and scientists are highly respected. My dear homeland, Iran, thank you for nurturing me in your cradle of knowledge, and also thank your men and women, who praised the independence of my mother, me, and my sisters and called us lionesses. I can't wait to see you.

Finally, I thank you, dear reader, for taking the time to turn the pages of my five years of scientific experience. I hope the small drop I gave to the endless sea of knowledge will be helpful for you and the future. And here, I end this section with a selection of poems by the Persian poet, Sohrab Sepehri, as follows:

"It does not matter where I am.
The sky is always mine.
Windows, ideas, air, love, earth, all mine.
Why does it matter if sometimes,
the mushrooms of nostalgia grow?"

Arezou (Arie) Meighan
Eindhoven, November 2021

Curriculum Vitae

Arezou Meighan was born in 1986 in Tehran, Iran. She received an M.Sc. degree in nano-electronic engineering from the University of Tabriz in 2010. Her master's research was on spin-based quantum information. Then she moved to the University of Applied Science and Technology and later to the Azad University of Tehran as a part-time lecturer in the electrical engineering department. Besides academia, she worked as an R&D engineer in the smart home industry and as a project manager in the railway industry. In July 2016, she started her Ph.D. research in the Photonic Integration group (PhI) at Eindhoven University of Technology (TU/e) in the Netherlands. Her work focuses on co-design and co-integration of the high-speed and high-density photonic and electronic integrated circuits. The results of this research are presented in this thesis. As of January 2021, she is working in the R&D department of SMART Photonics.

Publications and Patents

Publications

A. Meighan, M. J. Wale and K. Williams, *"High-Density 100 GHz-Class Mach-Zehnder Modulators integrated in a InP Generic Foundry Platform"*, OFC, 2022, **Submitted**.

A. Meighan, M. J. Wale and K. Williams, *"Electrical modeling of co-designed high-speed indium-phosphide Mach Zehnder modulator"*, in Journal of Lightwave Technology, 2021, **submitted**.

A. Meighan, M. J. Wale and K. Williams, "Waveguide width effect on increasing the Mach-Zehnder Modulators bandwidth", Benelux Symposium 2021, **Accepted**.

B. S. Vikram, **A. Meighan** , K.A. Williams1, and V. Dolores-Calzadilla1, *"Towards implementation of FMCW LiDAR with quadrature modulator architectures in generic InP photonic integration technology"*, Benelux Symposium 2021, **Accepted**.

A. Meighan, M. J. Wale and K. Williams, *"High-Density Coplanar Strip-Line Mach-Zehnder Modulators in a InP Generic Platform"*, in ECOC, Bordeaux, Sep. 2021.

W. Yao, X. Liu, M. K. Matters-Kammerer, **A. Meighan**, M. Spiegelberg, M. Trajkovic, J.J.G.M. Van der Tol, M. J. Wale, X. Zhang and K. Williams, *"Towards the Integration of InP Photonics With Silicon Electronics: Design and Technology Challenges,"* in Journal of Lightwave Technology, vol. 39, no. 4, pp. 999-1009, 15 Feb.15, 2021.

A. Meighan, Y. Yao, M. J. Wale and K. Williams, *"Design of 100 GHz-class Mach-Zehnder modulators in a generic indium phosphide platform"*, in IPC, Vancouver, BC, Canada, 2020.

A. Meighan, W. Yao, M. J. Wale and K. Williams, *"Microwave model for optimizing electro-optical modulation response of the Mach-Zehnder modulator"*, in ECIO, Online, 2020.

K. Williams, X. Liu, M. K. Matters-Kammerer, **A. Meighan**, M. Spiegelberg, M. Trajkovic, J. J. G. M. v. d. Tol, M. J. Wale, W. Yao and X. Zhang, *"Indium Phosphide Photonic Circuits on Silicon Electronics"*, in OFC, San Diego, 2020.

X. Zhang, X. Liu, M. Spiegelberg, **A. Meighan**, J. J. van der Tol and M. K. Matters-

Kammerer, *"A 50 Gb/s PAM-4 Optical Modulator Driver for 3D Photonic Electronic Wafer Scale Packaging"*, in MMS, Istanbul, Turkey, 31 Oct.-2 Nov. 2018.

A. Meighan, M. Wale, T. de Vries, E. Smalbrugge and K. Williams, *"Low resistance metal interconnection for direct wafer bonding of electronic to photonic ICs"* in 22nd Annual Symposium of the IEEE Photonics Society Benelux Chapter, Delft, 2017.

Patents

The design of the high-density and high-speed CPS modulators has been filed in an International Patent, *"Electro-Optical Modulator"*, Inventor: A. Meighan, Application No PCT/EP2021/075258.

The design of the Tapered MZMs with different input and output impedance has been filed in a UK Patent, *"Electro-Optical Modulator"*, Inventor: A. Meighan, Application No 2116110.4.