An E-Band SiGe High Efficiency, High Harmonic Suppression Amplifier Multiplier Chain With Wide Temperature Operating Range

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***Abstract*— This paper presents a monolithically integrated E-band amplifier multiplier chain (AMC) developed in 130 nm SiGe BiCMOS process. This E-band AMC is composed of a 25 GHz 1:1 power divider, two 25 GHz driver amplifiers ($DA_{1,2}$), a 75 GHz passive frequency tripler, and a 75 GHz power amplifier (PA). By applying a bypass tuning capacitor based power enhancing technique in the single-ended DA and PA, the output power and power-added-efficiency (PAE) of the AMC have been effectively improved. Benefiting from the proposed passive tripler core with second harmonic suppression function, and the impedance matching network with frequency selection characteristics, the AMC presents better harmonic suppression performance compared with the conventional topology. The bias circuits with temperature compensation are applied to the DA and PA to ensure the performance of the AMC when the temperature changes. The AMC has a measured output power exceeding 0 dBm in the entire E-band frequency range with a peak output power of 10.9 dBm at 77 GHz, and exhibits a record PAE of 8.25 %. Within the 3 dB operating frequency range from 69 to 87 GHz, the rejection of fundamental and second harmonics are better than 33.5 dB. The AMC can work properly between −40 °C and 125 °C with the proposed temperature compensation bias circuits.**

***Index Terms*— Amplifier multiplier chain, E-band, high efficiency, mm-Wave, SiGe, temperature.**

I. Introduction

IN RECENT years, with the gradual commercial application of 5G communication, research on various key technologies for B5G and 6G has been carried out in full swing. The millimeter wave (30-300 GHz) frequency band has become an important spectrum resource for future ultra-high-speed wireless communication applications due to its unique characteristics such as wide bandwidth, narrow beam, high reliability, and short wavelength [1]. Allocated by the federal communications commission (FCC) [2] and the confederation of European posts and telecommunications (CEPT) [3], the E-band (60-90 GHz) has been widely applied in point-to-point communications (71-76 GHz and 81-86 GHz) to enable multi-Gb/s wireless applications like mobile back-haul and small cell [4]. The E-band also has been extensively used in video transmission, wireless local area networks (WLAN) and 77 GHz frequency-modulated-continuous-wave (FMCW) radar sensors [5].

For these applications, a signal source with a wide output frequency tuning range, high output power, high efficiency, low phase noise and wide temperature operating range is one of the most essential component. In a multi-channel communication system, such a high-performance signal is needed to provide the local oscillator (LO), and in a multi-channel radar system, such a high-performance continuous wave signal generating unit is also necessary. However, the parasitic effects caused by the E-band layout connection will greatly deteriorate the output frequency tuning range and the phase noise of an E-band voltage controlled oscillator (VCO) [6]–[8]. Besides, it is challenging to design a broadband frequency divider chain in an E-band phase-locked loop (PLL) for E-band VCO output frequency locking. Meanwhile, such divider chain is power hungry [9], which in turn leads to low DC-to-RF conversion efficiency of the E-band signal source. In addition, whether it is an E-band communication or radar systems, in practical applications, the system needs to have better performance as the ambient temperature changes. However, there are few reported E-band signal sources designed with high and low temperature characteristics so far.

Alternatively, the combination of a low frequency signal source or a low frequency PLL with AMC to achieve the desired E-band signal source has been widely adopted to relax the performance specifications [10]–[14]. But, the AMC, which has many unwanted harmonics, would create multiple intermodulation products into the desired frequency band and distort the useful signal in the systems, especially for the communication systems with mixing units. Therefore, the spurious rejection of the AMC arises to be necessary [15].

In this paper, we present a high-performance AMC applicable to various E-band systems. A bypass tuning capacitor

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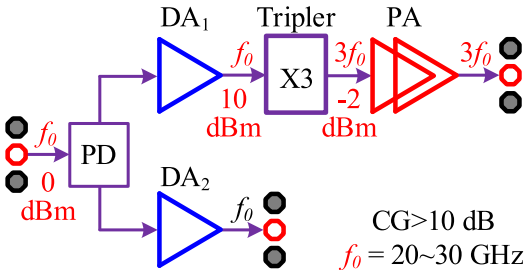

Fig. 1. Block diagram of the E-band AMC.

based power enhancing technique was adopted in the single-ended cascode topology DA and PA to improve the output power and the PAE. In the design of E-band passive frequency tripler core, the asymmetry of the layout connection often leads to poor second harmonic suppression. Thus, the tripler core with second harmonic rejection characteristic is proposed in this AMC. In addition, a bias circuit with temperature compensation function is proposed, which makes the key indicators of the AMC less fluctuate when the temperature changes. During the impedance matching design, the impedance matching networks with frequency selecting characteristics are adopted to effectively improve the harmonic suppression performance of the AMC. With all the proposed methods, the AMC has an measured output power exceeding 0 dBm in the entire E-band frequency range with a peak output power of 10.9 dBm at 77 GHz. The fundamental and second harmonic suppression is higher than 33.5 dB within the 3 dB frequency operating range. In Section II, the AMC architecture is described in detail. The AMC building blocks are explained in Section III and the design details of the sub-circuit is presented in Section IV. Measurement results are shown in Section V. Finally, this paper is summarized in Section VI.

II. The AMC Architecture

Fig. 1 depicts the block diagram of the E-band AMC, which composed of a 1:1 power divider (PD) that works at one-third of the output frequency, a one-stage single-ended cascode topology driver amplifier (DA_1), the driver amplifier (DA_2) with the same topology as DA_1 for detecting the input fundamental signal power level, a double-diode based passive E-band frequency tripler and a two-stage single-ended cascode structure E-band PA. The E-band AMC is designed in 130 nm SiGe BiCMOS process, featuring a cut-off frequency f_T of 200 GHz and a maximum oscillation frequency f_{MAX} of 250 GHz.

According to our previous work [16], the VCO designed based on this process can simultaneously obtain better phase noise and output frequency tuning range performance near 25 GHz, thus the input frequency of the AMC is set near 25 GHz and frequency tripler instead of frequency doubler is adopted for the E-band AMC design. In order to obtain better DC-to-RF conversion performance, the frequency tripler in this AMC adopts a passive double-diode structure.

There are several techniques currently used for E-band frequency tripler design [13], including third harmonic enhanced active type, injection-locked active type, and double-diode based passive type. The third harmonic enhanced active type tripler amplifies the desired third harmonic with better conversion gain. However, in order to achieve better even harmonic suppression characteristics, it often adopts a differential structure, resulting in a large chip area and a low PAE. The injection-locked frequency tripler does not require high input power and consumes less power, while the tuning range is limited. Therefore, the double-diode based passive type tripler that dissipates no dc power was adopted for the AMC design.

Due to the large conversion loss of the E-band passive double-diode based tripler and the insertion loss of single-ended to differential signal conversion balun, a two-stage single-ended cascode structure E-band PA is used at the output of the AMC to effectively increase the output power of the AMC with moderate chip area. In addition, due to the frequency selection characteristics of the matching network in the E-band tripler and PA, the harmonic suppression performance of the AMC can be effectively improved. The input fundamental signal power required by the entire AMC is 0 dBm, and the frequency range of the input fundamental signal covers 20 to 30 GHz.

III. Design of AMC Building Blocks

In this AMC, the small-signal gain of DA_1 and PA will restrict the output power of the AMC due to the limited input power, the PAE of DA_1 and PA will limits the DC-to-RF efficiency of the AMC, and the temperature operating range of the AMC is determined by $DA_{1,2}$ and PA.

A. Cascode Topology Power Amplifier With Power Enhancing Technique

Silicon-based millimeter-wave power amplifiers are often implemented using a common-emitter (CE) structure or a cascode structure [17]. The mm-wave power amplifier of the CE topology has lower DC power consumption, but its small signal gain is lower, and more stages need to be cascaded under the conditional of meeting the same gain. In the design of DA and PA in this AMC, due to the limitation of chip area, a more compact cascode structure is adopted. In addition, in order to obtain lower DC power consumption performance, DA and PA of the AMC are implemented in a single-ended structure.

The cascode topology is widely used in the design of millimeter-wave power amplifiers due to its higher gain and better reverse isolation performance [18]. However, it was discovered during the design process that for a single-ended cascode structure power amplifier, the bypass capacitor at the base of the common-base transistor (the bypass capacitor is used to connect the base of the common-base transistor to the RF ground without affecting the DC bias of the amplifier) has a greater impact on the power amplifier's gain [19]–[21], stability, output power and PAE performance. Therefore, the bypass capacitor of the common base transistor must be carefully designed. Thus, in the design of $DA_{1,2}$ and PA, the output power enhancement technology base on bypass capacitor C_{tune} is proposed. In order to effectively analyze the principle of the bypass capacitor, next we will analyze the

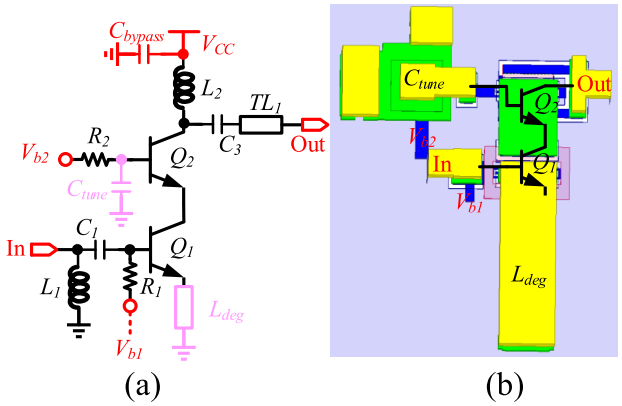

Fig. 2. (a) Schematic of $DA_{1,2}$, and (b) 3D view of the peripheral connection of the transistors in $DA_{1,2}$.

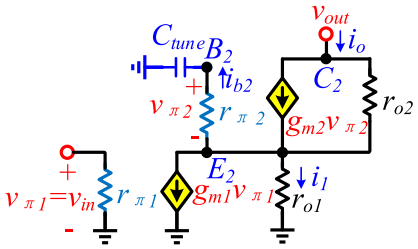

Fig. 3. Small-signal equivalent circuit of $DA_{1,2}$.

specific issues that need to be considered in the design of the bypass capacitor in DA.

The complete $DA_{1,2}$ circuit schematic diagram is shown in Fig. 2(a), where the transistors are biased in a class-AB working state, which is close to the process's f_T, and the corresponding current density is about 1 mA/μm. The emitter length of transistors Q_1, Q_2 are 12 μm. Together with the input parallel inductor L_1 and the series metal-insulator-metal (MIM) capacitor C_1, the input of the DA is well matched to 50 Ω. Besides, the inductor L_1 which is connected in parallel to the ground also plays the role of electrostatic protection (ESD). Compared to the conventional cascode topology, a tunable bypass capacitor C_{tune} is inserted in series between the RF ground and the base of transistor Q_2. For analyzing the effect of the bypass capacitor C_{tune}, we consider the small signal gain from input to output port. Fig. 3 shows the small signal equivalent circuit of $DA_{1,2}$, which is the equivalent circuit representation of Fig. 2(a) without the matching networks. For simplicity, the base-to-emitter capacitance C_{be}, the base-to-collector capacitance C_{bc}, and connection parasitic inductance are neglected, and we just replacing $Q_{1,2}$ with their hybrid-equivalent-circuit models [22]. Analysis of this circuit is straightforward and proceeds as follows.

The current i_{b2} flowing through the resistor $r_{\pi 2}$ can be expressed as

$$i_{b2} = \frac{-v_{\pi 2}}{r_{\pi 2}} \tag{1}$$

Similarly, the collector voltage node equation of transistor Q_2 is

$$v_{out} = (i_o - g_{m2}v_{\pi 2}) \cdot r_{o2} + i_1 \cdot r_{o1} \tag{2}$$

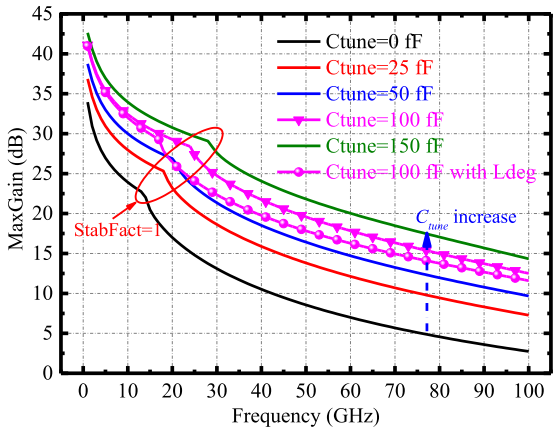

Fig. 4. Simulated MaxGain of the cascode topology power amplifier (DA_1) varying with the capacitance C_{tune}.

Next, we write a loop equation around the r_{o1}, $r_{\pi 2}$, C_{tune}, and RF ground loop as

$$i_1 \cdot r_{o1} = i_{b2} \cdot r_{\pi 2} + \frac{i_{b2}}{j\omega C_{tune}} \tag{3}$$

In addition, the current equation at the emitter node of transistor Q_2 can be written as

$$i_o = i_{b2} + g_{m1}v_{\pi 1} + i_1 \tag{4}$$

Combining (1) to (4), and considering the current relationship between the base and collector of a transistor, the expression of the small signal gain from the input port v_{in} to the output port v_{out} of the cascode amplifier can be approximated as (5), shown at the bottom of the next page.

It can be deduced from (5) that, as the value of the bypass tuning capacitor C_{tune} increases, the small signal gain of the amplifier continues to increase. In order to demonstrate the above theoretical analysis, Fig. 4 shows the simulated results of the maximum gain of the amplifier varying with the capacitance C_{tune}. It is noted that the maximum gain of the cascode topology amplifier has been greatly improved with the increase of the value of the tuning capacitance C_{tune}. Besides, for power amplifier design, in addition to the small signal gain, the maximum output power and the PAE are also very important indicators. Therefore, after introducing the output power boosting bypass tuning capacitor, we did a load-pull simulation on the amplifier. The maximum output power delivered and maximum PAE of the amplifier with the increase of the value of the tuning capacitance C_{tune} are illustrated in Fig. 5. As shown in Fig. 5, by introducing the tunable capacitor, the maximum output power and maximum PAE of the amplifier have been greatly improved.

It is worth mentioning that with the increase of the tuning capacitor C_{tune}, although the amplifier's (DA_1) small signal gain, output power, and PAE have been improved, but the stability of the amplifier at low frequencies has been deteriorated. Besides, the peripheral interface metal of the transistor Q_2 is M1, and the design rule stipulate that the MIM capacitor C_{tune} must be connected through the top thick metal layer AM. Thus, the connection of the MIM capacitor C_{tune} in the layout will include a base inductance, which is about 15 μm in length and the simulated inductance is about 7.6 pH.

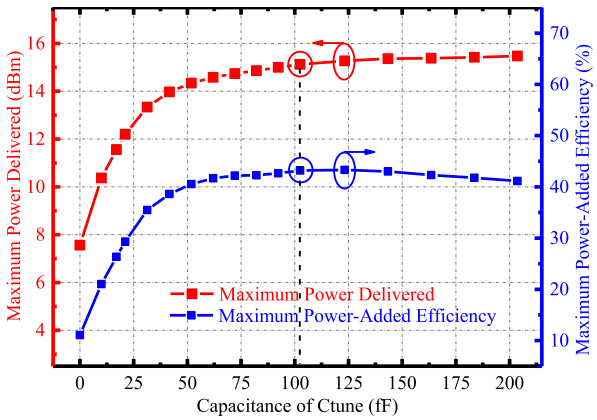

Fig. 5. Simulated maximum PAE and maximum power delivered of the power amplifier (DA_1).

Such a connected inductance will also deteriorate the performance of the amplifier.

In order to ensure the absolute stability of the amplifier, we introduced a negative feedback inductor L_{deg} in the emitter of the common-emitter transistor Q_1, which improves the stability of the amplifier and hardly affects the maximum output power of the amplifier, as shown in Fig. 2(a) and Fig. 4. The inductor L_{deg} is designed together with the peripheral connection of the transistor and the bypass tuning capacitor C_{tune}, and the length of the inductor is 43 μm with the width of 13 μm. Finally, the capacitance value of C_{tune} is set to 100 fF and the peripheral connection of the transistors in $DA_{1,2}$ is shown in Fig. 2(b).

B. Tripler Core With Second Harmonic Suppression

The frequency tripler in this AMC adopts a parallel double-diode structure, because it does not consume DC power. Normally, an ideal passive double-diode topology frequency tripler has excellent second harmonic suppression performance. However, the SiGe process we used does not provide a high-performance Schottky diode. The diode used in the tripler design is composed of an NPN transistor with its collector and base connected, as depicted in Fig. 6(a). Its equivalent circuit is shown in Fig. 6(b), including the capacitor C_{CS} from the collector to the dielectric substrate, the base channel capacitance $C_{VAR}(V_t)$ and the non-linear PN junction transconductance $G_{VAR}(V_t)$ controlled by the voltage across the diode [23].

Under ideal conditions (no asymmetric elements are introduced), the passive frequency tripler composed of the diodes shown in Fig. 6(a) hardly sees the second harmonic signal at its output, that is, the second harmonic is suppressed to infinity. In the actual design, the size of the transistor is usually large to deliver higher third harmonic output power, for example, the emitter size of the transistor in this design is 12 μm. Taking into account the spacing between the

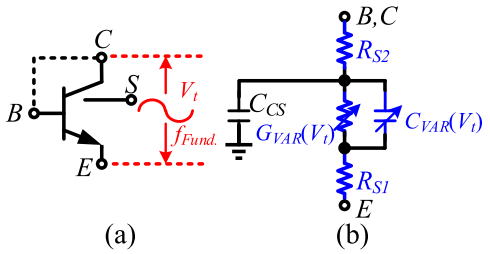

Fig. 6. (a) Schematic diagram of diode connection composed of NPN transistor, and (b) its equivalent circuit.

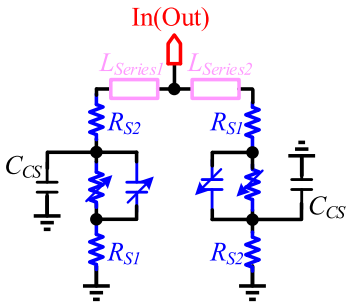

Fig. 7. Equivalent circuit of the passive tripler core with anti-parallel diode structure.

transistors required by the process design rules, the equivalent circuit of an anti-parallel diode structure tripler core in the actual design is shown in Fig. 7. The serial transmission lines $L_{Series1}$ and $L_{Series2}$ are the connecting lines that have to be introduced, which will have a greater impact on the conversion gain and second harmonic suppression performance of the tripler. Fig. 8 illustrates the simulated conversion gain and second harmonic rejection of the tripler core that vary with the length of the connecting lines. Similar to the previous hypothesis, when there is only $L_{Series1}$, and $L_{Series1}$ is short (less than 10 μm), the tripler core has better conversion gain and second harmonic suppression performance. When $L_{Series1}$ and $L_{Series2}$ exists at the same time (to ensure the symmetrical connection of the tripler core) and the length is large, that is, the input and output interface of the tripler is located in the middle of the two diodes, the second harmonic suppression of the tripler core is greatly deteriorated as shown in Fig. 8. Another way to connect the tripler core is that the input and output interface of the tripler is close to the diode on one side, that is, there is only $L_{Series1}$ and the length of $L_{Series2}$ is almost 0. It can be deduced from Fig. 8 that, the second harmonic suppression of the tripler will be greatly deteriorated due to the asymmetry of the tripler core. Considering the limitations of the process's design rules, the second harmonic rejection and conversion gain of the tripler core, the value of the series transmission line $L_{Series1}$ and $L_{Series2}$ are both selected as 30 μm and the symmetrical layout is carried out.

$$\frac{v_{out}}{v_{in}} = \frac{(\beta r_{o2} + g_{m2} v_{\pi 2} r_{o2} - 1) \cdot g_{m1} r_{o1} - g_{m1} r_{o1} / (1 + j w C_{tune})}{r_{o1} \cdot (\beta - 1)} \tag{5}$$

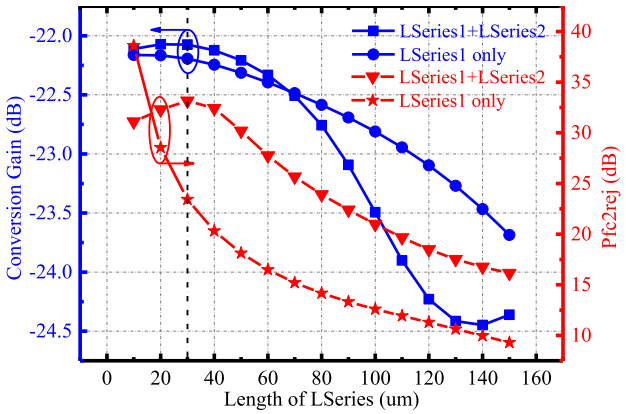

Fig. 8. Simulated conversion gain and second harmonic rejection of the tripler with the length of the series connection lines.

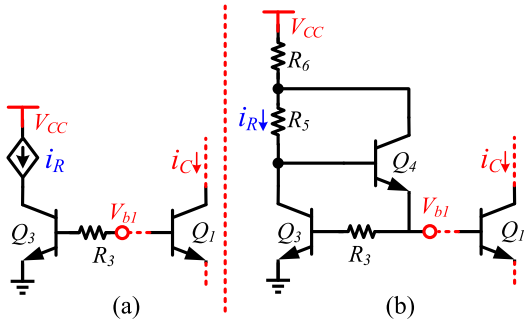

Fig. 9. (a) Traditional temperature compensation network (TTCN), and (b) the proposed temperature compensation network (PTCN).

C. Temperature Compensation Design

For most E-band applications, such as point-to-point wireless communication and FMCW, it is desired that the system can function well with moderated performance degradation over temperature variations. In order to ensure that the active circuit can exhibit good performance under high and low temperature, one of the conditions is to make the quasi-quiescent current of the circuit less fluctuate with temperature changes. For this AMC design, the DA and the PA are both cascode configuration, and the current can be reduced to nearly zero at low temperature (−40 °C) and increased to several times the room temperature (25 °C) at high temperature (125 °C), due to that β is a temperature-sensitive parameter and increase with increasing temperature. Therefore, a temperature compensation based bias circuit was adopted in our design to compensate for variation in the quasi-static current which is caused by temperature variation, as shown in Fig. 9 (b).

Since the emitter junction of transistor Q_1 and Q_3 are tied together, when they work in active region and ignoring base width modulation effects, according to the relationship between the base, collector and emitter current of a transistor, it can be obtained that

$$i_R = i_{C3} + i_{B4} \tag{6}$$

$$i_{C3} = \beta_3 i_{B3} \tag{7}$$

$$(1+\beta_4)\, i_{B4} = i_{B3} + i_{B1} \tag{8}$$

$$i_C = \beta_1 i_{B1} \tag{9}$$

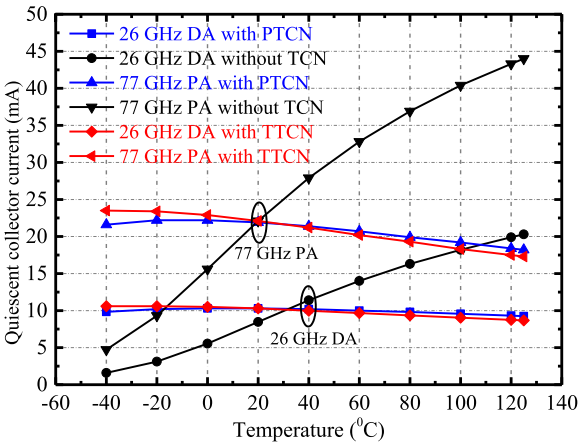

Fig. 10. Quiescent collector currents of the DA and PA with, and without temperature compensation network.

In addition, for the same process it is assumed that

$$\beta_1 = \beta_3 = \beta_4 = \beta \tag{10}$$

Then i_C can be simplified as

$$i_C = n \cdot \frac{\beta^2 + \beta}{\beta^2 + \beta + 2} \cdot i_R \approx n \cdot i_R \tag{11}$$

Where n represents the ratio of the emitter area of transistor Q_1 to transistor Q_3. From (11), it can be concluded that i_C is determined when i_R is fixed. Compared to the traditional temperature compensation network (TTCN) shown in Fig. 9(a), by utilizing the current amplification function of Q_4, current $i_{B1} + i_{B3}$ shunt to i_R were reduced greatly. Thus, current i_C is close to i_R, thereby effectively reducing the error introduced by the finite β value during the conversion of i_R to i_C. The direct result is that a smaller quasi-static current change will be obtained.

To verify the validity of the proposed temperature compensation bias circuit, the simulated results are compared with those of the uncompensated 26 GHz DA and 77 GHz PA, which has the same quiescent collector current at 25 °C. As illustrated in Fig. 10, the uncompensated PA has quiescent collector current of 22.1 mA at room temperature, and it varies from 4.73 mA to 44 mA as the temperature changes from −40 °C to 125 °C. However, with the proposed temperature compensation network (PTCN), the quiescent current changes only from 18.2 mA to 22.2 mA. Meanwhile, with the traditional temperature compensation network (TTCN), the quiescent current changes from 17.3 mA to 23.5 mA. In comparison, the PTCN has better temperature compensation performance. Benefiting from the PTCN, the quiescent current of DA has also been greatly improved, as shown in Fig. 10. This means that with this PTCN, the output power of AMC fluctuates in a smaller range under high and low temperature conditions.

IV. The AMC Sub-Circuits Design

In this section, we will present the circuit design methodology of the E-band AMC, including the consideration of each block, then present the simulated results of key building blocks. The detailed analysis and design of $DA_{1,2}$ have been

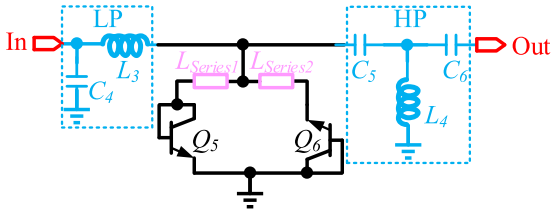

Fig. 11. Schematic of the E-band frequency tripler.

described in Section III.A, and then the design of the E-band tripler and PA will be introduced in detail.

A. The E-Band Passive Double-Diode Based Tripler Design

The schematic of the E-band passive double-diode based frequency tripler is shown in Fig. 11, which comprise an input low pass (LP) matching network, an odd-order harmonic generator [24], and an output high pass (HP) matching network. For the E-band double-diode based tripler, one of the design difficulties is the suppression of the second harmonic signal, which is caused by the asymmetry of the external connection of the transistor. In this design, full consideration is given to the connection limitations of diodes based on transistors when forming the passive tripler core, and proposes a second harmonic suppression improvement technology based on the series microstrip line tuning units ($L_{Series1}$, $L_{Series2}$), as shown in Fig. 11. The detailed analysis of the principle of the second harmonic rejection is given in Section III.B, and the measured results show that the second harmonic suppression exceeds 30 dB in the AMC working frequency band.

Because the E-band frequency tripler adopts a passive structure, the harmonic signals which coupled from the output port to the input port are harmful to the desired third harmonic signal at the output port [25], [26]. In this design, a LP filter composed of a shunt capacitor C_4 and a series inductor L_3 is inserted between the input port and the passive tripler core. The capacitor uses high quality factor MIM capacitor, and the inductor is routed in a serpentine pattern to save chip area. Such LP filter at the input before the tripler core can not only provide a low-impedance path to the ground for each high-order harmonic signals reflected to the input, but also play the role of input impedance matching (IMN). Another harmonics rejection technique aims to suppress the unwanted harmful harmonics at the output (mainly fundamental and second harmonic signal), which is realized by a HP filter connected between the tripler core and the output port, as depicted in Fig. 11. The HP filter is implemented by a T-type network composed of series capacitors C_5 and C_6, and parallel to ground inductance L_4. With the help of the HP filter, the low-frequency signal is attenuated by 30 dB at the output of the tripler, which greatly improves the fundamental signal rejection performance of the AMC. Meanwhile, the second harmonic signals has also been further suppressed. The simulated insertion loss of the LP and HP filters are demonstrated in Fig. 12. It is clear that both filters show good frequency selection characteristics.

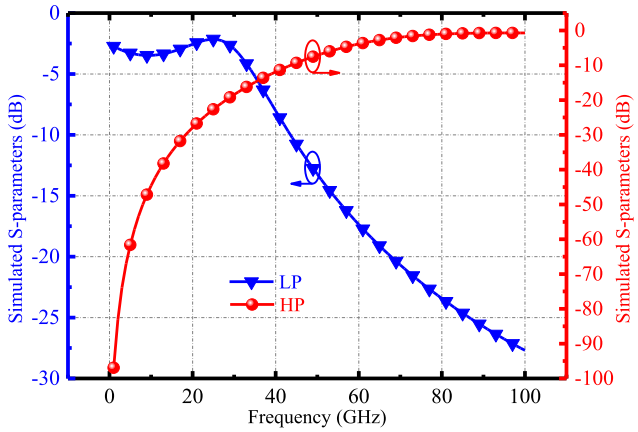

Fig. 12. The insertion loss of the simulated LP and HP filters.

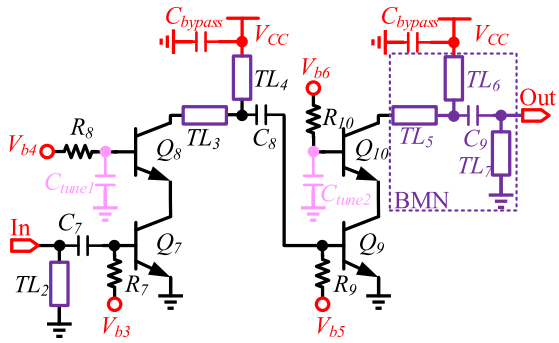

Fig. 13. Schematic of the E-band PA.

B. The E-Band PA Design

Due to the limited output power of the passive tripler, the PA is adopted after the passive tripler to make the AMC have a higher third harmonic output power [27], [28]. At the same time, the band-pass impedance matching network (BMN) of the PA also has further suppression characteristics for the unnecessary harmonics in the AMC. The circuit schematic of the E-band two-stage single-ended cascode structure PA is shown in Fig. 13. Cascode topology is selected mainly because of its superior small-signal gain performance when compared with common-emitter topology. With higher single-stage small-signal gain, the number of cascading stages can be reduced, thus resulting in a much smaller chip area and lower power consumption. Different from the low frequency band DA shown in section III.A, in the E-band, the MaxGain of the traditional cascode topology PA is limited, and it is usually only a few dB without any gain enhancement technology. Therefore, in the design of the two-stage PA, the bypass capacitor-based gain and output power enhancement technique proposed in Section III.A is adopted. The size of the emitter of the first stage transistors (Q_7, Q_8) is 8 μm, and the capacitance of the corresponding bypass capacitor C_{tune1} is 65 fF. The emitter size of the second-stage transistors (Q_9, Q_{10}) is 18 μm, and the capacitance of the associated bypass capacitor C_{tune2} is 100 fF. In addition, in the design of the two-stage amplifier unit, the temperature compensation feed network proposed in section III.C is used to ensure that the amplifier show good performance under high and low temperature conditions.

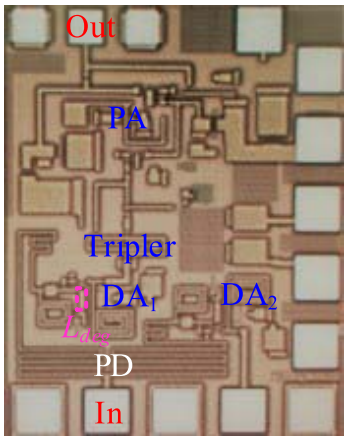

Fig. 14. Die photograph of the E-band AMC.

For the two-stage PA, the first driver stage typically operates within the linear region to provide considerable small-signal gain and avoid signal distortion. The second-stage power amplifier unit is used to achieve higher output power, and the corresponding transistor size is larger [29], [30]. The bandwidth of the PA is typically limited by the frequency response of the passive networks, especially the last output power matching network. To achieve broadband performance, in the design of the PA output power matching network, a multi-level broadband impedance matching network composed of a series inductance TL_5, a capacitor C_9, an inductance TL_6, and TL_7 connected in parallel to the ground is used. The output power matching network also shows bandpass characteristics, and the simulated insertion loss of the output power matching network is about 1.2 dB at 75 GHz.

It is worth noting that in the frequency band where the AMC works, the capacitance value of the RF PAD cannot be ignored. Therefore, in the design of the AMC input and output matching network, we incorporate the capacitance value of the PAD into the input and output matching network, and the capacitance value is about 28fF. In addition, the AMC is usually used with a PLL. If the output of the PLL does not have a DC blocking capacitor, a 1 pF capacitor can be connected in series with the input of the AMC first, and then the AMC and the output of the PLL can be connected.

V. Fabrication and Experimental Results

The E-band AMC has been fabricated in a commercial 130 nm SiGe BiCMOS process with seven metal layers. The chip photograph is shown in Fig. 14 with chip area of 940 × 730 μm^2 including RF/DC bias pads. The DC power consumption of the AMC is 137 mW. The AMC is measured via on wafer probing, with bonding wires to supply DC power.

The measurement of the AMC mainly includes two parts, namely the test of the output power and the test of the suppression of each harmonic. For the output power measurement, the input fundamental signal is provided by Keysights vector signal source E8257D, and the corresponding fundamental signal power is directly controlled by the signal source. The output power was measured with Keysight N1914A power meter and corresponding power head. Besides, frequency of fundamental and second harmonic were analyzed using two

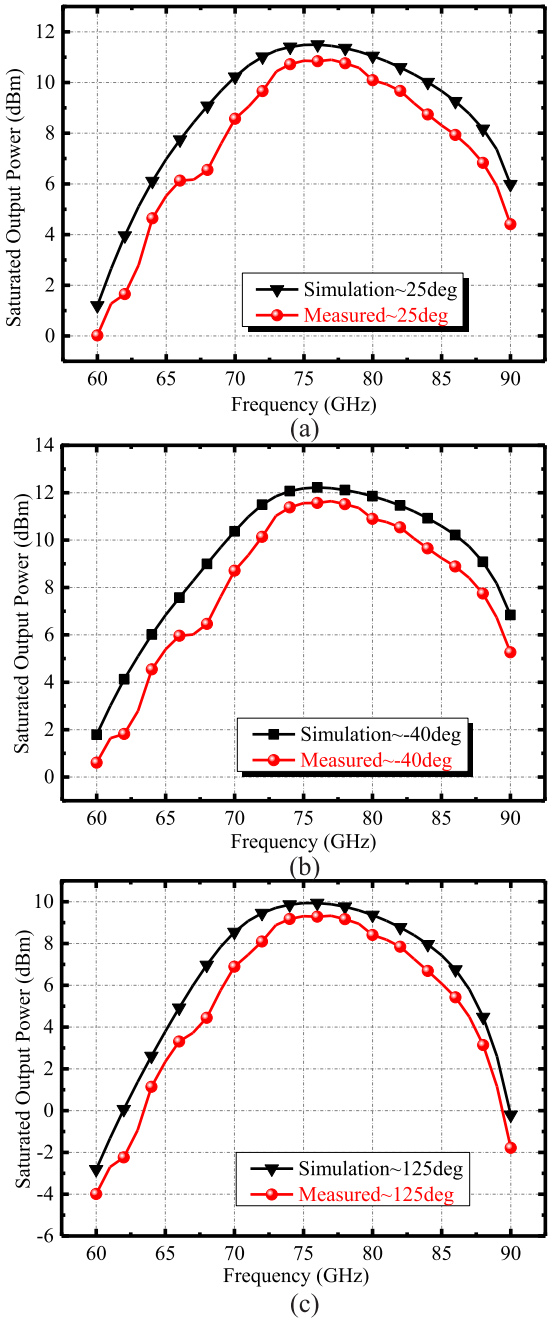

Fig. 15. Simulated and measured output power versus output frequency under 0 dBm input power at (a) 25 °C, (b) −40 °C, and (c) 125 °C.

configuration types: (1) Keysight N9030A spectrum analyzer for fundamental and (2) a V-band (50-75 GHz) harmonic mixer and N9030A spectrum analyzer for second harmonic. In addition, the losses caused by input coaxial cable, probe, and output waveguide have been calibrated.

Fig. 15(a) illustrates the measured results of the output power versus input frequency under input power level of 0 dBm at 25 °C. The results reveal that the 3dB bandwidth of the AMC under large-signal operation is approximately 18 GHz, ranging from 69 to 87 GHz. Benefiting from the proposed broadband high-performance impedance matching networks, the output power of the AMC is higher than 0 dBm over the entire E-band frequency at room temperature. The measured peak output power is 10.9 dBm at 77 GHz.

TABLE I

COMPARISON WITH SIGNAL SOURCE OPERATING IN SIMILAR FREQUENCY RANGES

Reference	[6]	[7]	[8]	[11]	[12]	[13]	[14]	**This Work**
Process	130 nm SiGe	130 nm SiGe	55 nm SiGe	65 nm CMOS	65 nm CMOS	130 nm SiGe	180 nm SiGe	**130 nm SiGe**
Topology	PLL+×4	PLL+×2	VCO+×4	×9	×3	×3	VCO+×3	**×3**
Frequency [GHz]	75-83	73.92-83.52	70-81	88-99.5	57-78	65-90	90-101	60-90
3 dB BW [GHz]	8	9.6	-	11.5	21	17	10.9	**18**
Pout [dBm]	9.5	-4	-	8.5	-2	9.9	-10.5	**10.9**
Harmonics Rejection [dBc]	-	-	-	>31	>20	>35	>20	**>33.5***
Pdc [mW]	590	510	50	438	60	158	75	**137**
PAE [%]	1.51	-	-	1.62	1.05	5.18	0.12	**8.25**

* Within 3 dB BW.

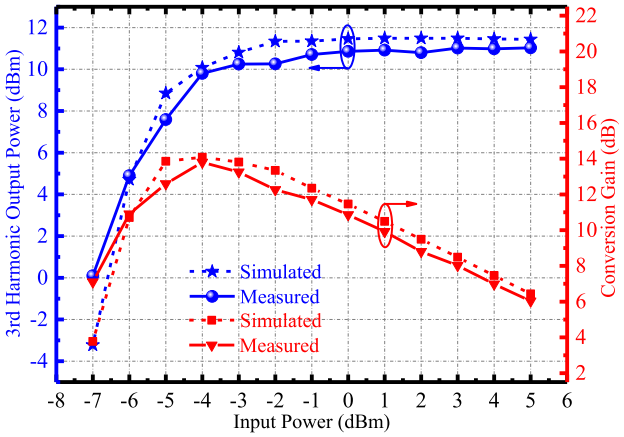

Fig. 16. Simulated and measured output power and conversion gain of the AMC with the fundamental frequency of 25 GHz.

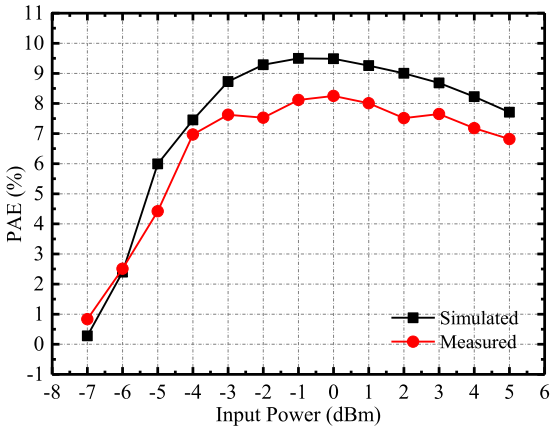

Fig. 17. Simulated and measured PAE of the AMC with the fundamental frequency of 25 GHz.

Comparing the measured results of the output power under different temperature conditions in Fig, 15 (a)(b)(c), it can be concluded that benefiting from the proposed temperature compensation bias network, the output power fluctuation range of the AMC is within 1.5 dB when the ambient temperature changes from −40 °C to 125 °C.

The simulated and measured third harmonic output power and conversion gain of the AMC versus input power at 25 GHz is illustrated in Fig. 16, from which it can be seen that the measured results match well with the simulation. Besides, the AMC achieves a measured peak conversion gain of 13. 8 dB with −4 dBm fundamental input power. The simulated and

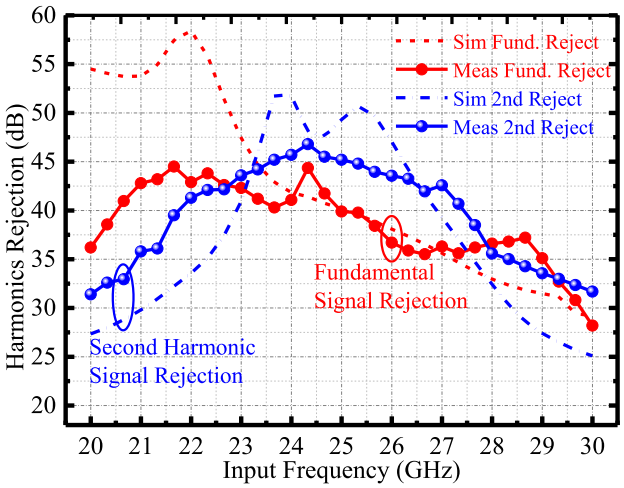

Fig. 18. Measured and simulated fundamental and second harmonic signal rejection of the AMC with the input power of 0 dBm.

measured PAE of the AMC (without DA_2) with the fundamental frequency of 25 GHz is depicted in Fig. 17. Benefiting from the bypass tuning capacitor in the single-ended DA and PA, the AMC demonstrate a record PAE of 8.25 % with the input power level of 0 dBm at 25 GHz. Fig. 18 plots the measured and simulated fundamental and second harmonic rejection versus input frequency at the input power level of 0 dBm. Thanks to the proposed unwanted harmonics rejection techniques, the results demonstrates that the measured fundamental and second harmonic suppressions within 3 dB bandwidth are better than 35 dB. As depicted in Fig. 18, the measured results and the simulation result show a large deviation, which may be caused by the frequency deviation of the HP or LP matching network in the AMC during the chip processing. To the best of the authors' knowledge, the proposed AMC has the highest output power and PAE that covers industrial temperature range compared with other silicon-based E-band or W-band frequency multipliers.

VI. CONCLUSION

This paper presents a monolithically integrated E-band amplifier multiplier chain (AMC) developed in 130 nm SiGe BiCMOS process, which is composed of a 25 GHz 1:1 PD, two 25 GHz DA, a 75 GHz passive frequency tripler, and a 75 GHz PA. By applying a bypass tuning capacitor based power enhancing technique in the single-ended DA and PA, the output power and power-added-efficiency (PAE) of the

AMC have been effectively improved. In the design of passive double-diode based frequency tripler core, the asymmetry of the layout often leads to poor second harmonic rejection. Therefore, the passive tripler core with second harmonic suppression is proposed in this AMC. In addition, the bias circuits with temperature compensation function are applied to the DA and PA to ensure the performance of the AMC when the temperature changes. Besides, the impedance matching networks with frequency selecting characteristics are adopted to further improve the harmonic suppression performance of the AMC. Benefiting from all the proposed methods, the AMC has a measured output power exceeding 0 dBm in the entire E-band frequency range with a peak output power of 10.9 dBm at 77 GHz, and exhibits a record PAE of 8.25 %. Within the 3 dB operating frequency range from 69 to 87 GHz, the rejection of fundamental and second harmonics are more than 33.5 dB. The AMC can work properly between -40 °C and 125 °C with the proposed temperature compensation bias circuits. Along with the considerable output power, PAE, high harmonics rejection, and wideband characteristic, the proposed E-band AMC is appropriate for various E-band communication or radar applications.

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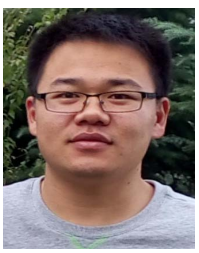

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