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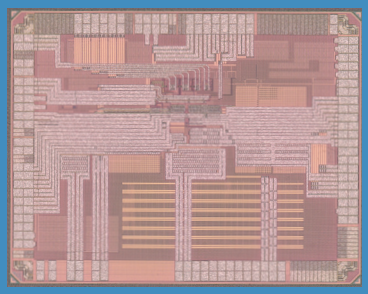

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Broadband Continuous-Time MASH Sigma-Delta ADCs

PROEFSCHRIFT

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Het onderzoek of ontwerp dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

Contents

List of symbols and abbreviations

Symbol	Description	Unit
3GPP	3rd Generation Partnership Project	
ADAS	advanced driver assistance systems	
ADC	Analog to digital converter	
BLMS	Block Least Mean Square	
BP	Band-pass	
BW	Bandwidth	
CDMA	Code-division multiple access	
CMFB	Common-mode feedback	
DEM	Dynamic element matching	
CIFF	Cascade-of-integrators, feedforward form	
CMFB	Common-mode feedback	
CT	Continuous-time	
CRFB	Cascade-of-resonators, feedback form	
CRFF	Cascade-of-resonators, feedforward form	
CLF	Connecting loop filters	
DAB	Digital audio broadcasting	
DAC	Digital to analog converter	
dBFS	dB full-scale	
DEM	dynamic element matching	
D-FF	D-flipflop	
DR	dynamic range	
DT	Discrete-time	
DWA	Data weighted averaging	
EDGE	Enhanced data rates for GSM evolution	
ENOB	Effective number of bits	bit
ELD	Excess loop delay	
ESD	electrostatic discharge	
FIR	Finite impulse response	
FM	Frequency modulation	
FMCW	Frequency-modulated continuous wave	
FoM	Figure of merit	
FoM_W	Waldon figure of merit	J/conversion-step

FoM_S	Schreier figure of merit	dB
F_s	Sampling frequency	Hz
f_T	Transit frequency of MOS transistors	
GBW	Gain bandwidth product	Hz
GPRS	General packet radio service	
GSM	Global system for mobile communications	
GRO	Gated-ring-oscillator	
HD2	2nd order harmonic	
HD3	3rd order harmonic	
IBN	In-band noise	
IC	Integrated circuit	
LDE	Layout-dependent effects	
IF	Intermediate frequency	
ILF	Internal loop filter	
IMD_2	2nd order inter-modulation-distortion	
IMD_3	3rd order inter-modulation-distortion	
INL	Integral non-linearity	
ISG	Inter-stage gain	
LDO	Low-dropout	
LP	Low-pass	
LSB	Least significant bit	
LTE	Long term evolution	
MASH	Multi-stAge noise SHaping	
MC	Monte-carlo	
MEC	metastability error compensation	
MOS	Metal-oxide-silicon	
MSA	Maximum stable input amplitude	
NCF	Noise cancellation filter	
NRZ	Non-return-to-zero	
NTF	Noise transfer function	
OBG	Out-of-band gain	
OSR	Over-sampling ratio	
OTA	Operational transconductance amplifier	
PC	Personal computers	
PLL	phase-locked loop	
PVT	Process, voltage and temperature	
PSRR	power supply rejection ratio	
RZ	Return-to-zero	
SAR	Successive approximation register	
SC	Switched-capacitor	
SDM	Sigma-Delta modulator	
SFDR	Spurious free dynamic range	
S&H	sample-and-hold	
SMASH	Sturdy MASH	
SNDR	Signal to noise and distortion ratio	

SNR	Signal to noise ratio	
SoC	System on chip	
SQNR	Signal to quantization noise ratio	
STF	Signal transfer function	
TDC	Time-to-digital converter	
THD	Total harmonic distortion	
TI	time-interleaved	
UGBW	Unity-gain bandwidth	Hz
UMTS	Universal mobile telecommunications system	
UWB	Ultra-wide-band	
V2X	Vehicle-to-everything	
V_{CM}	Common-mode voltage	V
VCO	Voltage-controlled oscillator	

Chapter 1

Introduction

This chapter introduces the research context of the thesis. First, the background of this research is given, which is further elaborated in more detail in Chapter 2. Afterwards, the problem definition is described. Moreover, this chapter presents the aim and the scope of this thesis. Then the original contributions are listed. In the end, the outline of this thesis is shown.

1.1 Background

The development of the semiconductor industry has been making our lives safer, smarter, easier, more productive and more efficient, by enabling numerous new products and applications. For example, high-speed networks (e.g. 5G) and smart phones have changed our lifestyle, and we can work, study, go shopping, play games, etc. with the same smart phones. Today's smart phones have more computation power than the computers that navigated the landing on the moon in 1960's. Electrification and automation become the main trends of today's automotive industry, which cannot happen without the advanced driver assistance systems (ADAS), power management, microcontrollers, etc. provided by the semiconductor industry. Breathing machines (respirators), CT scanners, etc. have saved millions of lives in the on-going Covid-19 crisis. Personal computers (PC) and tablets enable working from home and remote studying. All of the aforementioned products, services, applications and many more cannot come true without the development and innovation of the semiconductor industry. That's why although the world's economy is heavily impacted by the Covid-19 crisis, the demand for the semiconductor products (chips) is even higher.

Analog-to-digital converters (ADCs) are essential building blocks in many semiconductor products. The basic function of an ADC is to convert an analog signal into a digital signal. Light (image), sound, electromagnetic waves, etc. in nature are all analog signals. In modern electrical devices, the data are represented, processed, computed and stored (in most cases) in the format of digital signals. Without ADCs

(and digital-to-analog converters (DACs)), analog signals and digital signals are two separated domains. ADCs (and DACs) are the bridges to connect analog domain with digital domain, and hence they are widely used in many application categories of semiconductor products.

ΣΔ ADCs make use of the available bandwidth (BW) offered by integrated circuit (IC) technologies, and trade time resolution for amplitude resolution in an efficient way by noise shaping. Continuous-time (CT) ΣΔ ADCs are widely used in telecommunication, automotive, consumer electronics, healthcare and other applications. Compared to other types of ADCs which have an input sample-and-hold (S&H), CT ΣΔ ADCs have advantages of resistive input, inherent anti-aliasing filtering and easy integration. Broadband CT ΣΔ ADCs are integrated in many telecommunication and automotive products, e.g. 5G base station transceivers [1], and car radar [2]. Since future applications require more data rate and higher performance, CT ΣΔ ADCs with broader signal bandwidth are needed [3]. Indeed, the achievable signal BW scales up with the CMOS technology nodes, and it is of great interest to explore the BW boundary of CT ΣΔ ADCs for a given CMOS technology and a certain resolution target.

1.2 Problem definition

CT ΣΔ ADCs are widely used for medium-to-high resolution ($\geq$ 50 dB signal to noise and distortion ratio (SNDR)) and low-to-medium bandwidth ($\leq$ 100 MHz) ADC applications. For medium resolution applications (50 dB $\leq$ SNDR $\leq$ 70 dB), for the same SNDR, the reported broadest signal bandwidth of CT ΣΔ ADCs is less than the reported broadest signal bandwidth of pipelined ADCs and time-interleaved (TI) successive approximation register (SAR) ADCs [4] (see Chapter 2.3). CT ΣΔ ADCs have advantages in the system-level integration, however, the problem which motivates this research is that the current maximum achievable signal BW of CT ΣΔ ADCs is lower than the demanded signal BW of future automotive and telecommunication applications, e.g. car radar, base station. For CT ΣΔ ADCs, the signal BW is limited by the maximal achievable sampling rate and the over-sampling ratio (OSR). The minimum OSR is bounded by the order of the noise transfer function (NTF), quantizer resolution and the signal to quantization noise ratio (SQNR) target. The maximal achievable sampling rate is limited by the stability of the ΣΔ modulators (SDMs), the quantization gain and metastability error, and the maximum speed offered by the technology. The noise and linearity targets have impact on the maximal achievable sampling rate as well. In the end, the signal BW and resolution of the CT ΣΔ ADCs are bounded by power consumption and area.

The research questions that this thesis addresses are the following: How to maximize the achievable BW of a CT SDM in a given CMOS technology for a given DR? More specifically, what is the maximum achievable signal bandwidth of CT SDM in 40nm CMOS technology for a DR target of 60 $\sim$ 70 dB and a total power consumption of

less than 1 W? What SDM architectures should be chosen and what design techniques should be used? Are there new techniques that can be used to further increase the signal bandwidth? What are the fundamental limitations for the maximal achievable signal bandwidth for CT ΣΔ ADCs?

1.3 Aim of the thesis

The aim of this thesis is to explore the maximum achievable bandwidth of CT ΣΔ ADCs for a given CMOS technology and a certain resolution target. The motivation of this thesis is to bring the advantages of CT ΣΔ ADCs to a broader bandwidth than the state-of-the-art. More specifically, the target of this thesis is to explore the maximum achievable bandwidth of CT ΣΔ ADCs in a 40 nm CMOS technology for a dynamic range (DR) of 60 $\sim$ 70 dB and total power consumption of less than 1 W. The aim of this thesis is further elaborated as follows:

- Explore architecture choices and their implementation limitations for broadband CT ΣΔ ADCs. Research on the maximal SQNR potential of single-loop and Multi-stAge noise SHaping (MASH) ΣΔ ADC architectures, and synthesize a CT ΣΔ ADC architecture for test chip implementation.
- Investigate the challenges in the circuit implementation of broadband CT ΣΔ ADCs. Propose novel concepts for system-level and circuit-level solutions to combat these challenges.
- Design a broadband CT ΣΔ ADC test chip, validate the study of this thesis and prove the proposed concepts.

1.4 Scope of the thesis

The scope of this thesis is elaborated as follows:

- Since the motivation of this thesis is to bring the advantages of CT ΣΔ ADCs to applications with a broader bandwidth, other types of ADCs are not investigated in detail. This thesis focuses on low-pass (LP) CT ΣΔ ADCs, and hence band-pass (BP) CT ΣΔ ADCs are not investigated in detail.
- This thesis focuses on the core circuity of the ΣΔ modulator. Supply regulation circuits, such as low-dropout (LDO) regulators, are out of the scope of this thesis. The hardware implementation of some digital circuitry, such as decimation filter and noise cancellation filter, is out of the scope of this thesis.

- The target applications of the broadband CT ΣΔ ADCs in this thesis are future automotive and telecommunication applications, e.g. car radar, base station. For these applications, system on chip (SoC) is the main trend for transceiver products. To benefit for the system integration, CMOS technology is considered in this thesis. The ADC test chip design is performed in a 40 nm CMOS technology in this thesis.

1.5 Original contributions

The original contributions of this thesis are as follows:

- Generic formulas to calculate the SQNR limits for both single-loop and MASH SDMs (Chapter 5.1)
- A digital calibration of the errors due to the limited DC gain and 2nd pole of the loop filter integrators for MASH SDMs (Chapter 6).
- A current-mode multi-path excess loop delay (ELD) compensation technique (Chapter 7.2).
- Techniques overcoming the parasitic capacitance on the summation node (Chapter 7.3).
- A current-mode locally-time-interleaved multi-bit quantizer (Chapter 8.1).
- A comparator offset calibration technique (Chapter 8.2).
- A new implementation of the DAC linearization techniques (Chapter 9).
- A metastability error compensation technique (Chapter 10.4).
- A metastability shaping technique (Chapter 10.5).
- A 6-GHz-sampling 3-bit 2-1-1 MASH CT SDM test chip with the largest signal BW reported so far of 500 MHz. The MASH ADC test chip achieves 58 dB DR in 500 MHz BW when sampled at 6 GHz and it consumes 574 mW. If sampled at 4 GHz, it achieves 65 dB DR in 300 MHz BW and it consumes 506 mW.

1.6 Thesis outline

This thesis is divided into three parts and 12 chapters. The outline of this thesis is described below.

- **Part I** discusses the analysis, limitations and design aspects in the ΣΔ ADC architecture design. It is further divided into 4 chapters.
- **Chapter 2** elaborates on the potential of CT ΣΔ ADCs for broadband applications.
- **Chapter 3** presents the architecture design choices for broadband CT ΣΔ ADCs. It is part of the top-down approach of the broadband CT ΣΔ ADC design.
- **Chapter 4** discusses the challenges, non-idealities and limitations of the circuit implementation of broadband CT ΣΔ ADCs. It is part of the bottom-up approach of the broadband CT ΣΔ ADC design.
- **Chapter 5** presents a synthesis flow for broadband CT MASH ΣΔ modulators, on the basis of an exemplary ADC architecture for the target application defined earlier.
- **Part II** presents several novel design concepts proposed in this thesis. It is further divided into 5 chapters.
- **Chapter 6** proposes a digital automatic calibration method for broadband CT MASH ΣΔ ADCs. The main contribution of this method is the calibration of the errors due to the limited DC gain and 2nd pole of the loop filter integrators.
- **Chapter 7** discusses high-speed ELD compensation techniques for broadband CT ΣΔ ADCs. This chapter proposes a current-mode multi-path ELD compensation technique and techniques to overcome the parasitic capacitance on the summation node.
- **Chapter 8** presents a current-mode locally-time-interleaved multi-bit quantizer and a comparator offset calibration technique.
- **Chapter 9** proposes a new implementation of the DAC linearization techniques in broadband CT ΣΔ ADCs with the mapping engine in the digital domain.
- **Chapter 10** studies the impact of metastability errors in broadband CT ΣΔ ADCs. This chapter proposes two system-level solutions to combat the metastability errors – a metastability error compensation technique, and a metastability shaping technique.
- **Part III** presents the CT MASH ΣΔ ADC test chip design and validation. It contains 1 chapter.
- **Chapter 11** presents the circuit-level implementation, simulation and validation results of a 6-GHz-sampling 500-MHz-BW 2-1-1 MASH CT ΣΔ ADC test chip.
- **Chapter 12** presents the conclusions of this thesis and recommendations for future work.

Part I

Architecture: analysis, limitations and design aspects

Chapter 2

CT $\Sigma\Delta$ analog-to-digital conversion for broadband applications

This chapter elaborates on the potential of CT $\Sigma\Delta$ ADCs for broadband applications. Firstly, the evolution of mobile telecommunication standards shows the needs of increasing signal bandwidth. ADCs with broader bandwidth benefit from the speed advantage offered by more advanced CMOS technologies. The chapter further presents a typical receiver architecture and gives target ADC specifications for such broadband applications. Afterwards, the chapter depicts an overview of different ADC architectures. Low-pass CT $\Sigma\Delta$ ADCs are further compared to Nyquist ADCs in the context of a typical receiver system. In the end, the motivation of this thesis is presented, and conclusions are drawn.

2.1 Broadband applications

We have been witnessing and experiencing the expeditious development of new technologies. One example is our mobile phones over the last two decades – higher download/upload speed, more Apps, more advanced functions. Figure 2.1 shows the evolution of the mobile telecommunication standards. The 1st generation of the mobile telecommunication standards uses analog radio signals, which was launched for commercial use starting from 1979 and it can offer a maximal user's download speed of about 2.4 kbit/s. The first commercial 2G network based on GSM standard was launched in 1991, which increased the user's download speed to 35 kbit/s. Starting from 2G, digital radio signals are used in the transmission. Two standards are used worldwide as the 3G mobile telecommunication standards – UMTS and CDMA2000. They were first offered in 2001 and 2002, and the maximal user's download speed are 384 kbit/s and 2 Mbit/s, respectively. 4G standard LTE-Advanced started in commercial use around 2010, and can offer 100 Mbit/s download speed. Starting from 2019, 5G networks were launched whose download speed is up to 1.8 Gbit/s. Figure

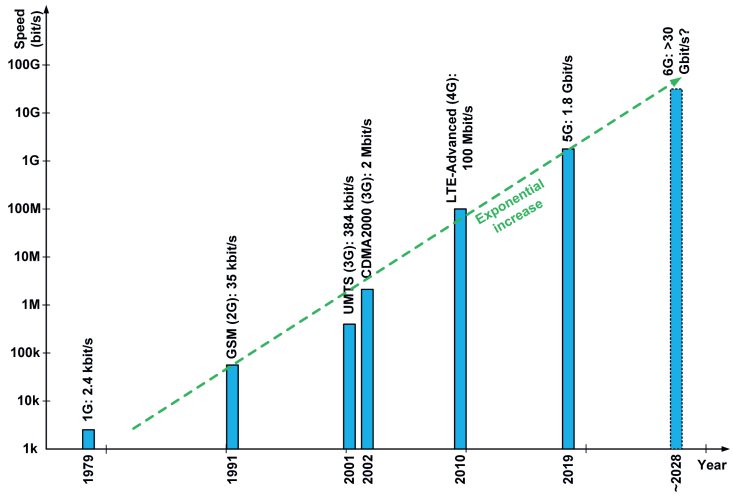


Figure 2.1: Mobile telecommunication standards evolution: user's download speed vs. year (based on [6]).

2.1 shows that the user's download speed increased exponentially in the last 30 years. If this trend continues, the next generation (6G) mobile telecommunication standard will appear around 2028 and it will offer a user's download speed of more than 30 Gbit/s. The exponential increasing trend resembles Moore's law [5].

The increasing download/upload speed is enabled by the breakthroughs in communication theory, hardware and software. According to the Shannon theory, the channel capacity C is defined by the signal BW, signal power P_S and noise power P_N [7]:

$$C = BW \cdot log_2 \frac{P_S + P_N}{P_N} \quad \text{[bit/s]} \tag{2.1}$$

To increase the channel capacity, the signal BW and/or signal to noise ratio (SNR) should be increased.

$$SNR = \frac{P_S}{P_N} \tag{2.2}$$

When the signal power is much larger than the noise power, the channel capacity is linearly proportional to the BW, while logarithmically proportional to the SNR. In more advanced CMOS technology with lower minimum transistor gate length, the supply voltage for the thin-oxide transistors becomes lower, while the maximum speed offered by the technology is higher. As the signal amplitude is limited by the supply voltage, the signal power P_S is lower. If the noise power P_N is limited by the thermal noise, the power consumption of the circuit increases by a factor of 4 to reduce the noise by 6 dB [8]. Thus in more advanced CMOS technology, it is usually more power efficient to increase the BW which benefits from the higher speed offered by the technology, to achieve a higher channel capacity C. This trend can be observed

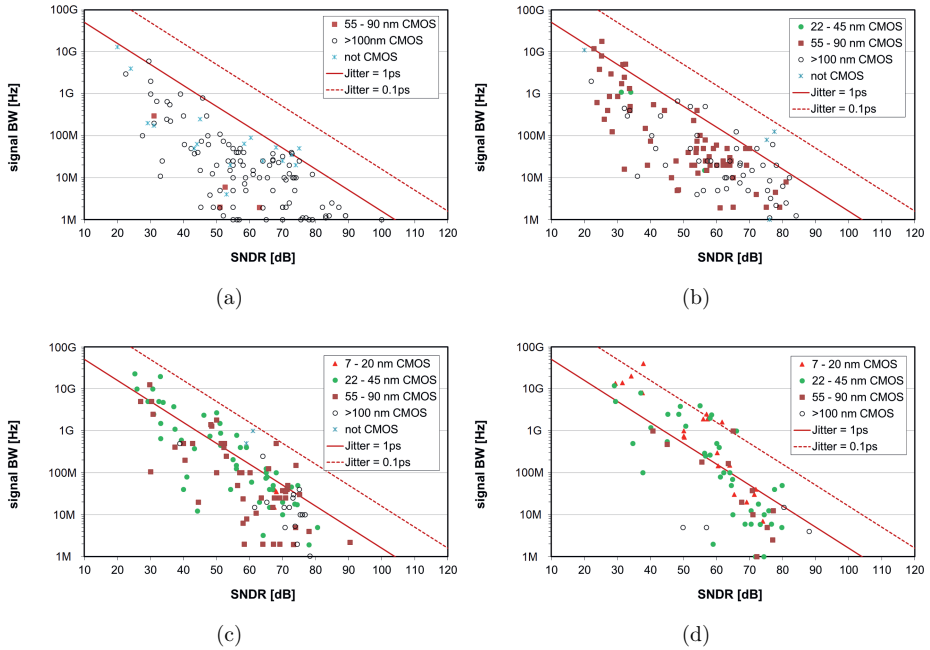


Figure 2.2: Historical overview of the signal BW vs. SNDR plots of the state-of-the-art ADCs with technology information (a) till 2005 (b) from 2006 till 2010 (c) from 2011 till 2015 (d) from 2016 till 2020 (based on [4]).

from Figure 2.2 as well – over the last 15 years, mainly the signal BW of the state-of-the-art ADCs increases, while their signal to noise and distortion ratio stays roughly in the same range. That's why the signal BW in the evolution of many applications is becoming broader and broader.

Actually there is no strict definition about broadband applications and narrow-band applications. They are relative. Firstly, broadband and narrow-band approaches can be defined based on the applications. For example, in the automotive frequency modulation (FM) radio applications, the narrow-band approach is to digitize only one or a few channels, and the corresponding signal bandwidth of the ADC is about a few hundred of kHz. Instead, a broadband approach is to digitize the whole band (e.g. FM and/or digital audio broadcasting (DAB) band), and the corresponding signal bandwidth of the ADC is a few tens of MHz [9].

Secondly, broadband and narrow-band should be defined according to the technology and the state-of-the-art at that time. Figure 2.2 shows the signal BW vs. SNDR plots of the state-of-the-art ADCs within four different time frames with technology information. Till the end of 2005, only a few published ADCs achieved an equiva-

lent sampling jitter error better or equal to 1 ps [10], and most of the ADCs were implemented in > 100 nm CMOS technology. And for medium-to-high resolution ADCs with SNDR $\geq$ 60 dB, the broadest signal BW is 90 MHz [11]. From 2006 till 2010, more ADCs outperformed 1 ps equivalent sampling jitter error, and about half of the ADCs were implemented in 55 - 90 nm CMOS technology. From 2011 till 2015, the best published ADC achieved an equivalent sampling jitter error very close to 0.1 ps [12], and 22 - 45 nm CMOS technology became popular for broadband ADCs. From 2016 till 2020, several published state-of-the-art ADCs already achieve an equivalent sampling jitter error better than 0.1 ps [13], and most of them were implemented in 7 - 45 nm CMOS technology. Moreover, for medium-to-high resolution ADCs with SNDR $\geq$ 60 dB, the broadest signal BW till now is 1.6 GHz [14]. Figure 2.2 shows that state-of-the-art ADCs have been moving towards broader bandwidth in the last two decades, which benefits from higher speed offered by more advanced CMOS technology.

Broadband approaches have many advantages compared to narrow-band approaches. Firstly, the available timing resolution offered by the technology is used. Moreover, the channel selection happens in the digital domain, which benefits from all the advantages of digital processing including perfect matching, low noise, power efficiency and friendly scaling over the technologies.

On the other hand, broadband approaches have some disadvantages. Firstly, speed (or bandwidth) limitations of the building blocks and the integrity of the clock often put limitations on the broadband systems. Moreover, the influence of the interconnect loading and crosstalk can become significant, and the RC delay of the interconnect adds up in the total delay. Last but not least, the in-band and out-of-band interference often places stringent requirements on the dynamic range and linearity of the broadband systems. The challenges for broadband CT $\Sigma\Delta$ ADCs will be studied in detail in Chapter 4.

2.2 Receiver architecture and target specifications for the ADC

In communication systems, a receiver captures the signal when it has passed through the communication channel [15]. The receiver is an essential part in many broadband application systems, e.g. base station for telecommunication, automotive radar, automotive radio, etc [16, 2, 9]. Figure 2.3 shows a simplified functional block diagram of a typical direct-conversion receiver with ADCs [15]. After mixing down and amplified by the baseband filter, the IF signal is filtered. The frequency components at the aliasing frequency need to be suppressed by the anti-aliasing filter, and the out-of-band interference needs to be reduced by the interference filter. After that, an input buffer is used to drive the ADC. After the ADC, a decimation filter is generally needed to remove the out-of-band noise and interference in the digital domain.

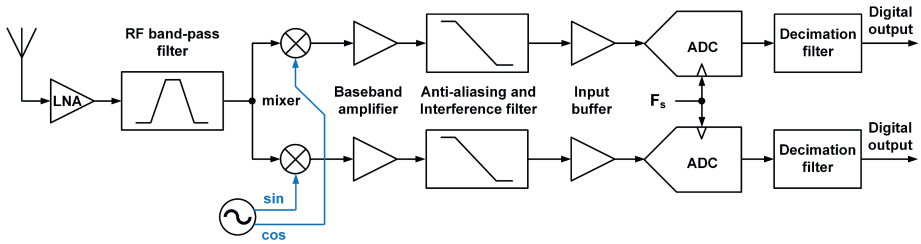


Figure 2.3: Simplified block diagram of a direct-conversion receiver with ADCs [15].

In the recently launched 5G base station transceiver SoC products, ADCs with signal BW 100 - 200 MHz and SNDR 60 - 65 dB are needed in the receivers [1]. This thesis studies the generic design aspects of broadband ADCs on the basis of a target application domain, e.g. future communication and automotive applications. However, the novel concepts and techniques described in Part II are generic, and can be applied to many other broadband applications. In defining the target specifications, not only the application requirements have to be considered, but also what is practically achievable in the technology chosen for the implementation. In this thesis, the broadband ADC is designed in a 40 nm CMOS technology. Considering the speed limitation of this technology, the primary design target for this ADC is chosen to be signal bandwidth of 500 MHz, SNDR $\geq$ 60 dB and dynamic range $\geq$ 63 dB. Further practical system, circuit and technology limitations will be addressed in the following chapters.

Power efficiency is another important criterion. First of all, in some battery-powered (or even cell-battery powered) broadband applications, such as UWB car key applications, the power budget for the ADCs is very limited [17]. On the other hand, even for other broadband applications for which the supply of the power is not such a big concern, such as base station and automotive radar applications, the power consumption of the ADCs is limited by the cooling efficiency of the package. The more power consumption of the ADCs, the more heat is generated, and the more expensive packages with more advanced cooling system are needed.

In the ADC community, two types of figure of merit (FoM) are commonly used:

- Walden FoM [18]:

$$FoM_W = \frac{P}{2 \cdot BW \cdot 2^{\frac{SNDR-1.76}{6.02}}} \quad \text{[J/conversion-step]} \tag{2.3}$$

- Schreier FoM [19]:

$$FoM_S = DR + 10 \cdot \log_{10} \frac{BW}{P} \quad \text{[dB]} \tag{2.4}$$

Table 2.1: ADC main target specifications

Signal bandwidth	500 MHz
Peak SNDR	$\geq$ 60 dB
Dynamic range	$\geq$ 63 dB
Power consumption	$\leq$ 700 mW
Walden FoM	$\leq$ 1 pJ/conv. step
Schreier FoM	$\geq$ 155 dB

In equations (2.3) and (2.4), P is the power consumption of the ADC, BW is the (reported) bandwidth of the ADC, $SNDR$ and DR are in dB. Although the Walden FoM and the Schreier FoM are written in different ways in their equations, they have only two differences. (1) In the Walden FoM SNDR is used to measure the amplitude resolution of the ADC, while in the Schreier FoM DR is used. The Schreier FoM focuses on the noise of the ADCs, and for the Walden FoM both noise and distortion are included. (2) In the Walden FoM the ADC power is doubled when the ADC resolution increases by 6 dB, while in the Schreier FoM the ADC power is quadrupled. The Schreier FoM shows the fundamental relationship between ADC power and ADC resolution because the ADC power is quadrupled to suppress the thermal noise power by 6 dB, while the Walden FoM is based on experimental evidence. Nevertheless, the Walden FoM is suitable for medium-to-low resolution ADCs, while the Schreier FoM is more suitable for high resolution and broadband ADCs [4].

Considering the target applications, the practical limitation from the technology, and the state-of-the-art, the main target specifications for the ADC are chosen and listed in Table 2.1. In Section 2.4, different ADC architectures are compared in the context of these target specifications.

2.3 ADC overview

Analog-to-digital converters can be grouped into different categories. Based on the distribution of the quantization noise in the Nyquist bandwidth, ADCs can be subdivided into Nyquist ADCs and noise-shaping ADCs. Here in this thesis, the Nyquist ADCs are defined as the ADCs with a uniformly distributed quantization noise in the Nyquist bandwidth. On the contrary, the noise-shaping ADCs are defined as the ADCs with a shaped quantization noise in the Nyquist bandwidth.

Because an ideal brick-wall anti-aliasing filter cannot be designed, both Nyquist ADCs and noise-shaping ADCs are oversampled in real receiver applications. The ratio

between half sampling rate and signal bandwidth is defined as oversampling ratio:

$$OSR = \frac{F_s}{2 \cdot BW} \tag{2.5}$$

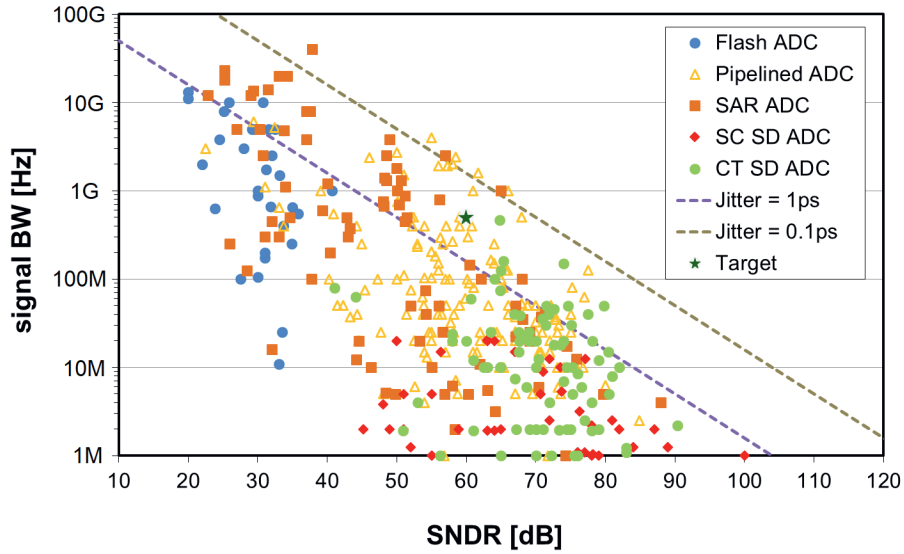
2.3.1 Nyquist ADCs

Common types of Nyquist ADCs are flash ADCs, pipelined ADCs, successive approximation register ADCs, algorithmic ADCs, dual slope ADCs, etc. Time-interleaving is a commonly used technique to increase the bandwidth of the ADC. Figure 2.4 gives an overview of the current state-of-the-art over different ADC architectures (based on [4]). Figure 2.4a shows the signal BW versus peak SNDR plot, and Figure 2.4b presents the Schreier FoM versus signal BW plot. The target specification is indicated as well.

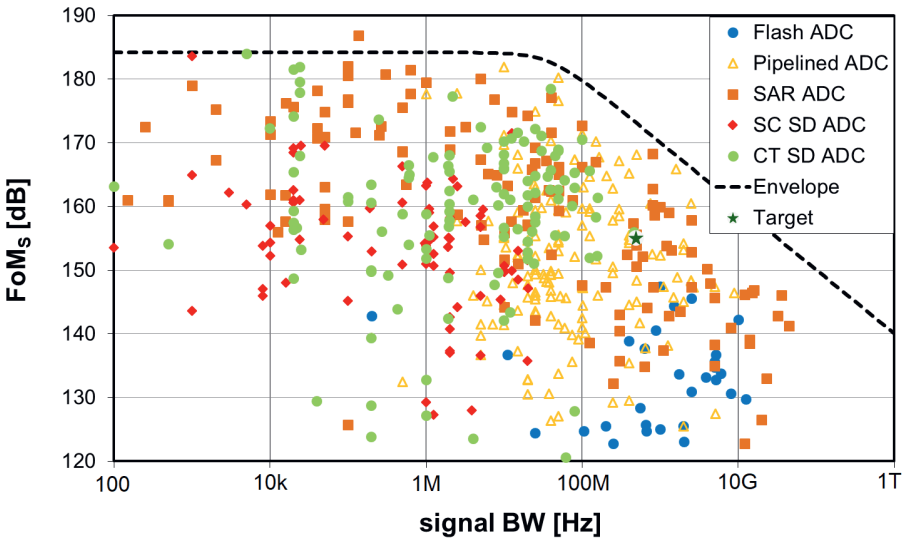
Flash ADCs are suitable for broadband applications, as the throughput time can be (almost) as short as the comparator delay [20]. The main limitation of flash ADCs is that the number of comparators increases exponentially with the number of bits. An N-bit flash ADC requires $2^N - 1$ comparators. Thus, it is power hungry and area consuming. The resolution for Flash ADCs is typically limited to maximally 6-7 bit, as shown in Figure 2.4a. Figure 2.4b shows that the signal BW of the published state-of-the-art flash ADCs is typically between 100 MHz and 10 GHz, with a Schreier FoM between 120 dB and 150 dB.

Pipelined ADCs are commonly used in broadband (BW $\geq$ 10 MHz) medium-to-high resolution (40 dB $\leq$ SNDR $\leq$ 80 dB) applications, as shown in Figure 2.4a [12]. The principle of pipelined ADCs is to achieve the overall resolution with several pipelined stages. Ideally, the overall resolution of the pipelined ADC equals the sum of the resolutions of every stage. The quantization error of every front-end stage is usually amplified by the residue amplifier to the full-scale of the following stage, and then quantized by the following stage. In reality, the resolution and sampling rate of pipelined ADCs are commonly limited by the performance of the residue amplifier (for example gain error and offset). Recently, a continuous-time pipelined ADC was demonstrated which benefits from inherent anti-alias filtering as well [21]. Figure 2.4b shows that pipelined ADCs (including pipelined SAR ADCs) have demonstrated excellent Schreier FoM recently for broadband medium resolution applications [14, 22].

SAR ADCs are widely used mainly thanks to their power efficiency, which is shown in Figure 2.4b [23, 24]. Moreover, a 1-bit-per-cycle SAR ADC is not sensitive to the comparator offset. For low to medium sampling rate (up to tens of MHz), the core of a SAR ADC can be designed without static current consumption. The resolution of a SAR ADC is commonly limited by the accuracy of the matching inside the DAC. For medium to high resolution above 10 ENOB, usually redundancy is added and sophisticated calibration techniques are applied. Time-interleaving can be applied to further increase the signal bandwidth of the SAR ADC [25].



(a)



(b)

Figure 2.4: (a) Signal BW vs. SNDR plot and (b) Schreier FoM vs. signal BW plot for different ADCs (based on [4]). Here flash ADCs include TI flash ADCs; pipelined ADCs includes pipelined SAR ADCs and TI pipelined ADCs; SAR ADCs include TI SAR ADCs.

Figure 2.4a shows that single-channel SAR ADCs are suitable for low-to-medium speed (BW $\leq$ 10 MHz) low-to-medium resolution (SNDR $\leq$ 60 dB) power efficient applications, while adding redundancy and calibration are helpful to increase their resolution, and time-interleaving is useful to increase the ADC BW.

2.3.2 Noise-shaping ADCs

Noise-shaping ADCs trade time resolution for amplitude resolution in a more efficient way considering oversampling than Nyquist ADCs, by filtering of the quantization noise. The signal bandwidth of the noise-shaping ADCs is usually much lower than the Nyquist bandwidth. The common types of noise-shaping ADCs are $\Sigma\Delta$ ADCs and noise-shaping SAR ADCs [26]. This thesis considers voltage-controlled oscillator (VCO)-based ADCs as a type of implementation of $\Sigma\Delta$ ADCs [27].

$\Sigma\Delta$ ADCs are composed of loop filter, quantizer and feedback DACs. They can be further divided into continuous-time $\Sigma\Delta$ ADCs and discrete-time (DT) $\Sigma\Delta$ ADCs, commonly implemented as switched-capacitor (SC) $\Sigma\Delta$ ADCs.

Switched-capacitor $\Sigma\Delta$ ADCs are suitable for narrow-band high resolution applications [28]. The switched-capacitor circuit can achieve high accuracy and high linearity at the same time [29]. Moreover, SC ADCs benefit from the easy scaling of the bandwidth by just changing the sampling clock rate. Their sensitivity to clock jitter is similar as the Nyquist ADCs.

However, compared to continuous-time $\Sigma\Delta$ ADCs, SC $\Sigma\Delta$ ADCs have two main drawbacks: (1) CT $\Sigma\Delta$ ADCs have the inherent anti-aliasing filtering, while SC $\Sigma\Delta$ ADCs (and most of the Nyquist ADCs) need an external dedicated anti-aliasing filter with an input buffer. (2) With the same amplifier unity-gain bandwidth limitation, CT $\Sigma\Delta$ ADCs can achieve much higher sampling rate than SC $\Sigma\Delta$ ADCs. Figure 2.4a shows that the signal bandwidth of the state-of-the-art SC $\Sigma\Delta$ ADCs is limited to about 20 MHz, which is more than 10 times lower than the maximal reported signal bandwidth of CT $\Sigma\Delta$ ADCs. Figure 2.4b shows that most of the SC ADCs have a Schreier FoM between 140 dB and 170 dB.

Continuous-time $\Sigma\Delta$ ADCs are widely used for medium-to-broad bandwidth (BW $\geq$ 1 MHz) and medium-to-high resolution (SNDR $\geq$ 50 dB) applications, as shown in Figure 2.4a [30, 16]. Their loop filters are implemented as continuous-time loop filters. The sampling of the input signal happens at the (input of the) quantizer, which is after the CT loop filter. Thus, CT $\Sigma\Delta$ ADCs benefit from resistive input and inherent anti-aliasing filtering. Compared to ADC architectures with explicit input sample-and-hold circuit, they can relax the anti-aliasing requirement of the input filter, and relax the driving ability requirement of the input buffer [31]. Figure 2.4b shows that CT $\Sigma\Delta$ ADCs have the potential to achieve excellent power efficiency for broadband medium resolution applications [32].

According to the location of the signal band, CT ΣΔ ADCs are further divided into low-pass CT ΣΔ ADCs and band-pass CT ΣΔ ADCs. For some applications, a receiver system with a bandpass ΣΔ ADC shows system-level advantages over the classical IQ receiver with two low-pass ADCs [33, 34]. However, it is too difficult to achieve broadband (BW = 500 MHz), medium resolution (SNDR ≈ 60 dB) and high carrier frequency ($f_c \geq 1$ GHz) at the same time. For example, a band-pass ΣΔ ADC with $f_c = 1$ GHz, BW = 500 MHz and SNDR ≈ 60 dB requires the loop filter amplifier to deliver ≥ 40 dB gain for the frequency 500 MHz - 1.5 GHz, which means a gain-bandwidth product (GBW) of 150 GHz [34]. In this thesis, an inverter-based amplifier is designed to achieve an open-loop GBW of about 12 GHz, with power consumption of 19 mW (details shown in Chapter 11.1). To achieve GBW of 150 GHz, a more complicated circuit for the amplifier has to be investigated, and more power would be spent, which is out of the scope of this thesis. This thesis decides not to choose the BP CT ΣΔ ADC.

2.4 CT ΣΔ ADCs compared to Nyquist ADCs

From Figure 2.4, the target specifications shown in Section 2.2 are promising to be achieved by either CT ΣΔ ADCs or Nyquist ADCs (mainly pipelined ADCs or TI SAR ADCs). To be able to perform the system-level comparison between CT ΣΔ ADCs and Nyquist ADCs, they need to be compared in the context of a typical receiver system, as shown in Figure 2.5.

Figure 2.5a shows the functional block diagram of a part of a typical receiver with a Nyquist ADC with an explicit input S&H circuit. An anti-aliasing filter is needed in this case to suppress the aliased band before the sampling; this filter is used to reduce the out-of-band interference as well. Considering the practical limitation that an ideal brick-wall anti-aliasing filter cannot be designed, the usable signal bandwidth of the Nyquist ADC is typically 1/2 to 1/4 of the Nyquist bandwidth [31, 35]. Figure 2.5a considers an optimistic OSR of 2 for the Nyquist ADC. Thus to achieve the target specifications (signal BW = 500 MHz and SNDR = 60 dB in the signal BW), a Nyquist ADC with a sampling rate of $F_S = 2$ GHz and SNDR = 57 dB for the Nyquist BW is needed, considering the noise is uniformly distributed in the Nyquist BW. In this case, even with a very sharp 6th order LP filter as the anti-aliasing filter with all the poles at the signal band-edge (500 MHz), the suppression is only 39 dB for the worst-case frequency (1.5 GHz). Moreover, the signal is suppressed by 18 dB at the band-edge compared with low frequency, which is not desired for most of the applications as well. The sampling capacitance C_S has to be large enough to suppress the sampled thermal noise. The available tracking time is usually only part of the sampling clock period. Together with the sampling accuracy, they put a very stringent requirement on the bandwidth of the S&H circuit and the driving ability of the input buffer, which is typically the same amplifier used in the anti-aliasing filter in the implementation. Both of the amplifier in the anti-aliasing filter and the S&H

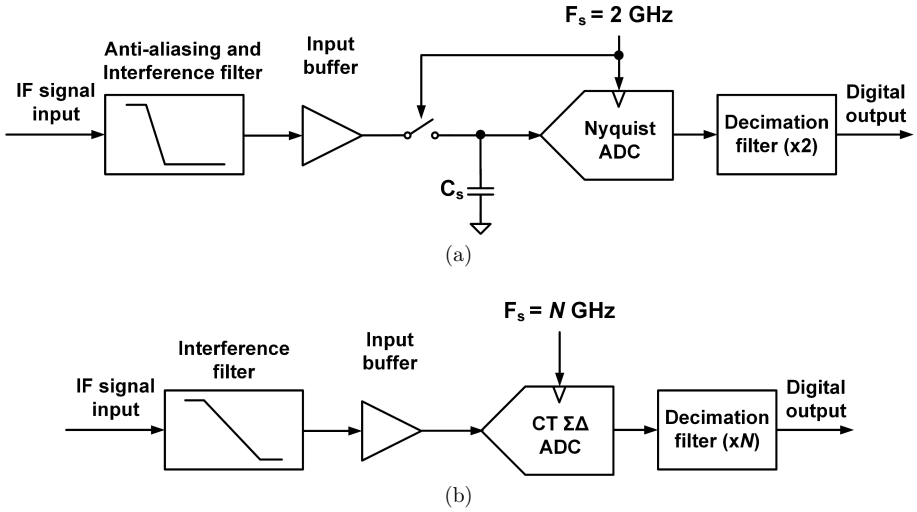


Figure 2.5: Part of a typical receiver with (a) a Nyquist ADC and (b) a CT ΣΔ ADC.

circuit must be linear enough, as their non-linearity directly intervenes with the ADC input. The clock distribution and the decimation filter add up in the total power consumption of this part of the receiver.

On the other hand, Figure 2.5b shows the corresponding part of a typical receiver with a CT ΣΔ ADC with OSR = N. Here a practical low OSR of about 7 is considered, which is based on a system-level design trade-off and will be explained in detail in Chapter 5. Please notice that the chosen 40 nm CMOS technology can offer the required speed of 7 GHz sampling rate for the CT ΣΔ ADC. Compared to the receiver with a Nyquist ADC, the extra speed is utilized by an SDM to achieve the resolution target via the noise shaping followed by the exchange of speed to resolution in the decimation filter. The inherent anti-aliasing filtering of a broadband medium resolution CT ΣΔ ADC is typically more than 60 dB for the worst case frequency, which is often more than the requirement of the applications. For some applications, a LP interference filter is needed to suppress the strong out-of-band interference in front of the CT ΣΔ ADC, such that the possible strong out-of-band interference does not limit the dynamic range of the ADC. The order of this interference filter can be much less than the anti-aliasing filter needed in Figure 2.5a, as the residue of the possible out-of-band interference that is not in the aliased band will be removed by the decimation filter. Moreover, CT ΣΔ ADCs typically have a resistive input. The input resistance for the target specification is about 500 Ω. The driving ability requirement for the input buffer is strongly relaxed compared to the receiver system in Figure 2.5a. Nevertheless, the CT ΣΔ ADC requires a sampling clock with a higher frequency and a more stringent clock jitter requirement. The decimation filter is running at a higher clock frequency, which consumes more power than in the case

Table 2.2: Comparison between receivers with a Nyquist ADC and with a CT ΣΔ ADC

Comparison item	Receiver with a Nyquist ADC	Receiver with a CT ΣΔ ADC
Anti-aliasing and interference filter	☹ stringent	☺ relaxed
Input buffer	☹ capacitive input	☺ resistive input
S&H circuit	☹ required	☺ not required
Clock	☺ lower frequency	☹ higher frequency
Decimation filter	☺ less power	☹ more power

of Figure 2.5a.

Table 2.2 summarizes the comparison. This chapter shows a qualitative comparison, and a quantitative comparison will be given in Chapter 11.4. A CT ΣΔ ADC relaxes the requirement of the anti-aliasing and interference filter, and relaxes the driving ability requirement of the input buffer. The receiver with a CT ΣΔ ADC does not need an S&H circuit preceding the ADC. However, the power consumption of the clock distribution and the decimation filter is higher. Overall, it is promising to achieve a lower total receiver power with a CT ΣΔ ADC compared to a Nyquist ADC.

2.5 Increasing the bandwidth of CT ΣΔ ADCs

The previous section presents that CT ΣΔ ADCs have many advantages compared to Nyquist ADCs, including inherent anti-aliasing filtering, resistive input, and omitting the input S&H circuit. These properties can simplify the receiver architecture, and benefit the system integration. This is the main reason why many modern broadband receiver applications, with the whole receiver (or transceiver, or a larger system including the digital circuitry) integrated on one chip, use CT ΣΔ ADCs [1, 2, 9].

Figure 2.4a shows that the signal BW of most of the state-of-the-art CT ΣΔ ADCs is limited to around 150 MHz. The motivation of this thesis is to bring the advantages of CT ΣΔ ADCs to a broader bandwidth. The target ADC signal bandwidth in this thesis is 500 MHz.

In the following chapters, broadband CT ΣΔ ADCs refer to the ADCs with signal BW and peak SNDR performance beyond the 'Jitter = 1 ps' line in Figure 2.4a. For the target specifications and applications of this thesis, broadband CT ΣΔ ADCs can be interpreted as ADCs with signal BW higher or equal to 100 MHz as well (with DR $\geq$ 60 dB).

2.6 Conclusions

The signal bandwidth in many communication and automotive applications has been increasing exponentially in the last few decades. ADCs with broader bandwidth have been developed in the same time, which make use of the speed advantage of more advanced technology. ADCs can be subdivided into Nyquist ADCs and noise-shaping ADCs based on the distribution of the quantization noise in the Nyquist bandwidth. $\Sigma\Delta$ ADCs trade time resolution for amplitude resolution in an efficient way by means of aggressive filtering of the quantization noise. Continuous-time low-pass $\Sigma\Delta$ ADCs are promising for the target specifications thanks to their resistive input, inherent anti-aliasing filtering and potential for broad bandwidth. Compared to a receiver with a Nyquist ADC with explicit S&H circuit, a CT $\Sigma\Delta$ ADC can relax the requirements on the anti-aliasing and interference filter, and input buffer. Moreover, it does not require an S&H circuit in front of the ADC. Although it leads to higher power consumption in clocking and decimation filter, the total receiver power with a CT $\Sigma\Delta$ ADC is promising to be lower. The motivation of this thesis is to bring the advantages of CT $\Sigma\Delta$ ADCs to a broader bandwidth.

Chapter 3

Architecture choices for broadband CT ΣΔ ADCs

This chapter elaborates on the architecture design choices for broadband CT ΣΔ ADCs. It is part of the top-down approach of the broadband CT ΣΔ ADC design. Firstly, this chapter gives a general description and definition for CT SDMs. Afterwards, this chapter discusses SDM parameter design choices and topology design choices separately. The SDM parameter design choices include noise transfer function order, quantizer resolution, OSR, zero optimization and out-of-band gain. The stability of the SDM is discussed as well. The SDM topology design choices contain single-loop, MASH and Sturdy MASH SDMs. As there are multiple trade-offs among the SDM parameter and topology choices, the chapter further reviews and benchmark the state-of-the-art broadband medium-to-high resolution CT ΣΔ ADCs to learn from them. In the end, the SDM parameter design space is reduced and conclusions are drawn.

3.1 CT SDM general description and definition

This section starts with a general description and definition for CT SDMs. A simplified block diagram of a CT SDM is shown in Figure 3.1a. Here a single-loop SDM is taken as an example. A CT SDM contains a continuous-time loop filter, a quantizer and one or more feedback DACs. They compose a negative feedback loop. Although a multi-bit quantizer is drawn in Figure 3.1a, the quantizer can be a 1-bit quantizer as well. The CT loop filter has a transfer function $H_s(s)$ for SDM input U, and a transfer function $H_n(s)$ for the feedback DAC output after taking the inverse sign.

Both the linear and non-linear characteristics of the CT SDM need to be considered. This section starts with the linear characteristics. Usually, designers use a linear model to analyze the CT SDM, which is depicted in Figure 3.1b. In the linear model,

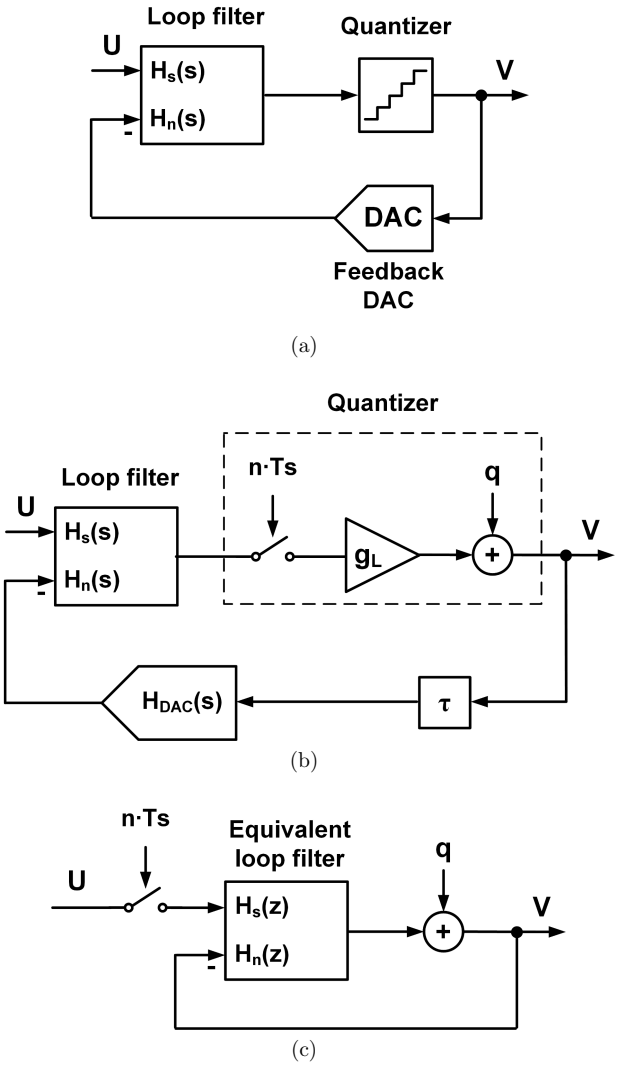


Figure 3.1: (a) Simplified block diagram of a CT SDM [19] (b) CT linear model of the SDM (c) Equivalent DT model of the SDM (based on [36]).

the CT loop filter is modelled as its continuous-time transfer functions $H_s(s)$ and $H_n(s)$. The quantizer is modelled as a sampler, a linear gain g_L and a quantization noise q. The DAC is modelled as its continuous-time transfer function $H_{DAC}(s)$, which takes the DAC pulse into account. The total delay of the feedback loop, including the quantizer delay, DAC delay and the propagation delay from quantizer to DAC, is modeled as a delay τ. In the linear model, the non-linear characteristic of the CT

SDM is ignored.

Most of the theories and analysis on the noise shaping and stability of the SDMs are done in discrete-time domain. For the purpose of analysis and design of the NTF, the equivalent discrete-time SDM model can be calculated, which is shown in Figure 3.1c. The equivalent DT loop filter transfer function for the quantization noise $H_n(z)$ can be calculated, taking into account the CT loop filter $H_n(s)$, DAC pulse $H_{DAC}(s)$, loop delay τ, and quantizer linear gain g_L. Impulse invariant transformation can be applied to guarantee that for the quantization noise q, the CT SDM model and equivalent DT SDM model have the same value for every sampled quantizer input at n·T_S [36]. A detail CT to DT transformation for a CT MASH SDM is given in Chapter 5.2. Notice that the DT SDM is equivalent to the CT SDM only for the quantization noise transfer function, but not for the signal transfer function (STF).

The noise transfer function is defined as the transfer function from the quantization noise q to the SDM output V, which can be calculated as:

$$NTF(z) = \frac{1}{1 + H_n(z)} \tag{3.1}$$

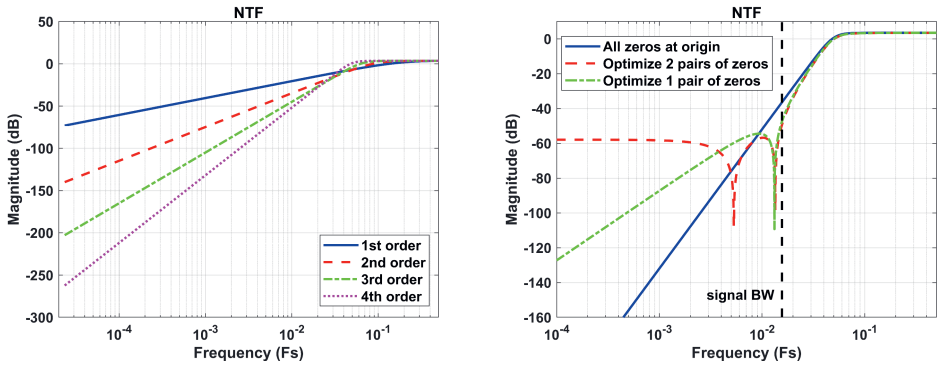
The shape of the NTF is mainly influenced by 4 parameters – NTF order, OBG, OSR and optimized zeros. Actually, the definition on the design parameters of the NTF and the resulting properties of the NTF depends on the synthesis flow of the NTF and the SDM as well. This thesis assumes the NTF is directly synthesized using the Delta Sigma toolbox [37]. NTF order is defined as the number of zeros in the NTF(z). OBG is defined as the magnitude of the NTF at the frequency of $\frac{F_s}{2}$, which is referred as H_{inf} in the literature as well. If the NTF order is higher or equal to two, one or more pairs of NTF zeros can be designed to be at an optimized frequency instead of DC, which gives more aggressive in-band noise shaping. This technique is referred as zero optimization. In this thesis, "more aggressive" in-band noise shaping means the in-band quantization noise is suppressed more strongly (same definition as [19]).

The signal transfer function is defined as the transfer function from the SDM input U to the SDM output V. For a CT SDM, the STF is a combined transfer function of s-domain and z-domain, because the input of the SDM is not sampled. This thesis gives an approximation of the STF for the CT SDM model in Figure 3.1b as:

$$STF(z) \approx \mathcal{Z}\Big\{\mathcal{L}^{-1}\Big\{H_s(s)\Big\}_{t=n}\Big\} \cdot g_L \cdot NTF(z) \tag{3.2}$$

Since $H_s(s)$ and $H_n(s)$ can be designed separately, the STF can be optimized independently from the NTF.

The non-linear characteristic of the ideal CT SDM model is due to the quantizer. Especially a 1-bit quantizer shows strong non-linear behavior, and its linear gain g_L is arbitrarily defined [19]. A multi-bit quantizer shows less non-linearity compared with a 1-bit quantizer, and its linear gain g_L is well defined. The non-linear characteristic of the quantizer is modeled as its phase and gain uncertainty as well [38].



(a) (b)

Figure 3.2: (a) NTF with different order (b) NTF with and without optimized zeros (CRFF or CRFB structure used here). The Delta Sigma toolbox is used [37].

3.2 SDM parameter design choices and related loop properties

This section discusses the SDM parameter design choices, including NTF order, zero optimization, quantizer resolution, OBG and OSR. Afterwards, the stability of the SDMs is addressed.

3.2.1 NTF order

The NTF order directly influences the slope of the NTF. Figure 3.2a shows the NTF magnitude from 1st order to 4th order, assuming the OBG = 1.5 and all the NTF zeros are at DC. For an Nth order loop filter, the NTF has a slope of $20 \cdot N$ dB/decade in the low frequency band. Table 3.1 shows the synthesized NTFs and summarizes the simulated SQNR for sine input with frequency $f_{in} = 0.0051\ F_S$ and amplitude $A_{in} = 0.5\ V_{ref}$ such that the quantizer is not overloaded. OSR = 32 in this simulation. The SQNR increases from 38.5 dB to 61.6 dB when NTF order increases from 1st order to 4th order.

3.2.2 Zero optimization

Figure 3.2b presents the 4th order NTF magnitude of three cases: (1) with all zeros at DC (2) with 2 pairs of zeros at optimized frequency (3) with 1 pair of zeros at optimized frequency and the other pair of zeros at DC. For all the three cases, OSR

Table 3.1: SQNR comparison for different NTF order

NTF order	quantizer	NTF(z)	SQNR
1st order	1-bit	$\frac{z-1}{z-0.3333}$	38.5 dB
2nd order	1-bit	$\frac{(z-1)^2}{z^2-1.225z+0.4415}$	51.2 dB
3rd order	1-bit	$\frac{(z-1)^3}{(z-0.6694)(z^2-1.531z+0.6639)}$	59.2 dB
4th order	1-bit	$\frac{(z-1)^4}{(z^2-1.493z+0.5647)(z^2-1.702z+0.7871)}$	61.6 dB

For all NTFs, OSR = 32, OBG = 1.5, no zero optimization. Simulated SQNR for sine input with frequency f_{in} = 0.0051 F_S and amplitude A_{in} = 0.5 V_{ref}.

Table 3.2: SQNR comparison with and without optimized zeros

NTF order	optimized zeros?	NTF(z)	SQNR
4th order	no	$\frac{(z-1)^4}{(z^2-1.493z+0.5647)(z^2-1.702z+0.7871)}$	61.6 dB
4th order	1 pair of zeros optimized	$\frac{(z-1)^2(z^2-1.993z+1)}{(z^2-1.491z+0.5633)(z^2-1.7z+0.7863)}$	73.4 dB
4th order	2 pairs of zeros optimized	$\frac{(z^2-1.999z+1)(z^2-1.993z+1)}{(z^2-1.49z+0.563)(z^2-1.7z+0.7861)}$	75.8 dB

For all NTFs, OSR = 32, OBG = 1.5. 1-bit quantizer is used. Simulated SQNR for sine input with frequency f_{in} = 0.0051 F_S and amplitude A_{in} = 0.5 V_{ref}.

= 32 and OBG = 1.5 are used. Optimized zeros can greatly suppress the in-band quantization noise close to the band-edge. Table 3.2 shows the corresponding NTFs and simulated SQNR for these three cases for sine input with frequency f_{in} = 0.0051 F_S and amplitude A_{in} = 0.5 V_{ref}. One pair of optimized zeros increases the SQNR from 61.6 dB to 73.4 dB. 2 pairs of optimized zeros further increase the SQNR to 75.8 dB.

3.2.3 Quantizer resolution

Quantizer resolution is an important parameter in the ΣΔ ADC architecture design. On one hand, ΣΔ ADCs with 1-bit quantizer is not sensitive to comparator offset and its 1-bit feedback DAC is inherently linear. On the other hand, multi-bit quantization offers a lower original unshaped quantization noise. Multi-bit quantizers have lower original unshaped quantization noise and a well-defined linear gain compared to a 1-bit quantizer. Thus, with the same targeted maximum stable input amplitude (MSA), the applicable out-of-band gain (OBG) is higher for SDMs with multi-bit quantizers than SDMs of the same order with a 1-bit quantizer, achieving a more aggressive noise shaping (see Section 3.2.4). This thesis refers to this property in the sense that SDMs with multi-bit quantizers are "more stable" than SDMs with a 1-bit quantizer

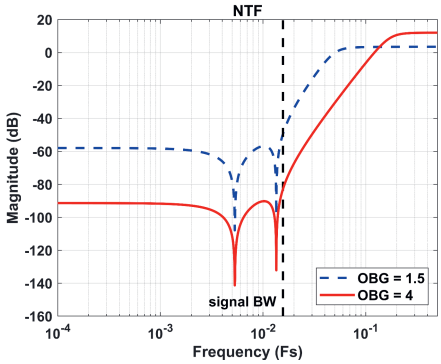


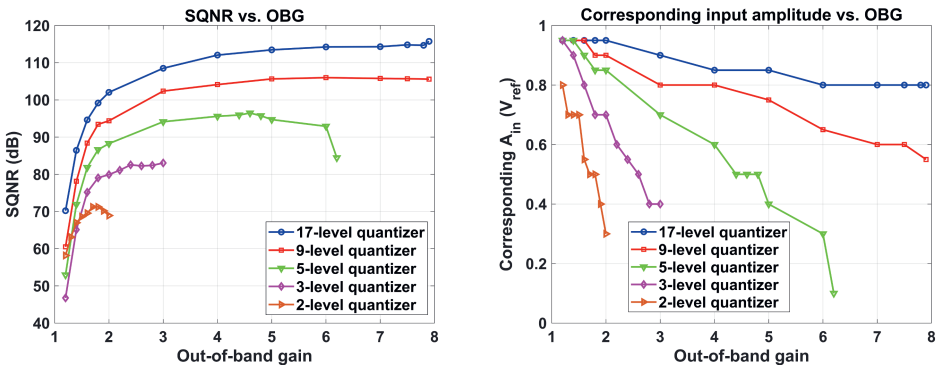
Figure 3.3: 4th order NTF with OBG = 1.5 and 4. Both with 2 pairs of optimized zeros. OSR = 32. CRFF or CRFB structure.

(same definition of "stable" as in [19]).

3.2.4 Out-of-band gain

Loop stability and aggressiveness of filter are related to the loop filter order and OBG. OBG indicates how much the high frequency quantization noise is amplified at $\frac{F_s}{2}$. For N^{th} order loop filter, the theoretical maximal OBG is 2^N when the NTF is designed with a flat transfer function close to $\frac{F_s}{2}$. Since high-order (loop filter order $\geq$ 3) 1-bit SDMs cannot tolerate too much amplification of high frequency quantization noise, their maximal applicable OBG is typically less than 2 [39]. For SDMs with multi-bit quantization, the applicable OBG is much larger. Figure 3.3 shows two 4th order NTFs, one with OBG = 1.5 and the other with OBG = 4. The NTF with OBG = 4 has more aggressive noise shaping, and its in-band quantization noise level is about 33 dB lower than OBG = 1.5.

Theoretically, when the quantizer resolution increases by 1 bit, the original unshaped quantization noise reduces by 6 dB. Moreover, multi-bit quantization allows to use higher OBG than 1-bit quantization, which further improve the SQNR. Figure 3.4a shows the peak SQNR versus OBG, for a 3rd order SDM in cascade-of-integrators, feedforward form (CIFF) with different quantizer resolution. Figure 3.4b shows the corresponding input amplitude to achieve peak SQNR for every case. With the same quantizer resolution, when OBG increases, the high frequency quantization noise is amplified more. Thus, when OBG increases, the maximum stable input amplitude (MSA) of the SDM is reduced. In practice, the peak SQNR should be achieved for an input amplitude higher or equal to 0.5 V_{ref}, otherwise it implies that too much quantization noise is in the system. For the simulated 3rd order CIFF structure, with 1-bit quantizer, the maximum SQNR is 71 dB with OBG = 1.7. On the other hand, for a 17-level quantizer, the maximum SQNR is more than 114 dB, which can be



(a) (b)

Figure 3.4: (a) SQNR vs. OBG with 2-level to 17-level quantizers (b) The corresponding input amplitude. 3rd order CIFF structure. OSR = 32. f_{in} = 0.001 F_S.

achieved with OBG from 6 to 7.9.

3.2.5 OSR

OSR is another important design parameter. Equation (2.5) shows that for a given signal BW, OSR is proportional to F_S. For narrow-band high-resolution (SNDR $\geq$ 80 dB) $\Sigma\Delta$ ADCs, typically a high OSR ($\geq$ 30) is used, to suppress the in-band quantization noise [40]. For broadband medium-resolution (50 dB $\leq$ SNDR $\leq$ 70 dB) $\Sigma\Delta$ ADCs, since the sampling frequency F_S is limited by the maximum speed offered by the technology, usually a relatively low OSR ($\leq$ 30) is used [16].

Figure 3.5 shows two 4th order NTFs with OSR = 8 and 32, respectively. When OSR increases, the in-band quantization noise is suppressed more. Table 3.3 shows that for 4th order SDMs with 3-bit quantizer, when OSR increases from 8 to 32, SQNR increases from 67.6 dB to 121.4 dB (for input amplitude A_{in} = 0.5 V_{ref}).

3.2.6 Stability

The stability analysis of the SDM can be found in the literature [19]. For this analysis both the linear model of the SDM and the non-linearity of the quantizer need to be considered. Firstly, the calculation of NTF is based on the linear model of SDM. The linear model of SDM ignores the non-linearity of the quantizer. Especially for 1-bit quantizer, its non-linearity is much higher than multi-bit quantizer. This thesis only gives some guidelines which are useful in the practical design of broadband CT $\Sigma\Delta$ ADCs.

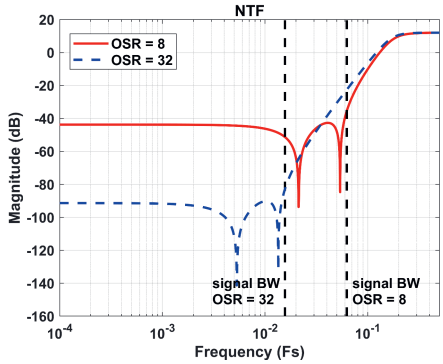


Figure 3.5: 4th order NTF with OSR = 8 and 32. Both with 2 pairs of optimized zeros. OBG = 4. CRFF or CRFB structure.

Table 3.3: SQNR comparison for different OSR

NTF order	quantizer	OSR	NTF(z)	SQNR
4th order	3-bit	8	$\frac{(z^2-1.982z+1)(z^2-1.887z+1)}{(z^2-0.7131z+0.1458)(z^2-0.6831z+0.3985)}$	67.6 dB
4th order	3-bit	32	$\frac{(z^2-1.999z+1)(z^2-1.993z+1)}{(z^2-0.7288z+0.1516)(z^2-0.7145z+0.4083)}$	121.4 dB

For all NTFs, OBG = 4 and 2 pairs of zeros are optimized. Simulated SQNR for sine input with frequency f_{in} = 0.325·BW and amplitude A_{in} = 0.5 V_{ref}. CRFF or CRFB structure.

- In general, higher-order SDMs have a worse stability than lower-order SDMs. 1st order SDMs are always stable with DC input with an amplitude less than the DAC full-scale. 1st order and 2nd order SDMs have much better stability than high-order SDMs with order ≥ 3 [19].

- In general, multi-bit quantization has better stability than 1-bit quantization. The reason it that multi-bit quantization has less original unshaped quantization noise, and it has a well-defined linear gain as well.

- In general, higher OBG leads to worse stability. However, for SDMs with loop filter order ≥ 2 with multi-bit quantization, too low OBG (< 2) makes the SDM tonal. In practice, high-order (≥ 3) 1-bit SDMs typically have OBG around 1.5, which is a trade-off between maximizing peak SQNR and limiting the amplification of high-frequency quantization noise. SDMs with loop filter order ≥ 2 and multi-bit ($\geq$ 2-bit) quantization usually have OBG ≥ 2 (see Figure 3.4).

As the feedback DACs have a fixed output full scale, the total output power of the DAC feedback is limited. This total power contains signal power and a shaped

quantization noise power. If the SDM input signal power is above the maximal allowed signal power of the SDM, the SDM is overloaded. Applications typically require that the SDM should recover from the overloading after the input overloading condition is removed, which is called overloading recovery. Automatic overloading recovery is generally achieved by 1st order and 2nd order SDMs without specific design, which is not the case for high-order (≥ 3) SDMs [41]. For high order SDMs, the overloading recovery can be achieved usually by two ways. The first way is to reset the loop filter internal nodes when the SDM overloading is detected. The second way is to put clippers at the loop filter internal nodes, such that when the overloading happens the SDM works as a 1st order SDM.

3.3 SDM topology design choices

This section further discusses the topology choice between single-loop, MASH, and Sturdy MASH SDMs.

3.3.1 Single-loop SDMs

SDMs with only one Sigma-Delta loop are called single-loop SDMs, such as the SDM shown in Figure 3.1a [30]. Single-loop SDMs typically have only one quantizer and one loop filter. The order of the NTF and the quantizer resolution are still design freedoms. Single-loop SDMs are widely used in many applications because of their simplicity compared to the MASH structure.

3.3.2 MASH

MASH SDMs are referred as cascaded SDMs as well in the literature [42]. They have more than one Sigma-Delta loop. Figure 3.6 shows the simplified block diagram of an exemplary CT MASH SDM. In this figure a MASH SDM containing two Sigma-Delta loops is shown as an example, in practice a MASH SDM can contain 3 or more Sigma-Delta loops. The principle of MASH SDM is that the quantization noise of the 1st loop is the input of the 2nd loop. The following equations are valid for the CT MASH SDM shown in Figure 3.6:

$$V_1 = STF_1(z) \cdot U + NTF_1(z) \cdot q_1 \tag{3.3}$$

$$V_2 = STF_2(z) \cdot U_2 + NTF_2(z) \cdot q_2 \tag{3.4}$$

$$U_2 = -a_{12} \cdot q_1 \tag{3.5}$$

Here, $STF_1(z)$ and $NTF_1(z)$ are the STF and NTF of the 1st loop, and $STF_2(z)$ and $NTF_2(z)$ are the STF and NTF of the 2nd loop. q_1 and q_2 are the quantization noise of the 1st and 2nd loop. a_{12} is a gain between 2 Sigma-Delta loops, which is called

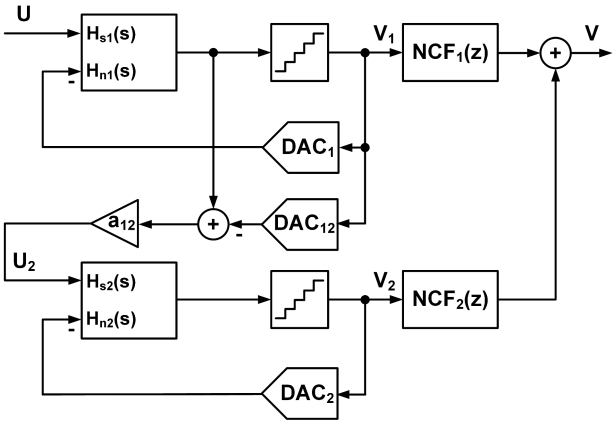


Figure 3.6: Simplified block diagram of a CT MASH SDM.

inter-stage gain (ISG). Here for simplicity, the total delay of 1st quantizer and DAC_{12} is considered to be much lower than the sampling clock period T_S and is neglected.

In this case, the following noise cancellation filter (NCF) can be applied:

$$NCF_1(z) = STF_2(z) \tag{3.6}$$

$$NCF_2(z) = \frac{NTF_1(z)}{a_{12}} \tag{3.7}$$

And the final SDM output can be calculated as:

$$\begin{aligned} V &= NCF_1(z) \cdot V_1 + NCF_2(z) \cdot V_2 \\ &= STF_1(z) \cdot STF_2(z) \cdot U + \frac{1}{a_{12}} NTF_1(z) \cdot NTF_2(z) \cdot q_2 \end{aligned} \tag{3.8}$$

Thus, the quantization noise of the 1st Sigma-Delta loop is completely canceled, and the quantization noise of the 2nd Sigma-Delta loop is shaped by the total order of both Sigma-Delta loops and the inter-stage gain. Typically multi-bit quantizers are used in the MASH SDMs [16]. Since the swing of the original unshaped quantization noise q_1 is lower than the maximal input swing of the 2nd loop, an ISG a_{12} of larger than one can be applied to amplify the swing of q_1. Applying ISG of larger than one further increases the SQNR.

MASH SDMs have two main advantages compared to single-loop SDMs. First, MASH SDMs can be built from 1st and 2nd order Sigma-Delta loops, which have much better stability than high-order (≥ 3) Sigma-Delta loops. Thus, MASH SDMs can achieve high-order noise shaping and maintain good stability as 1st and 2nd order SDMs. Second, when multi-bit quantizers are used in the MASH SDMs, inter-stage gains of larger than one can be applied which can further increase the SQNR.

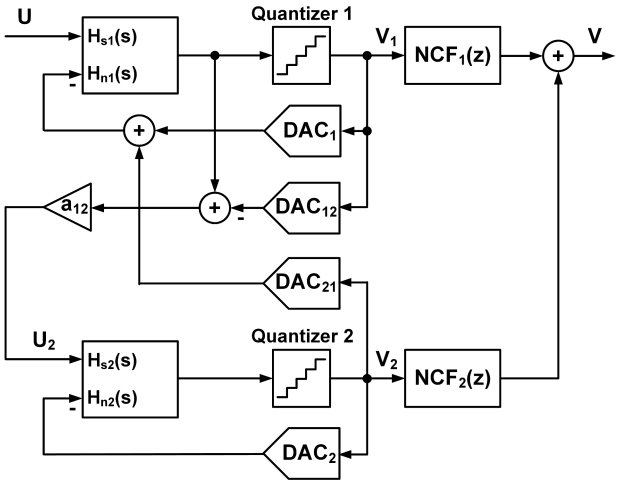


Figure 3.7: Simplified block diagram of a CT Sturdy MASH SDM.

MASH SDMs have some drawbacks. First, they need noise cancellation filters to remove the quantization noise of all Sigma-Delta loops except for the last loop, which are not required by the single-loop SDMs. Second, the design of MASH SDMs is generally more complicated than single-loop SDMs, especially regarding circuit non-idealities, such as excess-loop-delay compensation, analog and digital filter mismatch, parasitic poles and extra phase shift in the loop, etc. An overview of the challenges and non-idealities in broadband CT $\Sigma\Delta$ ADCs is given in Chapter 4. MASH SDMs are generally used to achieve broader BW and/or higher SNDR than single-loop SDMs at the cost of increased complexity.

3.3.3 Sturdy MASH

An architecture called 'Sturdy MASH' was proposed, in which the quantizer output of the 2nd loop is added back in the 1st loop, to simplify the noise cancellation filter and to relax the analog and digital loop filter matching requirements [43, 44]. It has been demonstrated for broadband CT $\Sigma\Delta$ ADCs [45, 46]. Figure 3.7 presents a simplified block diagram of a CT Sturdy MASH SDM [45]. Compared to the standard MASH structure, the noise cancellation filter of a Sturdy MASH is simpler. The matching requirement between the analog filter and digital NCF is relaxed.

The Sturdy MASH proposed in [44] has two main drawbacks. This section takes a Sturdy MASH with two Sigma-Delta loops as an example. First, the quantization noise of the 1st loop is not canceled for the Sturdy MASH, but shaped by the total order of 1st and 2nd loops. In this case, the final output of Sturdy MASH contains the quantization noise of both 1st and 2nd loop. Though inter-stage gain can be applied

in the Sturdy MASH, it only suppresses the quantization noise of the 2nd loop. Thus, the improvement on SQNR from the ISG is much reduced, compared to standard MASH. Second, the quantization noise of the 2nd loop is added in the 1st loop in Sturdy MASH. Thus, in the 1st loop the total power of unshaped quantization noise is higher, and only less aggressive NTF can be used for the 1st loop. Because of these two drawbacks, the achievable SQNR of a Sturdy MASH is lower than the standard MASH for the same loop filter order and quantizer resolution.

The CT Sturdy MASH demonstrated in [45, 46] has one additional drawback, which limits its application for very-broad-band ADCs. The total excess loop delay in the single-loop or MASH SDMs can be calculated as (see Chapter 4.5):

$$\tau_{ELD,S.L.\ or\ MASH} = \tau_Q + \tau_{DAC} \tag{3.9}$$

Here, τ_Q is the quantizer delay, and τ_{DAC} is the DAC delay. The propagation delay from the quantizer to the DAC is considered as part of τ_{DAC}.

In the CT Sturdy MASH, the quantizer output of the 2nd loop is added back in the 1st loop. In Figure 3.7, one feedback loop contains Quantizer 1, DAC_{12}, Quantizer 2 and DAC_{21}. Thus, the total ELD in the loop is:

$$\tau_{ELD,SMASH} = \tau_{Q1} + \tau_{DAC12} + \tau_{Q2} + \tau_{DAC21} \tag{3.10}$$

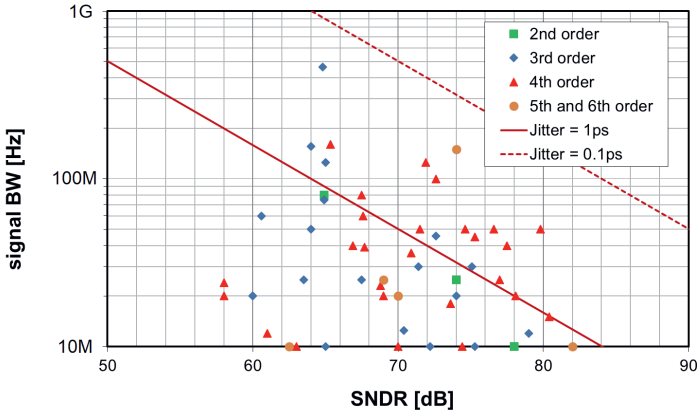
Here, τ_{Q1} is the delay of quantizer 1, τ_{DAC12} is the delay of DAC_{12}, τ_{Q2} is the delay of quantizer 2, and τ_{DAC21} is the delay of DAC_{21} [45, 46].

Assuming the same quantizer delay and the same DAC delay for CT single-loop, MASH and Sturdy MASH SDMs (considering the same technology, same metastability requirements, etc.), the highest achievable sampling rate of the CT single-loop or MASH SDMs is two times of that of the CT Sturdy MASH SDMs. In the literature, the highest sampling rate for multi-bit CT MASH (and single-loop) SDMs is 8 GHz [16], and the highest sampling rate for multi-bit CT Sturdy MASH SDMs is 1.8 GHz [45] ([16] and [45] are both in 28 nm CMOS). This drawback limits the application of CT Sturdy MASH for very-broad-band ΣΔ ADCs, for which the sampling rate has to be maximized to achieve the target very broad signal bandwidth.

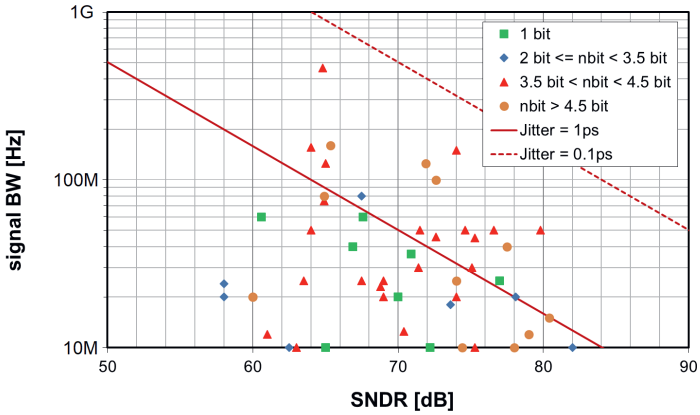
3.4 Benchmarking different ΣΔ ADCs

The previous sections show that the design of CT SDM contains a lot of trade-offs between aggressiveness of noise shaping, stability and system complexity. Chapter 4 shows more trade-offs on noise, linearity, power and circuit complexity. Thus, looking at the state-of-the-art broadband medium-to-high resolution CT ΣΔ ADCs for their SDM parameter and topology design choices is helpful and beneficial for our design.

Figure 3.8 and Figure 3.9 present the signal BW vs. SNDR plot for the state-of-the-art broadband (BW $\geq$ 10 MHz) medium-to-high resolution (SNDR $\geq$ 50 dB) CT



(a)

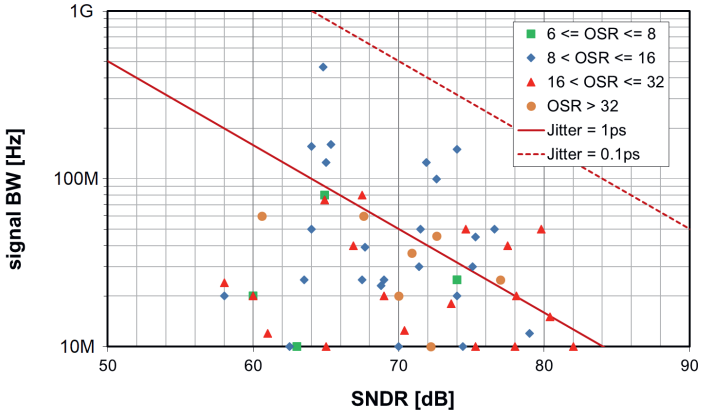


(b)

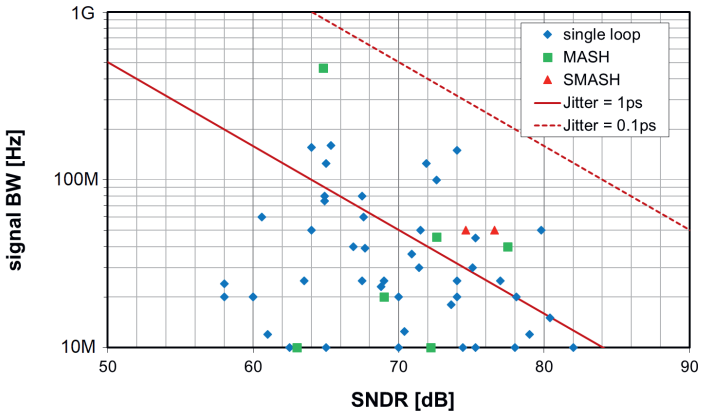
Figure 3.8: Signal BW vs. SNDR plot for CT ΣΔ ADCs with BW $\geq$ 10 MHz and SNDR $\geq$ 50 dB: (a) grouped by NTF order (b) grouped by quantizer resolution (based on [4]). Here NTF order is the total order including loop filter order and noise-shaping of quantizers. For a MASH/SMASH structure, NTF order is the total effective noise-shaping order of the MASH/SMASH. If more than one quantizer is used, the highest resolution is shown in (b).

ΣΔ ADCs (based on [4]). Here, all of the 53 reported CT ΣΔ ADCs are grouped according to 4 categories: (1) NTF order (2) quantizer resolution (3) OSR and (4) single-loop/MASH/SMASH.

Figure 3.8a shows the NTF order. About 85% of these ΣΔ ADCs have a total NTF



(a)



(b)

Figure 3.9: Signal BW vs. SNDR plot for CT ΣΔ ADCs with BW $\geq$ 10 MHz and SNDR $\geq$ 50 dB: (a) grouped by OSR (b) grouped by single-loop/MASH/SMASH (based on [4]).

order of either 3 or 4. Please notice that all of the 3 ΣΔ ADCs with NTF order of 6 are bandpass ΣΔ ADCs (or have a bandpass mode) [34, 47, 48]. The effective noise-shaping of these bandpass ΣΔ ADCs is actually 3rd order. So the majority of broadband medium-to-high resolution CT ΣΔ ADCs have 3rd or 4th order noise shaping, which is a trade-off between in-band quantization noise suppression and SDM stability and complexity.

Figure 3.8b presents the quantizer resolution. About 15% of these ADCs only use

1-bit quantization, since the 1-bit quantizer is not sensitive to its offset, and 1-bit DAC is inherently linear [9]. 55.6% of the ADCs in Figure 3.8b are using quantizers between 8-level and 17-level. The majority of these ΣΔ ADCs use flash sub-ADCs as the quantizers. Among all of the 12 ΣΔ ADCs with quantizer resolution $\geq$ 4.5 bit, only 2 ΣΔ ADCs use flash quantizers, and the other 10 ΣΔ ADCs use SAR, VCO-based, gated-ring-oscillator (GRO)-based, time-to-digital converter (TDC) or subranging quantizers [49, 27, 50, 51, 52].

Figure 3.9a shows the OSR. All of the 7 ΣΔ ADCs with signal BW $\geq$ 100 MHz have OSR between 8.6 and 16. For these 7 very-broad-band (BW $\geq$ 100 MHz) medium resolution (64 dB $\leq$ SNDR $\leq$ 74 dB) ΣΔ ADCs, reducing the OSR would increase the in-band quantization noise, while increasing the OSR would require an even higher sampling clock rate, which can reduce the power efficiency or it is even limited by the technology. Among all of the 8 ΣΔ ADCs with SNDR $\geq$ 77 dB, 7 of them have OSR $\geq$ 20. For them, high OSR ($\geq$ 20) facilitates the sufficient noise-shaping of the in-band quantization noise to achieve the targeted high SNDR.

In Figure 3.9b the ΣΔ ADCs are subdivided into single-loop, MASH and Sturdy MASH ΣΔ ADCs. Among the 53 ΣΔ ADCs, 45 ADCs are using single-loop SDM structures. 6 MASH ΣΔ ADCs and 2 Sturdy MASH ΣΔ ADCs are reported here. Among the 7 ΣΔ ADCs with signal BW $\geq$ 100 MHz, one of them uses the MASH structure and the other 6 ADCs are single-loop ΣΔ ADCs.

3.5 Design-space reduction

This section reviews the state-of-the-art broadband medium-to-high resolution CT ΣΔ ADCs in the context of the target specifications listed in Section 2.2. To achieve the target specifications (BW = 500 MHz, SNDR $\geq$ 60 dB), an NTF of either 3rd or 4th order is most promising. Since in our case the ADC non-linearity is tolerable as long as it is not limiting the SNDR target, multi-bit quantization is more beneficial because of its lower original unshaped quantization noise, better stability and enabling of more aggressive noise shaping. Flash quantizers between 8-level to 17-level are most promising from Figure 3.8b. Since this thesis targets at a very broad BW of 500 MHz, a relatively low OSR between 5 and 10 is a good choice. A higher OSR requires a sampling rate of more than 10 GHz which is not feasible to be implemented in the chosen 40nm CMOS technology considering multi-bit quantization. Both single-loop and MASH SDM structures are promising for our target specifications. This thesis decides not to choose the Sturdy MASH since the achievable SQNR of a Sturdy MASH is lower than the standard MASH for the same loop filter order and quantizer resolution, and the achievable sampling rate of a Sturdy MASH is lower than the standard MASH and single-loop SDMs. The exact system-level simulations regarding different NTF order, quantizer resolution, OSR for different single-loop and MASH structures are presented in Chapter 5.

3.6 Conclusions

Various design choices should be made for ΣΔ ADC architectures. The preliminary SDM design parameters are loop filter order, quantizer resolution and OSR. OBG and zero optimization should be decided according to the applications. Stability and STF should be considered as well. SDMs are further subdivided into single-loop and MASH SDMs. From the review of the state-of-the-art broadband medium-to-high resolution CT ΣΔ ADCs, the SDM design space is reduced for the target specifications. SDM architectures with 3rd or 4th order NTF, multi-bit quantization between 8-level and 17-level, OSR between 5 and 10, either with a single-loop or a MASH structure are promising. The exact SDM architecture design must consider the challenges, non-idealities and limitations from the circuit-level implementation, which is discussed in the next Chapter.

Chapter 4

Challenges of broadband CT ΣΔ ADCs

This chapter discusses the challenges, non-idealities and limitations of the circuit implementation of broadband CT ΣΔ ADCs. It is part of the bottom-up approach of the broadband CT ΣΔ ADC design. In this chapter, broadband ΣΔ ADCs refer to ADCs with signal BW of 100 MHz and higher. Firstly, the loop filter non-idealities are studied, including amplifier limited GBW, noise, non-linearity, and common-mode stability. This chapter further discusses the challenges in the quantizer implementation, including offset, quantization gain and metastability, and hysteresis. Afterwards, the DAC non-idealities are studied, including non-linearity and noise. Various clock non-idealities are discussed, like clock jitter, clock skew, and duty-cycle error. After describing the non-idealities in the building blocks, system-level non-idealities are discussed, including excess loop delay, coefficients variation, and digital and analog filter mismatch for MASH ΣΔ ADCs. Supply and reference non-idealities are discussed as well. This chapter presents the speed-resolution limitations from CMOS technologies. The non-idealities, challenges and limitations from circuit implementation justify limiting our design space for the SDM architecture design. In the end, conclusions are drawn.

4.1 Loop filter non-idealities

In low-pass CT ΣΔ ADCs, the loop filter is a low-pass filter, which is implemented from continuous-time integrators. Figure 4.1a shows the mathematical model of an ideal CT integrator. The integrator constant c is the UGBW of the integrator in [rad/s]. Generally a CT integrator can be implemented as an RC integrator or a Gm-C integrator.

Figure 4.1b presents an RC integrator. In the RC integrator, the amplifier is used in a

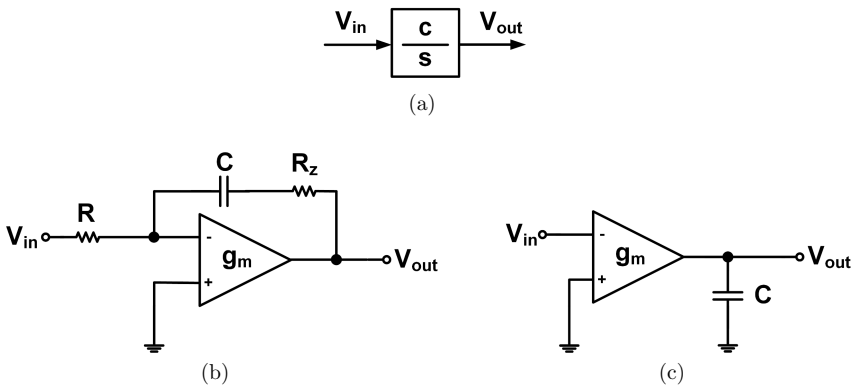


Figure 4.1: (a) Mathematical model of an integrator (b) an RC integrator (c) a Gm-C integrator.

feedback loop. g_m is the transconductance of the amplifier. A resistor R_z is added in series with the integration capacitor C to create a zero in the RC integrator transfer function, to compensate the phase shift due to the limited gain of the amplifier. The transfer function of the RC integrator is:

$$\frac{V_{out}}{V_{in}} = \frac{(g_m R_z - 1)sC + g_m}{sC(1 + g_m R)} \tag{4.1}$$

If $R_z = \frac{1}{g_m}$, the transfer function becomes:

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC(1 + g_m R)} \tag{4.2}$$

Commonly $g_m R \gg 1$, thus the UGBW of the RC integrator is:

$$UGBW \approx \frac{1}{2\pi RC} \quad \text{[Hz]} \tag{4.3}$$

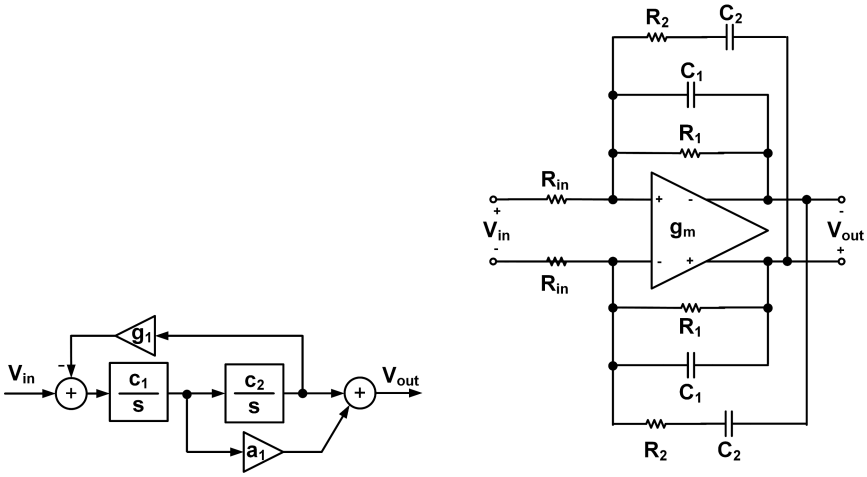
Figure 4.1c shows a Gm-C integrator. It uses the amplifier in an open loop. Its transfer function is:

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC} \tag{4.4}$$

The UGBW of the Gm-C integrator can be calculated as:

$$UGBW = \frac{g_m}{2\pi C} \quad \text{[Hz]} \tag{4.5}$$

When the order of the loop filter is larger than one, a set of two integrators can be combined into a resonator, as shown in Figure 4.2a (see Chapter 3.2.2). A resonator



(a) (b)

Figure 4.2: (a) Mathematical model of a resonator (b) a single-opamp resonator implementation.

can be implemented as two separate integrators, or a single-opamp resonator [53, 54]. Figure 4.2b shows one circuit implementation of a single-opamp resonator [54]. It uses the amplifier in a feedback loop. The resonance condition is [55, 9]:

$$\frac{C_1}{C_2} = \frac{R_1 - R_2}{R_1} \tag{4.6}$$

And the transfer function of the resonator is [55, 9]:

$$\frac{V_{out}}{V_{in}} = \frac{R_1}{R_{in}} \cdot \frac{1 + \frac{s}{R_2 C_2}}{1 + \frac{s^2}{R_1 R_2 C_1 C_2}} \tag{4.7}$$

Limited GBWs of the amplifiers have influence on the transfer function of the loop filter. It can introduce both an amplitude error and a phase error [56]. The parasitic capacitance at the output node of an RC integrator and a single-opamp resonator generates a parasitic pole. The phase shift of this output parasitic pole can be compensated by adding a resistor R_z in series with the integration capacitor (C in Figure 4.1b, or C_1 in Figure 4.2b). The parasitic capacitance on the output node of a Gm-C integrator can be considered as part of the total integration capacitance. Thus, the output parasitic capacitance does not add a parasitic pole to the transfer function of a Gm-C integrator. However, the parasitic capacitance is not well defined, and it can have voltage dependency. Thus, the accuracy and linearity of the UGBW of the Gm-C integrator can be affected if the parasitic capacitance is significant in the total integration capacitance. For all the above three implementations, the amplifiers' DC

gain and the gain in the signal BW are limited. The R and C coefficients need to be chosen considering the limited GBW of the amplifier and the parasitic poles [57]. Although the amplitude and phase errors caused by the limited GBW can be partially compensated, for the robustness of the SDMs, commonly a GBW of at least 1.5× of the ADC sampling frequency F_S is required for the amplifiers in the RC integrators, when this amplifier is not in a speed-critical loop (e.g. the ELD compensation loop) [58]. Notice that a much higher GBW of the amplifier can be requested by the other functionality of the amplifier and by the applications. For example, the amplifier in the RC integrator in [16] is used as the summation amplifier in the ELD compensation loop as well (see Section 4.5), and thus an effective GBW about 6.9× F_S is designed. In the bandpass ΣΔ ADC reported in [34], an effective GBW of 62.5× F_S is implemented for one amplifier used in RC integrator to meet the linearity target and to ensure the coefficient accuracy. For state-of-the-art broadband medium-to-high resolution CT ΣΔ ADCs, the sampling rate is up to 8 GHz [16]. Thus, the GBW requirement of the amplifiers is commonly much higher than the narrow-band CT ΣΔ ADCs. To achieve high GBW, amplifiers are generally more complex and power consuming. For example, a fifth-order multistage multipath feed-forward op-amp is reported to achieve 250 GHz effective GBW which consumes 100 mW power [34].

The noise from the loop filter contributes to the total input-referred noise of the ΣΔ ADC. Generally the input-referred loop filter noise is dominated by the input stage of the loop filter, since the noise from the following stages is suppressed by the gain of the front-end stages when referred to the SDM input. Loop filter noise contains mainly two parts – the noise from resistors and the noise from the amplifiers. The amplifier noise has two contributions – thermal noise and flicker noise. To reduce the thermal noise, the transconductance g_m of the input transistor should be increased. To reduce the flicker noise, the gate area needs to be increased [59]. Notice that PMOS transistors generally feature less flicker noise than NMOS transistors with the same gate area [60]. The noise requirement makes the loop filter design in broadband ΣΔ ADCs challenging for the following reasons. Firstly, the same SNDR target means lower in-band noise density for broadband ADCs than narrow-band ADCs. To achieve the overall noise density, the input resistance can be lower than 1 kΩ [9, 16]. The output current of the feedback DAC is inversely proportional to the input resistance, which is higher as well. The loop filter amplifier needs to provide the current to charge the integration capacitor. Secondly, to achieve the overall noise density, the thermal noise and flicker noise from the amplifier should be low enough. Thus, a high g_m is required, which means high current consumption. To reduce the flicker noise, large gate area is needed, which is contradictory to the high GBW requirement discussed in the last paragraph.

The non-linearity generated by the loop filter contributes to the overall non-linearity of the ΣΔ ADC. Similar to the noise, the input referred non-linearity of the loop filter is generally dominated by the input stage, when OSR is high (≥ 16). In an RC integrator or a single-opamp resonator, the amplifier is used in a feedback loop, and the input swing of the amplifier is equal to the integrator/resonator output swing divided by

the gain of the RC integrator or single-opamp resonator. On the contrary, in a Gm-C integrator, the amplifier input swing is equal to the input swing of the integrator. Generally the amplifier in a Gm-C integrator sees a much larger input swing than the amplifier in an RC integrator or a single-opamp resonator, and thus the achievable linearity of a Gm-C integrator is worse than that of an RC integrator or single-opamp resonator. Moreover, for all the above three implementations, the output swing of the amplifier is equal to the output swing of the integrator or resonator. In the ΣΔ ADC architecture design, the UGBW of the integrators need to be carefully scaled, such that the output swing of the integrators and/or resonators is optimal. If the output swing of the integrator and/or resonator is too high, the non-linearity of the amplifier can limit the SNDR and/or spurious free dynamic range (SFDR) specification of the ADC. If the output swing of the integrator and/or resonator is too low, the noise and distortion from the following stages might not be sufficiently suppressed by this integrator/resonator. The non-linearity is a challenge for broadband ΣΔ ADCs. Firstly, to suppress the input swing of the amplifier used in an RC integrator or a single-opamp resonator, high DC gain is required for the amplifier. It is challenging to achieve high DC gain and high GBW at the same time, and commonly multi-stage and/or multi-path amplifiers are needed [30, 9, 34]. Secondly, broadband ΣΔ ADCs commonly have a lower OSR than narrow-band ADCs. In some cases, the UGBW of the 1st integrator is comparable or lower than the signal BW, and thus the noise and non-linearity of the 2nd integrator are significant when referred to the SDM input. In this case, the decision on the 1st integrator output swing has direct impact on the overall noise, linearity and power consumption of the ΣΔ ADC.

Although Figure 4.1b and 4.1c are drawn single-ended, generally loop filters are implemented differentially. Therefore, the common-mode stability is another important aspect when designing the loop filter. Generally common-mode feedback (CMFB) circuitry is designed in the amplifier to keep its input and output common-mode voltages stable. The CMFB circuitry should be robust to have enough phase margin, gain margin and UGBW to handle the possible common-mode disturbance. In broadband ΣΔ ADCs, the requirement on the UGBW of the CMFB circuit is generally wider than that in narrow-band ΣΔ ADCs.

4.2 Quantizer non-idealities

Figure 4.3a shows the output characteristic of an ideal 1-bit comparator. Its output characteristic is:

$$V_{out} = \begin{cases} 1 & V_{in} \geq 0 \\ -1 & V_{in} < 0 \end{cases} \tag{4.8}$$

Figure 4.3b presents the output characteristic of a 1-bit comparator with an offset

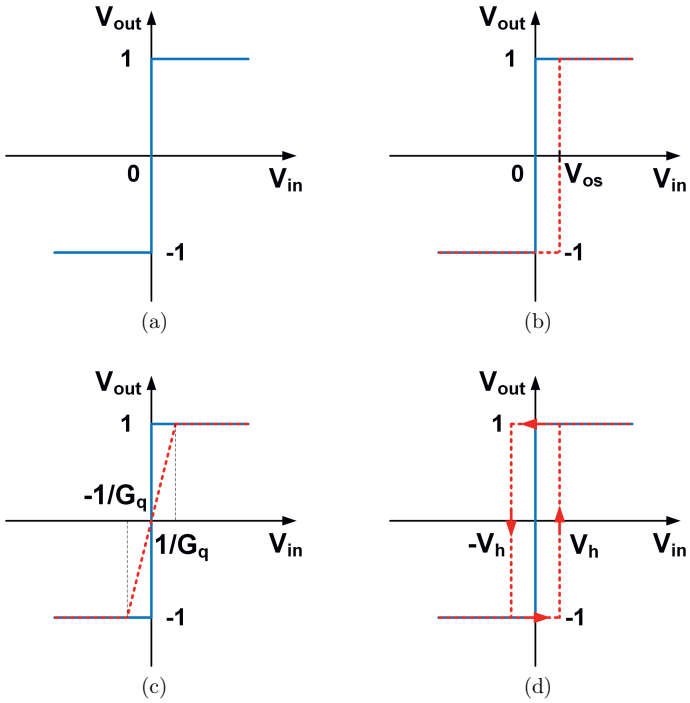


Figure 4.3: Output characteristic of (a) an ideal comparator (b) a comparator with offset V_{os} (c) a comparator with limited quantization gain G_q and (d) a comparator with hysteresis V_h.

V_{os}. Its output characteristic can be written as:

$$V_{out} = \begin{cases} 1 & V_{in} \geq V_{os} \\ -1 & V_{in} < V_{os} \end{cases} \tag{4.9}$$

Generally a ΣΔ ADC with 1-bit quantization is insensitive to comparator offset, which only slightly increases the power of the unshaped quantization noise. The requirement for the mismatch in offsets of the various comparators in a multibit quantizer is generally more stringent than a 1-bit quantizer because the LSB size is smaller. Offset in multibit quantizers leads to extra non-linearity. Since the quantization noise power is the integral of the square of the quantization error by its probability, the comparator offset in a multi-bit ΣΔ ADC increases the original quantization noise power (see Chapter 10.4). Thus, it can make the SDM overloaded. The offset requirement is determined by the noise and linearity specifications of the ΣΔ ADC. The comparator offset can be caused by the mismatch in the comparator circuit. Moreover, for a multi-bit quantizer, the mismatch of the references contributes to the total quantizer offset.

The design requirements of the comparator offset can be achieved by either intrinsic matching or comparator offset calibration [16]. Intrinsic matching requires large gate area for the matched transistors, which reduces the speed. In the design of a 3-bit quantizer in this thesis (shown in Chapter 11), the simulated standard deviation of a comparator in the 3-bit quantizer is about $\sigma = 2.6$ LSB, while the offset requirement is $\sigma \leq \frac{1}{6}$ LSB. A proposed comparator offset calibration technique for a multi-bit quantizer with current-mode multi-path excess loop delay compensation and local time-interleaved comparators is presented in Chapter 8.2.

Quantizer metastability is another limitation for broadband CT ΣΔ ADCs [61]. It is caused by the limited quantization gain G_q of the comparator, see Figure 4.3c. Assuming a comparator built from cross-coupled inverters with positive feedback, the quantization gain can be calculated as [62]:

$$G_q = e^{\frac{T_{reg}}{\tau}} \tag{4.10}$$

In this equation, T_{reg} is the regeneration time of the comparator, and τ is the regeneration time constant of the comparator. For the current state-of-the-art very-broadband (BW $\geq$ 100 MHz) CT ΣΔ ADCs, the sampling frequency can be as high as 8 GHz [16]. In this case, one sampling clock period (T_S) is only 125 ps. An SDM is a feedback system, and typically the total delay in the feedback loop is kept below 1 T_S using excess loop delay compensation. This is the upper limitation of the total delay in the feedback loop, including quantizer regeneration time, propagation delay from quantizer to DACs and the DACs' delay. Thus, the quantizer regeneration time is typically much lower than T_S. However, the minimal regeneration time constant τ of the comparator is limited by the technology and by the power budget. Thus, the total quantization gain G_q generated by the comparator within the available regeneration time is limited. As a consequence, the comparator might not be able to make a good decision within the time available. This is especially a problem for GHz-rate sampling CT ΣΔ ADCs. Figure 4.3c shows a simplified output characteristic for a comparator with limited quantization gain G_q. For simplicity, this thesis assumes a straight line between ($-\frac{1}{G_q}$,-1) and ($\frac{1}{G_q}$,1). In reality, exponentially asymptotically approaching to $V_{out} = 1$ and $V_{out} = -1$ is usually observed. The simplified output characteristic in Figure 4.3c can be written as:

$$V_{out} = \begin{cases} 1 & V_{in} \geq \frac{1}{G_q} \\ G_q \cdot V_{in} & -\frac{1}{G_q} \leq V_{in} < \frac{1}{G_q} \\ -1 & V_{in} < -\frac{1}{G_q} \end{cases} \tag{4.11}$$

The metastability error in CT ΣΔ ADCs is further elaborated in detail in Chapter 10. Two solutions are proposed to overcome the metastability error limitation in this thesis – (1) metastability error compensation (Chapter 10.4) and (2) metastability shaping technique (Chapter 10.5).

Hysteresis is another non-ideality of the quantizer. It describes the memory effect of the comparator – the comparator output does not only depend on the input, but

also on its previous output, e.g. by a non-ideal reset of the quantizer. Figure 4.3d presents the output characteristic of a 1-bit comparator with hysteresis V_h. Its output characteristic can be written as:

$$V_{out}(n) = \begin{cases} 1 & V_{in}(n) \geq V_h \text{ or } \Big(V_{in}(n) \geq -V_h \text{ and } V_{out}(n-1) = 1\Big) \\ -1 & V_{in}(n) < -V_h \text{ or } \Big(V_{in}(n) < V_h \text{ and } V_{out}(n-1) = -1\Big) \end{cases} \tag{4.12}$$

The quantizer hysteresis can make the SDM unstable. In case the quantizer hysteresis is due to a non-ideal reset, it can be reduced by improving the reset, such that a lower residue is left at the input. The hysteresis problem is especially a challenge for high sampling rate quantizers, so for broadband ΣΔ ADCs.

Quantizers have thermal noise and flicker noise. Generally the SDMs are not sensitive to the thermal noise and flicker noise from the quantizers because their power is much less than the quantization noise and they are shaped by the NTF.

This section has studied some quantizer non-idealities. Some other non-idealities, such as the sampling aperture of the quantizer, are out of the scope of this thesis. This section shows quantizer offset, limited quantization gain, hysteresis and noise separately with figures and equations. In real circuit, these non-idealities are combined.

4.3 DAC non-idealities

This section discusses the non-idealities of the feedback DACs. Some CT SDM architectures have more than one feedback DAC, such as the exemplary 2nd order CT SDM in feedback form shown in Figure 4.4. Here the feedback DACs have their output connected to the input of an integrator or a resonator of the loop filter. In this thesis, the feedback DAC whose output is connected to the input of the CT SDM is called the 1st DAC, such as DAC_1 in Figure 4.4. The noise and distortion originating from the 1st DAC is directly added to the SDM input without noise shaping. The noise and distortion originating from DAC_2 is 1st order high-pass filtered in the signal band when referred to SDM input.

In CT ΣΔ ADCs, the main FB DACs are mainly implemented as current-steering DACs or resistive DACs. Figure 4.5 shows some common circuit implementations of a 1-bit DAC, or a unit cell of a multibit DAC. Figure 4.5a shows the simplified schematic of a current-steering DAC with one-side switching [30]. Here the upper side current source I_{DAC} is switched according to the DAC input $D^{+/-}$. The bottom side current sources $0.5I_{DAC}$ are static and always connected to $\text{Out}^{+/-}$. It can be implemented as bottom side switching and upper side static as well.

Figure 4.5b presents the simplified schematic of a current-steering DAC with two-side switching [16, 63]. Here both the upper current source and the bottom current source

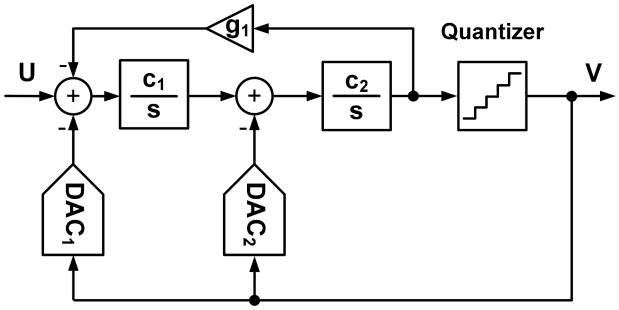


Figure 4.4: An exemplary 2nd order CT SDM in feedback form.

are switched. Sometimes this implementation requires a negative supply voltage $V_{supply,n}$ [16].

Figure 4.5c shows the simplified schematic of a resistive DAC [9]. It requires the common-mode output voltage of the DAC to be in the middle of the DAC supplies:

$$V_{cm,out} = \frac{V_{dd} + V_{ss}}{2} \quad [\mathrm{V}] \tag{4.13}$$

Based on the noise mechanism, DAC noise contains two contributions – thermal noise and flicker noise. The thermal noise is contributed by both resistors and transistors, while the flicker noise is contributed mainly by the transistors. For current-steering DACs in Figure 4.5a and Figure 4.5b, DAC noise is contributed mainly by the DAC current sources (I_{DAC} and $0.5I_{DAC}$) and the biasing circuit which generates the biasing voltages/currents for the DAC current sources. Notice that in the current-steering DAC with one-side switching (Figure 4.5a), the non-switching current sources $0.5I_{DAC}$ contribute SDM input-referred noise, too. In that perspective, the current-steering DAC with two-side switching has a noise benefit compared to the current-steering DAC with one-side switching. For the resistive DAC in Figure 4.5c, DAC noise is contributed mainly by the DAC resistor R_{DAC} and the noise from the DAC supply V_{dd}. A low-noise LDO regulator is generally required to regulate the supply for the resistive DAC. Since the same SNDR target means lower in-band noise density for broadband ADCs than narrow-band ADCs, it is more challenging to achieve the noise specification of the DACs for broadband ADCs.

Several mechanisms can generate non-linearity in the DAC. For multi-bit DACs, mismatch between the unit DAC cells generates non-linearity [64]. The mismatch introduces both amplitude error and timing error. For current-steering DACs shown in Figure 4.5a and Figure 4.5b, the mismatch on the switching current sources contributes to the DAC non-linearity directly. The mismatch on the non-switching current sources leads in first instance to a common-mode output current but not to a non-linearity. Considering some 2nd order effect, it might introduce some non-linearity as well. Typically its non-linear effect is not dominant in the CT SDM. When DAC

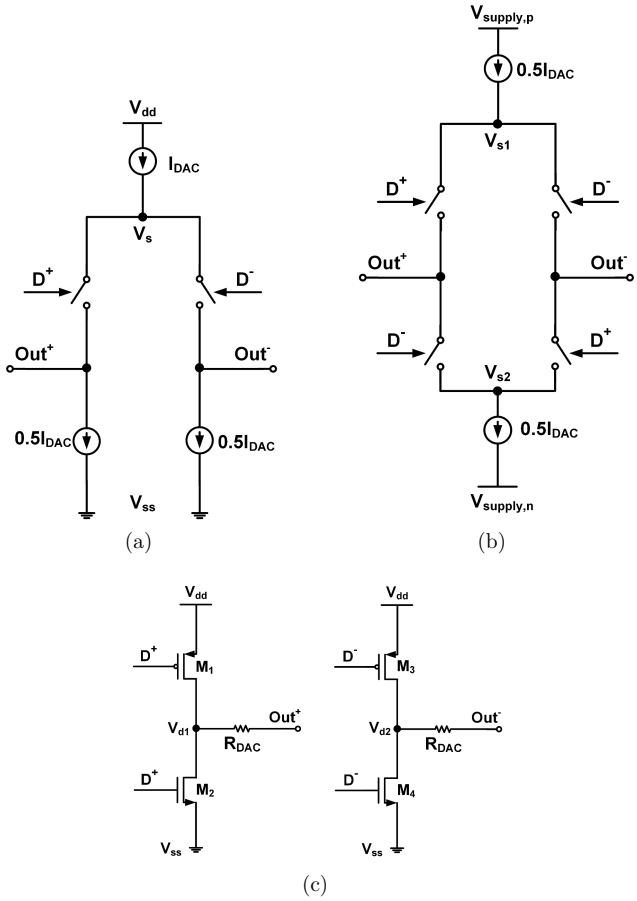


Figure 4.5: Simplified schematic of (a) a current-steering DAC with one-side switching (b) a current-steering DAC with two-side switching (c) a resistive DAC.

unit cells are mismatched, the DAC transfer function is not linear anymore. It has two types of impact in the content of ΣΔ ADCs – (1) the DAC non-linear transfer function mixes with the signal and interference, and generates harmonics and intermodulation distortion; (2) the DAC non-linear transfer function mixes with the out-of-band quantization noise which increases the in-band noise floor. The matching requirement should be considered in the sizing of the devices and in the layout. If intrinsic matching does not meet the requirements, DAC calibration techniques can be applied to improve the DAC linearity or to reduce the area [16, 65, 66, 67].

DAC non-linearity can be generated from the limited signal-dependent output impedance of the DAC together with the signal components at the DAC output node [63]. Adding a cascode transistor can increase the DAC output impedance, and thus decrease its

relative influence with respect to the load impedance [30]. The error charge caused by the limited DAC output impedance can be compensated [63]. For a resistive DAC shown in Figure 4.5c, the output impedance of the DAC is almost equal to R_{DAC}. To achieve high linearity with a resistive DAC, the DAC supply V_{dd} should be regulated by a low impedance LDO regulator, and the swing on the DAC output node $Out^{+/-}$ should be minimized [9].

Signal dependent switching timing errors can degrade the DAC linearity as well. In the current steering DACs shown in Figure 4.5a and 4.5b, DAC switching can generate a glitch on the nodes V_s, V_{s1} and V_{s2}. If this glitch is not settled before the next switching moment, it will introduce a signal dependent timing error. To limit this error, the crossing point of D^+ and D^- can be designed such that the glitch on these nodes are minimized. Moreover, the parasitic capacitance on the nodes V_s, V_{s1} and V_{s2} should be minimized to speed up the settling.

It is more challenging to achieve the same target linearity in dB for DACs in broadband ΣΔ ADCs than those in narrow-band ΣΔ ADCs for the following reasons. Broadband ΣΔ ADCs have a wider signal bandwidth and commonly a higher sampling rate. The DACs needs to deliver the required linearity for a bandwidth from DC to $\frac{F_S}{2}$, which is larger in broadband ΣΔ ADCs. At low frequency, the DAC linearity is commonly limited by the amplitude error. While at higher frequency, the timing error and the impact of the limited output impedance is more significant for the overall linearity performance [64]. Moreover, in broadband ΣΔ ADCs the available timing budget for the DAC delay is very limited. The matching requirement and the speed requirement are commonly contradictory. In many broadband ΣΔ ADC designs, the intrinsic matching is not enough, and thus DAC calibration is necessary [16, 65, 66, 67].

4.4 Clock non-idealities

The clock has various non-idealities, including clock jitter, clock skew, and duty cycle error. Here, clock jitter refers to the random noise on the timing of the rising and falling edges of the clock. It is generated from the thermal and flicker noise of the switching transistors in the clock generation and distribution circuit. Generally, CT ΣΔ ADCs are sensitive to the clock jitter on the DAC clock, while the clock jitter introduced error from the quantizer clock is shaped by the NTF [61]. The clock jitter introduced error generated at the 1st DAC whose output is connected to the SDM input is directly added to the SDM input without any noise shaping. The clock jitter introduced error generated at the DACs is influenced by the DAC pulse and number of bits. Generally, a return-to-zero (RZ) DAC with a rectangular DAC pulse is more sensitive to clock jitter than a non-return-to-zero (NRZ) DAC with a rectangular DAC pulse. Figure 4.6 shows the clock jitter introduced error in the feedback DAC output current for a 1-bit and a 2-bit NRZ DACs. A multi-bit NRZ DAC with a rectangular DAC pulse is less sensitive to clock jitter than a 1-bit NRZ DAC with a

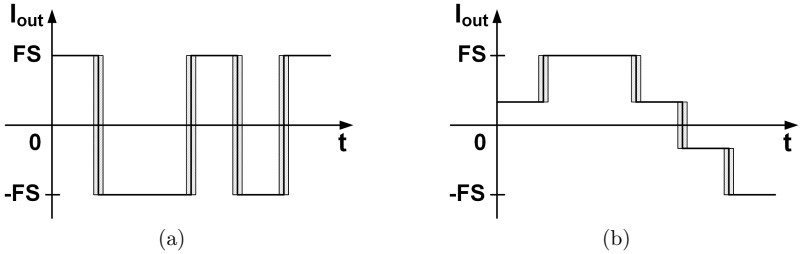


Figure 4.6: Clock jitter introduced error in the feedback DAC output current (a) for a 1-bit NRZ DAC (b) for a 2-bit NRZ DAC. Exemplary bit sequence for illustrative purpose.

rectangular DAC pulse, without specific jitter mitigation techniques. Applying finite impulse response (FIR) DACs can make the 1-bit CT ΣΔ ADCs less sensitive to the clock jitter [68].

Clock skew refers to the deterministic timing error on the rising and falling clock edges compared to the ideal clock. In Section 4.3, the timing error caused by the mismatch among DAC unit cells introduces clock skew, causing DAC non-linearity. Here the timing difference due to the mismatch on the sampling and buffering of the DAC input, the switching time difference caused by the mismatch of the DAC switches, and the different RC delay of local clock routing all contribute to the effective clock skew between the unit DAC cells.

The clock can have a duty-cycle error, which refers to the effect that the real clock has a different duty-cycle than the ideal clock. Some system and circuit choices make the SDMs more sensitive to the duty-cycle error. If all the circuitry of the SDM is triggered by only one clock edge (either a rising edge or a falling edge) of the SDM fundamental input clock, the SDM in principle is not sensitive to the duty-cycle error of the SDM fundamental input clock. Some circuits use both clock edges, or are clock level sensitive. For example, for a RZ DAC which gives non-zero output when its clock is high and zero output when its clock is low, the clock duty-cycle error is transformed into a gain error in the total charge of the DAC feedback.

Broadband CT ΣΔ ADCs need sharp clock edges in term of absolute value as the clock period is short. For example, in the 7 GHz sampling ΣΔ ADC test chip shown in Chapter 11, one clock period is only 143 ps. The 10% to 90% rising edge and 90% to 10% falling edge are designed to be less than 20 ps for the 7 GHz clock. Clock edges have mainly two impacts. First, an amplitude error on the clock is converted to a time error through the slope of the clock edges. Second, slow clock edges introduce more delay in the ΣΔ loop.

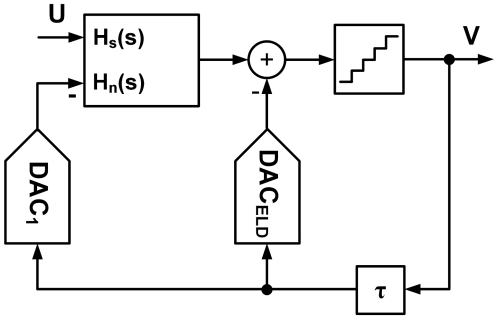


Figure 4.7: An CT SDM with ELD compensation.

4.5 System-level non-idealities

Excess loop delay refers to the total delay of the SDM feedback loop, including the quantizer delay (mainly quantizer regeneration time), DAC delay and the propagation delay from the quantizer to the DAC [69]. As shown in Figure 4.7, ELD can be compensated typically by adding a direct feedback path from the output to the input of the quantizer through DAC_{ELD} [69, 70]. For broadband (BW $\geq$ 10 MHz) medium-to-high resolution (SNDR $\geq$ 50 dB) CT $\Sigma\Delta$ ADCs, typically ELD up to one sampling clock period is compensated, to restore the stability and SQNR to that of the non-delayed SDM.

ELD compensation is susceptible to implementation non-idealities. For example, the ELD summation commonly has a limited bandwidth, which means an effective parasitic pole is at the summation node output. Figure 4.8 shows an exemplary 1-bit single-loop SDM with ELD compensation and a parasitic pole at the ELD summation output. In the ideal model, the ELD compensation loop has a delay of 0.5 T_S, while the main feedback loop through DAC_1 has a delay of 1 T_S. The parasitic pole adds extra delay (or phase shift) in the loop. For an exemplary 4th order 1-bit SDM, simulation results show that the parasitic pole frequency at the ELD summation node should be higher than 2 F_S, to maintain the performance and the robustness of the SDM. In this thesis, an overview for the state-of-the-art high-speed ELD compensation techniques is given in Chapter 7.1. A proposed current mode multi-path ELD compensation technique is presented in Chapter 7.2. And a proposed technique to overcome the parasitic capacitance on the ELD summation node is addressed in Chapter 7.3.

An SDM architecture is defined by many coefficients, including the UGBW of the integrators, the gain and resonance frequency of the resonator, the linear gain of the quantizer, and the output swing of the DACs. The loop delay through every feedback DAC is another coefficient in time. These coefficients can have variations caused by two reasons – (1) process, voltage and temperature (PVT) variation and (2) mismatch.

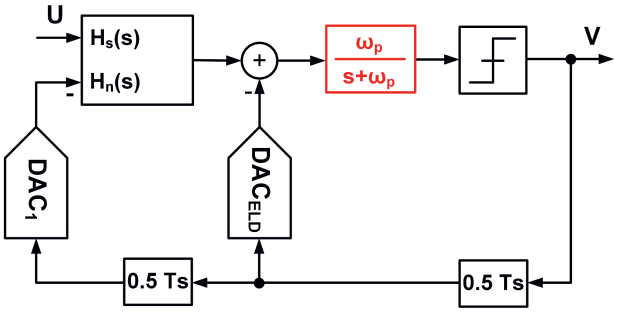


Figure 4.8: An exemplary CT SDM with ELD compensation and a parasitic pole at the ELD summation output.

PVT variation has a common impact on the same type of devices on the chip. For example, due to PVT variation, the UGBW of an RC integrator can vary typically up to about ± 30%. Usually a tunable capacitor bank is implemented for every RC integrator to calibrate the integrators' UGBW. On the other hand, mismatch causes different relative errors for similar devices on the chip [71]. Applying common-centroid layout and adding dummies are common ways to improve the matching. For more advanced CMOS technology, the layout dependent effect on the matching becomes more important. Since the coefficient variation is unavoidable, the SDM architecture should be designed robust enough to be able to tolerate a few percent of coefficient variation.

For CT MASH ΣΔ ADCs, digital noise cancellation filters are required to remove the quantization noise of all the stages except for the last stage (see Section 3.3.2). Perfect noise cancellation requires the digital noise cancellation filters and the corresponding analog filters to be matched, otherwise the quantization noise from the front-end stages is not perfectly canceled which can degrade the SNR of the MASH ΣΔ ADCs [42, 72, 73]. To reduce the quantization noise leakage, calibration of the digital NCF is typically required [42, 72, 73]. A proposed digital calibration technique for broadband CT MASH ΣΔ ADCs with relaxed filter requirements is presented in Chapter 6.

4.6 Supply and reference non-idealities

A stable supply and ground are essential for the resolution of broadband CT ΣΔ ADCs. Typically broadband ΣΔ ADCs require a low-impedance supply and ground over a wide bandwidth. A series resistance on the supply causes an IR drop, which reduces the speed, gain and bandwidth of some sensitive circuits. For example, a large IR drop can reduce the quantization gain of the comparator core, the GBW of the loop filter amplifier, and can increase the propagation delay of the buffers between the quantizer and the DAC. Moreover, noise and distortion can couple through the

supply or ground into the signal bandwidth, which can reduce the SNDR, DR or SFDR performance of the ADC. Broadband ΣΔ ADCs are more sensitive to the non-idealities of the supply and ground since their current consumption is typically higher than the narrow-band ADCs, and their in-band noise density is also lower than the narrow-band ADCs with the same DR. On-chip LDO regulators are required for sensitive supplies in some high-linearity broadband ΣΔ ADCs [9]. Sufficient on-chip decoupling capacitance should be designed with low routing resistance to the sensitive blocks which consumes dynamic current. Separating supplies between the sensitive blocks (e.g. input stage of the loop filter, 1st DAC, etc.) and the aggressors (e.g. quantizer) can be considered for improved isolation. Separation of ground can also be considered for improved isolation which makes the using of deep N-well necessary, and increases the layout area and complexity. Bonding wire inductance and resistance, and the supply and ground circuitry on the validation board should also be considered in the design and simulations.

CT ΣΔ ADCs commonly need some reference current and/or voltage. Non-idealities of the reference can degrade the ADC performance. For example, the ADC test chip in this thesis requires a reference current for the biasing block of its DAC (see Chapter 11). The noise of this reference current is copied to the DAC output current, and directly adds to the ADC input and it can degrade the DR of the ADC. Thus, a low noise reference current is needed. A bandgap circuit is typically needed to generate the reference voltage and/or current on chip in a commercial semiconductor product [74].

4.7 Limitations from CMOS technologies

To understand the speed-resolution limitations from CMOS technologies, this section further analyzes the state-of-the-art CT ΣΔ ADCs with Fs $\geq$ 1 GHz on their sampling rates, quantizer resolutions and technology nodes. Figure 4.9 shows the benchmark plot for those ADCs fabricated in 16 – 45 nm CMOS. The x-axis shows the sampling rate of the CT ΣΔ ADCs, and the y-axis shows their quantizer resolution. The ADCs are divided into 3 groups according to their fabrication technology: (1) 16 - 20 nm CMOS (2) 28 nm CMOS (3) 40 - 45 nm CMOS. From the benchmark it can be observed that at higher sampling rates, lesser bits are implemented in an ADC. The blue dotted line shows the state-of-the-art envelope for published 28 nm ADCs and the green dotted line shows the state-of-the-art line for 40 - 45 nm designs. From these lines it can be extracted that for the same number of bits, 28 nm CMOS technology achieves about 1.6 – 2× higher sampling rate compared to 40 nm CMOS thanks to the technology advantage. The transit frequencies (f_T) of MOS transistors of both 40 nm and 28 nm CMOS technologies are simulated. With the same current density, the NMOS transistor in the type with the lowest threshold voltage in 28 nm CMOS shows 1.6× higher f_T than that in 40 nm CMOS. In 28 nm CMOS technology smaller transistor structure can be used to achieve the same W/L

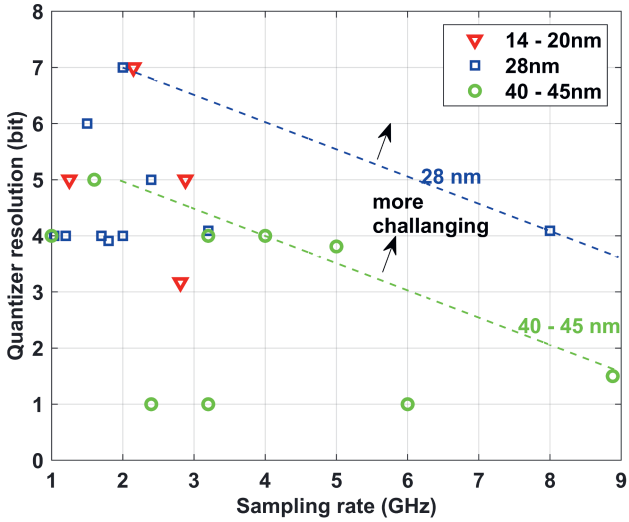


Figure 4.9: Quantizer resolution vs. sampling rate for state-of-the-art CT ΣΔ ADCs with Fs $\geq$ 1 GHz, fabricated in 16 – 45 nm CMOS (based on [4]).

as the 40 nm CMOS technology, which makes the layout more compact and reduces the routing parasitic resistance and capacitance. It is acknowledged here that the 28 nm state-of-the-art envelope only contains 2 data points. However, considering the better matching, higher speed and the miniaturization benefit of 28 nm CMOS, the 1.6 – 2× speed advantage compared to 40 nm CMOS is a realistic expectation. From this plot, it can be estimated that in the chosen 40 nm CMOS technology, the highest practically achievable sampling rate for 4-bit quantization is about 4 – 5 GHz, for 3-bit quantization is about 6 – 7 GHz, and for 2-bit quantization is about 8 GHz.

4.8 Design-space reduction

The non-idealities, challenges and limitations from circuit implementation justify limiting our design space for the SDM architecture design, with respect to choice of sampling rate F_S, NTF order, and quantizer resolution.

The maximal achievable ADC sampling rate F_S is limited by multiple factors. Firstly, commonly an RC integrator or a single-opamp resonator is used as the 1st stage of the loop filter to achieve high linearity. For the robustness of the ΣΔ ADC, the GBW of the amplifier used in this RC integrator or single-opamp resonator is typically at least $1.5\times F_S$. Actually, all of the circuits must have a wider bandwidth when a higher F_S is used, otherwise the parasitic poles can degrade the performance or even make

the SDM instable. If the F_S is very high, the GBW requirement of the amplifier is very high, thus the power consumption of the amplifier is very high which reduces the overall power efficiency of the ADC. Secondly, commonly ELD compensation techniques can compensate no more than 1 T_S delay in the SDM loop. When F_S is very high, e.g. 10 GHz, 1 T_S is only 100 ps. This is the total time budget for the quantizer regeneration time, the quantizer sampling delay, the propagation delay from the quantizer to DACs, and the DACs' delay. In this case, the quantizer hardly has enough regeneration time to generate the required quantization gain to combat the metastability error. Last but not least, the clock jitter introduced error is proportional to the relative clock jitter referred to the sampling clock period T_S. The higher F_S, the more stringent the absolute clock jitter requirement is. In 40 nm CMOS technology, considering multi-bit quantization, the estimated maximal achievable ADC sampling rate F_S is less than 10 GHz, which is mainly limited by the second point. On the other hand, the F_S should be at least 5 GHz such that the OSR is at least 5 to have sufficient in-band quantization noise suppression.

The maximal NTF order is limited by the circuit implementation non-idealities. To guarantee the stability for high-order low-pass SDMs with order larger or equal to 6, commonly the SQNR performance is sacrificed, which makes it less attractive. Moreover, for very low OSR between 5 and 10, the SQNR improvement is almost negligible for single-loop SDM when the NTF order is further increased above 5. Figure 3.8a shows that the state-of-the-art broadband CT $\Sigma\Delta$ ADCs mostly have noise shaping order less or equal to 5. Considering that the robustness of the $\Sigma\Delta$ ADC with coefficients variation and parasitic poles must be guaranteed, the maximal NTF order (N_O) is chosen to be less or equal to 5.

The choice on the quantizer resolution is limited by the circuit implementation challenges. Firstly, SDMs with multi-bit quantization are less sensitive to clock jitter compared to SDMs with 1-bit quantization. The higher limit on the quantizer resolution is bounded by two reasons. (1) It is bounded by the offset of a single comparator in a 1-bit quantizer, and especially the mismatch in offset between the various comparators in a multibit quantizer. For a quantizer with more bits, the offset requirement is more stringent, which requires larger area for matched devices and/or more sophisticated comparator offset calibration techniques. Notice that the larger device area and the additional circuit for offset calibration typically reduce the speed of the quantizer. (2) This thesis considers implementing the multi-bit quantizer as a flash sub-ADC, since the SDM sampling rate is about 5 GHz - 10 GHz to achieve the target signal BW and SNDR specification. The capacitive load caused by the flash quantizer increases exponentially with the number of bits. Figure 3.8 shows that the state-of-the-art broadband CT $\Sigma\Delta$ ADCs with flash quantizers mostly have no more than 17 quantization levels. Considering these limitations, the quantizer number of bits (N_Q) is limited to maximally about 4.09-bit (17-level).

At this step, the boundaries on the choice of the main design parameters are summarized in Table 4.1.

Table 4.1: Boundaries on the main SDM architecture design parameters

Sampling rate F_S	5 GHz $\leq F_S \leq$ 10 GHz
NTF order N_O	$N_O \leq 5$
Quantizer resolution N_Q	2-bit $\leq N_Q \leq$ 4.09-bit

4.9 Conclusions

Various challenges, non-idealities and limitations exist in the circuit implementation of broadband CT ΣΔ ADCs. The loop filter is affected by limited GBW of the amplifiers, noise, and non-linearity. Moreover, the common-mode stability should be guaranteed by circuit design. The quantizer is affected by offset, limited quantization gain and hysteresis. The DACs contribute noise and non-linearity to the SDM as well. The clock has clock jitter, clock skew and duty-cycle error. Coefficients variation should be accommodated by the SDM architecture design, and the excess loop delay should be compensated properly in the SDM. For CT MASH ΣΔ ADCs, the mismatch between the digital NCF and the analog filter should be calibrated. Considering the limitations from circuit implementation, SDM sampling frequency between 5 GHz and 10 GHz, NTF order less or equal to 5 and multi-bit quantizer with number of bits no more than 4.09 seems to be feasible to be implemented in the chosen 40 nm CMOS technology.

Chapter 5

Synthesis procedure for broadband CT ΣΔ ADC architectures

This chapter presents a synthesis flow for broadband CT MASH ΣΔ modulators, on the basis of an exemplary ADC architecture for the target application defined earlier. The information from the top-down design approach shown in Chapter 3 and the bottom-up design approach shown in Chapter 4 is considered in this synthesis flow. Firstly, the choice of the main design parameters is made, including the SDM topology, NTF order, quantizer resolution and OSR, based on simulation results of ideal SDM architectures and the speed-resolution limitation of the chosen 40 nm CMOS technology. Afterwards, this chapter presents a generic synthesis flow for broadband CT MASH ΣΔ modulators. This chapter further shows the additional system-level optimization of an exemplary CT MASH ΣΔ modulator for the target application. Various system-level verification results are presented to set specifications for the building blocks and to show the feasibility and robustness of the ADC architecture. In the end, conclusions are drawn.

5.1 Choice of main design parameters

The fundamental limitations for the bandwidth and resolution of CT ΣΔ ADCs are the resolution (or amplitude) limitation and the speed (or bandwidth) limitation, which are given by the technology. Although the device mismatch of the technology can be overcome with calibration, the resolution is still limited by the calibration accuracy, and the calibration circuitry adds to the load which reduces the speed and increases power consumption. The SQNR and BW of a single-loop SDM is limited mainly by three parameters: (1) the gain of the loop filter, (2) the quantizer resolution, and (3) the sampling rate. The gain of the loop filter in the signal bandwidth is determined by the loop filter order, OSR, OBG and zero optimization. Its accuracy is limited by the GBW of the amplifier and the accuracy of the coefficients in the

implementation. The quantizer resolution is limited by both the amplitude accuracy and the speed limitation. The mismatch of the comparator offset is limited by the amplitude accuracy, and the quantization gain is limited by the speed limitation of the technology. The sampling rate of the CT SDM is limited mainly by the speed limitation of the technology. Because all the three parameters (the loop filter gain, the quantizer resolution and the sampling rate) are limited by the resolution and speed limitation of the technology, the signal BW is limited for a certain SQNR target for single-loop SDMs. MASH SDMs benefit from the cancellation of the quantization noise of all front-end stages, which can alleviate the signal BW limitation of the single-loop SDMs. However, the cancellation of the quantization noise relies on the matching between the transfer functions, which is limited by both the amplitude accuracy and speed/bandwidth limitation of the technology.

The analysis in Chapter 3 and 4 concludes that for the target specification, the design space is reduced to OSR between 5 and 10, NTF order less or equal to 5, quantizer number of bits between 2 and 4.09 (17-level), and either a single-loop or MASH structure. This thesis chooses several representative single-loop and MASH SDM architectures with different order and quantizer resolution. Here single-loop SDMs up to 4th order are simulated. For very low OSR between 5 and 10, 5th order single-loop SDMs do not improve much the peak SQNR compared to 4th order single-loop SDMs, while increase the design complexity [19]. Several MASH structures up to 3 stages are considered here, since in practice an additional 4th stage can hardly increase the resolution of the MASH ADC due to implementation non-idealities. For example, due to the limited GBW of the loop filter amplifier, variation of MASH SDM parameters caused by device mismatch, and parasitic poles in the loop, the actual transfer functions in a MASH architecture deviate from the ideal transfer functions. This error commonly overloads the 4th stage, which does not improve the resolution of the MASH anymore. The ideal DT SDM models are optimized for different OSR between 5 and 10 and simulated in Matlab. The peak SQNR vs. OSR is plotted in Figure 5.1. Here, zero optimization is used to further improve the peak SQNR. In MASH SDMs, higher resolution quantizers in the front-end stages allow to use higher inter-stage gains. And higher resolution quantizer in the last stage can reduce the original quantization noise power which is suppressed by the overall noise shaping of the MASH. In practice, the quantizer in the 1st stage has more stringent quantization gain requirement. It implies that if the quantizer in the 1st stage is feasible to be implemented, then quantizers with the same resolution can be implemented in the back-end stages as well. Considering that the quantizer in the 1st stage can be reused or scaled in the back-end stages to save design effort, all the quantizers of the MASH have the same resolution in this simulation.

Figure 5.1 shows that for the same SDM architecture, the peak SQNR increases when the OSR increases. Some SDM architectures show similar SQNR versus OSR, for example 17-level 3rd order single-loop SDM and 9-level 4th order single-loop SDM. However, the peak SQNR of 9-level 4th order single-loop SDM increases faster when the OSR increases, compared to the 17-level 3rd order single-loop SDM, because higher

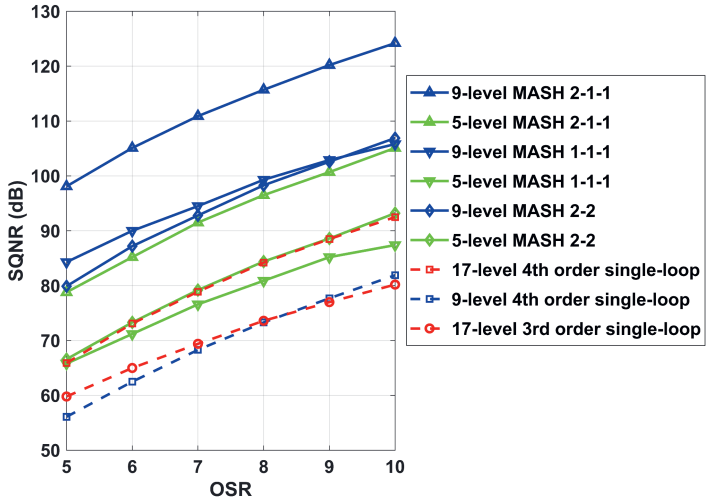


Figure 5.1: Simulated peak SQNR vs. OSR for different SDM architectures.

order NTF benefits more from increasing the OSR (see equation (5.1)). Another observation is that for OSR = 7, the peak SQNR of 9-level/17-level $3^{rd}/4^{th}$ order single loop SDMs is limited to about 79 dB. For the same OSR, an ideal 9-level 2-1-1 MASH SDM can achieve a peak SQNR of about 111 dB. Comparing the 9-level 2-1-1 MASH SDM with the 9-level 4th order single loop SDM, the original unshaped quantization noise power and the noise shaping order are the same. However, the 9-level 2-1-1 MASH SDM achieves a much higher peak SQNR of 111 dB than the peak SQNR of 68 dB for the 9-level 4th order single loop SDM. The huge benefit of peak SQNR is caused by two advantages of MASH SDM: (1) 2-1-1 MASH SDM is built from 1st order and 2nd order SDM stages, which allow to use higher OBG and more aggressive noise shaping than 4th order SDM. For example, assuming the SDM architectures are optimized with MSA of at least 0.7 $V_{FS,DAC}$ ($V_{FS,DAC}$ is the full-scale equivalent voltage from the DAC feedback), the maximal OBG for a 9-level 4th order single loop SDM is 5, while the maximal OBG for a 9-level 2-1-1 MASH SDM is 16. (2) In 9-level 2-1-1 MASH SDM, inter-stage gains of $a_{12} = a_{23} = 8$ are used which suppresses the quantization noise of the 3rd stage by 36.1 dB. Notice that in practice the inter-stage gains have to be reduced to create margin, otherwise the 2nd and 3rd stages would become overloaded by the unavoidable circuit implementation non-idealities, such as the phase and gain inaccuracy of the loop transfer functions. Thus, in practice the peak SQNR difference between single-loop and MASH SDMs is smaller than that in Figure 5.1. From this analysis, a general conclusion can be drawn regardless of the technology nodes of the implementation: *MASH SDMs can achieve a certain BW and DR target with lower OSR than single-loop SDMs for the same quantizer resolution. In a certain technology, for a certain DR target, MASH*

Table 5.1: Empirical value of C_{N_O,N_Q} in [dB] assuming 1-tone sine input.

N_O \ N_Q	2-level	4-level	5-level	8-level	9-level	17-level
1	-7.1	-7.1	-6.4	-5.1	-6	-5.3
2	-21.2	-14.2	-11	-11.2	-9.5	-8.6
3	-37.3	-23.3	-21.7	-17.3	-16.9	-14
4	-57.4	-36.3	-36.5	-27.3	-26.3	-21.4

The values for $N_Q = 2, 4, 8$ level are extracted from Figure 4.14 - 4.16 in [19]. The values for $N_Q = 5, 9, 17$ level come from simulations with ideal SDM models in Matlab. The Delta Sigma toolbox is used [37].

SDMs can achieve broader BW than single-loop SDMs.

In the literature, empirical SQNR limits versus OSR plots can be found for single-loop SDMs with different NTF order and quantizer resolution [19]. In [75], two formulas are given for the $SQNR_{max}$ for 1st order and the 2nd order SDMs over the quantizer resolution and OSR. In the following, this thesis generalizes the simulation results in Figure 5.1 and proposes generic formulas to calculate the SQNR limits for both single-loop and MASH SDMs. A fitting parameter in these formulas is derived empirically. For single-loop SDMs, the SQNR limit can be calculated as:

$$SQNR_{max} = C_{N_O,N_Q} + 6.02 \cdot \Big(N_Q + (N_O + 0.5) \cdot log_2(OSR)\Big) \quad \text{[dB]} \tag{5.1}$$

In this formula, the term $6.02 \cdot \Big(N_Q + (N_O + 0.5) \cdot log_2(OSR)\Big)$ is taken from literature [76], and this thesis proposes that the fitting constant C_{N_O,N_Q} is determined by both N_Q and N_O. Here, N_Q is the quantizer resolution in bit, and N_O is the NTF order. In this formula, the term $6.02 \cdot N_Q$ indicates the impact of the original quantization noise power without the noise shaping. The term $6.02 \cdot (N_O + 0.5) \cdot log_2(OSR)$ shows the impact of the ${N_O}^{th}$ order noise shaping with OSR on the in-band quantization noise power. C_{N_O,N_Q} is a fitting constant in dB which is influenced by four parameters: (1) OBG (2) the input power which is linked to the $SQNR_{max}$ (3) zero optimization for $N_O \geq 2$ (4) the input signal waveform. Assuming 1-tone sine input, C_{N_O,N_Q} is a constant that can be optimized for a certain NTF order and quantizer resolution. Figure 3.4 (Chapter 3.2) shows that for the same NTF order (3 in this figure), the OBG for the peak SQNR increases when the quantizer resolution increases. For the same NTF order and OBG, the corresponding input amplitude A_{in} increases when the quantizer resolution increases. The empirical value of C_{N_O,N_Q} is presented in Table 5.1. In this table, the values of C_{N_O,N_Q} are corresponding to the maximal achievable SQNR of ideal SDMs for a certain NTF order and a certain quantizer resolution. OBG and A_{in} are different for the values of C_{N_O,N_Q} in this table.

Figure 5.2a shows the comparison between the simulated $SQNR_{max}$ and the calcu-

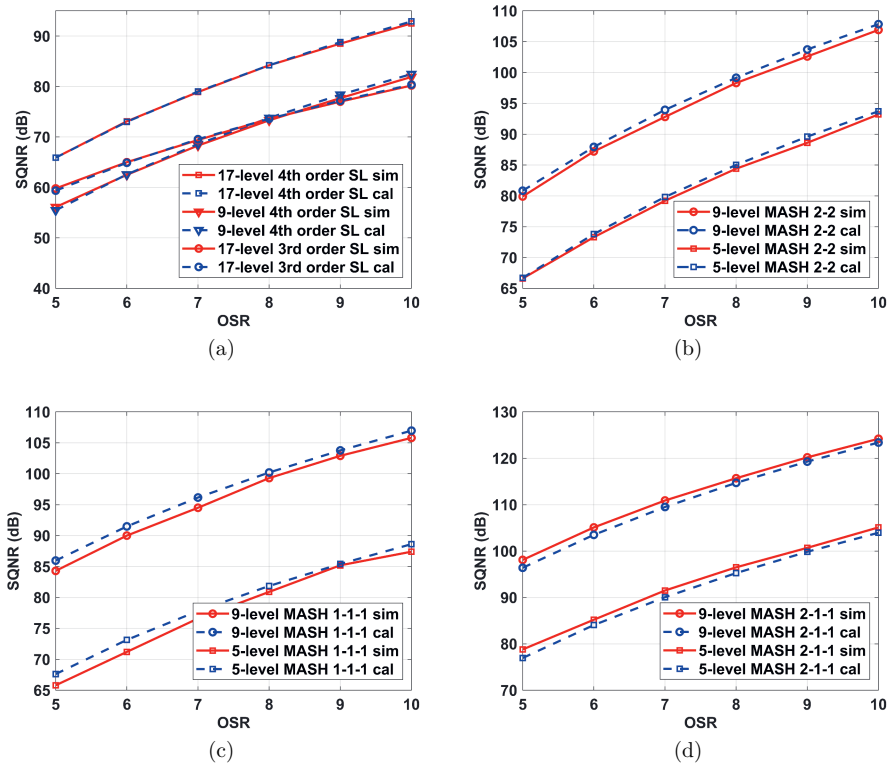


Figure 5.2: Comparison between simulated and calculated SQNR$_{max}$ versus OSR: (a) for 3rd order and 4th order single-loop SDM structures; (b) for 2-2 MASH structure; (c) for 1-1-1 MASH structure (d) for 2-1-1 MASH structure.

lated $SQNR_{max}$ with equation (5.1), for 3rd order and 4th order single-loop SDM architectures. The calculated $SQNR_{max}$ matches very well with the simulated $SQNR_{max}$, with a maximal error of 0.6 dB. It proves that the $6.02 \cdot (N_O + 0.5) \cdot log_2(OSR)$ term predicts the trend of $SQNR_{max}$ versus OSR, which is in some textbooks on SDMs as well [76]. By cross-checking the formula (5.1) with our simulation results and the literature [19], the accuracy of the formula (5.1) with the constant values in Table 5.1 is about $\pm$ 1 dB for the concerned single-loop SDMs (N_O between 1 and 4, N_Q between 1-bit and 17-level) with OSR between 5 and 16. Notice that in [75], the fitting constant only depends on the NTF order, but not on the quantizer resolution. In our formula (5.1), the fitting constant C_{N_O,N_Q} depends on both of the NTF order and the quantizer resolution, which is more accurate than [75] especially for NTF order $N_O \geq 2$.

As a next step, this thesis generalizes the results to MASH SDMs. Chapter 3.3.2

has shown the overall noise transfer function of a 2-stage MASH. The overall noise transfer function of a M-stage MASH can be generalized as:

$$NTF_{tot}(z) = \frac{1}{\prod_{i=1}^{M-1} a_{i,i+1}} \cdot \prod_{i=1}^{M} NTF_i(z) \tag{5.2}$$

Here, $a_{i,i+1}$ is the inter-stage gain from the ith stage to the (i+1)th stage. $NTF_i(z)$ is the noise transfer function of the ith stage.

For an M-stage MASH SDM, this thesis proposes the following empirical formula to calculate the SQNR limit:

$$\begin{aligned} SQNR_{max} = & \sum_{i=1}^{M} C_{N_{O,i},N_{Q,i}} + 6.02 \cdot \Big(N_{Q,M} + \sum_{i=1}^{M-1} log_2 a_{i,i+1} \\ & + (\sum_{i=1}^{M} N_{O,i} + 0.5) \cdot log_2(OSR) \Big) \quad \text{[dB]} \end{aligned} \tag{5.3}$$

Here, $N_{O,i}$ and $N_{Q,i}$ are the NTF order and the quantizer resolution in bit of the ith stage, i = 1, ..., M. $C_{N_{O,i},N_{Q,i}}$ is the corresponding constant of the ith stage. For the MASH structures in Figure 5.1, with a 9-level quantizer in the front-end stage, the ISG from this stage to the following stage is 8. And with a 5-level quantizer in the front-end stage, the ISG from this stage to the following stage is 4. In this formula, the term $\Big(C_{N_{O,i},N_{Q,i}} + 6.02 \cdot (N_{O,i} + 0.5) \cdot log_2(OSR)\Big)$ shows the impact of $NTF_i(z)$ on the overall $SQNR_{max}$ of the MASH. The term $6.02 \cdot log_2 a_{i,i+1}$ shows the impact of the ISG from the ith stage to the $(i+1)^{th}$ stage on the overall $SQNR_{max}$ of the MASH. Notice that both $NTF_i(z)$ and $a_{i,i+1}$ are in the overall NTF of the MASH in equation (5.2). The term $6.02 \cdot N_{Q,M}$ is because only the quantization noise of the last stage is in the final MASH output shaped by $NTF_{tot}(z)$, and the quantization noise of all front-end stages are canceled completely in the ideal MASH.

Figure 5.2b - 5.2d show the comparison between the simulated $SQNR_{max}$ and the calculated $SQNR_{max}$ with equation (5.3), for 3 MASH architectures. The constants C_{N_O,N_Q} extracted from the simulations of single-loop SDMs in Table 5.1 are used here. In Figure 5.2b - 5.2d, the maximal difference between calculated $SQNR_{max}$ and simulated $SQNR_{max}$ is 1.9 dB. By cross-checking the formula (5.3) with our simulation results, the accuracy of the formula (5.3) with the constant values in Table 5.1 is about ± 2 dB for the concerned MASH SDMs with OSR between 5 and 10.

The formulas (5.1) and (5.3) greatly simplify the assessment of the maximum achievable SQNR for various SDM architectures with different number of stages (M); different NTF order (N_O) and quantization resolution (N_Q) for these stages; the sequencing of the stages; and OSR. Although in Figure 5.1 all the quantizers of the MASH have the same resolution, the formula (5.3) can be used for the cases that the quantizers

of the MASH have different resolutions. Moreover, this empirically derived generalization of the problem provides insights which are useful for ΣΔ ADC architecture design. Firstly, the formula (5.3) implies that the $SQNR_{max}$ does not depend on the exact sequence of the MASH structures. For example, according to this formula, a 3-bit 2-1 MASH SDM and a 3-bit 1-2 MASH SDM have the same $SQNR_{max}$. Moreover, these two formulas give insights when comparing different MASH and/or single-loop structures. For example, if the 9-level 2-2 MASH structure is compared to the 9-level 2-1-1 MASH structure, their $\sum_{i=1}^{M} C_{N_{O,i},N_{Q,i}}$ values are very close (-19 dB for 2-2 MASH and -21.5 dB for 2-1-1 MASH), and it can be concluded that their $SQNR_{max}$ difference is mainly due to the fact that the 9-level 2-1-1 MASH has an extra ISG a_{23} which has a value of 8. Another example is to compare a 9-level 4th order single-loop SDM to a 9-level 2-1-1 MASH structure. Their total NTF order is the same. The quantizer resolution of the last stage in 2-1-1 MASH is the same as the 4th order single-loop SDM. Their $SQNR_{max}$ difference comes from two parts: (1) For the 9-level 4th order single-loop SDM, C_{N_O,N_Q} = -26.3 dB; while for the 9-level 2-1-1 MASH structure, $\sum_{i=1}^{3} C_{N_{O,i},N_{Q,i}}$ = -21.5 dB. (2) The effect of the inter-stage gains, represented by the term $6.02 \cdot \sum_{i=1}^{2} log_2 a_{i,i+1}$ boosts the $SQNR_{max}$ of the 9-level 2-1-1 MASH structure by 36.1 dB, which is not in the formula for the 9-level 4th order single-loop SDM.

With equations (5.1) and (5.3), the $SQNR_{max}$ of various single-loop and MASH structures can be calculated with different NTF order, quantizer resolution, OSR and MASH stages. For example, a 1-2 MASH SDM with OSR = 8.6 and two 17-level quantizers is reported in [16]. For this architecture, it can be calculated that the $SQNR_{max}$ is about 100 dB, assuming its maximal $a_{12} = 16$ for the 17-level quantizer.

For a certain bandwidth and resolution (SNDR or DR) target in a certain technology, an optimal OSR can be chosen to minimize the power consumption of the CT ΣΔ ADC. If the OSR is too high, an unnecessary high sampling rate leads to stringent requirements on the quantizer core regeneration time constant, the loop filter amplifier GBW, and the propagation delay from quantizer to DACs. So, it leads to unnecessarily high power consumption and design efforts. On the other hand, if the OSR is too low, to achieve the target SQNR, higher resolution quantizer and/or higher-order loop filter are needed [19]. For a flash-ADC-based quantizer, the total number of comparators is almost doubled when the quantizer resolution increases by 1-bit, and the comparator offset requirement is tighter. A higher-order loop filter generally requires more amplifiers, and it is more sensitive to parasitic poles and extra delay in the loop. Thus, both higher quantizer resolution and higher order loop filter lead to higher power consumption. The power consumption of the broadband CT ΣΔ ADCs is closely related to the circuit implementations as well.

Figure 5.1 shows the maximal achievable SQNR of ideal SDMs. However, in the real implementation, thermal noise, clock jitter, DAC non-linearity, loop filter amplifier limited GBW etc. all degrade the SNDR of the SDM. Thus a margin between the maximal SQNR of the ideal SDM and the SNDR target is necessary. To be able to

choose the optimal OSR, quantizer resolution, and order for the ADC test chip, this thesis considers the limitations from the implementation technology as well. Figure 4.9 has shown the speed-resolution limitation of the chosen 40 nm CMOS technology. *Considering Figure 5.1, Figure 4.9 and the required margin between the maximal SQNR and the SNDR target, it is not very realistic to design a single-loop ΣΔ ADC achieving the target SNDR of 60 dB and BW of 500 MHz. Thus, this thesis decides to choose a MASH structure.*

For the 1st stage of the MASH, this thesis decides to design a 2nd order SDM loop for the following reasons:

- 1st and 2nd order SDMs are more robust against parasitic poles and extra delay in the loop than higher order SDMs.
- A 2nd order SDM stage allows to implement a pair of optimized zeros, which can largely improve the peak SQNR (see Chapter 3.2).
- With the sample quantizer resolution, 2nd order SDM is less tonal than 1st order SDM. Thus, dithering is not compulsory for a 2nd order SDM for this application, which can simplify the overall system.
- For a 3-bit 1st order SDM, the MSA is about 1 $V_{FS,DAC}$. For a 3-bit 2nd order SDM, the MSA is about 0.9 $V_{FS,DAC}$. The difference in the signal power (1.8 dB) is not the dominant argument for this choice.

For the 3rd reason, this thesis would like to give further comments. For a MASH structure with a 1st order SDM as its 1st stage, ideally the tones in the quantization noise of the 1st stage is canceled by the MASH. However, a tonal 1st order 1st stage still introduces tones in the final MASH output in the following two cases: (1) When the back-end stages are overloaded, or when the analog transfer function is not ideally matched with the digital NCF, the tones in the quantization noise of the 1st stage cannot be fully canceled. (2) If the tones from the quantization noise of the 1st order 1st stage cause some extra tones (with different phase, amplitude, or frequency) at the DAC or the loop filter because of the non-linearity of the DAC or the loop filter, those extra tones cannot be canceled by the MASH and they will be present in the final MASH output. In some published MASH ADCs with a 1st order SDM as the 1st stage, dithering is applied at the cost of the dynamic range reduction [16].

From the aforementioned analysis, this thesis has chosen a MASH structure with a 2nd order SDM as its 1st stage. From Figure 4.9 it is estimated that the maximal sampling rate with 3-bit quantization in 40 nm CMOS is about 6 - 7 GHz. For the back-end stages, this thesis chooses 1st order SDMs because of its robustness and simplicity. Considering the peak SQNR potential, this thesis decides to design a 3-bit 2-1-1 MASH SDM test chip with OSR of 7 (thus F_S = 7 GHz). This thesis uses 3-bit (8-level) quantizers instead of 9-level quantizers to make the saving of the SDM output in an on-chip memory more efficient. With the formula (5.3), it can

be calculated that the $SQNR_{max}$ of a 3-bit 2-1-1 MASH SDM with OSR of 7 is about 106 dB, assuming its maximal $a_{12} = a_{23} = 7$ for the 3-bit quantizers. Its $SQNR_{max}$ is 6 dB higher than the 1-2 MASH SDM architecture with OSR = 8.6 and two 17-level quantizers reported in [16]. Moreover, to achieve the target 500 MHz BW, the 17-level 1-2 MASH SDM architecture with OSR = 8.6 requires to implement an SDM with 17-level quantization at 8.6 GHz, which seems not realistic (taking into account a reasonable power consumption) in 40 nm CMOS technology based on the information in Chapter 4.7 (Figure 4.9), while with the proposed 3-bit 2-1-1 MASH SDM architecture with OSR of 7, it requires to implement an SDM with 3-bit (8-level) quantization at 7 GHz, which is more realistic for the 40 nm CMOS technology.

For 3-bit 2-1-1 MASH architecture, the $SQNR_{max}$ of the ideal MASH SDM (106 dB) is much higher than the target specification of SNDR = 60 dB, which can make sure that the SNR is dominated by thermal noise instead of quantization noise, and at the same time leaves margin for system level optimization. Because of implementation difficulties (shown in Chapter 11.1), optimized zeroes are not used on the test chip. Much reduced inter-stage gains $a_{12} = 1.8$ and $a_{23} = 2.5$ are chosen to leave margin to accommodate implementation non-idealities. With these inter-stage gains, only the middle 4 (out of 8) quantization levels are triggered in the 2nd and 3rd loops in the ideal MASH SDM with full-scale input. With circuit implementation, due to the limited GBW of loop filter amplifiers, MASH SDM parameter variation and parasitic poles in the loop, the full-swing of the quantizers in the 2nd and 3rd loops are used with full-scale SDM input, justifying the choice of the ISG. Due to the reduction of the ISG from $a_{12} = a_{23} = 7$ to $a_{12} = 1.8$ and $a_{23} = 2.5$, the SQNR of the ideal MASH SDM is reduced from 106 dB to 89 dB. Since the optimized zeroes are not used on the test chip, the SQNR of the ideal MASH SDM is further reduced from 89 dB to 77.6 dB. The discrete-time model of the 3-bit 2-1-1 MASH SDM architecture is shown in Figure 5.3.

5.2 A generic synthesis flow for broadband CT MASH SDMs

In this section, the synthesis flow of a broadband CT MASH SDM architecture is presented. It is a generic synthesis flow which can be used for other broadband CT MASH SDM architectures with 1 T_S ELD compensation as well. This flow is suitable when the ELD is the dominant problem in the architecture design of broadband CT MASH ΣΔ ADCs. Its flowchart is shown in Figure 5.4.

1. Synthesize a DT MASH SDM model with zero loop delay based on the choices on the design parameters considering the target specifications. Then its internal loop filters (ILFs) and connecting loop filters (CLFs) in DT are derived [72].

2. Choose a CT MASH SDM model with 1 T_S loop delay, ELD compensation and

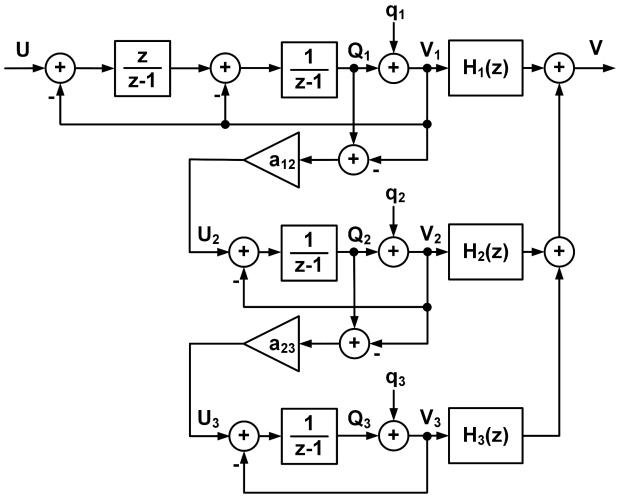


Figure 5.3: DT 2-1-1 MASH SDM model.

symbolic coefficients based on the required design freedom and implementation feasibility. Its ILFs and CLFs in CT are derived.

3. Perform CT-to-DT transformation with the impulse-invariant transformation method of the CT ILFs and CLFs with symbolic coefficients [36]. The equivalent DT ILFs and CLFs of the CT MASH model are obtained.

4. Equate the equivalent DT ILFs and CLFs (obtained in Step 3) with the desired DT ILFs and CLFs (obtained in Step 1). The coefficients of the CT MASH model are calculated by solving the equations.

5. Calculate the noise cancellation filters.

This synthesis flow starts with a DT MASH SDM with zero loop delay, and derive an equivalent CT MASH SDM with 1 T_S loop delay. This thesis considers it a better approach than directly synthesizing a CT MASH SDM in s-domain [73] for the following reasons: (1) It is straightforward to calculate the coefficients for a DT MASH SDM with zero loop delay when the main design parameters (OSR, order, OBG, etc.) are chosen. The CT-to-DT transformation and equations can be calculated and solved by Matlab. (2) In this synthesis flow, both the CT MASH SDM model and its equivalent DT MASH SDM model are acquired. Thus, it offers the flexibility to use the equivalent DT MASH SDM model for some simulations where it is more suitable, e.g. quantization gain simulation.

This section focuses on the mapping of the NTF. Other system-level optimization options such as STF optimization and dynamic range scaling are introduced in Section 5.3.

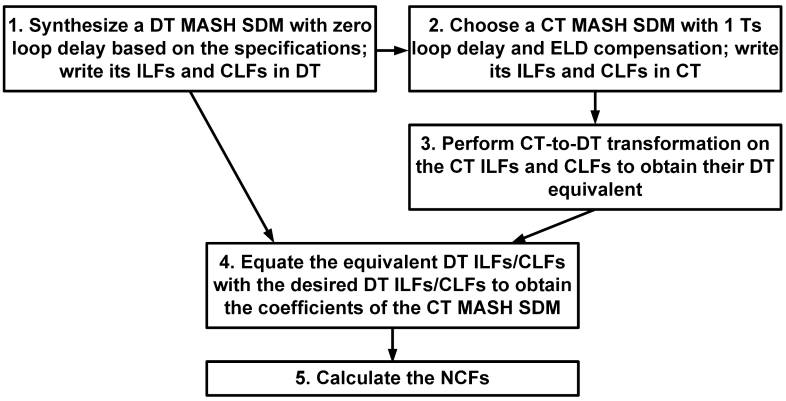


Figure 5.4: Flowchart of a generic synthesis procedure of broadband CT MASH SDMs.

5.2.1 Desired DT MASH SDM model

The desired DT MASH SDM model with zero loop delay is designed based on the requirements from the application and feasibility of implementation. It has been shown in the last section in Figure 5.3.

For the chosen 2-1-1 MASH architecture, 3 ILFs and 3 CLFs need to be mapped between the desired DT MASH model and the chosen CT MASH model. The internal loop filters are defined as the transfer function from the quantizer's output to the quantizer's input in the same SDM stage, and the connecting loop filters are defined as the transfer function from the quantizer's output of the upper stage to the quantizers' inputs of the lower stages. Here this thesis takes one ILF and one CLF as examples. In the desired DT MASH model (Figure 5.3), the ILF of the SDM stage 1 is the transfer function from V_1 to Q_1, which can be written as:

$$LF_{1,DT} = -\frac{2z-1}{(z-1)^2} \tag{5.4}$$

The CLF from stage 1 to stage 2 is the transfer function from V_1 to Q_2, which can be written as:

$$LF_{12,DT} = -\frac{a_{12}z^2}{(z-1)^3} \tag{5.5}$$

5.2.2 CT MASH SDM model

This thesis proposes a broadband CT MASH SDM model with enough design freedom which is feasible for circuit implementation. One clock period ELD is compensated in every SDM stage, which is essential for broadband applications. Connection paths

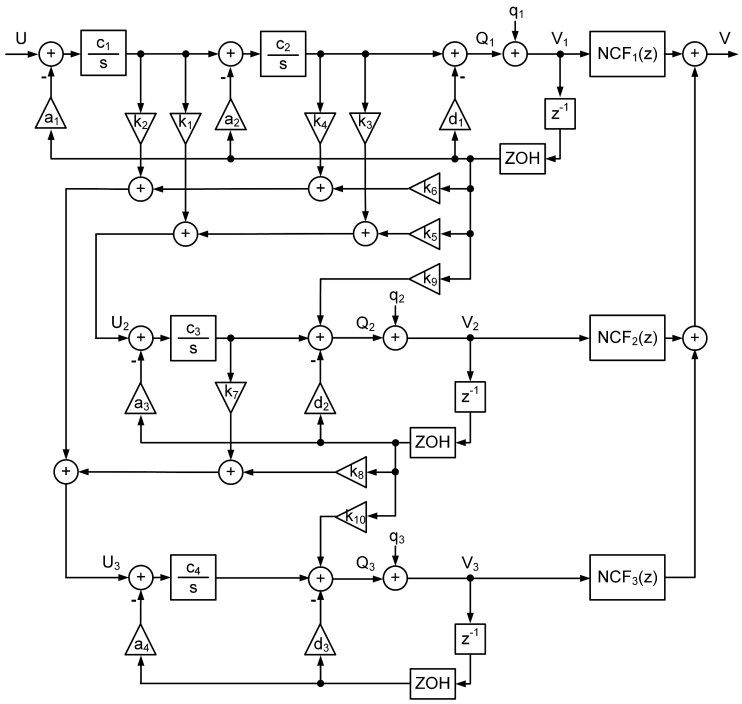


Figure 5.5: Initial CT 2-1-1 MASH SDM model.

$k_1 \sim k_{10}$ between the SDM stages offer the required design freedom to map both ILFs and CLFs [72, 77]. The initial CT model of the 3-bit 2-1-1 MASH SDM architecture is presented in Figure 5.5, which includes the paths needed for NTF mapping, but excludes the paths required for system-level optimization introduced in Section 5.3.

At this step, this thesis uses normalized sampling rate of $F_S = 1$, and dynamic range scaling of the CT model will be applied after the coefficients $a_1 \sim a_4$, $d_1 \sim d_3$ and $k_1 \sim k_{10}$ are calculated. Thus, at this step $c_1 = c_2 = c_3 = c_4 = 1$. Here, the total delay in the ELD feedback loop (e.g. from node V_1 through d_1 to node Q_1) is 1 (T_S). It indicates that at the next quantizer sampling moment, the ELD feedback signal is settled at the quantizer input. In circuit implementation, the quantizer delay is less than 1 (T_S), to allow the ELD DAC to settle.

In the CT MASH model (Figure 5.5), the corresponding ILF and CLF can be written as:

$$LF_{1,CT} = -\frac{a_1 + a_2 s}{s^2} - d_1 \tag{5.6}$$

$$LF_{12,CT} = -\frac{(a_1 k_1 + a_2 k_3)s + a_1 k_3}{s^3} + \frac{k_5}{s} + k_9 \tag{5.7}$$

Here, the ELD z^{-1} is not included in the equations (5.6) and (5.7), which will be

included in the following mapping equations (5.10) and (5.11).

5.2.3 CT-to-DT transformation

In this step, impulse-invariant transformation is applied to the CT ILFs and CLFs to get their DT equivalent [36]. Non-return-to-zero DAC pulse is used in this design, as multi-bit NRZ DAC is less sensitive to clock jitter than the return-to-zero DAC pulse. 1 T_S ELD is considered in the SDM loop. Thus, the equivalent DT transfer functions of the aforementioned CT ILF and CLF can be calculated as:

$$LF_{1,DT,eq.} = (1 - z^{-1})\mathcal{Z}\Big\{\mathcal{L}^{-1}\{\frac{LF_{1,CT}}{s}\}\Big\} \tag{5.8}$$

$$LF_{12,DT,eq.} = (1 - z^{-1})\mathcal{Z}\Big\{\mathcal{L}^{-1}\{\frac{LF_{12,CT}}{s}\}\Big\} \tag{5.9}$$

5.2.4 Equating equivalent and desired DT transfer functions

To ensure that the CT MASH model is equivalent to the desired DT MASH model regarding the noise transfer function, both ILFs and CLFs should be equivalent. Thus, the following equations can be written. Notice that the ELD z^{-1} in the CT MASH model is taken into account in the mapping here.

$$LF_{1,DT,eq.} = z \cdot LF_{1,DT} \tag{5.10}$$

$$LF_{12,DT,eq.} = z \cdot LF_{12,DT} \tag{5.11}$$

By solving the equations from the mapping of 3 ILFs and 3 CLFs, the value of the coefficients $a_1 \sim a_4$, $d_1 \sim d_3$ and $k_1 \sim k_{10}$ in the CT MASH model is acquired.

5.2.5 Noise cancellation filters calculation

The principle of NCF calculation has been shown with an exemplary 2-stage MASH in Chapter 3.3.2. Here, from the CT MASH model with determined coefficients, the NTF and STF of every stage can be calculated as follows.

$$NTF_1 = \frac{(z-1)^2}{z^2} \tag{5.12}$$

$$NTF_2 = NTF_3 = \frac{z-1}{z} \tag{5.13}$$

$$STF_1 = STF_2 = STF_2 = \frac{1}{z} \tag{5.14}$$

Thus, the NCFs for this 3-stage MASH can be calculated as:

$$NCF_1(z) = STF_2(z) \cdot STF_3(z) \tag{5.15}$$

$$NCF_2(z) = \frac{NTF_1(z) \cdot STF_3(z)}{a_{12}} \tag{5.16}$$

$$NCF_3(z) = \frac{NTF_1(z) \cdot NTF_2(z)}{a_{12}a_{23}} \tag{5.17}$$

5.3 System-level optimization

This section discusses further steps on the system-level optimization for the broadband CT MASH SDM architecture, including signal transfer function optimization and dynamic range scaling.

Signal transfer function of the CT MASH SDM can be optimized separately to the noise transfer function. Signal feedforward paths $b_2 \sim b_5$ are added in the CT MASH SDM architecture, shown in Figure 5.6. Their value is optimized such that the STF is flat in-band, and low-pass filtering out-of-band. At the same time, the UGBW of the 1st integrator c_1 is maximized to suppress the noise and non-linearity of the 2nd integrator ($\frac{c_2}{s}$) and 2nd DAC (a_2).

Afterwards, dynamic range scaling is applied to the CT MASH model. For the chosen 40 nm CMOS technology, the supply voltage of thin-oxide transistors is 1.1 V. The maximal swing at 4 integrators' output are scaled to be ± 0.5 V, considering different input frequency and full-scale input amplitude. If the integrator output swing is too large, the non-linearity of the amplifier in the implementation of this integrator can deteriorate the linearity of the MASH ADC. If the integrator output swing is too small, it implies that the UGBW of this integrator can be further increased to suppress the noise and non-linearity contributed by the back-end blocks of this integrator. In the end of this step, a CT 2-1-1 MASH SDM model with all coefficients is synthesized.

5.4 System-level verification and block-level specifications

To check the performance and robustness of the CT 2-1-1 MASH SDM architecture, and to define specifications for the building blocks, various system-level verifications of the 2-1-1 MASH model have been done in Matlab. Firstly, the SQNR of the ideal CT MASH SDM model with different input power is simulated, which is plotted in Figure 5.7a. The input frequency is 159 MHz, which is slightly lower than $\frac{1}{3}$ of the signal bandwidth, such that up to 3rd order harmonic (HD3) are in-band. Simulated dynamic range set by the in-band quantization noise is 77.6 dB. Simulated peak SQNR

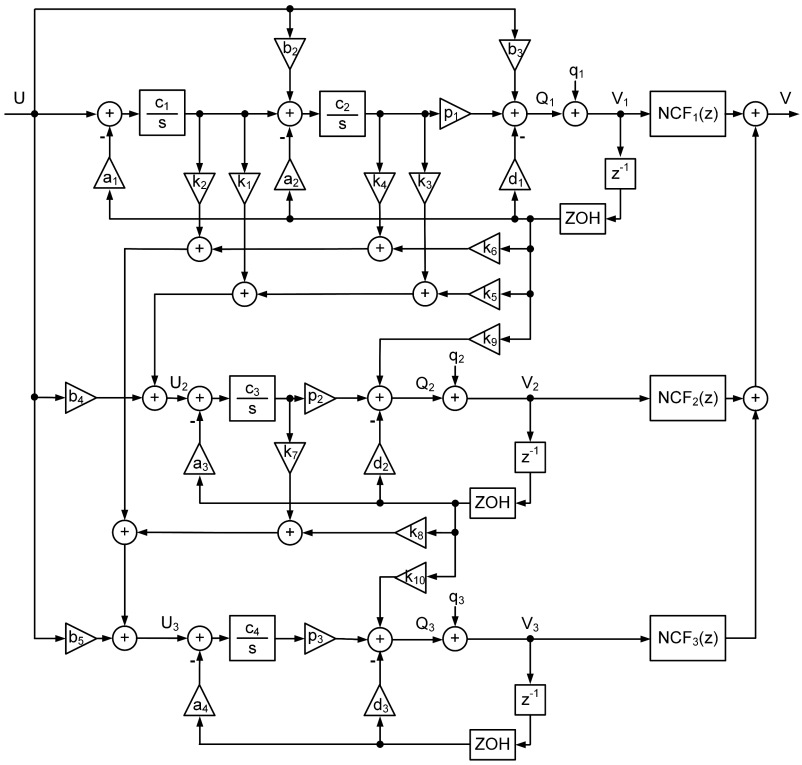


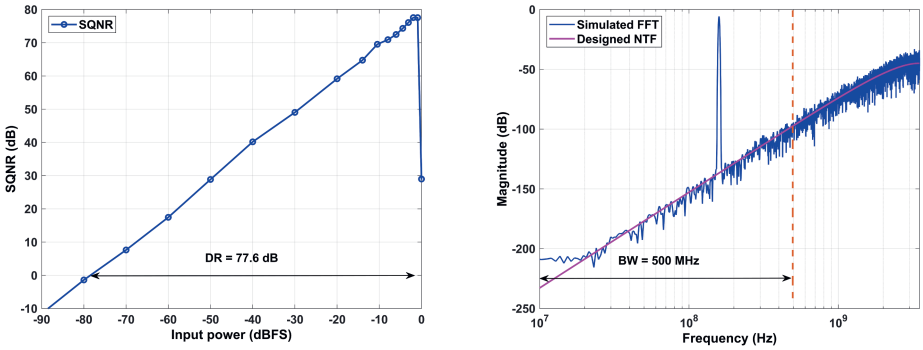
Figure 5.6: CT 2-1-1 MASH SDM model after system-level optimization.

is 77.6 dB, which is reached at an input amplitude of A_{in} = 0.8 V. The simulated output spectrum for the peak SQNR is shown in Figure 5.7b.

For the chosen ADC sampling rate of 7 GS/s, clock jitter is a very important specification for the design of the clock circuitry. Chapter 4.4 shows that CT ΣΔ ADCs are sensitive to the jitter in the DAC clock, while less sensitive to jitter in the quantizer clock. This thesis models clock jitter in the proposed CT MASH model and simulates its effect. Figure 5.8 presents the simulated SNDR versus the jitter of the DAC clock with input amplitude A_{in} = 0.7 V and input frequency f_{in} = 159 MHz. In literature it is written that for a low-pass ΣΔ ADC with NRZ DAC pulse, when the SNR is completely limited by the white jitter noise, the SNR can be calculated as [61, 78]:

$$SNR_{jitter} = 10 \cdot log_{10} \frac{OSR \cdot V_{in}^2}{2\sigma_{\delta y}^2 (\frac{\sigma_j}{T_S})^2} \quad \text{[dB]} \tag{5.18}$$

Here, V_{in} is the input amplitude. $\delta y = y(n) - y(n-1)$ and $y(n)$ is the SDM output. $\sigma_{\delta y}^2$ is the variance of δy, and σ_j is the standard deviation of the white jitter noise. From both Figure 5.8 and equation (5.18), for low-pass CT SDM with NRZ DAC



(a) (b)

Figure 5.7: (a) Simulated SQNR vs. input power for CT 2-1-1 MASH architecture (b) Simulated output spectrum for the peak SQNR.

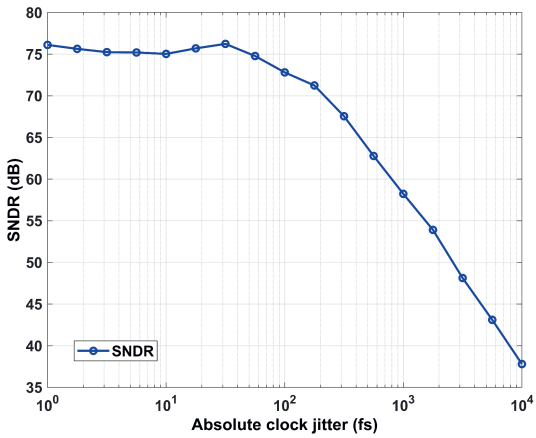


Figure 5.8: Simulated SNDR vs. clock jitter of the DAC clock.

pulse, when the SNR is completely dominated by the white jitter noise, the SNR reduces by 20 dB when the white jitter standard deviation σ_j increases by 10 times. Since the clock jitter error is designed to be not dominant in the SNDR of the ADC test chip, the DAC clock jitter specification is set to be less or equal to 100 fs.

To achieve the required quantization gain is essential for the SNDR target for broadband CT ΣΔ ADCs (see Chapter 4.2). Limited quantization gain is modeled using the linear gain model (equation (4.11)). The simulation with limited quantization gain is done with the DT MASH model for the following 3 reasons: (1) the CT MASH model and its equivalent DT MASH model show the same metastability behavior.

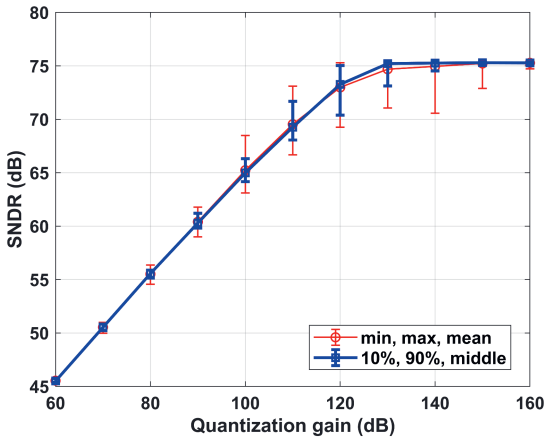


Figure 5.9: Simulated SNDR vs. quantization gain.

(2) Metastability error is a stochastic phenomenon, and for the target simulation accuracy, a very large number of samples (2^{20} sample) is simulated multiple times independently to achieve accurate result for quantization gain of 100 dB $\sim$ 160 dB. (3) With the CT SDM model, many points (close to 100) need to be calculated by the simulator in every clock period, while with the DT SDM model, only one point needs to be calculated in every clock period. Thus, for the same number of samples, the simulation speed with DT SDM model is about 100 times faster than the CT SDM model. Figure 5.9 shows the simulated SNDR versus the quantization gain, with input amplitude A_{in} = 0.7 V and input frequency f_{in} = 159 MHz. For every quantization gain, 50 independent simulations are run. Some statistics of the simulated SNDR are plotted, such as minimal, maximal, mean values (red line) and 10%, 90% and middle values (blue line). When the quantization gain is 130 dB, all of the 50 independent simulations achieve SNDR $\geq$ 71 dB, and 90% of the runs achieve SNDR $\geq$ 73 dB. Considering the SNDR target for this test chip is 60 dB, the target specification for the quantization gain is chosen to be higher or equal to 130 dB. Here, this thesis considers applications for which multiple measurements are done and the metastability error power averages out by the large amount of samples, such as automotive radar. However, some other applications can have a more stringent requirement for the occurrence rate of the metastability error.

The robustness of the proposed CT 2-1-1 MASH architecture is checked with simulations. All the parameters (a, b, c, d, k, p in Figure 5.6) are modeled with a Gaussian distributed error with a standard deviation σ. For every σ, 50 independent simulations are run. The simulated SNDR versus parameter variation σ is plotted in Figure 5.10. Some statistics of the simulated SNDR are plotted similar as in Figure 5.9, such as minimal, maximal, mean values (red line) and 10%, 90% and middle values (blue line). For CT MASH SDMs, the parameter variations can deteriorate

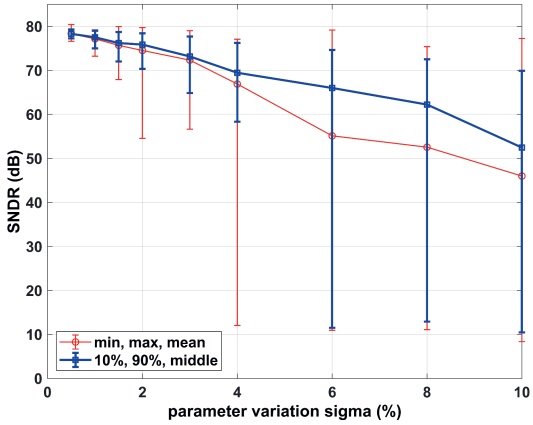


Figure 5.10: Simulated SNDR with parameter variations.

the SNDR or even the stability of the SDM for the following three reasons: (1) The parameter variations make the actual NTF deviating from the ideal NTF, which can deteriorate the SNDR and even the stability. (2) Because of the parameter variations, the analog transfer functions of the quantization noise do not match with the digital NCFs anymore, which causes noise leakage of the front-end quantization noise in the MASH output and deteriorates the resolution [42, 73]. (3) The parameter variations change both the noise transfer functions and the signal transfer functions, which can make the back-end stages of the MASH overloading with either the front-end quantization noise or the input signal. When the back-end stages are overloaded, part of the information on the quantization noise of the front-end stages is lost, and the front-end quantization noise cannot be efficiently canceled. Notice that the first point applies to single-loop SDMs as well, while the last two points are specific for MASH structures. With $\sigma = 1\%$, all 50 independent simulations achieve SNDR $\geq$ 73.2 dB, and 90% of the runs achieve SNDR $\geq$ 75 dB. With $\sigma = 2\%$, 90% of the runs achieve SNDR $\geq$ 70.4 dB.

Many other non-idealities are modeled and simulated with the CT MASH model or the equivalent DT MASH model. Based on the simulation results, ADC block-level and system-level target specifications are drawn, which are summarized in Table 5.2. The DC gain and parasitic pole specifications on the integrators is presented in Chapter 6, where the analog and digital filter mismatch calibration is considered.

Table 5.2: MASH ADC block- and system-level target specifications

Items		Target specifications
DAC clock jitter (RMS)		$\leq$ 100 fs
DAC static mismatch	DAC A1	$\sigma \leq 6 \cdot 10^{-4}$
	DAC A2 and K5	$\sigma \leq 1.2 \cdot 10^{-3}$
	Other DACs	$\sigma \leq 7 \cdot 10^{-3}$
Clock skew mismatch between DAC unit elements		$\sigma \leq$ 400 fs
Quantization gain	Quantizer 1	$\geq$ 130 dB
	Quantizer 2 and 3	$\geq$ 110 dB
Quantizer unit element offset mismatch		$\sigma \leq 2\%$ V_{FS} quantizer
Quantizer hysteresis		$\leq 7\%$ V_{FS} quantizer
Integrator non-linearity	Integrator 1	$h_3 \leq 0.01$
	Integrator 2	$h_3 \leq 0.03$
$V_{out} = (V_{in} - h_3 V_{in}^3)\frac{c_i}{s}$	Integrator 3 and 4	$h_3 \leq 0.1$
Loop delay variation		$\leq \pm$ 0.05 T_S
Parameter variation (a, b, c, d, k, p in Figure 5.6)		$\sigma \leq 1\%$

5.5 Conclusions

The synthesis of a broadband CT ΣΔ ADC architecture starts from a comparison of peak SQNR among multiple DT multi-bit single-loop and MASH ΣΔ ADC architectures. For broadband medium-to-high resolution CT SDMs, any resolution (SNDR or DR) target point imposes a bandwidth limitation for all relevant technology nodes in case of single loop SDMs. For CT MASH SDMs this limitation can be alleviated to allow for a broader bandwidth at the cost of complexity. This chapter proposes generic formulas to calculate the SQNR limits for both single-loop and MASH SDMs, which reduces the complexity of system level design and comparison significantly. Considering the speed-resolution limit of the 40 nm CMOS technology, a 3-bit 2-1-1 MASH ΣΔ ADC architecture is chosen for the test chip implementation because of its robustness and potential for broadband application. This MASH architecture shows 6 dB higher $SQNR_{max}$ potential than the 1-2 MASH architecture reported in [16], and it is more realistic to be implemented in the chosen 40 nm CMOS technology because of its lower sampling rate and quantizer resolution. A generic synthesis flow for broadband CT MASH SDMs is presented here, and a CT 2-1-1 MASH SDM architecture with 1-T_S ELD compensation is synthesized including system level optimization. Various

system-level simulations are run in Matlab, which show the robustness of the chosen architecture. Block-level and system-level design specifications are drawn based on the simulation results. The synthesized CT 3-bit 2-1-1 MASH $\Sigma\Delta$ ADC architecture is feasible to be implemented in the chosen 40 nm CMOS technology.

Part II

Novel design concepts

Chapter 6

A digital calibration technique for broadband CT MASH ΣΔ ADCs

This chapter proposes a digital automatic calibration method for broadband continuous-time MASH ΣΔ ADCs [79]. The main contribution of this method is the calibration of the errors due to the limited DC gain and 2nd pole of the loop filter integrators. Without the proposed calibration technique, the stringent DC gain and 2nd pole requirements demand power-hungry loop filter implementation, and the noise leakage due to the limited DC gain and 2nd pole can degrade the resolution of the MASH ΣΔ ADCs. The digital noise cancellation filters are calibrated by successive estimation of the DC gains and the 2nd pole, and updating the coefficients of the FIR filters. Extensive system-level and transistor-level simulations demonstrate the effectiveness and robustness of the proposed method. For an exemplary MASH ΣΔ ADC with BW of 600 MHz and SQNR of 75 dB, it can reduce the DC gain requirement by 15 dB, and the 2nd pole requirement by three times, making it an enabling technique for power-efficient GHz-range ΣΔ ADC applications. Although the exemplary 2-1-1 MASH ADC architecture in this chapter is slightly different compared to the 2-1-1 MASH architecture shown in Chapter 5 regarding the sampling rate, signal bandwidth, quantizer resolution and NTF, the proposed digital automatic calibration is generic and can be directly applied to the MASH architecture of the test chip implementation.

6.1 Introduction

Generally, two error sources negatively impact the accuracy of the SDM parameters – spread and device mismatch. The spread is caused by a process variation in the fabrication, supply voltage and temperature variations. The spread causes a common relative error on all of the same type of devices on chip, e.g. a common relative error on the resistance value of poly resistors, on the capacitance value of fringe capacitors, and on the threshold voltages of the PMOS and NMOS transistors. Device mismatch

is caused by the fabrication inaccuracy, which introduces different relative errors on the same type of devices [71].

Generally, the resolution of CT MASH ΣΔ ADCs is limited by the mismatch between analog loop filters and digital noise cancellation filters. Among all error sources, a dominant error source is the RC spread error, which causes the same relative error on the unity-gain bandwidth of all integrators. It can be typically up to ±30%. To overcome the limitation of the RC spread error, digital calibration [42] or digitally assisted analog tuning [73] have been demonstrated. RC spread calibration alone is usually sufficient to regain the SQNR for MASH ADCs with several tens of MHz BW, but for broadband MASH ADCs discussed in this thesis, the DC gain and 2nd pole effects of the analog integrators need to be taken into account as well.

The work of [80] proposes a digital calibration which can compensate the SNDR drop caused by both the RC spread and the finite gain and bandwidth of the opamps. It employs a Block Least Mean Square (BLMS) algorithm for adaptive tuning of the FIR filters. To ensure the convergence of the BLMS algorithm, it uses a very small step size μ (2^{-12} to 2^{-22}), a very large block size (2^{18}) and it needs a long calibration time (3000 iterations). Moreover, the BLMS algorithm is relatively complicated and requires multipliers, high order FIR filters (order 40) and a dither signal generator. The work of [80] calibrates the RC spread error in the digital domain; it does not correct the UGBW of the analog integrators. To avoid overloading of the cascaded loops, extra margin must be reserved for the large RC spread error by decreasing the inter-stage gains. Consequently, the maximal achievable SQNR is reduced.

In this chapter, a digital calibration algorithm for the integrator DC gain (A_{DC}) and 2nd pole (f_{p2}) is presented, which assists a preceding analog calibration of the RC spread errors as well. Firstly, the calibrations of the RC spread error and the error due to the limited A_{DC} and f_{p2} are split. The RC spread error is calibrated by the analog tuning. The digital part of the proposed calibration method focuses on the limited A_{DC} and f_{p2}, which makes it more efficient than [80]. Moreover, by analysing the error mechanisms, this thesis approximates them by a linear dependence between the NCF coefficients correction factors and the reciprocal of the DC gain A_{DC}^{-1} (or the reciprocal of the 2nd pole f_{p2}^{-1}). Based on this, the proposed method shows fast convergence and low calculation complexity. It needs simple hardware and is suitable for low-cost integration. Section 6.2 describes the modelling and analysis of the loop filter non-idealities. Section 6.3 presents the error sources causing the mismatch between the analog transfer function of the quantization noise and the digital NCF. Section 6.4 introduces the analog RC calibration. Section 6.5 presents the proposed digital calibration algorithm. System-level and transistor-level simulation results are shown in Section 6.6. Finally, Section 6.7 draws the conclusions.

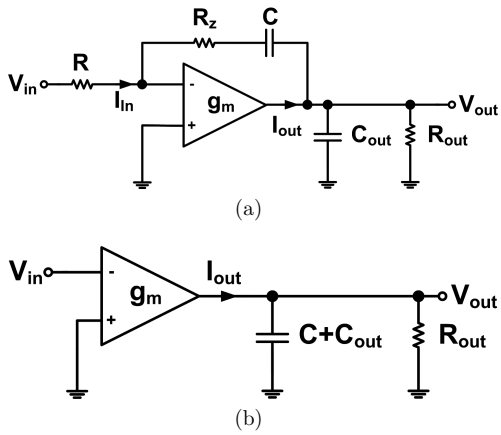


Figure 6.1: Model of the (a) RC integrator and (b) Gm-C integrator.

6.2 Modelling of the loop filter non-idealities

Chapter 4.1 shows that CT integrators can be implemented as either RC integrators (Figure 6.1a) or Gm-C integrators (Figure 6.1b). Here this chapter recaps their properties on linearity, DC gain and 2nd pole, and further give their models with limited DC gain and 2nd pole. The RC integrator shows better linearity and it has been commonly implemented as the 1st integrator at the input stage [42], where the integrator non-linearity is not shaped. However, the capacitance at the output of the amplifier (C_{out}) creates a 2nd pole in the transfer function of the RC integrator, which restricts its use in the fast loops. The transfer function of the RC integrator is modelled as (6.1), in which $UGBW$ is the designed UGBW of the RC integrator, and A_{DC} and f_{p2} are its DC gain and 2nd pole.

$$\frac{V_{out}}{V_{in}} = \frac{UGBW}{\frac{UGBW}{A_{DC}} + s + \frac{1}{2\pi f_{p2}} \cdot s^2} \tag{6.1}$$

On the contrary, the Gm-C integrator uses the amplifier in an open loop. It cannot achieve as high linearity as the RC integrator. The amplifier output capacitance C_{out} is in parallel with C, which does not create a 2nd pole, and only adds to the wanted pole. Gm-C integrators are commonly used in the high-speed paths, where the integrator non-linearity is shaped [42]. Its transfer function is modelled as:

$$\frac{V_{out}}{V_{in}} = \frac{UGBW}{\frac{UGBW}{A_{DC}} + s} \tag{6.2}$$

The following section discusses the impact of the limited DC gain and 2nd pole on the performance of MASH ΣΔ ADCs.

6.3 Mismatch between analog filter and digital NCF

This thesis considers the following three error sources causing the mismatch between the analog transfer function of the quantization noise and the digital NCF: (1) the RC spread (2) the limited DC gain and 2nd pole of the integrators (3) the parameter variation due to the device mismatch. In the following they are discussed.

The RC spread is a well-known problem for the CMOS technology. For the exemplary 2-1-1 MASH SDM used in this chapter, $\pm$ 20% RC time constant error causes a degradation of the peak SNDR from 75 dB to 48 $\sim$ 50 dB (shown in Figure 6.6). The calibration for the RC time constant error is introduced in Section 6.4.

The limited DC gain and 2nd pole of the integrators make the actual analog transfer functions of the quantization noise deviating from the ideal transfer functions. Thus, the actual analog transfer functions of the quantization noise are not matched with the digital NCFs, which causes noise leakage of the front-end quantization noise to the MASH output. The leaking front-end quantization noise is shaped by an NTF with less order than the ideal NTF of the MASH. Thus, the limited DC gain and 2nd pole can deteriorate the resolution of MASH SDMs. After the RC time constant error is calibrated, the limited DC gain and 2nd pole become dominant for the mismatch between the analog transfer functions and the digital NCF for broadband MASH SDMs. For the exemplary 2-1-1 MASH SDM used in this chapter, the requirements on the 1st - 3rd integrators' DC gain are higher than 40 dB, and the requirement on the 1st integrator's 2nd pole is higher than 30 GHz, without the proposed digital calibration technique in this chapter (shown in Figure 6.4). To achieve a DC gain of more than 40 dB and a 2nd pole of higher than 30 GHz for the 1st integrator leads to stringent requirement on the DC gain and GBW of its amplifier. An amplifier with complex architecture, e.g. multistage and multipath architecture, and high power consumption is needed which increases the design complexity and power consumption of the ADC [34]. The proposed digital calibration technique to combat these errors is shown in Section 6.5.

The last error source is the parameter variation (shown in Chapter 5.4 with Figure 5.10). Due to the device mismatch in the fabrication, the SDM parameters can deviate from their ideal values. Contrary to the RC spread, the parameter variation causes uncorrelated random errors on all SDM parameters. The calibration for the errors due to the parameter variation is out of the scope of this chapter. The MASH SDM architecture should be designed with enough robustness to accommodate the parameter variation. And the circuit design should guarantee that the parameter variation is within the tolerance.

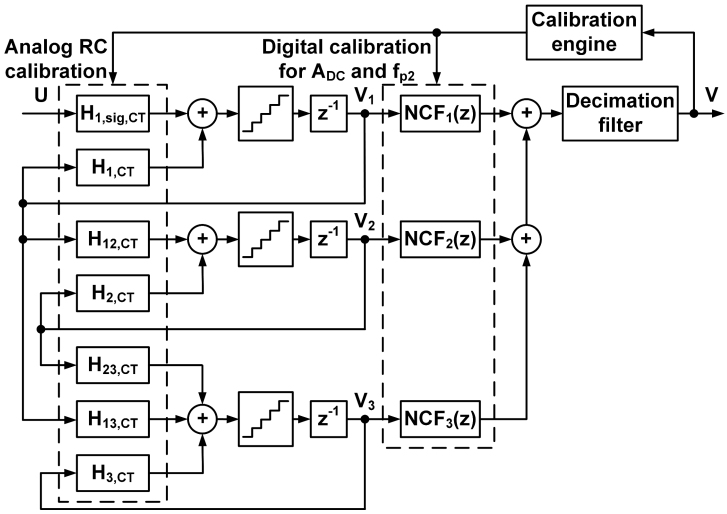


Figure 6.2: Block diagram of the proposed calibration technique

6.4 Analog RC calibration

The proposed calibration technique consists of two parts – analog calibration of the RC constants (UGBW of the integrators), and the digital calibration for the limited A_{DC} and f_{p2} by updating the NCF coefficients, as shown in Figure 6.2. The analog RC calibration is implemented similar as [73]. With no input signal, the variance of the decimation filter output is considered as the measurement of the in-band noise (IBN) [42]. With ideal NCFs, the capacitor banks in the RC integrator or the Gm-C integrator receive a code from the calibration engine. Assuming a common RC spread over the whole chip, the capacitor bank code can be swept to find a minimal value of the IBN. The minimum IBN indicates the correct capacitor bank code of the analog RC calibration.

6.5 Digital calibration algorithm

In this section, the proposed digital calibration algorithm for limited A_{DC} and f_{p2} is presented in detail, assuming pre-calibrated RC constants. Without loss of generality, a CT feedback 2-1-1 MASH $\Sigma\Delta$ ADC architecture is considered to substantiate the proposed calibration algorithm. The sampling frequency is chosen as $F_S = 8.4$ GS/s and OSR = 7, to achieve a signal BW = 600 MHz. Every loop uses 9-level quantization. The 1st integrator in the 1st loop is considered to be implemented as an RC integrator, while the remaining 3 integrators are implemented as Gm-C integrators.

6.5.1 Calculation of the correct digital NCFs

From the CT model of the loop filter with non-idealities, both the ILFs and the CLFs are derived. For the 2-1-1 MASH structure shown in Figure 6.2, in total 3 ILFs $H_{i,CT}$ and 3 CLFs $H_{ij,CT}$ are calculated. Here, $H_{i,CT}$ and $H_{ij,CT}$ contain both DAC pulse functions and the transfer functions of the CT loop filters.

Then, the impulse invariance transformation [36] is applied to calculate the effective DT noise transfer functions of every loop with the modelled loop filter non-idealities as (6.3) - (6.4). Without loss of generality, normalized sampling frequency $F_S = 1$ Hz is assumed.

$$H_{i,DT} = \mathcal{Z}\left\{\mathcal{L}^{-1}\{H_{i,CT}\}_{t=n}\right\} \tag{6.3}$$

$$NTF_i = \frac{1}{1 - z^{-1} \cdot H_{i,DT}} \tag{6.4}$$

Similarly, the effective transfer functions of the upper loops' quantization noise to the lower loops' output can be calculated as:

$$H_{ij,DT} = \mathcal{Z}\left\{\mathcal{L}^{-1}\{H_{ij,CT}\}_{t=n}\right\} \tag{6.5}$$

$$TF_{ij} = H_{ij,DT} \cdot z^{-1} \cdot NTF_j \tag{6.6}$$

Then, the correct digital NCFs which match the analog loop filters with the modelled non-idealities can be calculated as (6.7) - (6.9), such that the quantization noise of the 1st loop and the 2nd loop is completely cancelled in the final output. In (6.7), a_{12} and a_{23} are the designed inter-stage gains.

$$NCF_3 = \frac{NTF_1 \cdot NTF_2}{a_{12}a_{23}} \tag{6.7}$$

$$NCF_2 = -TF_{23} \cdot NCF_3 \tag{6.8}$$

$$NCF_1 = -TF_{13} \cdot NCF_3 \tag{6.9}$$

6.5.2 Calibration algorithm

The three calculated NCFs in Section 6.5.1 share the same denominator, which shows flat in-band magnitude with less than ±1 dB of gain. Thus the correction on the denominator can be ignored, without compromising performance. After calibration, the digital NCFs have the form of (6.10), in which only N_{12} – N_{15}, N_{22} – N_{25}, and N_{30} – N_{33} are non-zero. Three FIR filters of order 4 and tunable coefficients are required. Note that without calibration, three FIR filters of order 3, 4, 4, respectively, are already needed to implement the nominal NCFs. The extra hardware required by the proposed calibration is one extra order for one FIR filter and the tunability of the

FIR coefficients.

$$NCF_{i,cal} = \sum_{j=0}^{5} N_{ij} z^{-j} \tag{6.10}$$

Figure 6.3a shows the calculated NCF_1 coefficients versus different DC gain of the 1st integrator $A_{DC,1}$ in an otherwise ideal system. Figure 6.3b presents the difference between the calculated coefficients and the ideal coefficients, ΔN_{1j} (referred as the correction factors in this thesis), versus $A_{DC,1}$. ΔN_{1j} are linear functions of $A_{DC,1}^{-1}$ to the 1st order. It is similar for NCF_2 and NCF_3 coefficients. ΔN_{ij} versus the 2nd pole of the 1st integrator, and the DC gains of the 2nd and 3rd integrators shows similar dependence, by ignoring very small coefficients. This property can be summarized as (6.11), in which the inter-dependent part is ignored. In (6.11), $\alpha_{ij,A_{DC,k}}$ and $\alpha_{ij,f_{p12}}$ are the simulated coefficients of the linear functions.

$$\begin{aligned} N_{ij} &= N_{ij,nom} + \Delta N_{ij,A_{DC,1}} + \Delta N_{ij,f_{p12}} + \Delta N_{ij,A_{DC,2}} \\ &+ \Delta N_{ij,A_{DC,3}} \text{ , where } \Delta N_{ij,A_{DC,k}} \approx \alpha_{ij,A_{DC,k}} \cdot A_{DC,k}^{-1} \\ &\text{and } \Delta N_{ij,f_{p12}} \approx \alpha_{ij,f_{p12}} \cdot f_{p12}^{-1} \end{aligned} \tag{6.11}$$

Based on (6.11), a 4-dimensional calibration algorithm is proposed. For simplicity, the 1-dimensional calibration for $A_{DC,1}$ is explained in detail in the following, and the 4-dimensional calibration can be implemented similarly.

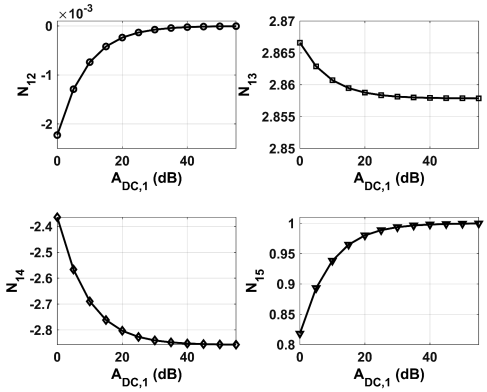
Initialization: The matrix of nominal FIR coefficients $[N_{ij,nom}]$ and the calculated correction factors for one initial guess $A_{DC,1,ini}$ $[\Delta N_{ij,A_{DC,1,ini}}]$ is stored.

Logarithmic scale binary search: With initial $step = 2^4 = 16$, $[\Delta N_{ij}] = [\Delta N_{ij,A_{DC,1,ini}}]$. The IBN is measured and compared for 3 settings of the NCF coefficients: (a) $[N_{ij,nom}]+[\Delta N_{ij}]$; (b) $[N_{ij,nom}]+[\Delta N_{ij}]\cdot step$; (c) $[N_{ij,nom}]+[\Delta N_{ij}]/step$. If the setting (b) (or (c)) leads to a lower IBN, $[\Delta N_{ij}] = [\Delta N_{ij}] \cdot step$ (or $[\Delta N_{ij}] = [\Delta N_{ij}]/step$); otherwise $step = \sqrt{step}$. Logarithmic scale binary search is finished until $step < 2$.

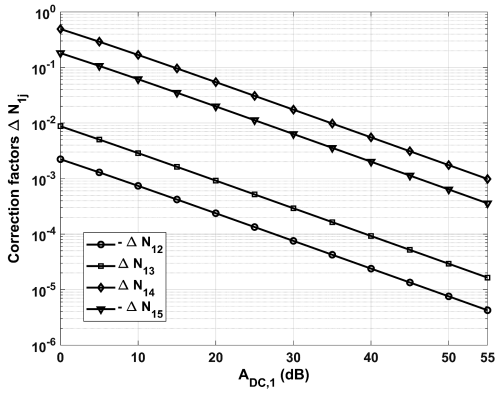
Linear scale binary search [72]: With initial $step = \frac{1}{2}$. The IBN is measured and compared for 3 settings of the NCF coefficients: (a) $[N_{ij,nom}]+[\Delta N_{ij}]$; (b) $[N_{ij,nom}]+[\Delta N_{ij}] \cdot (1 + step)$; (c) $[N_{ij,nom}] + [\Delta N_{ij}] \cdot (1 - step)$. If the setting (b) (or (c)) leads to a lower IBN, $[\Delta N_{ij}] = [\Delta N_{ij}] \cdot (1 + step)$ (or $[\Delta N_{ij}] = [\Delta N_{ij}] \cdot (1 - step)$); otherwise $step = step/2$. Linear scale binary search is finished until $step < step_{min}$. $[\Delta N_{ij,est}] = [\Delta N_{ij}]$.

The whole calibration algorithm requires only summations, bit shifts and comparisons. No multiplications are needed. Simulations show that the required estimation accuracy of the DC gains and the 2nd pole is within ± 10%, so the minimum step is $step_{min} = 5\%$. When the calibration is finished, the estimation of $A_{DC,1}$ can be calculated as (6.12), in which ΔN_{ij} can be any non-zero element in $[\Delta N_{ij}]$.

$$A_{DC,1,est} = A_{DC,1,ini} \cdot \frac{\Delta N_{ij,A_{DC,1,ini}}}{\Delta N_{ij,est}} \tag{6.12}$$



(a)



(b)

Figure 6.3: (a) $NCF_{1,cal}$ coefficients N_{1j} and (b) Correction factors ΔN_{1j} versus 1st integrator DC gain $A_{DC,1}$.

6.6 Simulation results

To verify the effectiveness of the proposed calibration algorithm, the SNDR before and after calibration versus the DC gains of the integrators and the 2nd pole of the 1st integrator are simulated separately in Matlab/Simulink, as shown in Figure 6.4. Only one DC gain or 2nd pole parameter is swept and the SDM is otherwise ideal in every figure. Firstly, the proposed calibration is run with no input signal, and the correct NCF coefficients are found and fixed. The digital calibration is run with no input signal since in this case the noise leakage due to the mismatch between the digital NCF and the analog transfer function is the dominant error source in the IBN before calibration. Then, a sinusoid signal with -3 dBFS amplitude whose

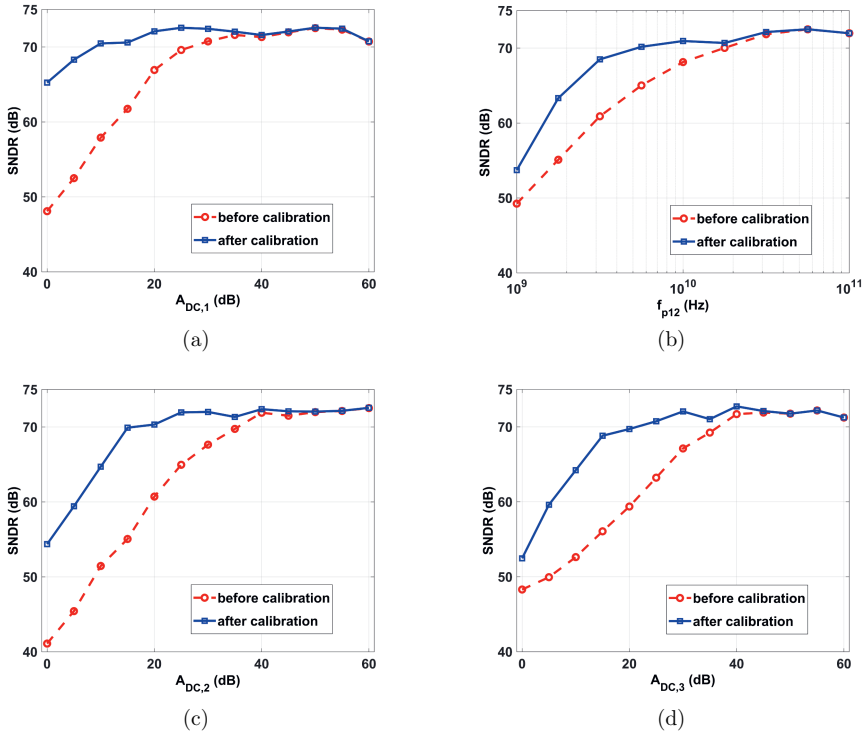


Figure 6.4: SNDR before and after proposed calibration: (a) versus 1st integrator DC gain; (b) versus 1st integrator 2nd pole; (c) versus 2nd integrator DC gain; (d) versus 3rd integrator DC gain.

frequency is at about 1/3 of the signal BW is used as the input signal to show the SNDR improvement, so that the 3rd order harmonic distortion is taken into account. When the analog loop filters are non-ideal, the quantizers can be slightly overloaded with close to full scale input. With the proposed calibration, NCFs and analog loop filters are matched, and the HD3 tones originated from the 1st and the 2nd quantizers are eliminated. Figure 6.4a, 6.4c, and 6.4d show that the DC gain requirements (for SNDR $>$ 70 dB) is relaxed by about 15 dB for the 1st – 3rd integrators with the proposed calibration. As the error due to the limited DC gain of the 4th integrator is already 3rd order shaped, its DC gain requirement is very low. With the proposed calibration, the DC gain requirements of 1st – 4th integrators are 25 dB, 25 dB, 30 dB, 20 dB, respectively. Figure 6.4b shows that the 2nd pole requirement of the 1st integrator is relaxed from higher than 17.8 GHz to 5.6 GHz.

To verify the convergence and robustness of the proposed 4-dimensional calibration, 200 independent simulations are done with full scale input amplitude in Matlab/Simulink. The DC gains of the 1st – 4th integrators are independently uniformly

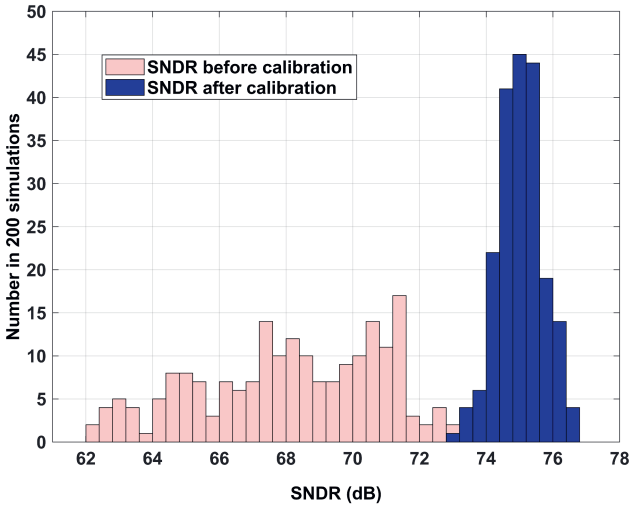


Figure 6.5: Histogram of the SNDR before and after proposed calibration: 200 independent simulations

distributed in the range of (25, 39) dB, (25, 39) dB, (30, 44) dB and (20, 34) dB, respectively. The 2nd pole of the 1st integrator is independently uniformly distributed in the range of (7, 35) GHz. Figure 6.4 shows that when the DC gain and the 2nd pole are in these ranges, they cause a significant degradation on SNDR without calibration. With the proposed calibration, the SNDR is restored close to that of the ideal SDM. Figure 6.5 shows the histogram of the simulated SNDR before and after the proposed calibration. Before calibration, the mean value of the SNDR is 68.1 dB with standard deviation $\sigma = 2.7$ dB, which is improved to 75 dB with $\sigma = 0.7$ dB after calibration. The mean value of the calibration time is 166 IBN measurements with $\sigma = 29$ IBN measurements. $2^{13} = 8192$ samples are used in every IBN measurement. It shows that the calibration algorithm always converges with large SNDR improvement. For all simulations in Figure 6.5, the IBN converges to the global minimum or to a local minimum, very close to the global minimum.

The proposed digital calibration can assist the analog calibration of the RC spread error. To verify that, the SNDR before and after digital calibration with full scale input amplitude versus different RC spread errors are simulated in Matlab/Simulink and presented in Figure 6.6. The integrator non-idealities are $A_{DC,1} = 35$ dB, $f_{p12} = 27$ GHz, $A_{DC,2} = 25.1$ dB, $A_{DC,3} = 38.6$ dB, and $A_{DC,4} = 28.1$ dB, which is one randomly generated setting from the simulation of Figure 6.5. The dashed red line shows that without the digital calibration, when the RC spread error is calibrated by analog tuning (Chapter 6.4) to about ±5%, the SNDR is limited by the limited A_{DC} and f_{p2}, and it is difficult to select the best code for the capacitor bank. For every

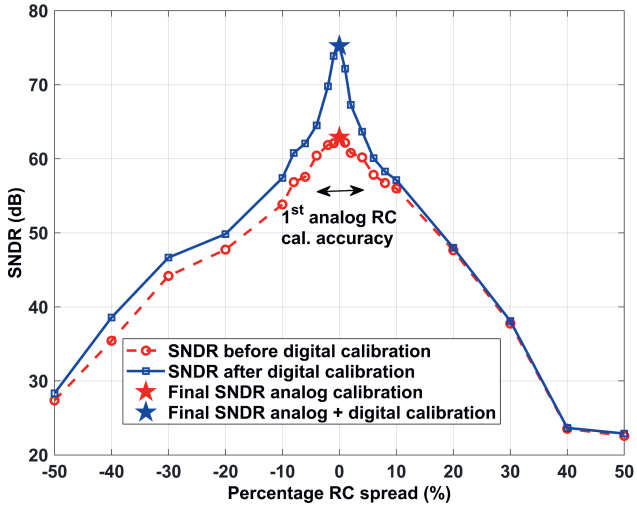


Figure 6.6: SNDR vs. RC spread before and after proposed calibration

RC spread value in Figure 6.6, the proposed digital calibration is applied. Since the digital calibration shows optimal performance for the pre-calibrated RC constants, it can clearly indicate the correct code for the analog calibration. Thanks to the digital calibration, the accuracy of the analog RC calibration is improved to be better than $\pm 1\%$. After the RC spread error is calibrated, the digital calibration improves the SNDR by 12.4 dB.

The proposed calibration method is further verified by the simulation of a transistor-level schematic of the 2-1-1 MASH loop filter in Cadence Virtuoso. The loop filter is designed in a 40 nm CMOS technology with inverter-based operational transconductance amplifiers (OTAs). The simulated DC gains of the 1st – 4th integrators are 27.9 dB, 31.3 dB, 33.9 dB, 32.2 dB, respectively, and the simulated 2nd pole of the 1st integrator is 12.3 GHz. The simulated FFT (8192 samples) before and after the proposed calibration with -3 dBFS input is shown in Figure 6.7. The expected quantization noise level is calculated with the synthesized ideal NTF. Before calibration, the IBN is -70.5 dBFS, and SNDR = 65.8 dB. After calibration, the IBN is improved to -75.2 dBFS, and SNDR is improved to 68.7 dB. The flat noise floor at low frequency (below 100 MHz) after calibration is limited by the DC gain of the integrators, which is not limiting the IBN. In another simulation with 0 dBFS input signal, the IBN is improved from -67.9 dBFS to -75.5 dBFS, very close to the IBN of the ideal SDM -76.5 dBFS.

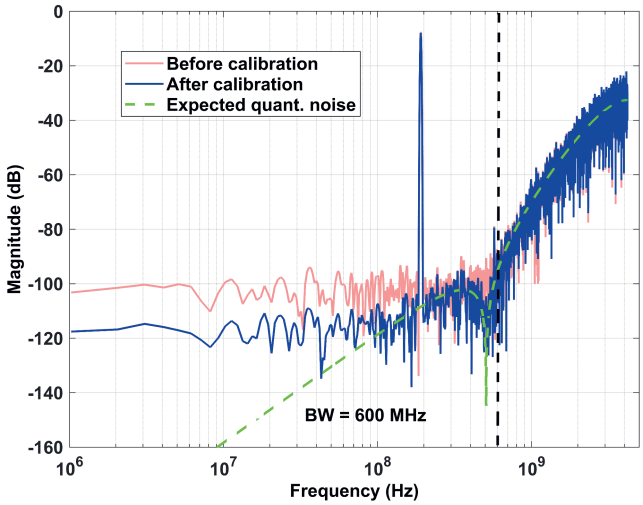


Figure 6.7: Simulated FFT with transistor-level model of the loop filter before and after proposed calibration

6.7 Conclusions

A calibration consisting of an analog calibration of the integrators' UGBW (RC value) and a novel digital calibration of the errors due to the integrators' limited DC gain and 2nd pole for CT MASH ΣΔ ADCs is proposed. It has very low calculation complexity, short calibration time, and requires simple hardware. Thus, it is suitable for low cost implementation. Extensive simulations show its robustness. For an exemplary 9-level 2-1-1 MASH architecture with BW of 600 MHz and SQNR of 75 dB, the proposed method relaxes the DC gain requirements of the 1st – 3rd integrators by about 15 dB, and relaxes the 2nd pole requirement of the 1st integrator from higher than 17.8 GHz to 5.6 GHz. Transistor level simulations demonstrate 7.6 dB improvement of the IBN. All these properties and results show its potential for power efficient GHz-range ADC applications.

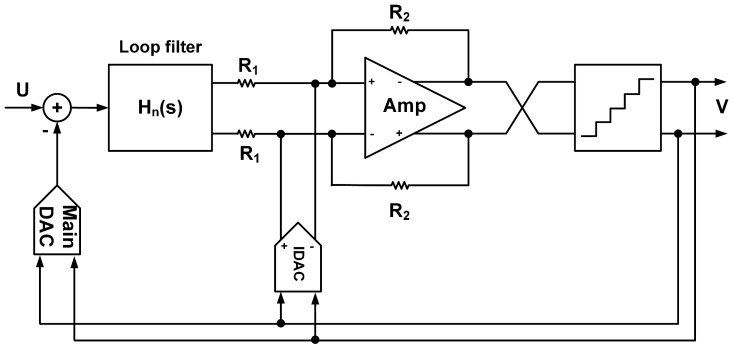
Chapter 7

High-speed ELD compensation

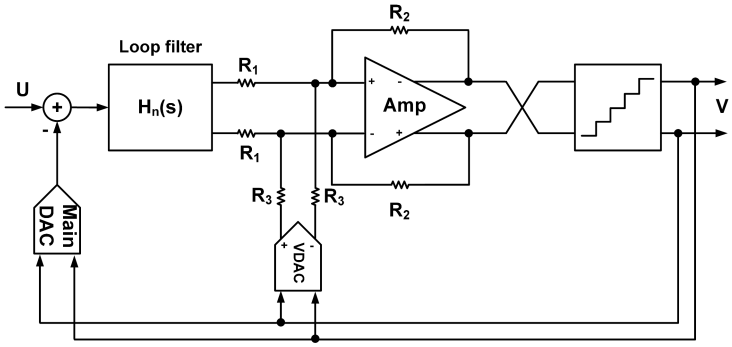
This chapter discusses high-speed ELD compensation techniques for broadband CT $\Sigma\Delta$ ADCs. First, the state-of-the-art high-speed ELD compensation techniques are studied and classified. The parasitic delay in the ELD loop itself e.g. due to the poles of the summing amplifier and pre-amplifier limits the maximal sampling rate of the $\Sigma\Delta$ ADCs, which is the problem that this chapter would like to solve. A novel current-mode multi-path ELD compensation technique is proposed in Section 7.2. This section is based on our publication [81] and patent [82]. Section 7.3 further employs cross-coupled feedforward capacitors to compensate the ELD settling delay caused by the parasitic capacitance on the summation nodes, and propose a generic summation node at the quantizer input. The "generic" here refers to the summation of an arbitrary signal required by the system optimization, which can be the SDM input, or an internal node of the loop filter, or an input from a proceeding stage in a MASH structure. In the end, conclusions are drawn.

7.1 Overview for high-speed ELD compensation techniques

Chapter 4.5 has introduced the concept of the excess loop delay and the ELD compensation. Chapter 5 has shown the synthesis of a broadband CT 2-1-1 MASH SDM architecture with 1 T_S ELD compensated in every stage. The ELD feedback information needs to settle before the next sampling moment of the quantizer, otherwise the resolution and stability of the SDMs can be negatively impacted. This section presents an overview on the state-of-the-art system-level and circuit-level implementations of high-speed ELD compensation techniques based on a literature study. Firstly, a conventional implementation of the ELD compensation with a dedicated summation amplifier is presented. Alternatively, the ELD compensation path can be implemented together with the last stage of the loop filter – either an RC integrator or a Gm-C integrator. Last but not least, the ELD compensation can be implemented with passive



(a)



(b)

Figure 7.1: Block diagram of an exemplary CT ΣΔ ADC with ELD compensation with a dedicated summation amplifier: (a) with a current-steering DAC (b) with a voltage DAC.

summation, either in voltage domain or in current domain. Digital ELD compensation techniques, and the ELD compensation techniques for VCO-based quantizers and TDC-based quantizers are out of the scope of this thesis [27, 51, 77, 83].

7.1.1 ELD compensation with dedicated summation amplifier

One conventional implementation of the summation of the loop filter output and the ELD DAC output is using a dedicated summation amplifier. It is called active summation as well. Two slightly different implementations are shown in Figure 7.1. In Figure 7.1a, a current steering DAC (IDAC) is used as the ELD compensation DAC. The loop filter output voltage is converted into the current domain by the resistors R_1, then summed with the IDAC output current. A slightly different implementation

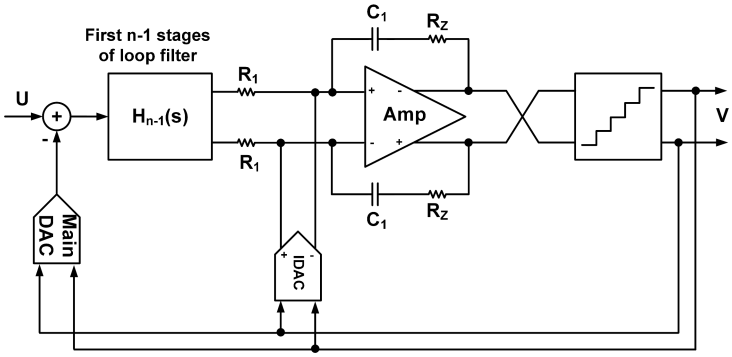


Figure 7.2: Block diagram of an exemplary CT ΣΔ ADC with ELD compensation with a RC integrator and a resistor R_z to generate a zero.

is shown in Figure 7.1b. A voltage DAC is used as the ELD compensation DAC in Figure 7.1b. In both Figure 7.1a and 7.1b, the summation amplifier output node contains the summation result of the loop filter output and the ELD DAC output. As the implementations of Figure 7.1a and 7.1b are very similar, in the following discussion, only one of these two alternative implementations is explicitly shown.

The approach of using a dedicated summation amplifier has advantages and disadvantages. The advantage is that the output swing of the summation amplifier can be chosen relatively large, which relaxes the offset requirement of the quantizer when a multi-bit quantizer is used. The disadvantage is that it requires a dedicated amplifier. And it requires a very high GBW from this amplifier, to achieve a far parasitic pole at the output of the amplifier. Thus, this summation amplifier typically has high power consumption.

7.1.2 ELD compensation with RC integrator with zero resistor

An alternative approach to implement the ELD compensation path is to build up a zero-order path around the last integrator. Figure 7.2 shows the 1st case – the last stage of the integrator is implemented as an RC integrator, and the zero-order path is achieved by adding a resistor R_z in series with the integration capacitor C_1. In this case, by choosing a proper value for R_z, the direct feedback path around the quantizer is achieved. This ELD compensation approach has been demonstrated in [63].

This approach has advantages and disadvantages. The advantage is that it reuses the amplifier of the integrator to build the ELD compensation path, and hence it saves the power consumption of an additional amplifier compared to Figure 7.1. The

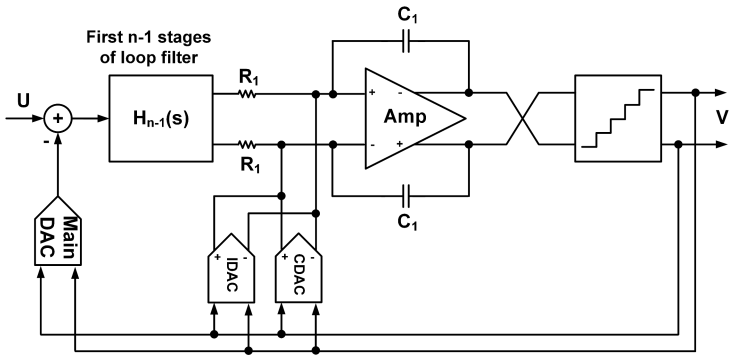


Figure 7.3: Block diagram of an exemplary CT ΣΔ ADC with ELD compensation with a RC integrator and a capacitive DAC.

disadvantage is that this approach imposes a very high requirement on the GBW of the amplifier.

7.1.3 ELD compensation with RC integrator and capacitive DAC

Figure 7.3 shows an alternative approach to Figure 7.2. Instead of using R_z, it adds a capacitive DAC (CDAC) to the virtual ground node of the RC integrator, in parallel with the existing current-steering DAC. By doing that, a C-C path with the CDAC and the integrator capacitor C_1 is formed, which is a zero-order path. This zero-order path is the ELD compensation path around the quantizer. This ELD compensation approach has been demonstrated in [16].

This approach has pros and cons. Similar as in Figure 7.2, it reuses the amplifier of the RC integrator, and hence doesn't need any additional amplifier. The C-C path formed by the CDAC and C_1 is able to implement a wide range for the ELD compensation coefficient. However, it has two disadvantages. Firstly, the amplifier is in the ELD compensation loop, and any parasitic pole at the output of the amplifier is in the ELD compensation loop. Thus it gives stringent GBW requirement on the amplifier. Secondly, the capacitive ratio between the capacitance used in the CDAC and C_1 is determined by the ELD feedback coefficient. CDAC adds to the load for the quantizer, which increases its power consumption.

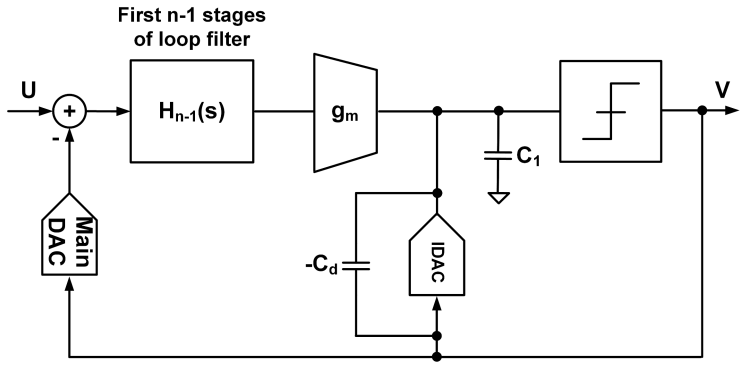


Figure 7.4: Block diagram of an exemplary CT ΣΔ ADC with ELD compensation with a Gm-C integrator and a capacitor $-C_d$.

7.1.4 ELD compensation with Gm-C integrator and capacitive DAC

The last stage of the integrator can be a Gm-C integrator as well. With this Gm-C integrator, there are two approaches to implement the ELD compensation loop. The 1st approach is shown in Figure 7.4. The current-steering DAC is the feedback DAC to the input of the last integrator. The capacitor $-C_d$ is used for the ELD compensation [84]. $-C_d$ is interpreted as two capacitors C_d between V_{in}^+ and V_{out}^-, and between V_{in}^- and V_{out}^+ in a differential implementation. The capacitor $-C_d$ with the integration capacitor C_1 forms a C-C path, which is a direct feedback path around the quantizer. This ELD compensation approach has been demonstrated in a 1-bit CT SDM in [84].

7.1.5 ELD compensation with Gm-C integrator, current-steering DAC and digital differentiator

An alternative approach to Figure 7.4 is to add a digital differentiator at the input of the current-steering DAC, as shown in Figure 7.5. In this approach, the quantizer output is firstly differentiated by the digital differentiator $(1 - z^{-0.5})$. After that, this differentiated quantizer output is converted to the current domain by the IDAC. The DAC current is summed with the amplifier (g_m) output current. And the summed current is integrated by the capacitor C_1. So the quantizer output is firstly differentiated by the digital differentiator, and later integrated by the capacitor. An ELD compensation loop is thus built. This ELD compensation approach has been demonstrated in [30].

This approach has pros and cons. The advantage is that the input parasitic capacitance of the quantizer can be considered as (part of) the integration capacitor C_1.

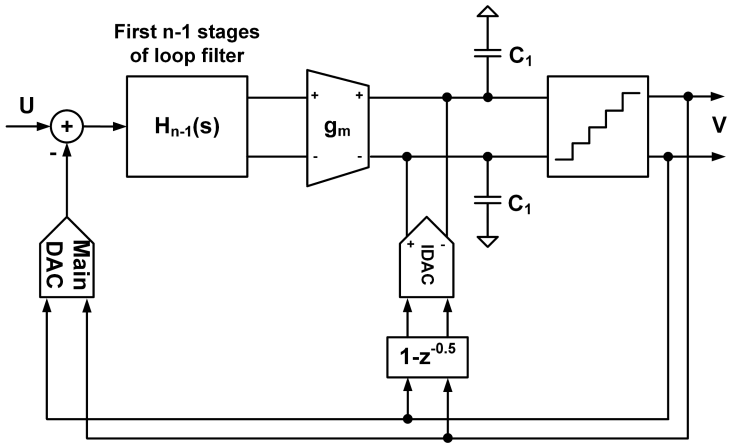


Figure 7.5: Block diagram of an exemplary CT ΣΔ ADC with ELD compensation with a Gm-C integrator, a current-steering DAC and a digital differentiator.

Thus, no parasitic pole is added at the summation node output. The disadvantage is that to implement the digital differentiator $(1 - z^{-0.5})$, half clock period delay $(z^{-0.5})$ is needed. Thus, the available time for the regeneration of the comparator is limited.

7.1.6 ELD compensation as passive summation in voltage domain with voltage DAC

Opposite to the active summation (Figure 7.1), passive summation is possible. Figure 7.6 shows the block diagram of an exemplary CT ΣΔ ADC with ELD compensation with passive summation in the voltage domain. The ELD DAC is implemented as a voltage DAC. By the RC network R_1 - R_3 and C_1 - C_3, the loop filter output and the ELD DAC output are summed at the quantizer input node. This ELD compensation approach has been demonstrated in [85].

This approach has pros and cons. The parasitic capacitance can be considered as (part of) C_3. Thus, no parasitic pole is added at the summation node output and the passive voltage summation can achieve very large bandwidth. Another advantage is that the passive summation consumes no power. It has a few disadvantages: (1) The passive summation has no gain. The signal swing at the summation output node is typically small, which is related to the gain from the loop filter output to the ELD summation node and the coefficient of the ELD DAC (e.g. p_1 and d_1 in Figure 5.6), and the loop filter output swing. In the scenario with multi-bit quantizer, a small input swing is not preferable because it means more stringent quantization gain and offset requirement for the quantizer. (2) The parasitic pole caused by C_2 and the impedance of the ELD DAC (VDAC) limits the maximal speed of the ELD loop. (3)

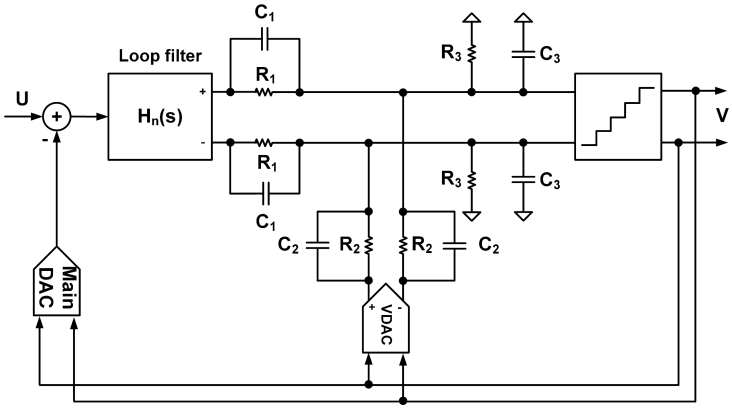


Figure 7.6: Block diagram of an exemplary CT ΣΔ ADC with ELD compensation with passive summation in voltage domain.

R_1 and C_1 add load to the loop filter, which increases its power consumption.

7.1.7 ELD compensation as passive summation in current domain with current-steering DAC

Passive summation can be implemented in the current domain as well. Figure 7.7a shows an exemplary CT ΣΔ ADC with ELD compensation with passive summation in current domain with a 1-bit quantizer. The loop filter output voltage is converted into current by a voltage-to-current (V/I) converter. The ELD DAC is implemented as a current steering DAC. The IDAC output current and Gm cell output current are summed in the current domain. The summation result is a current, which is taken as the input current by the 1-bit quantizer (comparator). This ELD compensation approach for SDMs with 1-bit quantization has been demonstrated in [86].

A passive ELD summation in the current domain has been demonstrated for a multi-bit CT SDM in [87]. Its block diagram is shown in Figure 7.7b. Similar as the 1-bit case, the loop filter output is converted to a current signal by a V/I converter. This current signal is summed with the ELD DAC output current signal in the current domain. The resulting current signal is converted into a voltage signal by a resistive ladder, and thus the reference information is included.

The passive summation in the current domain can achieve high bandwidth. However, the state-of-the-art approach shown in Figure 7.7b has two limitations. Firstly, the V/I and I/V conversions required in this approach add substantial delay, which is not suitable for the fast feedback loop in the multi-GHz sampling rate scenarios considered in this thesis. Another drawback is that the summation node drives 15 1-bit comparators in [87], which results in a large parasitic capacitance at the summation

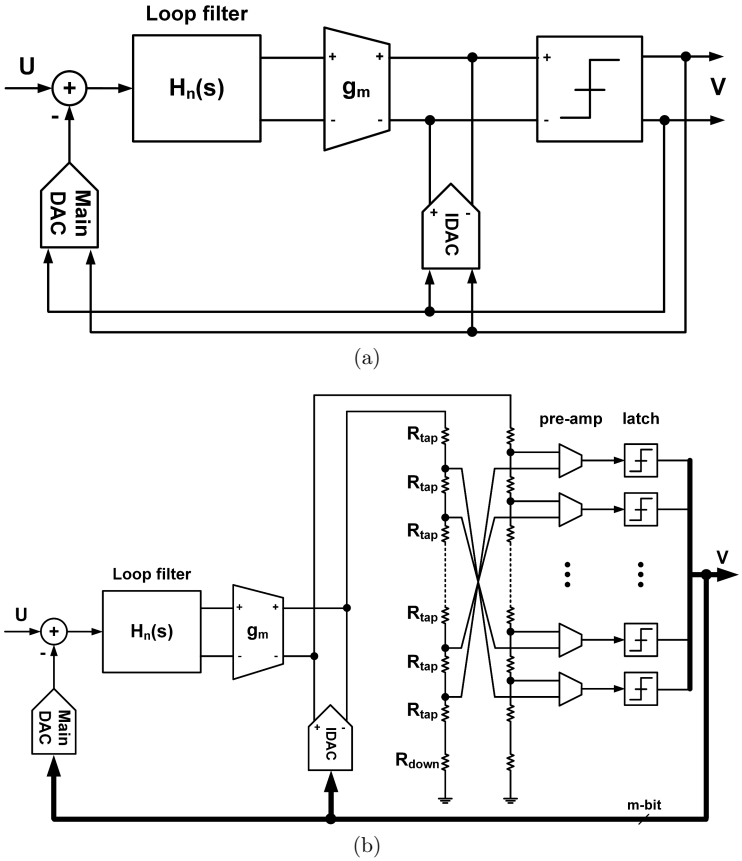


Figure 7.7: Block diagram of exemplary state-of-the-art CT ΣΔ ADCs with ELD compensation with passive summation in current domain: (a) with 1-bit quantizer (b) with multi-bit quantizer.

output node. It generates a pole and adds extra delay in the fast feedback loop. To overcome these limitations, a novel current-mode multi-path ELD compensation technique is proposed in the next section.

7.2 Current-mode multi-path ELD compensation

This section proposes both system-level and circuit-level solutions of a current-mode multi-path ELD compensation technique for CT ΣΔ ADCs with multi-bit quantization and several GHz sampling rate. Thanks to the proposed solutions, the amplifier of the loop filter is not in the fast feedback loop; the delay of the pre-amplifier of

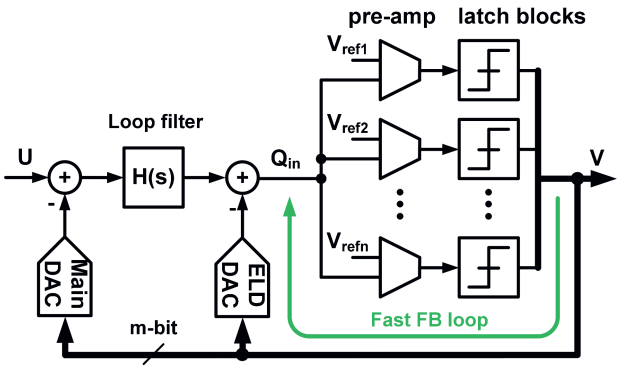


Figure 7.8: Conventional high speed SDM system architecture with multi-bit quantization and ELD compensation

the comparator is removed; and the effective regeneration time of the comparator latch is maximized. The proposed novelties enable CT ΣΔ ADCs with wide signal bandwidth and improved power efficiency. Extensive transistor-level simulations demonstrate their effectiveness and robustness. This section validates the proposed methods by transistor level design and simulations of an 8.4 GHz MASH ΣΔ ADC achieving an SQNR of 71 dB in a signal band of 600 MHz. This shows that the proposed solutions enable power-efficient multi-GHz ΣΔ ADC applications.

7.2.1 Introduction

The previous section has shown an overview for the high-speed ELD compensation techniques for CT ΣΔ ADCs, including ADCs with multi-bit quantization. Their limitations have been discussed, for ADC applications with multi-GHz sampling rate considered in this thesis. The conventional system architectures of high speed SDMs with multi-bit quantization and ELD compensation [16, 30, 63, 87] can be generalized as shown in Figure 7.8. The loop filter can be in either feedforward or feedback structure. Only one common fast feedback loop is used for the ELD compensation. In [16, 30, 63] the comparator input signal (Q_{in}) is compared to a series of reference voltages (V_{ref}) in the pre-amplifiers. In [87] pre-amplifiers are used as well. Besides their limitations discussed in the last section, in the scenario of a multi-GHz sampling frequency, the conventional system architecture has another problem – the pre-amplifiers have to be optimized for low delay, which limits the gain they can offer, while consuming a lot of power.

In this section, a novel current-mode multi-path ELD compensation scheme is proposed for very high speed CT ΣΔ ADCs with multi-bit quantization. The scheme is introduced via both system-level and circuit-level analysis, design and transistor-level simulations of an exemplary multi-GHz sampling CT ΣΔ ADC. The ELD DAC out-

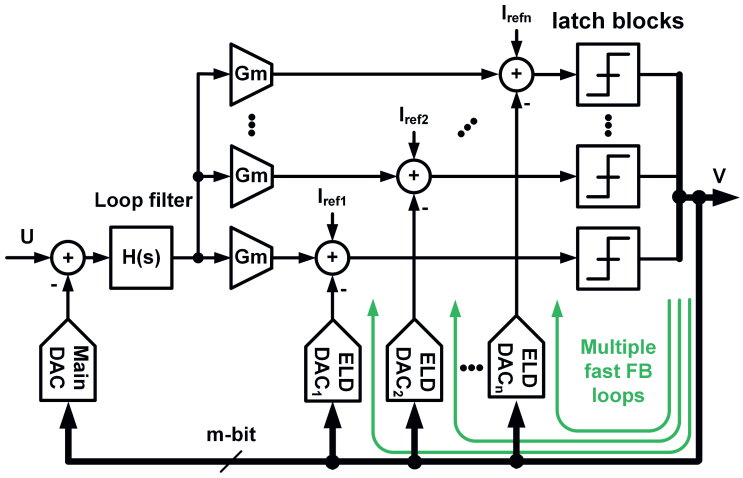


Figure 7.9: Proposed high speed SDM system architecture with multi-bit quantization and current-mode multi-path ELD compensation

put and the loop filter output are summed in the current domain. The summation node is duplicated, which allows combining the reference information in the same nodes. The loop filter amplifier is not in the fast feedback loop. The delay of the pre-amplifier is removed, and the effective regeneration time of the comparator latch is maximized for an optimal gain. Section 7.2.2 describes the proposed system architecture. Section 7.2.3 presents the circuit implementation. Transistor-level simulation results are shown in section 7.2.4. Finally, conclusions are drawn in section 7.2.5.

7.2.2 System architecture

To exclude the loop filter amplifier from the fast feedback loop, and to remove the pre-amplifier delay, a high speed SDM system architecture with multi-bit quantization and current-mode multi-path ELD compensation is proposed, as shown in Figure 7.9. Similar to [87], with a V/I converter (Gm cell), the loop filter output is converted into a current signal, and then summed with the ELD DAC output current. The summation result is the comparator input signal (Q_{in}) in the current domain. The Q_{in} current signal should drive a multi-bit comparator, which requires duplicating the Q_{in} signal. Usually, this duplication can be implemented in two ways. The first way is to convert the Q_{in} current signal back to the voltage domain [87], which is not suitable for multi-GHz sampling scenarios. The second way is to duplicate the Q_{in} current signal with a current mirror. However, the BW requirement for the current mirror is very high, and it adds some delay.

The proposed solution (Figure 7.9) is to duplicate the summation node. The Gm

cell and the ELD DAC need to be duplicated as well. Instead of comparing the Q_{in} voltage signal with reference voltage signals V_{refi} in the pre-amplifiers (Figure 7.8), the corresponding reference current signals I_{refi} are added in the same summation nodes. Thus, the pre-amplifiers are removed from the system. The resulting current signal directly drives a comparator latch. In the SDM with $(n+1)$-level quantization shown in Figure 7.9, n Gm cells and n ELD DACs are required, where every ELD DAC is a $(n+1)$-level DAC.

The novelty and advantages of the proposed system-level solution with respect to the state-of-the-art approaches [30, 16, 63, 87] are summarized as follows. Firstly, the state-of-the-art multi-bit SDMs with ELD compensation have only one fast feedback loop. The proposed system is the first ELD compensation based on multiple fast feedback loops. Compared with [30], the delay of the digital differentiator is removed from the fast feedback loop. Compared with [16] and [63], the loop filter amplifier is not in the fast feedback loop. Compared with [87], the delay of I/V conversion is removed. Moreover, the delay of the pre-amplifier is removed, and the effective regeneration time of the comparator latch is maximized for an improved quantization gain. Last, in Figure 7.8 the summation output Q_{in} needs to drive multiple pre-amplifiers. It implies that a large parasitic capacitance is on the node Q_{in}, which generates a pole and adds delay in the fast feedback loop. In Figure 7.9, the loop filter output drives multiple Gm cells. The parasitic capacitance on the loop filter output node generates a pole, but this pole is out of the fast feedback loops. Generally, the outer feedback loop is less sensitive to the extra delay than the fast feedback loops. A concern of the proposed system is that the number of the ELD DACs is increased, which need to be driven by the quantizer output V. Thus, the input capacitance of the ELD DACs should be minimized in the circuit design.

7.2.3 Circuit implementation

A transistor-level implementation of the proposed current-mode multi-path ELD compensation in a multi-bit SDM is shown in Figure 7.10. A Gm cell, an ELD DAC, the reference current, a latch block, the S&H circuit and buffers compose a slice of the ELD-compensated quantizer. The Gm cell is implemented as a source degenerated PMOS transconductance amplifier, which is composed of current sources I_s, a resistor R_s, a capacitor C_s, and thin-oxide PMOS transistors M_1, M_2. Source degeneration is employed to improve the linearity of the Gm cell for a large input swing of ± 250 mV. Capacitor C_s is added between the sources of M_1, M_2 to generate a zero in the transfer function of the V/I converter, and to compensate its delay. The bandwidth of the Gm cell affects the stability of the outer feedback loop, but not the fast feedback loop. The ELD DAC is implemented as a current steering DAC. NMOS switches M_3, M_4 and the current source $I_{dac,u}$ compose a unit ELD DAC. NMOS transistors M_5, M_6 and the current source $I_{ref,u}$ construct a reference current unit. For $(n+1)$-level quantization, n reference levels need to be created, and thus $(n-1)$ reference current units are required for every slice. The complementary Sp[1]/Sn[1] - Sp[$n-1$]/Sn[$n-1$]

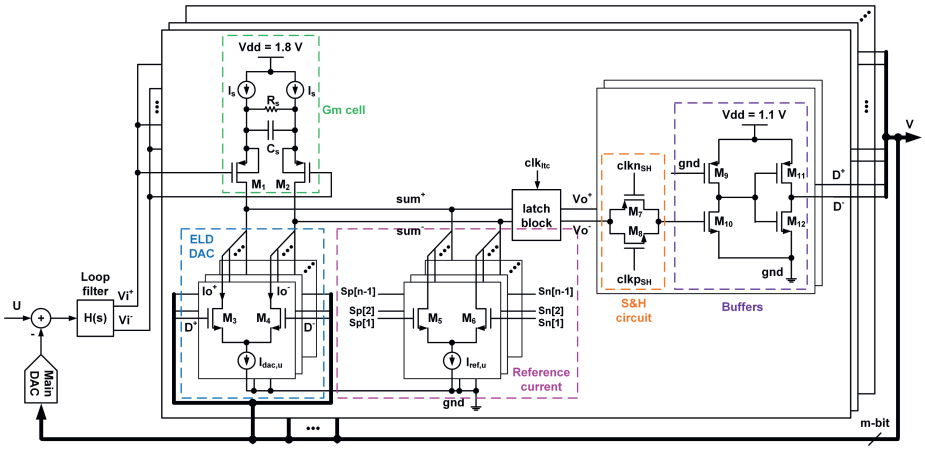


Figure 7.10: Proposed circuits of the SDM with multi-bit quantization and current-mode multi-path ELD compensation

can be configured to either Vdd (1.1 V) or gnd, which define the reference level of the slice. Among different slices, the proposed reference current circuits have the same common-mode current, and only their differential current is different. This property ensures that the circuits in different slices are working in the same common-mode condition.

After the latch block, a transmission gate (M_7, M_8) with complementary sampling clocks ($clkp_{SH}$ and $clkn_{SH}$) is employed to sample the latch output in the end of the latch's regeneration phase, and to hold it on its output capacitance. Two buffers are inserted between the sampled latch output and the input of the ELD DACs. The choice of the number of buffers is a trade-off between minimizing the load capacitance of the latch, and reducing the delay of the buffers. The 1st buffer (M_9, M_{10}) is an NMOS buffer with PMOS load, while the 2nd buffer (M_{11}, M_{12}) is a CMOS buffer. The NMOS buffer has lower input capacitance than the CMOS buffer, but it consumes more power. The CMOS buffer offers rail-to-rail driving ability. For the $(n+1)$-level quantization, one sampled latch output node should drive n unit ELD DACs after two buffers.

7.2.4 Simulation results

Without loss of generality, a CT feedback 2-1-1 MASH ΣΔ ADC with 3-bit quantization in every loop is considered to substantiate the proposed technique [79]. The sampling frequency is $F_S = 8.4$ GHz and the oversampling ratio is 7, to achieve a signal BW of 600 MHz. The proposed current-mode multi-path ELD-compensated 3-bit quantizers and the 2-1-1 MASH loop filter are designed at transistor-level in a 40 nm CMOS technology. The main DACs (all the other feedback DACs except for

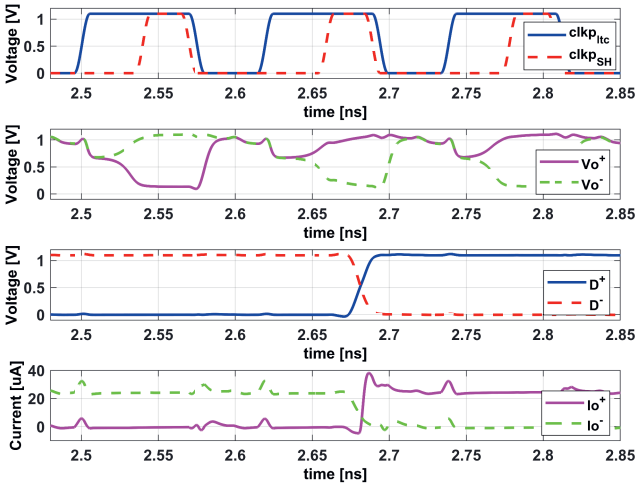


Figure 7.11: Clock timing diagram and signal behavior of the proposed circuits

the ELD DACs) are modelled in Verilog-A, including the extra load for the quantizers caused by the main DACs.

Figure 8.7 shows the clock diagram and the typical behavior of some important signals from the schematic simulation. When the latch clock signal clkp_{ltc} is high, the comparator latch is in the regeneration phase. When it is low, the latch is reset, and the summation result of loop filter output, ELD DAC output, and reference current is transferred to the latch as the initial condition of the next regeneration. The 2nd row depicts the latch differential output signal. At the end of the regeneration phase, the sampling clock signal clkp_{SH} becomes high, and the latch output is sampled. clkp_{SH} should become low before resetting the latch. The 3rd and 4th rows show the input voltage and the output current of a unit ELD DAC, respectively. Since the total delay of the fast feedback loop should be less than 1 T_S (119 ps), the ELD DAC output current must settle before the starting of the next regeneration. Moreover, the total delay of the current summation and the connection circuit between the summation node and the latch must be very short, such that the ELD feedback information reaches the latch before the start of the next regeneration. In other words, at the starting moment of the next regeneration, which is the sampling moment of the quantizer, the ELD feedback information of the previous sample must already change the latch initial condition, and this change must be settled. In Figure 8.7, the ELD DAC output current is settled more than 40 ps before the next positive clock edge of clkp_{ltc}. It indicates that the total delay of the ELD feedback path is not limiting the maximal sampling rate. The duty cycle of the latch clock clkp_{ltc} is set to 62%, which maximizes the regeneration time of the latch. In this design, the

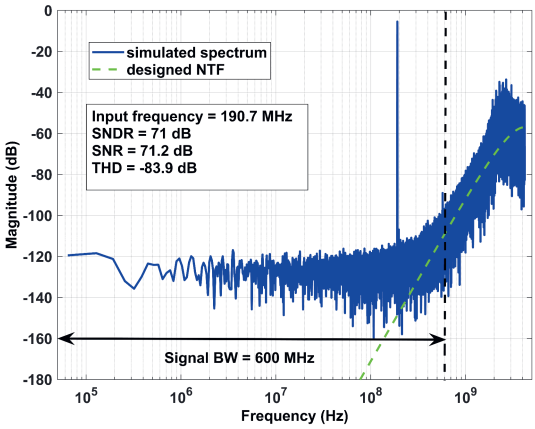


Figure 7.12: Simulated output spectrum of a 2-1-1 MASH ΣΔ modulator with the proposed system and circuits

maximal regeneration time of the latch is limited by the reset time and the time to acquire the next initial condition.

To verify the quantization gain of the transistor-level model of the proposed current-mode ELD-compensated 3-bit quantizers, the aforementioned 2-1-1 MASH ΣΔ ADC model was simulated for 134400 samples (16 us). In this model, the main DACs were modelled in Verilog-A such that if their differential input voltage is less than 316 mV, the unit DAC output cannot reach its full scale. It models 10 dB quantization gain of the main DAC switches, which is a pessimistic assumption. The transistor layout parasitic model was included in the simulation. Extra capacitance (20% of the total parasitic capacitance of that node) was added at the latch output nodes to model the increased parasitic capacitance because of the routing. Figure 8.8 depicts the simulated output spectrum (2^{17} samples) with -1.4 dBFS input signal. The simulated SQNR is 71 dB for BW = 600 MHz. Within the simulated 134400 samples of the main DAC output, no metastability error is observed.

The transistor-level simulations demonstrate the power efficiency of the proposed technique. The simulated power consumption of the ELD-compensated 3-bit quantizer in the 1st loop is 27.3 mW (3.9 mW per 1-bit quantization), including the Gm cells, ELD DACs, reference currents, latches, samplers and buffers. Figure 7.13 shows the simulated power breakdown of the ELD-compensated quantizer, in which "connection" indicates the power consumed by the connection circuit between the summation nodes and the latch blocks. 71% of the total power is used by the latches and the buffers, which provide the required quantization gain. The Gm cells, ELD DACs and reference currents only consume 22% of the power. Since the loop filter amplifier is not in the fast feedback loop, its GBW requirement is much relaxed. Inverter-based operational transconductance amplifiers (OTAs) were designed. Simulations show

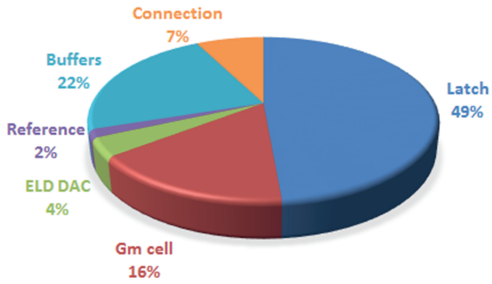


Figure 7.13: Simulated power consumption breakdown of the quantizer with ELD compensation

that the GBW of the loop filter amplifier is 14.3 GHz, and its power consumption is 8.2 mW.

In a state-of-the-art ELD-compensated multi-bit ΣΔ ADC with similar BW (465 MHz), F_S (8 GHz) and SNDR (67 dB) in 28 nm CMOS technology, the power consumption of the quantizer per 1-bit quantization is 5.8 mW [16]. The loop filter amplifier in the fast feedback loop consumes 135 mW, and its GBW is about 63 GHz. Compared to this state-of-the-art [16], our proposed technique relaxes the GBW requirement of the loop filter amplifier by a factor of 4.4, since it is moved out from the fast feedback loop. Its power consumption is reduced by a factor of more than 16. The ELD-compensated quantizer itself is 33% more power efficient, since the delay of the pre-amplifier is removed and the effective regeneration time of the comparator latch is maximized.

7.2.5 Conclusions

A novel current-mode multi-path ELD compensation for multi-GHz sampling CT ΣΔ ADCs with multi-bit quantization is proposed to solve the problem due to the parasitic delay caused by the poles of the summing amplifier and the pre-amplifier. The loop filter amplifier is not in the fast feedback loop, and its GBW requirement is relaxed. The delay of the pre-amplifiers is removed, leaving more effective regeneration time for the comparator latch. For an exemplary 2-1-1 MASH SDM with 3-bit quantization, a BW of 600 MHz and SQNR of 71 dB are achieved. Transistor-level simulations show that the GBW requirement and power consumption of the loop filter amplifier are reduced by a factor of 4.4 and 16 with respect to existing state-of-the-art ELD compensation techniques. All these properties and simulated results show the potential of our proposed techniques for power-efficient broadband medium-resolution ADC applications.

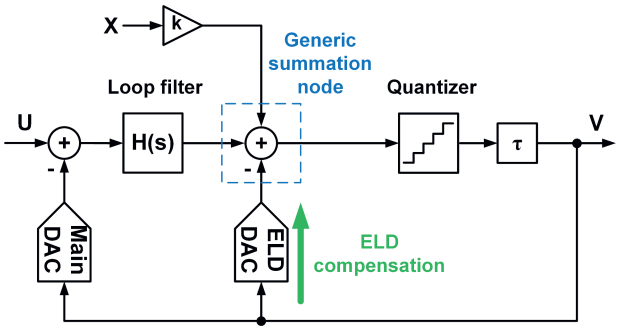


Figure 7.14: Simplified block diagram of an exemplary CT SDM with ELD compensation and a generic summation node

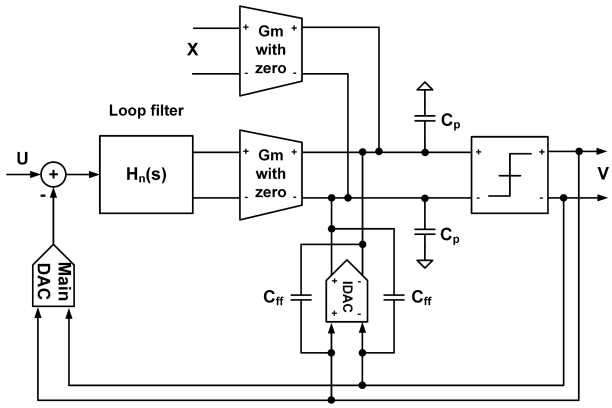
7.3 Overcoming parasitic capacitance on summation node

Section 7.1.7 shows the state-of-the-art current-mode ELD compensation technique for CT SDMs with 1-bit quantization in Figure 7.7a. The previous section proposes a current-mode multi-path ELD compensation for CT SDMs with multi-bit quantization. These two approaches have one limitation for multi-GHz sampling rate ΣΔ ADC applications – they are sensitive to the parasitic capacitance on the summation node. The layout design and extraction of a 3-bit quantizer with the proposed current-mode multi-path ELD compensation show that the parasitic capacitance on the summation output node is very large (about 50 fF in 40 nm CMOS). The design choices that lead to this large parasitic capacitance value is elaborated in Chapter 11.1.7. This parasitic capacitance causes two problems. Firstly, it causes an incomplete settling of the ELD feedback information. Secondly, it causes a parasitic pole in the loop filter path at the Gm cell output. These two problems can degrade the performance of the SDM, or even make it unstable.

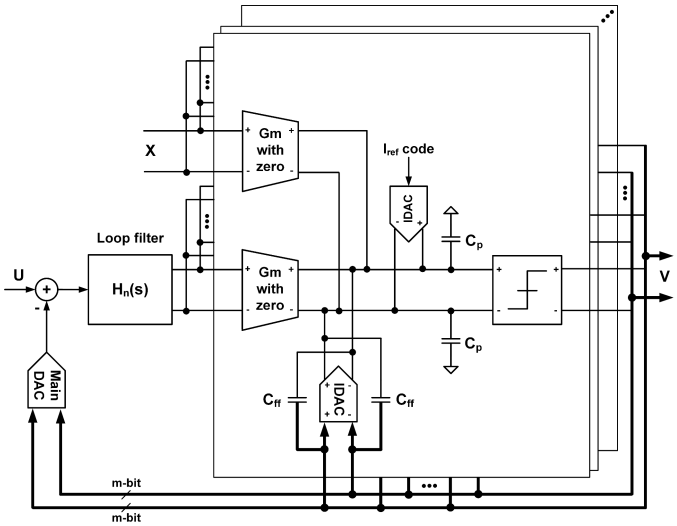
Another problem highlighted in this section is that a generic summation node is needed at the input of the quantizer in some SDM architectures for system-level optimization. It is needed in our 2-1-1 MASH architecture for the test chip implementation shown in Figure 5.6 as well. This generic summation node is missing or limiting the performance in the state-of-the-art approaches. This section proposes system-level and circuit-level solutions for the aforementioned problems.

7.3.1 System architecture

Figure 7.14 shows a simplified block diagram of an exemplary CT SDM with ELD compensation and a generic summation node. A generic summation node at the input of the quantizer is needed in some SDM architectures for the optimization of



(a)



(b)

Figure 7.15: Block diagram of an exemplary CT ΣΔ ADC with a generic summation node and the proposed ELD compensation technique with passive summation in current domain with a current-steering DAC with a feedforward capacitor, and gm stage with a zero: (a) for 1-bit quantization (b) for multi-bit quantization.

the thermal noise at the internal nodes of the loop filter, or for the optimization of the signal transfer function, or required by the feedforward loop filter architecture. In Figure 7.14, the node X can be the SDM input signal U, or an internal node in the loop filter.

Figure 7.15a and 7.15b show the block diagram an exemplary CT ΣΔ ADC with a

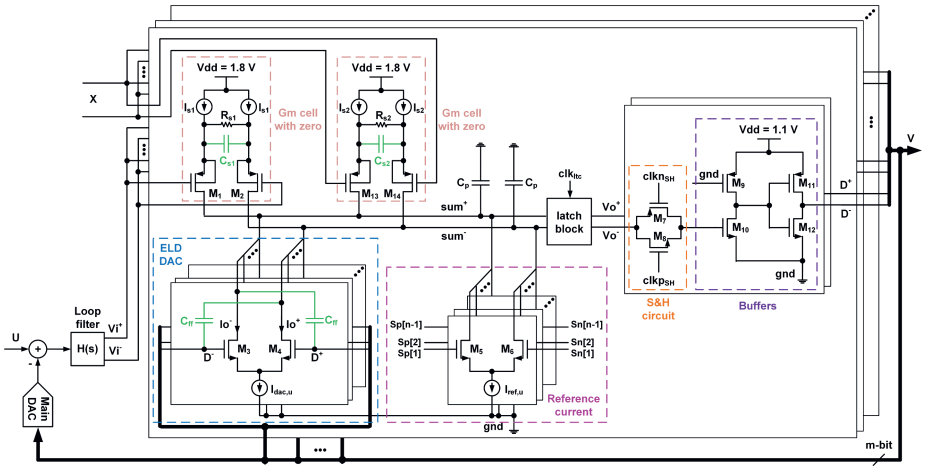


Figure 7.16: Proposed schematics of the SDM with multi-bit quantization, a generic summation node with current-mode multi-path ELD compensation with a feedforward capacitor, and Gm cell with a zero.

generic summation node and the proposed ELD compensation technique for 1-bit and multi-bit quantization, respectively. The generic summation node is implemented as the current summation. As shown in Fig 7.15a and 7.15b, the key features of the proposed approach are twofold. Firstly, in parallel with the current steering ELD DAC (IDAC), a feedforward capacitor C_{ff} is added between the input and output nodes of the DAC, to improve the settling of the ELD feedback information. Secondly, an additional zero is built in the Gm cell. This zero compensates the phase shift of the parasitic pole caused by the parasitic capacitance C_p and g_m. Thus, the problems caused by the parasitic capacitance C_p on both ELD path and loop filter path are compensated.

7.3.2 Circuit implementation

The transistor-level circuit implementation of the proposed SDM system is shown in Figure 7.16. Here an SDM with multi-bit quantization and the proposed generic summation node and ELD compensation approach is shown as an example, and the SDM with 1-bit quantization can be implemented in a similar way. It shows one slice of the duplicated ELD compensation loop and 1-bit comparator in detail. Here the SDM is assumed to use $(n+1)$-level quantization. So the SDM has totally n slices of duplicated ELD compensation loop and 1-bit comparator. The parasitic capacitance C_p on the summation nodes is explicitly drawn.

The Gm cell with zero, reference current, S&H circuit and buffers are implemented in the same way as described in Section 7.2.3. Compared to Figure 7.10, it has two

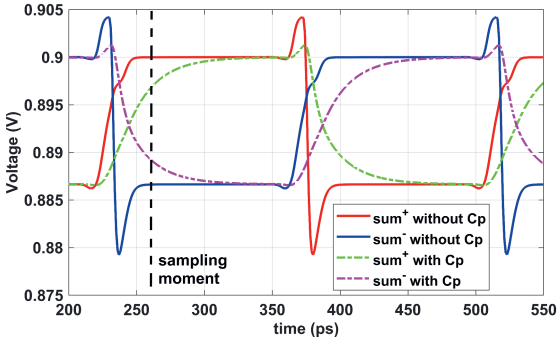
differences, besides the explicitly-drawn parasitic capacitance C_p: (1) It contains two Gm cells with zero here, one for the loop filter output Vi^+ and Vi^-, the other for the generic summation input X. (2) In every 1-bit current steering DAC, two cross-coupled feedforward capacitors C_{ff} are added (shown in green color in Figure 7.16). One capacitor C_{ff} is added between D^- and Io^+, while another capacitor C_{ff} is added between D^+ and Io^-. Notice that the Io^- node is connected to sum^+ node (strictly speaking they are the same node), while the Io^+ node is connected to sum^- node. The sum^+ and sum^- nodes are the summation nodes of the Gm cell output current, ELD DAC output current and the reference current. They are at the same time the input of the latch block.

7.3.3 Simulation results

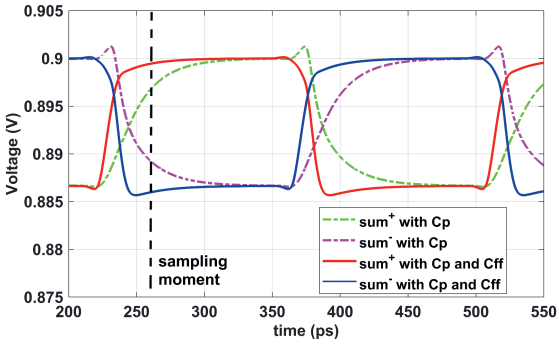
Figure 7.17 shows the transient simulation results on the ELD feedback settling, which confirms the effectiveness of the proposed system and circuit. In this simulation, only the ELD feedback signal settling on the summation output nodes are shown, and the Gm cell input voltages are connected to its common-mode voltage. Figure 7.17a shows the transient behavior of the voltages of sum^+ and sum^- nodes, with and without a parasitic capacitance C_p. The value of C_p comes from the post-layout extraction, which is 50 fF for the designed ADC test chip. The solid red and blue lines show sum^+ and sum^- voltages without the parasitic capacitance C_p. The settling of the summation node voltages is very fast. However, when there is a large parasitic capacitance C_p on the summation nodes, the settling becomes much slower, shown as the dashed green and magenta lines. In a target application of a 7 GHz sampling SDM, the available setting time between the switching of the ELD DAC input (D^+, D^-) and the sampling moment of the comparator latch is about 30 ps. The sampling moment is indicated in Figure 7.17a as the dashed black line. In this case, the differential voltage on the summation node ($sum^+ - sum^-$) should be switching between -13.4 mV to +13.4 mV. Without C_p, at the sampling moment the ELD feedback signal on the summation node is fully settled. However, in the case with a large parasitic capacitance C_p, at the sampling moment, the ELD feedback signal on the summation node is only 78.7% settled. In this case, the delay from the crossing-point of D^+ and D^- nodes, to 95% settling of the sum^+ and sum^- nodes is 61 ps.

Figure 7.17b shows the effect of the feedforward capacitance C_{ff}. With the same parasitic capacitance C_p, when the feedforward capacitance C_{ff} is added, which is 1.35 fF in this design, at the sampling moment the ELD feedback signal on the summation node is 100.4% settled. The settling of the ELD feedback signal is a bit overshot because C_{ff} is a little bit too large in this case. Of course the SDM stability and resolution is not sensitive to the residue ELD settling error of 0.4%. In this case, the delay from the crossing-point of D^+ and D^- nodes, to 95% settling of the sum^+ and sum^- nodes is reduced to 13 ps.

The functionality of the proposed Gm cell with zero is checked by AC simulation,



(a)

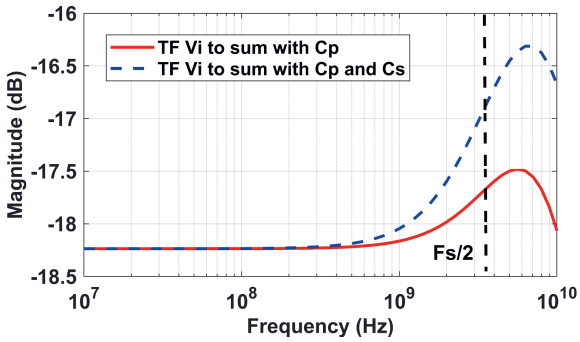


(b)

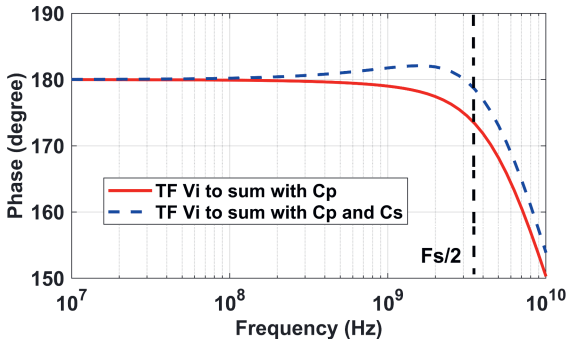
Figure 7.17: Transient simulation results on the ELD feedback settling: (a) sum^+ and sum^- voltages with and without C_p (b) sum^+ and sum^- voltages with C_p, with and without C_{ff}

which is shown in Figure 7.18. Figure 7.18a shows the magnitude of the transfer functions from the loop filter output node $Vi^{+/-}$ to the summation node $sum^+/-$, with and without the zero (generated by the capacitor C_{s1} with a value of 20 fF). Figure 11.5b shows the phase correspondingly. At $F_S/2$, which is 3.5 GHz in this design, the phase shift without C_{s1} is -6.5°. With C_{s1} which creates a zero in the transfer function of the Gm cell, the phase shift at $F_S/2$ is -1.3°. Please notice that if C_{s1} is further increased the phase can be further boosted up at $F_S/2$, but the phase between 500 MHz – 3 GHz will be higher than the desired value of 180°.

A 2-1-1 MASH SDM with 3-bit quantization is designed at transistor and layout level in a 40nm CMOS technology. In this SDM, the 3-bit quantizers, generic summation node, current-mode multi-path ELD compensation with a feedforward capacitor, and Gm cell with a zero are implemented at layout level. The other parts of the SDM are modeled at transistor level (schematic). Figure 7.19 shows the simulated output



(a)



(b)

Figure 7.18: AC simulation results on the transfer function of the gm cell with and without zero (Cs1): (a) magnitude from Vi to sum (b) phase from Vi to sum

spectrum. The red spectrum is before a calibration and the blue spectrum is after a digital calibration for the analog loop filter and digital NCF mismatch (this calibration is discussed in Chapter 6). After the Matlab calibration, the SDM achieves a SQNR of 66.2 dB for 500 MHz bandwidth. It shows that the proposed technique is verified with post-layout simulations.

7.3.4 Conclusions

In this section, a system-level and circuit-level approach to overcome the limitation caused by the parasitic capacitance on the summation node in the current-mode ELD compensation is proposed. Moreover, a generic summation node is added at the input of the quantizer to facilitate SDM system-level optimization. Transistor-level and post-layout simulations show the effectiveness of the proposed approach. Simulation results shows that the settling time of the ELD feedback signal at the

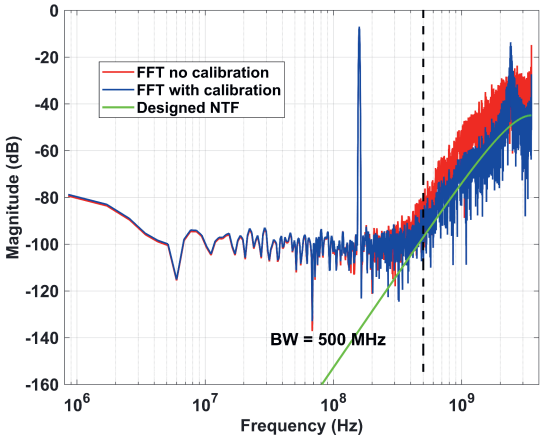


Figure 7.19: Simulated output spectrum of a 2-1-1 MASH SDM with the proposed generic summation node, ELD compensation loop and quantizer in post-layout

summation node output is reduced from 61 ps to 13 ps thanks to the feedforward capacitance, which allows higher sampling rate and broader BW for the SDMs. The parasitic pole at the loop filter path is compensated by the added zero in the Gm cell. The proposed system and circuit enable CT ΣΔ ADCs with higher sampling rate and broader signal BW.

7.4 Conclusions

This chapter studies the high-speed ELD compensation techniques. The state-of-the-art high-speed ELD compensation techniques are firstly studied and classified, which shows that the speed limitation of the ELD compensation is a bottleneck for multi-GHz sampling multi-bit ΣΔ ADCs. This chapter further proposes a current-mode multi-path ELD compensation for multi-GHz sampling multi-bit ΣΔ ADCs. The loop filter amplifier is not in the fast feedback loop, and its GBW requirement is relaxed. The delay of the pre-amplifiers is removed, leaving more effective regeneration time for the comparator latch. However, a large parasitic capacitance at the summation node is observed in the post-layout extraction, which limits the speed of the SDM. This chapter further proposes solutions to overcome the limitation caused by this parasitic capacitance. Cross-coupled feedforward capacitance C_{ff} can boost up the settling of the ELD feedback signal. And the phase shift in the loop filter path can be compensated by adding a zero in the Gm cell. Transistor-level and post-layout simulations show the effectiveness of the proposed techniques. Test chip measurement results are shown in Chapter 11. All these properties and results show the potential of our techniques for power-efficient broadband medium-resolution ADC applications.

Chapter 8

Comparators for broadband CT $\Sigma\Delta$ ADCs

This chapter presents two new techniques for high-speed comparators in broadband CT $\Sigma\Delta$ ADCs. In conventional $\Sigma\Delta$ ADCs, the comparator reset time restricts the maximal achievable ADC sampling rate and signal BW. Firstly, this chapter introduces a current-mode locally-time-interleaved multi-bit quantizer in Section 8.1, to move the comparator reset time out of the 1 T_S time budget. Thus, the ADC sampling rate and the signal BW can be further increased. The current-mode multi-path ELD compensation technique introduced in Section 7.2 has no gain in the summation, since it is passive. The offset originating from the comparator latch is amplified when referred to the loop filter output node, which reduces the ADC resolution, and has to be calibrated. A comparator offset calibration for the current-mode multi-path locally-time-interleaved ELD-compensated quantizer is proposed in Section 8.2. Conclusions are drawn in the end.

8.1 Current-mode locally-time-interleaved multi-bit quantizer

This section proposes a current-mode locally-time-interleaved (TI) multi-bit quantizer for CT $\Sigma\Delta$ ADCs with multi-GHz sampling rate. This technique allows for moving the comparator reset time out of the one sampling clock period time budget [24, 84, 88]. Thus, the ADC sampling rate can be further increased with the same requirement on the quantizer metastability, hence achieving a broader signal BW.

8.1.1 Motivation for quantizer time-interleaving

For multi-bit multi-GHz sampling CT ΣΔ ADCs, maximizing the effective regeneration time of the comparator referring to the ADC sampling period is essential to increase the ADC sampling rate and signal BW, while satisfying the requirement on the quantizer metastability. It requires high-speed ELD compensation [69, 77] and high-speed comparators. The state-of-the-art high-speed ELD compensation techniques have been reviewed in Chapter 7.1. In the conventional SDM system architecture with multi-bit quantization and ELD compensation shown in Figure 7.8, typically up to one sampling clock period (T_S) ELD is compensated.

Figure 8.1a shows an illustrative timing diagram for a broadband CT ΣΔ ADC without quantizer time-interleaving. Within 1 T_S, the multi-bit quantizer needs to complete three functions – regeneration (denoted as T_{reg}), reset (denoted as T_{rst}), and tracking the next initial condition (referred to as "input settling" and denoted as T_{set} in this chapter). The reset phase and the input settling phase can be either combined or separated: (1) If the reset phase and the input settling phase are combined, it means the latch input/output nodes are tracking the next initial condition when the latch is reset. In this case, the initial condition stored at the latch input/output nodes is relatively small. (2) If the reset phase and the input settling phase are separated, in the reset phase, the latch input/output nodes are reset. In the input settling phase, the reset switches are OFF, and the latch input/output nodes track the next initial condition. In this case, the initial condition stored at the latch input/output nodes is larger, which is beneficial for a higher quantization gain and a lower input referred comparator offset. However, it requires more complicated clock phases, and both of the reset time and the input settling time are shorter.

The minimum achievable value of the latch's regeneration time constant $\tau_{reg,min}$ is defined by the technology. Even if more power is spent by the latch, its time constant cannot be further reduced because self-loading is dominant. To achieve a certain DR (or peak SNDR) target for a certain BW, a minimum quantization gain requirement $G_{q,min}$ (in [dB]) can be derived, which should be generated by the latch (see Figure 5.9). Thus, the minimum effective regeneration time can be calculated as:

$$T_{reg,eff,min} = log(10^{\frac{G_{q,min}}{20}}) \cdot \tau_{reg,min} \tag{8.1}$$

In the end of the regeneration, the latch's output is sampled and passed to the main DAC and the ELD DAC. To guarantee that the latch's output is properly sampled before the resetting of the latch, the starting of the latch output sampling should be at least τ earlier than the starting of reset phase (this time τ is referred to as "sampling to reset delay" and denoted as $\tau_{smp-rst}$ in this chapter). With the current-mode multi-path ELD compensation technique proposed in Chapter 7.2, the ELD feedback path has less delay than the main feedback path. The propagation delay from the quantizer to the main DAC is denoted as τ_{prop}, and the delay of the main DAC itself is denoted as τ_{DAC}. The sampling aperture of the DAC sampler is considered as part of the DAC delay.

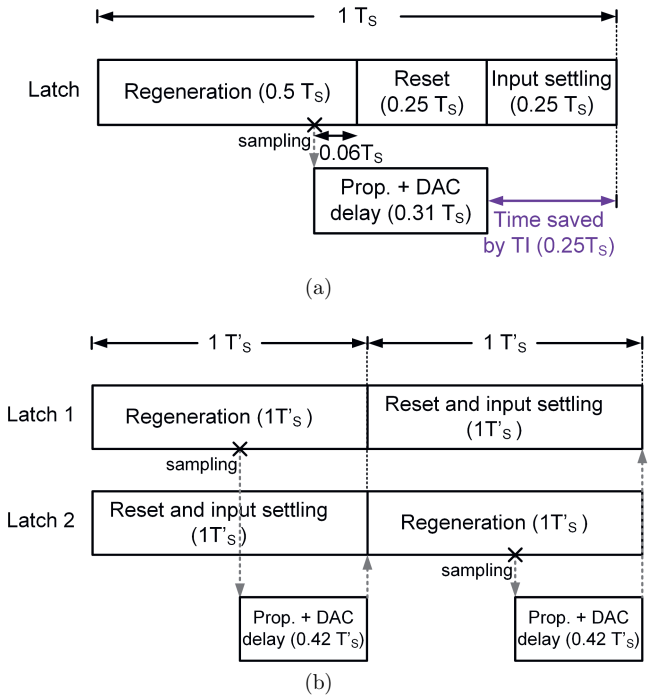


Figure 8.1: (a) Illustrative timing diagram without time-interleaving (b) Illustrative timing diagram with time-interleaving.

The reset time and input settling time should be separately optimized. Reducing the reset time forces to increase the size of the reset switch, to meet the requirement on the comparator hysteresis. However, sizing up the reset switch adds more load to the latch input/output node, which increases the regeneration time constant of the latch, and reduces its quantization gain.

In Figure 8.1a, the minimal achievable ADC sampling period $T_{S,min}$ is determined by the maximal time (or delay) of two paths:

$$T_{path1} = T_{reg,eff,min} + \tau_{smp-rst} + T_{rst} + T_{set} \tag{8.2}$$

$$T_{path2} = T_{reg,eff,min} + \tau_{prop} + \tau_{DAC} \tag{8.3}$$

$$T_{S,min} = max\{T_{path1}, T_{path2}\} \tag{8.4}$$

The reset time T_{rst} and the input settling time T_{set} can be moved out of the 1 T_S time budget by the quantizer time-interleaving [24, 84, 88]. When T_{path1} is longer than T_{path2}, it indicates that if quantizer time-interleaving is applied, $T_{S,min}$ can be reduced.

Schematic design and simulations in 40 nm CMOS technology has been done to es-

timate the maximal sampling rate for a 3-bit SDM with an SNDR target of at least 60 dB, with the SDM architecture shown in Chapter 5. Without quantizer time-interleaving, the minimal sampling period T_S is estimated to be about 160 ps. The latch's time constant is optimized to be 5.5 ps from schematic design. From the starting of the latch regeneration to the sampling of the latch's output, the effective regeneration time ($T_{reg,eff}$) should be at least 70 ps to generate the required quantization gain. The sampling to reset delay ($\tau_{smp-rst}$) is designed to be 10 ps. The propagation delay from the quantizer to the main DAC and the delay of the main DAC itself are about 50 ps together. The reset time and input settling time are optimized to be 40 ps each. From simulation, T_{path1} = 160 ps, and T_{path2} = 120 ps. Since $T_{path1} > T_{path2}$, the quantizer time-interleaving can be applied in this case to minimize T_S.

Figure 8.1b presents an illustrative timing diagram for a broadband CT ΣΔ ADC with quantizer time-interleaving. Latch 1 and Latch 2 are working in a time-interleaved way [24, 84, 88]. When one latch is in the regeneration phase, the other latch is in the reset and input settling phase. Thus, the reset and input settling time is moved out of the 1 T'_S time budget (T'_S in Figure 8.1b is smaller than T_S in Figure 8.1a), allowing the whole 1 T'_S time for the comparator regeneration. The regeneration time, reset and input settling time are both doubled referred to the ADC sampling period. The minimal T'_S is defined by T_{path2} only. With quantizer time-interleaving, the minimal achievable sampling period T'_S is estimated to be about 120 ps (based on schematic simulation results). Quantizer time-interleaving can enable 1.33× higher ADC sampling rate, and hence 1.33× broader signal BW.

In general, time-interleaving has advantages if the required performance (which is speed in the context of this chapter) is at the edge of what the technology can deliver. It means that the power dissipation increases stronger than linear with speed (e.g. to reduce the regeneration time constant of the latch). In another words, the speed is very costly there, and the properties of the technology are not used then efficiently.

The disadvantage of time-interleaving is that the system has different paths. The matching errors in both the function that is performed (e.g. gain, delay) and the differences in the (local) error signals like offsets, noise and interferences contribute to the total error of the system. The matching errors in the function cause modulation at half-clock frequency, leaving up to half-clock undesired signals ('pattern noise' in case of modulated DC-offsets), down-converted (down-mixing) noise, and modulated transfer functions (part of STF and NTF modulated at half clock). In the context of the quantizer time-interleaving in ΣΔ ADCs, the difference in the comparator offsets between the TI quantizers down-converts the out-of-band quantization noise into the signal band, and increases the in-band noise. This effect is presented in Section 8.1.3.

	Globally-TI	Locally-TI
Voltage-mode ELD	Voltage-mode globally-TI	Voltage-mode locally-TI
current-mode ELD	current-mode globally-TI	current-mode locally-TI

Figure 8.2: Quantizer time-interleaving implementation alternatives.

8.1.2 Quantizer time-interleaving implementation alternatives

Various quantizer time-interleaving techniques can be found in the literature [24, 84, 89, 88]. Figure 8.2 presents a two-dimensional classification on the implementation alternatives of quantizer time-interleaving techniques. First, the ELD compensation can be implemented either in the voltage-mode [88] or in the current-mode [81]. Second, the time-interleaving can be applied either at the multi-bit quantizer level (referred to as "globally-TI"), or at the 1-bit comparator level (referred to as "locally-TI"). The voltage-mode globally-TI quantizer has been proposed in [89, 88], and its block diagram is shown in Figure 8.3. The current-mode multi-path ELD compensation proposed in Chapter 7.2 has many advantages over the voltage-mode ELD compensation techniques. Thus, an implementation of the quantizer time-interleaving which is compatible with the current-mode ELD compensation is proposed in this thesis. A current-mode globally-TI quantizer requires to convert the current output from the ELD summation back into a voltage signal. The V/I and I/V conversions add substantial delay, which makes it not suitable for the ELD feedback loop in the multi-GHz sampling rate scenarios (discussed in Chapter 7). This thesis proposes a current-mode locally-TI quantizer shown in Figure 8.4, which will be discussed later. Since a current-mode ELD compensation has been chosen in this design (Chapter 7.2), a voltage-mode locally-TI quantizer (which is not compatible with the current-mode ELD compensation) has not been investigated in this thesis.

In an SDM with the voltage-mode globally-TI quantizer (Figure 8.3), the quantizer input voltage (V_{in}) needs to be switched to either multi-bit quantizer input at half SDM sampling frequency ($\frac{1}{2}$ F_S). The input parasitic capacitance (C_p) of a n-bit quantizer is $(2^n - 1)\times$ of the input parasitic capacitance of one of its composing comparators. The parasitic capacitance C_p needs to be charged in this switching period. The resistance R_{ON} of the switches and C_p define the charging time constant, which limits the speed of the quantizer input settling. The input settling time is part of the total ELD, which eventually limits the minimal achievable T_S.

In an SDM with the proposed current-mode locally-TI quantizer (Figure 8.4), each 1-bit comparator is locally time-interleaved with two comparator latches with current

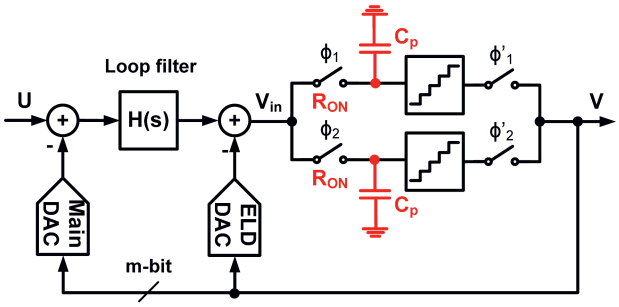


Figure 8.3: Block diagram of an ELD-compensated multi-bit SDM with the voltage-mode globally-TI quantizer [88, 89].

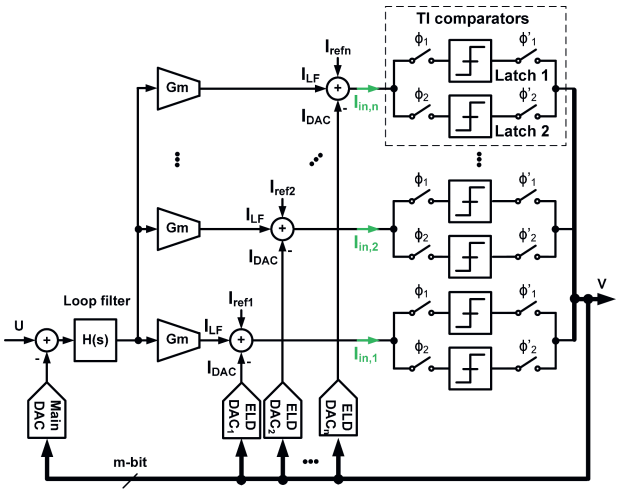


Figure 8.4: Block diagram of an ELD-compensated multi-bit SDM with a proposed current-mode locally-TI quantizer.

input, on top of the current-mode multi-path ELD compensation technique in Figure 7.9. The input current ($I_{in,n}$) of the TI comparators is switched to latch 1 when Φ_1 is high, and it is switched to latch 2 when Φ_2 is high. Since the time-interleaving happens in the current domain, R_{ON} of the TI switches is in series with the large output impedance $R_{out,gm}$ of the Gm cell, and R_{ON} is much lower than $R_{out,gm}$. The time constant is determined by the transconductance g_m of the Gm cell, and the input parasitic capacitance of the latch. Since R_{ON} of the TI switches does not determine the time constant, its requirement is much relaxed compared to the voltage-mode TI. This is beneficial for high-speed operation.

In general, it is more advantageous for high-speed operation to implement both of the ELD summation and the time-interleaving in the current domain for the following two

reasons: (1) summation is easier to be implemented in the current domain than in the voltage domain; (2) in the current domain, the requirement on the R_{ON} of the switches is relaxed. To benefit from the speed advantages offered by the combination of the current-mode multi-path ELD compensation and the quantizer time-interleaving, the proposed current-mode locally-TI quantizer technique is the preferred way for multi-GHz-sampling ΣΔ ADCs.

8.1.3 Sensitivity to comparator offset

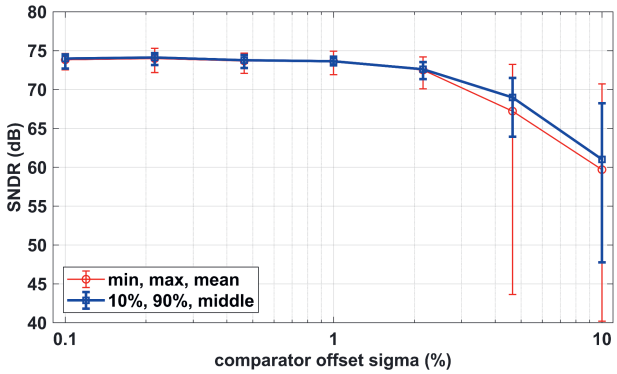
The current-mode multi-path ELD compensation technique proposed in Chapter 7.2 has no gain in its summation, since passive summation is used. The offset originating from the comparator latch is amplified when referred to the loop filter output node. Thus it is important to check how sensitive is the SNDR of the SDM to the comparator offset, in the scenarios with and without the quantizer time-interleaving.

Figure 8.5 presents the simulated SNDR versus the standard deviation $\sigma_{V_{OS}}$ of the comparator offset V_{OS}, with and without the quantizer time-interleaving. The 2-1-1 MASH SDM architecture in Chapter 5 is modelled in Matlab/Simulink. $\sigma_{V_{OS}}$ in this simulation is referred to the quantizer's input full-scale (V_{FS}). For every $\sigma_{V_{OS}}$, 50 independent simulations are run. Some statistics of the simulated SNDR are plotted, such as minimal, maximal, mean values (red line) and 10%, 90% and middle values (blue line). When $\sigma_{V_{OS}}$ is 10%, the simulated SNDR is 59.7 ± 8 dB ($\pm\sigma$) without the quantizer time-interleaving, which is limited by the comparator offset (Figure 8.5a). With the quantizer time-interleaving, the simulated SNDR is 57.8 ± 9.5 dB ($\pm\sigma$) for the same $\sigma_{V_{OS}}$ (Figure 8.5b). The SNDR is a bit more sensitive to the comparator offset, since the out-of-band quantization noise is mixed down in-band due to the different offset of the TI comparators. Fortunately this increased in-band quantization noise due to mixing down is shaped by the NTF, nevertheless the SNDR is in average reduced by 1.9 dB when $\sigma_{V_{OS}}$ is 10%. In both cases, to ensure that the SDM's SNDR is not limited by the comparator offset, $\sigma_{V_{OS}}$ should be less or equal to 2% of the quantizer's input full-scale. Notice that the simulation results shown in Figure 8.5b are generally valid for SDMs with quantizer time-interleaving, regardless of the implementation alternatives shown in Section 8.1.2.

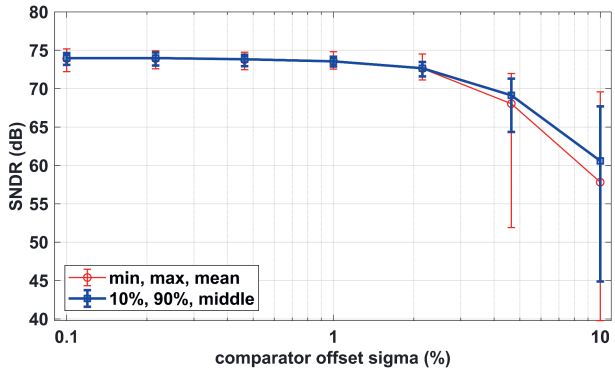
8.1.4 Circuit implementation

A transistor-level implementation of the proposed current-mode locally-TI multi-bit quantizer in a SDM is shown in Figure 8.6. A Gm cell, an ELD DAC, a reference DAC, two TI comparators, the S&H circuit and buffers compose a slice of the ELD-compensated quantizer. The Gm cell, ELD DAC, reference DAC, and buffers are discussed in Chapter 7.2.

The transistors M_7 - M_{22} compose one locally-TI comparator with current input. The



(a)



(b)

Figure 8.5: Simulated SNDR versus the standard deviation of the comparator offset σ (a) without the quantizer time-interleaving (b) with the quantizer time-interleaving.

transistors M_9 - M_{12} and M_{17} - M_{20} compose two NMOS latches. In the following description, the latch composed of M_9 - M_{12} is referred as latch 1, and the latch composed of M_{17} - M_{20} is referred as latch 2. The transistors M_7, M_8, M_{13} - M_{16}, M_{21} and M_{22} work as the switches between the summation nodes (sum^+ and sum^-) and the latch input/output nodes ($Vo1^{+/-}$ and $Vo2^{+/-}$). They are used as the reset switches of the latches as well. The input current is transformed to voltage via the ON resistance of M_8, M_{14}, M_{16} and M_{22}. Two complementary clock signals $clkp_{ltc}$ and $clkn_{ltc}$ are needed.

During the reset and input settling phase, the latch output nodes are set to a common-mode voltage plus a small differential voltage. For example, when latch 1 is in reset and input settling phase, the switches M_7, M_8, M_{13}, M_{14} are ON. The differential output current of the summation nodes (sum^+ and sum^-) is converted to a differential voltage on the latch input/output nodes ($Vo1^{+/-}$) by the ON resistance of M_8/M_{14}.

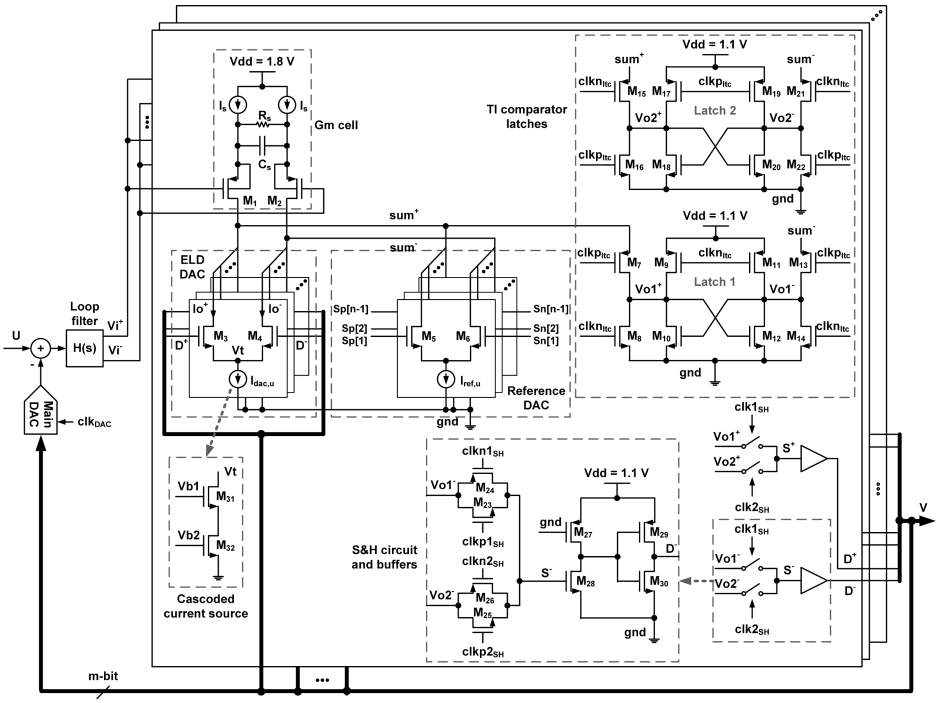


Figure 8.6: Proposed circuits of the SDM with locally-TI multi-bit quantizer.

The common-mode voltage on the latch input/output nodes ($Vo1^{+/-}$) is much lower than the threshold voltage of the NMOS, to turn off the positive feedback of the NMOS latch. Thus, no extra tail NMOS or PMOS transistor is required to turn off the latch. During the regeneration mode, the Drain-to-Source voltage V_{DS} is maximized and the transconductance (g_m) of the NMOS $M_{10}/M_{12}/M_{18}/M_{20}$ is maximized as well. Moreover, at the beginning of the regeneration, a large peak current is required to charge the internal nodes of the latch, such that the NMOS $M_{10}/M_{12}/M_{18}/M_{20}$ turn ON and the positive feedback starts. This peak current is not limited by the removed tail NMOS or PMOS transistor in this design. It is defined by the PMOS $M_9/M_{11}/M_{17}/M_{19}$.

A concern of the designed NMOS latch is that it has static current flowing on one branch, even when the latch output nodes are settled. This static current can be turned off when the decision has been made by the latch with the self-cut-off comparator technique presented in [34], at the cost of some extra load on the latch output nodes which reduces the speed of the latch. In this design, the self-cut-off comparator technique is not used. From schematic simulation results, an NMOS latch with PMOS load is employed to achieve 8.4 GHz sampling rate with more than 120 dB of quantization gain at the cost of 0.91 mW power per comparator latch.

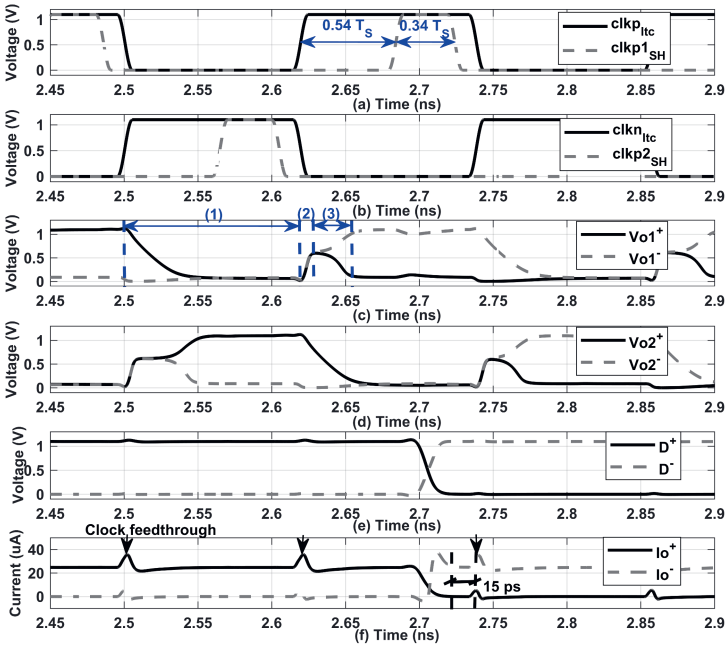


Figure 8.7: Clock timing diagram and some internal nodes of the proposed circuits: (a)–(b) latch clock and sampler clock; (c)–(d) latch 1 and latch 2 outputs; (e) sampled quantizer outputs after buffers; (f) unit ELD DAC output current.

After the TI comparators, two transmission gates (M_{23} - M_{26}) with two complementary sampling clocks ($clkp1_{SH}$/$clkn1_{SH}$, $clkp2_{SH}$/$clkn2_{SH}$) are employed to sample the TI comparators output at the end of the corresponding regeneration phase, and to hold it on their common output capacitance. The samplers (M_{23} - M_{26}) work as a multiplexer.

8.1.5 Simulation results

Without loss of generality, a CT feedback (FB) 2-1-1 MASH ΣΔ ADC with 3-bit quantization in every loop is considered to substantiate the proposed technique [79]. The sampling frequency is $F_S = 8.4$ GHz and the oversampling ratio is 7, to achieve a signal BW of 600 MHz. The proposed locally-TI 3-bit quantizers, the 2-1-1 MASH loop filter and the FB DACs are designed at transistor-level in a 40 nm CMOS technology.

Figure 8.7 shows the clock diagram and the internal nodes of the quantizer and ELD DAC from the schematic simulation. The latch clock signals $clkp_{ltc}$ and $clkn_{ltc}$ are at the half of the SDM sampling rate (4.2 GHz), and they are with 50% duty cycle.

Figure 8.7c and 8.7d depict the differential output signal of the TI comparators. At the end of the regeneration phase, the corresponding sampling clock signal clkp1$_{SH}$ (or clkp2$_{SH}$) becomes high, and the comparator output is sampled. clkp1$_{SH}$ (or clkp2$_{SH}$) should become low before resetting the comparator in order to hold the data. In Figure 8.7c, (1) indicates the reset and the input settling time, which is 1 T$_S$ (119 ps). (2) indicates that at the beginning of the regeneration phase of the latch 1, the common-mode voltage of Vo1$^{+/-}$ settles to about $\frac{1}{2}$V$_{dd}$. (3) indicates the exponential settling of the latch outputs Vo1$^{+/-}$. Although the regeneration time when the sampler is disconnected from the latch is 0.54 T$_S$ (discussed in detail later), the exponential settling phase is typically much less than 0.54 T$_S$ since the absolute value of the initial condition is larger than $\frac{1}{G_q}$ in most of the cases (G_q is the quantization gain of the latch). Figure 8.7e and 8.7f show the input voltage and the output current of a unit ELD DAC, respectively. Since the total delay of the fast FB loop should be less than 1 T$_S$, the ELD DAC output current must settle before the starting of the next regeneration of either comparator. In Figure 8.7f, the ELD DAC output current is settled about 15 ps before the next positive clock edge of clkp$_{ltc}$ or clkn$_{ltc}$, which is a tradeoff between maximizing the effective regeneration time of the latch, and the robustness of the ELD FB loop. The ELD FB loop is robust in this design, since the ELD FB loop can still be closed when the total additional delay caused by e.g. PVT variation, device mismatch, and layout-dependent effect is less than 15 ps. The peaks indicated by the arrows, caused by the clock feedthrough, do not degrade the resolution of the SDM.

In this design, the time between the starting of the regeneration, and the starting of the sampling of the latch output, is optimized to be 54% of T$_S$. During this time period, the latch in the regeneration phase is disconnected from the summation nodes, and its samplers are OFF. Thus the load on the latch output nodes (Vo1$^{+/-}$ or Vo2$^{+/-}$) is minimized, and the time constant τ of the latch is minimized. The simulated time constant τ of the latch at schematic level is 5.5 ps with load, and the latch offers the majority part of the total quantization gain. When clkp1$_{SH}$ (clkp2$_{SH}$) is high, which is optimized to be 34% of T$_S$ for this design, the corresponding pass gates turn ON, and the latch output is sampled at the parasitic capacitance on S$^{+/-}$ nodes. In this time period, although the load on the latch output nodes is increased, the positive feedback of the latch can still produce some quantization gain, if the latch output nodes are not settled. The total effective regeneration time is 0.88 T$_S$.

The aforementioned 2-1-1 MASH ΣΔ ADC was simulated for 134400 samples (16 us). The transistor layout parasitic model was included in the simulation. Extra capacitance (20% of the total parasitic capacitance of that node) was added at the latch output nodes to model the routing parasitic capacitance. Figure 8.8 depicts the simulated output spectrum (2^{17} samples) with -3.1 dBFS input signal. The simulated SQNR is 66.3 dB for BW = 600 MHz. Within the simulated 134400 samples of the main DAC output, no metastability error is observed. The transistor-level simulations demonstrate the power efficiency of the proposed technique. The simulated power consumption of the ELD-compensated 3-bit quantizer in the 1st loop is 28 mW (4

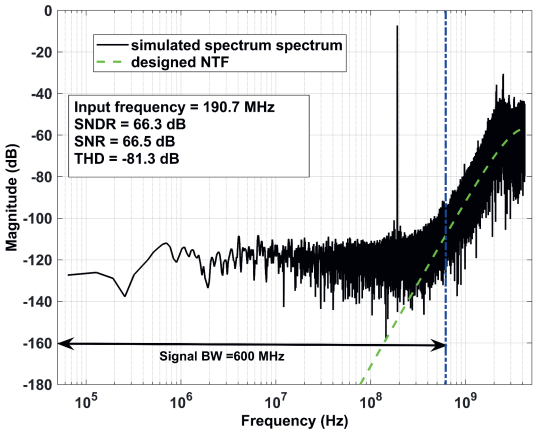


Figure 8.8: Simulated output spectrum of a 2-1-1 MASH ΣΔ modulator with the proposed system and circuits.

mW per 1-bit quantization). Monte-Carlo simulations with random mismatch show that the total input-referred offset has a standard deviation $\sigma = 3$ LSB (LSB is the least significant bit of the 3-bit quantizer), which requires calibration to maintain the ADC resolution. A comparator offset calibration for this current-mode multi-path TI quantizer is proposed in Section 8.2.

Table 8.1 compares this work to state-of-the-art ΣΔ ADCs. Thanks to the proposed current-mode locally-TI quantizer, the quantizer effective regeneration time is significantly increased from 0.54 T_S [16] to 0.88 T_S, which increases the quantization gain by several tens of dB. The test chip measurement results with the proposed technique will be presented in Chapter 11.

8.1.6 Conclusions

A novel current-mode locally-TI quantizer is proposed for multi-GHz sampling CT ΣΔ ADCs. It is compatible with the current-mode multi-path ELD compensation technique presented in Chapter 7.2. Applying quantizer time-interleaving can enable 1.33× higher ADC sampling rate and signal bandwidth. In proposed current-mode TI quantizer, the R_{ON} of the TI switches does not determine the time constant, and hence the R_{ON} requirement is relaxed compared to the voltage-mode TI quantizer. The reset time and the time to track the next initial condition of the comparator are moved out of the 1 T_S ELD time budget. For an exemplary 2-1-1 MASH SDM with 3-bit quantization, a BW of 600 MHz and an SQNR of 66.3 dB are demonstrated by transistor level simulations in 40 nm CMOS technology. All these properties and simulated results show the potential of the proposed technique for broadband ADC

Table 8.1: Comparison to state-of-the-art Σ Δ ADCs

	This work	[88]	[84]	[16]
Quantizer resolution	8-level	14-level	2-level	17-level
TI quantizer?	Current-mode TI	Voltage-mode TI	Voltage-mode TI	No
Effective reg. time	0.54 T_S + 0.34 T_S	N.A.	0.5 T_S	0.54 T_S
Sampling rate (F_S)	8.4 GHz	5 GHz	6 GHz	8 GHz
Signal BW	600 MHz	156 MHz	60 MHz	465 MHz
SNDR	66.3 dB	66.5 dB	67.6 dB	67 dB
1-bit quant. power	4 mW[a]	3.2 mW[b]	N.A.	5.8 mW[c]
CMOS technology	40 nm	40 nm	65 nm	28 nm
Note	simulation	measurement	measurement	measurement

[a] Including Gm cells, ELD DACs, reference DACs, 2x TI comparators, samplers and buffers
[b] Calculated from [88], excluding ELD compensation
[c] Comparator power, excluding ELD compensation

applications.

8.2 Comparator offset calibration

This section proposes an on-chip comparator offset calibration for broadband CT ΣΔ ADCs with current-mode multi-path ELD compensation (Section 7.2) and locally-TI multi-bit quantizer (Section 8.1).

8.2.1 Introduction

Section 7.1 presents an overview for high-speed ELD compensation techniques, including the active summation and the passive summation. Section 7.2 proposes a current-mode multi-path ELD compensation technique. The ELD compensation techniques with passive summation have one drawback – no gain can be made with passive summation, and thus the input swing of the multi-bit quantizer is reduced, which gives stringent requirements on the comparator offset to not degrade the DR and linearity of the ADC. The circuit implementation of the current-mode multi-path ELD compensation presented in Section 7.2 has an attenuation of 18 dB from the loop filter output to the sampled initial condition of the comparator latch, resulting from the ELD coefficient and an optimization for low phase shift. Thus, the offsets originating from the comparator latches are amplified by 18 dB when referred to the

loop filter output.

Generally the offset requirement can be achieved either by intrinsic matching or by calibration. For the test chip designed in this thesis, since the current-mode multi-path ELD compensation and the locally-TI multi-bit quantizer are applied, the pre-amplifier is removed since the reference currents are added on the ELD summation nodes. Transistor-level Monte-Carlo simulations show that the total input-referred (referred to the loop filter output node) comparator offset has a standard deviation σ = 3 LSB (LSB is the least significant bit of the 3-bit quantizer), which is dominated by the comparator latches (M_9 - M_{12} and M_{17} - M_{20} in Figure 8.6). If the offset requirement is chosen to be achieved by the intrinsic matching, which requires $\sigma \leq \frac{1}{6}$ LSB, the gate area of the transistors in the comparator core should be 324× larger (18^2 = 324), to reduce the offset standard deviation σ by 18× [71]. The parasitic capacitance of such huge transistors would reduce the speed and increase the power consumption of the comparator significantly. Thus, this thesis concludes that the comparator offset requirement cannot be achieved with the intrinsic matching for the target speed, and thus an offset calibration is required.

Transistor-level Monte-Carlo simulations show that the input referred offset has several contributors. Besides the comparator latches as the dominant contributor, the offset contributed by the PMOS transistors of the Gm cell (M_1, M_2 in Figure 8.6), and the switches between the summation nodes and the latches (M_7, M_8, M_{13} - M_{16}, M_{21} and M_{22} in Figure 8.6) needs to be calibrated as well. The calibration range is chosen to be more than $\pm 6\sigma$ of the total input-referred comparator offset for robustness. After offset calibration, the input-referred offset residue should be less than 0.5 LSB, to maintain the ADC resolution.

8.2.2 System architecture

To achieve the required calibration range and accuracy, an on-chip two-step coarse-fine calibration is proposed, as shown in Figure 8.9. The coarse calibration is done by injecting calibration current (I_{cal1}, I_{cal2}) directly at the latches' input, to cover the required calibration range. The fine calibration is achieved by adding a calibration current-steering DAC at the ELD summation node, to achieve the required calibration accuracy. Fine calibration range is more than 2 coarse calibration steps for robustness.

The SDM has two modes — a normal operation mode and a calibration mode. The mode is defined by the control signal in Figure 8.9 (this control signal is called "ena_cali"). In the calibration mode (ena_cali = 1), the quantizer input is disconnected from the loop filter output, and the quantizer input is connected to a fixed voltage, which is the common-mode voltage of the quantizer input during normal operation mode, with a differential voltage of 0. The ELD DAC input is disconnected from the quantizer output, and connected to a fixed code 0 (middle code). The differential reference current is also set to 0 in the calibration mode. Thus, the differential input of the latch is 0 when the offset is 0. The calibration algorithm is proposed per

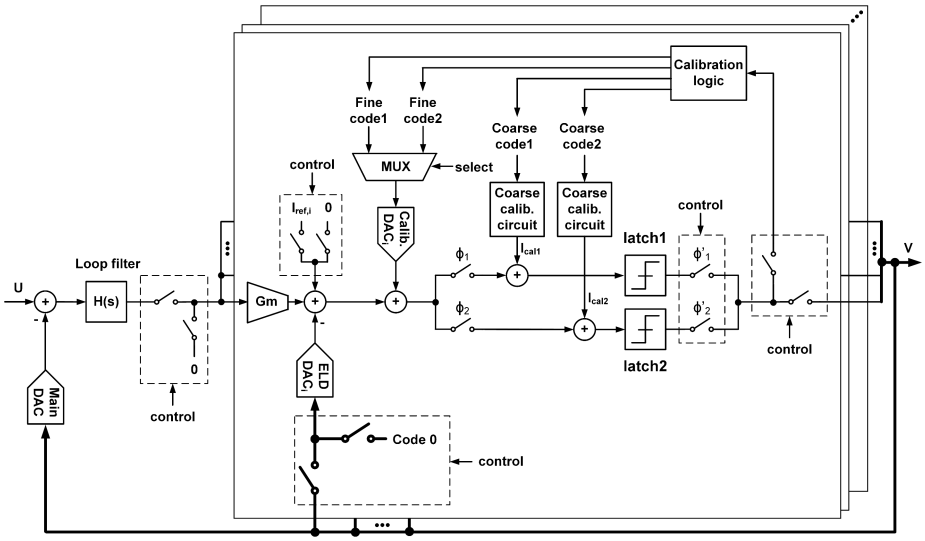


Figure 8.9: Proposed SDM system architecture with current-mode multi-path ELD compensation, locally-TI multi-bit quantizer, and comparator offset calibration circuits.

1-bit quantizer slice, shown as the calibration logic in Figure 8.9.

The principle of calibration algorithm is as follows. In the beginning, latch 1 is under calibration, and only its output is connected to the calibration logic. The coarse calibration code for latch 1 (referred to as coarse code 1) is swept from minus full scale to plus full scale by the minimum step of the coarse code. For every coarse code, the latch 1 output is recorded by the calibration logic. By design it is guaranteed that for the coarse code minus full scale, latch 1 output is always -1 for all possible cases of device mismatch (for a coverage of more than $\pm 6\sigma$). During the sweeping of the coarse code 1, when latch 1 output becomes +1, the correct calibration code is detected, and the sweeping is stopped. The calibration logic set the coarse code 1 by one minimum step back, to compensate the effect of the hysteresis. Now one round of the coarse calibration of latch 1 is finished. Sweeping is used in the calibration algorithm instead of the binary searching, since it is less sensitive to the hysteresis effect of the comparator. A unary weighted coarse calibration circuit can guarantee its transfer function to be inherently monotonic. The flowchart of one round of coarse calibration for latch 1 is shown in Figure 8.10.

Then, the coarse calibration of latch 2 starts. It is similar as the coarse calibration of latch 1. Schematic and post-layout simulations show that the calibration of latch 1 and latch 2 are not completely independent. The dependency can be caused by the following two reasons. (1) The calibration DAC and the summation node are shared by the fine calibration of latch 1 and latch 2, and the memory effect can cause

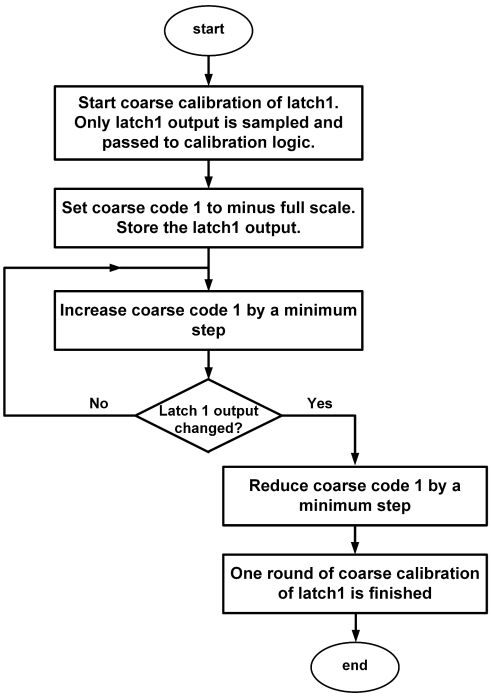


Figure 8.10: Flowchart of one round of coarse calibration (latch 1 as an example).

dependency. (2) Some dependency can be generated from the TI comparators (M_7 - M_{22} in Figure 8.6). During the transient between the reset and input settling phase to the regeneration phase, the comparison result of one latch can influence the initial condition of the other latch. Because the calibration of latch 1 and latch 2 are not completely independent, several iterations on the coarse calibration of latch 1 and latch 2 should be made. The coarse calibration of both latch 1 and latch 2 is finished when their detected coarse codes are not changed. From schematic and post-layout simulations, the coarse calibration codes always converge after a few iterations (e.g. latch 1 $\rightarrow$ latch 2 $\rightarrow$ latch 1 $\rightarrow$ latch 2 $\rightarrow$ latch 1).

After the coarse calibration iterations are finished, the fine calibration starts. Firstly latch 1 is under fine calibration. It also uses a similar principle by sweeping the fine code 1 from minus full scale to plus full scale with the minimum step, and detecting the changing of latch 1 output. After the changing of latch 1 output is detected, the sweeping stops, and the fine code 1 is set back by 1 minimum step. After the fine calibration of latch 1 is finished, the fine calibration of latch 2 starts. Several iterations on the fine calibration of latch 1 and latch 2 are also necessary. The fine calibration of both latch 1 and latch 2 is finished when their detected fine codes are not changed (or changed within one minimum step). From schematic and post-layout simulations, the fine calibration codes always converge within one minimum step after

a few iterations (e.g. latch 1 → latch 2 → latch 1 → latch 2 → latch 1). Notice that one minimum fine calibration step is designed to be about $\frac{1}{6}$ LSB. Thus, even if the fine calibration codes toggles within one minimum step in the last two iterations of the fine calibration, the residue comparator offset still meets the requirements.

The coarse calibration circuit is separated for latch 1 and latch 2, while the fine calibration circuit is combined for those two time-interleaved latches. It is implemented as a current steering DAC (referred to as calibration DAC). In the calibration mode, both two latches work in the time-interleaved way, even though only one latch output is sampled and passed to the calibration logic. The reason is to keep the environment of the quantizer in the calibration mode as close as possible to the normal operation mode. So, in both calibration mode and normal operation mode, the calibration DAC input toggles between two fine codes, implemented with a multiplexer (MUX). A delayed version of the latch clock signal (clkp_{ltc}/clkn_{ltc} in Figure 8.6) is used as the select signal for the multiplexer.

The requirement of the full swing and steps of the coarse and the fine calibration is as follows. In the worst case, the full swing of the coarse calibration should cover all the possible cases of the comparator offset (for a coverage of more than $\pm 6\sigma$). The full swing of the fine calibration should be larger than the largest coarse calibration step (the coarse calibration circuit can have different step size due to its own mismatch). And the largest fine calibration step should be less than the calibration accuracy required by the system (the calibration DAC may have different step size due to its own mismatch).

The flowchart on the operation principle of the current-mode locally-TI multi-bit quantizer and offset calibration, including both the calibration mode and the normal operation mode, is presented in Figure 8.11.

8.2.3 Circuit implementation

The transistor-level circuit implementation of an SDM with the proposed comparator offset calibration is shown in Figure 8.12. It shows one slice of the multi-bit quantizer in detail. In the following, only the additional circuit and functions compared to Figure 8.6 are explained in detail. They are used for the offset calibration.

The coarse calibration circuit is implemented as an array of small PMOS transistors, in parallel with the PMOS transistor of the latch. Their gates are connected to a series of control signals (ctrl1, ctrl2, ..., ctrln). E.g., when the control signal ctrl1 is the same as the clock signal of the latch clkp_{ltc}, the small PMOS transistor M_{33} is offering a certain amount of current at the same time of M_{17}. Thus, it implements a coarse step for the offset calibration. When ctrl1 is VDD (1.1 V), the PMOS transistor M_{33} is always OFF. The elements of coarse calibration circuit can be either unary weighted or binary weighted, or a combination of both (segmented into a unary part and a binary part). A unary weighted coarse calibration circuit is intrinsically monotonic.

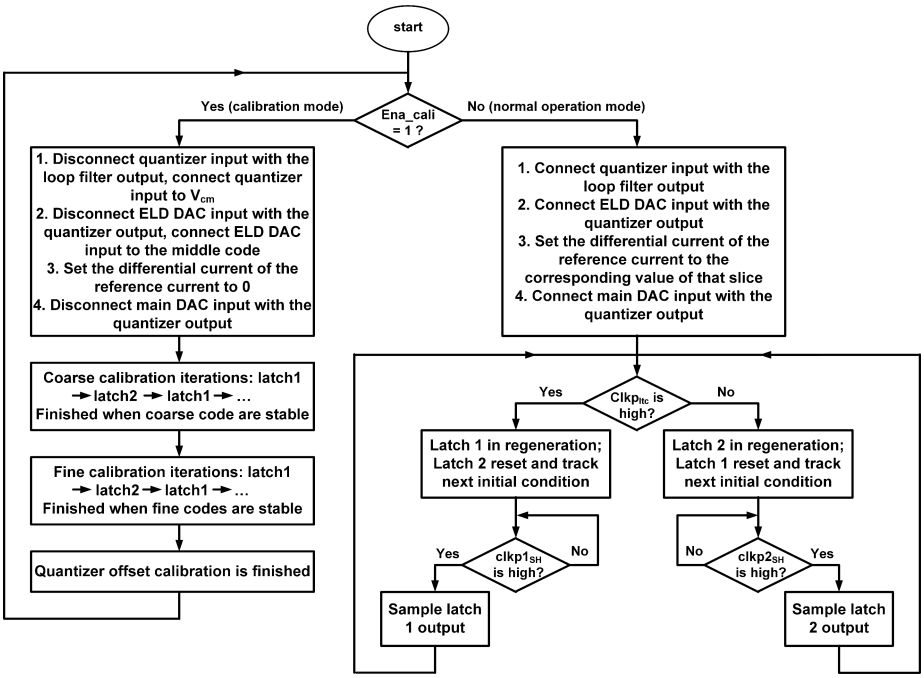


Figure 8.11: Flowchart of locally time-interleaved comparators and offset calibration.

The fine calibration circuit is implemented as a current steering DAC (referred to as calibration DAC), similar as the ELD DAC. The unit DAC elements can be either unary weighted or binary weighted, or a combination of both (segmented into a unary part and a binary part).

The calibration mode and the normal operation mode are defined by the master control of the SDM. The control signals from the master control are shown as green lines. The master control has three functions. First, it controls the switches between the loop filter and the quantizer, and between the sampled quantizer output and the main DACs. Second, it controls the input digital code of the reference DACs. E.g., for a 3-bit quantizer, the input codes of the reference DACs are all 0 (middle code) during the calibration mode. While those codes are -3, -2, -1, 0, 1, 2, 3, respectively during the normal operation mode. Third, it controls the exact calibration procedure. With two control signals (named "coarse_not_fine_cali" and "latch1_not_latch2_cali"), it defines 4 calibration modes – coarse calibration latch 1, coarse calibration latch 2, fine calibration latch 1 and fine calibration latch 2.

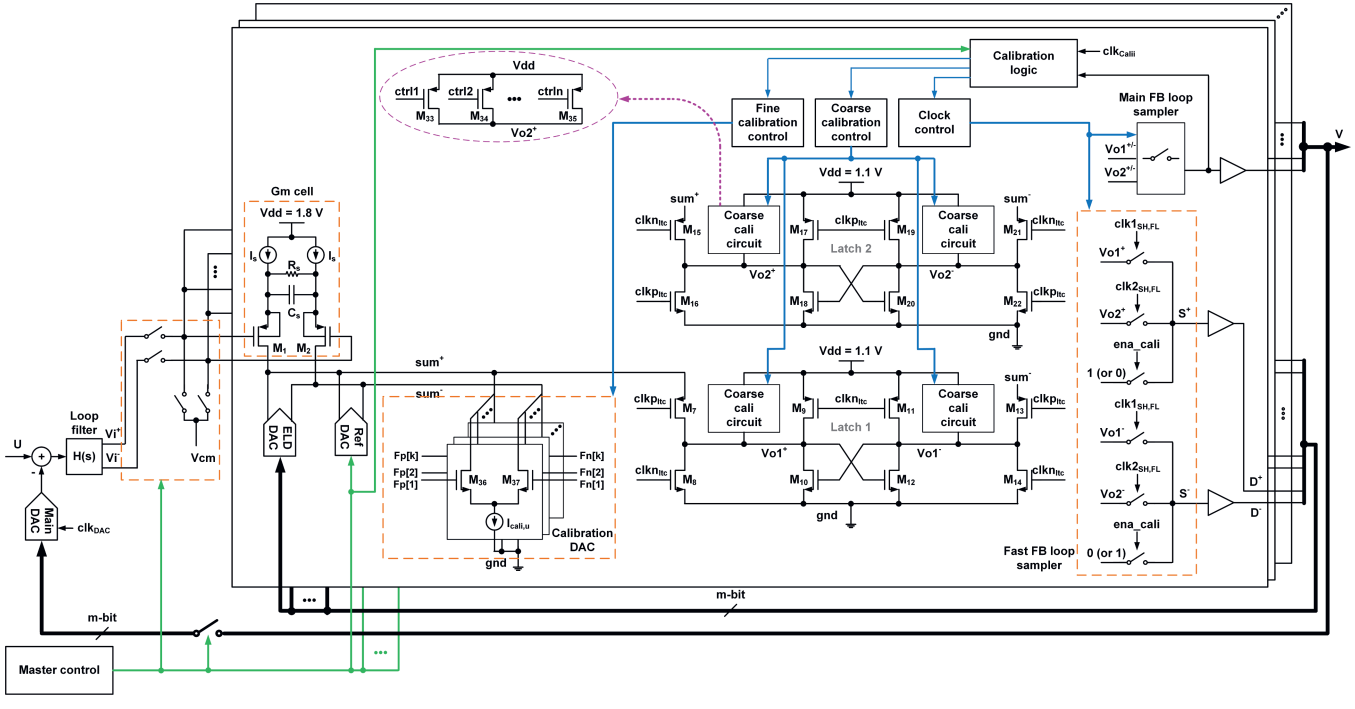


Figure 8.12: Proposed schematics of the SDM with current mode multi-path ELD compensation, locally-TI multi-bit quantizer, and comparator offset calibration circuits.

In the calibration mode, the local calibration logic block in every 1-bit slice generates and stores some control signals. It also generates and stores coarse code 1/2 and fine code 1/2 during both calibration mode and normal operation mode. The calibration logic block is a digital circuit, which is integrated on chip. It controls three analog blocks – coarse calibration control, fine calibration control, and clock control block.

The latch output samplers for the fast feedback loop (ELD compensation loop) and the main feedback loop are separated. The fast feedback loop sampler is shown in more detail in Figure 8.12. When the SDM is in the calibration mode, the control signal ena_cali is high; otherwise, when the SDM is in the normal operation mode, ena_cali is low. In the calibration mode, the sampling clocks $\text{clk1}_{SH,FL}$ and $\text{clk2}_{SH,FL}$ are disabled by the clock control block. The switches controlled by the ena_cali are ON, and the fast feedback loop sampler output is set to be 0 (or 1) depending on the number of the 1-bit quantizer slice. For half of the total amount of the 1-bit quantizer slices, the fast feedback loop sampler outputs are set to 1, while for the other half they are set to 0. These sampler outputs are transferred to the ELD DACs. Thus, a middle code is generated as the ELD DAC input during the calibration mode. Notice that if the number of the unit ELD DACs per slice is not an even number, one extra unit ELD DAC is required to generate a zero differential output current from the ELD DAC.

The main feedback loop sampler is implemented similarly as the fast feedback loop sampler. The difference is that the switches controlled by ena_cali are not needed in the main feedback loop sampler. It requires two sampling clocks – $\text{clk1}_{SH,ML}$ and $\text{clk2}_{SH,ML}$. In the normal operation mode, $\text{clk1}_{SH,ML}/\text{clk2}_{SH,ML}$ and $\text{clk1}_{SH,FL}/\text{clk2}_{SH,FL}$ are the same, which are shown as $\text{clk1}_{SH}/\text{clk2}_{SH}$ in Figure 8.6 (only the positive clock signals are shown in Figure 8.7 as $\text{clkp1}_{SH}/\text{clkp2}_{SH}$). In the calibration mode, $\text{clk1}_{SH,ML}/\text{clk2}_{SH,ML}$ and $\text{clk1}_{SH,FL}/\text{clk2}_{SH,FL}$ are different, since the main feedback loop sampler's output is passed to the calibration logic blocks as an input. When latch 1 is under calibration (either coarse calibration or fine calibration), only latch 1 output is sampled and passed to the calibration logic, while latch 2 output is not sampled. In this case, a control signal named ena_cali_latch1 is high. And only $\text{clk1}_{SH,ML}$ is enabled (the same as in the normal operation mode), while the $\text{clk2}_{SH,ML}$ is disabled. Similarly, when latch 2 is under calibration (either coarse calibration or fine calibration), only latch 2 output is sampled and passed to the calibration logic, while latch 1 output is not sampled. In this case, a control signal named ena_cali_latch2 is high. And only $\text{clk2}_{SH,ML}$ is enabled (the same as in the normal operation mode), while the $\text{clk1}_{SH,ML}$ is disabled.

The coarse calibration control circuit is shown in Figure 8.13. The coarse calibration control circuit for latch 2 is taken as an example, while the circuit for latch 1 can be designed similarly, by just switching clkp and clkn. The output ctrl is one of the control signals ctrl1, ctrl2, ..., ctrln in Figure 8.12. The function of this block is as follows. When the corresponding bit of coarse code 1/2 (code_P in Figure 8.13) is 1 (logic high, 1.1 V), its output (ctrl) should be the same as clkp_{ltc}. In this case, the transistors M_1 and M_4 are ON, such that the inverter composed of M_2 and M_3

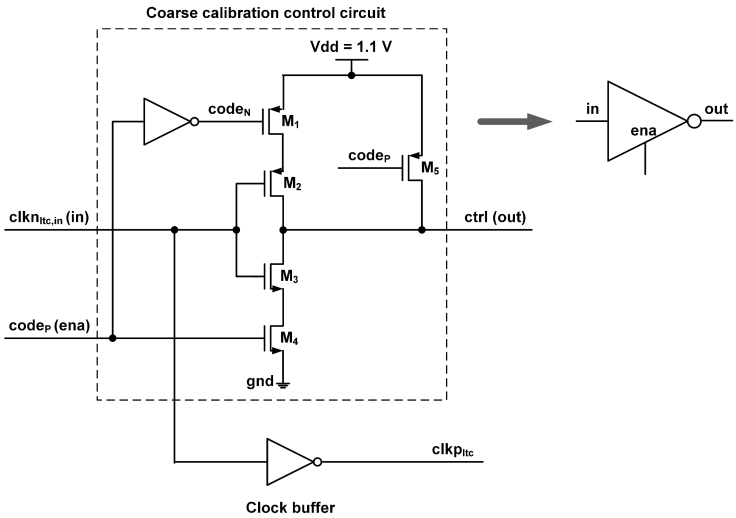


Figure 8.13: Coarse calibration control circuit for latch 2.

is working. The coarse calibration control circuit should be designed to have the same delay as the clock buffer. When code$_P$ is 0, the output of the coarse calibration control circuit should be VDD. In this case, the transistors M_1 and M_4 are OFF, and the inverter composed of M_2 and M_3 is not working. The transistor M_5 is ON, and it drives the ctrl node to VDD.

Actually, the coarse calibration control circuit can be considered as an inverter with an enable signal. Its symbol is defined in Figure 8.13. It has two inputs (in, ena) and one output (out). In Figure 8.13, in = clkn$_{ltc,in}$, ena = code$_P$, and out = ctrl. This inverter with an enable signal is also used in the clock control block.

The fine calibration control circuit is shown in Figure 8.14. This circuit works as a multiplexer. Delayed version of the latch clocks (clkp$_{ltc,d}$ and clkn$_{ltc,d}$) are used as the select signal for the multiplexer. The multiplexer function is achieved by using two pass gates (M_1 – M_4). The multiplexer output is further delayed and buffered with several inverters. In this design, the total delay from clkp$_{ltc}$ /clkn$_{ltc}$ to Fp/Fn is about 25% of the period of clkp$_{ltc}$ /clkn$_{ltc}$ (this delay is equivalent to half of the SDM sampling period T_S). The outputs Fp/Fn are one pair of the calibration DAC differential input signals Fp[1]/Fn[1], Fp[2]/Fn[2], ..., Fp[k]/Fn[k] in Figure 8.12.

The clock control circuit is shown in Figure 8.15. This circuit enables or disables the samplers' clock, clk1$_{SH,ML}$/clk2$_{SH,ML}$ and clk1$_{SH,FL}$/clk2$_{SH,FL}$, depending on the calibration procedure. The inverter with an enable signal shown in Figure 8.13 is reused here. Notice that clkn1$_{SH,ML}$, clkn2$_{SH,ML}$, clkn1$_{SH,FL}$ and clkn2$_{SH,FL}$ are the gate voltages of the PMOS transistors in the pass gates of the samplers, and clkp1$_{SH,ML}$, clkp2$_{SH,ML}$, clkp1$_{SH,FL}$ and clkp2$_{SH,FL}$ are the gate voltages of the NMOS transistors

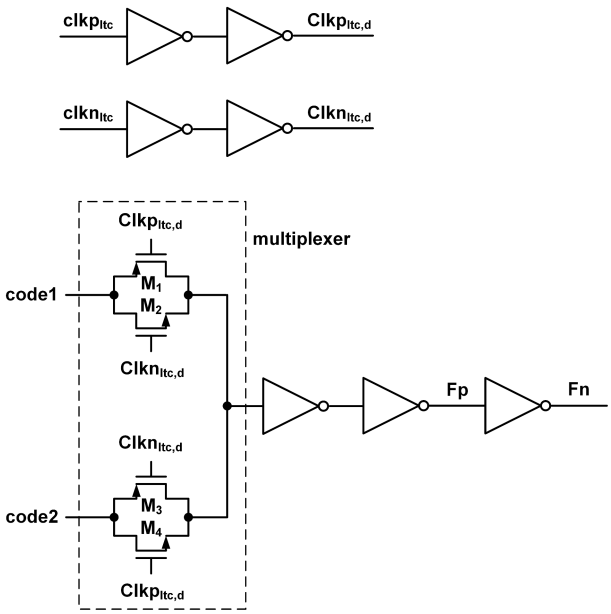


Figure 8.14: Fine calibration control circuit.

in the pass gates of the samplers, as shown in Figure 8.6. When the corresponding sampling clock is disabled, $\text{clkn1}_{SH,ML}$/$\text{clkn2}_{SH,ML}$/$\text{clkn1}_{SH,FL}$/$\text{clkn2}_{SH,FL}$ should be set to VDD (1.1 V), while $\text{clkp1}_{SH,ML}$/$\text{clkp2}_{SH,ML}$/$\text{clkp1}_{SH,FL}$/$\text{clkp2}_{SH,FL}$ should be set to GND (0 V).

The operation principle of the clock control circuit is as follows. When the SDM is in the normal operation mode, the control signals ena_cali, ena_cali_latch1 and ena_cali_latch2 are all logic low (0 V). Thus, all of the inverters with enable signals are working as normal inverters, and all of the sampling clock signals are enabled. When the SDM is in the calibration mode, ena_cali is logic high (1.1 V), and the fast feedback loop sampler's clock $\text{clk1}_{SH,FL}$/$\text{clk2}_{SH,FL}$ are disabled – $\text{clkn1}_{SH,FL}$/$\text{clkn2}_{SH,FL}$ are set to logic high (1.1 V), and $\text{clkp1}_{SH,FL}$/$\text{clkp2}_{SH,FL}$ are set to logic low (0 V). In the calibration mode, when latch 1 is under calibration (either coarse or fine calibration), ena_cali_latch1 is logic high, and the main feedback loop sampler's clock for latch 2 $\text{clk2}_{SH,ML}$ is disabled – $\text{clkn2}_{SH,ML}$ is set to logic high (1.1 V), and $\text{clkp2}_{SH,ML}$ are set to logic low (0 V). Thus, only latch 1 output is sampled by the main feedback loop sampler, and passed to the calibration logic block. Similarly, when latch 2 is under calibration (either coarse or fine calibration), ena_cali_latch2 is logic high, and the main feedback loop sampler's clock for latch 1 $\text{clk1}_{SH,ML}$ is disabled – $\text{clkn1}_{SH,ML}$ is set to logic high (1.1 V), and $\text{clkp1}_{SH,ML}$ are set to logic low (0 V).

Figure 8.16 shows the clock and control signals during the calibration mode. A part of the coarse calibration for latch 1 is shown as an example. In this case, ena_cali_latch1

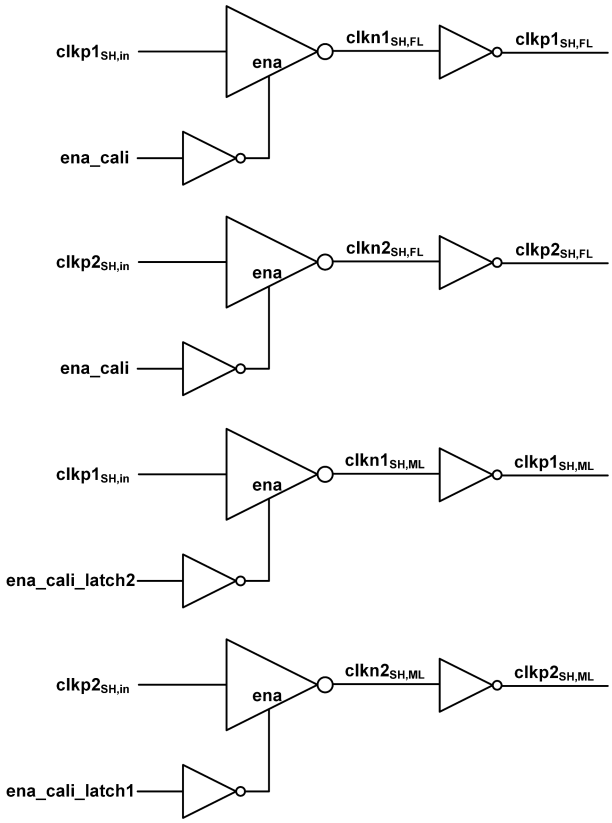


Figure 8.15: Clock control circuit.

is 1. Since only the DC offset needs to be calibrated, the calibration clock clk_{Cali} is designed to be at much lower frequency than the latch clock clkp_{ltc}. In the test chip, the calibration clock has a frequency 1024× lower than the sampling rate of the SDM. Although the calibration clock clk_{Cali} is at a much lower frequency, the latch clock $\text{clkp}_{ltc}/\text{clkn}_{ltc}$ is at the same frequency as the normal operation mode. Thus, any dynamic effects of the comparator offset which depends on the SDM's sampling rate are as far as possible preserved in the calibration mode. The calibration codes change at the negative clock edge of the calibration clock clk_{Cali}, while the sampled latch output is re-sampled by the calibration logic at the positive clock edge of clk_{Cali}. Thus, when one new calibration code is applied, the latch under calibration has many clock periods to stabilize the output, before the latch output is sampled by the calibration logic. In the calibration mode, the latch clock is the same as in the normal operation mode, while the sampler's clocks for the fast feedback loop $\text{clkp1}_{SH,FL}$ and $\text{clkp2}_{SH,FL}$ are disabled. When latch 1 is under calibration, the sampler's clock for the main feedback loop of latch 2 $\text{clkp2}_{SH,ML}$ is disabled, and vice versa.

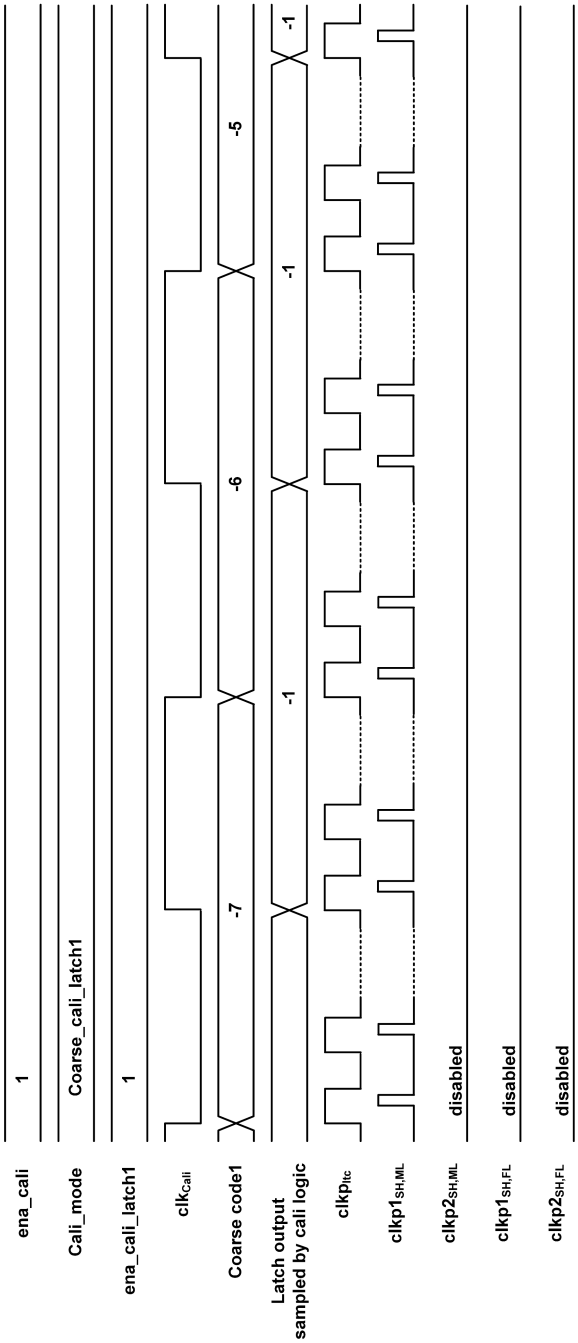


Figure 8.16: Clock and control signals during the calibration mode.

8.2.4 Simulation results

Transistor-level Monte-Carlo simulations with device mismatch are performed to verify the effectiveness of the proposed comparator offset calibration technique. Monte-Carlo simulations show that after calibration the maximal residue offset is about 0.12 LSB of the 3-bit quantizer. After calibration, the original SNDR of the ADC without device mismatch is restored.

The proposed comparator offset calibration has been implemented on the test chip. The area of the 'calibration logic' in Figure 8.12 is 2030 μm^2. The comparator offset calibration is run at the start-up, while the voltage and the temperature during the calibration mode should be as close as possible to the normal operation mode. Measurement results on the offset calibration are presented in Chapter 11, validating its effectiveness. In many applications, e.g. automotive radar, the operation of the receiver is duty-cycled – it has an ON time and an OFF time. The OFF time of the receiver can be used to run a foreground calibration, to track the temperature change.

8.2.5 Conclusions

This section proposes an on-chip comparator offset calibration technique for broadband CT $\Sigma\Delta$ ADCs with current-mode multi-path ELD compensation and locally-TI multi-bit quantizer. A two-step coarse-fine calibration is designed to achieve the required calibration range and accuracy. The calibrations for the locally-TI comparator latches are not independent, and hence iterations of coarse calibrations and fine calibrations of the TI comparators are required. Simulation results show that after the proposed calibration the input-referred comparator offset is reduced from 9 LSB (3σ) to 0.12 LSB. With the proposed calibration, the comparator offset requirement for the multi-bit quantizer is achieved, which achieves higher speed and better power efficiency than the approach of intrinsic matching. The proposed offset calibration guarantees the required linearity of the multi-bit quantizer with the current-mode multi-path ELD compensation and the locally-TI multi-bit quantizer techniques, and enables broadband CT $\Sigma\Delta$ ADC applications.

8.3 Conclusions

This chapter proposes two techniques for high-speed comparators in broadband CT $\Sigma\Delta$ ADC. A current-mode locally-time-interleaved multi-bit quantizer moves the reset time and the time to track the next initial condition of the comparator out of the 1 T_S ELD time budget, enabling 1.33× higher ADC sampling rate and signal BW. Compared to the voltage-mode globally-TI quantizer, the proposed current-mode locally-TI quantizer reduces the parasitic capacitance seen by the TI switches, reducing the settling time of comparator input and relaxing the R_{ON} requirement of the TI

switches. An on-chip two-step coarse-fine comparator offset calibration is proposed for broadband CT $\Sigma\Delta$ ADCs with the current-mode multi-path ELD compensation and the locally-TI multi-bit quantizers. With the proposed offset calibration, the input-referred comparator offset is reduced from 9 LSB (3σ) to 0.12 LSB. Both approaches together enable broadband CT $\Sigma\Delta$ ADCs with multi-bit quantization.

Chapter 9

DAC linearization techniques

Mismatch between the unit elements in the multi-bit DAC is often limiting the linearity of the ΣΔ ADCs with multi-bit quantization. Many linearization techniques for high-linearity DACs are proposed in the literature, such as sorting, data weighted averaging and randomization. However in the conventional way of implementing the DAC linearization techniques, it often increases the delay in the feedback loop, which limits the sampling rate and bandwidth of the ADC. This chapter proposes a novel implementation of the DAC linearization techniques by changing the reference codes of the multi-bit quantizer. It adds minimal to no delay in the feedback loop of the ΣΔ modulator, depending on the chosen DAC linearization technique, which is beneficial for high-speed ΣΔ ADC applications. The mapping engine is implemented in the digital domain, whose non-idealities do not interfere with the analog purity of the reference signal. It is a general purpose architecture which offers the flexibility to implement different static and dynamic DAC linearization techniques.

9.1 Introduction

Chapter 4.3 describes that mismatch between the unit DAC cells in multi-bit DACs generates non-linearity. The mismatch between the unit DAC cells creates randomly distributed errors. DAC mismatch can limit the DR and linearity performance of broadband CT ΣΔ ADCs with multi-bit quantization. Generally, the problem caused by the DAC mismatch can be mitigated in two ways – (1) by intrinsic matching (2) by calibration.

Many broadband multi-bit ΣΔ ADCs achieve the DAC linearity requirement by intrinsic matching [30]. By sizing up the matching-critical devices and careful layout (e.g. applying the common-centroid technique), a certain matching requirement can be achieved [71].

Various DAC calibration techniques can be found in the literature [90]. The static

error on the current sources of each unit DAC cell can be calibrated [91, 16]. In [66], the DAC mismatch error for every input bit is estimated and an auxiliary DAC is applied to compensate the DAC error in the analog domain. After the DAC mismatch error is estimated, it can also be compensated in the digital domain [65, 67]. When the mismatch error of every unit DAC cell is estimated, a certain sorting/mapping on the order of the unit DAC cells can be calculated by an algorithm, and the multi-bit DAC after sorting/mapping can achieve better (overall) linearity performance than with the default order [92, 64]. With sorting, the errors on the DAC unit elements mutually cancel each other, and the integral non-linearity (INL) of the DAC is improved. The overall linearity of the multi-bit SDM can be improved by switching/shuffling schemes as well, for example dynamic element matching (DEM) [93], data weighted averaging (DWA) [94, 95, 88, 96], element rotation [97]. With DWA and DEM, the power of the harmonic distortion is transformed to noise by randomizing the error. So THD improves but the noise deteriorates. Noise shaping and a relatively high OSR (typically ≥ 16) are required to reduce the noise penalty.

Besides various DAC linearization algorithms, different implementation of the DAC linearization algorithms can be found in the literature as well. This chapter assumes a 'mapping engine' is used to implement any of the above mentioned DAC sorting/mapping/switching techniques [64]. In $\Sigma\Delta$ ADCs, the mapping engine can be implemented as a switching matrix controlled by the logic [93, 96, 97, 88]. Traditionally, the mapping engine is implemented between the quantizers and the DACs in $\Sigma\Delta$ ADCs [93, 96]. In the state-of-the-art broadband CT $\Sigma\Delta$ ADCs, the mapping engine is implemented between the multi-bit quantizer's reference and the quantizer, to eliminate the delay of the mapping engine in the SDM feedback loop [97, 88]. These two alternative implementations are discussed in detail in the next section.

9.2 State-of-the-art implementations of DAC linearization techniques

Figure 9.1 shows the conventional implementation of DAC linearization techniques in multi-bit SDMs, with the mapping engine between the quantizer and the DAC [93, 96]. Here, the DAC linearization techniques can be sorting/mapping, DWA, randomized DWA, DEM, randomization, etc. In Figure 9.1, the mismatch sensor measures the static and/or dynamic mismatch between the unit elements of the main DAC [64]. A certain sorting, mapping or switching algorithm is implemented in the logic block. The required switches are implemented in the mapping engine. Here, τ_1 is the delay of the multi-bit quantizer, and τ_2 is the delay of the mapping engine.

The disadvantages of the conventional implementation shown in Figure 9.1 is that the mapping engine which implements the switches required by the DAC linearization techniques is in the feedback loop of the SDM. It adds capacitive and resistive load, and adds delay (τ_2) in the feedback loop. The extra delay caused by the mapping

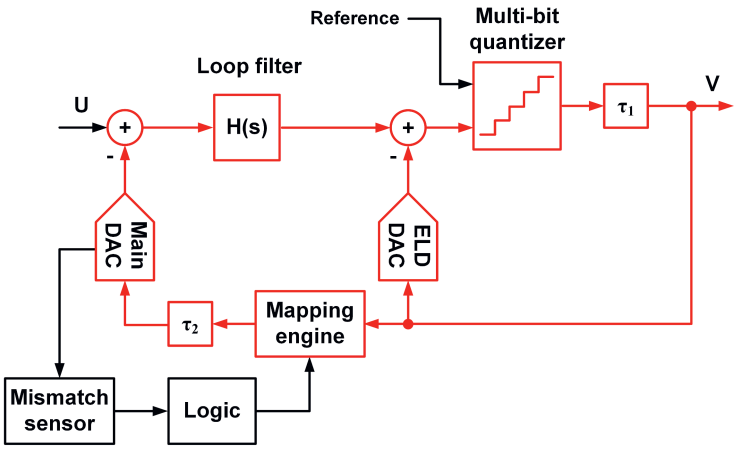


Figure 9.1: Conventional implementation of DAC linearization techniques in SDMs with the mapping engine between the quantizer and the DAC.

engine can negatively impact the performance of the SDM, or even make it unstable, especially in very high-speed SDMs with several GHz sampling rate [97]. In Figure 9.1 the red part of the figure shows the feedback loops of the SDM, which are speed critical and sensitive to extra delay.

In very high-speed multi-bit SDMs with several GHz sampling rate, the multi-bit quantizer is commonly implemented as a flash sub-ADC, since the latency of the quantizer contributes to the total ELD and flash ADCs have a low latency. This flash ADC compares the input signal with a series of references (reference voltages or reference currents). The unit 1-bit comparators in the flash ADC (multi-bit quantizer) and the unit elements in the main DAC are typically one-to-one connected through some connection circuitry, e.g. samplers, buffers, D-flipflops. In this case, instead of putting the mapping engine between the quantizer and the main DAC, the mapping engine can be inserted between the reference and the multi-bit quantizer (flash sub-ADC). By sorting/mapping/switching the reference among the unit 1-bit comparators, an effective sorting/mapping/switching of the unit elements of the DAC is achieved. The simplified block diagram of this implementation is shown in Figure 9.2 [97, 88]. The resistor ladder in [88] is considered as an implementation of the reference DAC, which delivers the required reference voltages. The mapping engine might need the quantizer output V or not, depending on the particular DAC linearization technique which needs to be implemented. In this implementation, the delay of the mapping engine is moved out from the SDM's feedback loops.

In the state-of-the-art implementation in Figure 9.2, the mapping engine is implemented in the analog domain, which has two disadvantages. First, the mapping engine typically contains some switches, and the non-idealities of the mapping engine (switches) interfere with the analog purity of the reference signal. For example, the

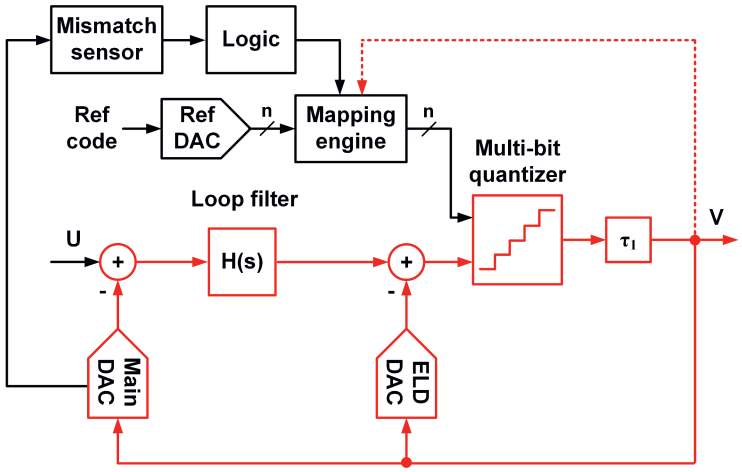


Figure 9.2: State-of-the-art implementation of DAC linearization techniques in SDMs with the mapping engine between the quantizer's reference DAC and the quantizer.

mapping engine adds load to the output of the reference DAC, which increases the time constant during the switching. Another example is that the mismatch of the switches contributes to the offset of the reference signal. Second, since the mapping engine is implemented in the analog domain, it is not flexible to switch to different DAC linearization techniques. In the next section, a new implementation of the DAC linearization techniques is proposed, where the mapping engine is moved to the digital domain to overcome the aforementioned limitations.

9.3 Proposed implementation of DAC linearization techniques

Figure 9.3 shows the proposed implementation of DAC linearization techniques, where the mapping engine is moved to the digital domain. For a $(n+1)$-level quantizer, the reference DAC is copied n times. The mapping engine is inserted between the reference DACs and their input codes (reference codes). By sorting/mapping/switching of the reference codes, a sorting/mapping/switching on the outputs of the reference DACs are achieved. When a voltage-mode multi-bit quantizer is considered, even if the reference DAC with voltage output (e.g. a resistor ladder) is copied n times, switches in the analog domain connecting different reference voltage levels to the multi-bit quantizer are still required to implement the mapping engine, which shows no extra benefits compared to Figure 9.2. However, when a current-mode multi-bit quantizer is considered, the duplication of the reference DACs with current output allows eliminating the switches at the DAC output in the analog domain and moving

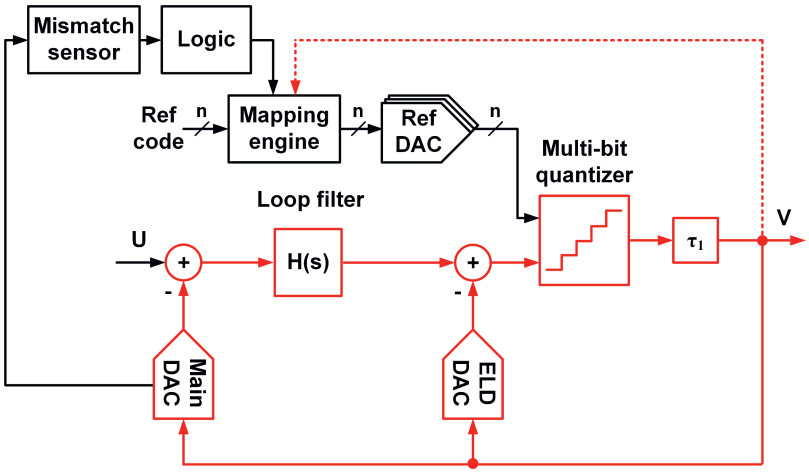


Figure 9.3: Proposed implementation of DAC linearization techniques in SDMs with the mapping engine between the reference code and the reference DAC.

the mapping engine completely into the digital domain. This is elaborated in the following with Figure 9.4 and Figure 9.5.

In the current-mode multi-path ELD compensation proposed in Chapter 7.2, a current-mode quantizer with duplicated reference DACs already exists. The system architecture shown in Figure 7.9 can be used to implement DAC linearization techniques in an efficient way, suitable for high-speed operation. Figure 9.4 shows one of the proposed SDM architectures with a current-mode quantizer and DAC linearization techniques that do not need the quantizer output. Here, a $(n+1)$-level quantizer is shown as an example. It contains n slices of a 1-bit comparator (latch), a $(n+1)$-level ELD DAC, a n-level reference DAC, a gm-cell and a current summation node. The reference DAC (Ref DAC) converts the reference code (Ref code) into a reference current. The $(n+1)$-level quantizer has n reference codes, which are {code 1, code 2, ..., code n}. The mapping engine connects the inputs {code 1, code 2, ..., code n} to the outputs {ref code 1, ref code 2, ..., ref code n} with a chosen order. Thus, a certain sorting/mapping/switching can be implemented.

Two main classes of the DAC linearization techniques can be distinguished that do not need the information of the quantizer output. First, it can be a static sorting/mapping technique [64]. In this case, with the measured information on the static and dynamic mismatch of the DAC unit elements, a certain optimal order of the DAC unit elements is calculated by the logic. This order of the DAC unit elements is fixed during the operation of the SDM. The mapping engine just needs to implement a fixed connection with a certain optimal order between the input codes and the output codes. In this case, as the mapping engine is not switched during the operation of the SDM, its delay has no impact on the operation of the SDM.

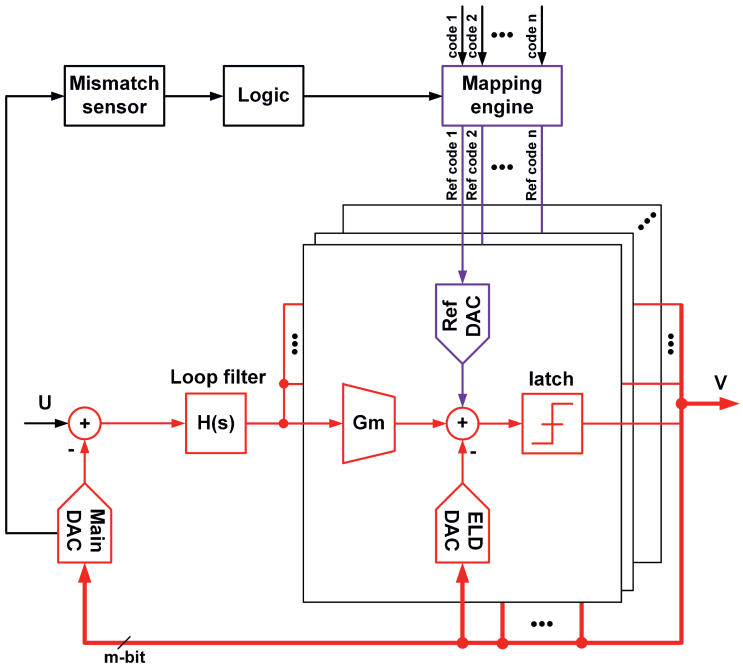


Figure 9.4: Proposed SDM architecture with a current-mode quantizer and DAC linearization techniques that do not need the quantizer output.

Second, the DAC linearization technique can also be a dynamic switching technique, for example a randomization technique. In this example, the order of the DAC unit elements is randomly switched during the operation of the SDM. After each switching, the reference DAC output current and the comparator input should be settled before the next sampling moment of the comparator. Thus, the total delay of the mapping engine and the reference DAC should be within one sampling clock period of the SDM.

The previous examples show architectures for SDMs that use linearization techniques that do not need the information of the DAC input. Some linearization techniques, however, do need this information, like DWA and randomized DWA. For those techniques this chapter proposes the architecture shown in Figure 9.5. The quantizer output V, which is the same as the DAC input, is now also an input of the mapping engine.

The mapping engine is part of a feedback loop now, and its switching speed is critical, like in the conventional implementation shown in Figure 9.1. Therefore it is shown in red in Figure 9.5 as well. However, the proposed implementation in Figure 9.5 still shows advantages compared to the conventional implementation, which are elaborated in the following. The main feedback loop of the SDM and the DAC linearization

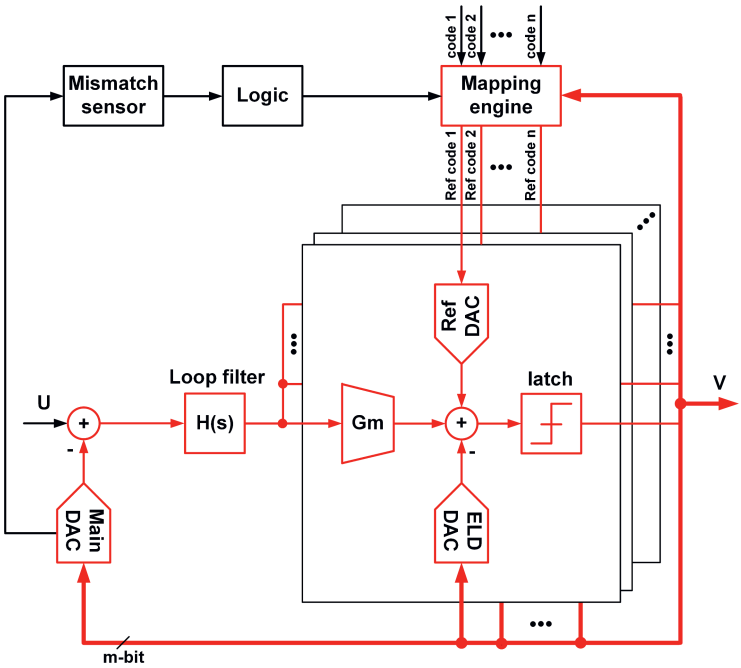


Figure 9.5: Proposed SDM architecture with a current-mode quantizer and DAC linearization techniques which need the quantizer output.

loop are (partially) decoupled. The DAC linearization loop contains the comparator (latch), mapping engine, reference DAC and the ELD summation node. The SDM main feedback loop contains the comparator (latch), main DAC, loop filter, Gm cell and ELD summation node. Thus, the SDM main feedback loop and the DAC linearization loop can be optimized separately for their different requirements. For example, the main DAC typically has a stringent noise and matching requirement. Thus, the unit element of the main DAC typically has a relatively large current (for lower thermal noise) and a relatively large area (for better matching and lower flicker noise). The reference DAC in the multi-bit quantizer typically has a relaxed noise and matching requirement compared to the main DAC, as the noise and non-linearity contributed by the reference DAC is shaped by the NTF. Thus, it can be beneficial to insert the mapping engine between the comparator and the reference DAC, compared to the conventional approach where the mapping engine is inserted between the comparator and the main DAC.

In Figure 9.5 the red part of the figure shows the main feedback loop, the ELD feedback loop and the DAC linearization loop of the SDM. The total delay of the DAC linearization loop should be maximally one sampling clock period. The total delay of the main feedback loop and the ELD feedback loop should be both maximally

one sampling clock period as well. The ELD DAC and the reference DAC can be implemented similarly (see Figure 9.6), which means they have a similar delay. It is essential to minimize the delay of the mapping engine in this scenario for high-speed $\Sigma\Delta$ ADC applications.

The proposed implementation in Figure 9.3, 9.4 and 9.5 have two advantages compared to the state-of-the-art implementation in Figure 9.2. First, the mapping engine is moved to the digital domain, and the analog purity of the reference signal is not interfered by the non-idealities of the mapping engine. Second, since the logic and the mapping engine are in the digital domain, it is a general purpose implementation and it offers the flexibility to switch to different DAC linearization techniques easily. A concern of the proposed implementation is that when a switching technique (e.g. DWA, DEM, randomization, rotation) is used, the reference DAC is in the switching path, and thus the delay of the reference DAC adds to the total delay of the path. The delay of the reference DAC is not a concern when a static sorting/mapping technique is used. A drawback of the proposed implementation is that the number of the reference DACs is increased.

Notice that the proposed approach is not capable to implement all the existing DAC linearization techniques. The proposed approach (Figure 9.5) cannot select the unit elements of the main DAC based on the current sample of the quantizer output. It can only select the order of the unit elements of the main DAC to be used based on the previous sample of the quantizer output.

Notice also that some block(s) shown in Figure 9.3, Figure 9.4 and Figure 9.5 maybe not necessary and hence omitted in certain applications. For example, some switching algorithms of the DAC unit elements (DWA, DEM, random switching, etc.) do not need the information on the mismatch of the DAC unit elements. Thus, the mismatch sensor can be omitted in those cases.

Finally, by sorting/mapping/switching of the reference code of the quantizer, the quantizer can be linearized as well. For a linearization technique which requires the information on the mismatch, e.g. a static sorting [64], a mismatch sensor which measures the mismatch information of the quantizer is needed. For a linearization technique which does not need the information on the mismatch, e.g. DWA or DEM, a mismatch sensor is not needed. By applying DWA or DEM, the quantizer mismatch is randomized and converted into noise.

This approach works on all the errors originating from the quantizer and the DAC in the $\Sigma\Delta$ loop. It can be achieved in two ways. (1) Mismatch sensors can be applied to measure the mismatch information on both the DAC and the quantizer. This information is used by a static or dynamic linearization technique to achieve the optimal performance of the $\Sigma\Delta$ loop. (2) The logic can determine an optimal sorting/mapping/switching with a static or dynamic linearization technique based on the overall performance of the $\Sigma\Delta$ loop, e.g. in-band noise, SNDR, THD. Thus, the errors originating from both the quantizer and the DAC are taken into account for

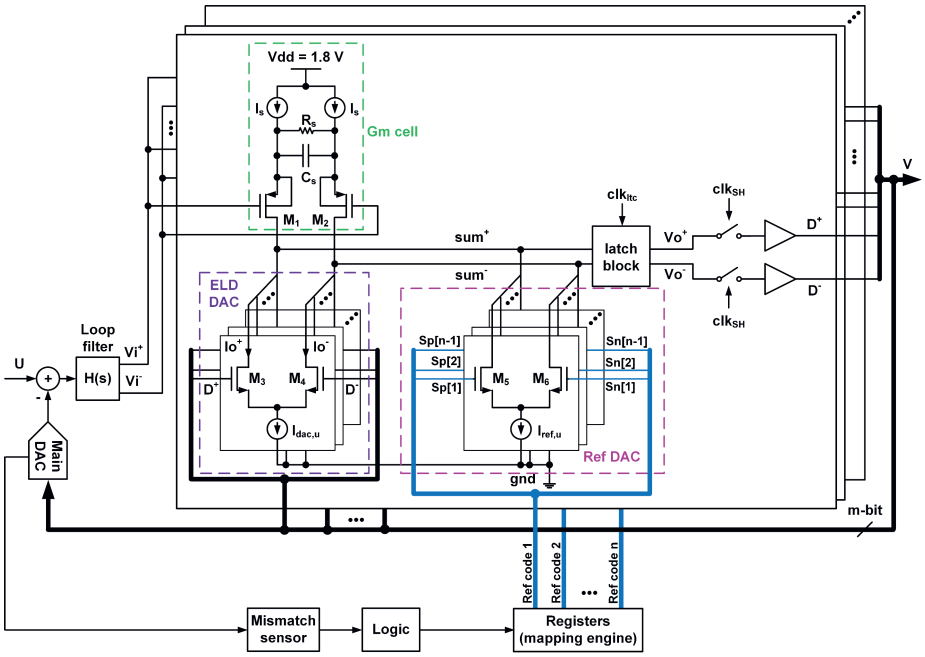


Figure 9.6: Exemplary schematic implementation of an SDM with a DAC linearization technique that does not need the quantizer output.

an optimal overall performance of the ΣΔ loop.

9.4 Circuit implementation

Figure 9.6 shows an exemplary schematic implementation of an SDM with a DAC linearization technique that does not need the quantizer output. It is a schematic implementation of the system in Figure 9.4. It shows one slice of the duplicated ELD compensation loop and 1-bit comparator in detail. This figure assumes the SDM uses $(n+1)$-level quantization. So the SDM has totally n slices of duplicated ELD compensation loop and 1-bit comparator. The circuit implementation of the Gm cell, ELD DAC, latch block, samplers and buffers have been described in Chapter 7.2 (similar as in Figure 7.10).

The NMOS transistors M_5 – M_6 and current sources $I_{ref,u}$ compose a unit reference DAC (Ref DAC). The reference DAC converts a digital input code (reference code) into an output current. The $(n+1)$-level quantizer shown in Figure 9.6 has n reference codes – ref code 1, ref code 2, , ref code n. These n reference codes together form a permutation of the n input codes {code 1, code 2, ..., code n}. The mapping engine

applies a certain sorting/mapping/switching on the connection from the input codes {code 1, code 2, ..., code n} to its output codes {ref code 1, ref code 2, ..., ref code n}. The mapping engine is implemented in digital domain as n registers. The reference codes are saved in those registers, which can be written according to the control signal from the logic.

Since the 1-bit latch blocks are one-to-one connected to the unit elements of the main DAC through the S&H circuit and buffers, by sorting/mapping/switching of the reference code of the reference DAC, a corresponding sorting/mapping/switching of the DAC unit elements is effectively achieved. For dynamic linearization techniques (e.g. DWA, DEM, randomization, rotation), the delay of the reference DAC contributes to the total delay of the DAC linearization loop. The ELD DAC typically has about $0.5T_S$ to settle (the other $0.5T_S$).

From the circuit implementation point of view, the proposed approach shows two additional advantages compared to the state-of-the-art approach (Figure 9.2). (1) In [88], the switches which implement the mapping engine between the resistor ladder (a voltage-mode reference DAC) and the multi-bit quantizer have an ON resistance R_{ON}. When the mapping engine is switching, R_{ON} of the switches is in series with the impedance of the resistor ladder. Together with the input parasitic capacitance of the quantizer a switching time constant is defined. To achieve high-speed switching, R_{ON} of the switches and the impedance of the resistor ladder should both be small, which increases the power consumption. In the proposed approach (Figure 9.6), since a current-mode reference DAC is used, the R_{ON} of the switches (M_5, M_6) is in series with the current source $I_{ref,u}$, which has a large output impedance. Thus, the R_{ON} of the switches (M_5, M_6) does not determine the switching time constant, and hence the requirement on the R_{ON} of the switches is relaxed compared to the state-of-the-art approach [88]. (2) In [88], the switches (which implement the mapping engine) are working at different reference voltage levels. Thus they have different R_{ON} (and parasitic capacitance), which creates errors on the output reference voltages of the mapping engine. In the proposed approach, since a unary current-mode reference DAC is used, all the switches (M_5, M_6) are working at the same voltage level. Thus, their R_{ON} (and parasitic capacitance) are the same.

9.5 Simulation results

This section shows the simulation results of a static sorting technique as an example to demonstrate the feasibility of the proposed approach in broadband $\Sigma\Delta$ ADCs. A sorting algorithm similar as in [64] has been modelled in Matlab. In this model, a 2-1-1 MASH SDM with 3-bit quantization in every loop is considered to verify the effectiveness of the proposed technique. Normally distributed (also known as Gaussian distributed) amplitude errors have been modelled on the 7 unit elements of the 3-bit feedback DAC. The sorting algorithm is applied to the first DAC in the first stage, and uses the error information $\{\varepsilon_1, \varepsilon_2, ..., \varepsilon_7\}$ on that DAC. The sorting

algorithm is as follows:

1. The common-mode error $\frac{\sum_{n=1}^{7}\varepsilon_n}{7}$ is firstly subtracted from the error information $\{\varepsilon_1, \varepsilon_2, ..., \varepsilon_7\}$ to get $\{\varepsilon'_1, \varepsilon'_2, ..., \varepsilon'_7\}$.
2. The maximal absolute value in $\{\varepsilon'_1, \varepsilon'_2, ..., \varepsilon'_7\}$ is chosen as the 1st element after sorting. If for example ε'_3 is chosen, then $\{\varepsilon'_3\}$ is called the sorted error, and $\{\varepsilon'_1, \varepsilon'_2, \varepsilon'_4, \varepsilon'_5, \varepsilon'_6, \varepsilon'_7\}$ is called the unsorted errors.
3. From the unsorted errors, every error is added to the summation of the current sorted errors. The one which gets the minimal absolute summation result is picked as the next sorted error. This sorting scheme continues until all the errors are sorted. For example, after sorting, the sorted errors are $\{\varepsilon'_3, \varepsilon'_7, \varepsilon'_1, \varepsilon'_6, \varepsilon'_4, \varepsilon'_2, \varepsilon'_5\}$.
4. The common-mode error $\frac{\sum_{n=1}^{7}\varepsilon_n}{7}$ is added back to the sorted errors. From the previous example, the finally sorted error permutation is $\{\varepsilon_3, \varepsilon_7, \varepsilon_1, \varepsilon_6, \varepsilon_4, \varepsilon_2, \varepsilon_5\}$.

With this sorting algorithm, the original random errors are sorted to form a certain permutation, such that the errors of the unit elements are mutually partially compensated. In the majority of cases, the INL due to the differential errors is reduced after the sorting, which reduces the harmonic distortion of the SDM. This sorting algorithm is not sensitive to the common-mode error, which causes a DC offset of the SDM.

Figure 9.7 shows the simulated SNDR of 100 Monte-Carlo runs with the 3-bit DAC with normally distributed amplitude error $\sigma = 0.3\%$, before and after the sorting. The input signal is a sine wave with amplitude 0.85 V at 190 MHz. The signal bandwidth of the SDM is 600 MHz. Before applying the sorting, the SDM shows SNDR = 66.7 $\pm$ 3.3 dB ($\pm\sigma$), SNR = 73.3 $\pm$ 1.9 dB ($\pm\sigma$), THD = -68.4 $\pm$ 4.6 dB ($\pm\sigma$). After applying the sorting, the SDM shows SNDR = 70.2 $\pm$ 2.5 dB ($\pm\sigma$), SNR = 72.5 $\pm$ 1.9 dB ($\pm\sigma$), THD = -75.2 $\pm$ 4.9 dB ($\pm\sigma$). In average, the SNDR is improved by 3.5 dB, and the THD is reduced by 6.8 dB.

Figure 9.8a shows a typical output spectrum of the SDM in those 100 Monte-Carlo runs, before and after the sorting. Figure 9.8b shows the INL of the DAC before and after the sorting. Figure 9.8b shows that after applying the sorting algorithm, the maximum absolute value of INL is reduced from about $10 \cdot 10^{-3}$ to about $6 \cdot 10^{-3}$ (relative value referred to the DAC's full-scale output). Figure 9.8a shows that the HD2 is reduced from -68 dBc to -73.4 dBc, and the SNDR is increased from 67.1 dB to 70.2 dB.

Notice that the focus of this chapter is not on the optimization algorithm. The focus and contribution of this chapter is on a new implementation of the DAC linearization techniques in broadband CT $\Sigma\Delta$ ADCs, which is a general purpose architecture supporting various static and dynamic linearization techniques.

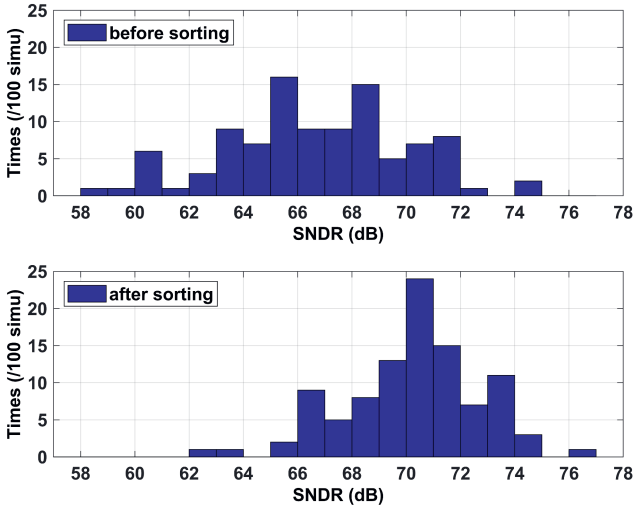
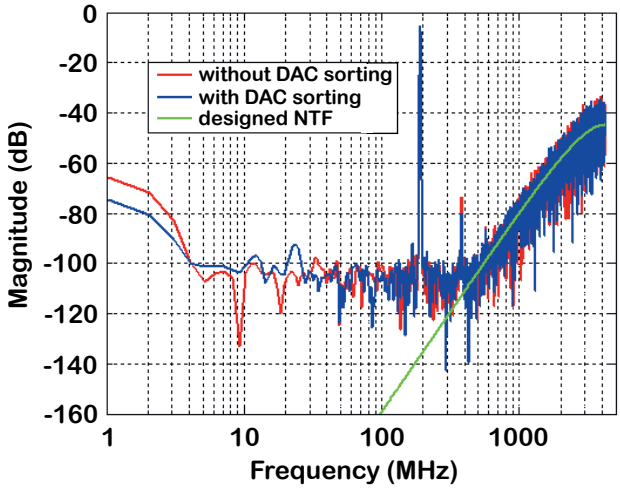


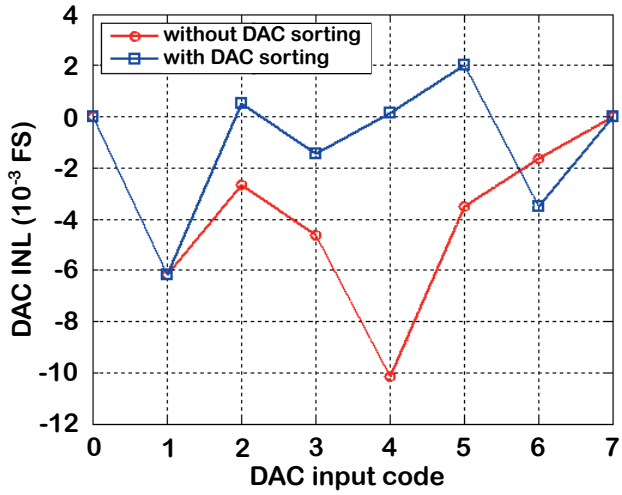
Figure 9.7: Simulated SNDR of 100 Monte-Carlo runs with 3-bit DAC with normally distributed amplitude error $\sigma = 0.3\%$, before and after 1-dimensional sorting.

9.6 Conclusions

This chapter proposes a new implementation of the DAC linearization techniques in broadband CT $\Sigma\Delta$ ADCs with the mapping engine in the digital domain. The system architecture of the current-mode multi-path ELD compensation is used to implement DAC linearization techniques by sorting/mapping/switching the input codes of the reference DACs. Since the mapping engine is in the digital domain, its non-idealities do not interfere with the analog purity of the reference signal. It is a general purpose architecture and it offers the flexibility to implement different static and dynamic DAC linearization techniques. Simulation results show that a static sorting of a 3-bit DAC improves the SNDR in average by 3.5 dB, and improves the THD in average by 6.8 dB. These properties and simulation results show the potential of the proposed approach for broadband high-linearity $\Sigma\Delta$ ADC applications.



(a)



(b)

Figure 9.8: (a) Simulated typical output spectrum of the SDM before and after sorting (b) Integral non-linearity (INL) of the DAC before and after sorting for this run.

Chapter 10

Overcoming metastability error limitations

This chapter studies the impact of metastability errors in broadband CT $\Sigma\Delta$ ADCs. Metastability errors are introduced in Chapter 4.2 and they stem from the inability of the quantizers to take decisions within the allocated time. In the beginning, Section 10.1 describes the scope of this chapter. Section 10.2 reviews the state of the art in metastability error modeling and metastability error mitigation techniques. Section 10.3 describes the error mechanism that is responsible for the impact the metastability has on the performance of CT SDMs, and proposes a more general model to describe the impact of the metastability error in CT SDMs. To overcome the metastability problem, two novel system-level solutions are proposed. Section 10.4 first proposes a metastability error compensation (MEC) technique, which measures and compensates the metastability error and restores the target SNDR. Next, Section 10.5 proposes a metastability shaping technique to shape and suppress the metastability error by the NTF, in a similar way as the quantization noise is suppressed by it [98]. With this technique, the required quantization gain can be generated in two T_S, instead of one T_S. In the end, conclusions are drawn.

10.1 Introduction

In this chapter, both a metastability error compensation technique (Section 10.4) and a metastability shaping technique (Section 10.5) are proposed and investigated at the conceptual level. The effectiveness of the proposed techniques is validated through mathematical analysis, Matlab modeling and simulations. The transistor-level implementation, test chip design and validation of these two techniques are out of the scope of this thesis because of time limitation.

This chapter takes the following assumptions in the analysis. (1) The metastability

is assumed to be caused by the limited quantization gain in the loop. All of the quantization gain in the $\Sigma\Delta$ loop is modeled in the quantizer. The DAC has no quantization gain (or its quantization gain is 1). The digital output logic of the SDM has infinite quantization gain, which is out of the $\Sigma\Delta$ loop (see Figure 10.1). (2) A linear gain model is assumed, as shown in equation (4.11). (3) Since the metastability error can be described as a stochastic effect, its probability is assumed to be independent from the quantizer offset, hysteresis and noise. Thus, the results of this chapter are also valid in the presence of these non-idealities. (4) The quantizer input is uniformly distributed in the defined input swing (-1, 1).

10.2 State of the art in metastability error modeling and mitigation

In this section the state of the art in metastability error modeling and metastability error mitigation techniques are presented. Chapter 4.2 discusses the 1-bit comparator's output characteristic with limited quantization gain in equation (4.11). Chapter 5.4 shows the simulated SNDR versus the quantization gain in Figure 5.9. When the quantizer cannot take a decision within its allocated time budget, the problem with the metastability error arises. In this case the SNDR of the SDM can significantly reduce.

10.2.1 State-of-the-art modeling of metastability error mechanism

In the literature, the variation in the zero-crossing time of the feedback DAC, caused by the metastability in the quantizer, is seen as the error mechanism that is responsible for the impact the metastability has on the performance of CT SDMs [61, 99]. In [61], the quantizer output drives the feedback DAC without re-sampling. The quantizer has shorter delay when its input is large, and it has longer delay when its input is small. Thus, in the case that the DAC input is switching, the DAC output crosses earlier when the quantizer input is larger. The limited quantization gain of the quantizer causes a variation of the DAC zero-crossing time depending on the quantizer input, which adds an unshaped error in the output spectrum of the SDM.

This thesis finds that the quantizer characteristics shown in Fig. 18 in [61] describes the quantizer metastability accurately. However, this thesis finds that the error mechanism shown in [61] (variation in the DAC zero-crossing time) is not very accurate in some cases when the metastability errors happens in broadband CT $\Sigma\Delta$ ADCs. One example is that when metastability errors occur in CT $\Sigma\Delta$ ADCs, it can happen that the DAC switches are not operating in the designed state. The designed state is that one switch is ON, and the other switch is OFF. When metastability errors

occur, it can happen that both switches are ON (as will be discussed later on, see Figure 10.2). It means that the DAC output does not settle to the desired value. This phenomenon cannot be explained by the variation in the DAC zero-crossing time. Section 10.3 presents a proposed more-general error mechanism and modeling to describe the impact of the metastability error in CT SDMs.

10.2.2 State-of-the-art metastability error mitigation techniques

In the literature, three techniques that mitigate the metastability error in broadband CT ΣΔ ADCs are:

- Applying the ELD compensation to allow typically up to 1 T_S delay in the ΣΔ loop, such that more time is available for the quantizer to generate the required quantization gain.
- Re-sampling the DAC input close to the main DAC with a low-jitter clock, to reduce the errors caused by the clock jitter, the clock skew, and the metastability error [30].
- Tapping the SDM output logic as close as possible to the main DAC input, such that the SDM output is as close as possible to the correct digital representation of the DAC output [30].

A block diagram of a state-of-the-art broadband CT SDM with the aforementioned implementation details is presented in Figure 10.1. Here, the DAC driver is composed of a sampler, and/or a buffer, and/or a D-flipflop (D-FF). The quantizer output is re-sampled by the DAC driver with a DAC clock clk_{DAC}, and clk_Q is the quantizer clock. A_{fb} is the analog feedback signal in the SDM which is the main DAC output as well. D_{out} is the digital output of the SDM.

Many more technologies are proposed in the literature to mitigate the metastability error in ΣΔ ADCs. For example, the time constant τ of the comparator core can be reduced by increasing its current (and power consumption). However, the minimal achievable time constant τ is limited by the technology (e.g. by self loading), and in that case τ cannot be further reduced even if more power is consumed. Besides, time-interleaving of the quantizer can effectively move the reset time of the quantizer out of the ELD time budget, which can maximize the available regeneration time of the comparator core [24]. The state-of-the-art technologies are limited by the available regeneration time and the achievable time constant. In this chapter, two novel techniques are proposed to overcome the metastability error limitation. A metastability error compensation technique is proposed in Section 10.4, where the principle of feedforward correction is used, and the compensation effectiveness relies on the accuracy and matching of the compensation circuit. A metastability shaping

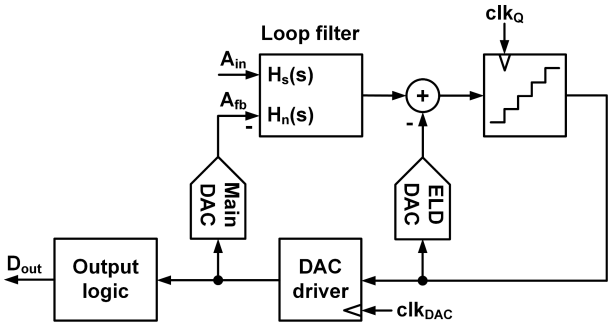


Figure 10.1: Block diagram of a broadband CT SDM with some implementation details

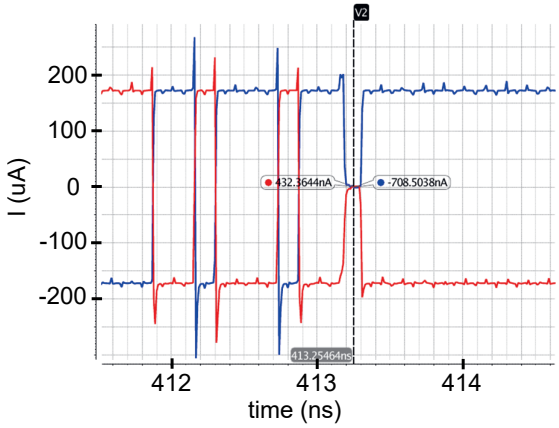
technique is proposed in Section 10.5, where the principle of feedback correction is applied, and it relies on the gain made in the feedback loop.

10.3 Proposed modeling of metastability error mechanism

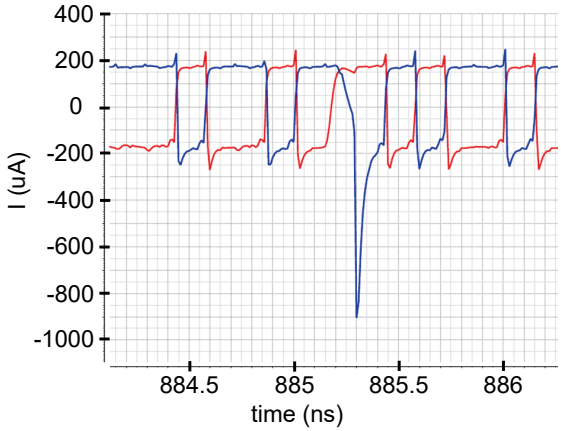
This section describes the error mechanism that is responsible for the impact the metastability has on the performance of CT SDMs in detail. Afterwards, this section proposes a more general model to describe the impact of the metastability error in CT SDMs.

The following description refers to the block diagram of a state-of-the-art broadband CT SDM shown in Figure 10.1. The output of the quantizer is in the ideal case a perfect staircase signal (or a combination of ideal block waveforms) which on the one hand can be translated to a digital signal that forms the output of the SDM D_{out}, and on the other hand, via an ideal DAC, to an analog waveform A_{fb} which is made equal by the $\Sigma\Delta$ loop to the input signal A_{in} in the band of interest. The output of the SDM D_{out} is then the correct digital representation of the DAC output A_{fb} and thus of the input signal of the SDM A_{in}.

Assuming now a non-ideal quantizer with a finite quantization gain. In that case, the latches in the quantizer, which form the core of the comparator, can be not fast enough to reach the maximum output levels for certain (small) input signals. The DAC has no quantization gain, and it converts an unsaturated input to an unsaturated output A_{fb}. The SDM digital output logic has infinite quantization gain, and D_{out} is always a saturated digital signal. In this case, the SDM output D_{out} is no longer the digital counterpart of the DAC output A_{fb}, and the information inside and outside the $\Sigma\Delta$ loop misaligns. Within the signal bandwidth, the DAC output A_{fb} is made equal by



(a)



(b)

Figure 10.2: Metastability errors observed during simulations of an exemplary CT SDM (a) both DAC switches are ON for 1 T_S (b) one DAC switch is OFF, and the other switch is half-OFF for 1 T_S.

the ΣΔ loop to the input signal A_{in}, no matter the output waveform of the DAC. In this case, D_{out} is not the correct digital representation of A_{fb} and thus of A_{in}.

The analysis in the previous paragraph is based on the assumptions of a simplified SDM model given in Section 10.1. With a realistic circuit implementation of a broadband CT ΣΔ ADC, the metastability error is more complicated. When the quantizer output is metastable, the behavior of the DAC circuitry may be different from the desired operation. Figure 10.2 shows two examples of metastability errors that appear in the simulations of the schematic and post-layout model of the CT SDM in this

thesis. In these simulations, the quantizer is in post-layout, and the rest of the SDM is in schematic. Figure 10.2 shows the output current of a unit DAC cell of DAC 1 in the 1st SDM stage (see Figure 5.6). It is implemented as a current-steering DAC with one-side switching (Figure 4.5a). The blue lines and red lines are the output current I_{out}^{+} and I_{out}^{-} of the unit DAC cell. The SDM sampling clock period is about 143 ps (F_S = 7 GHz). When no metastability error happens, the legal output of the unit DAC cell is $\pm\frac{1}{2}I_{DAC}$ (here about ± 170 μA). In Figure 10.2a, at t = 413.2 ns, both switches of the unit DAC cell are ON for 1 T_S because of a metastability error. Thus, the differential output current is about 0 A, which is illegal and D_{out} does not have such a level to represent it. In Figure 10.2b, at t = 885.2 ns, for 1 T_S, one DAC switch is OFF, but the other DAC switch is not fully ON (it gradually turns "half ON"), because of a metastability error. In this case, because the current source I_{DAC} from the top is still ON, some extra charge is stored at V_s node (Figure 4.5a). Thus for the next T_S, even if the DAC input is a fully settled digital signal (no metastability), the extra charge at V_s node causes a strange and illegal waveform of the DAC output current. When a metastability error happens like Figure 10.2b, D_{out} cannot represent the real DAC feedback current, either.

The error mechanism that is responsible for the impact the metastability has on the performance of CT SDMs is summarized in the following. When the quantizer output is metastable, with certain probability, the SDM output D_{out} is no longer the digital counterpart of the DAC output A_{fb}. The DAC output A_{fb} is made equal by the loop to the input signal A_{in}, no matter the output waveform of the DAC. The difference between D_{out} and A_{fb} (both referred to their full-scale to make them unit-less) is defined as the metastability error of the CT SDM in this thesis, which is added out of the $\Sigma\Delta$ loop by the digital output logic.

$$E_{meta} = D_{out} - A_{fb} \tag{10.1}$$

In equation (10.1), A_{fb} is normalized by the full-scale feedback charge of the DAC. Figure 10.3 shows an illustrative plot of output currents of an ideal DAC and a real DAC implementation. In the left figure, the blue line shows the output current of an ideal DAC, when its input is not metastable. Here a non-return-to-zero DAC with rectangular pulse is considered. The area under the blue line is the full-scale feedback charge of the ideal DAC. The red line shows one case of the output current of the ideal DAC when the DAC's input is metastable (not saturated), and the ideal DAC has no quantization gain here. In the case of the red line, A_{fb} is defined as the area under the red line normalized by the area under the blue line. In the right figure, the green line shows the output current of a real DAC implementation, when the DAC input is not metastable. Green line shows a certain settling behavior of the DAC output current. The difference between the green line and the blue line causes both an amplitude error and a timing error (delay), which can change the NTF of the SDM. Both the amplitude error and the timing error can be compensated to restore the ideal NTF. The difference between the green line and the blue line is not the metastability error. The area under the green line is the full-scale feedback charge

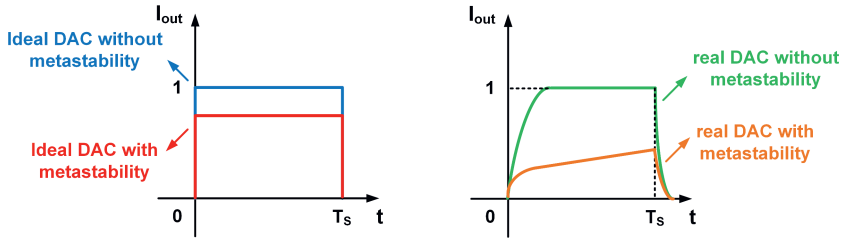


Figure 10.3: Output currents of an ideal DAC and a real DAC implementation

of the real DAC implementation. The light brown line shows one case of the output current of the real DAC when the DAC's input is metastable. In the case of the light brown line, A_{fb} is defined as the area under the light brown line normalized by the area under the green line.

This thesis makes a few remarks on the definition of the metastability error in equation (10.1). (1) The formula assumes that the difference between D_{out} and A_{fb} is due completely to a metastability error. With a real circuit implementation, the DAC's noise and non-linearity make A_{fb} deviating from D_{out} as well, which is not taken into account in this discussion, and thus not in this definition of the metastability error. (2) In this definition, the DAC output A_{fb} is normalized by its full-scale feedback charge. The shape of the DAC pulse and the transient of the DAC settling, when the quantizer output is fully settled (not metastable), change the full-scale feedback charge of the DAC output. But those two effects do not have an impact on the definition of the metastability error here. (3) This definition is not restricted to the assumptions made in Section 10.1; it is generally valid for CT $\Sigma\Delta$ ADCs. It is still valid even if a more sophisticated model for the quantizer is used, or if the quantization gain and thresholds of the DAC driver and DAC are considered (in Figure 10.1). The metastability errors shown in Figure 10.2 are covered by this definition as well.

A simplified model of a CT SDM with the metastability error E_{meta} is shown in Figure 10.4, with a 1st order equivalent of the quantizer and the DAC. In this figure, some details in Figure 10.1 are omitted, such as the DAC driver. This model is generally valid for CT SDMs with metastability error and ELD compensation, irrelevant to the implementation details. When V is metastable, it is an imperfect analog staircase signal (due to the finite quantization gain of the quantizer). The 'DAC' function here represents the analog transfer function from its (analog) staircase input to its output, which represents the imperfect transfer function of the actual DAC block. All the quantization gain of the $\Sigma\Delta$ loop is modelled at the quantizer (defined as G_q). For the SDM output the situation is different: the output logic is translating the imperfect staircase signal of the quantizer to a discrete-amplitude output signal V' (that can be represented by a digital signal D_{out}). The difference between this output signal and the signal at the output of the DAC function is modelled by E_{meta}. V is the DAC input and the input of the digital output logic, and V' is the SDM

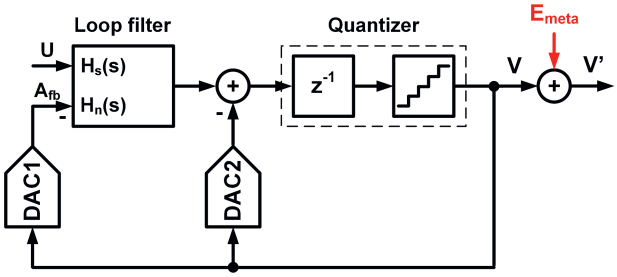


Figure 10.4: Block diagram of a CT SDM with metastability error

output which is considered always as a fully settled digital signal (V' in Figure 10.4 is equivalent to D_{out} in Figure 10.1). Under the assumptions in Section 10.1 and the aforementioned modeling, V and A_{fb} have the same information. The equation (10.1) can be re-written as:

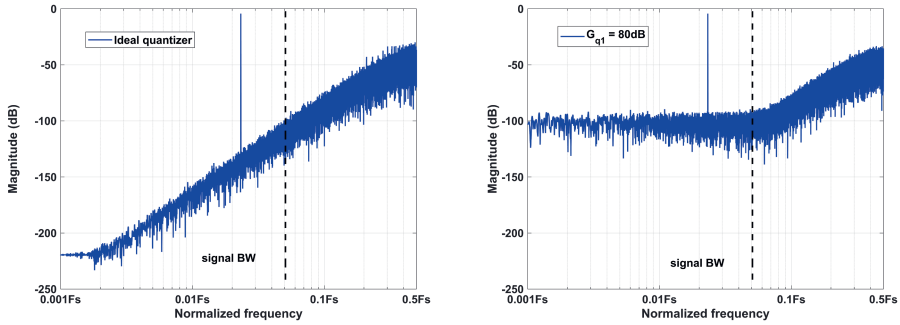
$$E_{meta} = V' - V \tag{10.2}$$

If the sampled quantizer input is very small ($V_{in} < \frac{1}{G_q}$, where V_{in} is referred to its full-scale to make it unit-less), the quantizer output is not a fully settled signal. In this case, a metastability error happens. Because the metastability error E_{meta} is added out of the $\Sigma\Delta$ loop, it is not shaped by the NTF. The transfer function of the metastability error E_{meta} to the SDM output is 1. The result is that in the output spectrum of the SDM, the in-band noise level increases.

This effect is shown in Figure 10.5. Figure 10.5a shows the simulated output spectrum (2^{17} samples) of a 4th order SDM with ideal quantizer, and its quantization noise shows 80 dB/dec slope. Figure 10.5b shows the output spectrum (2^{17} samples) when the total loop quantization gain $G_q = 80$ dB. In this case the metastability error happens with a certain probability (in average 8 times per 10000 samples, with the 9-level quantizer used in this simulation). The metastability error can be modelled as a white noise, and it is not shaped. So the output spectrum shows a flat increased in-band noise. The problem is that the metastability error can degrade the SNDR and the dynamic range of the $\Sigma\Delta$ ADC. Simulations show that with a quantization gain of 80 dB, the SNDR is reduced from 75.3 dB to 55.6 dB, by 19.7 dB, compared to the case with an ideal quantizer (see Figure 5.9).

10.4 Metastability error compensation

This section proposes a novel metastability error compensation (MEC) circuit, to measure and compensate the metastability error of the SDM. Firstly, its operation principle is presented in 10.4.1. The circuit non-idealities in the MEC circuit are considered in 10.4.2. In the end, conclusions are drawn.



(a) (b)

Figure 10.5: (a) Simulated output spectrum with ideal quantizer (b) Simulated output spectrum with 80 dB quantization gain.

10.4.1 Operation principle

The operation principle of the proposed metastability error compensation circuit is introduced here. Figure 10.6 shows the block diagram of a CT $\Sigma\Delta$ ADC with the metastability error compensation circuit. The MEC circuit is composed of 2 extra quantizers (2nd quantizer and 3rd quantizer), 2 extra DACs (DAC 3 and DAC 4), an analog delay element, a digital delay element, an analog summation function and a digital summation function.

The operation principle of the metastability error compensation circuit is as follows. If the quantizer output in the SDM (represented as V in Figure 10.6) is in metastable state, it will be resampled by the 2nd quantizer and amplified by the quantization gain of the 2nd quantizer. The probability of the metastability error at the 2nd quantizer output (represented as V' in Figure 10.6) is reduced by its quantization gain. The metastability error of the 1st quantizer is converted partly to the quantization noise of the 2nd quantizer, and partly to the metastability error of the 2nd quantizer, depending on its quantization gain.

Both 1st quantizer and 2nd quantizer outputs are converted to analog signals by DAC 3 and DAC 4, respectively. The analog delay element delays DAC 3 output for the same time as the delay of the 2nd quantizer (which is the regeneration time of the 2nd quantizer). Then the output of the analog summation is the subtraction of the corresponding analog signals of V and V' for the same sample, which is the majority part of the metastability error of the SDM ($-E_{meta}$). So the output of the 3rd quantizer is the digital representation of the majority part of the metastability error of the SDM. The digital delay element delays V' for the same time as the delay of the 3rd quantizer. For the output of the digital summation (V_c in Figure 10.6), the majority part of the metastability error in the SDM is compensated, and only a

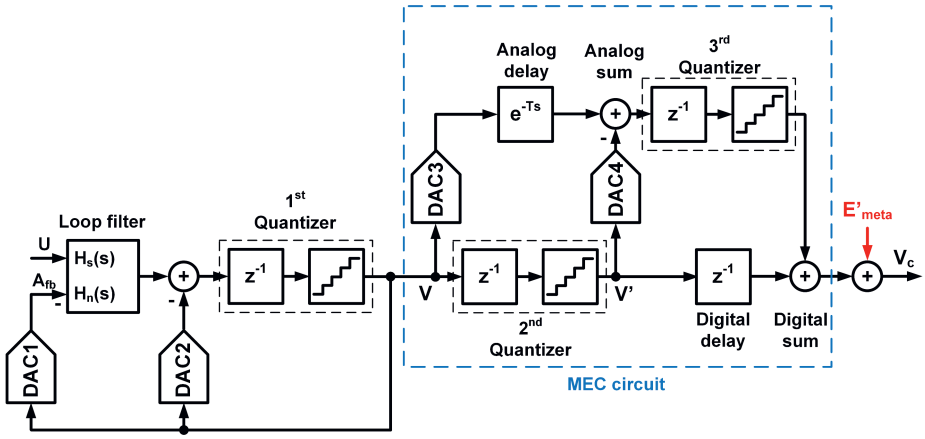


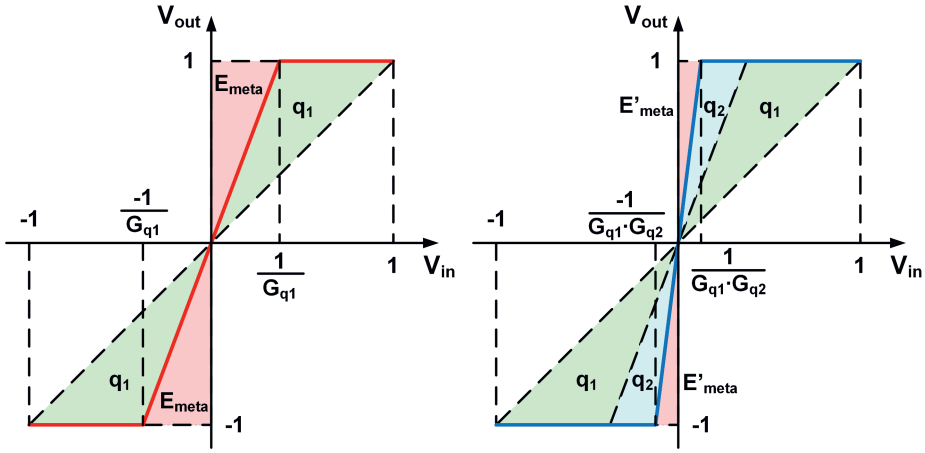
Figure 10.6: Block diagram of a CT SDM with the proposed metastability error compensation circuit

residue metastability error E'_{meta} with a much reduced power than E_{meta} is left (the detailed power calculation for E'_{meta} is shown later).

The requirement on the building blocks of the metastability error compensation circuit is as follows. The 2nd quantizer should have the same resolution (number of quantization levels) as the 1st quantizer. The 1st quantizer is assumed to be an m-level multi-bit quantizer (m $\geq$ 2), and it is composed of m-1 pre-amplifiers and m-1 latches. The pre-amplifiers compare the input signal with a series of references (voltage or current). Then, in this case, the 2nd quantizer is composed of only m-1 latches. The 2nd quantizer performs a re-quantization of the 1st quantizer's output at the 1-bit level: every latch of the 2nd quantizer directly samples the output of one fixed latch of the 1st quantizer, and then performs the regeneration. The 2nd quantizer needs to process all the quantization levels of the 1st quantizer, since the information on which bit is metastable is not known to it.

Another requirement is that DAC 3 and DAC 4 should be the exact replica of DAC 1, which means that they have the same quantization gain as DAC 1, and they behave the same as DAC 1 even when their input is metastable. In the following analysis, the quantization gain of DAC 1, DAC 3 and DAC 4 are assumed to be all one, for simplicity. The quantization gain of the 1st quantizer and the 2nd quantizer are assumed to be G_{q1} and G_{q2}, respectively. For the moment, all the components are assumed to be ideal and the 3rd quantizer has infinite resolution.

The mathematical analysis of the metastability error compensation is described as follows for $\Sigma\Delta$ ADCs with 1-bit quantizers, with the help of the diagrams shown in Figure 10.7. Figure 10.7a shows the diagram of the quantization noise and the metastability error of the conventional $\Sigma\Delta$ ADC shown in Figure 10.4. The red line is the output characteristic of the quantizer in the SDM. The distance in y-axis



(a) (b)

Figure 10.7: Diagram of the quantization noise and the metastability error: (a) of the conventional SDM shown in Figure 10.4; (b) of the SDM with the metastability error compensation circuit shown in Figure 10.6.

between the red line and the $V_{out} = V_{in}$ line is the quantization error of this quantizer (referred as the quantization noise as well), and it is denoted as q_1. The quantization noise is added in the ΣΔ loop at the quantizer, and it is shaped by the NTF. The light red area is the metastability error in the conventional ΣΔ ADC, which is denoted as E_{meta}. The metastability error is added out of the ΣΔ loop by the digital output logic, and hence unshaped. In the conventional ΣΔ ADC, the metastability error happens with a probability of $\frac{1}{G_{q1}}$. Thus, the probability density function of the metastability error is

$$f(x)_{meta} = \begin{cases} \frac{1}{2G_{q1}} & \text{, if} -1 \leq x \leq 1 \\ 0 & \text{, if else} \end{cases} \tag{10.3}$$

The power of the metastability error in the conventional SDM can be calculated as

$$P_{E_{meta}} = \int_{x=-1}^{1} x^2 \cdot \frac{1}{2G_{q1}}\, dx \;= \frac{1}{3G_{q1}} \tag{10.4}$$

Similarly, the probability density function of the quantization noise of the quantizer in the SDM q_1 is

$$f(x)_{q_1} = \begin{cases} \frac{1}{2\cdot(1-\frac{1}{G_{q1}})} & \text{, if} -(1-\frac{1}{G_{q1}}) \leq x \leq 1-\frac{1}{G_{q1}} \\ 0 & \text{, if else} \end{cases} \tag{10.5}$$

The power of the quantization noise q_1 of the quantizer in the SDM can be calculated as

$$P_{q_1} = \int_{x=-(1-\frac{1}{G_{q1}})}^{1-\frac{1}{G_{q1}}} x^2 \cdot \frac{1}{2 \cdot (1 - \frac{1}{G_{q1}})} \, dx \; = \frac{1}{3}\Big(1 - \frac{1}{G_{q1}}\Big)^2 \tag{10.6}$$

Even with relatively low total loop quantization gain G_{q1} (e.g. 40 dB), the power of the metastability error is far lower than the unshaped quantization noise. However, the quantization noise is in the $\Sigma\Delta$ loop and shaped by the designed noise transfer function. So the in-band quantization noise in the final output is very much suppressed. The metastability error is added out of the $\Sigma\Delta$ loop and directly on the SDM output, which is not shaped. So the power of the metastability error seems to be very low, but it can cause dramatic degradation on the overall performance of the $\Sigma\Delta$ ADCs.

Figure 10.7b shows the diagram of the quantization noise and the metastability error of the $\Sigma\Delta$ ADC with the metastability error compensation circuit shown in Figure 10.6. The blue line is the overall output characteristic of the 1st quantizer and the 2nd quantizer. The light green part is the same as in Figure 10.7a. The light blue area is the quantization noise of the 2nd quantizer. When the input voltage (referred to its full-scale) of the 1st quantizer is within $(\frac{1}{G_{q1}G_{q2}}, \frac{1}{G_{q1}})$ or $(-\frac{1}{G_{q1}}, -\frac{1}{G_{q1}G_{q2}})$, the output of DAC 1 and DAC 3 have metastability errors, and the output of DAC 4 has no metastability error because of the additional quantization gain of the 2nd quantizer G_{q2}. So at the output of DAC 4, the metastability error happens with a probability of $\frac{1}{G_{q1}G_{q2}}$, which is G_{q2} times lower than the conventional $\Sigma\Delta$ ADC. The metastability error at the output of DAC 4 is referred as the residual metastability error E'_{meta}, for a metastability error compensation circuit that is ideal, except for the limited quantization gain of the 2nd quantizer (this assumption is referred as the ideal metastability error compensation circuit in the following). Its power can, similarly as in (10.4), be calculated as

$$P_{E'_{meta}} = \frac{1}{3G_{2,tot}} \tag{10.7}$$

Here, $G_{2,tot} = G_{q1} \cdot G_{q2}$.

The probability density function of the quantization noise of the 2nd quantizer (denoted as q_2) is

$$f(x)_{q_2} = \begin{cases} \frac{1}{2G_{q1} \cdot (1 - \frac{1}{G_{q2}})} & \text{, if} -(1 - \frac{1}{G_{q2}}) \leq x \leq 1 - \frac{1}{G_{q2}} \\ 0 & \text{, if else} \end{cases} \tag{10.8}$$

The power of the quantization noise of the 2nd quantizer is

$$P_{q_2} = \frac{1}{3G_{q1}}\Big(1 - \frac{1}{G_{q2}}\Big)^2 \tag{10.9}$$

Notice that the original metastability error E_{meta} in Figure 10.4 is divided into two parts in the ΣΔ ADC with the metastability error compensation circuit, and q_2 is the majority part.

$$E_{meta} = q_2 + E'_{meta} \tag{10.10}$$

The corresponding analog signal of the quantization noise of the 2nd quantizer q_2 is actually the output of the analog summer in Figure 10.6 with a minus sign. This signal is quantized by the 3rd quantizer and subtracted from the digital output of the SDM. So in the ΣΔ ADC with an ideal metastability error compensation circuit in Figure 10.6, its final output after compensation V_c only contains unshaped residual metastability error E'_{meta} and shaped (by the designed NTF) quantization noise of the 1st quantizer q_1, and the quantization noise of the 2nd quantizer q_2 is completely canceled.

The metastability error for unary multi-bit quantizers can be analyzed similarly. For an m-level quantizer (considered as a flash sub-ADC here) composed of m-1 comparators with a quantization gain of G_{q1}, the equation (10.4) can be re-written as:

$$P_{E_{meta}} = \int_{x=-\frac{1}{m-1}}^{\frac{1}{m-1}} x^2 \cdot \frac{(m-1)^2}{2G_{q1}}\, dx \; = \frac{1}{3 \cdot (m-1) \cdot G_{q1}} \tag{10.11}$$

Figure 10.8 shows the simulated 3rd quantizer input signal of a ΣΔ ADC with the metastability error compensation circuit whose 1st quantizer and 2nd quantizer are 9-level, and $G_{q1} = 80$ dB, $G_{q2} = 40$ dB. The time domain signal has a specific property – for a probability of $1-\frac{8}{G_{q1}} = 99.92\%$ (8 in the numerator because the 9-level quantizer is composed of 8 1-bit comparators, and any comparator can become metastable), no metastability error happens in the ΣΔ loop, and the 3rd quantizer input is 0. And for a probability of 0.08%, a metastability error happens in the ΣΔ loop, and the 3rd quantizer input is within ± 0.5 LSB_1 of the 1st quantizer (in this case it is within ± 1/8; LSB_1 denotes the least significant bit of the 1st quantizer).

In practice, the 3rd quantizer has limited resolution, and it has its own quantization noise. One important design consideration is, when no metastability error happens in the ΣΔ loop (99.92% probability in Figure 10.8), the 3rd quantizer should NOT introduce a new error. This is achieved by giving the 3rd quantizer a legal output level 0. In this case, when the 3rd quantizer input is within ± 0.5 LSB_3 (LSB_3 denotes the least significant bit of the 3rd quantizer), the 3rd quantizer output is 0. Later it will be shown that the metastability error compensation circuit has a ± 0.5 LSB_3 error-insensitive interval thanks to the legal output level 0.

If the 3rd quantizer has a legal output 0, when its input is 0 (99.92% probability in Figure 10.8), its output is 0 as well. In this case, the 3rd quantizer does nothing, and hence does not introduce any error. In other words, only when the metastability errors happen in the ΣΔ loop ($\frac{m-1}{G_{q1}} = 0.08\%$ probability in Figure 10.8), the 3rd quantizer is effectively working, and its quantization noise is important. The power of the

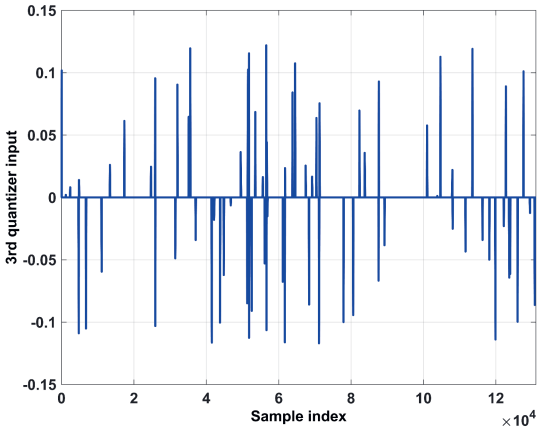


Figure 10.8: Simulated 3rd quantizer input when G_{q1} = 80 dB, and G_{q2} = 40 dB

introduced error in the final output V_c by the 3rd quantizer with limited resolution can be calculated as

$$P_{E_{q3}} = \frac{m-1}{G_{q1}} \cdot P_{q3} = \frac{m-1}{G_{q1}} \cdot \frac{LSB_3^2}{12} \tag{10.12}$$

In equation (10.12), E_{q3} is the introduced error in the final output by the 3rd quantizer, q_3 is the quantization error of the 3rd quantizer, and m is the number of quantization levels of the 1st and 2nd quantizer.

Because of this property, the 3rd quantizer does not need a very high resolution, even though the target resolution of the ΣΔ ADC after compensation is very high. E.g. from simulation, for a 4th order ΣΔ ADC with 9-level quantizer in the ΣΔ loop and G_{q1} = 80 dB, when the 3rd quantizer has 17 quantization levels (4.09 bit) for the input swing (-1/8, 1/8), the overall output after compensation V_c achieves SNDR = 75.1 dB (12.2 ENOB). In this case the SNDR is limited by the in-band shaped quantization noise $NTF \cdot q_1$ (SNDR = 76.5 dB for the ideal ΣΔ ADC). Notice that without the metastability error compensation circuit, SNDR = 60.9 dB which is completely limited by the in-band metastability error. In this case, the simulated output spectrum with and without the metastability error compensation circuit for 2^{17} samples is shown in Figure 10.9. For this exemplary 4th order ΣΔ ADC, the OSR is 10.

Figure 10.10 presents the simulated SNDR versus total loop quantization gain (G_{q1}) with and without the metastability error compensation circuit. The ΣΔ ADC uses a 9-level quantizer in the ΣΔ loop. The MEC circuit employs a 17-level 3rd quantizer for its input swing (-1/8, 1/8). Without the MEC, to achieve SNDR $\geq$ 75 dB, the total loop quantization gain of the ΣΔ loop (G_{q1}) should be at least 120 dB.

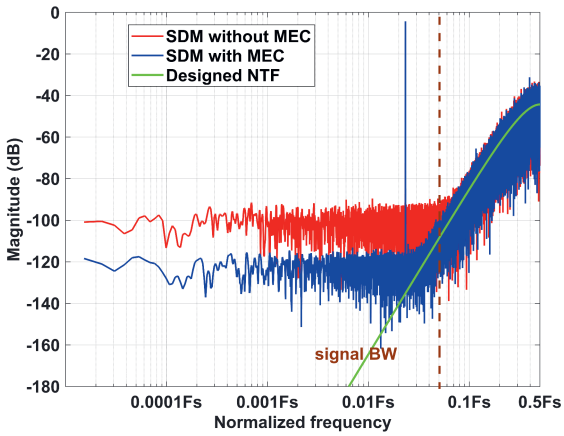


Figure 10.9: Simulated output spectrum of a 4th order SDM with and without metastability error compensation circuit, $G_{q1} = 80$ dB, $G_{q2} = 40$ dB

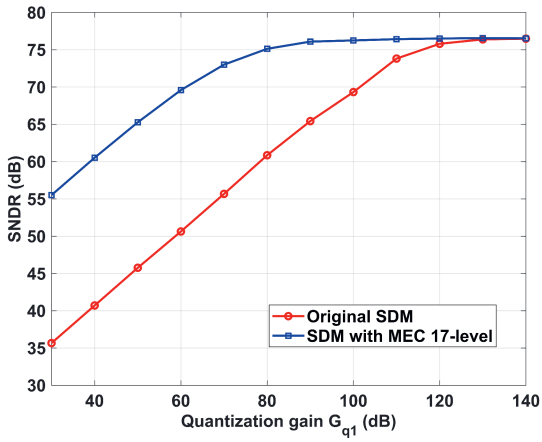


Figure 10.10: Simulated SNDR versus total loop quantization gain (G_{q1}) with and without the metastability error compensation circuit with a 17-level 3rd quantizer

With the metastability error compensation circuit, the requirement for the total loop quantization gain (G_{q1}) is relaxed to 80 dB. In this case, the quantization gain of the 2nd quantizer should be at least 40 dB.

This thesis crosses check the simulation results in Figure 10.9 and 10.10 with the equations (10.11) and (10.12). In Figure 10.9 and 10.10, a sine wave with an amplitude of 1 (referred to SDM input full scale) is used as the SDM input. The signal power

is:

$$P_s = \frac{1^2}{2} = 0.5 \tag{10.13}$$

For a 9-level quantizer with a quantization gain G_{q1} of 80 dB (red line in Figure 10.9), the calculated metastability error power with equation (10.11) is $P_{meta,80dB} = 4.2 \cdot 10^{-6}$. And the calculated metastability error limited SNR is:

$$SNR_{meta,80dB} = 10 \cdot log_{10} \frac{P_s \cdot OSR}{P_{meta,80dB}} = 60.8 \text{ dB} \tag{10.14}$$

The in-band metastability error power is much larger than the in-band quantization noise power. The calculated $SNR_{meta,80dB}$ matches very well with the simulation results in Figure 10.9 and 10.10.

For a 9-level quantizer with a quantization gain G_{q1} of 120 dB, the calculated metastability error power with equation (10.11) is $P_{meta,120dB} = 4.2 \cdot 10^{-8}$. And the calculated metastability error limited SNR is:

$$SNR_{meta,120dB} = 10 \cdot log_{10} \frac{P_s \cdot OSR}{P_{meta,120dB}} = 80.8 \text{ dB} \tag{10.15}$$

In this case, the in-band metastability error power is less than the in-band quantization noise power, so the overall SNR (75.8 dB) is not degraded much compared with the SNR of the ideal SDM (76.5 dB).

For a 9-level quantizer with a quantization gain G_{q1} of 80 dB and the MEC with a 17-level 3rd quantizer (blue line in Figure 10.9), the quantization noise power introduced by the 3rd quantizer is:

$$P_{E_{q3}} = \frac{8}{10^4} \cdot \frac{(\frac{1}{16} \cdot \frac{2}{8})^2}{12} = 1.6 \cdot 10^{-8} \tag{10.16}$$

The in-band 3rd quantizer's quantization noise power (unshaped) is less than the in-band 1st quantizer's quantization noise power (shaped by the NTF), so a 17-level quantizer offers enough resolution as the 3rd quantizer.

In the simulations, the probability and the histogram of the metastability error are compared with the analysis. The simulations prove that the assumption that the quantizer input is uniformly distributed in the defined input swing (-1, 1) is valid, and the analysis and calculation are correct.

10.4.2 Consideration of the circuit non-idealities

This section so far considers only the limited resolution of the 3rd quantizer. In this sub-section, the other main non-idealities of the building blocks of the metastability error compensation circuit is considered.

As mentioned in the last sub-section, because the 3rd quantizer is designed to have a legal output level 0, if the 3rd quantizer input is within ± 0.5 LSB_3, the 3rd quantizer output is 0. When no metastability error happens in the ΣΔ loop (with a very high probability of $1 - \frac{m-1}{G_{q1}}$), the ideal input of the 3rd quantizer is 0, and the desired output is 0. So if the circuit non-idealities (e.g. mismatch of the unit elements of DAC 3 and DAC 4, the sampled thermal noise at the input of the 3rd quantizer, etc.) introduce a small error at the input of the 3rd quantizer which is less than ± 0.5 LSB_3, it introduces no error in the final output of the SDM V_c for a very high probability. In short, at the input node of the 3rd quantizer, if the total error caused by the circuit non-idealities is less than ± 0.5 LSB_3, it is suppressed by the total loop quantization gain of the ΣΔ loop (G_{q1}) in the final output V_c.

$$P_{E_{DAC2,mm}} = \frac{m-1}{G_{q1}} \cdot P_{DAC2,mm} \tag{10.17}$$

$$P_{E_{DAC3,mm}} = \frac{m-1}{G_{q1}} \cdot P_{DAC3,mm} \tag{10.18}$$

$$P_{E_{Vin3,tn}} = \frac{m-1}{G_{q1}} \cdot P_{Vin3,tn} \tag{10.19}$$

In equation (10.17) – (10.19), $P_{E_{DAC2,mm}}$, $P_{E_{DAC3,mm}}$ and $P_{E_{Vin3,tn}}$ represent the power of the errors in the final output V_c caused by the unit element mismatch of DAC 3, the unit element mismatch of DAC 4, and the sampled thermal noise on the 3rd quantizer input, respectively. And $P_{DAC2,mm}$, $P_{DAC3,mm}$ and $P_{Vin3,tn}$ represent the original power of the errors caused by the unit element mismatch of DAC 3, the unit element mismatch of DAC 4, and the sampled thermal noise on the 3rd quantizer input, respectively. In this case, the interval (-0.5 LSB_3, 0.5 LSB_3) is defined as the error-insensitive interval.

However, if the total error at the 3rd quantizer input is (with a non-negligible probability) higher than 0.5 LSB_3 or lower than -0.5 LSB_3, it means that even when no metastability error happens in the ΣΔ loop, the 3rd quantizer output is not 0 but LSB_3 or -LSB_3. In this case, some extra error is introduced into the final output V_c even when no metastability error happens, and hence the total error power is not suppressed by the total loop quantization gain. It degrades the overall resolution of the SDM a lot, which can be even lower than the conventional SDM without metastability error compensation circuit.

As shown in Figure 10.11, the error-insensitive interval can be increased by removing two 1-bit comparators with reference -0.5 LSB_3 and 0.5 LSB_3. Thus, when the 3rd quantizer input is within (-1.5 LSB_3, 1.5 LSB_3), its output is 0. In this case the error-insensitive interval is enlarged by a factor of 3. Then, the requirement of the DAC 3 and DAC 4 unit element mismatch, and the input thermal noise of the 3rd quantizer, etc. is further relaxed. This quantizer is referred to the non-uniform quantizer in the following. Its drawback is a slightly reduction of the SNDR because when the

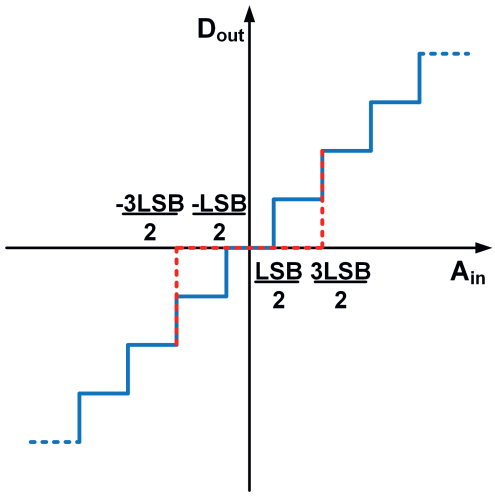


Figure 10.11: Output characteristic of a 17-level uniform quantizer (solid blue line) and a 15-level non-uniform quantizer (dash red line). The complete input and output swing are not shown here.

metastability error in the ΣΔ loop is in the interval of (-1.5 LSB_3, -0.5 LSB_3) or (0.5 LSB_3, 1.5 LSB_3), the output of this non-uniform quantizer is 0, and this small metastability error is not compensated. From simulation, compared to the 17-level uniform 3rd quantizer, with the 15-level non-uniform quantizer the SNDR drops by 0.6 dB.

Similar as the DAC 3 and DAC 4 unit element mismatch error, and the sampled thermal noise at the 3rd quantizer input node, thanks to the error-insensitive interval, the performance of the metastability error compensation circuit is not sensitive to the offset errors on the reference of the 3rd quantizer. From the simulation, the standard deviation of the reference offset error should be less than 4% of its input swing ($-\frac{1}{8}$, $\frac{1}{8}$) for the 15-level non-uniform 3rd quantizer.

Because the 3rd quantizer is not in a feedback loop, the requirement of its quantization gain is very low. From the simulation, higher than 20 dB quantization gain is enough for the 3rd quantizer. As the 3rd quantizer is not in a feedback loop, only its throughput is required to be the same as the sampling rate of the SDM, but its latency is not required to be one clock period. The digital delay in Figure 10.6 should equal the latency of the 3rd quantizer. Thus the 3rd quantizer can be implemented as e.g. a pipelined ADC (instead of a flash ADC) to reduce the number of comparators and its power consumption.

Table 10.1 summarizes the requirements on the building blocks of the metastability error compensation circuit. In all simulations, the SDM uses a 9-level quantizer in the ΣΔ loop, and the total loop quantization gain is 80 dB. The SNDR target after

Table 10.1: Summary of the requirements on the building blocks of the metastability error compensation circuit

Scenarios	17-level uniform 3rd quantizer	15-level non-uniform 3rd quantizer
DAC 3 and DAC 4 linearity	8-bit	7-bit
2nd quantizer quantization gain	$\geq$ 40 dB	$\geq$ 40 dB
3rd quantizer quantization gain	$\geq$ 20 dB	$\geq$ 20 dB
3rd quantizer reference offset σ	1.3% of $(-\frac{1}{8}, \frac{1}{8})$	4% of $(-\frac{1}{8}, \frac{1}{8})$
Sampled thermal noise at 3rd quantizer input	$\leq$ -55 dB	$\leq$ -46 dB

compensation is 74 dB (12 ENOB), including all considered circuit non-idealities in the metastability error compensation circuit. The ideal ΣΔ ADC has SNDR = 76.5 dB. It shows that even for an overall resolution target of 12 ENOB, the requirements of the building blocks of the MEC circuit are relatively low, mainly thanks to the error-insensitive interval. The MEC circuit is promising to be implemented in modern CMOS technologies.

The aforesaid analysis uses single-loop ΣΔ ADCs as examples. The metastability error compensation circuit can be implemented in MASH ΣΔ ADCs as well. For MASH ΣΔ ADCs, generally the metastability error generated in the 1st ΣΔ loop is dominant in the overall metastability error in the final output, because the metastability error generated in the back-end ΣΔ loops is shaped by the noise transfer function of the preceding ΣΔ loop(s). So typically it is enough to apply the metastability error compensation circuit only to the 1st ΣΔ loop output.

10.4.3 Power, area, and performance considerations

The MEC circuit is proposed to overcome the metastability limitation and enable a higher sampling rate and signal bandwidth for a certain technology. For the 3-bit 2-1-1 MASH SDM test chip designed in this thesis (Chapter 11), the practically achievable minimum time constant of the comparator core is about 6.5 ps, considering the layout effect and loading. Without the MEC circuit, 120 dB of quantization gain is required for the 1st quantizer (Figure 10.10). Assuming the regeneration time of the quantizer is maximized to be 0.5 T_S (the other 0.5 T_S is for the propagation time from the quantizer to the DAC, and the DAC delay), the maximal achievable sampling rate of the SDM is

$$F_{S,max,w/o\ MEC} = \frac{1}{ln(10^{\frac{120}{20}}) \times 6.5 \cdot 10^{-12} \times 2} \approx 5.57 \text{ GHz} \tag{10.20}$$

With the proposed MEC circuit, the quantization gain requirement for the 1st quantizer is reduced to 80 dB. Two scenarios are considered in the estimation of the maximal achievable sampling rate of the SDM with the MEC circuit. In the first scenario, assuming the quantizer regeneration time is 0.5 T_S, the maximal achievable sampling rate of the SDM is increased to

$$F_{S,max,with\ MEC,case1} = \frac{1}{ln(10^{\frac{80}{20}}) \times 6.5 \cdot 10^{-12} \times 2} \approx 8.35 \text{ GHz} \tag{10.21}$$

In the second scenario, assuming the propagation delay from the quantizer to the DAC and the DAC delay is independent from the MEC circuit, and only the regeneration time of the quantizer can be reduced by applying the MEC circuit, the maximal achievable sampling rate of the SDM is

$$F_{S,max,with\ MEC,case2} = \frac{1}{(ln(10^{\frac{80}{20}}) + ln(10^{\frac{120}{20}})) \times 6.5 \cdot 10^{-12}} \approx 6.68 \text{ GHz} \tag{10.22}$$

The aforementioned example shows that when the maximal achievable sampling rate (and signal BW) of the state-of-the-art SDM for a certain technology is limited by the metastability error to $F_{S,max,w/o\ MEC}$, the proposed MEC circuit can mitigate the metastability limitation and enable a 1.2× ∼ 1.5× higher maximal achievable sampling rate.

The extra power and area needed for the MEC circuit should also be considered. The quantization gain requirement of the 2nd quantizer is about 2× less than the 1st quantizer in dB, which means the time constant of the 2nd quantizer can be 2× larger than the 1st quantizer to save power. The quantization gain requirement of the 3rd quantizer is only $\geq$ 20 dB, which can be achieved with power-efficient circuit. DAC 3 and DAC 4 can be implemented as a scaled version of DAC 1 to save power, at the cost of slightly degraded matching performance [100]. The analog delay and summation can be implemented with a sample-and-hold circuit, which is passive [101]. The total power consumption of the MEC circuit is estimated to be 0.5× ∼ 1× of that of the main ΣΔ loop, considering the ΣΔ loop consumes power for loop filter and ELD compensation, which are not needed in the MEC circuit [100].

DAC 3 and DAC 4 should be the exact copy or a scaled copy of DAC 1, to guarantee the required matching. The rest blocks of the MEC circuit do not have stringent matching requirements. The area of the MEC circuit is estimated to be 0.5× ∼ 1× of that of the main ΣΔ loop as well.

The minimum time constant of the comparator core is limited by the technology. Without the MEC circuit, even if the power of the MEC circuit is spent in the 1st quantizer, its time constant cannot be further reduced (e.g. since self-loading is dominant), and the SDM sampling rate is still limited by the metastability error and thus cannot be increased.

10.4.4 Conclusions

A novel metastability error compensation circuit is proposed in this section. It reproduces the metastability error out of the $\Sigma\Delta$ loop, measures it and compensates it in the digital domain. For the exemplary 4th order 9-level $\Sigma\Delta$ ADC, the MEC circuit can relax the total quantization gain requirement in the $\Sigma\Delta$ loop by 40 dB for the same 74 dB SNDR target. The unique property of the error-insensitive interval is introduced in the MEC circuit. Thanks to the error-insensitive interval, the requirements on the building blocks in the MEC circuit are not stringent and the MEC circuit is promising for implementation in modern CMOS technologies. The proposed MEC circuit overcomes the metastability limitation, and enables CT $\Sigma\Delta$ ADCs with $1.2\times \sim 1.5\times$ higher maximal sampling rate, achieving broader bandwidth and/or higher resolution.

10.5 Metastability shaping technique

The previous section proposes a MEC circuit to reproduce the metastability error out of the $\Sigma\Delta$ loop, measure it and compensate it. This section proposes an alternative solution to combat the metastability error – noise shaping the (original) metastability error. With this technique, more quantization gain needs to be generated in the $\Sigma\Delta$ loop, which means more regeneration time is needed for the quantizer (assuming the minimum time constant τ is limited, see equation (4.10)). Thus, ELD compensation is relevant in this section.

10.5.1 Conventional ELD compensation

The ELD compensation has been shown in Chapter 4.5. Figure 10.4 depicts the block diagram of an exemplary CT SDM with the metastability error and the ELD compensation. This section takes a 4th order single-loop 1-bit CT SDM as an example. However, the proposed metastability shaping technique can be applied to other CT SDM architectures as well, including multi-bit SDMs and MASH structures.

The impact of the metastability error for the exemplary 4th order 1-bit SDM is shown in Figure 10.12. Compared to Figure 10.5, this figure shows the same information on the impact of the metastability error, but now for a different SDM example. The blue line shows the simulated output spectrum (2^{19} samples) of a 4th order SDM with an ideal 1-bit quantizer. The red line shows the output spectrum (2^{19} samples) when the total loop quantization gain $G_1 = 60$ dB. In this simulation, the simulated SNDR of the SDM with an ideal quantizer is 81.2 dB. The simulated SNDR is dropped to 46.5 dB, for the conventional SDM with total loop quantization gain of 60 dB.

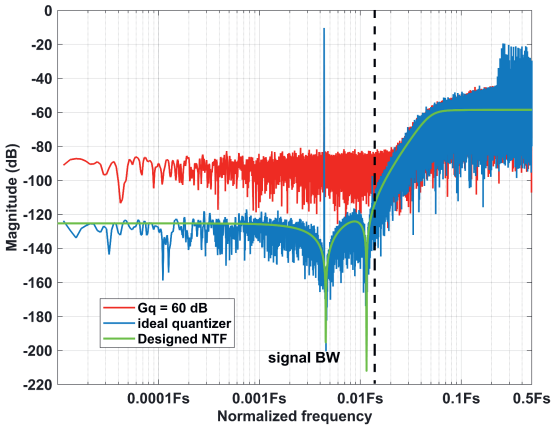


Figure 10.12: Simulated output spectrum of a 4th order 1-bit SDM with and without metastability error

10.5.2 Proposed metastability shaping technique

The block diagram of a continuous-time ΣΔ ADC with the proposed metastability shaping technique is shown in Figure 10.13. Two quantizers are used in the SDM. One T_S delay (z^{-1} in the z-domain) is modelled for each quantizer, including its regeneration time, the DAC delay and propagation delay from the quantizer to the DACs. The direct feedback loop from quantizer 1 output ($V1$) to its input through DAC 3 is the inner ELD compensation loop, which is the 1st order feedback loop of the SDM. The feedback loop from quantizer 2 output (V) to quantizer 1 input through DAC 2 is the outer ELD compensation loop, which is the 2nd order feedback loop of the SDM. The feedback loop through DAC 1 is the main feedback loop of the SDM, which has stringent requirement on the total quantization gain. The advantage of the proposed technique is as follows. A 2nd ELD compensation loop can compensate the delay of another one T_S, allowing more time to generate more quantization gain with a 2nd quantizer in the ΣΔ loop. The inner ELD compensation loop has the quantization gain from only one quantizer generated from 1 T_S timing budget, but fortunately this loop does not require high quantization gain. The outer ELD compensation loop and the main feedback loop have the quantization gain from two quantizers generated from 2 T_S timing budget, which fulfills the quantization gain requirement to suppress the metastability error. The metastability shaping technique is an example of nested loop design, whose advantage is to offer the freedom of separate optimization for decoupled problems.

The proposed metastability shaping technique can also be applied to multi-bit SDMs. In that case, quantizer 2 should have the same resolution (number of quantization levels) as quantizer 1. Quantizer 2 performs a re-quantization of the quantizer 1's

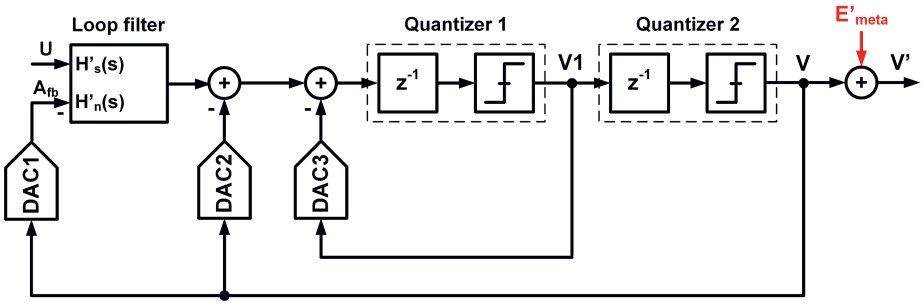


Figure 10.13: Block diagram of a continuous-time ΣΔ ADC with the proposed metastability shaping technique

output at the 1-bit level: every latch of quantizer 2 directly samples the output of one fixed latch of quantizer 1, and then performs the regeneration. Quantizer 2 does not need a reference input.

With the metastability shaping technique, the total quantization gain of the main feedback loop through DAC 1 is actually the summation of quantization gain of quantizer 1 and quantizer 2. Because quantizer 2 has extra regeneration time (one T_S minus the propagation delay and DAC delay) to generate quantization gain, the total quantization gain in the main feedback loop can be much larger than the conventional SDM in Figure 10.4. On the other hand, although the inner ELD compensation loop through DAC 3 has only the quantization gain of quantizer 1, this loop has a much relaxed requirement on the quantization gain.

To map the SDM to the designed noise transfer function, the loop filter feedback transfer function $H'_n(s)$ and its parameters need to be re-calculated, compared with the loop filter in the conventional SDM $H_n(s)$. Here in Figure 10.4 and 10.13, the loop filter is drawn as in the feed-forward structure. But the proposed metastability shaping technique can be used for SDMs with feedback structure or any hybrid feed-forward/feedback structures as well. Moreover, the proposed technique can be further extended to using 3 and more quantizers.

The mathematical analysis of the metastability shaping technique is described as follows for ΣΔ ADCs with 1-bit quantizers. The case with multi-bit quantizers is similar. Actually, it has some similarity compared with the mathematical analysis of the metastability error compensation circuit shown in the previous section. The diagrams in Figure 10.7 can still be used. Figure 10.7a represents the quantization noise and the metastability error for the conventional SDM in Figure 10.4. Similar as in the last section, the red line shows the output characteristic of the quantizer in the conventional SDM in Figure 10.4. The light green area is the quantization noise q_1, and the light red area is the metastability error of the conventional SDM E_{meta}. If the same definition of the quantization gain of the 1st quantizer G_{q1} is made, equations (10.3) - (10.6) and (10.11) hold for the conventional SDM in Figure 10.4 as well.

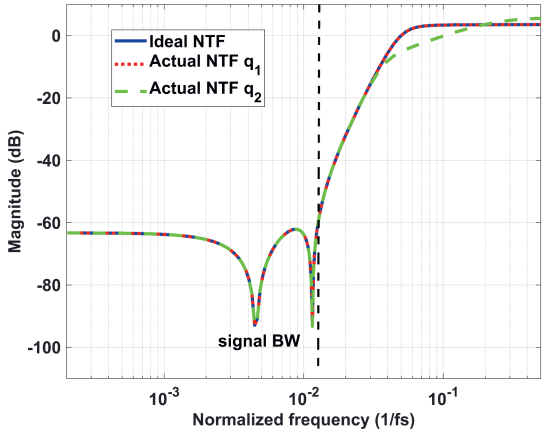


Figure 10.14: Calculated noise transfer functions for the quantization noise of quantizer 1 and quantizer 2

Figure 10.7b represents the quantization noise and the metastability error for the SDM with the proposed metastability shaping technique in Figure 10.13. Similar as in the previous section, the blue line shows the overall output characteristic of the quantizer 1 and quantizer 2. The light green area is the quantization noise of quantizer 1 q_1, and the light blue area is the quantization noise of quantizer 2 q_2. The light red area is the metastability error E'_{meta} added at the SDM output for the SDM with the proposed metastability shaping technique. If the same definition of the quantization gain of the 2nd quantizer G_{q2} is made, equations (10.7) - (10.10) hold for the SDM with the metastability shaping technique in Figure 10.13 as well.

Both of the quantization noise of quantizer 1 and quantizer 2 are shaped by a full-order noise transfer function, as shown in Figure 10.14. Full-order means the same order as the loop filter. The blue line shows the ideal noise transfer function of the conventional SDM. The dotted red line shows the actual NTF of the quantization noise of the quantizer 1 (q_1), which is exactly the same as the ideal NTF. With the design freedom offered by the SDM parameters, only one actual NTF (either for the quantization noise of the quantizer 1 or that of the quantizer 2) can be mapped to the ideal NTF. The actual NTF of q_1 is chosen to be mapped to be the same as the ideal NTF, and thus the actual NTF of quantization noise of the quantizer 2 is the result of this mapping. The dashed green line shows the actual NTF of the quantization noise of the quantizer 2 (q_2). Its in-band part overlaps with the ideal NTF, while its high-frequency part is a bit different. Its out-of-band gain is slightly higher than the ideal NTF, but it does not harm the stability of the SDM, because the power of the quantization noise of quantizer 2 (q_2) is much lower than the quantization noise of quantizer 1 (q_1).

Figure 10.15 shows the simulated output spectrum (2^{19} samples) of the 4th order 1-bit

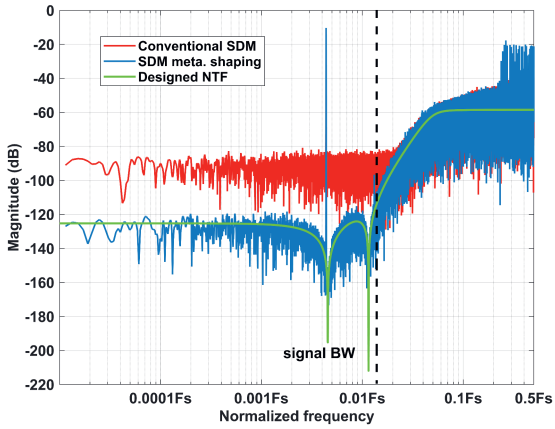


Figure 10.15: Simulated output spectrum of a 4th order SDM with and without the metastability shaping technique, each quantizer has 60 dB gain

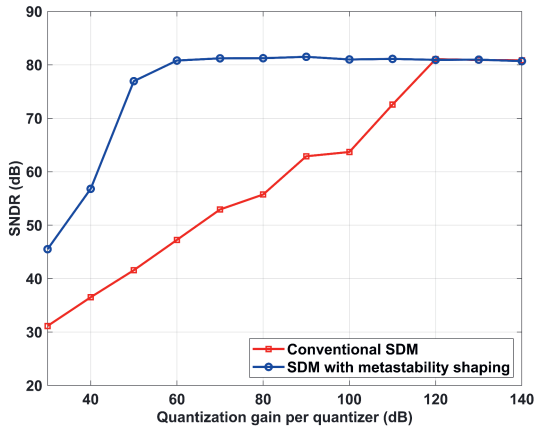


Figure 10.16: Simulated SNDR versus the quantization gain per quantizer with and without the metastability shaping technique

SDM with and without the proposed metastability shaping technique. Each quantizer has 60 dB quantization gain in this simulation ($G_{q1} = G_{q2} = 60$ dB). The simulated SNDR with the proposed metastability shaping technique is 81 dB, which is the same as the ideal SDM with an ideal quantizer.

Figure 10.16 presents the simulated SNDR versus the quantization gain per quantizer with and without the proposed metastability shaping technique. With the metastability shaping technique, the quantization gain of quantizer 1 and quantizer 2 are as-

sumed to be equal. Without the metastability error compensation circuit, to achieve SNDR $\geq$ 80 dB, the total quantization gain of the $\Sigma\Delta$ loop should be at least 120 dB. With the metastability shaping technique, the requirement for the quantization gain per quantizer is relaxed to 60 dB. For a quantization gain of 60 dB per quantizer, the metastability shaping technique improves the SNDR of the SDM from 47.3 dB to 80.8 dB by 33.5 dB.

10.5.3 Conclusions

This section presents a novel metastability shaping technique for broadband CT $\Sigma\Delta$ ADCs. A 2nd ELD compensation loop can compensate the delay of another one T_S, allowing more time to generate more quantization gain with a 2nd quantizer in the $\Sigma\Delta$ loop. The quantization noise from both quantizers experiences the same in-band noise shaping of the original full-order NTF, and the stability of the SDM is not sacrificed. For a quantization gain of 60 dB per quantizer, the metastability shaping technique improves the SNDR of the SDM by 33.5 dB. The proposed metastability shaping technique breaks the metastability limitation for broadband CT $\Sigma\Delta$ ADCs, and enables CT $\Sigma\Delta$ ADCs with broader bandwidth, higher resolution and better power efficiency.

10.6 Conclusions

This chapter proposes two system-level solutions to combat the metastability errors. For CT $\Sigma\Delta$ ADCs, the metastability error is added out of the $\Sigma\Delta$ loop at the SDM output, and hence it is not shaped by the NTF. In the first approach, a novel metastability error compensation circuit is presented, which reproduces the metastability error out of the $\Sigma\Delta$ loop, measures it and compensates it in the digital domain. The power of the metastability error is linked to the quantization gain via equations. For the exemplary 4th order 9-level $\Sigma\Delta$ ADC, the MEC circuit can relax the total quantization gain requirement in the $\Sigma\Delta$ loop by 40 dB for the same 74 dB SNDR target, which can result in increasing the sampling rate and signal bandwidth. In the second approach, a metastability shaping technique is shown, which employs a 2nd ELD compensation loop to compensate the delay of another one T_S. This extra one T_S of compensated delay is used by a 2nd quantizer to generate the required additional quantization gain. Thus, the majority of the original metastability error is transferred to the quantization noise of the 2nd quantizer and shaped by the same order of NTF. For a moderate quantization gain of 60 dB per quantizer, the metastability shaping technique improves the SNDR of the exemplary 4th order SDM by 33.5 dB. Both approaches can relax the quantization gain requirement of the quantizer in one T_S timing budget significantly, and they are promising for implementation in modern CMOS technologies. These two novel approaches can overcome the metastability

limitations for broadband CT $\Sigma\Delta$ ADCs, and enables CT $\Sigma\Delta$ ADCs with broader bandwidth, higher resolution and better power efficiency.

Part III

Test chip design and validation

Chapter 11

A 6 GHz 500 MHz BW 2-1-1 MASH CT ΣΔ ADC

This chapter presents the circuit-level implementation, simulation and validation results of a 6-GHz-sampling 500-MHz-BW 2-1-1 MASH CT ΣΔ ADC test chip. Section 11.1 shows the circuit-level implementation of the test chip, including perspectives regarding schematic and layout design. Section 11.2 presents schematic and post-layout simulation results. Section 11.3 presents the measurement results. The validation results are compared to the state-of-the-art broadband CT ΣΔ ADCs in Section 11.4. Section 11.5 concludes this chapter.

11.1 Circuit-level implementation

This section presents the circuit-level implementation of a 2-1-1 MASH CT ΣΔ ADC test chip in 40 nm CMOS technology. First, this section shows the implementation block diagram of the MASH ΣΔ ADC. Afterwards, the circuit-level implementation of the main building blocks – loop filter, DACs, quantizers and clock circuitry are elaborated. This section further discusses some measurement-assistance blocks, including demultiplexers (demux) and on-chip memory. In the end, the layout floorplanning of the MASH ΣΔ ADC is presented.

For this ADC test chip, the following design concepts presented in Part II are implemented on chip:

- The current-mode multi-path ELD compensation (Chapter 7.2).
- The techniques to overcome the parasitic capacitance on the summation node (Chapter 7.3).
- The current-mode locally-time-interleaved multi-bit quantizer (Chapter 8.1).

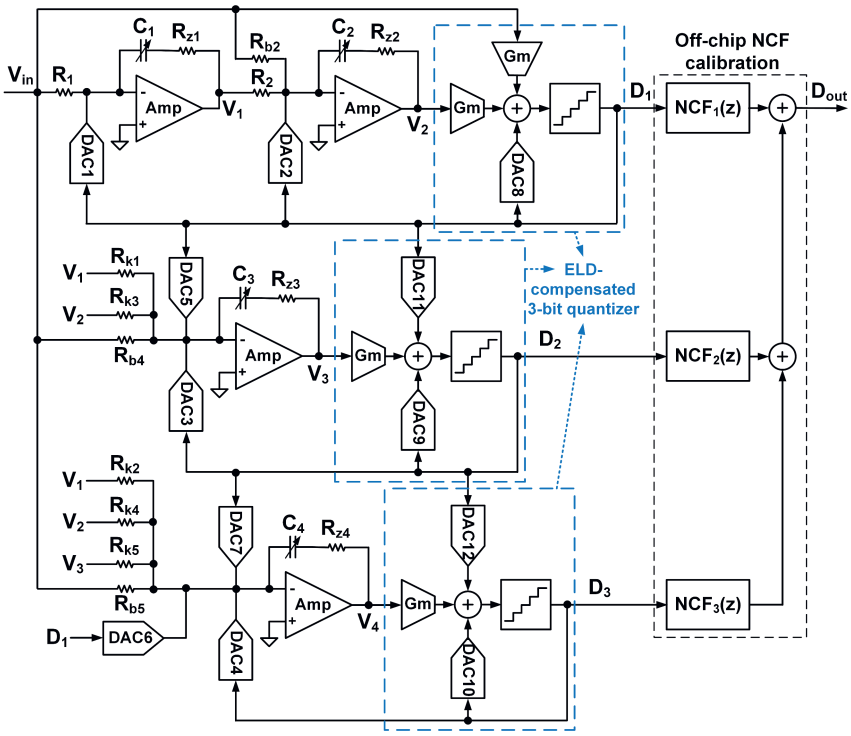


Figure 11.1: Implementation block diagram of the CT 2-1-1 MASH SDM. It is drawn as single-ended here, but the actual implementation is differential.

- The comparator offset calibration (Chapter 8.2).

Besides, the registers shown in Figure 9.6 are implemented on chip to enable applying a static sorting technique on the unit DAC elements. However, the mismatch sensor and logic in Figure 9.6 are not implemented. Moreover, the metastability error compensation technique and the metastability shaping technique shown in Chapter 10 are not implemented on chip.

11.1.1 2-1-1 MASH SDM architecture

Chapter 5 shows the CT 2-1-1 MASH SDM model in Figure 5.6. Figure 11.1 presents the implementation block diagram of the CT 2-1-1 MASH ΣΔ ADC. 4 active RC integrators compose the 2-1-1 MASH loop filter, with inverter-based amplifiers. Integration capacitors C_1 – C_4 are tunable with a {-40%, +120%} range and 1.25% step. The tunable range is up to +120% such that the designed ADC sampling rate is tunable between 3.5 GHz and 7 GHz. R_{b2}, R_{b4}, and R_{b5} implement signal feed-

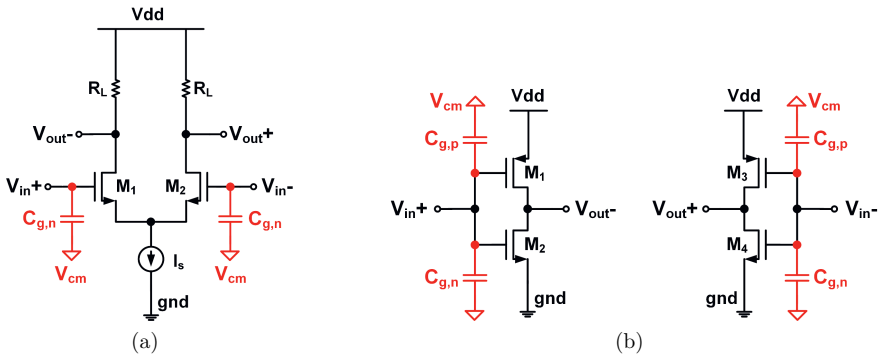


Figure 11.2: (a) A differential-pair-based amplifier. (b) A pseudo-differential inverter-based amplifier.

forward paths b_2, b_4 and b_5. The signal feedforward path b_3 is implemented by a Gm cell to the ELD summation node of the 1st loop. R_{k1} — R_{k5}, DAC 5 — DAC 7 and DAC 11 – DAC 12 feed the quantization errors into the subsequent stages. The ELD-compensated 3-bit quantizer in the 1st stage has 2 Gm cells and 1 ELD DAC in every 1-bit slice, and those in the 2nd and 3rd stages have 1 Gm cell and 2 ELD DACs in every 1-bit slice. DAC 1 – DAC 7 are referred to as main DACs, and DAC 8 – DAC 12 are referred to as ELD DACs. The noise cancellation filters (NCF_1 – NCF_3) are implemented off-chip as 10-tap FIR filters. The mismatch between the analog filter and NCF is calibrated off-chip with 10-bit coefficient accuracy, similarly to the digital calibration shown in Chapter 6.

11.1.2 Loop filter and amplifiers

The 2-1-1 MASH loop filter needs 4 amplifiers, as shown in Figure 11.1. The amplifier can be implemented either as a differential-pair-based amplifier [30] or an inverter-based amplifier [9, 102, 103, 104]. At least two dimensions for classification can be applied here: (1) differential vs. pseudo-differential; (2) current-biasing vs. voltage-biasing. Although an inverter-based amplifier can be implemented as differential and with current-biasing as well [103], the voltage headroom of the PMOS and NMOS transistors which contribute to the transconductance g_m of the amplifier is reduced compared to the pseudo-differential inverter-based amplifier with voltage-biasing [9]. A differential-pair-based amplifier with current-biasing [30] and a pseudo-differential inverter-based amplifier with voltage-biasing [9] are compared, since these two implementations are the most promising candidates as the loop filter amplifier considered in this thesis. Simplified transistor-level implementations of a 1-stage differential-pair-based amplifier with current-biasing and a 1-stage pseudo-differential inverter-based amplifier with voltage-biasing are shown in Figure 11.2a and 11.2b, respectively. Their advantages and disadvantages are compared as follows:

- Voltage headroom: In a differential-pair-based amplifier (Figure 11.2a), at least 3 transistors are stacked between the supply, if the load R_L is implemented as a PMOS transistor. If R_L is implemented as a resistor, 2 transistors and a resistor are stacked between the supply. In an inverter-based amplifier (Figure 11.2b), only 2 transistors are stacked between the supply. Thus, in a pseudo-differential inverter-based amplifier, the transistors have more voltage headroom and higher current density. This benefit of the inverter-based amplifier is more obvious when a more advanced technology node with a lower supply is considered.

- Transconductance g_m: In the differential-pair-based amplifier, only the transconductance g_m of the NMOS transistor contributes to the gain of the amplifier. In the inverter-based amplifier, the transconductance g_m of both of the NMOS transistor and the PMOS transistor contributes to the gain. With an inverter-based amplifier, a higher total g_m can be made with the same current, compared to the differential-pair-based amplifier.

- Common-mode stability: The common-mode voltage of an amplifier should be stabilized around the designed value, typically through a common-mode feedback (CMFB) loop. Since the differential-pair-based amplifier has a differential structure, it has the advantage of an easy common-mode control. The inverter-based amplifier (in Figure 11.2b) has a pseudo differential structure. The stability of the CMFB loop in an inverter-based amplifier is typically more sensitive to PVT variation and device mismatch.

- Input capacitance: In the differential-pair-based amplifier, only the gate capacitance of the NMOS transistor $C_{g,n}$ contributes to the input parasitic capacitance. In the inverter-based amplifier, the gate capacitance of both of the NMOS transistor $C_{g,n}$ and the PMOS transistor $C_{g,p}$ contributes to the total input parasitic capacitance. The ratio between the width of the PMOS transistor W_p and the width of the NMOS transistor W_n (considering they have the same length) should be optimized for speed and common-mode voltage, which depends on the CMOS technology as well. In the inverter-based amplifier designed in this thesis in 40 nm CMOS technology, the ratio W_p/W_n is optimized to be about 2.

- Output capacitance: For a differential-pair-based amplifier, the drain capacitance of the NMOS transistor $C_{d,n}$ contributes to the output capacitance. If R_L is implemented as a PMOS transistor, the drain capacitance of this PMOS transistor $C_{d,p}$ contributes to the output capacitance as well. Otherwise if R_L is implemented as a resistor, the parasitic capacitance of the resistor contributes to the output capacitance of the amplifier. For an inverter-based amplifier, the drain capacitance of both of the NMOS transistor $C_{d,n}$ and the PMOS transistor $C_{d,p}$ contributes to the output capacitance. Typically, W_p/W_n in the inverter-based amplifier is larger than W_p/W_n of the differential-pair-based amplifier (when R_L is implemented as a PMOS transistor).

- Output swing: Typically a differential-pair-based amplifier has a smaller output swing than an inverter-based amplifier. In some literature, the inverter-based amplifier is claimed to have an almost rail-to-rail output swing [105]. However, when the output swing of the inverter-based amplifier is too large (e.g. larger than $V_{dd}/2$), the non-linearity of the inverter-based amplifier can become dominant in the total non-linearity of the ΣΔ ADC, and limits the linearity of the ADC. This thesis optimizes the differential output swing of an inverter-based amplifier to be about ±0.5 V (with a 1.1 V supply).

- Linearity: The source degeneration technique can be used to improve the linearity for both of the differential-pair-based amplifier and the inverter-based amplifier [106]. In the context of the loop filter amplifier in this thesis, the amplifier is used in RC integrators (in a close-loop configuration), and its input swing is very small (about ±20 mV) since the input swing equals to the output swing suppressed by the gain of the amplifier. Together with an optimized output swing discussed in the previous point, the work of [9] demonstrates better than 100 dB linearity (THD) with inverter-based amplifiers for a signal BW of 25 MHz.

- Thermal noise: This thesis gives a quantitative comparison on the relationship between the total current I_{tot}, transconductance of the amplifier G_m and the square of thermal noise current i_{tn}^2 between the differential-pair-based amplifier and the inverter-based amplifier, used in an RC integrator in a broadband CT ΣΔ ADC. The RC integrator has a certain DC gain and 2nd pole requirement (see Chapter 6). The amplifier can be modeled as its transconductance G_m, its output capacitance C_{out}, and its output resistance R_{out}. Here C_{out} is the total capacitance at the output node of the amplifier, which is typically not dominated by the parasitic output capacitance of the amplifier itself, but dominated by the load of the amplifier (e.g. parasitic capacitance of the integration capacitor, routing capacitance and input parasitic capacitance of the back-end stage). Thus, to achieve a certain 2nd pole requirement, the amplifier has a fixed requirement on its transconductance G_m. It is discussed in the last point that the input swing of the amplifier is very small (about ±20 mV). Typically in the context of a RC integrator in a broadband CT ΣΔ ADC, the transistors which contribute to G_m are working in the saturation region. In the literature, for a MOS transistor in saturation region, the ratio between the transconductance of a transistor g_m and its drain current I_d can be calculated as $\frac{g_m}{I_d} = \frac{2}{V_{GS}-V_t}$ [59]. It shows that $\frac{g_m}{I_d}$ depends on the biasing condition. It is reasonable to assume that with a proper optimization, $V_{GS} - V_t$ has a similar value among the NMOS M_1/M_2 in Figure 11.2a, and the NMOS M_2/M_4 and PMOS M_1/M_3 in Figure 11.2b. In this analysis, the ratio between g_m and I_d is assumed to be a constant $\frac{g_m}{I_d}$, which is valid for both the NMOS M_1/M_2 in Figure 11.2a, and the NMOS M_2/M_4 and PMOS M_1/M_3 in Figure 11.2b. In the differential-pair-based amplifier, $G_m = g_{m,N}$. Since M_1 uses half of the total current I_{tot} ($I_{tot} = I_s$ in Figure 11.2a), it can be calculated that the required total current

Table 11.1: Quantitative comparison between a differential-pair-based amplifier and an inverter-based amplifier on current and thermal noise for the same transconductance G_m

	I_{tot}	i_{tn}^2
Differential-pair-based amplifier	$\frac{2 \cdot G_m}{\frac{g_m}{I_d}}$	$4kT\gamma G_m$
Inverter-based amplifier	$\frac{G_m}{\frac{g_m}{I_d}}$	$4kT\gamma G_m$

is $I_{tot} = \frac{2 \cdot G_m}{\frac{g_m}{I_d}}$ under the aforementioned assumptions. In the inverter-based amplifier, $G_m = g_{m,N} + g_{m,P}$. It can be calculated that $I_{tot} = \frac{G_m}{\frac{g_m}{I_d}}$. Furthermore, it can be calculated that in both cases the input thermal noise current square $i_{tn}^2 = 4kT\gamma G_m$ [59]. This quantitative comparison is summarized in Table 11.1. It shows that to achieve the same amplifier G_m, the inverter-based amplifier needs 2× less current than the differential-pair based amplifier. It also shows that to achieve the same input-referred thermal noise current density, the inverter-based amplifier needs 2× less current than the differential-pair based amplifier. So the inverter-based amplifier has a clear advantage (2×) for both transconductance and thermal noise. Strictly speaking, the assumption that $\frac{g_m}{I_d}$ is the same constant for both PMOS and NMOS and in both differential-pair-based amplifier and inverter-based-amplifier is not very accurate. With a proper optimization, $V_{GS} - V_t$ can be slightly different among the NMOS M_1/M_2 in Figure 11.2a, and the NMOS M_2/M_4 and PMOS M_1/M_3 in Figure 11.2b. Considering this argument, this thesis concludes that the transconductance benefit and the thermal noise benefit of the inverter-based amplifier is about 2×, compared to the differential-pair-based amplifier.

- Power supply rejection: For the differential-pair-based amplifier in Figure 11.2a, the current source I_s offers a certain power supply rejection ratio (PSRR). For the inverter-based amplifier in Figure 11.2b, since it is voltage-biased, its power supply rejection is worse than the differential-pair-based amplifier. It is more sensitive to the noise on the supply. Thus, it is beneficial to use an on-chip LDO to regulate the supply for the inverter-based amplifier [9].

Based on the aforementioned comparison and considering the requirements of the loop filter amplifiers, a pseudo-differential multi-path Miller-compensated inverter-based amplifier is used for the loop filters, mainly because of its advantages regarding the voltage headroom, transconductance and noise. A source-degenerated differential-pair-based PMOS amplifier, is used to implement the Gm cell in the ELD-compensated 3-bit quantizers, for two reasons: (1) it offers high linearity with a large input swing; (2) its input and output common-mode voltages are more suitable for the application (discussed in Chapter 7). The circuit implementation of the multi-path Miller-compensated inverter-based amplifier is shown in Figure 11.3.

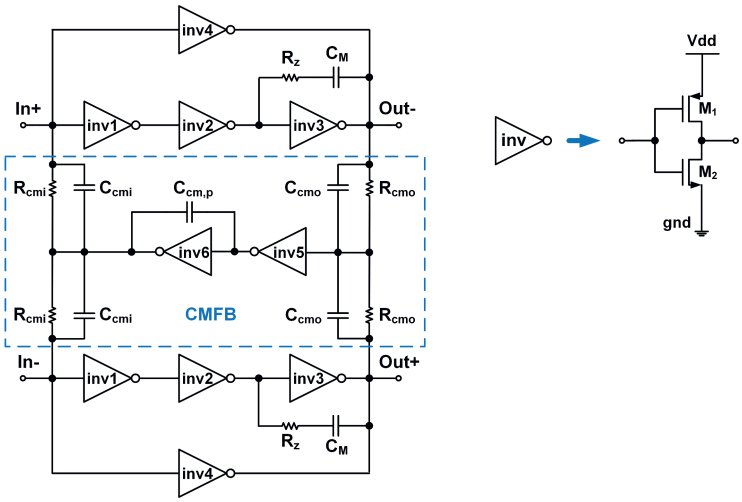


Figure 11.3: Inverter based amplifier.

The concept of the multi-path Miller-compensated structure proposed for a differential-pair-based amplifier in [107] is used in the design of the inverter-based amplifier. The differential path of the amplifier contains two paths. One path contains 3 inverters (inv 1 – inv 3), which is the high-gain low-speed path. Another path is composed of only one inverter (inv4), which is the high-speed low-gain path. A Miller capacitor C_M is inserted in parallel with inverter 3 (inv 3), to generate a dominant pole at the output node of inverter 2 (inv 2) [107]. A resistor R_z is inserted in series with C_M to generate a zero in the transfer function and to compensate the phase shift of the parasitic poles. Inverter 1, 2 and 4 use length of 80 nm, instead of the minimum length of 40 nm, to reduce their flicker noise and to achieve a higher g_m and gain. Inverter 3 uses the minimum length of 40 nm to achieve wide bandwidth, since its flicker noise is suppressed by the gain of inverter 1 and 2 when referred to the amplifier's input. All the inverters 1 – 6 have the same trip voltage, which is the input and output common-mode voltage of the amplifier. From AC noise simulation, the simulated flicker noise 3-dB-corner-frequency (when the thermal noise density equals to the flicker noise density) is about 16 MHz.

The circuit inside the dashed blue line is the common-mode feedback circuit [9]. R_{cmo} and C_{cmo} sense the output common-mode voltage. Inverters 5 and 6 make gain in the CMFB circuit. They use the minimum length of 40 nm for high-speed operation. Notice that the gain of the differential path contributes to the total gain of the CMFB loop as well. R_{cmi} and C_{cmi} form the actuator to correct the input common-mode voltage. In the CMFB circuit, C_{cmo} and C_{cmi} generate zeros in the transfer function of the CMFB loop, compensating the path shift caused by the parasitic poles. $C_{cm,p}$ is inserted in parallel with inverter 6, which creates a pole in the CMFB loop, reducing its bandwidth and increasing its gain margin. From post-layout simulation with the

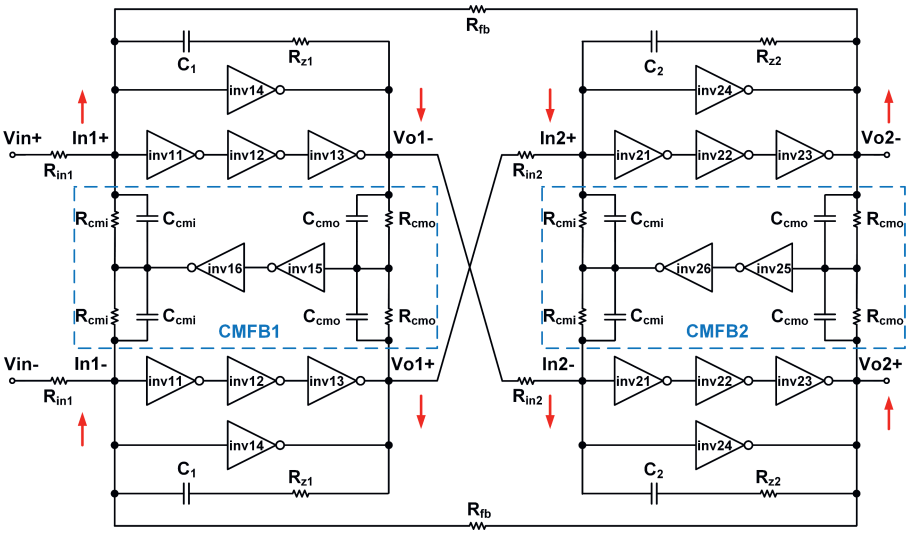


Figure 11.4: Notch implementation can lead to a positive CMFB problem.

RC integrator layout, the CMFB loop has a worst-case phase margin of 70 degree, and a worst-case gain margin of 7 dB, over the considered process corners.

Chapter 5.1 mentions that the optimized zeros are not used on the ADC test chip because of implementation difficulties. Here, this limitation is described in detail. Figure 11.4 presents the considered circuit implementation of two RC integrators and a feedback path R_{fb} to realize the optimized zeros, with the inverter-based amplifiers shown in Figure 11.3. Some implementation details in Figure 11.3, such as R_z (in parallel with C_M), C_M and $C_{cm,p}$, are not shown here for simplicity. The implementation of the optimized zeros has two problems: (1) it generates a global positive CMFB loop; (2) it generates a "big latch". These two problems are elaborated in the following.

Since the OSR is very low (OSR = 7) in this design, after the system-level optimization shown in Chapter 5.3, the UGBW of the 1st integrator is only 0.48× signal BW. It means that the noise contributed by the 2nd integrator and DAC 2 in the frequency band (0.48×BW, BW) is amplified when referred to the ADC input. The notch frequency (result from the optimized zeros) is optimized to be 0.85× BW. Because of the low OSR, the notch frequency is higher referred to F_S compared to the case with high OSR. To implement the chosen SDM architecture and parameters, the ratio R_{in1}/R_{fb} is 0.97. Calculated from the SNDR and BW target and based on an optimized noise budgeting, the resistance values are chosen to be R_{in1} = 500 Ω, R_{in2} = 500 Ω, R_{fb} = 515 Ω.

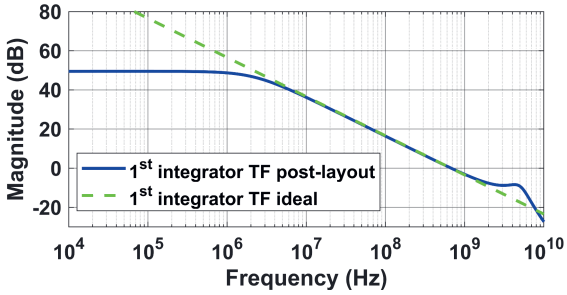
The low resistance values of R_{in1}, R_{in2} and R_{fb} cause a problem in the common-mode stability of the circuit in Figure 11.4. First, the circuits in CMFB1 and CMFB2 are

for the moment ignored, and the reaction of the differential circuit on a common-mode disturbance is analyzed. Assume a common-mode disturbance $+\Delta V_{cm}$ at the SDM input nodes Vin+/-. Then, the 1st integrator output nodes Vo1+/- see a common-mode disturbance $-G_1 \cdot \Delta V_{cm}$, where G_1 is the common-mode gain of the 1st RC integrator. A minus sign is in the formula since the differential path of the inverter-based amplifier has either 1 or 3 inverters. Similarly, the 2nd integrator output nodes Vo2+/- see a common-mode disturbance $+G_1 \cdot G_2 \cdot \Delta V_{cm}$, where G_2 is the common-mode gain of the 2nd RC integrator. The common-mode disturbance is fed back to the 1st amplifier input nodes In1+/- with a value $+\frac{R_{in1}}{R_{in1}+R_{fb}} G_1 \cdot G_2 \cdot \Delta V_{cm}$. A global positive feedback loop for the common-mode disturbance is thus formed. The directions of the common-mode disturbances in this example are drawn as red arrows in Figure 11.4 for illustration purpose. Since $\frac{R_{in1}}{R_{in1}+R_{fb}}$ is 0.49 in this design, the global positive CMFB loop is very strong. The local negative CMFB loops through the CMFB circuits of the inverter-based amplifiers (CMFB1 and CMFB2 in the figure) must be stronger than the global positive feedback loop, to keep the common-mode voltage stable. It requires very low resistance value for the R_{cmi} in the local negative CMFB loops. However, when R_{cmi} is lower, it contributes more SDM input-referred noise. The PVT variation and device mismatch make the common-mode stability more fragile.

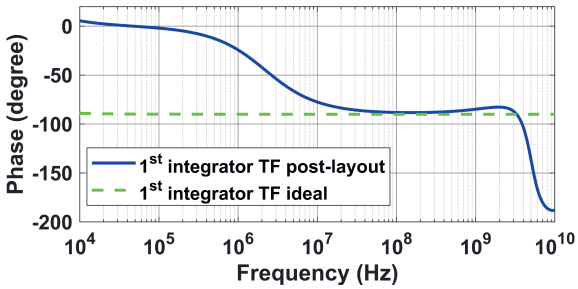
The notch implementation can cause another problem considering the transient behavior (large signal) and the start-up of the circuit. Figure 11.4 shows a big loop inv11 - inv12 - inv13 - R_{in2} - inv21 - inv22 - inv23 - R_{fb} - inv11 - inv12 - inv13 - R_{in2} - inv21 - inv22 - inv23 - R_{fb}. Since both R_{in2} and R_{fb} are very low, this loop tends to work as a "big latch" composed of 12 inverters. Actually there are more similar loops composed of $4 - 12$ inverters. In the start-up of the chip, or because of a common-mode disturbance, or due to PVT variation and device mismatch, the nodes Vo1+/- and/or Vo2+/- can be trapped at Vdd or GND. In that case, because of the "big latch", it is very difficult to get out of this state.

Notice that the global positive CMFB loop exists in many designs as a result of the implementation of the notch (optimized zeros). The unique challenge faced in this design is caused by the low OSR, broad signal BW and high SNDR (or DR) target. The stability of the common-mode feedback loop for the inverter-based amplifier is more sensitive to PVT variation and device mismatch than the differential-pair-based amplifier because of its pseudo-differential structure. In this design, the optimized zeros are not implemented. The SQNR of the ideal SDM without optimized zeros is still high enough for the SNDR target.

Figure 11.5 shows the simulated feedback transfer function of the 1st RC integrator with its post-layout extracted model. The DC gain of the 1st integrator is 49.5 dB. At $F_S/2$ (3.5 GHz), the phase of the 1st RC integrator is -93°, which means -3° phase shift compared to the ideal transfer function. At around 5 GHz, some poles and zeros cause deviations of both magnitude and phase, which are due to the limited GBW of the inverter-based amplifier, routing resistance in the amplifier layout, and



(a)



(b)

Figure 11.5: AC simulation results on the feedback transfer function of the 1st integrator: (a) magnitude (b) phase.

phase compensation techniques used in the amplifier (R_z in Figure 11.3) and in the integrator (R_{z1} in Figure 11.4). The frequency for which the phase drops to -135° (5 GHz in Figure 11.5) can be further pushed to a higher value at the cost of more power consumption, which is not needed for this design. In an open-loop testbench with the 1st inverter-based amplifier in post-layout extracted model (with load), the simulated GBW of the amplifier is about 10 GHz. The stability of the common-mode feedback loop is carefully verified for all four amplifiers. For the worst-case amplifier (in this design it is the amplifier in the 2nd integrator), over the considered process and temperature corners the worst-case phase margin of the CMFB loop is 70°, and the worst-case gain margin is 7.4 dB. All four inverter-based amplifiers in the loop filter have the same device size in the differential path for re-use purpose. The simulated power consumption of the 1st inverter-based amplifier is 18.4 mW.

11.1.3 Main DACs

In Chapter 4.3 three alternative circuit implementations of the main DAC unit element are shown in Figure 4.5. Their advantages and disadvantages (compared to the

alternatives) are recapitulated here:

- The current-steering DAC with one-side switching (Figure 4.5a) has a few advantages [30]: (1) It requires simple DAC input logic to generate the switch control voltage $D^{+/-}$. (2) It can offer high output impedance, which means that it does not need an on-chip LDO to regulate its supply. (3) It does not require a negative supply. However, the main drawback of this implementation is that it has a noise penalty compared to the other two alternatives. The non-switching current sources ($0.5I_{DAC}$) do not contribute to the differential signal, but they contribute to the noise.

- The current-steering DAC with two-side switching (Figure 4.5b) has a few advantages [16, 63]: (1) It contributes less noise compared to the current-steering DAC with one-side switching. (2) It can offer high output impedance. However, it has some disadvantages as well: (1) It requires a more complicated DAC input logic to generate those two pairs of switch control voltages. (2) In some cases, it requires a negative supply [16].

- The resistive DAC (Figure 4.5c) has a few advantages [9]: (1) It has the best noise performance among all three alternatives, even if the noise on the supply (for the resistive DAC) and the noise on the DAC biasing circuit (for current-steering DACs) are included. (2) Since the matching of resistors is generally better than the matching of transistors, it is capable to achieve much better linearity [9]. (3) Its DAC input logic can be as simple as the current-steering DAC with one-side switching. However, its main drawback is that its output impedance (almost equal to R_{DAC}) is much lower than the current-steering DACs. Thus, a low-impedance low-noise wideband LDO must be integrated on-chip to provide its supply [9].

Since the resistive DAC requires a high-performance LDO to regulate its supply, which is not available in this design (and not in the scope of this thesis either), the resistive DAC was not chosen for this ADC test chip. Based on the aforementioned comparison between one-side switching and two-side switching, it is decided to implement the main DACs as current-steering DACs with one-side switching, with the unit DAC cell similar as in [30]. The schematic of a unit cell of the main DAC with a driver is presented in Figure 11.6.

In this design, the DAC driver is composed of an inverter and a pass-gate controlled by the DAC clock $\mathrm{clkp/n}_{DAC}$. It has less delay than the DAC driver used in the work of [30], which is composed of a D-FF and two inverters, but it has less quantization gain as well. This DAC driver is designed for 7 GHz sampling rate, which means T_S is only 143 ps and the delay of the DAC driver must be minimized. Two alternative implementations of the data path are compared: (1) inverter – pass gate – DAC cell; (2) pass gate – inverter – DAC cell. The main drawback of (2) is that the mismatch of the inverters contributes to the different clock skew errors (timing errors) among the

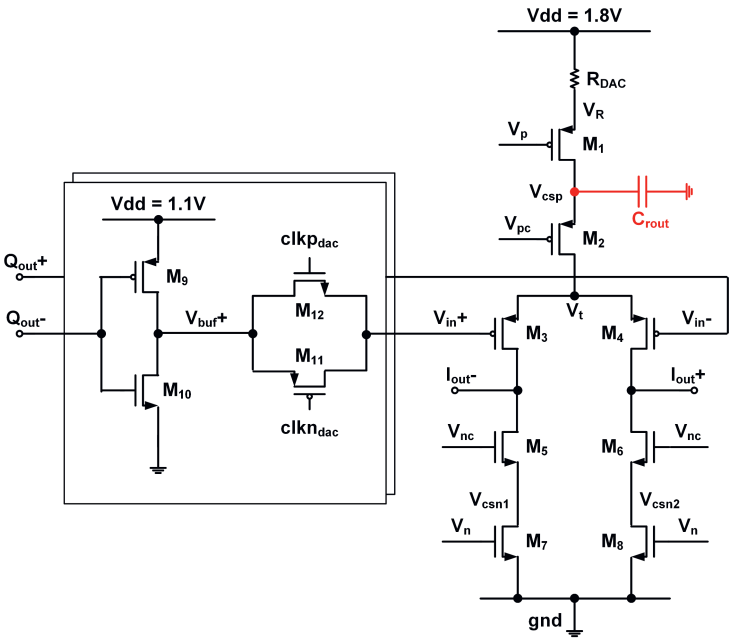


Figure 11.6: Schematic of a unit cell of the main DAC with driver.

unit DAC slices. The advantage of (2) is that the DAC switch control signals V_{in}+/- have a sharper edge than (1) with the same size of the inverter and pass gate. Based on the results of schematic Monte-Carlo (MC) simulations with device mismatch, (1) is chosen because of its better linearity.

In the layout design, the DAC switching core with cascode (M_2 - M_6), pass-gate (M_{11} - M_{12}) and inverter (M_9 - M_{10}) are defined as the "DAC core" and it is placed between the quantizers and the loop filter (see Figure 11.14). R_{DAC} and M_1 compose a source-degenerated PMOS current source. M_7 and M_8 are NMOS current sources. Both source-degenerated PMOS current source and NMOS current source are placed a bit further away from the SDM's high-speed core, since they only offer static currents (see Figure 11.14). The detailed layout floorplanning is shown in Section 11.1.7. However, since the DAC core and DAC current source are not placed together, the routing between M_1 and M_2 is about 230 μm long, which creates a parasitic capacitance of C_{rout} = 40 fF for DAC 1. The PMOS cascode transistor M_2 is designed in the deep saturation region and has a gain of 15 dB. It can suppress the effective parasitic capacitance seen by the V_t node caused by C_{rout}. However, since a large voltage headroom (238 mV) is occupied by M_2, the voltage drop on R_{DAC} is only 0.5 V. Reducing the voltage drop on R_{DAC} increases the DAC noise.

In the literature, common-centroid layout is often applied to the DAC current source which has critical matching requirement. However, in advanced CMOS technologies

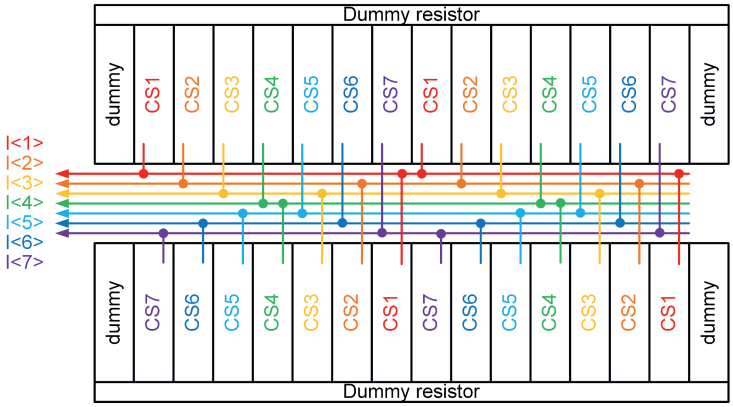


Figure 11.7: Layout floorplan of the source-degenerated PMOS current source.

(such as 40 nm and 28 nm CMOS), the layout-dependent effects (LDE), including the well proximity effect, have a significant impact on the properties of the devices [108]. In this design, the source-degenerated PMOS current sources have stringent matching requirement, since their mismatch errors contribute to DAC and ADC non-linearity. The layout floorplan of the source-degenerated PMOS current sources of DAC 1 is presented in Figure 11.7, considering both the common-centroid layout and LDE. Every unit current source I_{DAC} is divided into 4 equal pieces $\frac{1}{4}I_{DAC}$. Those 28 current source elements of $\frac{1}{4}I_{DAC}$ are placed into two rows. They are placed in a common-centroid way. The mismatch caused by LDE are canceled mutually at the first order. Dummy elements and dummy resistors are placed surrounding the active devices (in the current source element, the resistor R_{DAC} is placed close to the dummy resistor). The routing resistance and capacitance are equal among 7 unit current sources at the output nodes I<1>, ..., I<7>. Post-layout simulation with the LDE extracted shows that the systematic mismatch current among 7 unit current sources is only 23 nA, which is -83 dB referred to the nominal unit output current of 340 μA.

11.1.4 Quantizers with ELD compensation

ELD-compensated 3-bit quantizers are designed for the ADC test chip with the techniques presented in Chapter 7.2, 7.3, 8.1 and 8.2. In the layout design of the current-mode locally-TI quantizer, a limitation caused by the coupling capacitance between the input/output nodes of two TI latches is detected. Figure 11.8 shows the layout of the TI-latches, samplers and buffers of Figure 8.6 ($M_7 - M_{30}$), in an intermediate phase during the design. The routing of the TI latches' input/output nodes $Vo1^{+/-}$ and $Vo2^{+/-}$ are highlighted in yellow, blue, white and red colors. They are crossed at the samplers (the design has a pair of main FB loop samplers and a pair of fast

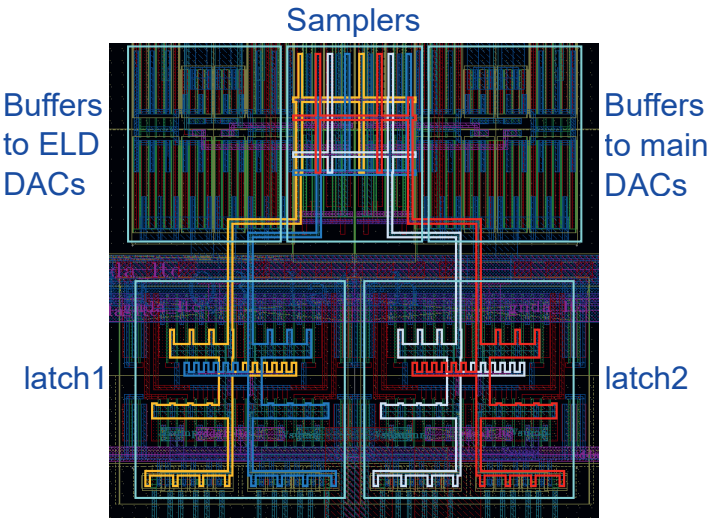


Figure 11.8: Layout of TI comparators, samplers and buffers in an intermediate design phase.

Table 11.2: Extracted coupling capacitance between TI latches' input/output nodes

	$Vo2^+$	$Vo2^-$
$Vo1^+$	201 aF	112 aF
$Vo1^-$	150 aF	166 aF

FB loop samplers as shown in Figure 8.12).

The coupling capacitance between the TI latches' input/output nodes from post-layout extraction is presented in Table 11.2. It shows that the coupling capacitance is not symmetrical. Thus, one latch output directly couples to the other latch's input. Although the unsymmetrical coupling capacitance seems very small (around 100 aF), its impact is significant. The reason is that from the loop filter output to the sampled initial condition of the comparator latch, the signal swing is attenuated by 18 dB (discussed in Chapter 8.2). Thus, the initial condition has a very small swing. On the other hand, since the latch output has a rail-to-rail swing, the error caused by the unsymmetrical coupling capacitance on the initial condition is significant. Another drawback of this layout is that the routing of $Vo1^{+/-}$ and $Vo2^{+/-}$ nodes is relatively long, which adds a relatively large routing capacitance and degrades the regeneration time constant of the latch.

Although the coupling capacitance between latch 1 and latch 2 can be reduced by revising the layout, it sacrifices the local floorplanning and it adds more routing capacitance to the sampler's output nodes. The solution used in this thesis is to add

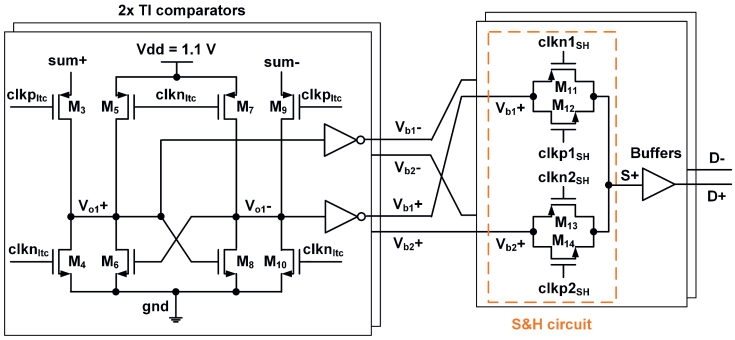


Figure 11.9: Schematic of TI comparators, an additional buffer, and samplers.

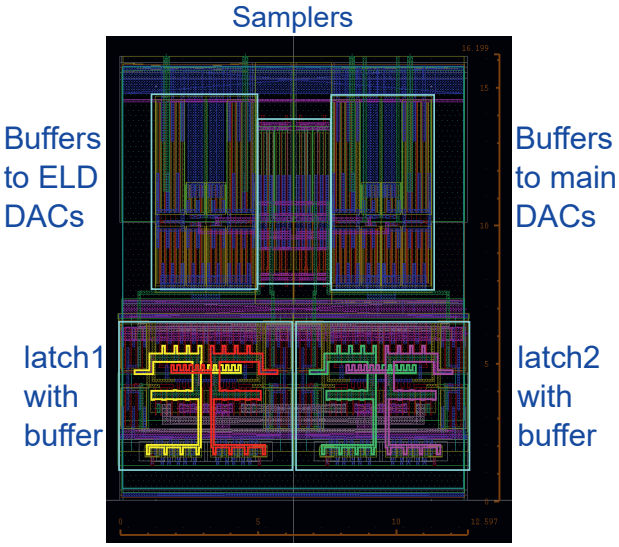


Figure 11.10: Final layout of TI comparators, the additional buffer, samplers and buffers.

a buffer between the latches' input/output nodes and the samplers. A NMOS buffer with PMOS load is used to minimize the parasitic capacitance on the latch output nodes. The schematic of the TI comparators, the additional buffer and samplers is presented in Figure 11.9.

Figure 11.10 shows the final layout of the TI-latches, the additional buffer, samplers and buffers. It shows that the routing of the input/output nodes of latch 1 (highlighted in yellow and red color) is separated more from the routing of the input/output nodes of latch 2 (highlighted in green and magenta color), compared to Figure 11.8. Post-layout extraction and simulation show that the coupling capacitance between

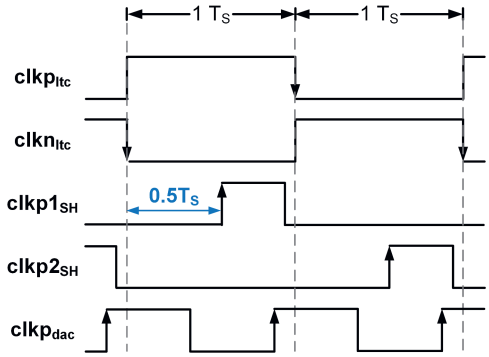


Figure 11.11: Clock signals for the MASH SDM.

$Vo1^{+/-}$ and $Vo2^{+/-}$ nodes is negligible.

11.1.5 Clock

The 2-1-1 MASH ΣΔ modulator needs a few clock signals. As shown in Chapter 8.1, the current-mode locally-time-interleaved quantizers need three pairs of clock signals – $\text{clkp}_{ltc}/\text{clkn}_{ltc}$, $\text{clkp1}_{SH}/\text{clkn1}_{SH}$, $\text{clkp2}_{SH}/\text{clkn2}_{SH}$. The clock phases clkn1_{SH} and clkn2_{SH} are locally generated inside the quantizers from their opposite phases. Section 11.1.3 shows that the main DACs require clock signals $\text{clkp}_{dac}/\text{clkn}_{dac}$. Figure 11.11 presents an overview of the clock signals for the MASH SDM. In this figure, clkn_{dac} is not shown, which is the opposite phase of clkp_{dac}.

The TI latch clocks $\text{clkp}_{ltc}/\text{clkn}_{ltc}$ have a frequency of $F_S/2$ and a duty cycle of 50%. Quantizer sampling clocks clkp1_{SH} and clkp2_{SH} have a frequency of $F_S/2$ and a duty cycle of about 20%. The sampling clocks clkp1_{SH} and clkp2_{SH} become low ∼15 ps earlier than the starting of the reset phase of the corresponding latch. The DAC clock $\text{clkp}_{dac}/\text{clkn}_{dac}$ have a frequency of F_S and a duty cycle of 50%. The rising edge of clkp_{dac} is ∼15 ps earlier than the falling edge of $\text{clkp}_{ltc}/\text{clkn}_{ltc}$, which equals to the DAC clock to DAC output (current) delay.

Figure 11.12 shows part of the clock circuitry on the 2-1-1 MASH ΣΔ modulator test chip. It shows the clock distribution and phase generation for the clock signals required by the main DACs and the quantizers. The clock signals needed by the demux, the calibration logic for the comparator offset calibration, the digital top-level control and memory are not shown in this figure; they are generated with some clock dividers and buffers. The clock circuitry shown in Figure 11.12 can be divided into two groups – a "clock receiver" and a "clock buffer". The clock receiver is designed to receive a 3.5 GHz – 7 GHz differential sine wave generated off-chip, and translate it to a close-to-square-wave differential clock signal. The clock input signals $\text{clkp}_{in}/\text{clkn}_{in}$ are AC coupled to the 1st inverter's input through a capacitor C_{AC}. At

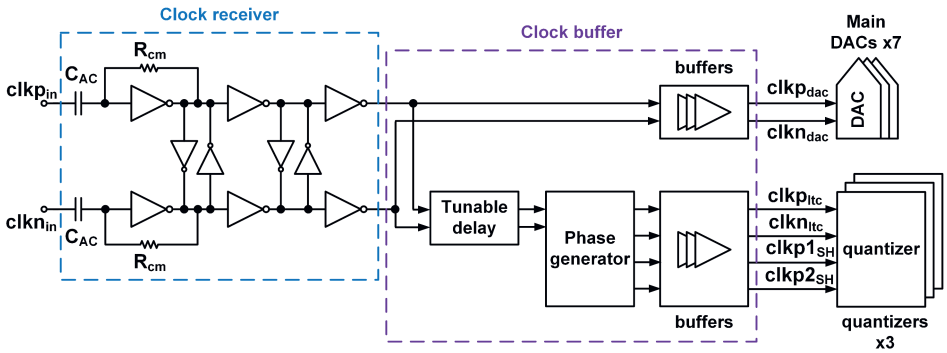


Figure 11.12: Clock circuitry.

the input of the 1st inverter, the common-mode voltage is determined by the inverter itself through a resistor R_{cm}. Cross-coupled inverters (weaker than the 1st and 2nd inverter) are added at the 1st and 2nd inverter's outputs for clock-skew correction. At the output nodes of the clock receiver, the rising and falling edges (10% to 90%) are ∼40 ps from post-layout simulation.

In the "clock buffer" the circuits for the generation and distribution of DAC clocks and quantizer clocks are separated. The DAC clock path only contains a few buffers, such that low clock jitter is achieved. The quantizer clock path contains a tunable delay block, a phase generator, and some buffers. With the tunable delay block, the relative delay between the DAC clocks and the quantizer clocks can be tuned in a range of $0 \sim 2\times T_S$ with a step of 5 ps (for $F_S = 7$ GHz, simulated at TT corner, 65°C). The phase generator generates four clock signals/phases – clkp_{ltc}, clkn_{ltc}, clkp1_{SH} and clkp2_{SH}. The buffers drive three quantizers as load. From post-layout simulations, the rising/falling edges (10% to 90%) of the clock signals seen by the main DACs and quantizers are about 20 ps.

11.1.6 Measurement-assistance blocks

The MASH SDM test chip has digital outputs from three SDM stages (D_1, D_2, D_3 in Figure 11.1). Totally, 21 bit of unary-coded output at F_S is generated. It is very challenging to capture and synchronize the output data at F_S (7 GHz) directly in the measurement. To facilitate the data capture, the MASH SDM output is demultiplexed 32× and stored in an on-chip memory. Figure 11.13 shows a block diagram of the MASH SDM, demux and on-chip memory. Data rates are indicated in the figure for $F_S = 7$ GHz. The main DAC switch control signals (V_{in}+/- in Figure 11.6) are used as the SDM digital output signals. They are buffered and then subsequently driving a local demux (×4). After the local demux, the frequency of the data is reduced to 1.75 GHz ($F_S/4$), and it can be routed for a few hundred μm to the remote demux (×8).

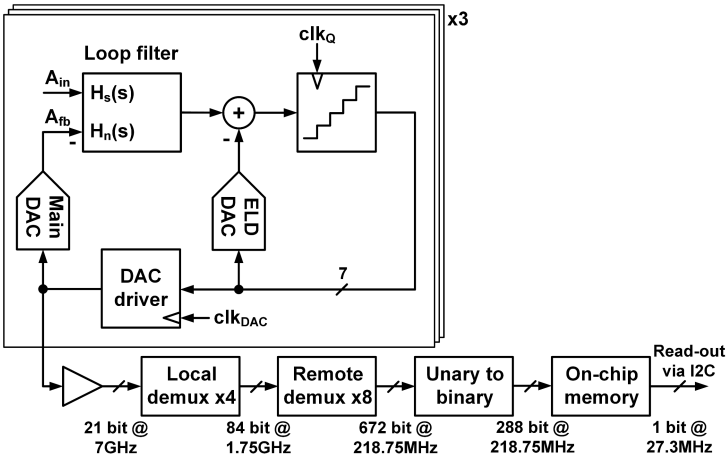


Figure 11.13: Block diagram of SDM, demux and on-chip memory.

After the remote demux, the frequency of the data is further reduced to 218.75 MHz ($F_S/32$). At this frequency, the 7-bit unary-coded quantizer output is converted to a 3-bit binary-coded format, to save memory space. This data is saved in an on-chip memory (1.5 Mbit). In the measurement, the data in the memory is read out via an I2C interface at 27.3 MHz ($F_S/256$).

11.1.7 Layout floorplanning

Layout floorplanning is critical for broadband GHz-sampling ADCs. Figure 11.14 shows the micrograph of the ADC test chip. The digital blocks and analog blocks are separated in the floorplanning. The digital blocks include the digital control and memory block, and the quantizer calibration block. The remaining blocks are analog (or mixed-signal) blocks.

The key strategy in this layout design is to make the ADC high-speed core layout as compact as possible. The ADC high-speed core is defined as the loop filter, the ELD-compensated quantizer cores, the main DAC cores, local clock buffers, and the local demux.

The ELD-compensated quantizer's high-speed core contains the high-speed circuitry of the quantizer, including local clock buffers, Gm cells, ELD summation nodes, reference DAC core, ELD DAC core, TI latches, samplers and buffers, coarse calibration circuit, calibration DAC core, coarse calibration control circuit, etc. The ELD DAC, reference DAC and calibration DAC are implemented similarly (see Figure 8.6 and 8.12). The current sources $I_{dac,u}$, $I_{ref,u}$ and $I_{cali,u}$ are implemented as cascaded NMOS current sources. For the ELD DAC, reference DAC and calibration DAC,

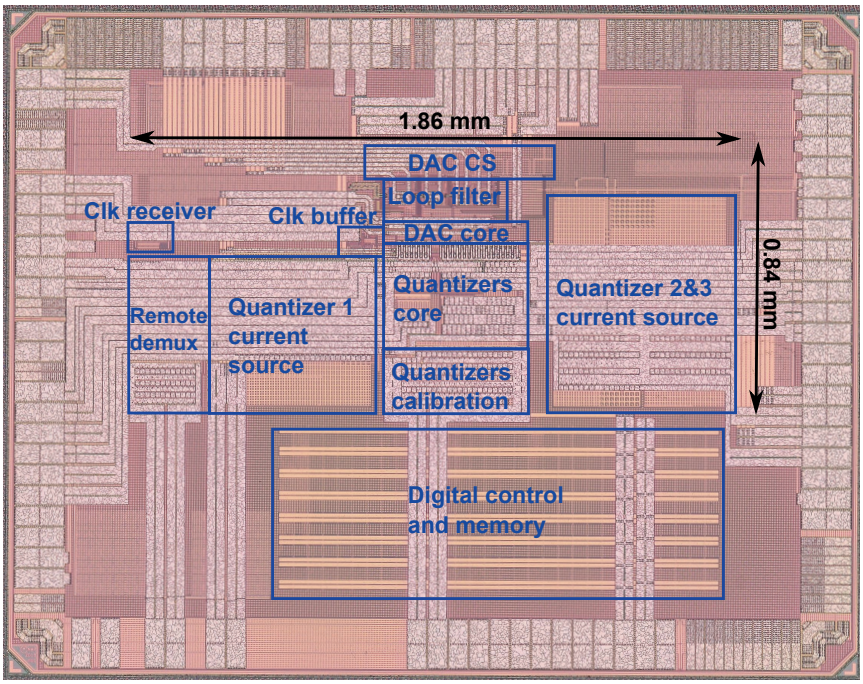


Figure 11.14: Chip micrograph.

their switches and NMOS cascode transistors are defined as their high-speed core (DAC core), e.g. M_3, M_4 and M_{31} for the ELD DAC in Figure 8.6. The NMOS current source transistors (e.g. M_{32} in Figure 8.6) are placed further away in the layout floorplan, since they do not have high-speed switching. They are matching critical and they have large gate area.

As shown in Figure 11.14, the quantizer's high-speed core is placed close to the main DAC cores and the loop filter. The other auxiliary circuitry in the quantizers, e.g. the fine calibration control circuit in Figure 8.12, is placed between the quantizers' high-speed core and the quantizer calibration.

The static circuitry, including the main DACs' current source and the quantizers' current source, is placed around the ADC's high-speed core. As shown in Figure 11.14, the ADC's high-speed core has an area of about 400 μm $\times$ 400 μm.

The ADC architecture presented in Figure 11.1 shows an additional challenge in the floorplanning of this design – it has two additional ELD DACs (DAC 11 and DAC 12) compared to other MASH architectures, e.g. the work of [16]. Figure 11.15 shows the local floorplanning of the 1st and 2nd quantizer core and the ELD DAC cores (DAC 8, DAC 9 and DAC 11) in an intermediate design phase. The layout of the 1st quantizer is divided into 7 slices, in the same way as done with its schematic. Every

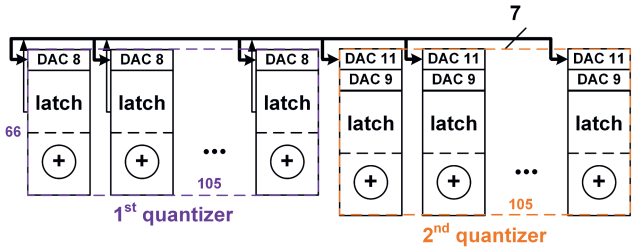


Figure 11.15: Local floorplanning of the 1st and 2nd quantizer cores and the ELD DAC cores (DAC 8, DAC 9 and DAC 11) in an intermediate design phase. "7" indicates that the 1st quantizer has a 7-bit unary-coded output. The actual implementation is differential.

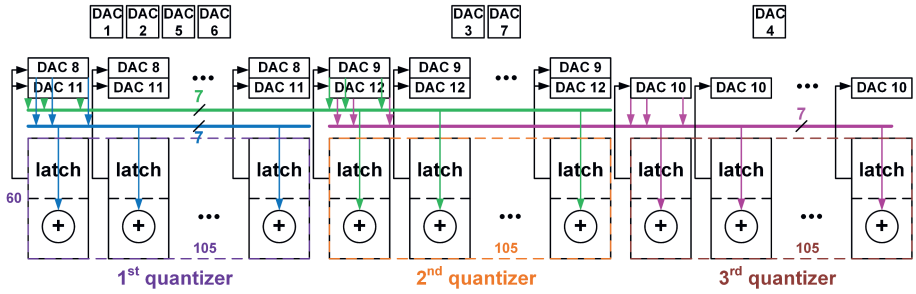


Figure 11.16: Final floorplanning of quantizer cores, ELD DAC cores and main DAC cores. "7" indicates 7 single-ended analog routing lines. The actual implementation is differential.

slice contains the TI latches, an ELD summation node, the ELD DAC core, etc. The ELD DAC core unit cells, whose output currents are added to the summation node of the slice, are placed in that slice. The x-dimension of the 1st quantizer core is 105 μm, and its y-dimension is 66 μm. The routing of the 1st quantizer's output to DAC 8 and DAC 11 is shown explicitly ($D^{+/-}$ nodes in Figure 8.6). Layout design shows that the total routing length of $D^{+/-}$ nodes is about 420 μm (for every bit), and the extracted routing capacitance is about 20 fF. The buffers between the fast FB loop sampler and $D^{+/-}$ nodes cannot drive this extra load. Increasing the size of the buffers adds load to the latch, and increases its regeneration time constant.

This problem is solved by changing the layout floorplanning. The final floorplanning of the quantizer cores, ELD DAC cores and main DAC cores is presented in Figure 11.16. In the final floorplanning, the ELD DAC core unit cells who are driven by the 1-bit quantizer output of the slice, are placed in that slice. The routing of $D^{+/-}$ nodes is significantly reduced, and the routing capacitance is reduced from 20 fF to 4 fF from post-layout extraction. This is achieved at a cost that the routing length

of the ELD DAC output current is significantly increased. Since the routing of the ELD DAC output current is part of the routing of the ELD summation node, the routing capacitance on the summation node is increased by about 20 fF compared to the old layout floorplanning in Figure 11.15. Fortunately, the problems caused by the additional routing capacitance on the summation node can be overcome by the techniques proposed in Chapter 7.3. From Figure 11.15 to Figure 11.16, the trade-off is that the long routing is moved from the $D^{+/-}$ nodes to the ELD DAC output current nodes. A large routing capacitance of about 20 fF is also moved accordingly. This routing capacitance is a load to a voltage signal $D^{+/-}$ in Figure 11.15, and it becomes a load to a current signal of the ELD DAC output current in Figure 11.16. In Figure 11.16 the placement of the main DAC cores (DAC 1 – DAC 7) is presented as well.

11.1.8 Challenges in the layout design phase

In this thesis, a traditional design flow for the MASH SDM test chip design is followed:

1. ΣΔ ADC architecture design, system-level modeling and simulations in Matlab/Simulink.
2. Schematic design and verification. The transistor layout parasitic model ('presimu') provided by the foundry is used. TT corner 65°C is considered. Monte-Carlo simulations with local mismatch are performed.
3. Layout design and verification. Post-layout extraction is done with the option 'RC coupled'. TT corner 65°C is considered.
4. Chip measurement.

In the layout design phase, a lot of challenges were encountered, mainly due to the following reasons:

1. The parasitics estimated by the 'presimu' are too optimistic. Post-layout extraction of a layout of the transistors gives more parasitics than 'presimu'.
2. Routing capacitance, coupling capacitance, and routing resistance cause problems in high-speed loops.

To overcome those challenges in the layout design phase, both schematic design and layout design of multiple blocks have several iterations. The maximal applicable sampling rate is reduced from 8.4 GHz in schematic simulations, to 7 GHz in post-layout simulations. Since the circuit of multiple blocks has to be sized up 2×, 4× or even more to achieve the target sampling rate and signal bandwidth, the power consumption of the SDM and clock increases by about 4× from schematic simulations

(147 mW) to post-layout simulations (619 mW). This section gives a few examples to elaborate it in more details.

In this design, the ELD-compensated quantizers consume the majority of the total power (see Figure 11.23), since the ELD-compensation loop is implemented in the quantizers. In the schematic design phase, the current source used in the input Gm cell of the 1st quantizer has a value $I_S = 300\ \mu A$ (see Figure 8.6). In the layout design phase, the total routing capacitance on the summation node is about 50 fF. To be able to drive this additional load, the current source of the Gm cell is increased by $4\times$ to $I_S = 1.2$ mA.

In the layout design phase, the routing capacitance on the buffered 1st quantizer output nodes ($D^{+/-}$ nodes in Figure 8.6) is about 15 fF in the main feedback loop and 28 fF in the fast feedback loop ($D^{+/-}$ nodes are separated for main feedback loop and fast feedback loop, see Figure 8.12). The additional load from routing capacitance can be easily solved by adding some buffers with increased driving ability in lower speed ADCs. However, in this design, the target sampling rate in the layout design phase is 7 GHz, which means $T_S \approx 143$ ps. One additional inverter in the data path from the quantizer to the main DAC adds about 15 ps delay in post-layout simulations. This design allows only three buffers (one NMOS buffer with PMOS load, two CMOS buffers) and two pass-gates between the comparator core and the main DAC core, without any room to insert even one additional buffer. Thus, to drive the additional routing capacitance, the buffers, pass-gates, comparator core, Gm cell, ELD DAC, reference DAC, etc. have to be sized up and re-optimized. As a final result of this re-optimization, the transistor size of the comparator core (M_9 - M_{12} in Figure 8.6) is increased by about $4\times$, and the transistor size of the CMOS buffer driving $D^{+/-}$ nodes (M_{29} - M_{30} in Figure 8.6) is increased by about $6\times$. The simulated regeneration time constant of the comparator core in schematic design phase after optimization (in schematic simulation) is about $\tau = 5.5$ ps. The simulated regeneration time constant of the comparator core in layout design phase after optimization (in post-layout simulation) is about $\tau = 6.5$ ps. The regeneration time constant is degraded, since the self-loading of the overall ELD compensation loop (comparator core - sampler - buffers - ELD DAC - comparator core) is dominant. Even if the transistor size of the comparator core would be doubled again, after re-optimization of the whole ELD compensation loop, the improvement on the regeneration time constant is negligible.

In the layout design phase, because of the additional device parasitic capacitance, routing capacitance, routing resistance (including supply and ground routing), and increased load (from quantizers), the GBW of the loop filter amplifier with load is reduced, and the phase shift of the loop filter transfer functions at $F_S/2$ increases. To keep the stability and resolution of the MASH SDM, the transistor size of the loop filter amplifiers (which are inverter-based amplifiers) is increased by about $2\times$. A similar trend is also observed in the main DACs and clock circuitry.

Based on the aforementioned elaboration, this thesis concludes that, to achieve the target of 500 MHz BW, the MASH ADC test chip finally needs to be designed very

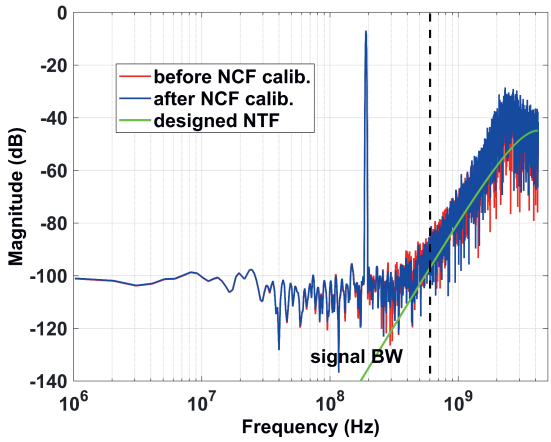


Figure 11.17: Simulated output spectrum with MASH SDM and clock at schematic level (TT corner, 65°C, no mismatch, no noise).

close to the speed boundary of the chosen 40 nm CMOS technology. To achieve the target sampling rate and signal bandwidth, the power consumption increases not linearly, but exponentially. It can explain why the figure-of-merit of this design is worse than the designs whose signal BW and peak SNDR (or DR) performance are not bounded by technology performance (see Chapter 11.4).

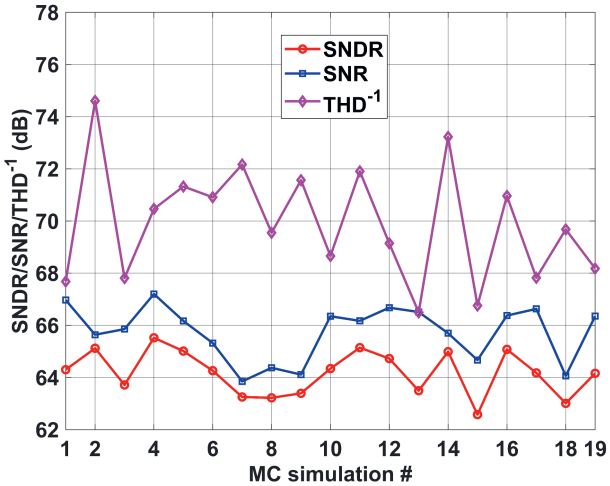
11.2 Simulation results

This section presents transistor-level simulation results of the 2-1-1 MASH ΣΔ ADC test chip. First, schematic simulation results are presented. Afterwards, post-layout simulation results are shown.

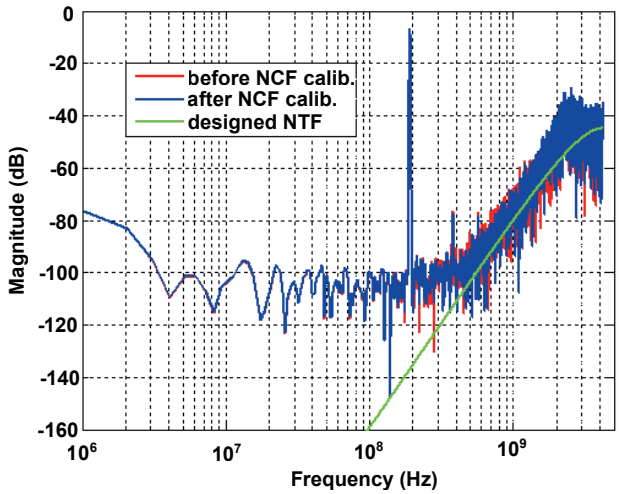
11.2.1 Schematic simulation results

For the following schematic simulation results, the 2-1-1 MASH ΣΔ modulator (including loop filter, ELD-compensated quantizers, main DACs) and clock distribution circuit are modeled at schematic level. The transistor layout parasitic model ('presimu') provided by the foundry is used. TT corner 65°C is considered. In the schematic simulations, ADC sampling frequency is $F_S = 8.4$ GHz, OSR = 7, and signal BW = 600 MHz. Input signal is a sine wave with frequency $f_{in} = 190.75$ MHz, and amplitude $A_{in} = 0.7$ V.

Figure 11.17 shows the simulated output spectrum with the MASH SDM and clock



(a)

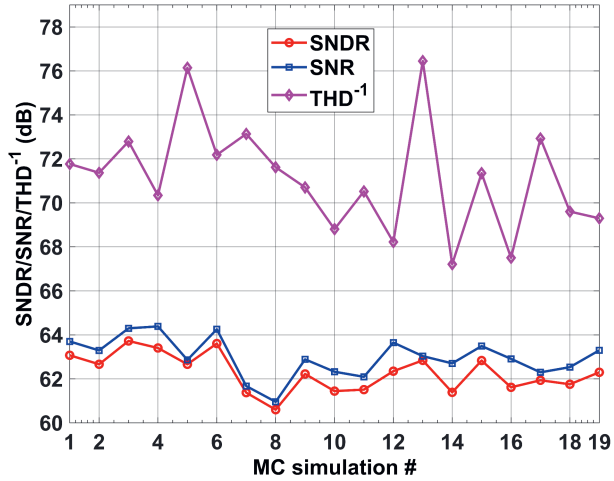


(b)

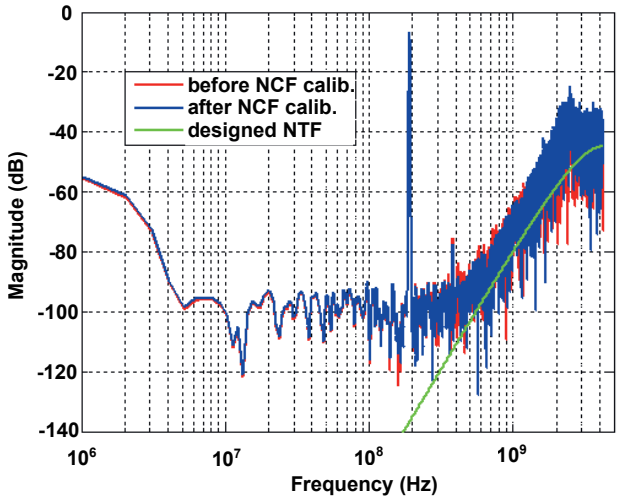
Figure 11.18: Monte-Carlo simulation results with MASH SDM and clock at schematic level, with device mismatch only on the main DACs: (a) SNDR, SNR and THD of 19 independent simulations; (b) typical output spectrum.

at schematic level, without device mismatch and noise. The simulated SQNR is 69 dB for a signal BW of 600 MHz.

Monte-Carlo simulation with MASH SDM and clock at schematic level, with device mismatch only on the main DACs, are performed. Figure 11.18a presents the simu-



(a)



(b)

Figure 11.19: Monte-Carlo simulation results with MASH SDM and clock at schematic level with noise, with device mismatch only on the main DACs: (a) SNDR, SNR and THD of 19 independent simulations; (b) typical output spectrum.

lated SNDR, SNR and THD of 19 independent MC runs after calibration of the NCF coefficients. The simulated SNDR = 64.2 ± 0.9 dB (mean $\pm\sigma$), SNR = 65.7 ± 1 dB (mean $\pm\sigma$), and THD = -69.9 ± 2.2 dB (mean $\pm\sigma$). Figure 11.18b shows one typical output spectrum from this MC simulation, where SNDR = 64.2 dB, SNR = 66.6 dB and THD = -67.8 dB.

Table 11.3: Overview of noise and distortion contributions from schematic simulations

Item	noise and distortion power	
	in [V^2]	referred to signal power of A_{in} = 0.7 V sine input
Quantization noise	3.08×10^{-8}	-69 dB
Thermal and flicker noise	5.11×10^{-8}	-66.8 dB
Clock-jitter-introduced error	6.7×10^{-9}	-75.6 dB
DAC-mismatch-introduced error	6.23×10^{-8}	-65.9 dB
Total in-band noise and distortion	1.51×10^{-7}	-62.1 dB

Monte-Carlo simulation with MASH SDM and clock at schematic level, with device mismatch only on the main DACs, are performed with noise as well. Figure 11.19a shows the simulated SNDR, SNR and THD of 19 independent MC runs after calibration of the NCF coefficients. The simulated SNDR = 62.3 ± 0.9 dB (mean $\pm\sigma$), SNR = 63 ± 0.9 dB (mean $\pm\sigma$), and THD = -71.2 ± 2.5 dB (mean $\pm\sigma$). Figure 11.19b shows one typical output spectrum from this MC simulation, where SNDR = 62.3 dB, SNR = 63.3 dB and THD = -69.3 dB.

An overview of the noise and distortion contributions from schematic simulations with an A_{in} = 0.7 V sine input is presented in Table 11.3. A peak SNDR of 62.1 dB is expected for a signal BW of 600 MHz (F_S = 8.4 GHz). The peak SNDR is mainly limited by the DAC mismatch and transient noise (due to thermal noise and flicker noise).

11.2.2 Post-layout simulation results

For the following post-layout simulation results, the 2-1-1 MASH ΣΔ modulator and clock distribution circuit are post-layout extracted models (RC coupled). TT corner 65°C is considered. In the post-layout simulations, ADC sampling frequency is F_S = 7 GHz, OSR = 7, and signal BW = 500 MHz. The sampling frequency has to be reduced from 8.4 GHz to 7 GHz, otherwise the main feedback loop cannot be closed in 1 T_S. Input signal is a sine wave with frequency f_{in} = 158.95 MHz, and amplitude A_{in} = 0.7 V.

Figure 11.20 shows the simulated output spectrum with the MASH SDM and clock post-layout extracted, without device mismatch and noise. The simulated SQNR is 60.1 dB for a signal BW of 500 MHz. Notice that the out-of-band NTF peaking in the blue spectrum is an artifact from the calibration of the NCF coefficients. In the red spectrum (before calibration of the NCF coefficients), the out-of-band NTF peaking

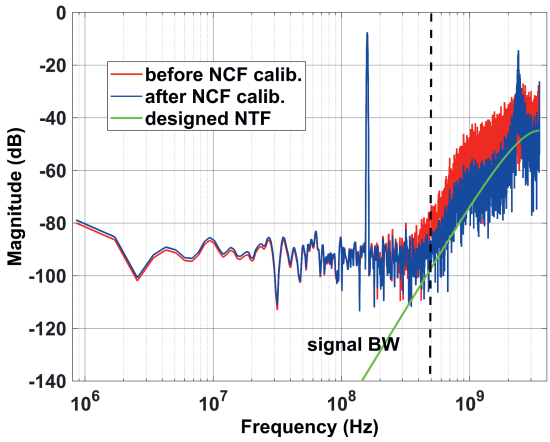


Figure 11.20: Simulated output spectrum with MASH SDM and clock post-layout extracted (TT corner, 65°C, no mismatch, no noise).

is much lower.

Assuming the transient noise, clock-jitter-introduced error and DAC-mismatch-introduced error are the same as in the schematic simulations, the expected SNDR with SDM and clock post-layout extracted is 58.3 dB for a signal BW of 500 MHz ($F_S = 7$ GHz). The simulated power consumption of MASH SDM and clock is 619 mW.

11.3 Test chip validation

The CT 2-1-1 MASH SDM test chip has been fabricated in a 40 nm CMOS technology. For thin-oxide transistors, only the sub-type of super-low-threshold-voltage and normal-threshold-voltage transistors are used. The total area of the SDM, clock circuitry and demux is 1.56 mm^2, in which the area of the SDM and clock buffer is 1.34 mm^2. This section presents the measurement results. Figure 11.21 shows a photo of the validation board with a test chip sample during the measurement.

A low-phase-noise signal generator (Keysight E8257D) is used to generate the required clock signal [109]. The calculated clock jitter (RMS value) for a 6 GHz output clock signal from this clock generator is about 29 fs. The simulated on-chip clock jitter contribution for the DAC clock is about 44 fs. Thus, the calculated total clock jitter for the DAC clock is about 53 fs, which is below the clock jitter specification of 100 fs.

The MASH SDM test chip has been measured with 4 GHz, 5 GHz and 6 GHz sampling rates. This chapter presents the measurement results of single-tone test with 4 GHz

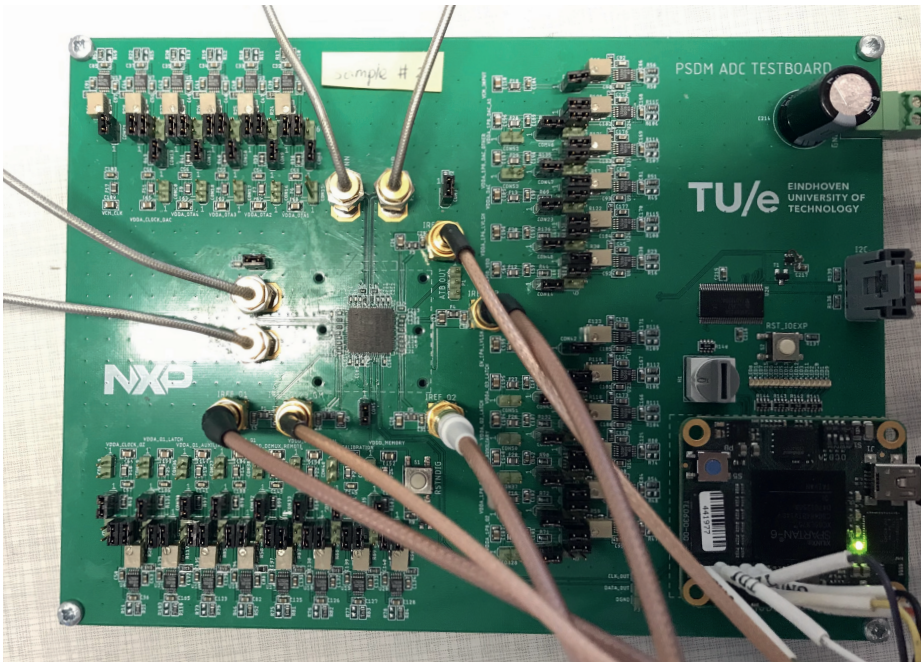


Figure 11.21: Validation board with a test chip sample during the measurement.

and 6 GHz sampling rates, and the measurement results of two-tone test with 5 GHz sampling rate. The possible reasons why the maximal applicable sampling rate in the measurement is lower than the simulation is explained in Section 11.3.5.

11.3.1 Comparator offset calibration

The comparator offset calibration presented in Chapter 8.2 is implemented on chip. In the calibration mode, the main DAC input should be disconnected from the quantizer output. However, adding a switch in the data path from the quantizer to the main DAC as shown in Figure 8.12 increases the propagation delay from the quantizer to the main DAC. This switch is not implemented on chip. In the measurement, in the calibration mode, the supplies of the loop filter and the main DACs are OFF. The supplies of the quantizers, digital top-level control, and calibration logic are ON. The input common-mode voltage of the quantizer is generated by a diode-connected inverter (which is a replica of one inverter used in the inverter-based amplifier).

In the measurement, the following calibration procedure is used, which is defined by the digital top-level control:

1. Coarse calibration: latch 1 → latch 2 → latch 1 → latch 2 → latch 1.

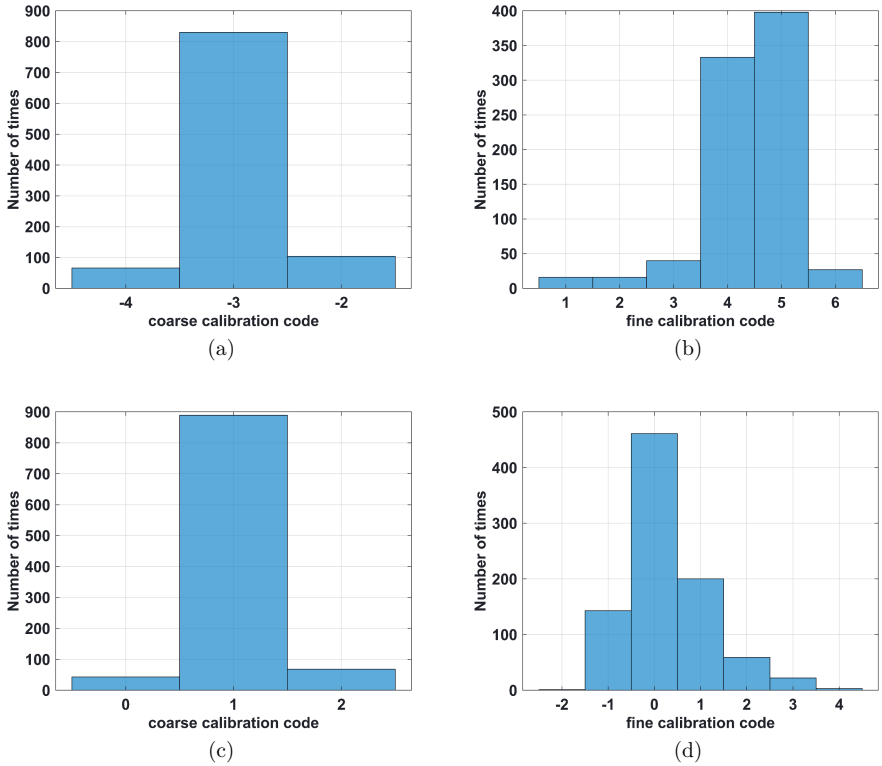


Figure 11.22: Histogram of the calibration codes in 1000 independent measurements: (a) coarse calibration code for latch 1 of the 4th comparator in the 1st quantizer; (b) fine calibration code for latch 1 of the 4th comparator in the 1st quantizer, when its coarse code = -3; (c) coarse calibration code for latch 2 of the 4th comparator in the 1st quantizer (d) fine calibration code for latch 2 of the 4th comparator in the 1st quantizer, when its coarse code = 1.

2. Fine calibration: latch 1 → latch 2 → latch 1 → latch 2 → latch 1.

In the measurement, it is found that the calibration codes are not always the same when the calibration is repeated (for the same test chip sample, the same temperature and voltage). For the same test chip sample, 1000 independent comparator offset calibrations are performed (each time the test chip is reset at the beginning). The histograms of the coarse and fine calibration codes for latch 1 and latch 2 of the 4th comparator in the 1st quantizer are presented in Figure 11.22, which is a typical case among the comparators of three quantizers. Figure 11.22a and 11.22c show that even the coarse calibration codes have a spread over 3 codes (the spread is 2 codes for some of the other latches). Typically one coarse calibration code is dominant,

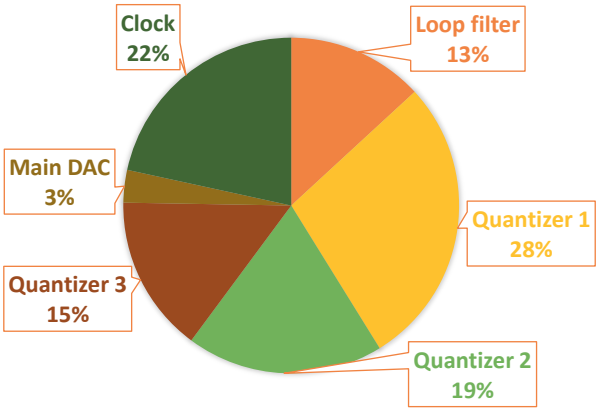


Figure 11.23: Power breakdown when $F_S = 6$ GHz.

e.g. the dominant coarse code is -3 in Figure 11.22a. Figure 11.22b and 11.22d show the histograms of the fine calibration codes, when their coarse calibration code is the dominant code. With the same coarse calibration code, the fine calibration code typically has a spread of $6 \sim 7$ codes. The distribution of the fine calibration code is close to a Gaussian distribution, with one or two dominant codes. Thermal noise causes the spread of coarse and fine calibration codes. Generally, the performance of the $\Sigma\Delta$ ADCs is not sensitive to the thermal noise of the quantizer, since its thermal noise power is typically much lower than the quantization noise power. For this reason, the quantizer thermal noise is relatively large compared to the fine calibration step, and it directly influences the calibration code found by the calibration procedure. The error in the comparator offset calibration caused by the thermal noise can be averaged out by performing a large amount of independent calibrations, and choosing the calibration codes (the combination of a coarse code and a fine code) which appear most frequently. Since redundancy is built in between the fine calibration range and the coarse calibration step, even if the coarse calibration code has a $+1$ or -1 error due to thermal noise, the fine calibration range is large enough to find a correct fine calibration code to compensate the error.

11.3.2 Power consumption

The MASH SDM uses 1.1 V supply, except for DAC 1 $\sim$ DAC 7 and quantizer input Gm cells that use 1.8 V supply. The power consumption of the $\Sigma\Delta$ modulator and the clock buffer is 574 mW when operating at $F_S = 6$ GHz, and 506 mW when operating at $F_S = 4$ GHz. The clock receiver has a power consumption of 17 mW when operating at $F_S = 6$ GHz, and 11 mW when operating at $F_S = 4$ GHz. The power and area of the clock receiver is excluded in the total SDM power and area in the benchmarking (Section 11.4), since it is not required when the $\Sigma\Delta$ ADC is

integrated in a receiver/transceiver product (the ADC clock is typically generated by an on-chip phase-locked loop (PLL) in a receiver/transceiver (SoC) product).

Figure 11.23 shows the power breakdown of the $\Sigma\Delta$ modulator and the clock buffer when F_S = 6 GHz. Since the ELD compensation is implemented in the quantizers, three quantizers consume 62% of the total power of the SDM and clock.

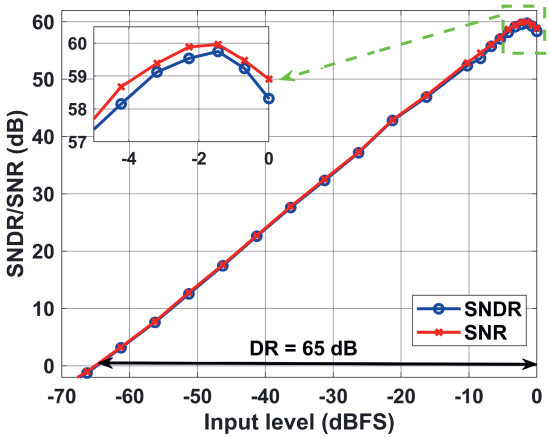
11.3.3 Single-tone test

The ADC has been measured with 4 GHz and 6 GHz sampling rates. Figure 11.24 presents the measured SNDR/SNR versus the input level. At 4 GHz sampling rate the measured DR and peak SNDR of the 2-1-1 MASH SDM in 300 MHz bandwidth are 65 dB and 60 dB respectively. If the output of the 3rd stage is not used, the 2-1 MASH SDM has a peak SNDR of 55 dB. The 3rd stage increases the peak SNDR by 5 dB, demonstrating the need of the 3rd stage. At 6 GHz sampling rate the DR and peak SNDR of the 2-1-1 MASH SDM in 500 MHz bandwidth are 58 dB and 54 dB respectively.

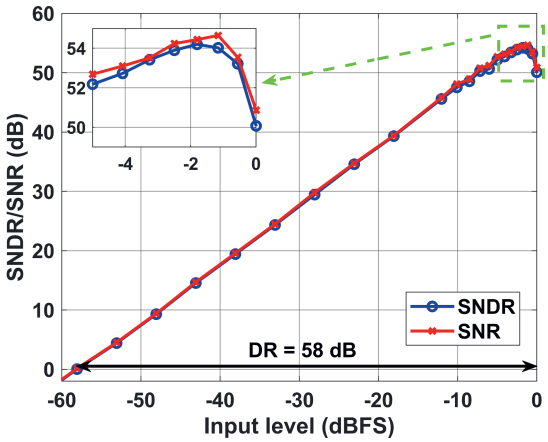
Figure 11.25 shows the output spectra with 4 GHz and 6 GHz sampling rates before and after the comparator offset calibration. Before the comparator offset calibration, the 2nd and 3rd loops are partially overloaded, since the comparator offset of the proceeding loops is amplified by the inter-stage gain and causes a large offset error on the 2nd and 3rd loop's input signals. The comparator offset calibration improves the SNDR by 17 dB, and it improves the SFDR by 18 dB in 300 MHz BW at 4 GHz sampling rate. When the MASH SDM is sampled at 6 GHz, the comparator offset calibration improves the SNDR by 24 dB, and it improves the SFDR by 22 dB in 500 MHz BW. From the out-of-band noise it can be observed that the modulator is very stable and no NTF peaking is observed, thanks to the current-mode ELD compensation. When F_S is increased from 4 GHz to 6 GHz, the in-band noise floor increases by 5 dB due to increased metastability errors.

11.3.4 Two-tone test

A two-tone test has been performed with 5 GHz sampling rate. Two input tones of A_{in} = -9 dBFS at f_{in1} = 255 MHz and f_{in2} = 305 MHz are applied. The choice of f_{in1} and f_{in2} is limited by the available filters for the measurement. The measured spectrum (2^{17}-point) is presented in Figure 11.26. For a signal BW of 375 MHz, the measured 2nd order inter-modulation-distortion (IMD_2) is -70.1 dBc, and the 3rd order inter-modulation-distortion (IMD_3) is -68.2 dBc.



(a)



(b)

Figure 11.24: SNDR/SNR vs. input level for (a) F_S = 4 GHz, BW = 300 MHz (f_{in} = 80 MHz); (b) F_S = 6 GHz, BW = 500 MHz (f_{in} = 140 MHz). 0 dBFS = 0.75 V_{peak}.

11.3.5 Measurement results compared to simulation results

This MASH ΣΔ ADC is designed to maximize the signal BW and sampling rate for the chosen 40 nm CMOS technology, for the peak SNDR and DR target given in Chapter 2.2. Post-layout simulation (TT corner, 65 °C, RC coupled post-layout extraction, no device mismatch, no transient noise) shows that a peak SNDR of 60.1 dB is achieved for signal BW of 500 MHz with F_S = 7 GHz. In the measurement,

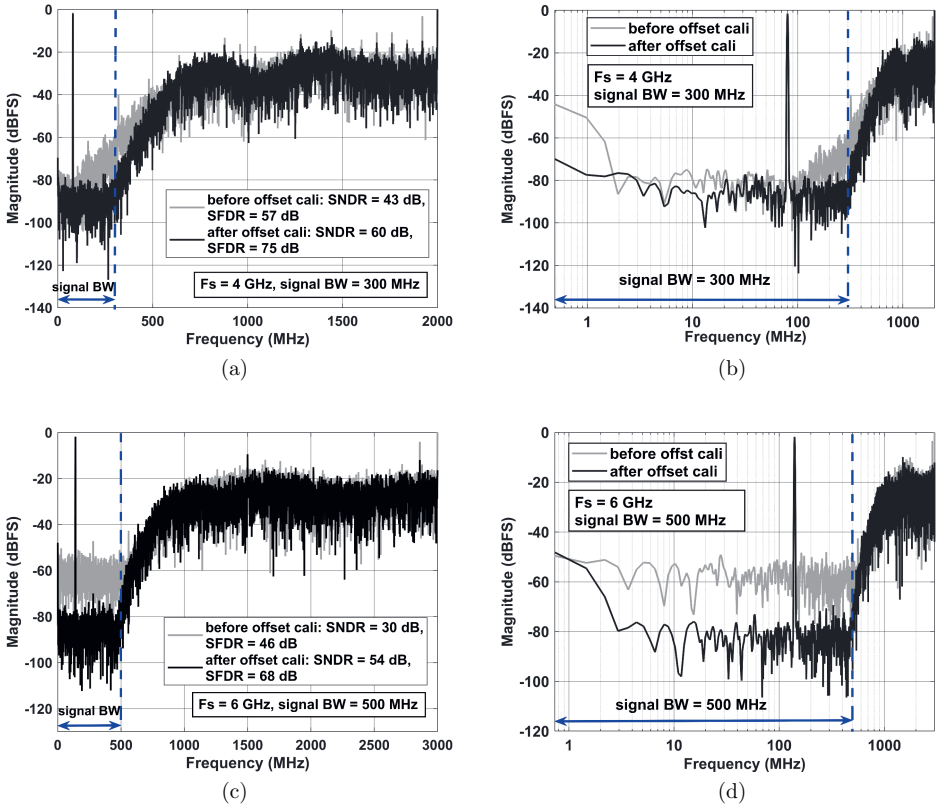


Figure 11.25: Measured spectra (16384-point) before and after the comparator offset calibration: (a) with an A_{in} = -1.5 dBFS and f_{in} = 80 MHz input and F_S = 4 GHz in a linear frequency axis; (b) with an A_{in} = -1.5 dBFS and f_{in} = 80 MHz input and F_S = 4 GHz in a logarithmic frequency axis; (c) with a A_{in} = -1.8 dBFS and f_{in} = 140 MHz input and F_S = 6 GHz in a linear frequency axis; (d) with a A_{in} = -1.8 dBFS and f_{in} = 140 MHz input and F_S = 6 GHz in a logarithmic frequency axis.

the peak SNDR and DR of the ADC with F_S = 6 GHz are degraded compared to the post-layout simulation results because of increased metastability errors. Without input signal, when the sampling rate is increased to 6.5 GHz, the noise shaping of the SDM is still visible, although the noise floor further increases. The ΣΔ modulator is not stable when the sampling rate is 7 GHz in the measurement (no noise shaping observed).

An overview on the comparison among the schematic simulation, post-layout simulation and measurement results is presented in Table 11.4. From schematic simulations, the achievable sampling rate is F_S = 8.4 GHz. A peak SNDR of 62.1 dB is expected

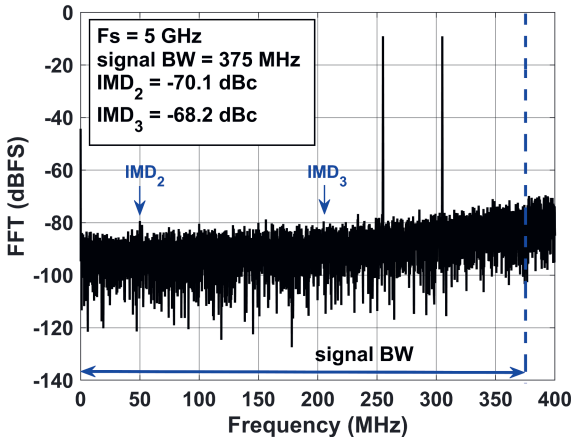


Figure 11.26: Measured spectra (2^{17}-point) with two input tones of A_{in} = -9 dBFS at f_{in1} = 255 MHz and f_{in2} = 305 MHz, F_S = 5 GHz.

Table 11.4: Comparison between measurement and simulation results

Items	Post-layout simulation	Measurement	
F_S (GHz)	7	6	4
signal BW (MHz)	500	500	300
peak SNDR (dB)	58.3[a]	54	60
DR (dB)	61.3[a]	58	65
power consumption (mW)	619	574	506
FoM_W (fJ/conv. step)	921	1402	1032
FoM_S (dB)	150	147	153

[a] Including quantization noise, thermal noise and DAC mismatch.

for a signal BW of 600 MHz, and the total power consumption of SDM and clock is 147 mW. From post-layout simulations, the maximal achievable sampling rate is F_S = 7 GHz. A peak SNDR of 58.3 dB is expected for a signal BW of 500 MHz, and the total power consumption of SDM and clock is 619 mW. In the measurement, the maximal applicable sampling rate is F_S = 6 GHz. At F_S = 6 GHz, the metastability error power is much higher than the post-layout simulations.

Compared to the post-layout simulation results, the measurement results have degra-

dation. The possible reasons are:

1. Device mismatch. Device mismatch can reduce the quantization gain of the quantizer and the data path from the quantizer to the main DACs, and increase the metastability errors. Figure 8.6 and Figure 11.6 show that the data path from the comparator core to the DAC cell contains one NMOS buffer with PMOS load, two CMOS buffers, and two pass-gates. There are two separated single-ended paths, which have a poor common-mode rejection (common-mode rejection is sacrificed to achieve high speed). Device mismatch changes the threshold voltages of those buffers, which can cause more metastability errors.

2. Supply and ground degradation. In the measurement, a large IR drop is observed from the supply and ground potentials measured at the LDOs on the validation board, to the supply and ground potentials measured on-chip through the analog test bus. The IR drop from the supply and ground together is up to 157 mV. From post-layout simulations, the maximal on-chip IR drop from the supply and ground together is up to 70 mV. No on-chip LDOs are used in this test chip. Simulations with the bonding wires modeled as inductance and resistance show an increased in-band noise floor, since the main DACs' output currents are modulated by the data-dependent supply and ground bouncing. The degradation of the supply and ground reduces the quantization gain in the loop as well, and increases the metastability errors.

3. The timing (especially the quantizer regeneration time) cannot be accurately tuned in the measurement. The design centering for the timing alignment is done according to post-layout simulation results for $F_S = 7$ GHz. In the measurement, only the relative delay between the DAC clock signals and the quantizer clock signals can be tuned. The quantizer regeneration time cannot be tuned separately, except for changing the ADC sampling rate. Thus, the timing alignment and the quantizer regeneration time can be not as optimal as in the post-layout simulations, e.g. due to PVT variations and device mismatch.

4. It is possible that the device models for simulations and post-layout extraction are not accurate enough for the target performance.

11.4 Benchmarking

The measured performance is summarized and compared to the state-of-the-art CT $\Sigma\Delta$ ADCs with signal BW $\geq$ 100 MHz in Figure 11.27. The state-of-the-art broadband CT $\Sigma\Delta$ ADCs can be divided into two categories. The works of [16, 88, 34, 30] maximize signal BW and peak SNDR (or DR) for given technologies. To maximize the signal BW and the sampling rate, they use flash sub-ADCs as the quantizers. Their Schreier FoMs are between 156 dB and 159 dB. The works of [63, 27, 52] optimize for the power efficiency of the ADC. For their technologies (16 nm and 28 nm

CMOS), their signal BW and peak SNDR (or DR) performances are not bounded by technology performance. Their Schreier FoMs are between 168 dB and 174 dB.

For the MASH ADC test chip at $F_S = 4$ GHz, the probability of the metastability error is very low, and its influence on the peak SNDR and DR is not dominant. The static current consumption is dominant in the overall current consumption. It is mainly due to the static current in the ELD-compensated quantizers, loop filter and main DACs. The major part of the static current consumption, which is in the ELD-compensated quantizers and the loop filter, is required to achieve the target sampling rate (7 GHz) in the chosen 40 nm CMOS technology. The static current consumption in the main DACs is needed to achieve low thermal noise. Since the static current does not scale with the sampling rate, the Schreier FoM of this ADC at $F_S = 4$ GHz (153 dB) is a few dB less than the other $\Sigma\Delta$ ADCs which maximize the signal BW and peak SNDR (or DR). The aim of this work is to maximize the signal BW and sampling rate in a given technology, which is achieved at the cost of the static current consumption in the building blocks. At $F_S = 6$ GHz, the Schreier FoM is degraded by the increased metastability errors.

This ADC achieves the broadest signal bandwidth of 500 MHz for CT $\Sigma\Delta$ ADCs, while being implemented in a very mature 40 nm CMOS node. This ADC achieves less peak SNDR, DR and power efficiency with a similar signal BW compared to the work of [16], which is implemented at a more advanced technology node. The reported signal bandwidth of single-loop $\Sigma\Delta$ ADCs is limited to about 160 MHz [63]. With MASH SDM architecture, the signal bandwidth is increased to 500 MHz by about 3×. This signal bandwidth extension is achieved at the cost of more design complexity, for example:

- A MASH SDM architecture requires an additional digital noise cancellation filter. Matching is required between the analog transfer functions and digital noise cancellation filter, otherwise noise leakage can degrade the resolution of the MASH $\Sigma\Delta$ ADCs [73]. Calibrations are typically required to achieve the matching requirements.
- MASH $\Sigma\Delta$ ADCs have more stringent requirements on the loop filter amplifier GBW, parasitic poles in the loop and coefficient accuracy. These non-idealities can cause signal leakage and noise leakage, which can overload the back-end stages and degrade the resolution of the MASH $\Sigma\Delta$ ADCs [110].

The measured performance is further compared to the state-of-the-art CT LP $\Sigma\Delta$ ADCs with $F_S \geq 1$ GHz in 40 - 45 nm CMOS in Figure 11.28 [88, 30, 111, 86, 112, 113, 31]. The signal BW (500 MHz) of this work is more than 3× higher than any other reported CT $\Sigma\Delta$ ADCs in 40 - 45 nm CMOS. This work demonstrates the highest sampling frequency of 6 GHz for a 3-bit $\Sigma\Delta$ modulator in 40 nm CMOS.

	This work		[16] JSSC 16 Dong et al.	[88] VLSIC 17 Dayanik et al.	[34] JSSC 12 Shibata et al.	[30] JSSC 11 Bolatkale et al.	[63] ISSCC 16 Wu et al.	[27] ISSCC 17 Huang et al.	[52] ISSCC 19 Wang et al.
Technology (nm)	**40**		28	40	65	45	16	16	28
Architecture	**2-1-1 MASH**		1-2 MASH	3rd order	6th order	3rd order	4th order	4th order	4th order
Quantizer resolution (bit)	**3**		4	3.7	4.1	4	5	7	7
Vdd (V)	**1.8 / 1.1**		1.8 / 1.0 / -1.0	1.95 / 1.1 / -0.55	2.5 / 1.0 / -2.5	1.8 / 1.1	1.5 / 1.4 / 0.8	1.5 / 1.35 / 1	1.5 / 1.1
Area (mm^2)	**1.56**		1.4	0.45	5.5	0.9	0.155	0.217	0.019
Fs (GHz)	**4**	**6**	8	5	4	4	2.88	2.15	2
OSR	**6.67**	**6**	8.6	16	13.3	16	9	8.6	10
Bandwidth (MHz)	**300**	**500**	465	156	150	125	160	125	100
Peak SNDR (dB)	**60**	**54**	67	66.5	n.a.	65	65.3	71.9	72.6
DR (dB)	**65**	**58**	72	70	73	70	72	74.8	76.3
Noise spectral density (dBc/Hz)	**-150**	**-145**	-159	-152	-155	-151	-154	-156	-156
THD (dBc)	**-73**	**-67**	n.a.	n.a.	n.a.	-74	-71	-80	n.a.
SFDR (dB)	**75**	**68**	80	83	n.a.	76	n.a.	n.a.	84
Power (mW)	**506**	**574**	890	233	750	256	40	54	16.3
FoM_S (dB)	**153**	**147**	159	158	156	157	168	168	174
Categories	Maximize signal BW and resolution						Optimize power efficiency		

$FoM_S = DR+10*\log10(BW/P)$

Figure 11.27: Comparison table with state-of-the-art CT ΣΔ ADCs with signal BW ≥ 100 MHz.

	This work		[88] VLSIC 17 Dayanik et al.	[30] JSSC 11 Bolatkale et al.	[111] JSSC 17 Briseno-Vidrios et al.	[86] ISSCC 12 Srinivasan et al.	[112] JSSC 17 Edward et al.	[113] JSSC 15 Xing et al.	[31] JSSC 16 Loeda et al.
Technology (nm)	**40**		40	45	40	45	40	40	40
Architecture	**2-1-1 MASH**		3rd order	3rd order	3rd order	3rd order	2-2 MASH	1-1 MASH	4th order
Quantizer resolution (bit)	**3**		3.7	4	4	1	4	5	1
Vdd (V)	**1.8 / 1.1**		1.95 / 1.1 / -0.55	1.8 / 1.1	1.1	1.8 / 1.4	2.5 / 1.15 / 1.1	0.9	n.a.
Area (mm^2)	**1.56**		0.45	0.9	0.072	0.49	0.265	0.017	0.0194
Fs (GHz)	**4**	**6**	5	4	3.2	6	1	1.6	2.4
OSR	**6.67**	**6**	16	16	21.3	50	9.9	20	30
Bandwidth (MHz)	**300**	**500**	156	125	75	60	50.3	40	40
Peak SNDR (dB)	**60**	**54**	66.5	65	65.5	60.6	74.4	59.5	66.9
DR (dB)	**65**	**58**	70	70	n.a.	n.a.	76.8	n.a.	67.8
Noise spectral density (dBc/Hz)	**-150**	**-145**	-152	-151	n.a.	n.a.	-154	n.a.	-144
THD (dBc)	**-73**	**-67**	n.a.	-74	n.a.	n.a.	n.a.	n.a.	n.a.
SFDR (dB)	**75**	**68**	83	76	n.a.	75	84	67.6	n.a.
Power (mW)	**506**	**574**	233	256	22.8	20	43	2.57	5.25
FoM_S (dB)	**153**	**147**	158	157	163	n.a.	167.5	n.a.	167

FoM_S = DR+10*log10(BW/P)

Figure 11.28: Comparison table with state-of-the-art CT LP $\Sigma\Delta$ ADCs with $F_S \geq 1$ GHz in 40 - 45 nm CMOS.

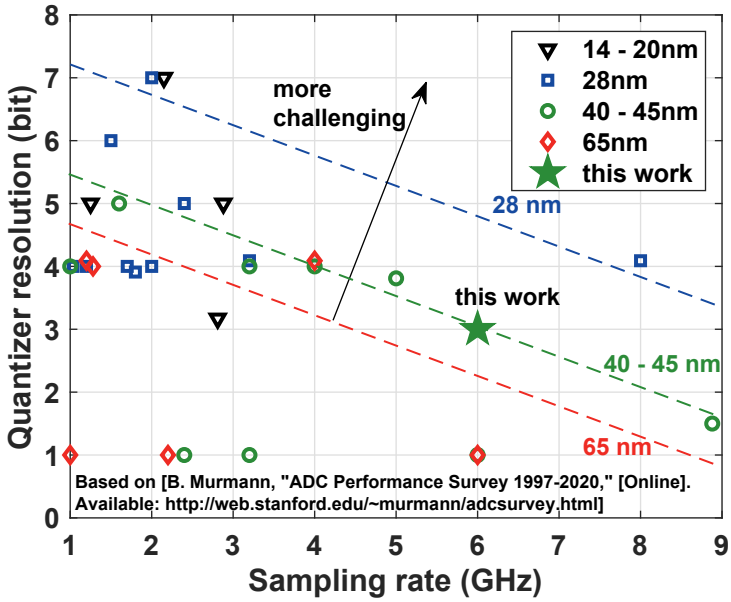


Figure 11.29: Benchmarking plot of quantizer resolution (bit) vs. sampling rate (F_S) for state-of-the-art CT ΣΔ ADCs with $F_S \geq 1$ GHz, fabricated in 14 – 65 nm CMOS.

Figure 11.29 shows a benchmarking plot of the quantizer resolution vs. sampling rate for state-of-the-art CT ΣΔ ADCs with $F_S \geq 1$ GHz, fabricated in 14 – 65 nm CMOS. The blue/green/red dashed lines show the state-of-the-art envelopes for published 28 nm / 40 - 45 nm / 65 nm ADCs (3 best designs are considered for the envelopes). From these lines it can be extracted that for the same number of bits, 28 nm CMOS achieves ∼1.6 – 2× higher sampling rate compared to 40 nm thanks to the technology advantage. Based on the technology benchmark it is expected that the bandwidth of ΣΔ ADCs can be extended further into the GHz range for more advanced technology nodes like 28 nm CMOS and beyond, employing the techniques of this work.

11.5 Conclusions

This chapter presents the circuit-level implementation and validation results of a 6-GHz-sampling 500-MHz-BW 2-1-1 MASH CT ΣΔ ADC in 40 nm CMOS technology. A multi-path Miller-compensated inverter-based amplifier is designed as the loop filter amplifier for its high GBW and power efficiency. The layout floorplan of the current source of the main DACs is not only common-centroid, but it also averages out the errors caused by the layout-dependent effects and the routing resistance. A buffer is added between the comparator core and the samplers to reduce the coupling

capacitance between the time-interleaved comparators.

Measurement results show that the calibration codes from the on-chip comparator offset calibration have a close-to-Gaussian-distributed spread caused by the quantizer thermal noise, and this error can be averaged out by performing multiple independent calibrations. At 4 GHz sampling rate the measured DR and peak SNDR in 300 MHz bandwidth are 65 dB and 60 dB respectively. At 6 GHz sampling rate the DR and peak SNDR in 500 MHz bandwidth are 58 dB and 54 dB respectively. The MASH ADC test chip is designed very close to the speed boundary of the chosen 40 nm CMOS technology. To maximize the sampling rate and signal bandwidth, the figure-of-merit is sacrificed since the power consumption increases exponentially with the sampling rate in the chosen 40 nm CMOS technology. In this design, the maximal sampling rate of the MASH SDM is limited by the main feedback loop, which means T_S is bounded by the regeneration time needed to generate the required quantization gain, plus the propagation delay (from quantizer to main DACs) and DAC delay to close the loop.

The target signal bandwidth of 500 MHz is indeed achievable in the chosen 40 nm CMOS technology; however, the power consumption increases exponentially with the sampling rate to achieve this signal bandwidth. If the power efficiency is also considered, 40 nm CMOS is not the best choice for this target specification if a more advanced technology node like 28 nm CMOS is also available. If the MASH ADC is ported from 40 nm CMOS into 28 nm CMOS, a broader signal BW and/or better power efficiency is expected for the following reasons: (1) 28 nm CMOS has faster transistors than 40 nm CMOS. In this design, the comparator core (M_9 - M_{12} and M_{17} - M_{20} in Figure 8.6) achieves a regeneration time constant of $\tau = 6.5$ ps and it consumes 6 mA in post-layout simulations. In a state-of-the-art broadband CT ΣΔ ADC designed in 28 nm CMOS technology, a comparator core achieves a regeneration time constant of $\tau = 5.5$ ps and it consumes 4 mA [16]. (2) Since 28 nm CMOS technology has better matching than 40 nm CMOS technology, the area of the matching-critical blocks can be reduced, which reduces the length of the interconnections. (3) Since the minimum length in 28 nm CMOS is smaller, the devices are shrunk compared to 40 nm CMOS. Thus, the length of the interconnection is shorter in 28 nm CMOS, which reduces the parasitics of the interconnection. Notice that for the same length, the parasitics of the interconnection in 28 nm CMOS are not smaller than in 40 nm CMOS. For the same type of metal layers, the routing resistance per square in 28 nm CMOS is larger than in 40 nm CMOS, since the metal layers are thinner. The routing capacitance per unit area (e.g. per 100 nm × 100 nm) is also larger in 28 nm CMOS, since the distance (dielectric) between metal layers is smaller.

The MASH SDM test chip design and validation prove that MASH SDM architectures can achieve a broader signal bandwidth than single-loop SDM architectures, for the same peak SNDR (or DR) target in the same technology nodes, at the cost of more design complexity.

The effectiveness of current-mode multi-path ELD compensation, current-mode locally-time-interleaved quantizer, and comparator offset calibration are proven with measurements. Thanks to the proposed techniques, the highest sampling rate of 6 GHz is demonstrated for a 3-bit SDM in 40 nm CMOS, which enables the broadest BW of 500 MHz for CT $\Sigma\Delta$ ADCs. Based on the technology benchmark it is expected that the bandwidth of $\Sigma\Delta$ ADCs can be extended further into the GHz range for more advanced technology nodes like 28 nm CMOS and beyond, employing the techniques of this work.

Chapter 12

Conclusions and recommendations

This chapter presents the conclusions of this thesis and recommendations for future work. First, Section 12.1 draws conclusions of this thesis. Afterwards, Section 12.2 provides recommendations for future work in broadband CT ΣΔ ADCs.

12.1 Conclusions

In a given technology, for a given DR target, MASH ΣΔ ADCs can achieve broader signal BW than single-loop ΣΔ ADCs, at the cost of more complexity. Single-loop ΣΔ ADCs have a simpler architecture than MASH ΣΔ ADCs. However, the out-of-band gain of the overall noise transfer function of a MASH ΣΔ ADC can be higher than the OBG of a single-loop ΣΔ ADC, for the same NTF order and quantizer resolution. Moreover, for MASH ΣΔ ADCs with multi-bit quantization, an inter-stage gain of higher than 1 can be applied to further improve the signal to quantization noise ratio. So MASH ΣΔ ADCs can achieve a certain BW and dynamic range target with lower OSR than single-loop ΣΔ ADCs for the same quantizer resolution.

The generic formulas proposed in this thesis to calculate the SQNR limits for both single-loop and MASH SDMs reduce the complexity of system level design and comparison significantly. The formulas can be used to calculate the SQNR limits for any single-loop or MASH SDM architectures with any NTF order, quantizer resolution, and OSR, and any NTF order for the sub-stages for MASH structures.

The proposed digital calibration of the errors due to the integrators' limited DC gain and 2nd pole for CT MASH ΣΔ ADCs can relax the DC gain requirements of the 1st – 3rd integrators by about 15 dB, and the 2nd pole requirement of the 1st integrator by 3×.

The proposed current-mode multi-path ELD compensation technique can solve the problem due to the parasitic delay caused by the poles of the summing amplifier

and the pre-amplifier for multi-GHz sampling multi-bit ΣΔ ADCs. The test chip measurement results prove its effectiveness.

The limitations caused by the parasitic capacitance on the ELD summation node can be overcome by adding a cross-coupled feedforward capacitor C_{ff} in parallel with the ELD DAC, and by creating a zero in the transfer function of the V/I converter (Gm cell). The test chip measurement results prove its effectiveness.

The proposed current-mode locally-time-interleaved multi-bit quantizer can move the reset time and the time to track the next initial condition of the comparator out of the 1 T_S ELD time budget, and enable 1.33× higher ADC sampling rate and signal BW. The test chip measurement results prove its effectiveness.

The proposed two-step coarse-fine comparator offset calibration can calibrate the offset of the locally-time-interleaved comparators and restore the ADC resolution. The test chip measurement results prove its effectiveness.

The proposed implementation of the DAC linearization techniques in broadband CT ΣΔ ADCs with the mapping engine in the digital domain can ensure that the non-idealities of the mapping engine do not interfere with the analog purity of the reference signal. It is a general-purpose architecture and it offers the flexibility to implement different static and dynamic DAC linearization techniques.

The metastability errors in broadband CT ΣΔ ADCs can be counteracted by the proposed two system-level solutions – the metastability error compensation technique, and the metastability shaping technique.

The 3-bit 2-1-1 MASH CT ΣΔ modulator test chip in 40 nm CMOS technology achieves 58 dB DR and 54 dB peak SNDR in 500 MHz bandwidth when sampled at 6 GHz and consumes 574 mW power. It achieves 65 dB DR and 60 dB peak SNDR in 300 MHz bandwidth when sampled at 4 GHz, while consuming 506 mW power. Thanks to the proposed techniques, the highest sampling rate of 6 GHz is demonstrated for a 3-bit SDM in 40 nm CMOS, which enables the broadest BW of 500 MHz for CT ΣΔ ADCs.

To achieve the target of 500 MHz BW, the MASH ADC test chip is designed very close to the speed boundary of the chosen 40 nm CMOS technology. The maximal achievable sampling rate and the signal bandwidth are limited by the total time needed by the main feedback loop, including the regeneration time to generate the required quantization gain, and the propagation delay and DAC delay to close the main feedback loop and to maintain the stability of the SDM. The main limitations for the performance (resolution, signal BW, power efficiency) of the test chip are metastability errors and layout parasitics (especially interconnections).

The main conclusions of the thesis are:

- In a given technology, for a given DR target and a maximum power boundary, the achievable signal bandwidth can be maximized by applying multi-stage

noise-shaping (MASH), multi-bit quantization, and by maximizing the sampling frequency.

- This thesis demonstrates the broadest signal BW of 500 MHz for CT ΣΔ ADCs, and the highest sampling rate of 6 GHz for 3-bit ΣΔ ADCs in 40 nm CMOS.

Based on the technology benchmark it is expected that the bandwidth of ΣΔ ADCs can be extended further toward the GHz range for more advanced technology nodes like 28 nm CMOS and beyond, employing the techniques of this thesis.

12.2 Recommendations for future work

From the design and validation of the MASH ADC test chip, some circuit-implementation limitations in the test chip were discovered. They are not fundamental limitations of the CT MASH ΣΔ ADC or the technology, and give rise to recommendations for future research. The limitations are first listed here and then followed by the recommendations:

- The approach of using multiple paths to extract the quantization noise of the preceding stages leads to challenges in the circuit implementation.
- The mismatch of the quantizer current sources is not calibrated, which leads to large area.
- No on-chip LDOs are used for the MASH ADC test chip, which might cause performance degradation.
- Too high signal leakage is observed in the measurement, which limits the peak SNDR and DR of the MASH ΣΔ ADC by a few dB.
- Not enough tunability is designed for the clock signals, and the regeneration time of the comparator core cannot be optimized in the measurement.
- Current-steering DACs with one-side switching are used as the main feedback DACs, which give noise penalty compared to resistive DACs.

Investigation on alternative approaches which can simplify the extraction of the quantization noise of the preceding stages is recommended for future research of broadband MASH ΣΔ ADCs. For the 2-1-1 MASH ΣΔ ADC architecture synthesized in this thesis, multiple paths ($k_1 \sim k_{10}$ in Figure 5.6) are used to extract the quantization noise of the preceding SDM stage as the input of a next SDM stage. This approach has two limitations in the circuit implementation (especially in the layout design phase): (1) matching is required among multiple paths for an accurate extraction of the quantization noise. Due to coefficients mismatch, limited GBW of loop filter amplifiers,

parasitic poles in the loops, etc., the transfer functions of those paths deviate from the ideal transfer functions. One consequence is that it results in undesired signal and quantization noise leakage, which occupies signal swing in the back-end SDM stages. This effect causes the back-end stages to reach overload with a smaller maximal input signal power than the ideal MASH SDM, which reduces the peak SNDR and DR of the MASH ΣΔ ADC. The 2nd consequence is that the real transfer function of the analog loop filter does not match the digital noise cancellation filter, which causes noise leakage in the MASH output and requires calibration of the NCF coefficients. (2) The additional ELD DACs (DAC 11 and DAC 12 in Figure 11.1) add extra load to the quantizer and add complexity in the layout floorplanning.

Investigation on alternative comparator offset calibration techniques is recommended to reduce the total area of the SDM. The comparator offset calibration technique proposed in Chapter 8.2 does not calibrate the amplitude error of the current sources of the reference DAC, ELD DAC and calibration DAC. Since the accuracy of the current sources for the quantizers relies on intrinsic matching, the quantizer current sources occupy a relatively large area (see Figure 11.14). System-level simulations show that the reference DAC's current sources have a more stringent matching requirement than the ELD DAC's and calibration DAC's current sources. For future research in comparator offset calibration, it is recommended to include the calibration of the relevant current sources. Thus, the total SDM area can be reduced.

On-chip LDOs are recommended to generate all sensitive supplies. Better ground strategy is recommended as well. For this MASH ΣΔ ADC test chip, no on-chip LDOs are used, and all the supplies are provided from outside the chip (generated on PCB). Moreover, many supply and ground domains are separated on chip. This supply and ground strategy has two limitations: (1) it is sensitive to bonding wire inductance, which can cause supply and ground bouncing. (2) it leads to electrostatic discharge (ESD) risk. Cross-domain protection circuits are not used on this test chip since they add delay in the high-speed loops. For future work in the design of broadband ΣΔ ADCs (especially for products), this thesis gives the following suggestions:

- All of the performance sensitive supplies should be generated on chip with LDOs, including all of the 1.1 V and 1.8 V supplies for the loop filter, main DACs, quantizers, clock circuitry. Proper decoupling capacitors should be added on-chip to regulate the supplies. Thus, the performance of the ADC is less sensitive to bonding wire inductance.
- Do not split ground domains unless it is necessary. Loop filter and main DACs are recommended to share the same analog ground on chip.

For future work in the design of broadband MASH ΣΔ ADCs, it is suggested to add tunability for the signal component in the back-end stages. In this MASH ΣΔ ADC test chip, too high signal leakage is observed in the measurement (the signal power in the 2nd and 3rd stage is close to the signal power in the 1st stage), which limits the peak SNDR and DR (by roughly $2 \sim 3$ dB).

For future work in design of broadband ΣΔ ADCs, it is suggested to add extra tunability on the clock signals. E.g., if the regeneration time of the comparator core can be independently tuned, an optimal quantization gain can be achieved in the measurement [16]. However, this additional tuning (in this paragraph and the previous paragraph) adds extra costs, e.g. design complexity, power consumption, calibration/trimming time (which add cost to the products).

For future work, it is suggested to consider using a resistive DAC as the main DAC, for its low noise and high linearity. The supply (or reference voltage) for the resistive DAC should be generated on chip with a low-noise high-performance LDO [9].

This thesis has a suggestion on simulations/verifications for future work in design of broadband (MASH) ΣΔ ADCs. Monte-Carlo simulations with device mismatch should be performed with the post-layout extracted model of the ΣΔ modulator. PVT corner simulations and a combination of PVT corners and device mismatch should also be performed with the post-layout extracted model for product design. Thus, if the metastability error increases when device mismatch is enabled, or when PVT corner is considered, it will be captured in these simulations.

Moreover, for several novel concepts proposed in this thesis, either they are not implemented on the test chip, or the measurement results cannot prove their effectiveness. Further research is recommended on those techniques as well.

For the new implementation of the DAC linearization techniques proposed in Chapter 9, the registers (mapping engine) shown in Figure 9.6 are implemented on the MASH ADC test chip. In the measurement (both single-tone test and two-tone test), different permutations on the reference codes were tried. However, no distinguishable difference on the harmonic distortion (in single-tone test) or inter-modulation distortion (in two-tone test) were measured. Future research on the proposed implementation of the DAC linearization techniques is recommended, to show the effectiveness of this approach with measurement results.

In the measurement of the MASH ΣΔ ADC test chip, the peak SNDR and DR of the MASH ADC at 6 GHz sampling rate is mainly limited by the increased metastability error. It is a pity that the proposed system-level solutions to combat the metastability errors – the metastability error compensation technique (Chapter 10.4), and the metastability shaping technique (Chapter 10.5) – were not implemented on the test chip. During this thesis, we have supervised two master student's projects to investigate the circuit implementation of the proposed metastability error compensation technique [101, 100]. The implementation of the analog delay and summation, and the matching requirement among DAC 1, DAC 3 and DAC 4 (in Figure 10.6) have been studied at transistor-level. Schematic simulations show that the MEC circuit is feasible to be implemented in modern CMOS technologies. Unfortunately, for this PhD work, no time was left to further investigate the circuit implementation of the metastability shaping technique. The comparator offset of quantizer 2 (in Figure 10.13) might be a concern due to its impact on the stability of the SDM, which

requests further investigation. For future research, it is definitely recommended to investigate the circuit implementation of these two techniques to combat the metastability errors, and to show the effectiveness of these two techniques with measurement results.

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1. **C. Zhang**, L.J. Breems, G.I. Radulov, M. Bolatkale, J.A. Hegt and A.H.M. van Roermund, "A digital calibration technique for wide-band CT MASH ΣΔ ADCs with relaxed filter requirements," in *IEEE International Symposium on Circuits and Systems*, Montreal, Canada, May 22 – 25, 2016, pp. 1486 – 1489.

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11. **C. Zhang**, L.J. Breems and S. Bajoria, "Techniques for linearizing digital-to-analog converters in Sigma-Delta analog-to-digital converters" *US patent* filed.

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Summary
Broadband Continuous-Time MASH Sigma-Delta ADCs

This PhD dissertation describes a study to the design of broadband continuous-time MASH $\Sigma\Delta$ ADCs. Architecture choices and implementation challenges are addressed, and based on that a test chip is designed for a CT 2-1-1 MASH $\Sigma\Delta$ modulator with 3-bit quantization. Several new concepts are proposed in this dissertation, including a digital calibration of the mismatch between the analog loop filter and the digital noise cancellation filter; a current-mode multi-path ELD compensation; a current-mode locally-time-interleaved quantizer; a comparator offset calibration; a metastability error compensation technique; and a metastability shaping technique. Several of these new concepts have been validated with a 6 GS/s 0.5 GHz bandwidth continuous-time 2-1-1 MASH 3b $\Sigma\Delta$ modulator test chip in 40 nm CMOS. The MASH ADC test chip achieves 65 dB DR in 300 MHz BW when sampled at 4 GHz, and 58 dB DR in 500 MHz BW when sampled at 6 GHz.

Samenvatting

Deze thesis beschrijft een onderzoek naar het ontwerpen van breedbandige tijdcontinue MASH ΣΔ ADC's. Architectuurkeuzes en implementatieuitdagingen worden behandeld en uitgaande daarvan wordt een testchip ontworpen voor een tijdcontinue 2-1-1 MASH ΣΔ-modulator. Diverse nieuwe concepten worden in deze dissertatie voorgesteld, waaronder digitale calibratie van de afwijkingen tussen het analoge lusfilter en het digitale ruisonderdrukkingsfilter; een stroom-gebaseerde meerpads ELD-compensatie; een kwantisator die op stroomsturing en lokale tijd-multiplexing is gebaseerd; een offset-calibratie voor de comparator; een techniek om metastabiliteitsfouten te compenseren; en een methode om metastabiliteitsfouten buiten de signaalband te schuiven. Een aantal van die concepten zijn gevalideerd met een 6 GS/s 0.5 GHz bandbreedte tijdcontinue 2-1-1 MASH 3b ΣΔ-modulator-testchip in 40 nm CMOS. De MASH ADC testchip realiseert 65 dB DR in 300 MHz bandbreedte wanneer hij met 4GHz geklokt wordt, en 58 dB DR in 500 MHz BW wanneer hij met 6GHz geklokt wordt.

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Biography

Chenming Zhang was born in Yongqing, Hebei Province, China in 1988. From 2006 to 2007, he studied at Tongji University, Shanghai, China. He received the Bachelor of Science degree (cum laude) in Electronic Engineering from Politecnico di Torino, Turin, Italy, in 2010, and the Master of Science degree in Electrical Engineering and Information Technology from ETH Zürich, Zürich, Switzerland, in 2013. Since 2013, he started to pursue his PhD's degree in the integrated circuits group (named mixed-signal microelectronics group at that time) at Eindhoven University of Technology, Eindhoven, The Netherlands. His PhD project is on broadband continuous-time MASH Sigma-Delta ADCs.

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