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Versatile butt-joint regrowth for dense photonic integration

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Abstract: Butt-joint regrowth is widely used in photonic integration, but it has been challenging to break the density-quality tradeoff due to the edge growth rate enhancement (GRE) effect. In this work, we propose a scheme to circumvent this tradeoff by using large regrowth masks whose centers are exposed to epi-growth for neutralization of the excessive species. With the GRE under control, epi-stacks with arbitrarily large sizes supporting dense arrays can be butt-joint integrated with minimal compromise to their epitaxy quality. In our experiment, multi-quantum-well-based material of an exceptionally large area of 0.5×1.7 mm^2 was epitaxially integrated with passive InP material on the same wafer. A more than $20\times$ reduction in edge topology compared to conventional methods was achieved.

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1. Introduction

Integration density is key to photonic integrated chips [1]. Not only does the high density lowers the cost per component, but it also powers more advanced functionalities to be realized in a single chip, examples of which include optical phased arrays [2,3], multi-channel optical transceivers [4], high throughput optical switches [5,6], and photonic artificial neural networks [7]. To realize such sophisticated PICs, multiple photonic components each providing unique functions are needed, including light generation and amplification, modulation, detection, filtering, and waveguiding. Since these components are usually based on materials with different layer structures and doping [8], how to integrate them on the same wafer is of central importance. For III-V based materials, this can be realized by quantum well intermixing (QWI) [9], polarization-based integration scheme (POLIS) [10], vertical twin guide [11], butt-joint regrowth (BJR) [12], etc. The BJR approach has been popular among industry [8] for its highest flexibility, in which components can be individually optimized on their native material platforms without compromising each other.

In the BJR process, high component density can be achieved either by densely spaced masks or big masks within which compact arrays of components can be fabricated. However, at high-density and large-scale, both approaches face the challenges of undesired high topology around the mask edge [13] and polycrystalline growth on the mask. In the epitaxy process, due to the masks being present, species on top of the masked region will be blocked and therefore contribute to higher concentrations in the surrounding areas through vapor phase diffusion (VPD) and surface diffusion [14]. The concentration variation will enhance the growth rates near the mask edge, and, in extreme cases, across the whole wafer. This is referred to as the growth rate enhancement (GRE) effect, and it will result in a high-topology surface [15,16], jeopardizing subsequent processes. It could also deteriorate the optical performance of the components if the high topology coincides with the light path. Furthermore, polycrystalline growth will take

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place on the mask surface [17] if the accumulated species concentration on top of the masks goes beyond a certain threshold, rendering the entire process unreliable. Generally, the denser/larger the masks are, the more pronounced these problems are.

Conventionally, to avoid these problems, masks used in the BJR process need to be sufficiently small in at least one dimension (e.g., a few microns in width) and far apart from each other (a spacing of a hundred microns and more), which significantly limits the integration density. The overall masked area is also limited to avoid global GRE across the whole wafer. Efforts have been made to overcome this challenge by using low chamber pressure [13,16] or in-situ etching [18], but it has not been possible to decouple the high GRE topology and polycrystalline growth problems completely from the process with arbitrary mask sizes. Besides, they normally require re-development of the fabrication process outside the commonly used process window, which is a large effort with a risk for lower process quality.

In this work, we propose to use novel masks with an opening in the center to tackle this density hurdle. Our method offers high versatility in that, the edge growth profile is independent of the masks' sizes, distributions on the wafer, and placing densities, in a reasonably large range. The general idea and process flow are first presented in the method section, followed by theoretical analysis and experiments on an InP membrane platform. Comparative experiments have also been conducted on exceptionally large masks reaching areas of 0.5×1.7 mm^2 ($\sim 50\times$ larger than conventional masks), showing more than $20\times$ reduction in the edge topology with our method.

2. Method

In our approach, the area of the masked region can be arbitrarily large, such that a dense array of components can be directly realized within one region instead of a sparse array of small isolated regions. Here, the commonly used BJR application, active-passive integration, is used as an example to illustrate our idea, but our method can also be used for the integration of other materials. The proposed process flow is shown in Fig. 1, where the "active" and "passive" concepts can contain complex structures. It may also contain etchstops that will eventually be removed. For example, if applying this method to the layer structure in [12], the active material will contain the multi-quantum wells (MQW), the separate confinement heterostructure (SCH) layers, and the lower part of the InP top cladding, while the passive material will be Q1.25 and the regrown lower part of the InP top cladding. A conventional BJR process flow can also be found in [12] as a comparison.

The detailed process flow is as follows: Step 1: The dielectric mask defining the region for active material is prepared by deposition, conventional lithography, and etching, as seen in Fig. 1(a). Step 2: The unmasked regions are removed by selective etch. This step should be well-calibrated to create an undercut profile as shown in Fig. 1(b) for compensation of the GRE-induced "rabbit ears" found near the mask edges during regrowth [19]. Step 3: The center part of the mask is opened up by lithography and selective etch, leaving only a narrow frame with the frame's stripe width of around ten microns, small enough for low GRE. Step 4: The regrowth of the passive material occurs both in the opening of the mask and in the previously etched regions. Step 5: The material grown in the opening of the mask is removed by lithography and selective etch. Here the lithographic alignment tolerance is very relaxed. The tolerance is determined by the stripe width of the frame mentioned in step 3, which is in the order of ten microns. Step 6: After mask removal and cleaning, large-scale monolithic integration of active and passive materials with a near-flat surface topology is obtained. Since in step 3 the center of the mask is opened, we refer to our method as the "open mask" method in the following paragraphs. As seen in Fig. 2, dense active-passive integration can be achieved by populating the obtained large active and passive regions by ridge-type semiconductor optical amplifiers (SOA) and waveguides, using just standard processes including top cladding growth, lithography, ridge etch, and metallization. In post-processing, there's no limit on the device pitch from the GRE

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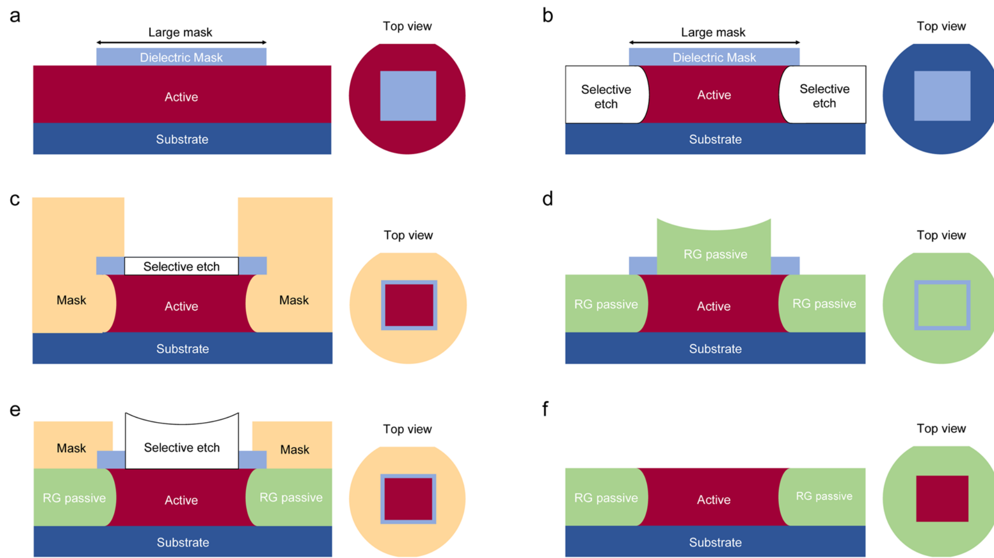

Fig. 1. Illustration of the BJR process for active-passive integration, with a center-opened mask. Note that the etch-stop layers are not shown for clarity. **a:** Prepare mask on the starting epi-wafer defining active and passive regions. **b:** Selectively etch the active material in the unmasked region for regrowth of the passive material. **c:** Etch open the center of the mask, leaving only a narrow frame along the edge. **d:** Regrow the passive material. **e:** Use an additional mask to protect the regrown material and selectively remove the unneeded material grown on top of the active material. **f:** Remove all masks, and a low-topology surface is obtained.

effect. By changing the material composition, our method can also be applied to ridge-type electro-absorption modulators or phase modulators.

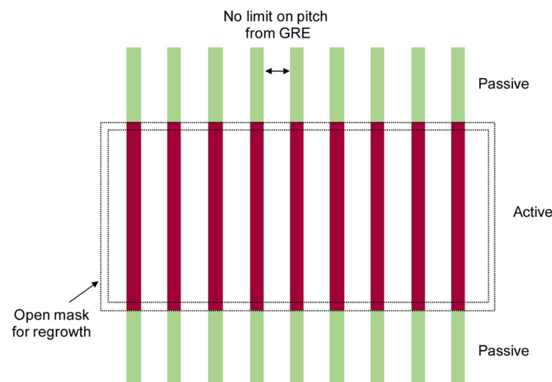

Fig. 2. Illustration of a dense integration scheme using the open mask and large areas of functional materials.

An alternative way for the first three steps is: In step 1, the open mask is defined directly by lithography; In step 2, photoresist is used to seal the opening in the mask; In step 3, the unprotected region is removed by selective etch. The alternative approach theoretically yields the same result as the original flow, but the choice of photoresist can be different based on the cleanroom inventory.

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3. Theory

The GRE effect and polycrystalline growth are mainly caused by lateral diffusion in the vapor phase [20] and high species concentrations above the mask [17], respectively. Therefore, we have used a VPD model [21] to verify our method. The Laplace equation for species concentration has been solved in 2D by finite-element method (FEM), with the boundary conditions indicated in Fig. 3(a). The virtual chamber dimensions W and H have been chosen to be 0.6 mm and 1 mm, respectively. A convergence test has been done to ensure that the virtual chamber is sufficiently large to exclude the influence from chamber walls. The diffusion length (D/k_s) has been set to 10 μm, a typical value of InP [21]. The GRE factor R has been calculated by the species concentration near the semiconductor surface with the presence of masks, divided by a reference value in a separate, maskless simulation.

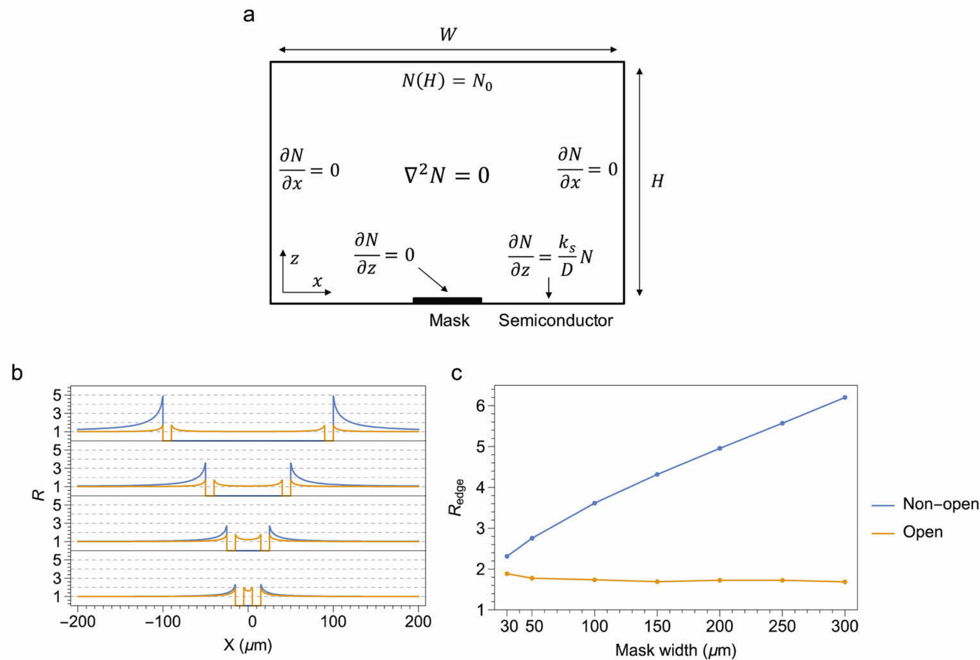

Fig. 3. The GRE factors obtained from 2D VPD modelling. **a:** Schematics showing the boundary conditions of the VPD model. **b:** Comparison between the GRE factor curves of the open and non-open masks at different dimensions. **c:** GRE factors at the outer edges of the masks (R_{edge}) of the open and non-open masks at different dimensions.

As seen in Fig. 3(b), by exploiting the opening in the mask, most of the species formerly contributing to the detrimental GRE effect and polycrystalline growth were now instead trapped in a controlled manner. The low R (< 2) at the edge of the open mask also implied low excessive species above the mask, and thus reduced chance of polycrystalline growth. A significant reduction in the GRE effect can be observed, with the open mask having increasingly more advantage over the non-open mask when it goes to larger dimensions, as seen in Fig. 3(c). By using the open mask, the GRE effect of the giant mask can be effectively converted to that of narrow stripes, whose GRE and "rabbit-ears" can be well compensated by a mature undercut process. Therefore, no re-development of the epitaxy process is needed, and our open mask approach can be seamlessly plugged into the existing foundry process, which makes it easy-to-use and low-cost.

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Furthermore, in our approach, since effectively only the "outline" of the mask is used to define different material regions, the GRE effect does not scale with the intended sizes of the regrowth region. Therefore, this method remains valid for regrowth area ratios ranging from 0% to nearly 100%. This decoupling of the GRE effect from the regrowth area size brings more versatility in that, the process flow only needs to be optimized once for a particular frame stripe width, and then it can be used for arbitrary sizes of regrowth regions. This feature makes our approach capable of dealing with a broad range of regrown component densities in a single epitaxy process, which is crucial for generic PIC foundries to offer high flexibility to designers.

Although our proposed flow has two extra lithographic steps (Fig. 1(c) and Fig. 1(e)) compared to the basic BJR process [12], these two steps are of high fabrication robustness and can be done by entry-level machines like contact lithography or stepper lithography. This is because the overlay error tolerance in these two steps is determined by the stripe width, which is usually in the order of ten microns. Accounting for this and due to the high potential gain in integration density, we expect the cost per component would drop dramatically even if there exist two extra lithographic steps.

4. Experiment

We have validated the open mask approach for active-passive integration, by inspecting the cross-sectional butt-joint profile after regrowth and comparing it with conventional BJR schemes [12] on the indium phosphide membrane on silicon (IMOS) platform [11], which highlights nanophotonic InP components and therefore a route to high-density. On the butt-joint IMOS platform, the active material is an InGaAsP-based double-heterostructure (MQW sandwiched by doped InP claddings), while the passive material is intrinsic InP. The device cross-sections of this platform are illustrated in Fig. 4 [11,22], where the regrown Q1.25 is to be removed after wafer flipping and bonding. In our experiment, masks with the same length of 0.5 mm and widths ranging from 0.1 mm to 1.7 mm have been included. If considering practical limitations like thermal dissipation, an array of more than 150 SOAs can be implemented with a pitch of 10 µm in the $0.5 \times 1.7\,mm^2$ region.

The process started with the epi-wafer with active materials, whose crystal orientation is depicted in Fig. 5(a). After the 200 nm-thick SiO_2 mask preparation by plasma-enhanced chemical vapor deposition (PECVD), lithography, and BHF wet etch (Fig. 1(a)), the regions unprotected by the masks were selectively wet-etched by HCl/H_3PO_4 and citric acid, creating a fine-tuned undercut profile (Fig. 1(b)). The undercut profile has been calibrated to create a low-topology surface after regrowth with narrow stripes. Then, the open mask pattern (Fig. 1(c)) was obtained by lithography and BHF wet etch. The frame stripe width of the open mask was chosen to be 10 µm, which was the same as in our conventional BJR process with narrow stripes. The shared stripe width configuration facilitates the high compatibility with our existing component library and process flow. The passive material, a 300 nm-thick intrinsic InP layer, following a 20 nm-thick Q1.25 etchstop, was then grown by metalorganic vapor-phase epitaxy (MOVPE) using the conventional BJR recipe after a CH_3OH/Br_2 surface cleaning procedure. After epitaxy, the wafer was taken out for inspection.

Figure 5(a) shows the region on the wafer with a mask area of $0.5 \times 1.7\,mm^2$. The butt-joint after regrowth in the inner side of the mask has been characterized by focused ion beam (FIB) milling and scanning electron microscope (SEM). As seen in Fig. 5, the regrown InP was clean and absent of polycrystals, thanks to the opening in the mask. Note that due to the GRE effect, the material grown on top of the active region was not flat and much thicker than the regrown thickness, 300 nm. However, this was not a problem since it will be later selectively removed.

A control experiment has also been done using the same wafer and mask dimension, but with no openings on the mask. As seen in Fig. 6(a), due to the giant $0.5 \times 1.7\,mm^2$ size of the mask used, considerable polycrystalline growth on the hard mask can be found forming little black

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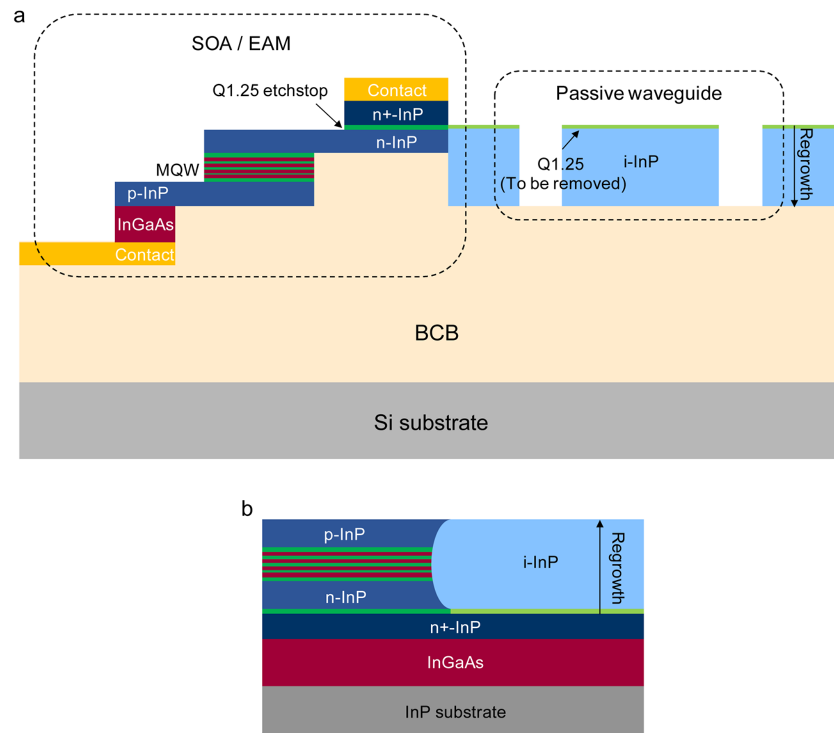

Fig. 4. Device cross-sections of the butt-joint IMOS platform. **a:** Cross-sections after bonding to silicon. The InP wafer is flipped, and with substrate removed. The original regrowth direction and layers done before bonding are drawn in the figure. **b:** Cross-sectional illustration along the butt-joint before bonding.

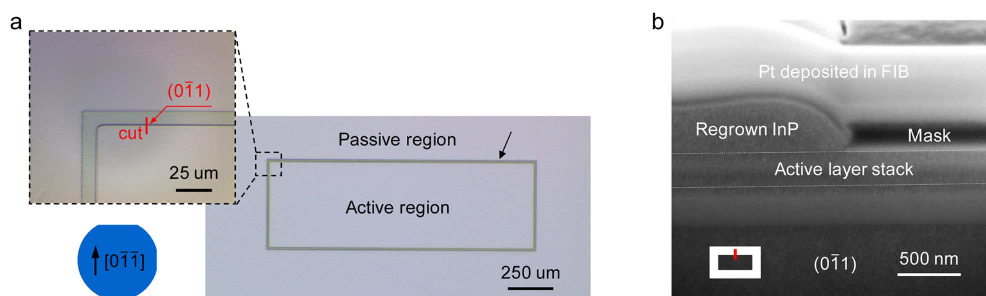

Fig. 5. Image of the wafer after BJR (step 4, Fig. 1(d)). **a:** Microscope image of the open mask with a stripe width of 10 µm and a dimension of 0.5 × 1.7 mm^2. The black arrow indicates the SiO_2 mask. The FIB cut position is labeled in the inset. **b:** SEM image of the facet created by FIB at the plane (0 $\bar{1}$ 1) of the inner side of the open mask. The plane for cross-section is indicated in red on the white rectangle. Notice that platinum for protection during FIB milling is still present. The regrown InP shown in the picture will be selectively removed in the next steps.

dots under the microscope. To quantify the height of polycrystalline material and the surface topology, a step profilometer has been used. As can be seen in Fig. 6(b), the polycrystalline material "spikes" reached heights of more than 1 μm, and over 800 nm edge overgrowth was present. This high topology renders it highly challenging for further processing. In contrast, an excellent and well-controlled surface topology has been obtained with the open mask. A less than 50 nm excess growth on the edge, which is more than 20 times reduction, can be observed in Fig. 6(b).

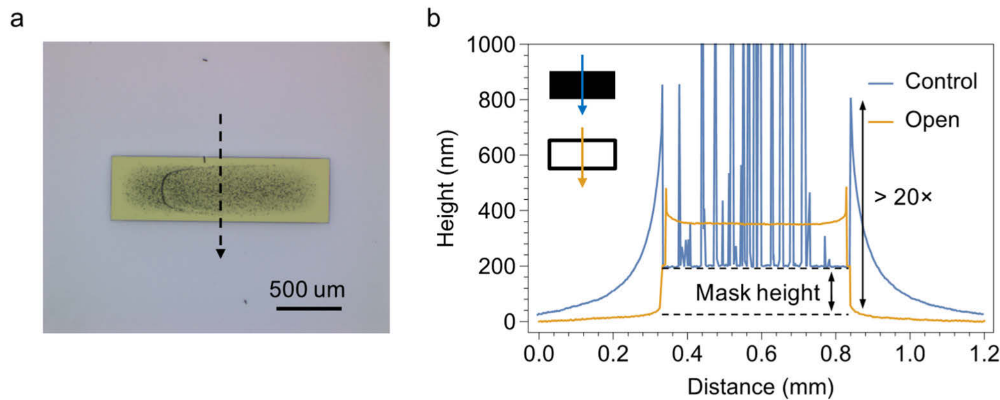

Fig. 6. Regrowth results of the open mask compared to non-open mask (control). **a:** Microscope image of the dielectric mask with a dimension of 0.5×1.7 mm^2 after regrowth. Black dots on top of the mask indicate severe polycrystal growth occurred in the process. The arrow with a dashed line indicates profilometer scanning direction in b. **b:** Surface topology of the open mask versus non-open mask (control) with the same dimension of 0.5 $\times$ 1.7 mm^2. Profilometer scanning directions are indicated by the blue and yellow arrows over the solid and open rectangles representing the mask shapes. For clarity, the height is truncated at 1000 nm.

Successful removal of the material grown in the mask opening is crucial for obtaining a near-planar surface in the end. We have first used HCl/H_3PO_4(1:4) to etch away InP and then $H_2SO_4/H_2O_2/H_2O$(1:1:10) to remove the quaternary etch-stop. SiO_2 hard mask was used in this process for protecting the passive material. FIB and SEM were utilized again to verify this process. As seen in Fig. 7(a), the regrown InP material has been successfully removed selectively (compared to Fig. 5(b)) leaving a flat and continuous surface in the active region. The active/passive interface shown in Fig. 7(b) was also nearly flat due to the carefully tuned undercut size compensating for the GRE effect. To further verify the quality of the butt-joint, we have cleaved the wafer and performed a stain etch using $K_3[Fe(CN)_6]/KOH/H_2O$(12:17:200). The stain etch process has distinct material-dependent etch rate, thus providing enhanced differentiation under SEM, as seen in Fig. 7(c). The small "spiking" near the butt-joint interface (between original n-InP and regrown i-InP) was the Q1.25 etchstop, which was grown on the sloped n-InP surface during the regrowth process. Since this Q1.25 was buried in InP and only had a thickness of 20 nm, the impact on light path was minimal. At this stage, successful butt-joint integration of mm-sized active material with passive material has been achieved. Now with the limit on integration density by the BJR process lifted, conventional process for PIC fabrication can be used to yield high-density photonic chips.

To demonstrate the versatility of our approach, we have also compared the surface profiles of open masks of different sizes. As seen in Fig. 8(a), the surface profile after regrowth of the two open masks were almost identical, even if their areas differ from each other by over 150%. By opening up the majority of the mask in the center, the GRE effect induced by the hard mask has

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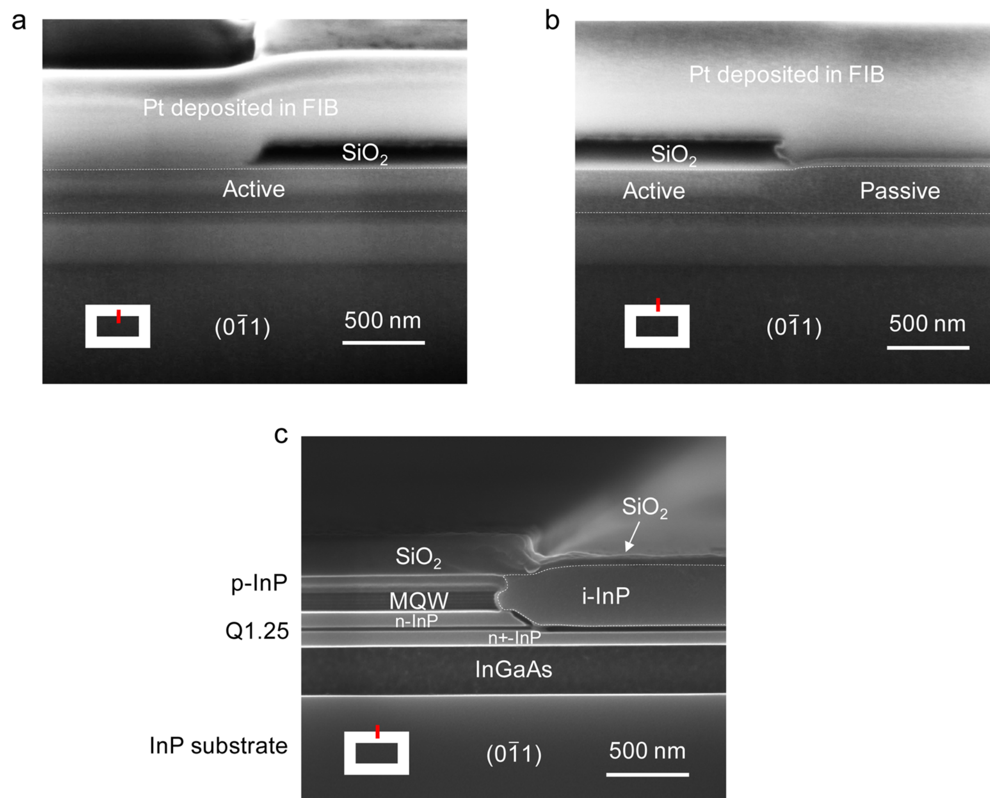

Fig. 7. Image of the wafer after removing the material grown in the mask opening (step 5). The crystal orientation is the same as in Fig. 5. The planes for cross-section are indicated in red on the white rectangles. Platinum for protection in the FIB process is present in both images. **a:** SEM image of the interface between the active layer stack and the inner edge of the open mask. **b:** SEM image of the interface between the outer edge of the open mask and the passive layer stack. Note that the thin SiO_2 hard mask is still present on top of the passive material. **c:** SEM image of the butt-joint after wafer cleaving and stain etch for enhanced resolution. InGaAs and quaternary materials appear as darker-colored trenches since they are etched faster. The white edgings are due to edge effects in the SEM when imaging well-defined trenches.

been reduced to a minimal level, which was effectively the same as that of separate striped mask islands. To validate this point, a standalone striped mask with a length of 0.5 mm and a width of 10 μm, the same as the frame stripe width of the open mask, has also been included in the same epitaxy batch on the same wafer. The surface profiles right after regrowth of this striped mask and the open mask are shown in Fig. 8(b). Note that the standalone mask had undercut profiles beneath the mask on both sides, while the open mask only had undercut on the outer side of the profile. As seen in Fig. 8(b), on the undercut side, the surface profiles of the standalone stripe and open mask overlapped well with each other, indicating the equivalence in terms of the GRE effects of these two types of masks.

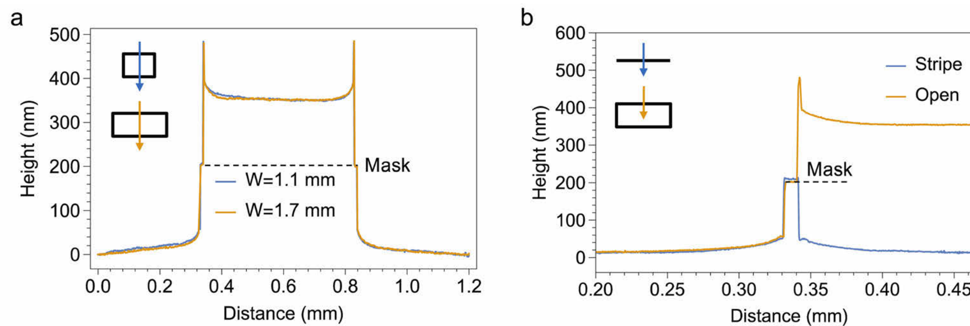

Fig. 8. Surface profiles right after regrowth for open masks with different sizes and a standalone striped mask. Profilometer scanning directions are indicated by the blue and yellow arrows over the solid and open rectangles representing the mask shapes. **a:** Surface profiles of the open masks of sizes of 0.5×1.1 mm^2 (blue) and 0.5×1.7 mm^2 (yellow). **b:** Surface profiles of the open mask and single stripe. The stripe widths are both 10 μm.

The independence of the GRE effect from the mask size leads to the high versatility and compatibility of the open mask approach. It effectively decouples the GRE fabrication requirement from the chip layout workflow. Now the GRE strength is determined by the stripe width of the open mask instead of the actual active or passive region, and the stripe width can be fixed and well-calibrated once for all in fabrication. In this way, PIC design can leverage much-enhanced freedom in placing components with densities ranging from standalone to extremely high, without being constrained in design rules raising from the BJR process.

5. Conclusion

In this work, dielectric masks with openings in the center (open masks) have been used to relieve the GRE effect and polycrystalline growth during the butt-joint regrowth process. Our approach highlights three major advantages: no need to re-develop the epitaxy-recipe, high versatility in BJR size choices, and relaxed process tolerance. By using this method, BJR of large area sizes reaching 0.5×1.7 mm^2 has been achieved with edge GRE reduced by more than 20 times. This work can be of high value to the PIC industry, as it can be readily adapted for different layer-stacks to significantly boost the integration density. This will open up new design opportunities and for emerging advanced applications such as optical phased array and optical switches.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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