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PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof. dr. ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op vrijdag 18 juni 2021 om 16:00 uur

door

Roy Leonardus Maria Op het Veld

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To my grandfather, Theo

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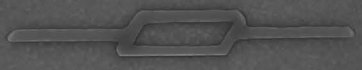
List of abbreviations

A-B	Aharonov-Bohm
Al	Aluminium
BHF	Buffered hydrofluoric acid
CCD	Charge-coupled device
DOS	Density of states
EBL	Electron beam lithography
EHT	Electron high tension
FFT	Fast-Fourier transform
FIB	Focused ion beam
IPA	Isopropanol
InAs	Indium arsenide
InP	Indium phosphide
InSANe	In-plane Selective Area Networks
InSb	Indium antimonide
LN_2	Liquid nitrogen
MBE	Molecular beam epitaxy
MIBK	Methyl isobutyl ketone
MOCVD	Metalorganic chemical vapor deposition
MOVPE	Metalorganic vapor-phase epitaxy
N-NW-S	Normal-nanowire-superconductor
NW	Nanowire
PECVD	Plasma-enhanced chemical vapor deposition
Pb	Lead
Pt	Platinum
SAG	Selective area growth
SC	Superconductor
SEM	Scanning electron microscope
Sn	Tin
STEM	Scanning transmission electron microscopy
TEM	Transmission electron microscopy
TMIn	Tri-methyl-indium
TMSb	Tri-methyl-antimony
VLS	Vapor-liquid-solid

Chapter 1

Introduction



Human history has seen many big leaps forward in the evolution of technology, from the first use of agriculture about 11,000 years ago up to the latest evolution: computer technology.[1,2] There are many important discoveries that helped change the pace of technological advances, that can be categorized in two parts. First, the ability to communicate/ transmit information beyond simple face-to-face communication. This includes the invention of writing, printing, radio, television, and the internet, all accelerating and scaling up the distribution of knowledge around the world. Second, the invention of calculators, and later computers, gave us access to computational power specifically suitable for tasks that are more difficult for the human brain, allowing us to solve problems we could not easily solve before.

1.1. Computer versus human brain

A "normal" computer, or just a computer as we know it right now, is defined as follows:

> "an electronic device for storing and processing data, typically in binary form, according to instructions given to it in a variable program." *Oxford dictionary*

This includes PCs, laptops, tablets, phones, smartwatches, cell towers, satellites, etc. and is incorporated nowadays in almost everything around us, even a fridge has some computational power, though very minor, to regulate the temperature for example. The computer chips in these objects are all based on the very same material and principle: a silicon-based transistor in an electronic circuit (see Figure 1.1).

The transistor can in this case be used as an electronic switch, like how a light switch would work. If the gate is off (binary "zero"), no current is flowing (light switch is off). When the gate is charged, a current will start flowing between source and drain (binary "one") (flip the switch and the light turns on). This forms the physical basis for the "bit". By combining the computational power of many transistors in an array, a computer chip can be made, allowing for more complicated tasks. This scales in a linear fashion, meaning that doubling the number of transistors will lead to a doubling in computational power.

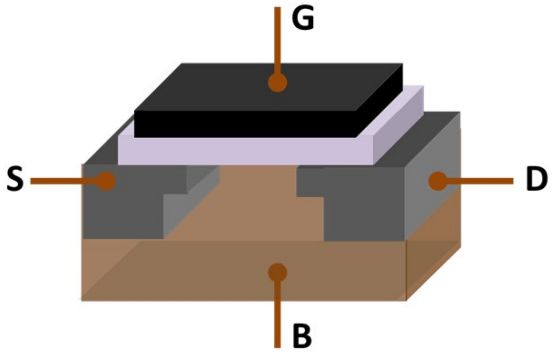


Figure 1.1 | Schematic overview of a single transistor.
A transistor with the Source (S) and Drain (D) in grey, the Body (B) in brown and the Gate (G) in black, separated from the source and drain by an insulating layer (pink). Image from Wikipedia.org.

In 1975, Gordon Moore predicted such doubling of the number of transistors in a chip every two years, known as Moore's law.[3] This has been the main target for the semiconductor industry since then. By making the single transistor smaller and smaller, less material and less power is consumed, allowing for an increased number of transistors for the same area. In recent years, however, this has become increasingly difficult as the physical limitations of going smaller are being reached. The vertical dimension in state-of-the-art transistors are nowadays as small as 5 nm,[4] which roughly equates to a chain of only 10 silicon atoms, leading to multiple problems.

Although the computational power of computers nowadays was unimaginable 100 years ago, there are some limitations to its abilities. When compared to a human brain, a computer is very good at performing numerical calculations and linear operations (summation, multiplication, array operations, etc.). Its limitations compared to for example the capabilities of the human brain (for example in recognizing complicated images) lie in the intrinsic nature of its core components. A computer chip is specifically designed to perform a certain type of calculation as efficient and as fast as possible, like creating images (graphical processing unit). Therefore, the design of every transistor, a chip's base component, is extremely rigid, allowing it to be extremely small and energy efficient, while at the same time be produced in large volumes. On the other hand, major advances have been made on the software side by developing for example new machine learning

algorithms. The latest supercomputers seem to be able to perform tasks that before seemed too difficult for computers. An interesting example here is facial recognition, a technique used by big companies like Facebook and Google,[5,6] but also by law enforcement and national intelligence agencies.[7] There is however significant evidence that this technology is severely flawed.[8] The important thing to note here, is that this kind of technology was mainly enabled because of their increase in computational power, brute forcing a silicon-based machine to do something a carbon-based brain is far better at, with significantly less energy requirements. Complex challenges, for example climate or weather models, or calculating the molecular structure of large molecules, would require parallel computing, since in these examples many different parameters are dependent on each other. This is impossible to do in an efficient way with classical computer architecture.

The human brain, however, works on a very different principle. It is optimized to grow and change over time, learn, forget, and adapt; strong requirements to ensure a person's survival in an ever-changing environment. This is achieved by making the core components, neurons, axons, and dendrites, very adaptive. The neuron (or transistor of the brain) connects to other neurons by dendrites, or interconnects.[9] By strengthening the dendrites that are used often and allowing unused dendrites to decay, the brain learns new things and improves its efficiency in performing certain tasks. This method of optimization in combination with the ability to create new interconnects enables the human brain to perform incredibly complex tasks that are otherwise difficult or nearly impossible to perform with a computer, with an energy consumption of around 20 W for a single human brain, versus around 30 MW for the largest supercomputer "Fugaku".[10-12] By comparing the average computational power of the human brain, 1 exaFLOPS (or $1x10^{18}$ FLOPS) to that of the Fugaku supercomputer, around 442 petaFLOPS ($4.42x10^{17}$ FLOPS), we can estimate that the human brain still has roughly 2.3 times more computational power than Fugaku and is roughly 3.4 million times more energy efficient (today, 2021).[13] It is therefore worth to investigate if there is another path that leads to better computers, or to computers that give us the ability to calculate or investigate things that are not (and might never be) possible with current computer technology.

One technology that tries to overcome these limitations is neuromorphic computing, in which the design of hardware components is inspired on the neural network of the human brain.[14] Each "neuron" can act independently sending signals to different other neurons, creating a more flexible way of communicating compared to classical transistors-in-a-chip approach. The basic chip either uses pure digital CMOS technology (as do classical chips), or a hybrid between analogue and digital components, allowing for a significant increase in energy efficiency. The current state-of-the-art neuromorphic chips consume about 2.3 µW/neuron.[15] The computational performance not only depends on the number of neurons, but also on the number of synapses per neuron and the underlying circuit design.

An alternative concept would be a quantum computer, which is predicted to enable incredible things with promises ranging from solving all traffic issues to simply calculating a cure for a specific disease.[16] But as with every new technology, going from initial theories to actual real-life applications requires a lot of time and effort; Just like understanding the physics of nuclear fusion, does not give you a nuclear fusion reactor large enough to provide for the entire human energy demand. So, what makes quantum computers so promising (and challenging)?

1.2. Quantum computer

What makes quantum computer different? The idea behind a quantum computer is that instead of having a simple on/off switch which can produce either a "zero" or a "one", the intrinsic component is a superposition of a quantum state, which can be "zero" and "one" at the same time, but can also take any value in between, a bit comparable to an analogue computer. This is called a quantum bit or qubit. The other important quantum mechanical ingredient is entanglement; two particles can be generated in such a way that their quantum states depend on each other and they can no longer be described independently.[17] These two quantum mechanical principles, superposition and entanglement, lead to an exponential increase in computational power; every qubit added to the entangled system doubles the computational power. This is the promise of a quantum computer.

The idea of a quantum computer is often posed as a solution to classical computers, in which performance gain would be reached by switching to a new technology rather than going smaller in transistor size. However, simply put, classical computers are good at performing linear calculations, i.e., one after the other, while quantum computers are more suitable for parallel calculations. A quantum computer would never be faster at performing linear operations. They are so fundamentally different that they should be viewed as separate technologies with each their own goal and purpose, leading to a completely different class of problems that can be addressed, making them very suitable as complementary technologies.

1.3. Approaches to quantum computing

There are different ideas and approaches, which are currently being investigated for quantum computation, with varying levels of success, and although some claim to have achieved multi-qubit computations already, none of these techniques have been able to demonstrate a commercially viable machine. An overview is shown in Figure 1.2.

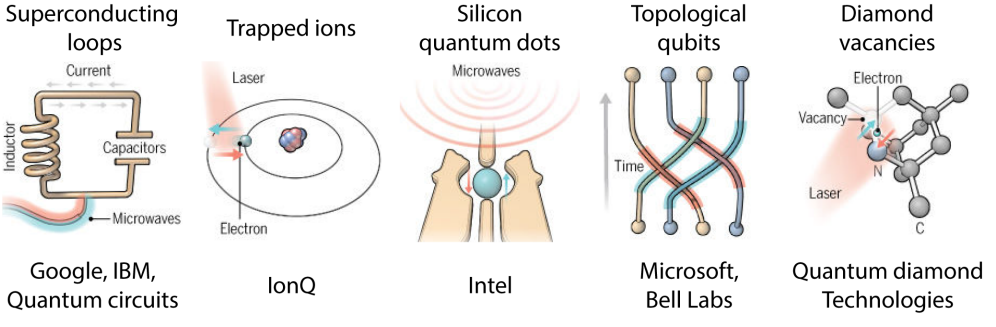


Figure 1.2 | Overview of different approaches to quantum computing. Overview of the different approaches to quantum computation currently being investigated by the companies noted below each technique. Edited from sciencemag.org

Every one of these techniques has its own advantages and disadvantages with regards to the most important aspects: the lifetime of the quantum state, the accuracy of the measurement (success rate) and the scalability (the number qubits that can be entangled).[18-24] Where the superconducting qubit is very fast, but unstable (short lifetime), the trapped ions are the opposite: slow, but very stable. Silicon quantum

dots are stable, but hard to entangle and must be kept cold. Diamond vacancies, on the other hand can operate at room temperature but are very difficult to entangle (so poor scaling of the total qubit system). Finally, topological qubits are predicted to have the highest success rate but are not yet demonstrated experimentally. So, in summary, the main issue with almost all these techniques is the fundamental fragility of a quantum state leading to decoherence, or loss of the quantum information. The coherence time, a measure for how long the quantum state is stable, is very short, and limits the number of quantum operations that can be done before the information is lost. Therefore, it is also difficult/impossible to scale to larger circuits. A huge number (10^6) of overhead quantum bits per quantum bit is needed to maintain the quantum information. This is the main challenge for developing a quantum computer.

One solution could be to use topology. Topology describes a geometric object when it is being deformed. Simply put, objects with the same number of holes (a table and a pencil (0 holes), a coffee cup and a donut (1 hole), or a pair of scissors and spectacles (2 holes)) are mathematically identical. It costs a lot of energy to change the topology of a system (i.e., to add or remove a hole). Therefore, topology is predicted to be useful to stabilize or 'preserve' a quantum state, making it possible to scale to larger quantum systems. A topological quantum bit can be realized in a superconductor-semiconductor hybrid device.[25] A Majorana state in this system carries the quantum information. This technique, however, is still in early fundamental stages and has to date not produced a qubit. The experiments and results described in this thesis show a physical approach, superconductor-semiconductor nanowire hybrids, to make a platform that could host these Majorana fermions and potentially make the first topological quantum computer a reality.

The motivation for this thesis and the lay-out of the platform applicable to this topic are described in Chapter 2. The setups and machines most important to the work described in this thesis are briefly discussed in Chapter 3. The results are split over three chapters: out-of-plane InSb nanowire growth in Chapter 4, in-plane nanowire growth in Chapter 5 and the realization of selective superconductor-semiconductor nanowire hybrids is discussed in Chapter 6. Finally, a

conclusion and an outlook on the future expansion of the field are discussed.

1.4. References

1 Tudge, C. *Neanderthals, bandits and farmers: How agriculture really began*. (Yale University Press, 1999).

2 Buchanan, R. A. History of technology. *Encyclopædia Britannica* (2020).

3 Moore, G. E. *Cramming more components onto integrated circuits*. (McGraw-Hill New York, NY, USA:, 1965).

4 IEEE.org. *International Roadmap For Devices and Systems*. (IEEE, 2020).

5 Singer, N. Facebook's Push for Facial Recognition Prompts Privacy Alarms. *The New York Times* (2018).

6 Google. Our approach to facial recognition.

7 Interpol. Facial recognition.

8 Marcus, G. & Davis, E. *Rebooting AI: Building artificial intelligence we can trust*. (Vintage, 2019).

9 Neuroscience, S. f. The Neuron. *Brainfacts.org*.

10 Moss, S. Fugaku retains top spot as world's most powerful supercomputer in Top500 ranking. *DataCenterDynamics* (2020).

11 top500.org. Supercomupter Fugaku. *top500* (2020).

12 Ling, J. Power of a human brain. *The physics factbook* (2001).

13 Markram, H. The human brain project. *Scientific American* **306**, 50-55 (2012).

14 Intel. Neuromorphic Computing. *Intel.com* (2020).

15 Furber, S. *et al.* Neuromorphic Computing Technology (NCT) state of the art overview. *NEUROTECH* **3517266** (2020).

16 Bernal, N. Unlocking secrets of the universe, curing disease and supercharging AI: How Britain can win the race to create quantum computers. *The Telegraph* (2019).

17 Horodecki, R., Horodecki, P., Horodecki, M. & Horodecki, K. Quantum entanglement. *Reviews of modern physics* **81**, 865 (2009).

18 Popkin, G. Scientists are close to building a quantum computer that can beat a conventional one. *Sciencemag* (2016).

19 Google. Google Quantum. *research.google* (2020).

20 Microsoft. Microsoft quantum. *Microsoft.com* (2020).

21 IBM. IBM quantum. *IBM.com* (2020).

22 IonQ. A true quantum leap. *ionq.com* (2020).

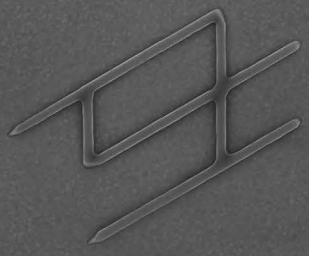
23 Intel. Intel Quantum computing. *Intel.com* (2020).

24 QDTI. Quantum Diamond Technologies. *QDTI.com* (2020).

25 Lutchyn, R. M. *et al.* Majorana zero modes in superconductor–semiconductor heterostructures. *Nature Reviews Materials* **3**, 52-68, doi:10.1038/s41578-018-0003-1 (2018).

Chapter 2

Background



2.1. Introduction

One of the most peculiar claims in the theory of quantum mechanics is a discovery by Ettore Majorana in 1937, in which he found a real solution to the Dirac equation, which describes that all half integer fermions have an anti-particle that is different from themselves.[1,2] The solution of Majorana suggests that there exists a particle that is also its own anti-particle, meaning it cannot have electric charge, making it very difficult to detect. These Majorana fermions were originally thought to give an explanation for the neutrino, and although neutrino's have been demonstrated to exist experimentally, Majorana fermions still have not been successfully detected.[3] In 2001, a new approach was proposed by Kitaev, in which a combination of a semiconducting quantum wire with a superconductor could potentially host Majorana fermions.[4] In 2010, a clear path was proposed for realizing such quantum structures: a semiconducting nanowire, partially covered with a superconducting thin film with a magnetic field applied in-plane along the nanowire (see Figure 2.1).[5,6]

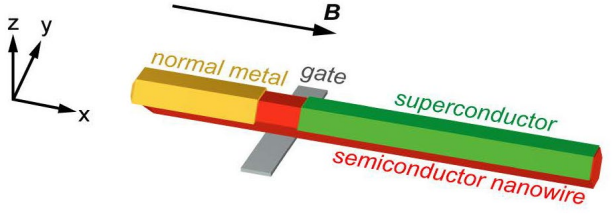


Figure 2.1 | Schematic of semiconductor-superconductor hybrid for detecting Majorana fermions
A semiconductor nanowire (red) partially covered with superconducting material (green) and a normal metal (yellow). A tunnel gate is located underneath the metal-free region of the nanowire. A magnetic field needs to be applied along the nanowire in order to be able to detect a signature of a Majorana fermion. Source:[7,8]

Looking at the electronic dispersion of the quantum wire, it needs to have discrete energy levels (Figure 2.2a).[1,7,9] A strong Rashba spin-orbit interaction will cause the energy band to split in two separated spin ("up" and "down") directions and shift $\pm k_{SO}$ along k_x direction and an energy E_{SO} down (Figure 2.2b). Ideal candidates for this type of experiment are therefore heavy element materials due to their strong spin-orbit interaction. Examples are InSb, InAs (group III-V

materials), but potentially also PbTe or SnTe (group IV-VI materials). By applying an external magnetic field along the nanowire, an energy gap opens up at the crossing of the two energy bands (**Figure 2.2c**) with an energy two times the Zeeman energy $2E_z$. By adding an s-wave superconductor to the system and fixing the chemical potential μ to the middle of the Zeeman gap, the energy spectrum is mirrored around the Fermi level, with a superconducting gap opening up at finite k (**Figure 2.2d**). Looking at the nanowire device layout (**Figure 2.1**), the Majorana pair is localized at the ends of the induced superconducting region in the nanowire (where the superconducting segment ends).

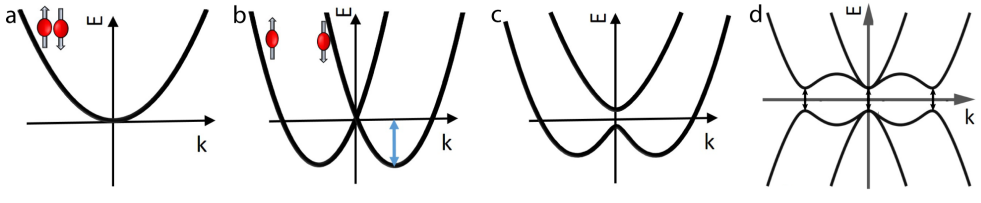


Figure 2.2 | Electronic dispersion of a quantum wire
Energy dispersion without (**a**) and with the effect of Rashba spin-orbit interaction (SOI) (**b**), an applied external magnetic field (**c**) and an added superconductor to the quantum wire (**d**). Adapted from:[1,9]

Upon applying an in-plane magnetic field to an InSb nanowire, which was partially covered by a NbTiN superconducting segment, the first signatures of Majoranas (or Majorana zero modes) have been demonstrated in 2012.[10] However, no definitive proof for the existence of Majorana fermions has been shown to date.

One possible method for demonstrating the existence of Majorana fermions is by performing a so-called "braiding" experiment (**Figure 2.3**), in which two Majorana fermions are exchanged by moving them around while keeping them far enough apart such that they do not interact (γ_2 moves down, then γ_3 moves from right to left, then γ_2 moves up-right in the example). This requires a three-terminal or T-shaped nanowire network with three superconducting islands, each hosting a Majorana pair located at the outer ends of the island.

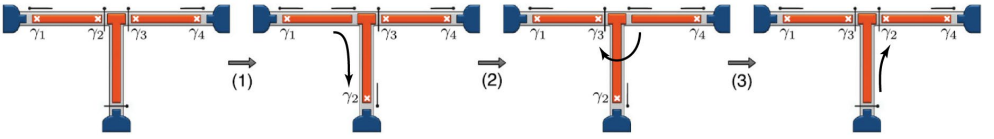


Figure 2.3 | T-shaped nanowire network for Majorana braiding
Basic T-shaped semiconductor (grey) network design with superconducting islands (orange) to perform a Majorana braiding experiment. Adapted from:[11].

Another option is using a nanowire network to create a readout or manipulation circuit for a single topological qubit.[12,13] As shown in Figure 2.4, this requires three pairs of Majoranas (crosses), located at the ends of a topological superconductor segment (superconductor on semiconductor, blue). Furthermore, this three-by-two nanowire network (three horizontal and two vertical at the ends) consists of normal contacts at the ends (R, yellow), three gate defined quantum dots (red) and a superconducting bridge between two of the topological segments. By changing the parity of one of the quantum dots (odd or even number of electrons on it by using the Coulomb blockade), the phase in the corresponding loop is shifted by π, swapping coupled Majorana states. This is considered a more convenient way of braiding.

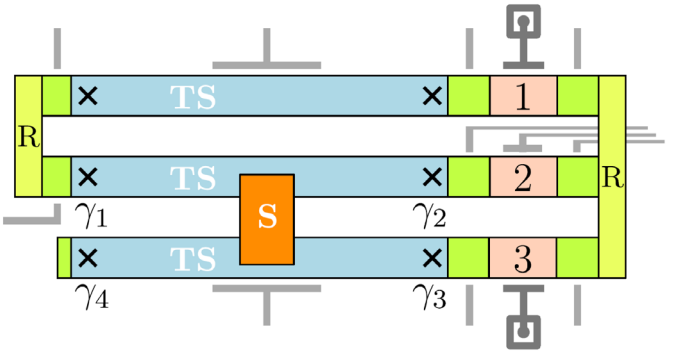


Figure 2.4 | Schematic for a semiconductor-superconductor single qubit design
Design proposal for a single topological qubit, with a semiconductor nanowire network (green), superconductor on semiconductor (i.e., TS, topological superconductor blue), normal metal readout contacts (R, yellow), superconductor only (S, orange) and gate defined quantum dots (1, 2, 3, red). Three pairs of Majoranas form at the end of the topological superconductor segment (crosses). Image source:[13]

Considering that this three-by-two design would accommodate a single topological qubit, scalability is an important aspect of the physical realization of semiconductor-superconductor hybrid devices. In this thesis, the focus will be on III-V materials, with InSb in particular. The different growth techniques (out-of-plane nanowire growth and in-plane growth) for achieving high-quality nanowires as well as nanowire networks are discussed as well as the advantages and limitations of each method. Finally, a brief overview of interesting superconducting materials is described.

2.2. III-V semiconductors

III-V semiconductors are very promising materials for a wide range of applications, from opto-electronics to quantum computing applications.[4,6,14-17] These materials can be grown as thin layers, to create a 2-dimensional electron gas (2DEG) for example.[18,19] These can be used to define 1-dimensional electron channels by chemical etching or by utilizing gate electrodes; this is known as the *top-down* approach.[20] Alternatively nanowires can be assembled starting from molecular or atomic precursors; this is known as the *bottom-up* approach.[21] We have chosen to work with the bottom-up approach, since it offers the possibilities of 1) forming well-defined surface termination by low-energy flat facets, 2) creating heterostructures. This chapter represents a summary of InSb nanowire growth over the years, with a specific focus on research towards quantum computing applications.

2.2.1. Epitaxial growth

For high-quality in-plane growth of one semiconductor on top of another, several aspects are of key importance: i) realizing epitaxial growth, ii) accommodating differences in unit cell dimensions, and iii) realizing layer-by-layer growth rather than island formation.

Epitaxial growth implies the continuation of the crystal lattice from substrate to overlayer. Apart from a clean substrate surface, important for high quality epitaxy is matching of the lattice constants of the different materials, where a lattice mismatch can cause defects at the interface between the layers or even cause defects that propagate through the grown semiconductor material. Figure 2.5 shows the energy band alignment of the different III-V and group IV semiconductors versus the lattice constant of the material. The main interest in the field of topological quantum computing based on Majorana quasiparticles is focused on InAs and InSb. Both materials have a relatively small band gap, and especially InSb has a relatively large lattice constant compared to any other III-V semiconductor.

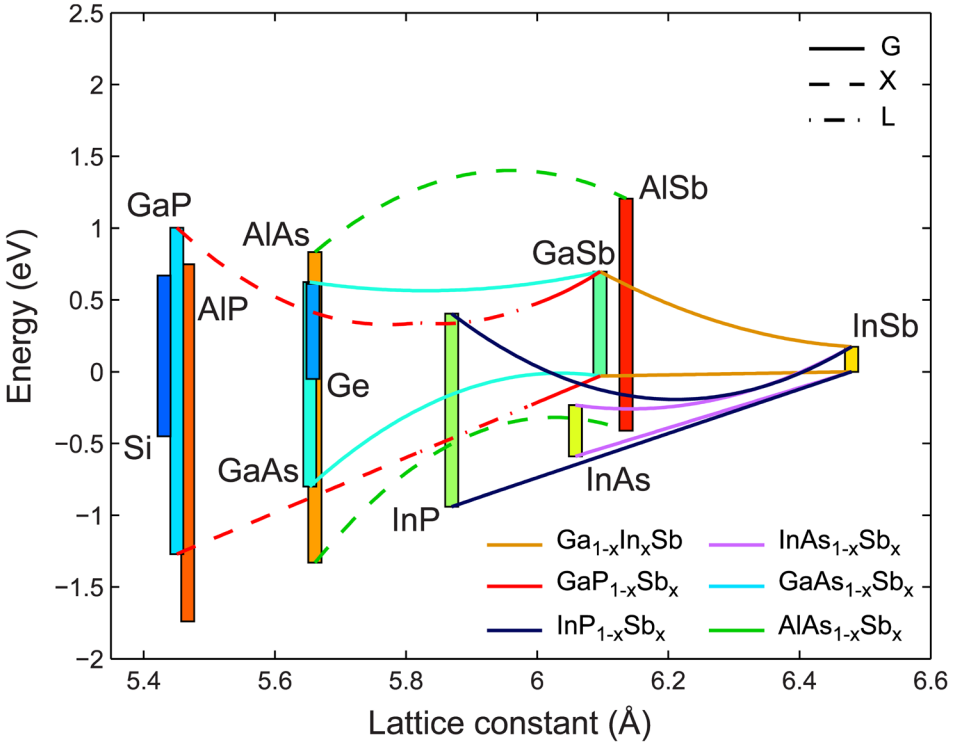


Figure 2.5 | Bandgap versus lattice constant for III-V semiconductors
Bandgap energy alignment of different III-V semiconductor materials (and silicon and germanium) versus the lattice constant of each material. InAs (middle) and InSb (far right) both have relatively small bandgaps, but very different lattice constants. Image source:[22]

For the epitaxial growth of thin layers three growth modes have been identified, their occurrence depending on the lattice mismatch to and surface energy of the underlying layer (see **Figure 2.6**): Volmer-Weber (VW), Stranski-Krastanov (SK) or Frank-Van der Merwe (FM).[23,24] When the adlayer of atoms has a higher surface energy than the substrate and there is a large lattice mismatch between the substrate and film material, the film will grow in separated islands (VW), which will expand and eventually merge to form a film. Due to the large lattice mismatch and the different islands merging, many crystal defects can be present in the final film. If the surface energy of the adlayer is lower than the substrate, layer-by-layer growth initiates. If, however, there is a lattice mismatch between the substrate and film, the strain induced in the few monolayers of film results in island growth on top (SK). The

last growth mode (FM) occurs when the lattice mismatch between the substrate and the film material is very small and the surface energy of the film material is smaller or equal to the substrate surface energy. In this case, the film grows in a layer-by-layer fashion and is therefore particularly suitable to grow high-quality 2DEG materials with very low defect densities.

An example where many requirements for high-quality epitaxial growth are successfully addressed is that of a stack for a 2-dimensional electron gas (2DEG).[25] In this case, a III-V semiconductor substrate is used and a stack of buffer layers, the material of interest (InSb, InAs, etc.)[18,19,26-28] and capping layers are grown on top. The buffer layers accommodate for (part of) the lattice mismatch, thereby minimizing the defect density. In addition, it is crucial that the bandgap of the material of interest is smaller than those of the buffer and capping layers, in order to confine the electronic transport to the active layer.

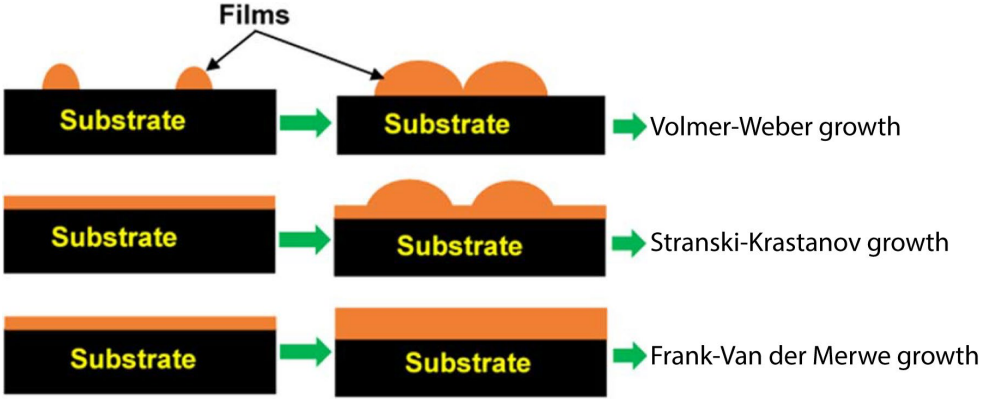


Figure 2.6 | Thin film growth modes
Different growth modes for thin film deposition. **a**: Island growth or Volmer-Weber growth. **b**: strained layer and then island growth or Stranski-Krastanov growth. **c**: layer by layer growth or Frank-Van der Merwe growth. Image source:[23]

2.2.2. Out-of-plane nanowire growth

As represented in **Figure 2.5**, the lattice constant between InSb and any other III-V semiconductor is rather significant, making it difficult to grow high-quality films on insulating substrates. First attempts to create Majorana devices were therefore done using nanowires. Nanowires only have a minimum amount of surface contact

with the substrate, thereby allowing for defect-free strain relaxation in the close vicinity of the substrate-nanowire interface. This allows for the growth of e.g., high-quality InSb nanowires on InP substrates. Nanowires grown based on the vapor-liquid-solid mechanism were first demonstrated in 1964 by researchers from Bell Labs.[29] The principle uses a semiconductor substrate covered with metal nanoparticles, for InSb this is generally gold, but also silver has been demonstrated to work[30-32] (catalyst-free InSb nanowire growth has been shown as well, but with significant poorer crystal quality).[33-35] By heating up the substrate above the eutectic temperature, the metal and the semiconductor can form an alloy. Exposing it to precursor materials (vapor), the gold particles can absorb the precursors from the gas phase and become liquid. Upon supersaturation of the nanoparticle, a layer of semiconductor material (solid) crystallizes between the substrate and the particle. This way, the nanowire "grows" underneath the gold droplet. A complication for growing InSb nanowires is the low surface energy of Sb, leading to a change in contact angle between the gold particle and the substrate surface, which in turn causes the gold nanoparticles to crawl over the substrate surface rather than grow a nanowire upwards, as sketched in **Figure 2.7a**.[36] The first papers showing successful growth of InSb nanowires solved this issue by growing InAs or InP stems first, using Trimethylindium (TMIn) and arsine (AsH_3) or TMIn and phosphine (PH_3), respectively, as precursor materials in a metal-organic vapor phase epitaxy machine (MOVPE)[37-39] or chemical beam epitaxy (CBE).[40,41] The InSb nanowires are consecutively grown on top the stems (as in **Figure 2.7b**). The advantage of this approach is that the gold droplet is "locked" to the top surface of the stem, blocking it from crawling. As **Figure 2.7c** and **Figure 2.7d** show, there is significant layer growth on the substrate surface, which directly competes with the nanowires for supply material. This can be solved by using an amorphous mask (e.g., Si_xN_y, SiO_x, AlO_x) in which small openings are etched and filled with a thin layer of gold. This allows for faster growth of the InSb nanowires as well as the ability to grow large-scale ordered arrays (**Figure 2.7e** and **Figure 2.7f**). For the purpose of this thesis, the VLS method has two main challenges: 1) For the procedure with an InP stem described above, the InSb wire length is limited. 2) Out-of-plane nanowire growth yields limited scalability. Here, the challenges as well as the routes to overcome them are discussed.

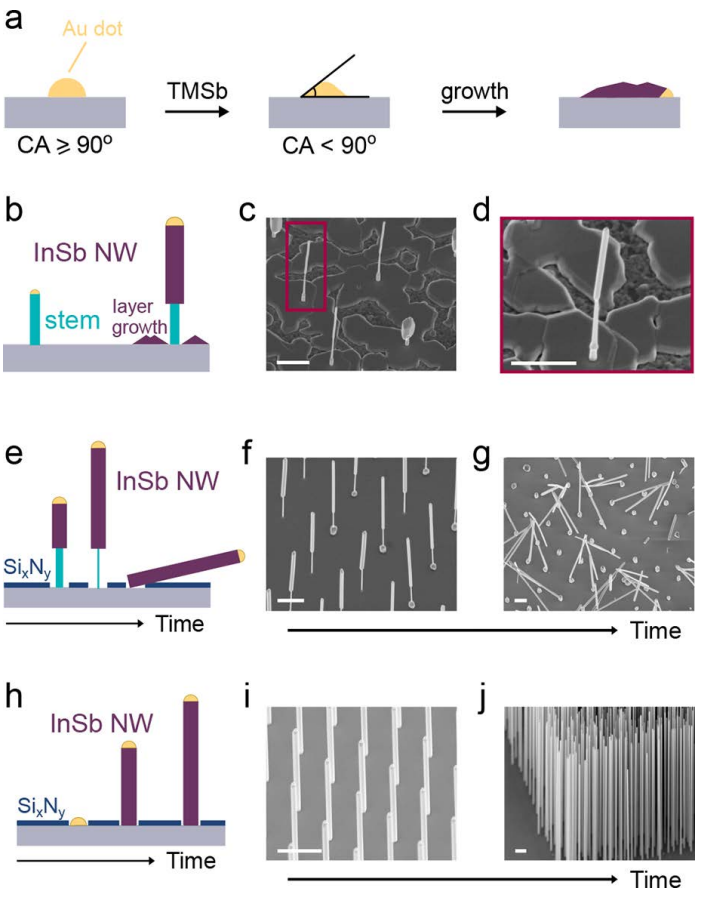


Figure 2.7 | Overview of nucleation and growth limitations and solutions of InSb nanowires

a: During the nucleation step of InSb nanowire growth the gold droplet is filled with Sb, changing the contact angle of the gold catalyst and the substrate, causing the droplet to crawl during subsequent growth. **b**: First, an InP stem is grown using the gold catalyst. Next, the InSb nanowire is grown on top of the stem to avoid the crawling depicted in (**a**). (**c**) and (**d**) show a typical scanning electron microscope (SEM) image of InSb nanowires grown on stems. Note that there is significant parasitic layer growth on the substrate. A Si_xN_y mask can prevent this parasitic growth (**e**) and allow for longer growth times. During growth of the InSb nanowire, the InP stems slowly evaporate (**f**) and eventually break (**g**), limiting the maximum length of the InSb nanowires. A solution for this is to grow stemless InSb nanowires on an InSb substrate (**h-j**) allowing for very long (>10 µm) InSb nanowires. Image source:[36].

1) The limitations in the length of the InSb nanowires are set by the evaporation of the InP stem during growth of the InSb top part. Under the growth conditions in **Figure 2.7e**, the amorphous mask suppresses the evaporation of phosphorus from the substrate during InSb growth (grown at temperatures above evaporation temperature of phosphorus), which reduces the background pressure of phosphorus in the chamber. Although this can be beneficial for the doping levels in the InSb nanowire, it does cause the InP stems to evaporate faster during the growth of the InSb nanowire. Over time, the InP stems will not be able to support the weight of the InSb nanowires and start collapsing (**Figure 2.7g**), intrinsically limiting the maximum length of the InSb nanowires to only several micrometres. Another consequence of using stems as a basis, is the incorporation of phosphorus (0.11 +- 0.02 %) and arsenic (5.5 +_ 0.5 %) in the InSb nanowire, which can be detrimental for quantum transport experiments. A solution for this is growing homoepitaxially on InSb 111 substrates[42,43] with an amorphous mask (**Figure 2.7h**),[36] leading to well controlled long nanowires, reproducible on a large scale (**Figure 2.7i** and **Figure 2.7j**), with mobilities averaging $\mu = 4.4 \times 10^4$ cm^2/(V·s).

2) The development of growing stemless InSb nanowires is an important achievement to create high quality and high purity material for Majorana-related quantum experiments. However, as can be seen in **Figure 2.4** at the beginning of this chapter, in order to perform an actual quantum bit operation with Majorana quasi-particles (i.e., Majorana braiding experiment) a network of several nanowires is required. Nanowire networks can be achieved by the VLS mechanism by growing the nanowires inclined to the substrate surface. This can be done by manipulating the droplet position on top of the stem before starting the InSb nanowire growth[44] or halfway the stem and growing kinked stems.[45] The main limitation of this technique is control over the actual droplet position and therefore the chance of successfully forming InSb networks. This is solved by using substrates with V-grooves which are fabricated with well-defined nanowire positions and growth directions, allowing the realization of both InAs and InSb nanowire networks (**Figure 2.8a**).[46,47]

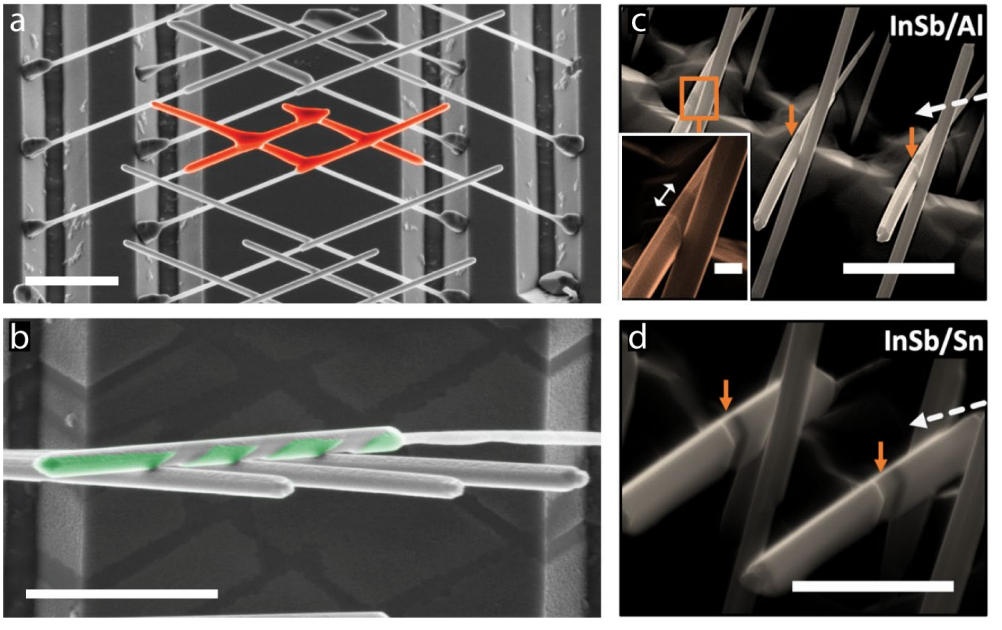


Figure 2.8 | Trenched substrates yielding nanowire networks and semiconductor-superconductor hybrids.
a: InP (100) substrate with etched trenches. An amorphous mask and patterned gold dots on the trench sides enabled the growth of InSb nanowire networks (red) on InP stems. **b**: InSb nanowire with multiple well-defined superconductor islands (aluminium, green) by using other nanowires as shadowing objects. **c, d**: Trenched InSb wires with shadowed aluminium and tin. The shadows are indicated by the orange arrows (inset in **c** is a zoom I on the shadow region). Scale bars are 1 µm. **a, b** edited from[46] and **c, d** edited from[47].

This technique also enables the shadowed deposition of superconductors on the nanowires (Figure 2.8b-d). As shown in Figure 2.1, a basic device consists of a semiconducting nanowire with a superconducting island. In order to create a well-defined island, the nanowire could be fully covered with a superconductor from one side and subsequently etched selectively. However, this causes damage to the nanowire surface exactly at the region where the Majorana quasiparticle is predicted to appear. Alternatively, one nanowire in the trench can be used as a shadowing object in front of a second wire. This way, a well-defined shadow region occurs while leaving the nanowire surface fully intact. This technique thus allows for *in-situ* superconductor island deposition, leading to a high-quality interface between wire and superconductor.

The major limitation for the VLS method is scalability. By growing a nanowire network using the VLS method as shown in Figure 2.8a, the complexity increases with every nanowire added to the network. Additionally, the junctions are at least two times the wire diameter, locally affecting the one-dimensionality of the system. As will be shown later in this thesis (Chapter 4), a single qubit design as shown in Figure 2.4 is technically possible, although it is already very challenging to achieve. Larger networks have been impossible to generate with VLS nanowires to date. Therefore, a different approach is required to move to larger scale one-dimensional networks.

2.2.3. In-plane nanowire networks

Scalable nanowire networks can be realized in-plane, using selective area growth or epitaxial lateral overgrowth.[48] The technique uses a crystalline substrate (silicon or a III-V compound) with an amorphous mask on top. Certain areas of the mask are etched through to the substrate in a predefined pattern (lines, networks etc.).[49-54] An example is shown in Figure 2.9a, where InAs nanowire networks are successfully grown on InP and GaAs (100) substrates with and without buffer layers.[50] The in-plane crystal directions need to be considered as it influences the preferred terminating side facets of the nanowire (see insets), and defines the directions along which nanowires can grow. The final stable terminating facets are defined by the crystal directions with the lowest surface energies. These surface energies are dependent on the growth material, the growth temperature and the V/III ratio during the growth.[55] In most III-V semiconductors (110) facets dominate the growth form. However, for InAs as well as InSb, the surface energy of (110) and (111) facets are similar, the family of terminating facets depending on the in-plane crystal direction and V/III ratio during growth (see Figure 2.9a insets).[50,55]

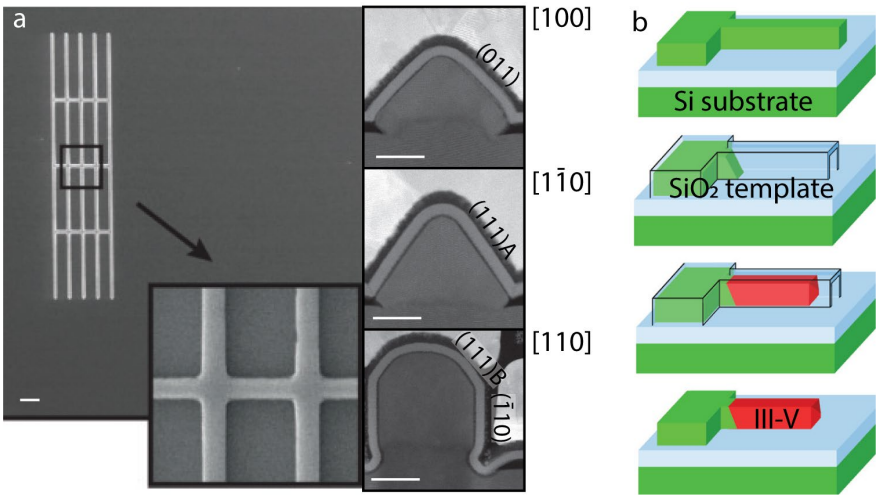


Figure 2.9 | In-plane nanowire growth techniques
a: SEM image of an in-plane InAs nanowire network grown using a selective area mask in a molecular beam epitaxy (MBE) machine. Scale bar is 1 µm. Zoom-in shows the junction uniformity. Insets: Cross-section TEM image showing the morphology of the nanowire grown along different growth directions (mentioned on the right). Scale bars are 50 nm. Image adapted from[50]. **b**: Schematic of in-plane grown nanowires using a silicon oxide tube template. A silicon seed inside is used as the nucleation point to grow a III-V semiconductor nanowire. Image adapted from[56].

Another method to grow in-plane nanowires is by using template-assisted growth (see Figure 2.9b), in which a silicon substrate is etched back and covered with an amorphous oxide mask to define the intended shape of the nanostructure.[56] Next, the hollow SiO_2 template with a silicon seed is used to grow a III-V semiconductor on silicon in the predefined pattern. Finally, the template oxide layer is removed to expose the III-V nanostructure. The advantage of the template-assisted selective epitaxy (TASE) technique is the precise control over the final dimensions of the nanowires, as the SiO_x tunnel defines the width and height. A disadvantage of this technique is the difficulty of growing closed-loop networks. Since the source material needs to reach the growth front, loops in the network will not fully grow if one of the arms will grow until the entrance of the SiO_x tunnel and cuts off further supply of material. Another complication is for the creation of superconducting islands, which requires the SiO_x to be etched first, potentially contaminating the nanowire surface, and reducing the interface quality between wire and superconductor.

2.2.4. Crystal defects

Regardless of the method used, the lattice mismatch between the substrate material and the nanowire material can cause crystal defects which could influence the electronic transport properties of the semiconductor. Crystal defects can generally be classified in four categories:[57,58] **1.** Point or zero-dimensional defects (Figure 2.10a), in which one (or a few) atom(s) is a) missing (vacancy), b) in between the lattice atoms (interstitial), c) of a different material is placed in the lattice (substitution) or d) misplaced (Frenkel pair). These types of defects are mainly dependent on contaminations in the growth chamber during growth, impurities in the source material, or on the ratio between the compounds in case of an alloy semiconductor (e.g., Pb/Te ratio during PbTe growth). **2.** Line or one-dimensional defects, in which a line of atoms is misaligned (see Figure 2.10b) or missing. When, for example, a material with a larger lattice constant is grown on top of substrate with a smaller lattice constant, a misfit dislocation can occur at the interface to accommodate for the lattice mismatch. This is an important type of defect throughout this thesis, due to the large lattice mismatch of InSb with any other III-V semiconductor. **3.** planar or two-dimensional defects are defects that propagate through a plane of atoms, like a twin-plane, an anti-phase boundary or a grain boundary. Twin planes are crystal defects in which the stacking of the different atomic layers is altered, as can be seen in Figure 2.10c, where an ABC stacking sequence is flipped (ABCABACBA, red atoms). Twin planes crossing the nanowire radially, will have a profound effect on the electronic properties of the semiconductor, acting as a carrier scattering source and changing the lattice strain, thereby influencing the electron mobility.[59] Antiphase boundaries, as shown in Figure 2.10d for example (gallium-white, phosphorus-black), are a type of defect in which the stacking of one part of the crystal is mirrored to the other part (left and right-side in the figure), causing atoms of the same type to be placed next to each other instead of in an alternating fashion. This leads to a local electronic charge (energy barrier) in the material, negatively influencing the electronic properties (like mobility).[60] **4.** volume or three-dimensional defects are a type of defect that can be considered as voids in the crystal or inclusion of foreign materials, like the vacancy or interstitial in (1.), but on a slightly larger (3D) scale. An example of this could be residuals of mask material in an etched mask opening on the

substrate. These nanometre-sized pieces of amorphous material could still be overgrown by the semiconductor nanowire. It is therefore important to create a clean substrate surface prior to growth.

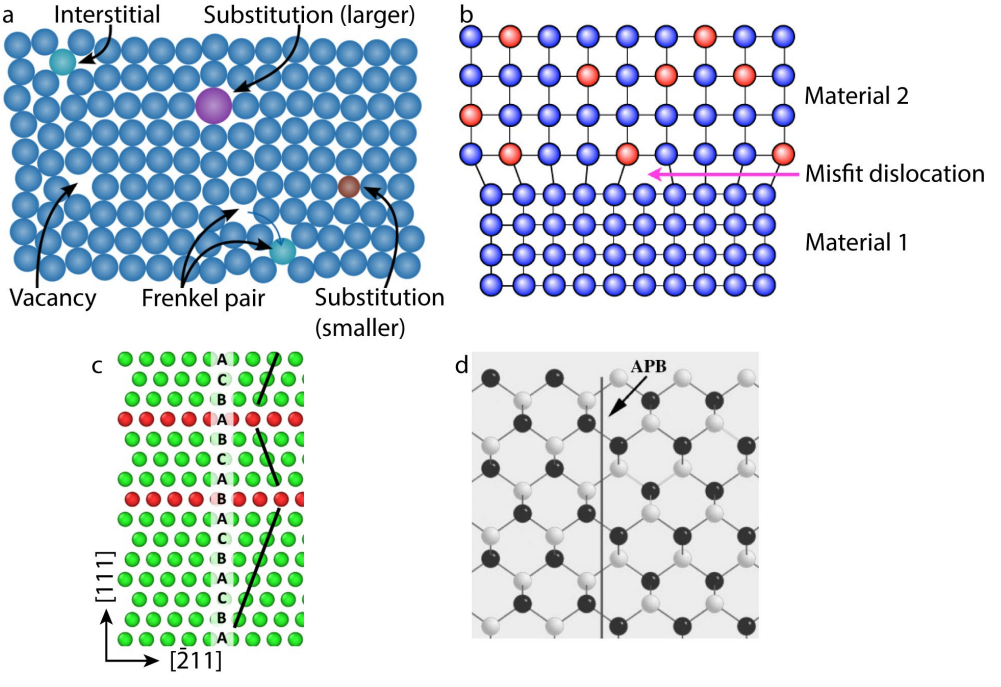


Figure 2.10 | Schematics of crystal defects
a: A schematic summarizing the different types of point defects that can occur in a crystal. b: Misfit dislocation at the interface between two materials with different lattice constant. c: Twin plane boundaries (red), causing the crystal direction to flip. d: anti-phase boundary example in a gallium phosphide (GaP) lattice. Adapted from:[61-64]

2.3. Superconductors

Superconductivity, in which a current can move through a medium without electrical resistance, was first discovered by Heike Kamerlingh Onnes in 1911 in mercury.[65] This state can be achieved when the material reaches temperatures lower than the critical temperature T_c and the external magnetic field stays below the critical coercive field value H_c. Since then, many more materials have been shown to demonstrate superconducting properties, ranging from single element metals, alloys, to copper oxides and even twisted layers of graphene.[66,67] These superconductors can generally be categorized in two sets: Type I and type II superconductors, in which the difference can be found in how they expel magnetic fields.[68] Although the superconductivity for all materials breaks down above their specific T_c, they respond differently to magnetic fields. Type I superconductors lose their superconducting properties above a certain critical magnetic field H_c, whereas type II superconductors start creating vortices (magnetic flux quantum) in the material above a critical field H_{c1} and behave as normal conductors above an even higher critical field H_{c2}. These vortices have normal (as in non-superconducting) cores containing fermionic states that behave as quasiparticle poisoning the hard gap required for the Majorana bound states (i.e., the Majorana quasiparticle can localize in any of the vortices). Therefore, only type I superconductors should be considered for semiconductor-superconductor hybrids for the detection of Majorana fermions.

Furthermore, the superconducting film should be thin (less than 100 nm) such that it can withstand high parallel magnetic fields, and uniform to minimize disorder. On the practical side, the superconductor material ideally forms a self-terminating oxide to avoid oxidation of the complete film and removing the need for a capping layer. Materials that match closely in lattice constant with the semiconductor nanowire are favoured as they are expected to form closed films at only a few nanometres thickness (see material growth modes Figure 2.6). A list of the most promising candidates is shown in Table 2.1.

Element	T_c (K)	H_c (T)	T_{melt} (^{0}C)
aluminium (Al)	1.2	0.01	660
lead (Pb)	7.2	0.08	328
white tin (β-Sn)	3.7	0.03	232
niobium (Nb)	9.2	0.83	2477
vanadium (V)	5.1	0.14	1910
indium (In)	3.4	0.03	156

Table 2.1 | Overview of promising superconductors for hybrid semiconductor-superconductor topological systems.
Overview of promising superconducting materials and their relevant superconducting properties critical temperature (T_c) and critical field (H_c). For processing and device applications, the material melting temperature (T_{melt}) is relevant. Data compiled from:[68-74].

The most researched superconductor from this is aluminium in combination with both InAs as well as InSb nanowires.[46,51,75] Lead and tin are interesting for their higher critical temperature and the first results in combination with InAs and InSb nanowires have been published recently.[47,76] Indium is a potentially suitable candidate in particular for the combination with InAs and InSb as this could potentially remove the intermixing problems that could occur at the semiconductor-superconductor interface. Niobium and vanadium are particularly interesting for their relatively high T_c as well as high H_c but are difficult to process due to their extremely high melting points. This could however be solved by using a shadow deposition technique which would exclude the need for selective etching of the superconductor, a method that has been demonstrated to work for other superconductors.[46,47,77]

2.4. References

1 Zuo, K. & Mourik, V. *Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices*, (2016).

2 Majorana, E. Soryushiron Kenkyu. *Engl. transl from Nuovo Cimento 14, 171 (1937)* **63**, 149 (1981).

3 Reines, F. & Cowan, C. L. Detection of the Free Neutrino. *Physical Review* **92**, 830-831, doi:10.1103/PhysRev.92.830 (1953).

4 Kitaev, A. Y. Unpaired Majorana fermions in quantum wires. *Physics-Uspekhi* **44**, 131-136, doi:10.1070/1063-7869/44/10s/s29 (2001).

5 Lutchyn, R. M., Sau, J. D. & Das Sarma, S. Majorana Fermions and a Topological Phase Transition in Semiconductor-Superconductor Heterostructures. *Physical Review Letters* **105**, 077001, doi:10.1103/PhysRevLett.105.077001 (2010).

6 Oreg, Y., Refael, G. & von Oppen, F. Helical Liquids and Majorana Bound States in Quantum Wires. *Physical Review Letters* **105**, 177002, doi:10.1103/PhysRevLett.105.177002 (2010).

7 Gazibegovic, S. Bottom-up Grown InSb Nanowire Quantum Devices. *PhD Thesis* (2019).

8 Gül, O. Ballistic Majorana nanowire devices. *doctoral thesis*, doi:doi.org/10.4233/uuid:5f84f8a9-b4e7-4248-a9cb-be9bde19b69d (2017).

9 Op het Veld, R. L. M. Controllable Built-in Tunnel Barrier in InSb Nanowires: a New Path Towards Majoranas. *TU/e Master thesis* (2016).

10 Mourik, V. *et al.* Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices. *Science* **336**, 1003-1007, doi:10.1126/science.1222360 (2012).

11 David Aasen *et al.* Milestones toward Majorana-based quantum computing. *Arxiv* (2016).

12 Karzig, T. *et al.* Scalable designs for quasiparticle-poisoning-protected topological quantum computation with Majorana zero modes. *Physical Review B* **95**, 235305, doi:10.1103/PhysRevB.95.235305 (2017).

13 Plugge, S., Rasmussen, A., Egger, R. & Flensberg, K. Majorana box qubits. *New Journal of Physics* **19**, doi:10.1088/1367-2630/aa54e1 (2017).

14 Riel, H., Wernersson, L.-E., Hong, M. & del Alamo, J. A. III–V compound semiconductor transistors—from planar to nanowire structures. *MRS Bulletin* **39**, 668-677, doi:10.1557/mrs.2014.137 (2014).

15 Gong, C. *et al.* Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors. *Applied Physics Letters* **103**, 053513, doi:10.1063/1.4817409 (2013).

16 Rogalski, A. History of infrared detectors. *Opto-Electronics Review* **20**, 279-308, doi:10.2478/s11772-012-0037-7 (2012).

17 Mingo, N. Thermoelectric figure of merit and maximum power factor in III–V semiconductor nanowires. *Applied Physics Letters* **84**, 2652-2654, doi:10.1063/1.1695629 (2004).

18 Joo, K. S., Chun, S. H., Lim, J. Y., Song, J. D. & Chang, J. Y. Metamorphic growth of InAlAs/InGaAs MQW and InAs HEMT structures on GaAs. *Physica E: Low-dimensional Systems and Nanostructures* **40**, 2874-2878, doi:10.1016/j.physe.2008.01.014 (2008).

19 Thomas, C. *et al.* High-mobility InAs 2DEGs on GaSb substrates: A platform for mesoscopic quantum transport. *Physical Review Materials* **2**, 104602, doi:10.1103/PhysRevMaterials.2.104602 (2018).

20 Wharam, D. A. *et al.* One-dimensional transport and the quantisation of the ballistic resistance. *Journal of Physics C: Solid State Physics* **21**, L209-L214, doi:10.1088/0022-3719/21/8/002 (1988).

21 Hobbs, R. G., Petkov, N. & Holmes, J. D. Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms. *Chemistry of Materials* **24**, 1975-1991, doi:10.1021/cm300570n (2012).

22 Borg, M. B. & Wernersson, L.-E. Synthesis and properties of antimonide nanowires. *Nanotechnology* **24**, 202001, doi:10.1088/0957-4484/24/20/202001 (2013).

23 Mbam, S. O., Nwonu, S. E., Orelaja, O. A., Nwigwe, U. S. & Gou, X.-F. Thin-film coating; historical evolution, conventional deposition technologies, stress-state micro/nano-level measurement/models and prospects projection: a critical review. *Materials Research Express* **6**, 122001, doi:10.1088/2053-1591/ab52cd (2019).

24 Harsha, K. S. *Principles of vapor deposition of thin films*. (Elsevier, 2005).

25 Pfeiffer, L. *et al.* Formation of a high quality two-dimensional electron gas on cleaved GaAs. **56**, 1697-1699, doi:10.1063/1.103121 (1990).

26 Golding, T. D., Martinka, M. & Dinan, J. H. Molecular-beam epitaxial growth of InSb/CdTe heterojunctions for multilayer structures. *Journal of Applied Physics* **64**, 1873-1877, doi:10.1063/1.341737 (1988).

27 Yi, W. *et al.* Gate-tunable high mobility remote-doped InSb/In1−xAlxSb quantum well heterostructures. *Applied Physics Letters* **106**, 142103, doi:10.1063/1.4917027 (2015).

28 Kudo, M. & Mishima, T. MBE growth of Si-doped InAlAsSb layers lattice-matched with InAs. *Journal of Crystal Growth* **175-176**, 844-848, doi:10.1016/S0022-0248(96)00935-9 (1997).

29 Wagner, a. R. & Ellis, s. W. J. A. p. l. Vapor-liquid-solid mechanism of single crystal growth. **4**, 89-90 (1964).

30 Huang, K. *et al.* Silver catalyzed gallium phosphide nanowires integrated on silicon andin situAg-alloying induced bandgap transition. *Nanotechnology* **26**, 255706, doi:10.1088/0957-4484/26/25/255706 (2015).

31 Vogel, A. T. *et al.* Ag-assisted CBE growth of ordered InSb nanowire arrays. *Nanotechnology* **22**, 015605, doi:10.1088/0957-4484/22/1/015605 (2010).

32 Wittemann, J. V., Münchgesang, W., Senz, S. & Schmidt, V. Silver catalyzed ultrathin silicon nanowires grown by low-temperature chemical-vapor-deposition. **107**, 096105, doi:10.1063/1.3393601 (2010).

33 Mandl, B. *et al.* Crystal structure control in Au-free self-seeded InSb wire growth. *Nanotechnology* **22**, 145603, doi:10.1088/0957-4484/22/14/145603 (2011).

34 Arif, O. *et al.* Growth of Self-Catalyzed InAs/InSb Axial Heterostructured Nanowires: Experiment and Theory. **10**, 494 (2020).

35 Pozuelo, M. *et al.* Self-catalyzed growth of InP/InSb axial nanowire heterostructures. *Journal of Crystal Growth* **329**, 6-11, doi:10.1016/j.jcrysgro.2011.06.034 (2011).

36 Badawy, G. *et al.* High Mobility Stemless InSb Nanowires. *Nano Letters* **19**, 3575-3582, doi:10.1021/acs.nanolett.9b00545 (2019).

37 Caroff, P. *et al.* High-Quality InAs/InSb Nanowire Heterostructures Grown by Metal–Organic Vapor-Phase Epitaxy. **4**, 878-882, doi:10.1002/smll.200700892 (2008).

38 Plissard, S. R. *et al.* From InSb Nanowires to Nanocubes: Looking for the Sweet Spot. *Nano Letters* **12**, 1794-1798, doi:10.1021/nl203846g (2012).

39 Caroff, P. *et al.* InSb heterostructure nanowires: MOVPE growth under extreme lattice mismatch. *Nanotechnology* **20**, 495606, doi:10.1088/0957-4484/20/49/495606 (2009).

40 Ercolani, D. *et al.* InAs/InSb nanowire heterostructures grown by chemical beam epitaxy. *Nanotechnology* **20**, 505605, doi:10.1088/0957-4484/20/50/505605 (2009).

41 Li, A., Sibirev, N. V., Ercolani, D., Dubrovskii, V. G. & Sorba, L. Readsorption Assisted Growth of InAs/InSb Heterostructured Nanowire Arrays. *Crystal Growth & Design* **13**, 878-882, doi:10.1021/cg301565p (2013).

42 Park, H. D., Prokes, S. M., Twigg, M. E., Ding, Y. & Wang, Z. L. Growth of high quality, epitaxial InSb nanowires. *Journal of Crystal Growth* **304**, 399-401, doi:10.1016/j.jcrysgro.2007.03.023 (2007).

43 Vogel, A. T. *et al.* Fabrication of High-Quality InSb Nanowire Arrays by Chemical Beam Epitaxy. *Crystal Growth & Design* **11**, 1896-1900, doi:10.1021/cg200066q (2011).

44 Plissard, S. R. *et al.* Formation and electronic properties of InSb nanocrosses. *Nature Nanotechnology* **8**, 859-864, doi:10.1038/nnano.2013.198 (2013).

45 Car, D., Wang, J., Verheijen, M. A., Bakkers, E. P. A. M. & Plissard, S. R. Rationally Designed Single-Crystalline Nanowire Networks. *Advanced Materials* **26**, 4875-4879, doi:10.1002/adma.201400924 (2014).

46 Gazibegovic, S. *et al.* Epitaxy of advanced nanowire quantum devices. *Nature* **548**, 434-438, doi:10.1038/nature23468 (2017).

47 Khan, S. A. *et al.* Highly Transparent Gatable Superconducting Shadow Junctions. *ACS Nano*, doi:10.1021/acsnano.0c02979 (2020).

48 Hiramatsu, K. *et al.* Recent Progress in Selective Area Growth and Epitaxial Lateral Overgrowth of III-Nitrides: Effects of Reactor Pressure in MOVPE Growth. **176**, 535-543, doi:10.1002/(SICI)1521-396X(199911)176:1<535::AID-PSSA535>3.0.CO;2-I (1999).

49 Aseev, P. *et al.* Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks. *Nano Letters*, doi:10.1021/acs.nanolett.8b03733 (2018).

50 Krizek, F. *et al.* Field effect enhancement in buffered quantum nanowire networks. *Physical Review Materials* **2**, 093401, doi:10.1103/PhysRevMaterials.2.093401 (2018).

51 Vaitiekėnas, S. *et al.* Selective-Area-Grown Semiconductor-Superconductor Hybrids: A Basis for Topological Networks. *Physical Review Letters* **121**, 147701, doi:10.1103/PhysRevLett.121.147701 (2018).

52 Desplanque, L., Bucamp, A., Troadec, D., Patriarche, G. & Wallart, X. In-plane InSb nanowires grown by selective area molecular beam epitaxy on semi-insulating substrate. *Nanotechnology* **29**, 305705, doi:10.1088/1361-6528/aac321 (2018).

53 Desplanque, L., Bucamp, A., Troadec, D., Patriarche, G. & Wallart, X. Selective area molecular beam epitaxy of InSb nanostructures on mismatched substrates. *Journal of Crystal Growth* **512**, 6-10, doi:10.1016/j.jcrysgro.2019.02.012 (2019).

54 Friedl, M. *et al.* Template-Assisted Scalable Nanowire Networks. *Nano Letters* **18**, 2666-2671, doi:10.1021/acs.nanolett.8b00554 (2018).

55 Lin, A., Shapiro, J. N., Eisele, H. & Huffaker, D. L. Tuning the Au-Free InSb Nanocrystal Morphologies Grown by Patterned Metal–Organic Chemical Vapor Deposition. *Advanced Functional Materials* **24**, 4311-4316, doi:10.1002/adfm.201303390 (2014).

56 Schmid, H. *et al.* Template-assisted selective epitaxy of III–V nanoscale devices for co-planar heterogeneous integration with Si. **106**, 233101, doi:10.1063/1.4921962 (2015).

57 Balluffi, R. W. *Introduction to elasticity theory for crystal defects*. (World Scientific Publishing Company, 2016).

58 Bollmann, W. *Crystal defects and crystalline interfaces*. (Springer Science & Business Media, 2012).

59 Shimamura, K., Yuan, Z., Shimojo, F. & Nakano, A. Effects of twins on the electronic properties of GaAs. *Applied Physics Letters* **103**, 022105, doi:10.1063/1.4811746 (2013).

60 Ahn, K. H., Lookman, T., Saxena, A. & Bishop, A. R. Electronic properties of structural twin and antiphase boundaries in materials with strong electron-lattice couplings. *Physical Review B* **71**, 212102, doi:10.1103/PhysRevB.71.212102 (2005).

61 Paul, D. Misfit dislocations. *University of Glasgow Semiconductor device group* (2020).

62 Madhu. Difference between point defect and line defect. *Differencebetween.com* (2018).

63 Karewar, S., Sietsma, J. & Santofimia, M. J. Effect of pre-existing defects in the parent fcc phase on atomistic mechanisms during the martensitic transformation in pure Fe: A molecular dynamics study. *Acta Materialia* **142**, 71-81, doi:10.1016/j.actamat.2017.09.049 (2018).

64 Cohen, D. & Carter, C. B. Structure of the (110) antiphase boundary in gallium phosphide. *Journal of Microscopy* **208**, 84-99, doi:10.1046/j.1365-2818.2002.01070.x (2002).

65 Buckel, W. & Kleiner, R. *Superconductivity: fundamentals and applications*. (John Wiley & Sons, 2008).

66 Ginsberg, D. M. *Physical properties of high temperature superconductors I*. (World scientific, 1998).

67 Cao, Y. *et al.* Unconventional superconductivity in magic-angle graphene superlattices. *Nature* **556**, 43-50, doi:10.1038/nature26160 (2018).

68 Foner, S. & Schwartz, B. B. *Superconductor materials science: metallurgy, fabrication, and applications*. Vol. 68 (Springer Science & Business Media, 2012).

69 Cochran, J. F. & Mapother, D. E. Superconducting Transition in Aluminum. *Physical Review* **111**, 132-142, doi:10.1103/PhysRev.111.132 (1958).

70 Sekula, S. T. & Kernohan, R. H. Magnetic Properties of Superconducting Vanadium. *Physical Review B* **5**, 904-911, doi:10.1103/PhysRevB.5.904 (1972).

71 Eisenstein, J. Superconducting Elements. *Reviews of Modern Physics* **26**, 277-291, doi:10.1103/RevModPhys.26.277 (1954).

72 Matthias, B. T., Geballe, T. H. & Compton, V. B. Superconductivity. *Reviews of Modern Physics* **35**, 1-22, doi:10.1103/RevModPhys.35.1 (1963).

73 Kuzmenko, V., Melnikov, V. & Sudovtsov, A. J. S. P.-J. Concerning the superconductivity of amorphous vanadium films. **47**, 1081-1086 (1978).

74 Peters, S. Superconducting materials for InSb nanowire hybrids. *TU/e Bachelor thesis* (2020).

75 Krogstrup, P. *et al.* Epitaxy of semiconductor–superconductor nanowires. *Nature Materials* **14**, 400-406, doi:10.1038/nmat4176 (2015).

76 Pendharkar, M. *et al.* Parity-preserving and magnetic field resilient superconductivity in indium antimonide nanowires with tin shells. (2019).

77 Heedt, S. *et al.* Shadow-wall lithography of ballistic superconductor-semiconductor quantum devices. (2020).

Chapter 3

Growth and Experimental Methods

Most of the work presented in this thesis is based on experiments performed inside the Nanolab@TUe cleanroom facilities.[1]

In this chapter, the different tools used for the growth and analysis of nanowire samples are briefly described. The core of the work is focused on epitaxial growth of semiconductor-on-semiconductor or superconductor-on-semiconductor using Metal-Organic Vapor Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE). Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) are characterization techniques used for analysing the nanowire samples. These techniques are comprehensively described below.

3.1 MOVPE

Metal-Organic vapor phase epitaxy (MOVPE) (also called Metal-Organic chemical vapor deposition (MOCVD)) is a low-pressure technique for growing high-quality semiconductor materials.[2] The MOVPE reactor used for the work presented in this thesis is an Aixtron horizontal flow reactor with two different reactor chambers that share the same gas lines (Figure 3.1a). In general, these systems are comprised of several sections: a gas cabinet, the reactor, and a glovebox, as schematically represented in Figure 3.1b. The gas cabinet contains the gas lines and the bubblers with the metal-organic source material. When the system is idle, the material sources are closed, and the gas lines and reactor are continuously flushed with purified nitrogen (N_2) gas to avoid oxidation and, for safety reasons, to remove any trace gases that might form over time inside the reactor. When the reactor is running (i.e., growing semiconductor material), hydrogen gas (H_2) is used as a carrier gas. Hydrogen (H_2) gas enters on the left and carries hydride source materials (e.g., PH_3 and AsH_3) or metal-organic source materials (e.g., TMIn, TMSb, TEGa, ...), which are stored in bubblers.

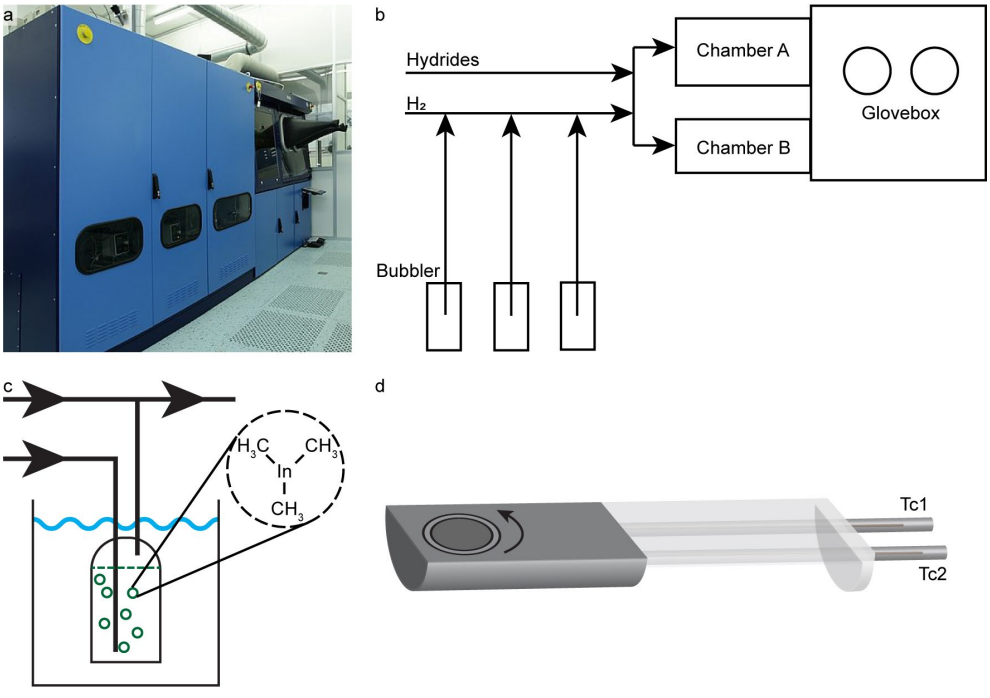


Figure 3.1 | Metal-organic vapor phase epitaxy machine
a. Picture of the metal-organic vapor phase epitaxy (MOVPE) tool used for the experiments in this thesis. **b**. Schematic overview of the system shown in (**a**). **c**. Schematic of the workings of a bubbler with a Tri-methyl-Indium (TMIn) molecule in the inset. **d**. Perspective view of the inside of a growth chamber with susceptor (grey), rotating disk to carry the sample, glass liner and two thermocouples (Tc1 and Tc2).

The bubbler (sketched in Figure 3.1c) is placed in a thermostatic bath, to control the vapor pressure of the precursor material, which ensures reproducibility of material extraction efficiencies and longevity of the source material. When a source is used, H_2 gas is flowing through the bubbler, taking along source material molecules. This gas mixture is then diluted with H_2 in the main gas lines of the system and combined with gas mixtures from other sources. An example of a metal-organic molecule is Tri-Methyl-Indium (TMIn), which is shown in the inset. The evaporation rate of the metal-organic source material depends on the specific source material molecule, the H_2 gas flow rate, the bubbler temperature and bubbler pressure.[2] Prior to the growth, the gas mixture is vented to the exhaust to allow the flows to stabilize. Material growth

is initiated by directing the flow to the growth chamber (chamber A or B on Figure 3.1b).

A glass cylinder, called a liner, forms the outer shell of the reactor chamber. Around the liner, an array of water-cooled infrared heating lamps is positioned to heat the susceptor, which is shown in Figure 3.1d. A silicon carbide (SiC) coated graphite susceptor (grey) is located at the centre of the chamber, with a rotating disk that carries the sample. The gas flow enters the chamber, flows over the susceptor, onto the downstream plate (glass) and exits the chamber on the right. The rotation disk ensures uniform supply of source material during the growth. Precise temperature control is achieved by using two thermocouples (Tc1 and Tc2) at the heart of the susceptor which provide active feedback to a proportional-integral-derivative (PID) controller.

Sample loading and unloading occurs via the loading door of the chamber, through the glovebox (Figure 3.1b) on the right side of the system. The glovebox is an enclosed area under N_2 overpressure to avoid oxygen or water to enter the reactor or react with the growth substrate. Samples can also be stored for longer periods of time in the glovebox to protect them from ambient air.

3.2 MBE

Molecular beam epitaxy (MBE) is an ultra-high vacuum (UHV) technique (10^{-11} mbar range) for growing high-quality epitaxial semiconductor materials, using high-purity elemental (or compound) source materials.[3,4] Where MOVPE suffers from hydrogen and carbon incorporation in the semiconductor layers due to the H_2 carrier gas and the organic molecules of the source material, MBE is designed to minimize any impurities into the grown semiconductor material. By using a segmented design, several steps of cleaning/degassing and a combination of various pumping techniques, an ultra-high vacuum can be created and maintained to minimize impurity incorporation in the grown semiconductor.

An MBE chamber (Figure 3.2a) generally consists of a double walled stainless-steel chamber with a cryo-shroud. A manipulator arm (Figure 3.2b) with an integrated heater and thermocouple carries the sample holder and a main shutter can block the incoming material flux. Sources containing the growth material are located at the bottom of the

chamber all oriented directly at the sample position. Each cell can be independently controlled in temperature and is specifically designed for the material it contains. A beam flux monitor (BFM) can be moved to the sample position to measure the beam equivalent pressure of a source material being evaporated in the chamber, allowing for precise control of the growth flux.

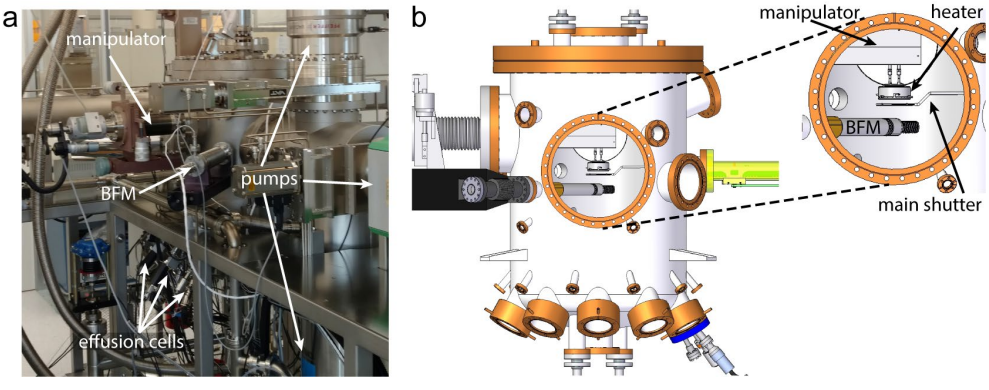


Figure 3.2 | Molecular beam epitaxy system for III-V semiconductors and hydrogen cleaning
a. Picture of the molecular beam epitaxy (MBE) chamber used for III-V semiconductor growth and hydrogen cleaning. **b**. Schematic of the MBE chamber, with the manipulator on the left, a beam flux monitor (BFM) and a main shutter (also see inset). The hydrogen cell is depicted on the bottom.

The ultra-high vacuum in the chamber is achieved by combining several pumping techniques.[5] After closing an MBE chamber, it is pumped with a regular backing pump to low 10^{-2} mbar. The turbopump then takes over and pumps the system further down to low 10^{-6} mbar. With the turbo running, the chamber is baked at 120-150 ^{0}C for several days to outgas the chamber walls and remove water molecules as much as possible from the system. After baking, liquid nitrogen (LN_2) is turned on and will flow through the shrouds (chamber walls) to cool them down to around 77 K acting as a condenser for atoms impinging on the inside walls. The turbopump is then closed and the system is pumped with an ion pump and cryopump, achieving pressures around 10^{-11} mbar. This is the final setup in which semiconductor growth will be performed.

The schematic shown in Figure 3.3 represents a top view of the system used for this thesis. A long transfer tube (horizontal, left to right)

serves to transfer samples from the load locks (left end inside the glovebox and right end) to a degas station or one of the three growth chambers. Each segment is separated using gate valves with the idea that each segment, from load lock towards growth chamber, contains cleaner samples and a better (higher) vacuum.

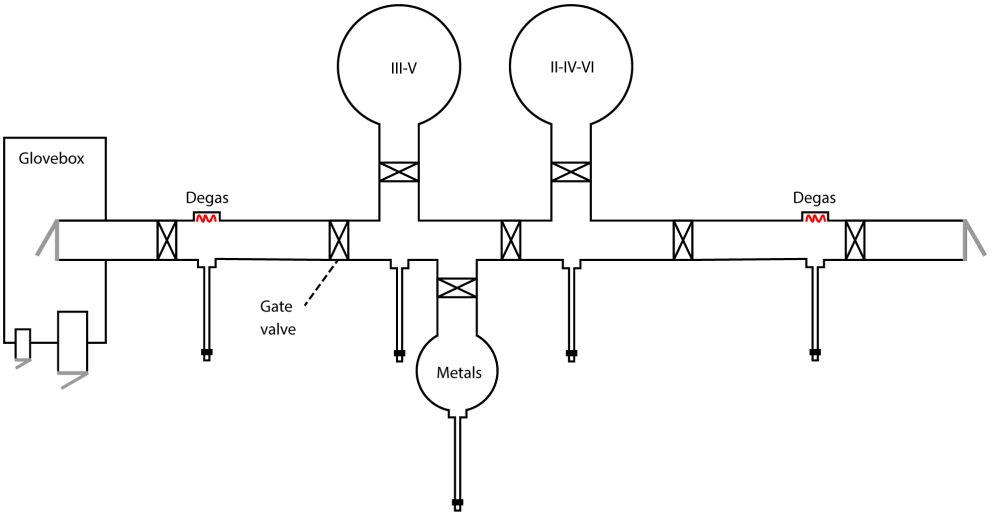


Figure 3.3 | Top view of the molecular beam epitaxy system at Nanolab@TUe
Top view schematic of the molecular beam epitaxy (MBE) system at Nanolab@TUe.[1] The system consists of three different chambers for III-V semiconductors, II-IV-VI semiconductors, and metals. On the left side, samples can be loaded through a glovebox. On the right, directly from ambient. Each segment is separated with gate valves to ensure cleanliness and ultra-high vacuum in the system.

A sample holder is first outgassed at around 600 ^{0}C for 3 hours before mounting any sample, ensuring there are no residual organics or water from the production or cleaning process. Next, samples are mounted using either pure metallic gallium or indium as glue. Indium has a melting point of 429.8 K (156.6 ^{0}C)[6] and is generally used for mounting samples as it is easier to work with for mounting and it does not tend to crawl over the top surface of a sample at higher temperatures. Gallium is used for temperature sensitive samples as its melting point is around 303 K (30 ^{0}C), making it easier to mount and unmount samples without the need for additional heating. The disadvantage is that it tends to crawl over a sample surface at higher temperatures, especially with samples that are covered with a dielectric

layer like Si_xN_y or SiO_x. After the sample is mounted, it is loaded into a load lock, pumped down, and degassed for 2 hours at 300 ^{0}C at a degas station. After this, the sample can be grown on. For this thesis, the III-V chamber (Figure 3.2) is used for hydrogen cleaning and the metals chamber (Figure 3.4) for the deposition of superconductors.

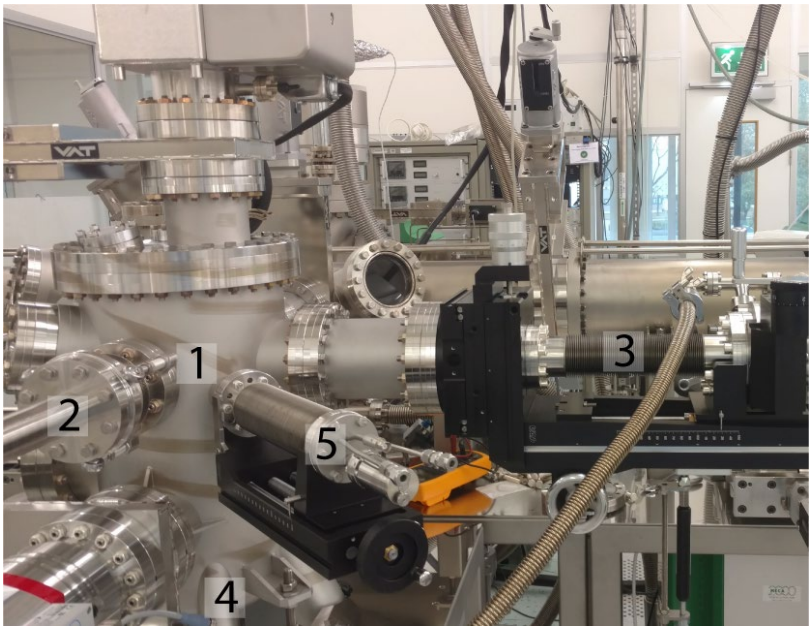


Figure 3.4 | Molecular beam epitaxy chamber for metal deposition
Picture of molecular beam epitaxy (MBE) chamber for metal deposition at cryogenic temperatures. The sample can be loaded into the chamber (**1**) using the loading arm (**2**) onto a cold-stage manipulator (**3**) that can cool with liquid nitrogen (LN2). The deposition rate of the materials from the effusion cells (**4**) can be accurately measured by a quartz crystal monitor (QCM) (**5**).

The chamber in Figure 3.4 is designed for the deposition of superconductors or other metals at low temperatures. The manipulator (3) can be cooled using LN_2 down to 107 K (-166 ^{0}C). In order to get a uniform thin layer of a superconducting metal (e.g., Al) the low substrate temperature allows for decreasing the diffusion length of the impinging adatoms, avoiding the aluminium to ball up and form separate droplets on the semiconductor surface. The metals are evaporated from effusion cells (4) and the deposition rate can be measured using a quartz crystal monitor (QCM, 5).

3.3 Scanning electron microscopy

By using a focused beam of electrons, physical features on the micro- and nanoscale can be visualized. An image is created by scanning a sample area spot by spot in a xy-pattern and capturing electrons that come from the sample surface on a detector.[7] Hence the name scanning electron microscopy or SEM.

A schematic cross-section of an SEM is shown in Figure 3.5a. At the top of the column, an electron beam is created by applying a high voltage on a field emission gun (FE-gun). The electrons are then accelerated and focused in a narrow bundle by using an aperture, magnetic and electrostatic lenses, and coils. To have a well-focused beam hitting the sample surface, the aperture and the astigmatism of the beam need to be adjusted regularly. When the aperture is not perfectly aligned, the beam can partially hit the aperture edge causing electrons to scatter and interfere with the electron bundle, adding distortions and noise to the final image. The astigmatism occurs when the beam does not have a perfectly circular cross-section but slightly elliptical, causing the image to stretch in one direction. To overcome this issue, a stigmator is used to generate an electric quadrupole field that can make tiny adjustments to the electron beam, enabling the user to create a symmetric beam, increasing the image resolution and quality.

Finally, scan coils at the bottom of the column allow for the bundle to move over the sample in an xy-pattern to create an image of the sample surface, pixel by pixel. The electrons coming from the sample surface can be detected with the in-lens detectors and can be either backscattering electrons, meaning they are from the incident beam and scattered on the atoms of the sample, or secondary electrons, which are expelled from the surface atoms by the kinetic energy of the impeding electron beam. The results acquired throughout this thesis are acquired using secondary electrons, which will give a higher resolution on surface details.

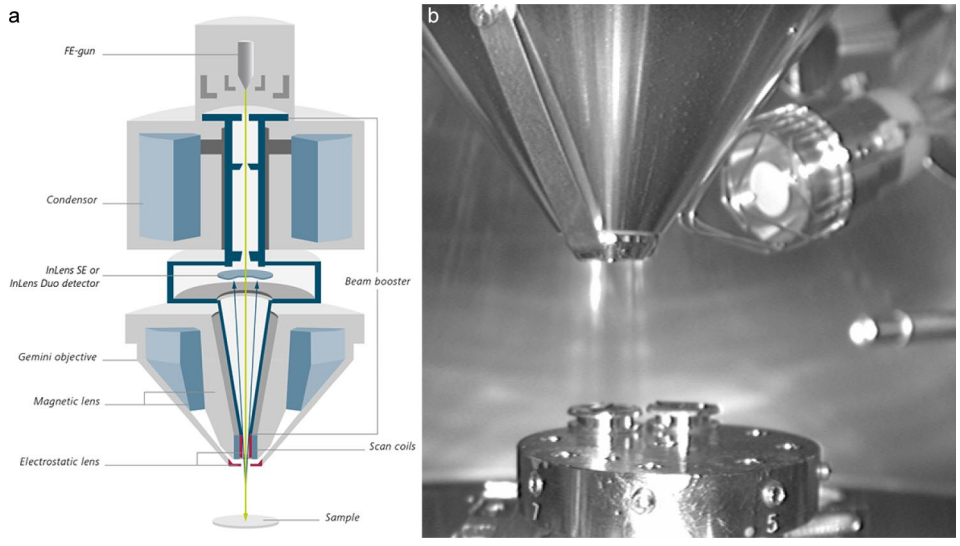


Figure 3.5 | Scanning electron microscope
a. Cross-section schematic view of a Zeiss Sigma scanning electron microscope (SEM).[8] **b**. Picture of the inside of the chamber showing the 5-axes stage with samples, the beam column and manipulator tip.

3.4 Nanomanipulation of nanowires

Nanowires grown out-of-plane, either vertical or inclined under an angle, need to be transferred to other substrates to enable additional studies. For crystallographic characterization by transmission electron microscopy (TEM), nanowires need to be transferred to a TEM-grid, generally consisting of a copper mesh covered with a thin carbon film with holes in it. For electrical transport measurements, nanowires need to be transferred to a suitable substrate that usually has a general or local bottom gate(s) with a dielectric layer on top to electrically insulate the nanowire from the gates. Here, nanowires can be contacted and characterized by electrical transport measurements. For both cases, swiping the growth chip on top of the designated substrate could deposit nanowires for the desired analysis. However, this technique has some intrinsic limitations. The nanowires tend to be spread randomly over the target substrate, with them mostly sticking to the copper mesh for TEM-grids and being randomly oriented, possibly in bundles together, on transport chips, making local gating from the bottom difficult. Additionally, this method can damage the final substrate and add a lot of contamination to the chip.

A way to solve this is by using a nanomanipulator as shown in Figure 3.6a, which consists of a set of piezo-electric motors that can move a tungsten needle, with a micrometre-thick tip, with nanometre accuracy. This way a single nanowire can be taken from the growth substrate (Figure 3.6b) and positioned precisely on the target substrate, enabling a plethora of experiments and analyses on these nanowires. Some examples are: a wire can be placed exactly over a hole in a TEM-grid (Figure 3.6c); it can be positioned exactly perpendicular to and over a bridging gap allowing to perform strain analysis on a quantum dot in the middle of the nanowire; or placing two nanowires in each other's extension to allow for a single focused ion beam (FIB) cut on two nanowires at the same time for TEM analysis. This can all be done while exactly knowing from which location the nanowire came, allowing studying wires from a specific growth pattern with controlled diameter and pitch. Also, nanowires from the same chip can be used for electrical and crystallographic characterization, ensuring the results from these techniques can be correlated to the same nanowires.

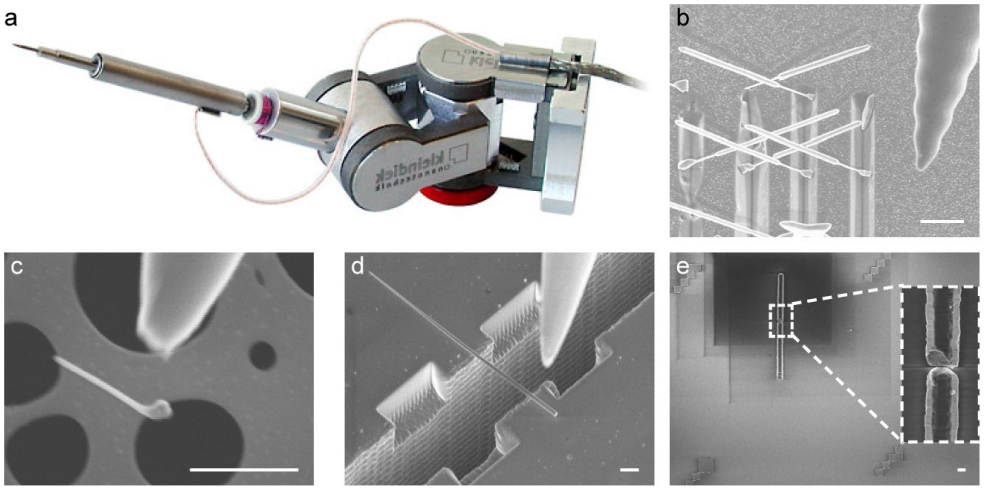


Figure 3.6 | Precise nanowire transfer by nanomanipulator
a. Image of a Kleindiek mm3a-rotip nanomanipulator used to transfer nanowires from the growth substrate to a characterization substrate.[9] **b**. Growth substrate with nanowires grown under an angle. The manipulator tip is on the right showing the sharpness of the tip. Scale bar is 1 µm. **c-e**. Various applications for nanowire characterization substrates demonstrating the advantages and applicability of this technique. Scale bars are 1 µm.

3.4.1 Tutorial

Transferring nanowires using the nanomanipulator is rather straightforward but requires a lot of practice. A few tips and tricks can come in handy when setting up the system for the first time. Figure 3.7 shows how the general system preparation looks like.

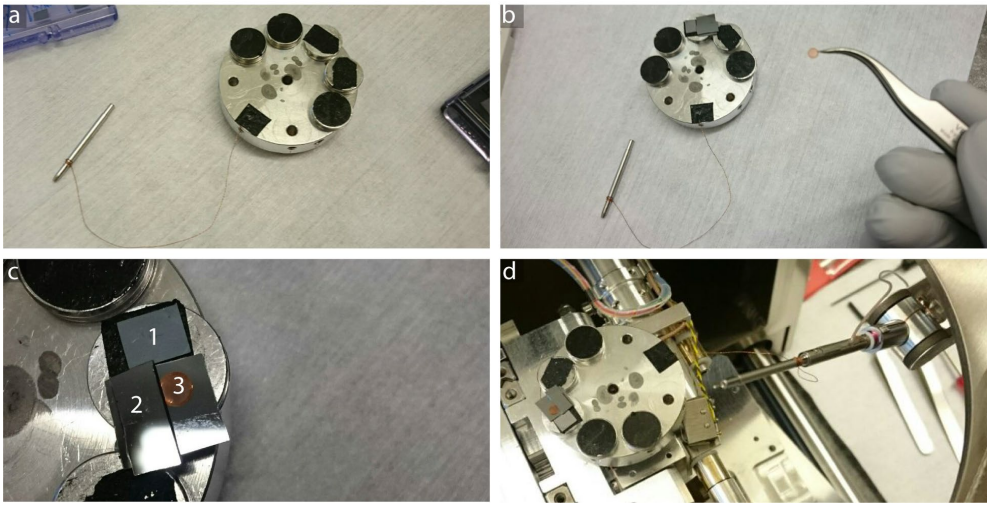


Figure 3.7 | System preparation for nanomanipulation
a: Manipulator end-piece connected to the holder with a copper wire for electrically grounding the system. **b**: chips mounted on the opposite side of the copper wire and a TEM-grid held by a tweezer. **c**: Zoom-in on the chips, with a growth substrate (1, upper) and TEM-grid carrier (2, lower) silicon chip. The TEM-grid (3) is mounted on the silicon with only its very edge sticking to a carbon sticker. **d**: Full assembly mounted back into the SEM and ready to be pumped down.

After venting the chamber, the holder and front part of the manipulator can be taken out. These two components need to be electrically shorted to have the same ground and avoiding a potential difference between manipulator and sample during transfer. This is important because without this, the electron beam of the SEM will charge the sample and manipulator tip differently and cause a potential difference. This can be observed by VLS nanowires bending towards the tip as the tip moves closer to the substrate during nanomanipulation, which will either cause the nanowires to stick to the tip making it impossible to deposit them elsewhere, or by burning/melting the nanowire due to the high current passing through them upon touching

the nanowires. It depends on the grounding of the sample what is more likely, but either way, it is undesirable. The shorting can be done by connecting the manipulator end to the holder with an insulation-free thin copper wire (Figure 3.7a). Make sure the wire is fixed on both ends (wrap it a few times around the manipulator end and fix it with a carbon sticker on the holder end). A few stubs can be mounted on the opposite side of where the copper wire is mounted, and the growth and deposition chip can be mounted on the stubs. Figure 3.7b shows the final setup, with the chips mounted opposite of the wire. The tweezer holds a fragile TEM-grid, consisting of a copper mesh covered with a very thin carbon films containing holes. In order to transfer nanowires to the TEM-grid, a special carrier chip is made to avoid the grid from sticking to carbon film, which would tear it apart when attempted to remove. Figure 3.7c is a zoom-in on the carrier chip, which is simply a 1x1 cm silicon chip with a small piece of carbon tape on one half, covered again by a 0.5x1 cm^2 silicon piece. The TEM-grid can be put on the flat non-sticking silicon and moved in between the two silicon pieces, such that the edge of the TEM-grid is slightly sticking to the carbon sticker avoiding any sliding during transfer. Finally, everything can be mounted into the SEM (Figure 3.7d) with the chips on the left side (as this side will tilt up later) and the front-end of the manipulator mounted back on the rest of the manipulator. Finally, the transfer tip, a tungsten tip on a tiny aluminium rod, needs to be mounted into the manipulator for the actual transferring.

After the SEM is pumped down, the stage can be tilted to 30 degrees, with the samples to the topside of the stage. The manipulator will then have plenty of space to move between the column and the stage. After turning on the extra high tension (EHT), move the manipulator to the sample and in the viewing field of the SEM. Slowly move the tip to the substrate until it just touches and then perform the standard aligning of the aperture, astigmatism, contrast, and brightness. This is done after the tip is in view because it will create significant distortions in the electron beam, making any prior adjustments useless. The system can now be used for transferring nanowires.

3.5 Transmission electron microscopy

Transmission electron microscopy or TEM is an electron-based imaging technique with sub-nanometre resolution.[10,11] It allows for the imaging of the atomic structure and defect analysis of crystal lattices. Nanowire samples can be imaged in the TEM by transferring them onto a TEM grid, a copper mesh with a punctured carbon film. Alternatively, they can be prepared by using focused ion beam (FIB, sputtering using gallium atoms) to cut out a slice of a sample (about 50-100 nm thick by several micron long). This is done with all the in-plane grown nanowires in Chapter 5 and Chapter 6. There are three main modes used for imaging: TEM mode, scanning TEM or STEM, and energy dispersive x-ray spectroscopy (EDX) mapping. Figure 3.8 shows a schematic overview of the main difference between TEM mode and STEM mode.

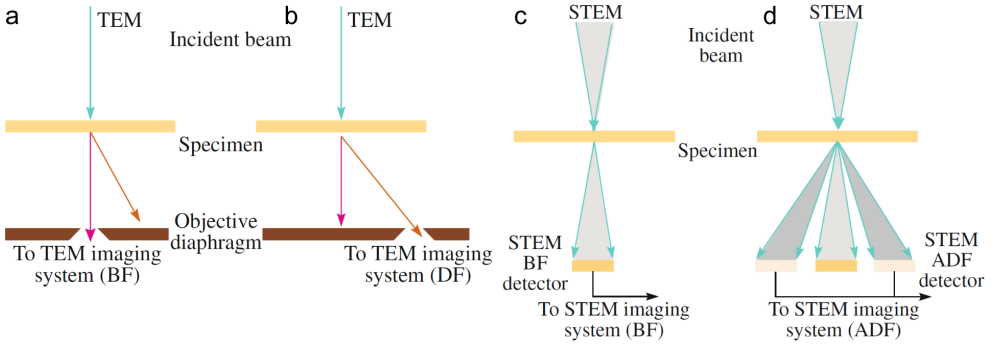


Figure 3.8 | Schematic overview of TEM and STEM mode
a,b: Schematic overview of transmission electron microscopy (TEM), in which a parallel beam of electrons hits the sample, an objective diaphragm filters the beam. Either the transmitted beam is passed through to the imaging system to form a bright field image (BF) (**a**), or a diffracted beam is passed, forming a dark field (DF) image (**b**).[10] **c,d**: Scanning transmission electron microscopy (STEM) overview.[12] Electrons are focused on the sample surface in a convergent beam. The electrons that pass through the sample can be collected by the bright field detector (BF) (**c**), the annular dark field detector (ADF) or the High-angle ADF (HAADF) detector (**d**).

In TEM mode, a parallel beam of electrons hits the specimen, travels through the atomic lattice and the resulting interference pattern is collected by a CCD detector. By using a small aperture in the focal plane of the objective lens (the objective aperture), the diffracted beams are blocked, and the transmitted beam will form a bright field image.[13]

In dark field mode, a specific diffraction spot (other than the transmitted beam) is chosen using the objective aperture, which will only highlight the regions in the sample contributing to this specific diffraction spot. This allows for the detection of a specific crystallographic orientation in the sample and can be used to detect crystal defects. Instead of creating a magnified image in TEM mode, also the back-focal plane can be projected onto the CCD camera, yielding an electron diffraction pattern (Figure 3.9). The periodicities in this reciprocal space image, as well as the angles between the various directions are characteristic for a specific crystal structure. Alternatively, images similar to the electron diffraction pattern can be obtained by creating a Fast Fourier Transform (FFT) of (a selected region of) an atomic resolution TEM image. The latter is used in this thesis to study the crystal structure and epitaxial relations. In STEM mode, the electron beam is focused on the sample in a convergent beam. The resulting signal is collected by multiple detectors: A bright field (BF) detector, an annular dark field (ADF) detector, and a high-angle annular dark field (HAADF) detector.

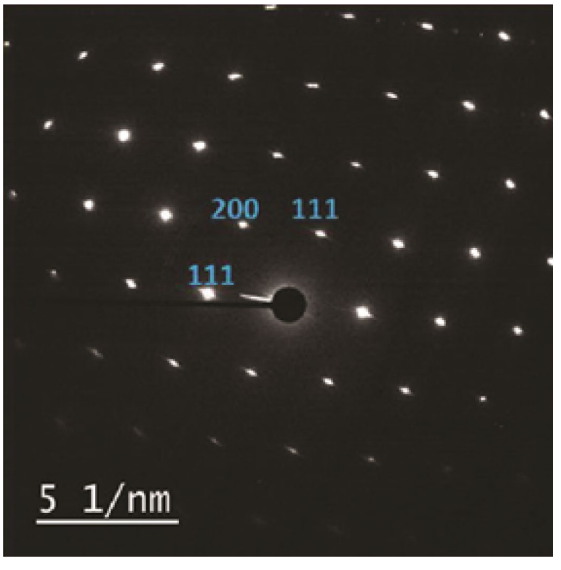


Figure 3.9 | Diffraction pattern
Typical example of a diffraction pattern from an InSb nanowire, with the direct beam spot in the middle and an array of diffraction spots around it. The symmetry of the pattern as well as the periodicities of this reciprocal lattice are key to uniquely identify the crystal phase and orientation. '111' and '200' represent the Miller indices hkl of the selected diffraction spots. Image source:[14]

The bright field detector captures the signal of the direct beam passing through the sample as can be seen in Figure 3.8b. In this case, thicker regions of the sample, or materials with a higher electron weight appear darker on the resulting image. Using the HAADF detector, which collects the electrons scattered to high angles, away from the diffraction scattering, leads to images where the atomic mass and material thickness define the contrast, with a higher brightness for heavier atoms.

Finally, energy-dispersive X-ray spectroscopy (EDX) mapping can be done on a sample to identify the elements present in different regions of the sample. Electrons travelling through the sample may eject electrons from an inner shell, thereby creating an electron-hole pair. An electron from a higher energy shell may then fill the hole, thereby emitting an X-ray photon with an energy characteristic for this transition. Each element has its own set of characteristic energies, leading to an energy spectrum with distinct peaks. These energy peaks can be attributed to different elemental materials and by combining the information extracted from this energy spectrum with the position the X-rays originated from in the sample, an EDX mapping is made, giving detailed information on the material composition of different regions of the sample.

3.6 References

1 *Nanolab@TUe*, <nanolabnl.nl/locations/eindhoven/> (2020).

2 Breiland, W. G. *et al.* Organometallic vapor phase epitaxy (OMVPE). *Materials Science and Engineering: R: Reports* **24**, 241-274, doi:10.1016/S0927-796X(98)00018-7 (1999).

3 Cho, A. Y. & Ballamy, W. C. GaAs planar technology by molecular beam epitaxy (MBE). **46**, 783-785, doi:10.1063/1.321645 (1975).

4 Cho, A. Y. Film Deposition by Molecular-Beam Techniques. **8**, S31-S38, doi:10.1116/1.1316387 (1971).

5 Panish, M. B. & Temkin, H. *Gas source molecular beam epitaxy*. (Springer-Verlag, 1993).

6 National Institute for Science and Technology, Gaithersburg, USA.

7 Goldstein, J. I. *et al. Scanning electron microscopy and x-ray microanalysis*. (Springer, 2018).

8 ZEISS. *Sigma ZEISS*, <zeiss.com/microscopy/int/products/scanning-electron-microscopes/sigma.html> (2020).

9 Kleindiek nanotechnik. MM3A-RoTip. (2020).

10 Williams, D. B. & Carter, C. B. *Transmission electron microscopy*. (Springer, 2009).

11 Gazibegovic, S. Bottom-up Grown InSb Nanowire Quantum Devices. *PhD Thesis* (2019).

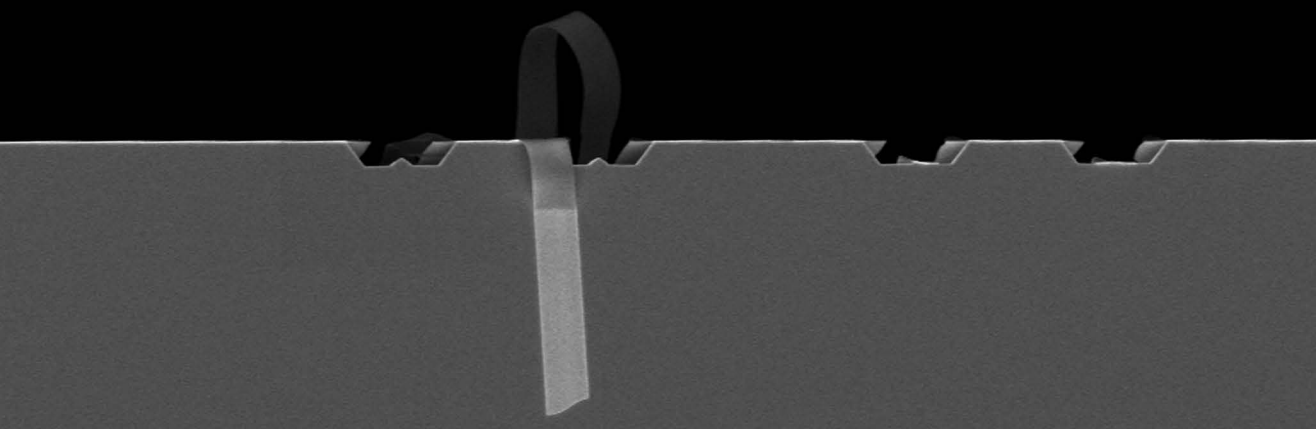
12 Wolf, S., Shimoni, E., Elbaum, M. & Houben, L. 33-60 (2018).

13 Edington, J. W. in *The Operation and Calibration of the Electron Microscope* 1-34 (Macmillan Education UK, 1974).

14 Gazibegovic, S. *et al.* Epitaxy of advanced nanowire quantum devices. *Nature* **548**, 434-438, doi:10.1038/nature23468 (2017).

Chapter 4

Out-of-plane InSb Nanowire Networks for Quantum Devices



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4.1. Introduction

InSb nanowires have been shown to be very promising candidates for topological quantum computing, due to their strong spin-orbit coupling, high electron mobility and large Landé g-factor.[1-5] These InSb nanowires were grown using bare InP (111)B substrates with an electron beam lithography patterned array of 8 nm thick gold droplets.[6] In order to achieve more complicated InSb nanowire networks using the VLS method, previously, InP stems were grown vertically on InP (100) substrates and then kinked to the <111>B direction by changing the growth parameters.[7] These stems are also necessary to ensure proper InSb nanowire growth (as described in Chapter 2.2.2.). Then, the InSb nanowires were grown on top along the <111>B direction. Although that did sometimes lead to InSb nano-crosses, the kinking would be left or right with a 50/50 percent chance, leading to a 25 percent chance of adjacent nanowires growing towards each other, drastically impacting the yield. Furthermore, more complex structures were not possible with this technique due to limitations in maximum growth time versus required minimum length.

To overcome these limitations, a new platform is designed to allow well controlled positioning and growth of the InSb nanowires enabling the formation of complex nanowire networks.[8] This new technique uses an InP(100) substrate that is selectively etched to form trenches with exposed and opposing {111}B facets. Nanowire growth orthogonal to these facets enables the preferred <111>B growth direction of the InSb VLS grown nanowires, which will allow the nanowires starting from opposing B facets to grow towards each other.[9] This process has been further developed to achieve a high level of control over the trench size, depth and gold droplet position leading to the creation of well-defined final InSb nanowire networks. Alternatively, nanowires can be used as shadowing objects by letting two or more nanowires from opposing facets cross but not merge, allowing for selective superconductor deposition from a directional material source.[8]

4.2. Substrate development

A schematic overview of the substrate processing is shown in Figure 4.1. An InP (100) substrate is covered with a SiO_x mask (Figure 4.1a) which is subsequently selectively etched using reactive ion etching to open the areas where the trenches will be formed later (Figure 4.1b). The trenches can be etched by using a liquid chemical etching method or a gas phase etching technique, both are discussed in more detail below. Both methods involve anisotropic etching, resulting in the exposure of {111}B side facets (Figure 4.1c) which are required for the <111>B growth of InSb VLS nanowires. The first mask is stripped (Figure 4.1d) and an amorphous 20 nm thick Si_xN_y mask is deposited to cover the entire substrate surface Figure 4.1e). Finally, holes are selectively etched in the mask using buffered HF on the sides of the trenches and an 8 nm thick gold layer is deposited in the openings of the mask using a standard lift-off process (Figure 4.1f). The final substrate will look as shown in Figure 4.1g, where the gold droplets are aligned to each other on opposing sides of different trenches. A more detailed processing recipe is described in Section 4.7.1.

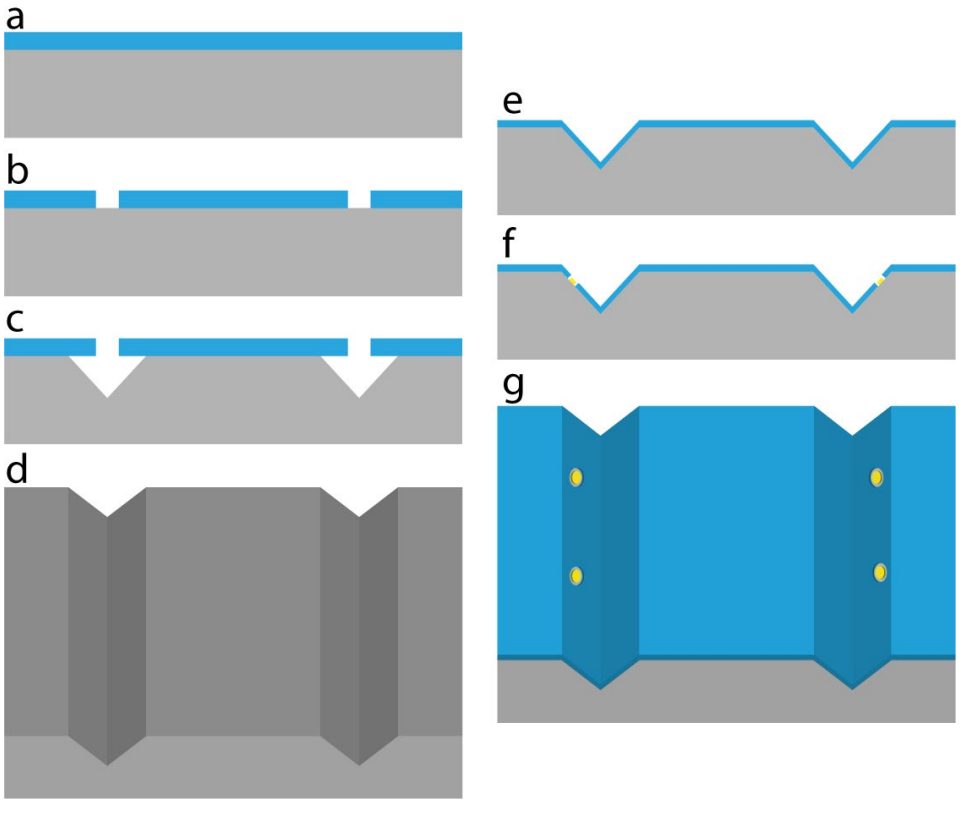


Figure 4.1 | Schematic overview of critical substrate processing steps
a: An InP (100) substrate (grey) is covered with a 50 nm thick SiO_x mask (light blue). **b**: The trench openings (around 200 nm wide) are etched into the mask using reactive ion etching. **c**: The trenches are etched through the openings of the mask exposing {111}B side facets. **d**: Perspective view of the substrate after mask removal. Trenches with {111}B facets on both sides are visible. **e**: A 20 nm thick Si_xN_y mask (light blue) is deposited on the substrate. **f**: Holes are etched in the mask using buffered HF and gold is deposited in the holes to form gold droplets that act as catalysts during InSb growth. **g**: Perspective view of a final substrate design with gold droplets on opposing sides in different trenches so nanowires can grow towards each other (see details in Section 4.7.1 and 4.7.2).

4.2.1. Trenches: wet chemical versus MOVPE etched

There are two main techniques to create InP (100) substrates with {111}B terminated trenches. The first technique is by using a liquid chemical solution to etch into the InP substrate. There are many etchants for InP reported in literature, allowing for the exposure of different specific crystal planes.[10-14] In this particular case, the use of hydrogen bromide (HBr) and phosphoric acid (H_3PO_4) in a specific ratio has been chosen to create {111}B terminated trenches.[10] **Figure 4.2** shows cross-section SEM images of a typical trench etched in an InP (100) substrate with a SiO_x mask on top and ~150 nm wide mask openings.

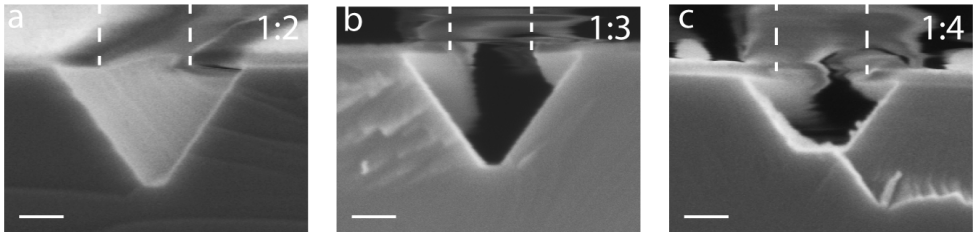


Figure 4.2 | Liquid chemical etching of trenches in InP (100) substrates
a-c: Cross-section scanning electron microscope images (SEM) of etched trenches using etchant solutions with different ratios of HBr to H3PO4 as noted in the top right of the image. The inclined {111}B side facets are visible in all cases and a horizontal {100} facet on the bottom of the trench is still well pronounced after using a more diluted etch **(c)**. In all three images, the mask opening width is around 150 nm (indicated by the white dashed lines) and the etching time is 10 seconds. Scale bars are 100 nm.

As can be seen in **Figure 4.2**, changing the ratio of the HBr to H_3PO_4 in the solution (indicated on the top-right of each image), the geometry of the trench is altered, and different terminating facets can be observed. In all cases, the inclined side facets are {111}B facets. A higher concentration of H_3PO_4, however, leads to a more pronounced formation of a horizontal {100} facet on the bottom of the trench. The etching time is 10 seconds for all three images, but the height of the trench decreases with increasing H_3PO_4 fraction, while the under-etching of the mask remains comparable (around 100 nm), indicating that the vertical etch rate of the (100) facet is slowed down, while the lateral etch rate of the {111}B facets remains similar. By keeping the HBr:H_3PO_4 ratio constant at 1:4 (as in **Figure 4.2c**) the time evolution of the etching can be investigated (**Figure 4.3**).

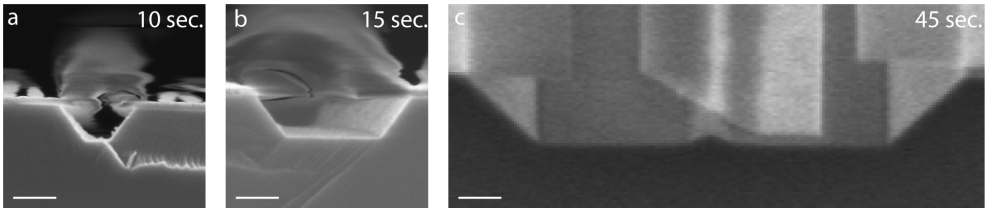


Figure 4.3 | Liquid chemical etching of InP (100) substrates as a function of time **a-c**: Scanning electron microscope (SEM) images showing the time evolution of wet-etched trenches in InP (100) substrates using a 1:4 HBr:H_3PO_4 solution. The mask openings are all around 150 nm and all scale bars are 200 nm. **a**: After 10 seconds of etching, the canal shape is formed with a horizontal {100} bottom plane. There is some etching under the mask and {111}B side facets are formed. **b**: The trenches continue to etch vertically as well as laterally, with faster lateral etching. **c**: After 45 seconds of etching, two neighbouring trenches are merging and the Si_xN_y mask has collapsed.

Figure 4.3 shows three cross-section SEM images of trenches etched into an InP (100) substrate with a 50 nm thick SiO_x mask on top and 150 nm wide openings in the mask. All three images have the same scale, making them directly comparable to one another. The etching times are noted in the top-right of each image and are 10, 15, and 45 seconds for Figure 4.3a, b, and c, respectively. The aimed width of the final trench was between 700 nm and 800 nm for geometrical reasons, while the etched widths of the trenches here are around 300 nm for Figure 4.3a, around 700 nm for Figure 4.3b and more than 900 nm for Figure 4.3c (because of the merging of the two trenches in Figure 4.3c, the precise width is hard to determine). Given that the liquid etching step is performed in a manual fashion, where a sample is clamped with a tweezer, and dipped into the solution for a set amount of time, the exact dimensions are very difficult to reproduce with such small timescales. One could argue that there are solutions to this, by diluting the solution with water, potentially slowing down the etch rate, reducing the etching temperature, or using some type of automated "dipping machine". Since control of the trench dimensions is crucial, we explore a more reliable and reproducible technique.

An alternative method to wet chemical etching is to use gas phase etching. It has been shown that hydrogen chloride (HCl) gas in a metal-organic vapor-phase epitaxy (MOVPE) tool can be used for etching InP.[15] For more information on the MOVPE tool see Chapter 3.1.

All pressures, valves, material flows, etc. are computer controlled in this machine, allowing for very precise and reproducible processing. For the trench etching experiments, an InP (100) substrate with a 50 nm thick SiO_x mask on top is used. Mask openings of around 200 nm wide and 50 µm long are etched using reactive ion etching. Before the sample is loaded into the MOVPE reactor, the sample is dipped in an H_3PO_4:H_2O 1:3 solution to remove the surface oxide from the InP surface in the mask openings. This will ensure a smoother etching of the trenches later on. Next, the sample is loaded in the reactor and a recipe is started. Here, the recipes all follow the same steps (see Section 4.7.1). The sample is heated up under a PH_3 overpressure of 60 sccm and the trenches are subsequently etched at a temperature of 635 ^{0}C with 20 sccm of PH_3 and 2 sccm of HCl. PH_3 is added as an overpressure gas to reduce the phosphorus desorption from the substrate, while the HCl reacts with the indium to form $InCl_3$. The results are shown in Figure 4.4, with the total etching time (i.e., HCl gas flow on) indicated in the top-right of each SEM image.

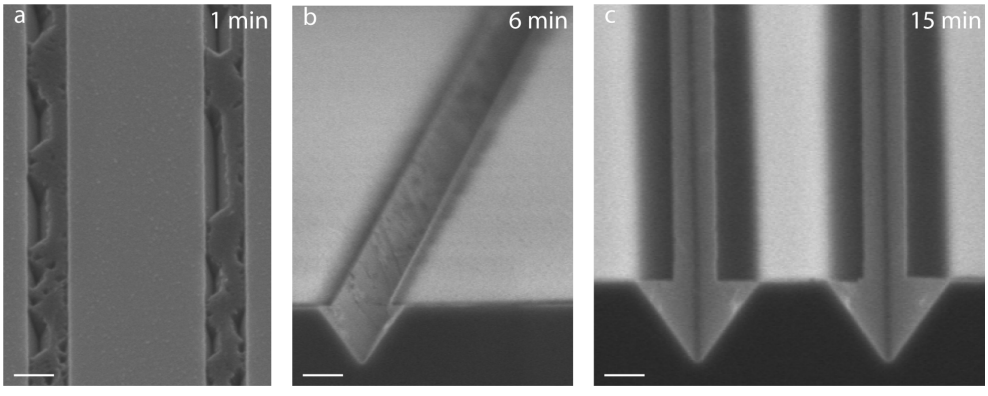


Figure 4.4 | Etching trenches in InP (100) substrates using HCl gas-phase etching in an MOVPE
An InP (100) substrate with a Si_xN_y mask is etched in a metal-organic vapor phase epitaxy (MOVPE) machine. Mask openings are around 200 nm and scale bars are 200 nm. **a**: After 1 minute of etching. small pit holes and segments are etched into the InP (100) substrate, immediately exposing {111}B side facets. **b**: After 6 minutes of etching the entire trench is etched into a V-groove, terminated by {111}B side facets. These facets still show some roughness. **c**: 15 minutes of etching the trenches shows very uniform and clean trenches with smooth {111}B side facets.

Figure 4.4a shows the result after 1 minute of HCl etching in the MOVPE. Nanometre sized pinholes and small segments of several hundred nanometres length are etched into the InP and these regions tend to already form stable {111}B facets indicating the strong selectivity of this etching method. In addition to the {111}B facets, the etch pits are terminated by smaller {110} facets in the length direction of the mask opening. After 6 minutes of etching (Figure 4.4b), the full V-shaped trench is etched, just slightly wider than the mask opening, and with well-defined {111}B terminating facets. These facets still exhibit some roughness and tiny spots, potentially indium droplets that are not yet etched away. After 15 minutes of etching (Figure 4.4c) the trenches are etched around 600 nm wide with very clean side facets. The etching time in Figure 4.4c is 2.5 times longer than in Figure 4.4b, while the trenches have etched only about twice as wide (from around 300 nm to around 600 nm), indicating the relatively slow etching rate of the {111}B facets in the trenches. This is advantageous, because it allows for very uniform and smooth etching of the stable 111B planes and a very precise control over the final width of the trenches.

After the trenches are etched, the SiO_x mask is removed and a 20 nm thick Si_xN_y layer is deposited uniformly over the new InP surface. Holes are etched into the mask using a buffered HF 7:1 solution at pre-defined positions using e-beam lithography and an 8 nm thick gold layer is deposited and by using a standard lift-off technique, gold droplets only remain in the mask openings. See Section 4.7.1 for more details. The positioning of the gold droplets on the trench side facets is very sensitive to the actual width and position of the trench. If the trenches are being etched wider than designed, the droplets are positioned too deep into the trench and the resulting nanowire will end up hitting the opposite side of the trench during growth. If the trench is etched too little, the gold droplet might be positioned partially on the edge of the trench or even on the top (100) surface. This would result in the nanowire crawling or growing randomly in the left or right inclined <111>B direction (50/50 chance). Hence, the etched width of the trenches is critical for the final positioning of the gold droplets. By using MOVPE etching with HCl gas, the final width of the trench can be controlled up to 50 nanometres accurate. Another factor that influences the accuracy in droplet positioning is the accuracy in alignment of the mask openings for the trenches to the crystal direction of the substrate. The

alignment part is a manual process using the large wafer-flat to position the wafer markers. Empirical data has shown that this can be done within 0.3 degrees accuracy. This can become more obvious on long trenches (> 100 µm) since the etching follows the crystal direction, leading to a larger lateral offset between mask opening and trench for longer trenches.

4.3. InSb nanowire growth

A number of envisioned transport experiments require InSb nanowire networks with different geometries and shadow configurations. For instance, a Majorana interference device requires a loop with a superconducting island on one of its arms. Different geometries can be realized by tuning the design of the substrate; the trench dimensions and the Au-particle position. Figure 4.5 shows the different general steps in the process of creating the final InSb nanostructure.

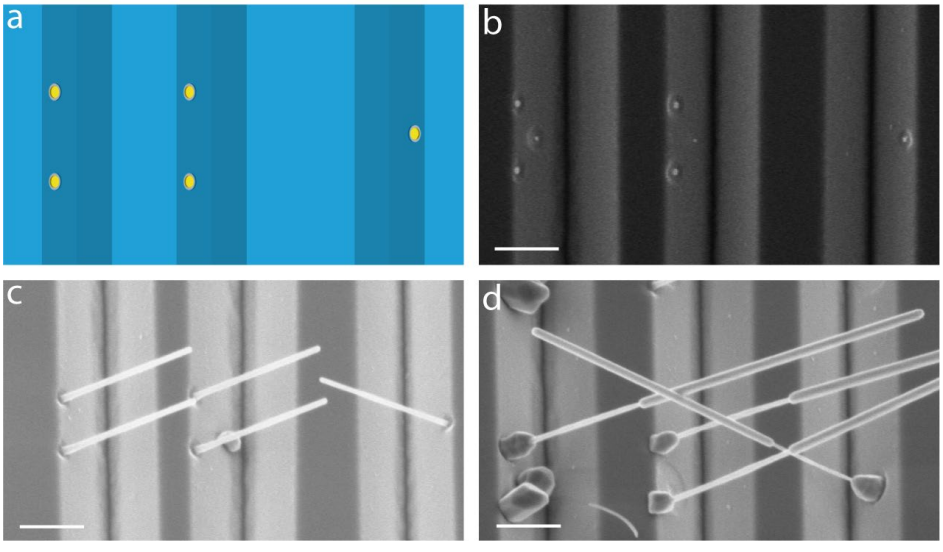


Figure 4.5 | Steps in the creation of InSb nanowires on trenches
a: Schematic overview of an InP (100) substrate covered by a SixNy mask (light blue). The trenches (darker blue) contain gold droplets (yellow) in small mask openings. **b**: Scanning electron microscope (SEM) image showing the gold dots positioned on the sides of the trenches. **c**: InP stems are grown from the gold catalysts using a metal-organic vapor phase epitaxy (MOVPE) machine. **d**: InSb nanowires are subsequently grown on top of the InP stems using the same MOVPE technique. All scale bars are 500 nm.

First a design is made as shown in Figure 4.5a, where the darker blue regions are the trenches. The gold droplets (yellow) are generally positioned on opposing sides of the trenches such that the nanowires will grow towards each other, as their preferred growth direction is a <111>B direction, i.e. orthogonal to the trench wall. In this two-by-two-by-one design example, the idea is that two sets of nanowires on the left side will act as shadowing objects for the nanowire growing from the right side. Shadow deposition is discussed later in this chapter. The representative substrate after all the processing is shown in Figure 4.5b, showing a top-view SEM image with three trenches (lighter grey) and the gold droplets. Next, InP stems are grown from these gold droplets (see Figure 4.5c) to a length of about 1.5 µm and subsequently the InSb nanowires are grown on top (see Figure 4.5d).

A critical parameter in the design of these substrates is the offset between the nanowires on the left and the right side, as shown in the schematic in Figure 4.6a, indicated by the white and the black dashed line.

When the offset is larger than the diameter of the InSb nanowire, the two opposing nanowires miss and grow past each other as seen in the SEM image in Figure 4.6b. This design can be used for shadow deposition of metal contacts on the nanowires by loading the grown substrate into a molecular beam epitaxy machine, where a directional beam of material can be deposited under any specified inclined angle.

If the offset between the gold droplets is just within the diameter of the nanowire (as in Figure 4.6c), the InSb nanowires can grow towards each other and merge at the crossing, forming a nano-cross as shown in the SEM image in Figure 4.6d. By adding more gold droplets on specific position in the design, this will allow for the formation of nanowire networks with multiple junctions.

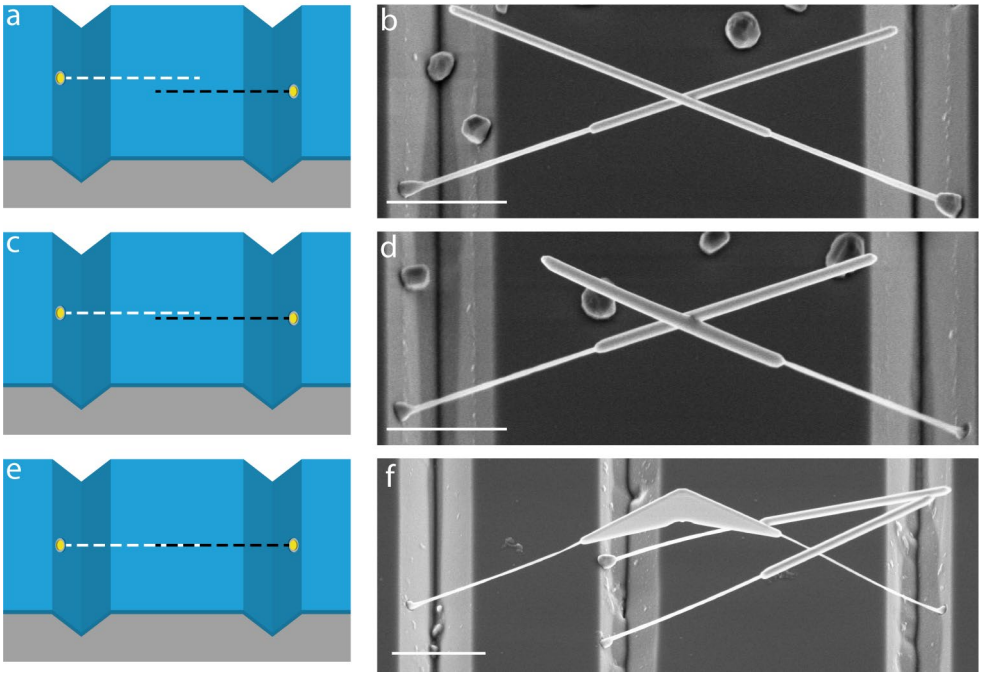


Figure 4.6 | Importance of gold droplet offset for resulting InSb nanowire structure
The offset of two opposing gold droplets is indicated with the white and black dashed line. **a**: The offset is larger than the expected nanowire diameter. **b**: Scanning electron microscope image (SEM) of the final growth result of **(a)**. InP stems are grown from the gold droplets and InSb nanowires are then grown on top of the stems. Here, the nanowires grow past each other and just miss each other. **c**: The offset between the opposing gold droplets is slightly less than the expected nanowire diameter. **d**: Result of an offset as shown in **(c)**. The InSb nanowires continue to grow past each other but start merging at the junction due to lateral overgrowth. **e**: There is no offset between the gold droplets. **f**: As a result of no offset between the droplets, the two gold droplets meet during growth and the InSb starts forming a nanoflake. All scale bars are 1 µm.

With no offset between the droplets (Figure 4.6e), the nanowires, while growing towards each other, will meet and merge. A nanoflake will start forming by vapor-solid (VS) growth on the inside corner of the junction (Figure 4.6f). A common problem when growing InSb layers for 2-dimensional electron gas (2DEG) experiments is the large lattice mismatch between InSb and other III-V semiconductors, making high quality strain-free 2D InSb difficult to achieve. The nanoflakes grown with the new platform shown here can overcome this issue. There are

also other ways to grow InSb 2D nanoflakes, for example by homoepitaxy on InSb substrates.[16] To use these InSb structures as a basis for quantum devices, the creation of hybrid heterostructures and the growth of networks are critical. These two parts will be discussed in more detail.

4.4. Semiconductor-superconductor hybrids

In Sb nanowires have been used in the past in combination with NbTiN as a superconducting layer to show the first signatures of Majorana zero modes.[1] The nanowires were deposited on a transport chip and the superconducting contacts were lithographically defined, after which the nanowire surface was etched to remove surface oxides before evaporation of the superconducting contact. This methodology caused a rough interface between the semiconductor and the superconductor. To reduce surface states, and improve the quality of semi-/superconductor interface, the trenches platform can be used to perform in-situ directional deposition of superconductors by using MBE (see Chapter 3.2), allowing for higher quality and more complicated hybrid structures for topological quantum experiments. An example of such a structure is based on the principle of shadow deposition of superconductors on wires grown with an offset (Figure 4.6a). After the InSb nanostructures are grown on a trenches substrate with an offset between opposing nanowires as shown in Figure 4.6a and Figure 4.6b, the sample is taken from the MOVPE, mounted on a holder, and loaded into a molecular beam epitaxy (MBE) machine. The sample is degassed and then hydrogen cleaned to gently remove any surface oxides from the nanowire side facets. Next, the holder is loaded into a small MBE chamber on a manipulator that is cooled down to -166 ^{0}C by using liquid nitrogen. The low temperature on the manipulator is crucial during the aluminium deposition to ensure a smooth layer. At higher temperatures, the aluminium atoms are more mobile and diffuse over the nanowire surface, forming separate islands. The aluminium is evaporated along the direction of the trench at an angle between 25 and 45 degrees to the normal of the substrate, with a deposition rate of 5.5 Å/min, creating a 10 nm thick layer. Finally, the sample is moved to the load lock and exposed to an O_2/N_2 20/80 percent mixture for 10 minutes, to create a self-terminating AlOx shell around the Al.[8] Several nanowires from a design like in Figure 4.6a and Figure 4.6b are transferred to a TEM-grid

to analyse in a transmission electron microscope (TEM). The results are shown in Figure 4.7.

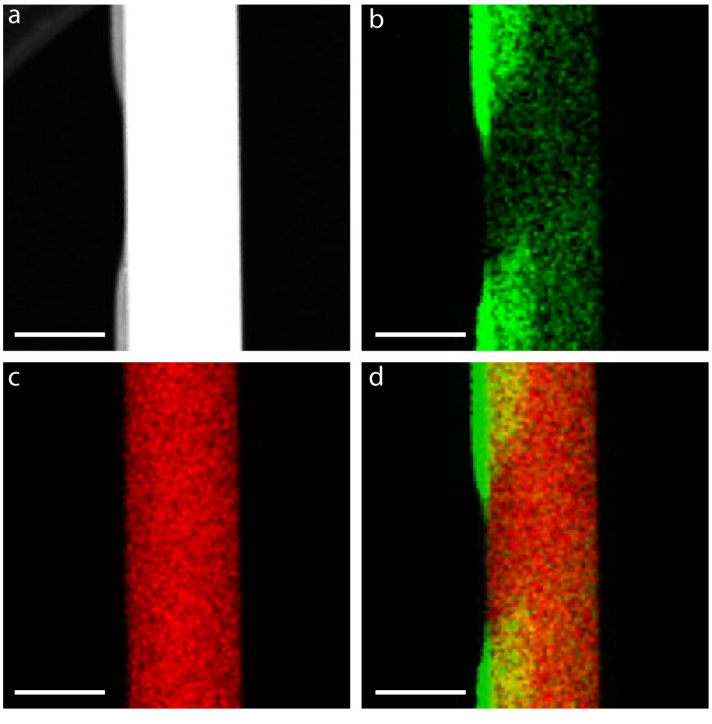


Figure 4.7 | Transmission electron microscope analysis of a shadowed InSb nanowire
a: High-angle annular dark field scanning transmission electron microscopy (HAADF STEM) image of an InSb nanowire (white) with a shadowed 10 nm thick aluminium layer (light grey on the left of the wire). **b**: Energy dispersive x-ray spectroscopy (EDX) elemental mapping of the aluminium layer (green) deposited on the nanowire with a well-defined shadow region visible. **c**: elemental mapping of the indium content in the nanowire. **d**: overlay of **(b)** and **(c)**, showing the aluminium on the left side of the nanowire. All scale bars are 100 nm.

The HAADF STEM image in combination with the EDX data in Figure 4.7 shows the Al-InSb nanowire with a metallic aluminium layer on the left side of the nanowire and an inclined shadow region. This inclination is the result of the 107 degree angle between two <111>B grown InSb nanowires. The EDX results show that the shadowed area is free from any aluminium and the width of about 100 nm can be attributed to the diameter of the InSb nanowire that was used as the shadow object.

The result of a more complicated design, with two shadowing wires in front of a nanowire can be seen in Figure 4.8, resulting in three distinctive islands of aluminium on the nanowire, which can be used to perform superconducting island experiments.

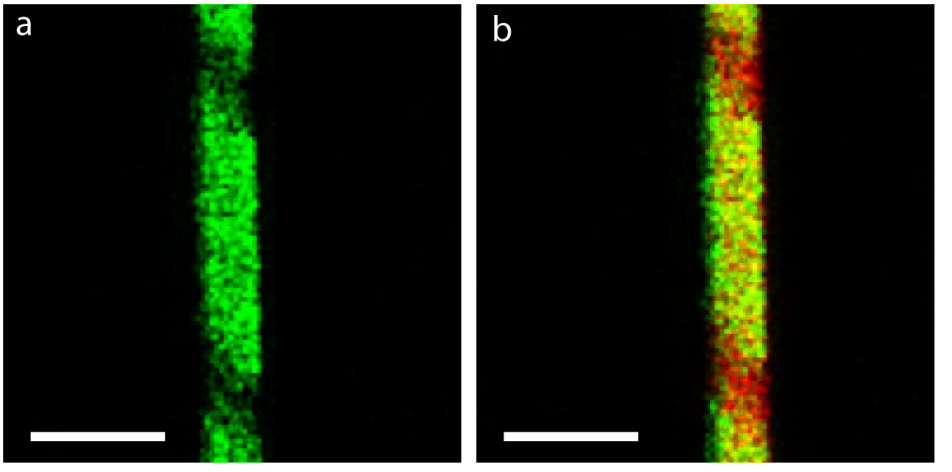


Figure 4.8 | Energy dispersive x-ray spectroscopy of a double shadowed InSb nanowire
a: Energy dispersive x-ray spectroscopy (EDX) element mapping of the aluminium deposited on an InSb nanowire, with two well-defined shadow regions. **b**: Overlay of the elemental mappings of the aluminium layer and the indium of the nanowire. Scale bars are 300 nm.

The interface quality between the InSb nanowire and aluminium layer can be visualized using high-resolution transmission electron microscopy (HRTEM). Figure 4.9 shows a side-view image with the InSb-Al-AlOx stack (left-to-right) with the rows of InSb atoms clearly visible. The aluminium layer is formed from crystal grains with different orientations. In this example the grain on the top of the image is within the same zone-axis as the nanowire, revealing the crystal planes of the grain, indicating an epitaxial relation between the nanowire and the aluminium with an oxide-free interface and no interface roughness. The AlOx is an amorphous layer that passivates the aluminium and prevents it from further oxidation.

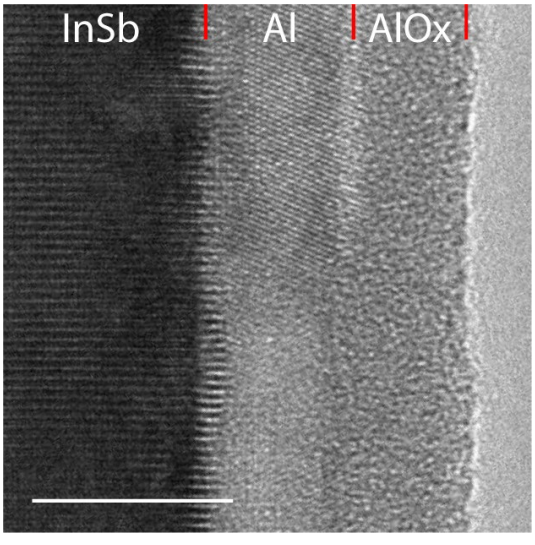


Figure 4.9 | TEM image of an InSb nanowire with epitaxial aluminium
High resolution transmission electron microscopy image (HRTEM) of an InSb nanowire with a 5-nanometre thick epitaxial aluminium layer on top. The aluminium is passivated by oxidation of the aluminium at low temperatures, forming a self-terminating AlOx layer. Scale bar is 5 nanometres.

4.5. Scalability

In an effort to make larger InSb nanowire networks, several complications are inherent to the method described in Section 4.2. First, there is a minimum distance required between the trenches to avoid them from merging during the trench etch step, implying a minimum distance between consecutive nanowires in a larger network. Second, the InP stems evaporate during the subsequent growth of the InSb nanowires due to the higher growth temperature required for InSb growth, which limits the maximum growth time for the nanowires and therefore inherently limits the size of the nanowire network.

By growing thicker and shorter InP stems of around 200 nanometres, the evaporation of the stems can be slowed down, allowing for the largest VLS grown InSb nanowire network to date, a three-by-three network as depicted in the SEM image in Figure 4.10. This is large enough for developing a single qubit device, which would require at least a two-by-three nanowire network.

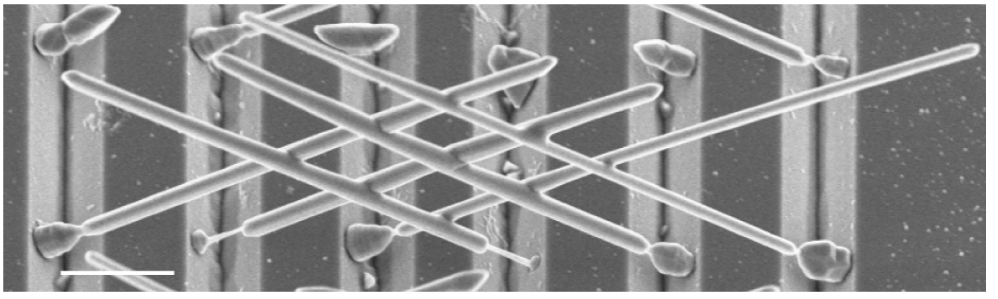


Figure 4.10 | Three by Three InSb nanowire network
Scanning electron microscope image of a three by three InSb nanowire network, showing the most complicated InSb nanowire network to date based on the vapor-liquid-solid (VLS) method. Scale bar is 1 µm.

Although this technique provides the highest quality InSb nanowires to date, it is not a scalable technique. The yield of these structures is unfortunately very low, since with every nanowire added to the structure, the probability of every nanowire growing and every junction merging properly is decreased. The maximum size of the network is also limited because of the evaporation of the InP stems. Even if there is a solution to this (for example begin able to grow without stems), the junction that merges first would grow thicker than the junction that merges last. In a larger network, this can become more apparent and loose the 1-dimensional confinement locally. Perhaps the biggest drawback is that every structure needs to be manually selected, picked up and deposited on a device substrate before any meaningful experiments can be done, making this a non-scalable process.

4.6. Conclusion

VLS grown InSb nanowires are promising candidates for topological quantum computational devices. This requires more than just single nanowires. The growth of networks can be achieved by using trenched InP (100) substrates. These trenches can be etched using HCl gas phase etching using an MOVPE reactor. This allows for precise control of the trench width, and thus the positioning of the gold droplets. This platform can be used to shadow deposit aluminium superconductor on the nanowires with clean and high-quality junctions, which have shown the first hard superconducting gap in InSb nanowires. Networks can be made by growing nanowires from different trenches towards each other and let them merge, which was

achieved up to three by three nanowires, but with a very low yield, making this platform unsuitable for scalable quantum devices.

4.7. Appendix

4.7.1. Substrate processing

An InP (100) undoped 2-inch single-side polished wafer is used as the substrate for developing trenches. The process consists of three parts: making etched markers, creating the trenches, and deposition of the gold droplets.

Marker etching

- Mask: A Si_xN_y mask of around 100 nm is deposited using plasma enhanced chemical vapor deposition (PECVD, Oxford Instruments PlasmaLab system 100).
- Resist: A layer of ZEP520A resist is spun at 2700 RPM for 60 seconds and consecutively baked starting at 100 ^{0}C, linearly increased to 200 ^{0}C over a 15-minute period.
- Lithography: Markers of 20 by 20 μm^2 are exposed using an electron beam lithography (EBL) tool (Raith EBPG5150).
- Developing resist: Dip the wafer in n-amylacetate for 1 minute, then rinse in a Methyl-iso-butylketon: isopropanol (MIBK:IPA 89:11) mixture for 45 seconds, and finally a rinse in IPA for 1 minute. Blow-dry with N_2.
- Mask etching: Etching Si_xN_y using reactive ion etching with a CHF_3:O_2 mixture for 1 minute 15 seconds (Oxford Instruments PlasmaLab system 100 RIE).
- Remove resist: oxygen plasma clean with an Oxford instruments PlasmaLab system 100 (RIE), 15 mT, 50W, 20 sccm O_2, 5 minutes.
- Etch markers into substrate: inductively coupled plasma etch (ICP) with an Oxford Instruments PlasmaLab system 100 modular cluster system ICP 180, in an etch/descum cycling fashion for 30 cycles. Parameters: *Etch*: t: 60s, T = 60 °C, p= 6 mtorr, RF substrate bias power: 110 W, ICP: 200 W, CH_4: 30 sccm, H_2: 10 sccm; *Descum* t: 16 s, T = 60 °C, p = 18 mtorr, RF: 110 W, ICP: 200 W, O_2: 40 sccm.
- Cleaning after ICP etch: oxygen plasma clean with an Oxford instruments PlasmaLab system 100 (RIE), 15 mT, 50 W, 20 sccm O_2, 5 minutes.

Trenches

- Remove mask: Dip wafer in buffered HF 7:1 for 3 minutes to remove the Si_xN_y mask from the markers step. Water rinse until bath resistance is > 9 MΩ. Blow-dry with N_2.
- Surface treatment: Dip wafer in H_2O:H_3PO_4 10:1 for 3 minutes, rinse in water (water resistance > 8 MΩ). Blow-dry with N_2.
- Mask deposition: Deposit 20 nm of SiO_x using PECVD (Oxford instruments PlasmaLab system 100), time: 41 seconds.
- Resist: Spin ZEP520A at 5000 RPM for 30 seconds, then bake for 15 minutes from 125 ^{0}C to 200 ^{0}C.
- Lithography: Write trenches using EBL (Raith EBPG5150).
- Develop resist: 1 minute n-amyl acetate, 45 seconds Methyl-iso-butylketon: isopropanol (MIBK:IPA 89:11), 1 minute isopropanol, blow-dry with N_2.
- Etch mask: reactive ion etching using pure CHF_3 for 3 minutes 30 seconds.
- Resist removal: Oxygen plasma treatment with Oxford instruments PlasmaLab system 100 (RIE), 15 mT, 50W, 20 sccm O_2, 5 minutes.
- Surface treatment: Dip wafer in H_2O:H_3PO_4 10:1 for 3 minutes, rinse in water (water resistance > 8 MΩ). Blow-dry with N_2.
- Etch the trenches: Load wafer in MOVPE, run recipe. Heat-up and anneal sample at 650 ^{0}C for 10 minutes, PH_3 flow 55 sccm. Cooldown to 635 ^{0}C for etching. Etch for 5 minutes 30 seconds with PH_3 flow 20 sccm and HCl flow 2 sccm. The final etching time depends on the designed and desired trench width. Cool down under PH_3 flow 55 sccm.

Gold dots

- Mask removal: BHF 7:1 for 3 minutes, water rinse (> 8 MΩ resistance), blow-dry with N_2.
- Surface treatment: H_2O:H_3PO_4 10:1 for 3 minutes, water rinse (> 8 MΩ resistance), blow-dry with N_2.
- Mask: 10 nm Si_xN_y deposition (42 seconds) using PECVD (Oxford Instruments PlasmaLab system 100).
- Resist: Spin adhesion promoter AR 300-80 at 4000 RPM for 60 seconds, bake at 180 ^{0}C for 2 minutes. Spin resist CSAR AR-P 6200.04 at 4000 RPM for 60 seconds, bake at 150 ^{0}C for 2 minutes.

- Lithography: Write dots on sides of trenches using EBL (Raith EBPG5150).
- Develop: CSAR developer AR 600-546 for 1 minute followed by isopropanol rinse for 1 minute.
- Etch mask: etch Si_xN_y mask for 16 seconds using BHF 7:1, rinse with water (> 8 MΩ resistance), blow-dry with N_2.
- Gold deposition: Evaporate 8 nm of gold using e-beam evaporation at 1 Å/s.
- Lift-off: lift-off using PRS3000 overnight (>8 hours). Rinse in isopropanol. Blow-dry with N_2.

4.7.2. Nanowire growth

After the substrate processing is complete, the nanowires can be grown using MOVPE. This consists of two parts: growth of the InP stems and growth of the InSb nanowires. The general growth scheme is the same for both steps.

The InP stems are grown by loading the sample into the MOVPE reactor, heating up to 510 ^{0}C and anneal for 5 minutes under 55 sccm of PH_3. The reactor is then cooled to 450 ^{0}C and InP stems are grown for 14 minutes with flows of TMIn 8 sccm, PH_3 36 sccm and HCl 5.6 sccm. The sample is cooled down under 55 sccm of PH_3.

InSb nanowires are grown with the following recipe: Heat up to 495 ^{0}C under AsH_3 26 sccm. Turn off AsH_3 and turn on TMIn at 30 sccm for 30 seconds. Turn off TMIn for 2 minutes. Grow InSb at 495 ^{0}C with TMIn flow 30 sccm, TMSb flow 8.3 sccm for 32 minutes. Cool down under TMSb flow 30 sccm.

4.7.3. Superconductor deposition

When the nanowires are grown, the samples are mounted on a tantalum holder using gallium as bonding agent. The samples are loaded into the MBE system and degassed at 350 ^{0}C for 2 hours. Next, the sample is loaded into an MBE chamber for hydrogen cleaning. Hydrogen cleaning is done at 400 ^{0}C for 20 minutes at a chamber pressure of 1.5 x 10^{-5} mbar and a H_2 flow of 20 sccm under continuous rotation of a downward facing sample. The holder is cooled in the chamber until the pressure is in the 10^{-9} mbar range and the holder temperature is below 120 ^{0}C. The holder is unloaded to the transfer tube

and cooled down to room temperature. For the metal deposition, the sample holder is loaded into the MBE chamber on a manipulator that is cooled using liquid nitrogen (LN_2). The holder is cooled for 2 hours to reach a temperature of -165 ^{0}C. The aluminum cell is heated up to 1040 ^{0}C to reach a deposition rate of 5.5 Å/min and a 15 nm thick layer of Al is deposited. After deposition, the sample is transferred to the MBE load lock as soon as possible (generally under 10 minutes) and exposed to an O_2:N_2 2:8 mixture for 10 minutes at a pressure in the 10^{-3} mbar range. Finally, the sample is warmed up to room temperature before unloading.

4.8. References

1 Mourik, V. *et al.* Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices. *Science* **336**, 1003-1007, doi:10.1126/science.1222360 (2012).

2 Poerschke, R. & Madelung, O. Semiconductors Group IV Elements and III-V Compounds. *Data in Science Technology*, 124 (1991).

3 van Weperen, I. *et al.* Spin-orbit interaction in InSb nanowires. *Physical Review B* **91**, 201413, doi:10.1103/PhysRevB.91.201413 (2015).

4 Vurgaftman, I., Meyer, J. R. & Ram-Mohan, L. R. Band parameters for III–V compound semiconductors and their alloys. *Journal of Applied Physics* **89**, 5815-5875, doi:10.1063/1.1368156 (2001).

5 Bommer, J. D. S. *et al.* Spin-Orbit Protection of Induced Superconductivity in Majorana Nanowires. *Arxiv:1807.01940v1* (2018).

6 Plissard, S. R. *et al.* From InSb Nanowires to Nanocubes: Looking for the Sweet Spot. *Nano Letters* **12**, 1794-1798, doi:10.1021/nl203846g (2012).

7 Car, D., Wang, J., Verheijen, M. A., Bakkers, E. P. A. M. & Plissard, S. R. Rationally Designed Single-Crystalline Nanowire Networks. *Advanced Materials* **26**, 4875-4879, doi:10.1002/adma.201400924 (2014).

8 Gazibegovic, S. *et al.* Epitaxy of advanced nanowire quantum devices. *Nature* **548**, 434-438, doi:10.1038/nature23468 (2017).

9 Dalacu, D., Kam, A., Austing, D. G. & Poole, P. J. Droplet Dynamics in Controlled InAs Nanowire Interconnections. *Nano Letters* **13**, 2676-2681, doi:10.1021/nl400820w (2013).

10 Adachi, S. Chemical Etching Characteristics of (001)InP. *Journal of The Electrochemical Society* **128**, 1342, doi:10.1149/1.2127633 (1981).

11 Adachi, S. Chemical Etching of InGaAsP/InP DH Wafer. *Journal of The Electrochemical Society* **129**, 1053, doi:10.1149/1.2124014 (1982).

12 Huo, D. T. C., Wynn, J. D., Napholtz, S. G. & Wilt, D. P. Controlled Undercutting of V-Groove Channels for InP by Photoresist Etch Mask. *Journal of The Electrochemical Society* **135**, 1231-1234, doi:10.1149/1.2095935 (2019).

13 Kappelt, M. & Bimberg, D. Wet Chemical Etching of High Quality V-Grooves with {111} A Sidewalls on (001) InP. *Journal of The Electrochemical Society* **143**, 3271-3273, doi:10.1149/1.1837196 (2019).

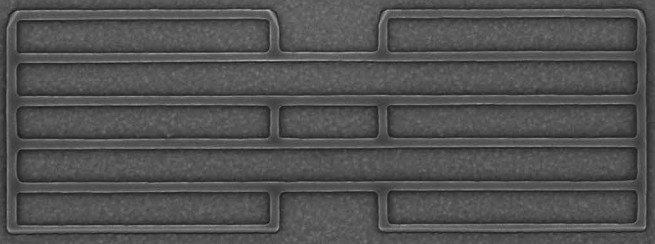
14 Wang, J. Wet Chemical Etching for V-grooves into InP Substrates. *Journal of The Electrochemical Society* **145**, 2931, doi:10.1149/1.1838739 (1998).

15 Caneau, C., Bhat, R., Koza, M., Hayes, J. R. & Esagui, R. Etching of InP by HCl in an OMVPE reactor. *Journal of Crystal Growth* **107**, 203-208, doi:10.1016/0022-0248(91)90457-G (1991).

16 Gazibegovic, S. *et al.* Bottom-Up Grown 2D InSb Nanostructures. *Advanced Materials* **31**, 1808181, doi:10.1002/adma.201808181 (2019).

Chapter 5

In-plane Selective Area InSb-Al Nanowire Quantum Networks



Based on Roy L.M. Op het Veld, Di Xu et al., In-plane selective area InSb–Al nanowire quantum networks, Nature comm. phys., 2020, 3, 59. Raw data on https://zenodo.org/record/4589484

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Transmission electron microscopy: Marcel A. Verheijen; TU/e and Eurofins Material Science, Eindhoven, Netherlands

Quantum transport: Di Xu and Hao Zhang; TU-delft

Abstract

Strong spin-orbit semiconductor nanowires coupled to a superconductor are predicted to host Majorana zero modes. Exchange (braiding) operations of Majorana modes form the logical gates of a topological quantum computer and require a network of nanowires. Here, we utilize an in-plane selective-area growth technique for InSb-Al semiconductor-superconductor nanowire networks. Transport channels, free from extended defects, in InSb nanowire networks are realized on insulating, but heavily mismatched InP (111)B substrates by full relaxation of the lattice mismatch at the nanowire/substrate interface and nucleation of a complete network from a single nucleation site by optimizing the surface diffusion length of the adatoms. Essential quantum transport phenomena for topological quantum computing are demonstrated in these structures including phase coherence lengths exceeding several micrometres with Aharonov-Bohm oscillations up to five harmonics and a hard superconducting gap accompanied by 2*e*-periodic Coulomb oscillations with an Al-based Cooper pair island integrated in the nanowire network.

5.1. Introduction

Indium-antimonide (InSb) and indium-arsenide (InAs) nanowires are promising candidates for realizing Majorana-based topological quantum computers.[1] InSb, in particular, is interesting for its high electron mobility, strong spin-orbit coupling and large Landé g-factor.[2-5] Over the past years, extensive efforts have been made to improve the quality of InSb nanowires, grown by the vapor-liquid-solid (VLS) mechanism.[6,7] A major achievement is the clean and epitaxial semiconductor-superconductor interface relying on *in-situ* metal evaporation and complex substrate processing.[8,9] This has been critical for showing the first quantized conductance of Majorana zero-modes, a milestone towards braiding experiments.[10] To braid these Majorana states, scalable nanowire networks with a high degree of interconnectivity are required.[11] Recently, out-of-plane growth of InSb nanowire networks has been demonstrated by merging multiple wires during VLS growth. Phase-coherent and ballistic transport have been observed, demonstrating the high quality of these network structures.[8,12] This technique, however, requires predefined positioning of the nanowires with nanometre accuracy in order to form networks, leading

to a drastic decrease in yield with increasing network complexity. Moreover, merging of VLS nanowires inevitably forms a widening of the nanowire diameter at and around the junction with a 75% chance of a defect forming at the junction, which negatively affects the one-dimensionality of the system.[8]

A more scalable approach, would be to use an in-plane selective-area growth (SAG) technique (i.e. parallel to the substrate surface), that relies on a template or mask to selectively grow one semiconductor material on top of another.[13-19] This technique has several advantages over out-of-plane growth. First, the flexibility of network designs is significantly enhanced, as the preferred design can be written and etched directly into a mask enabling complex structures. Second, the growth can be confined within the mask, keeping the entire structure one-dimensional with an easily controllable and constant cross-section size. Finally, the technique excels in scalability, readily allowing for the growth of complex structures suggested for Majorana braiding experiments in a variety of theoretical proposals.[11,20,21] The large lattice mismatch between InSb and any other III-V semiconductor substrate material,[22] however, poses an important challenge making it difficult to grow defect-free InSb nanowires on large-bandgap or insulating substrates. Furthermore, the disorder created by the lattice mismatch can be detrimental to the topological protection of Majorana states.[23] Most of the previous SAG studies have focused on an InAs-based material system for nanowire networks,[14-17,19] which has a smaller lattice mismatch with InP or GaAs substrates. InSb nanowires have been grown by SAG using molecular beam epitaxy (MBE).[18,24] Here, we demonstrate an in-plane SAG technique for scalable and high quality InSb nanowire networks, which shows all the relevant quantum transport properties (e.g. long coherence length and excellent induced superconducting properties) necessary for topological qubits.

5.2. Growth of in-plane Selective Area InSb networks

In this study we use InP as a substrate because it has a type I band alignment with InSb and becomes semi-insulating at low temperatures (see Figure 2.5). The large band gap of 1.34 eV compared to 0.17 eV of InSb ensures good confinement.[25] The lattice mismatch between these materials is 10.4 %, making large scale defect-free growth of InSb a challenge.[26] It is important to have defect-free single-crystalline material to obtain a high carrier mobility by reducing electron scattering.[27] On a (100) substrate, many stacking faults are expected to form inclined to the substrate (along the {111} planes) to relax the lattice strain.[13] To avoid the formation of these inclined defects, we use InP (111)B as growth substrate. We will show that strain from the lattice mismatch is relieved directly at the substrate/nanowire interface. Moreover, atomically flat twin planes can form parallel to the substrate, above which the nanowires grow without extended defects, separating the mismatch-induced disorder from the nanowire top part. On a (111)B substrate, growth nuclei with an odd and even number of horizontal twins will have a 180°-rotated crystallographic orientation with respect to each other. When these nuclei merge by lateral growth, an inclined defect is formed at the interface; details of the atomic structure of such a defect can be found in Figure 5.10. These defects may act as scattering sites for electrons and can be found in many reported SAG studies.[13,17,19,27] Therefore, it is important to enable growth of a complete, in-plane network structure from a single nucleation site, which is difficult to achieve for MBE grown InSb.[18,24] For this, a large surface diffusion length of the precursor material is required as well as a low nucleation probability. Here, we show that metalorganic vapour-phase epitaxy (MOVPE) grown InSb in-plane selective area networks (InSANe) can indeed generate complicated 1D networks from a single nucleation site.

First, the desired structures are etched into a 20-nm-thick Si_xN_y mask (see Section 5.6.1), aligned to four different crystal directions, the [-211], [-101], [-1-12] and [0-11], on an InP (111)B substrate (see Figure 5.1a).

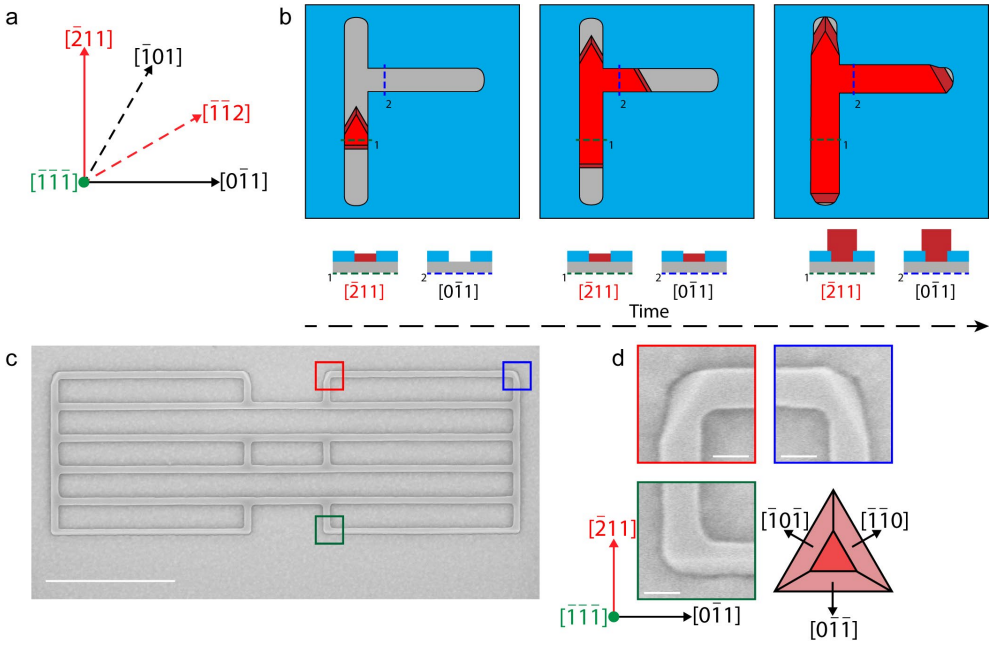

Figure 5.1 | Controlled growth of in-plane selective area InSb networks
a: The four growth directions on a (111)B substrate suitable for in-plane nanowire growth. **b:** Time evolution for growth of an in-plane InSb (red) nanowire network on an InP (111)B substrate (grey) with a 20 nm thick Si_xN_y mask (light blue) for selectivity. The growth fronts remain the same during the growth of the network. Schematics of the cross-sections below show the relative height of the InSb compared to the height of the mask. The network grows much faster in the in-plane direction than the out-of-plane direction (see also Figure 5.12). **c:** SEM image of the in-plane InSb nanowires controllably grown in the <112> and the <110> families of crystal directions. Scale bar is 1 µm. **d:** Zoom-in on the corners of the structure in (**c**). Scale bar is 50 nm. The {110} facets that form the growth fronts are still visible at these edges.

These four orientations are all three-fold symmetric, such that networks can be grown with angles of 30, 60 and 90 degrees between two nanowires as shown in Figure 5.2.

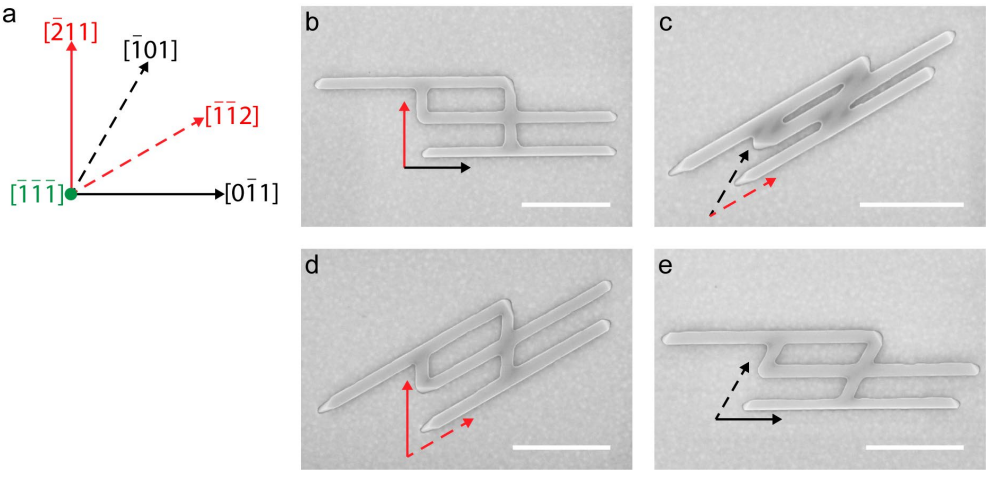

Figure 5.2 | Sensitivity to crystal directions
In-plane InSb nanowires can be grown in specific crystal directions, namely the <112> and the <110> families of directions. In order to create in-plane networks, mask openings must be in any combination of these directions. **a**: Crystal directions on a (111)B substrate showing the first quadrant of <112> and <110> directions. Combinations can be made with <112> and <110> directions in either 90 degrees (**b**) or 30 degrees (**c**). under 60 degrees angles combinations of <112> directions (**d**) or <110> directions (**e**) can be defined. Scale bars in the SEM images **b-e** are 500 nm.

The growth starts by forming a nucleus in one of the lines, which develops into an InSb island over time (Figure 5.1b and Figure 5.11). All nuclei are terminated with a {111}B top facet and {110} side facets (Figure 5.1b), regardless of the line orientation, implying that surface growth kinetics, the families of most stable available side facets and lateral growth rates are identical for all <110> and <112> growth directions. For longer growth times, the growth continues, starting from this single nucleus, in the lateral direction following the mask opening by growing {110} facets, as evidenced by atomic force microscopy (AFM) and transmission electron microscopy (TEM). When the structure is fully grown in the in-plane direction, the growth continues in the vertical <111>B direction. The height of the InSb network can be precisely tuned by the growth time (see Figure 5.12). Under ideal conditions, a yield (i.e., fully filled pattern without overgrowth in corners or parasitic growth) of up to 80% can be achieved for structures several microns in length (see Figure 5.13). When the InSb grows higher than the mask, it also starts to expand in the lateral direction, especially at acute corners of

the structure (Figure 5.12 and Figure 5.14), which is not ideal for transport measurements as the one-dimensional confinement is lost. An example of a network is shown in Figure 5.1c (and Figure 5.15), whose structure corresponds to the proposed geometry of a four-topological-qubit device.[20] The {110} planes of the original growth fronts are visible on the convex corners of this structure (Figure 5.1d). These facets do not form on the concave corners due to the connection with another branch of the network (Figure 5.14). Our platform provides freedom of design and scalability for a plethora of device structures as demonstrated in Figure 5.3.

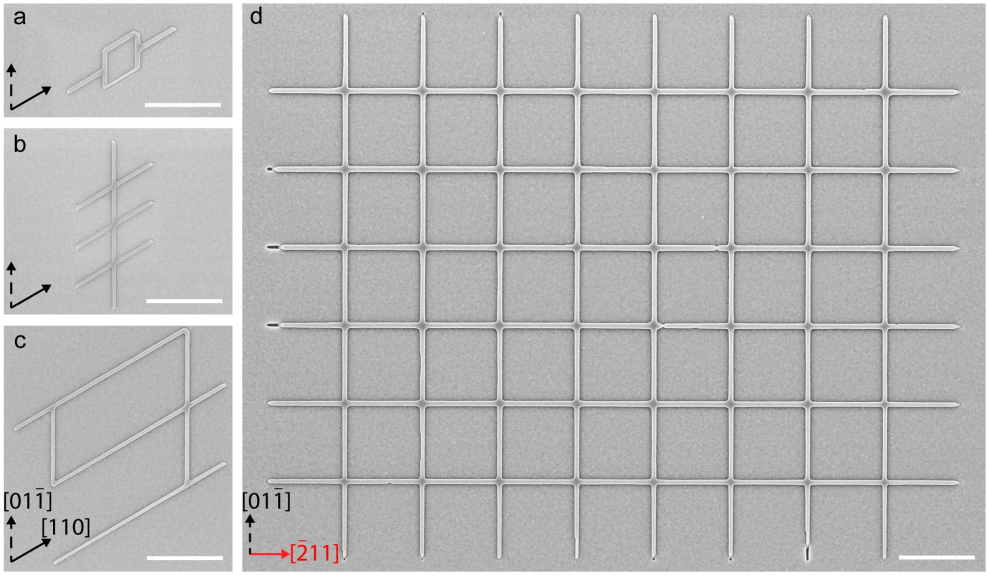

Figure 5.3 | Scalability of In-plane Selective Area Networks of InSb nanowires a-d: To demonstrate the scalability of this growth technique, different network designs in different sizes have been grown on the same substrate in the same growth run. All scalebars are the same size and represent 1 µm, showing that networks ranging from 200 nm by 200 nm loops (**a**), up to 11 µm by 11 µm hashtag networks (**d**) can be grown at the same time, independent of crystal direction, given that the mask is opened in <112> and/or <110> crystal directions.

In order to minimize the formation of inclined defects, the number of nucleation sites in the mask openings per unit length (n) is investigated as a function of the input V/III ratio of the Tri-Methyl-Indium (TMIn) and Tri-Methyl-Antimony (TMSb) precursors. For this purpose, InSb is grown for a short time (1 minute) to observe the early stages of nucleation and understand the nucleation probability as a

function of V/III ratio. *n* is determined for growth in the <112> and <110> oriented trenches for different V/III ratios (Figure 5.4).

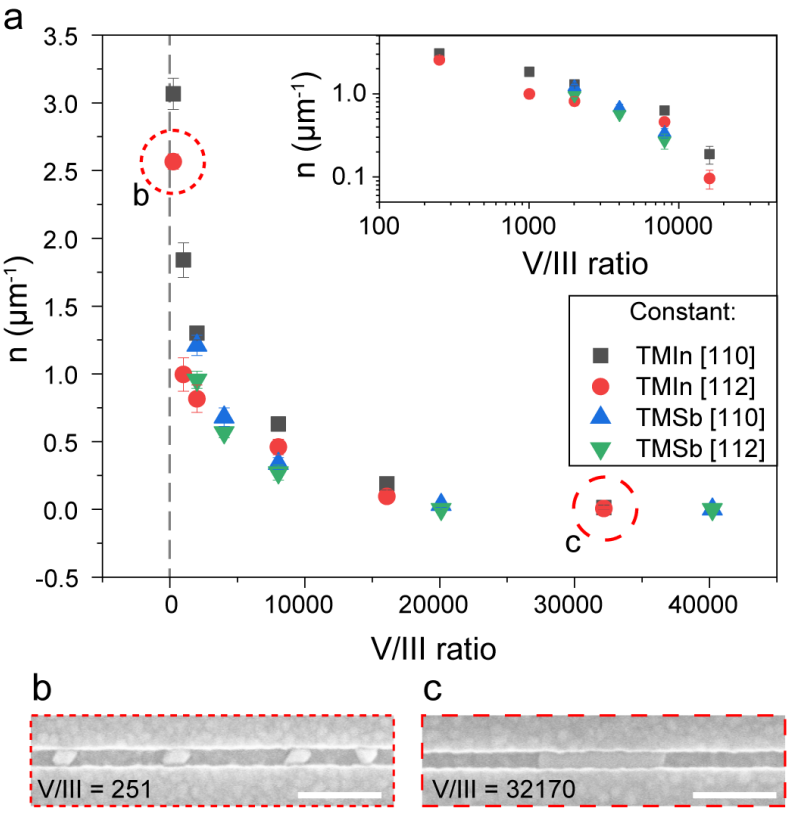

Figure 5.4 | Effect of V/III ratio on nucleation of InSb on InP (111)B
a: The average number of nucleation points *n* per micrometre trench length as a function of the V/III ratio during the growth for different crystal directions of the mask openings ([110] and [112]). The datapoint averages are gathered by analysing 500 µm length of mask opening (10 lines, each 50 µm long) and error bars represent the standard deviation. **Inset**: Logarithmic plot of the data up to a V/III ratio of 20,000. **b, c**: Top-view scanning electron microscopy (SEM) images showing the different morphologies of, and distance between, InSb islands for low (b) and high (c) V/III ratios. Scale bar in **b, c** is 200 nm.

Datapoints are averages of ten 40 nm wide and 50 µm long lines on each sample. The results show a clear decrease of *n*, and thus an increase of the diffusion length of the adatoms on the InP surface, with increasing V/III ratio. At the highest TMSb pressures, the nucleation of InSb islands is completely inhibited. The inset in Figure 5.4a is a logarithmic plot of the same data up to a V/III ratio of 20,000, showing a

decrease of n with increasing V/III ratio. We note that there is no parasitic growth on the mask under any of these conditions. The red-circle and black-square (blue and green triangle) data points are all taken with the same TMSb (TMIn) partial pressure and varying TMIn (TMSb) partial pressure, respectively. Figure 5.4a shows that these datapoints all follow the same trend, implying that it is the ratio rather than the absolute value of the flow that influences the nucleation of the InSb on the InP in the studied range. Figure 5.4b shows a scanning electron microscopy (SEM) image of nuclei grown using a low V/III ratio. The InSb islands are only tens of nanometres long and approximately 20 nm wide. Figure 5.4c shows an SEM image of a representative nucleus grown with a very high V/III ratio. Here, the InSb island is much longer (300 nm) and less than 20 nm high. The time series in Figure 5.12 shows that the InSb structures nucleate from a single site and over time, during growth under the same growth conditions, no new nucleation sites appear as all grown segments in a single structure are connected at all times. From these results, we conclude that Sb changes the surface energy on the InP substrate and enhances the surface diffusion of the In precursor material.[28] For the growth of large networks, a high V/III ratio is thus beneficial to have a minimum number of nucleation events. By integrating over the total volume of all nuclei in a 50 µm long line structure, we find that the lateral growth rate is determined by the TMIn flux (with higher flux giving faster growth rates) and the V/III ratio (with higher V/III ratio giving slower growth rates). The largest single-crystalline networks we have fabricated with our method have a wire diameter of around 60 nm with lengths of up to 11 µm (see Figure 5.3d).

5.3. Physical characterization

The structural quality of the in-plane wires has been investigated by transmission electron microscopy (TEM). Focused Ion Beam (FIB) sample preparation was used to cut out cross-sections parallel and perpendicular to the long axis of in-plane [-211] and [0-11] oriented nanowires. Figure 5.5a shows a cross-sectional view of a nanowire grown along the [-211] direction.

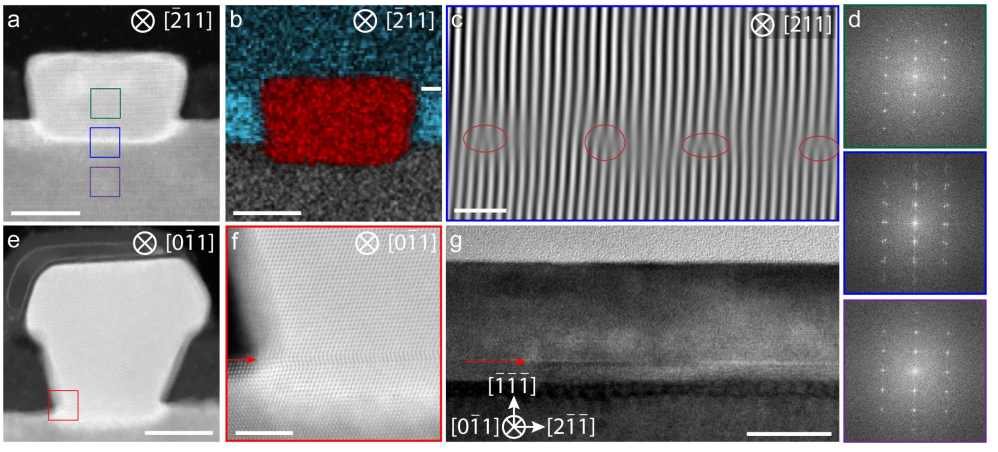

Figure 5.5 | Crystal quality analysis of InSb nanowires and the InSb/InP interface

a: Cross-section HAADF-STEM image of an In-plane Selective Area (InSANe) InSb nanowire grown and imaged along the [-211] direction. Scale bar is 20 nm. **b**: Energy-Dispersive X-Ray spectroscopy (EDX) map of **(a)** with P (grey), Sb (red) and Si (light blue) depicted showing the InSb nanowire, the InP substrate, the Si_xN_y mask and the SiO_x deposited in the FIB as a protective layer. The top of the mask is indicated by a white dash on the right. Scale bar is 20 nm. **c:** Zoom-in on the InSb/InP interface in **(a)** (blue square) focusing on the atomic columns using an Inverse Fast Fourier Transform procedure filtered for the (110) periodicity. Scale bar is 1 nm. The vertical lines represent the columns of atoms which, at the interface of InSb/InP, show misfit dislocations, encircled in red. Counting the ratio of InSb columns and InP columns gives a lattice mismatch of 10.34%. **d:** Fast-Fourier Transform images of the InSb nanowire (**a**, green), the InSb/InP interface (**a**, blue) and the InP substrate (**a**, purple), demonstrating that the InSb and InP regions are both single-crystalline. The Fast Fourier Transform (FFT) of the InSb/InP interface region shows double spots indicating an epitaxial relation and two different unit cell parameters. **e**: Cross-section HAADF-STEM image of an InSANe InSb nanowire grown and imaged along the [0-11] direction. Scale bar is 20 nm. **f**: Zoom-in of (**e**) where a pair of horizontal twin planes can be observed a few nanometres above the InP/InSb interface. Scale bar is 5 nm. **g**: Bright Field TEM image of a sample cut along a <112> direction grown wire, looking in the perpendicular <110> zone axis. A few nanometres above the InP/InSb interface, a horizontal twin plane can be observed along the entire observed length of the wire, indicated here by a red arrow. Scale bar is 20 nm.

The Energy-Dispersive X-Ray spectroscopy (EDX) elemental mapping (Figure 5.5b) shows the InP substrate (grey) with the InSb nanowire (red) grown slightly higher than the Si_xN_y mask (light blue, top indicated by a white dash on the right). An Inverse Fast Fourier Transform (IFFT) of a zoom-in on the InSb/InP interface (Figure 5.5c) shows misfit dislocations (Section 0-1) and their confinement to the interface between the two materials. This real space image was constructed by filtering for the (110) periodicity in the Fast Fourier Transform (FFT) pattern of a high-resolution scanning TEM (STEM) image and subsequently creating an Inverse FFT image. In this image, the ratio of the number of InP/InSb atomic planes is 96/87 = 1.1034. The 10.34 % decrease in vertical lattice planes is in good agreement with the reported value of a 10.4 % lattice mismatch between InSb and InP,[4] indicating that the heterostructure is fully relaxed (inelastically) at the interface in the lateral direction. Here, it should be mentioned that when imaging orthogonally to this crystal direction the InP/InSb interface cannot be imaged accurately due to the slight recess of the wire into the substrate. A resulting TEM sample would have to be thinner than the line width of 20 nm and should only contain the InSb line itself to avoid the superposition of the InSb line and the substrate adjacent to it. It is virtually impossible to create such a TEM sample. Most likely, along the long axis, misfit dislocation planes will also be present with the dislocation lines located at the interface, as we do not see vertically extending defects orthogonal to the long axis of the wires in TEM studies. An FFT of the InSb, the InSb/InP interface and the InP regions of the high-resolution STEM image (Figure 5.5d in green, blue and purple box, respectively) show that the InSb and the InP are both single-crystalline while the FFT pattern of the interface region displays a combination of two single-crystalline patterns with a different lattice constant indicating that the materials are epitaxially related and fully relaxed. To visualize the presence of horizontal twin planes (Section 0-4) in the InSb structures, we investigate a cross-section of a nanowire grown along the <110> direction (Figure 5.5e). A zoom-in on the bottom part (Figure 5.5f) reveals a set of two twin boundaries a few nanometres above the InP/InSb interface (Figure 5.5g). Horizontal twin planes have in total been observed in 12 out of 17 TEM samples (6 in perpendicular cuts of <110> grown wires and 6 in parallel cuts of <112> grown wires, the other 5 TEM samples did not show horizontal twin planes). The twin planes are always located within a few nanometres above the InSb/InP

interface and a single-crystalline InSb transport channel always forms above the horizontal twin. Once a twin plane is formed in a nucleus it will be extended into the rest of the network by lateral growth. We note that antiphase boundaries (Section 0-2) and inclined twin planes (Section 0-3) are absent in these structures. The complete relaxation of lattice strain at the nanowire/substrate interface (bottom part) followed by horizontal twin planes helps to separate the electron wavefunctions in the active region of the device from the interface disorder.[29] This effect allows us to fabricate in-plane InSb nanowires on InP that can have quantum transport properties comparable to free-standing structures as demonstrated by the high quality quantum transport in the next section.

The next important step is to introduce superconductivity in the InSb InSANe system. In order to form superconducting contacts for the creation of Majorana zero modes, the InSANe InSb samples, after growth, are transferred from an MOVPE to an MBE system. Here, the surface oxides are removed using atomic-hydrogen cleaning under (ultra-high vacuum) UHV conditions followed by 7 nm aluminium deposition at a sample temperature of around 120 K, leading to a clean and smooth InSb-Al interface as shown in Figure 5.6.[8] More details on the deposition process can be found in Chapter 3.2.

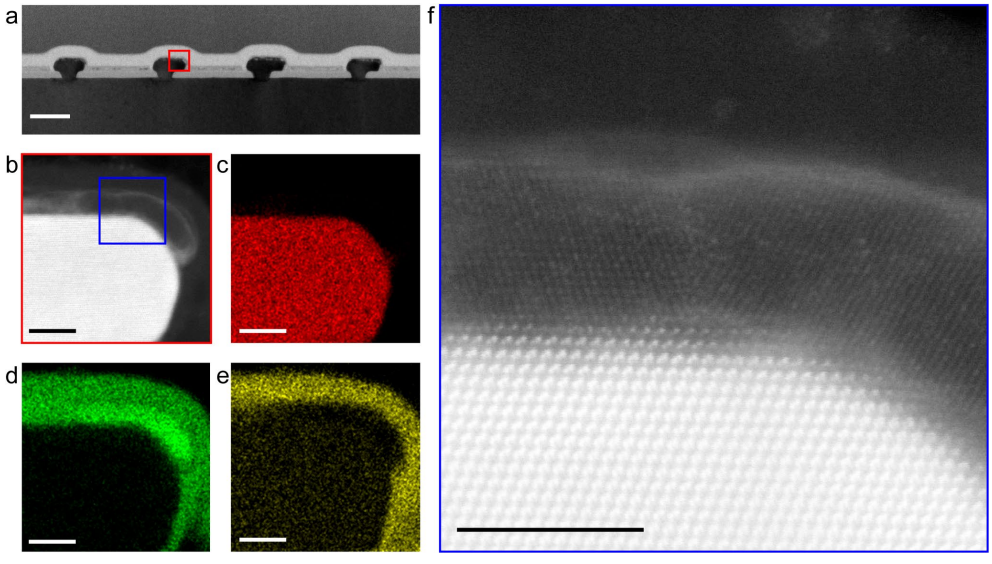

Figure 5.6 | Al interface in the InSANe InSb-Al hybrid system
a: Cross-section bright field TEM image of four InSANe InSb nanowires grown on top of an InP (111)B substrate. Scale bar is 100 nm. **b**: HAADF-STEM zoom-in of the red area in **(a)**, showing the InSb nanowire top edge with a 5 nm Al layer deposited on the wire. Energy-Dispersive X-Ray spectroscopy (EDX) analysis of the area in **(b)** shows the Sb (**c**, red), Al (**d**, green) and O (**e**, yellow) in the InSb-Al hybrid network, depicting an oxide free InSb-Al interface. Scale bar is 10 nm. **f**: A zoom-in on the interface in **(b)** shows the clean and smooth interface between the InSb wire and the Al. The crystal lattices of two separate Al grains can be identified in the image, showing the high quality of the Al layer. Scale bar is 5 nm.

5.4. Quantum transport

We now turn to the quantum transport properties of our InSb InSANe system to demonstrate its feasibility for topological quantum information processing. The key ingredient in the measurement-based gate operation and topological qubit readout is the phase coherence, which can be revealed by the Aharonov-Bohm (AB) effect.[11,20] The magneto-conductance in Figure 5.7a reveals the AB oscillations in a fabricated InSANe device shown in the inset of Figure 5.7b.

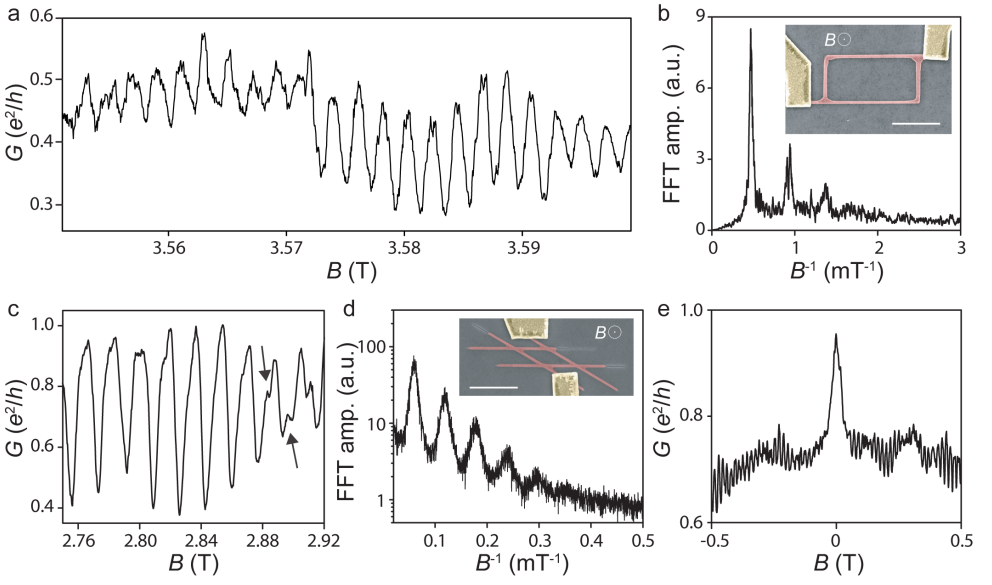

Figure 5.7 | Aharonov-Bohm and weak-anti-localization effects in InSANe nanowire loops

a: Magneto-conductance of device A shows Aharonov-Bohm (AB) oscillations with a period of ~ 2 mT. **b**: Fast Fourier Transform (FFT) spectrum of the AB oscillations from device A, indicating the frequency peaks up to the 3rd order harmonic. Inset, false-colour scanning electron microscopy (SEM) image of the device. An InSb nanowire loop (red) is in contact with normal metal electrodes Cr/Au (yellow) with an out-of-plane magnetic field and a fridge temperature of 20 mK. The device has a global top gate that is not shown in the SEM image. Scale bar is 1 µm. The measured AB period matches the loop area of ~ 2 µm^2. **c**: Magneto-conductance of device B shows a larger AB period and oscillation amplitude (~0.6 e^2/h), due to its smaller loop area compared to device A. The arrows indicate oscillations due to higher AB harmonics. **d**: FFT spectrum of device B (SEM in inset with scale bar 1 µm) showing up to five harmonic peaks. **e**: Magneto-conductance of device B (ensemble averaged) shows a sharp weak anti-localization peak at B = 0 T.

The oscillation amplitude is ~20 % of e^2/h at 20 mK., about an order of magnitude larger than for previously reported InSb VLS nanowire network structures.[8] Therefore, higher harmonics (up to the third) in the Fast Fourier Transform (FFT) are observed (**Figure 5.7b**). This means that the electron's interference due to phase coherence remains measurable after circulating through the loop 1.5 times, translating to ~9 microns in this device. We note that the precise value of the phase coherence length is not crucial, and that a large AB amplitude, especially higher orders of AB oscillations, presents the qualitative advancement in this work compared to previous studies. A second device shows an even larger AB amplitude (~60 % of e^2/h in **Figure 5.7c**) and up to 5 harmonics in the FFT spectrum (**Figure 5.7d**) with the SEM image of the device shown in the inset of **Figure 5.7d**. The measured AB period matches the loop area in all measured devices, *i.e.* their periods equal h/ne (for the n^{th} harmonic). This result corroborates that the lattice-mismatch-induced disorder at the nanowire-substrate interface has negligible effect on the phase coherent transport. Finally, we observe a sharp weak anti-localization (WAL) peak in the magneto-conductance of this device around zero magnetic field (**Figure 5.7e**), indicating the strong spin-orbit nature of the InSb nanowire. Fitting this WAL curve requires a new theoretical model applicable for nanowire networks, which will be developed in future studies.

Next, we investigate the InSb-Al InSANe semiconductor-superconductor system. Since *in-situ* shadowing methods to selectively grow superconductors on these InSb in-plane structures are not yet developed, we exploit a reliable selective etching recipe to selectively etch Al on InSb. This novel fabrication recipe enables us to define the positions of tunnel barriers and the Al film by lithography, facilitating flexible device designs. **Figure 5.8a** shows such a device where part of the Al is selectively etched away, and a tunnel gate electrode is added to deplete the InSb wire locally. A super-gate is deposited on the superconducting region of the nanowire whose cross-section is shown in **Figure 5.8b**.

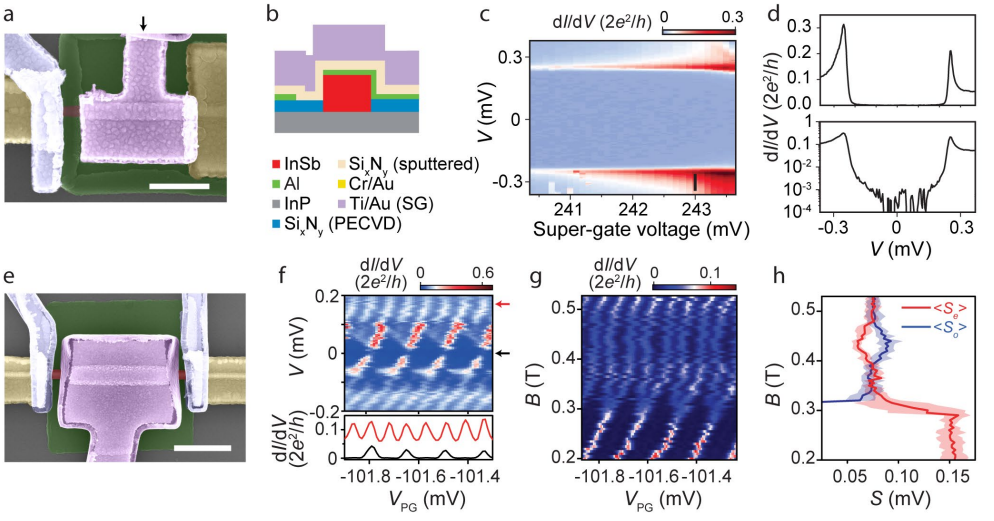

Figure 5.8 | Hard gap and 2e-periodic Coulomb blockade in InSANe InSb-Al hybrid nanowire devices

a: False-colour scanning electron microscopy (SEM) of a typical normal-nanowire-superconductor (N-NW-S) device for illustration purpose, with a schematic of the device cross-section (**b**) at the position indicated by the black arrow in (**a**). The InSb nanowire (red) is covered by a 7 nm thick Al layer (green, covered by the etch mask). Part of the Al film on the nanowire is selectively etched (see methods) before normal metal electrodes deposition (yellow, Cr/Au) and gate-tuneable tunnel barrier. The tunnel- and super-gates are Ti/Au (blue and purple, respectively), deposited on top and separated from the wire by a Si_xN_y dielectric layer as seen in the cross-section schematic on the right. Scale bar is 500 nm. Fridge temperature is 20 mK. **c**: Differential conductance (dI/dV) as a function of bias voltage (V) and super-gate voltage in the tunnelling regime, resolving a hard superconducting gap (Δ~250 μeV) with the line-cuts (both linear and logarithmic scale) shown in (**d**) at gate voltage indicated by black bar in (**c**). The sub-gap/above-gap conductance suppression reaches two orders of magnitude. **e**: False-colour SEM of the superconducting island device. The Al island on the nanowire is around 1 µm long, with a top plunger gate (purple) to tune the electron density, and two tunnel-gates (blue) to control the tunnel coupling to the two leads. Scale bar is 500 nm. **f:** Differential conductance of the island device as a function of bias and plunger-gate voltage resolving the Coulomb blockade diamonds. The horizontal line-cut at zero bias (black curve) shows 2e-periodic Coulomb oscillations where each peak corresponds to adding/removing two electrons (one Cooper pair), suggesting negligible quasi-particle poisoning. At higher bias voltage where quasi-particle can be excited, the Coulomb oscillations become 1e-periodic. **g**: Magnetic field dependence of the Coulomb oscillations at zero bias voltage with the field

direction along the wire. The 2*e*-peaks split into 1*e*-peaks at around 0.3 Tesla, indicating a sub-gap state crosses zero energy. **h**: even (S_e red) and odd (S_o blue) peak spacing extracted from (**g**), with error bars indicated with shaded areas, showing possible Majorana or Andreev oscillations.

The differential conductance on this normal-nanowire-superconductor (N-NW-S) device reflects the quasi-particle density-of-states in the proximitized nanowire segment, *i.e.* the induced superconducting gap as shown in **Figure 5.8c** with a line-cut in **Figure 5.8d**. The sub-gap conductance reaches zero, indicating a hard gap, a necessary condition for topological protection. Magnetic field dependence of accidental quantum dot levels reveals an effective *g*-factor of 18.6 (see **Figure 5.16**), smaller than the bare InSb g-factor of around 50 (see **Figure 5.17**) but significantly larger than that of Al ($|g|=2$), indicating the wavefunction hybridizes between InSb and Al.[29,30] The measured hard gap with a gap size close to Al bulk, together with the effective *g*-factor defined by the coupling between Al and InSb, suggest that the electron wavefunction is mainly distributed near the top (close to Al) where the wire is single-crystalline with no noticeable disorder.[31-33] This again supports that disorder at the InP/InSb interface has a negligible effect (see **Figure 5.18**, a cross-section TEM of a typical device).

Finally, we explore the transport of a hybrid InSb/Al island device (**Figure 5.8e**), with a finite charging energy. The charging energy of the hybrid island can mediate the coupling between the two Majorana states for qubit operations and readout.[11,20,34] If the charging energy is less than the superconducting gap, the system ground state energetically 'favours' an even number of electrons, *i.e.* all electrons on the island form Cooper pairs in the superconducting condensate.[35] In transport, each Coulomb blockade diamond then corresponds to 2 electrons (1 Cooper pair), as shown in **Figure 5.8f**, as well as in **Figure 5.19**. The 2*e*-periodic Coulomb oscillation at zero bias (black curve) indicates negligible quasi-particle poisoning. A higher bias voltage can excite quasi-particles, resulting in the regular 1*e*-periodic Coulomb oscillations (red curve). Applying a magnetic field along the nanowire splits the 2*e*-peaks into 1*e*-peaks (**Figure 5.8g**), with oscillating even/odd peak spacing (**Figure 5.8h**). This 2*e* to 1*e* transition might be interpreted as the appearance of two Majorana states, which allows the coherent 'teleportation' of a single electron.[35] The oscillating peak spacing could

be attributed to overlapping Majorana wavefunctions.[36] We note that a trivial explanation for the 2e to 1e transition based on Andreev-bound states cannot be ruled out at this point.[37-39]

5.5. Conclusions

We have studied the crystal quality, morphology, and growth dynamics of in-plane InSb nanowires on InP (111)B substrates. Despite the large mismatch between the wires and the substrate, single-crystalline transport channels, free from extended defects, are formed due to immediate strain-relaxation at the nanowire-substrate interface. Correspondingly, these in-plane InSb based devices show high-quality quantum transport, with long phase coherence length, a hard superconducting gap, 2*e*-Coulomb blockade peaks and possible Majorana/Andreev signatures. The quality and scalability of this platform can be taken to the next level with the development of a technique to selectively deposit superconducting metals, avoiding the need to selectively etch material to make transport devices. This will allow for more complicated transport experiments, including key experiments like correlation and Majorana braiding.[40]

5.6. Appendix

5.6.1. Substrate fabrication recipe

An InP (111)B undoped 2-inch single-side polished wafer is used as the growth substrate for In-plane Selective Area Network (InSANe) InSb nanowires. The step-by-step recipe is as follows:

- Native oxide removal: Dip wafer in an H_2O:H_3PO_4 solution with a 10:1 ratio for 3 minutes and subsequently rinse wafer in ultra-pure water until clean (resistance bath >8 MΩ). Blow dry with N_2 gun.
- Amorphous mask layer: Deposit a 20 nm thick Si_xN_y using plasma enhanced chemical vapor deposition (PeCVD, Oxford Instruments PlasmaLab system 100).
- Resist: Spin ZEP520A+C60 mixture at 2000 RPM for 60 seconds followed by baking on a hotplate for 15 minutes at 150 ^{0}C.
- Lithography: Electron beam lithography to write patterns (Raith EBPG5150)
- Developing resist: Dip wafer in n-amyl acetate for 60 seconds followed by a Methyl-iso-butylketon: isopropanol (MIBK:IPA 89:11) mixture for 45 seconds and finally an IPA rinse (around 1 minute). Blow dry with N_2 gun.
- Mask etching: Etching of the Si_xN_y mask is done by using reactive ion etching with pure CHF_3 for 1 minute 15 seconds (Oxford Instruments PlasmaLab system 100 RIE).
- Remove resist: Put the wafer in a beaker with PRS3000 overnight (>8 hours). The next day, put the beaker with PRS3000+wafer in an ultrasound bath for a few minutes. Then dip the wafer in acetone for ~1 minute and then isopropanol for ~1 minute. Blow dry with N_2 gun.
- Removing resist residues: Clean wafer using an oxygen plasma treatment. (Oxford Instruments PlasmaLab system 100 (RIE), 15 mT, 50 W, 20 sccm O_2, 5 minutes).
- Oxide removal just prior to growth: InP surface oxide removal by dipping wafer in H_2O:H_3PO_4 10:1 solution for 3 minutes, followed by rinsing in a water bath (resistance >8 MΩ).

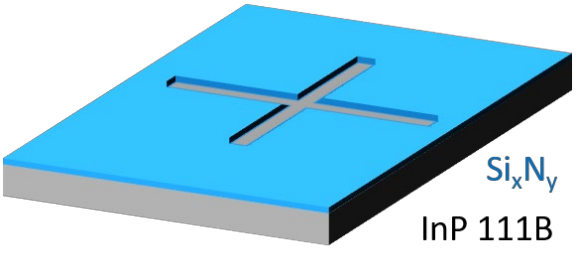

Figure 5.9 | Substrate after processing
Perspective view schematic of the final substrate after processing with an InP (111)B substrate (grey) and a 20 nm thick, selectively etched, amorphous Si_xN_y mask on top (light blue).

5.6.2. Growth of in-plane InSb networks

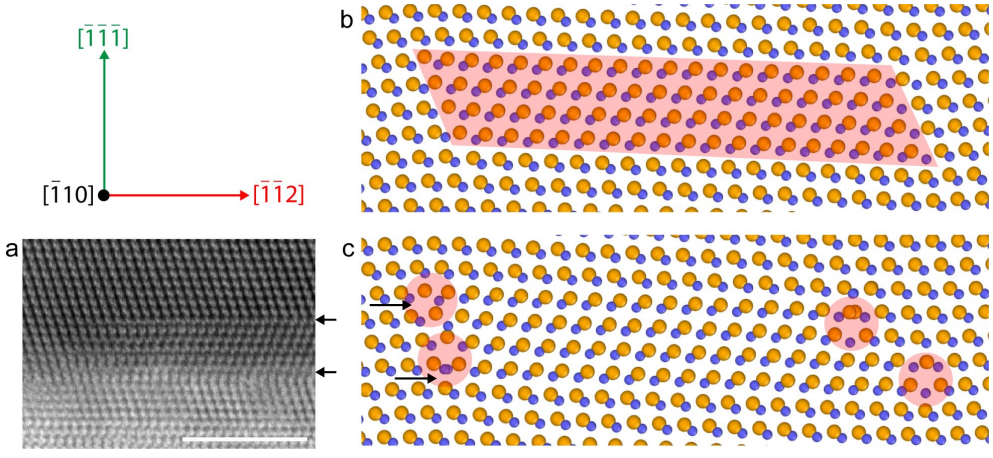

Figure 5.10 | Molecular Dynamics simulation on crystal relaxation between two twinned regions
a: Cross-section HAADF-STEM image looking along the <110> zone axis, with a twinned region on the right, indicated by the black arrows. Scale bar is 5 nm. The twinned region is not present on the left side of the image. In order to understand how the twins are connected to the original crystal orientation at their lateral boundaries, atomic simulations are performed using the semi-empirical Vashishta energy potentials for InP, which takes the first- and second-nearest neighbours into account. There is no potential available for InSb, but there is no general limitation, since we are looking for crystallographic ordering, which is the same for both semiconductors. **b**: Crystal cell containing a twinned region (marked in red, starting at the black arrows, with the same orientation as in the TEM image) with lateral boundaries parallel to the <110> direction prior to molecular dynamics (MD) annealing and energy minimization. **c**: crystal cell after MD annealing and energy minimization. 90^0 extrinsic stacking fault dislocation lines are formed parallel to the <1-10> direction (highlighted by red circles in the schematic cross-section), each composed by two 30^0 Shockley partial dislocations located in consecutive lattice planes. This is the only way a (111) oriented twin in the InSb lattice can be terminated and connected to the original crystal orientation, without forming amorphous regions at their boundary. It should be noted that raising the annealing temperature to 1000 K did not change the final structure of the InP cell in **(b)**. In conclusion, twins are always accompanied by dislocation lines running along all the <110> directions in the basic (111) plane, providing additional relieve of the residual misfit stain. This enables the InSb crystal above the twin plane to be completely free of any strain-induced defects.

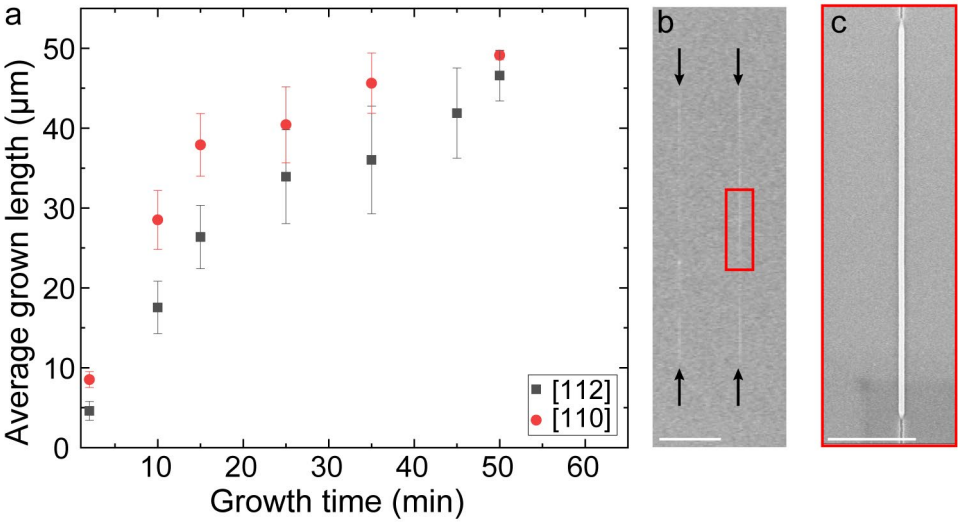

Figure 5.11 | Crystal direction dependent grown length of InSb nanowires as a function of growth time

a: Average grown length of InSb in-plane nanowires in 50 μm long openings in the mask in the <112> (black squares) and <110> (red circles) crystal directions as a function of growth time. In all cases the same temperature of 470 ^{0}C and V/III ratio of ~8000 is used during growth in the metalorganic vapour-phase epitaxy (MOVPE). The error bars are the standard deviation of the average, taken over ten lines per datapoint. **b**: Scanning electron microscopy (SEM) image showing two 50 μm long lines (indicated with black arrows) in the <112> direction after 35 minutes of growth. Scale bar is 10 μm. A zoom-in is shown in (**c**), clearly showing a grown InSb nanowire (bright white), with at the top and bottom of the image a small segment in the mask that is not yet filled by InSb growth. Scale bar is 1 μm.

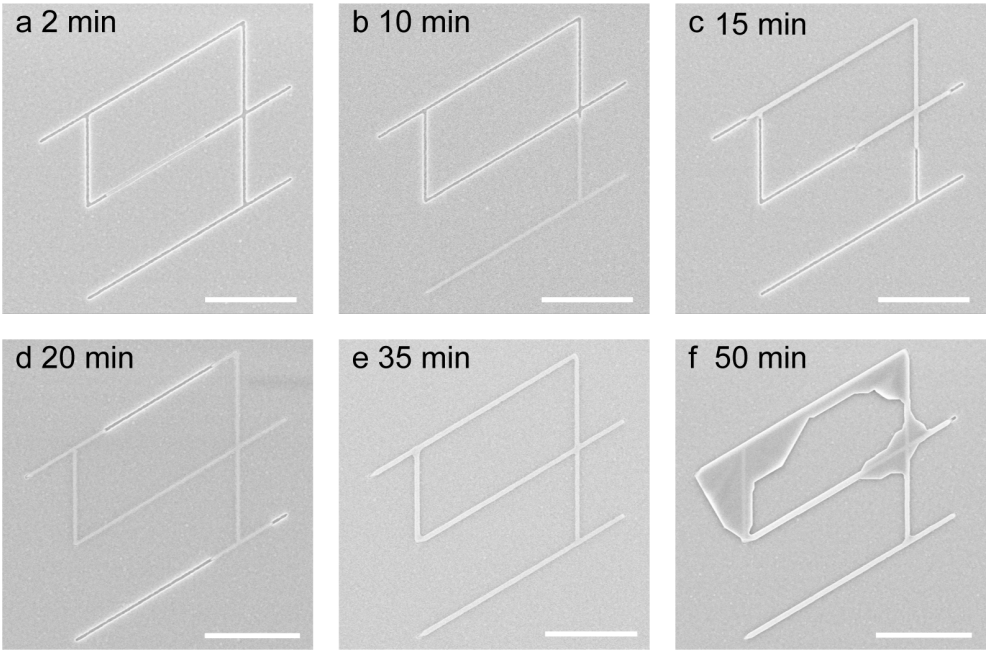

Figure 5.12 | Network growth as a function of growth time
a-f: Scanning electron microscopy (SEM) images of a representative structure (out of hundreds of similar structures on the same sample) at different growth times under the same growth conditions. Scale bars are 1 µm. The growth starts with one nucleation site (**a**) and starts growing outwards, following the openings in the mask (**b-d**). Note that no new nucleation sites are formed. Once the structure is fully filled, it starts to grow only in the vertical direction **(e)**. When growth is not stopped in time, the structure starts growing out of and over the mask (**f**).

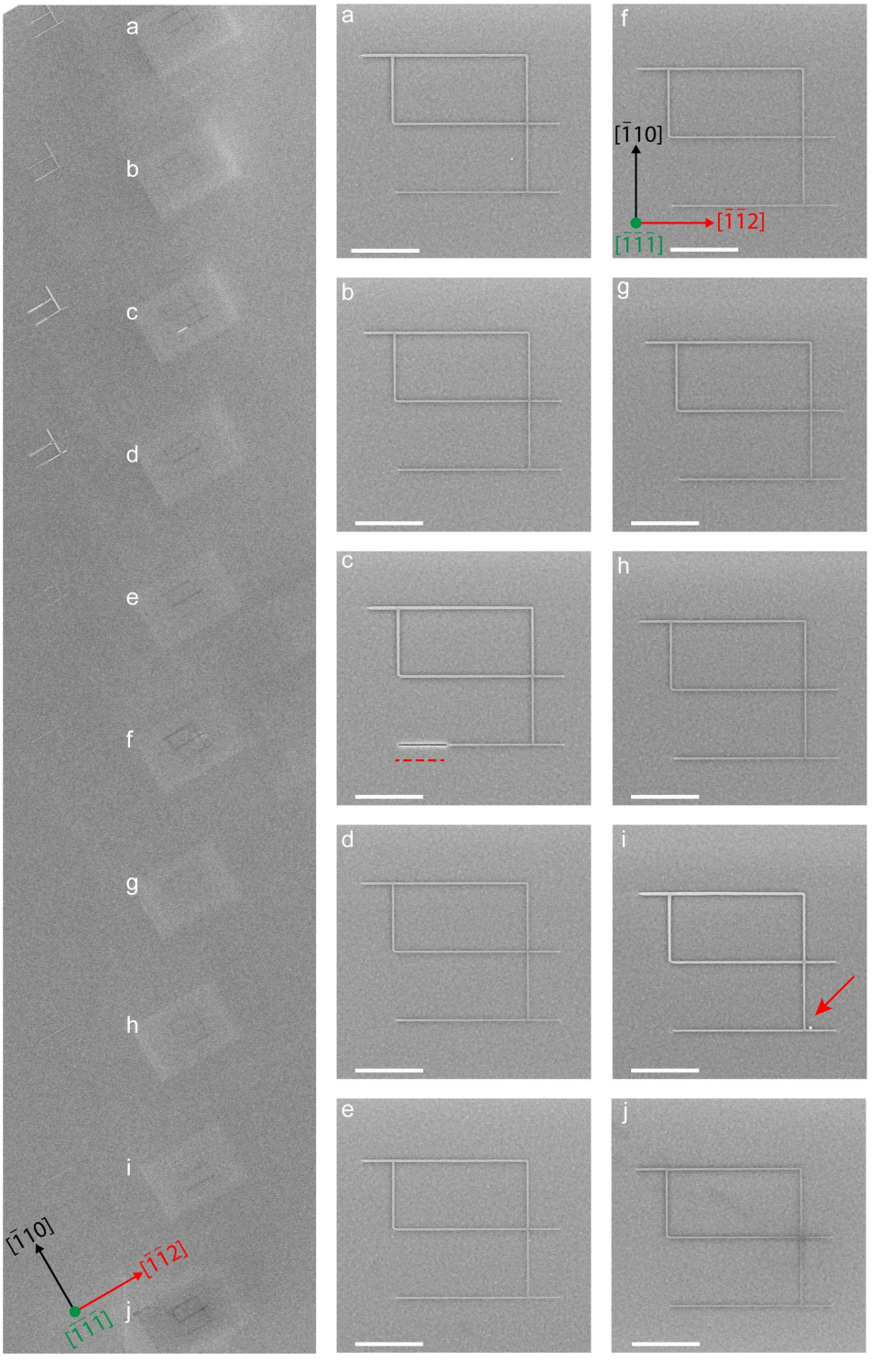
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Figure 5.13 | Yield demonstration of well grown structures
Overview SEM image of a region on the sample containing 10 repetitions of the same design, in this case a single qubit structure, labelled **(a-j)**. Scale bars are 1 µm. As evidenced in **(a-j)**, a yield of up to 80% can be achieved under ideal growth conditions. **(c)** shows a structure where the last part of the bottom arm is not fully grown (red dashed line). **i:** scanning electron microscopy (SEM) image of a fully-grown structure with a small particle close to the bottom arm, indicated by the red arrow.

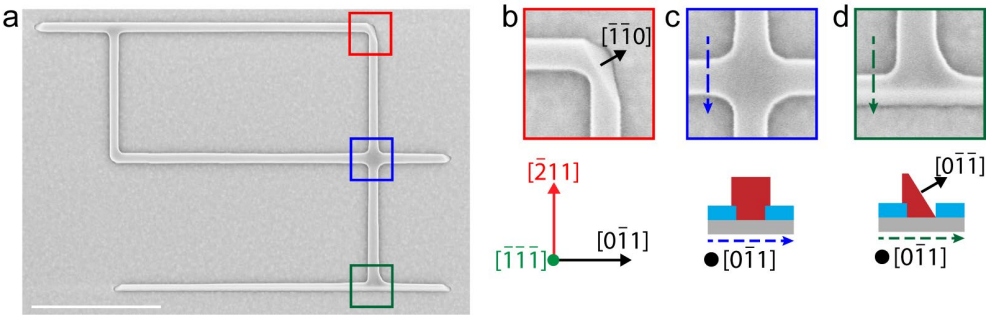

Figure 5.14 | Influence of extended arms on terminating side facets
a: Scanning electron microscope image of an InSb nanowire network in a single qubit design structure. Scale bar is 1 µm. The terminating {110} side facets shown in Figure 5.1 are visible in (**b**) (red square) and (**d**) (green square). **b**: The top-right corner of the structure shows the (-1-10) terminating facet. **c**: The cross-junction is missing the (0-1-1) terminating side facet, which is present in (**d**). The extra arm extending down changes the preferred terminating side facet here. A sketch is shown for both (**c**) and (**d**) to illustrate the difference in geometry.

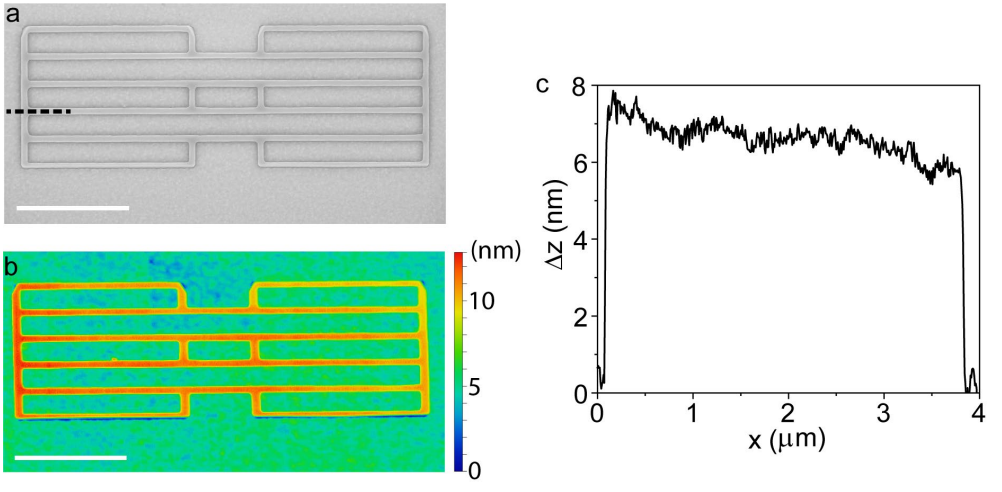

Figure 5.15 | Atomic force microscopy analysis of in-plane selective-area InSb network

a: Scanning electron microscopy (SEM) image of a 4-qubit design. **b**: Atomic force microscopy (AFM) height colour map of the same structure as in (**a**) showing the uniform height of the InSb structure. **c**: Line cut taken through the 4th line in the [110] direction showing the height relative to the top surface of the Si_xN_y mask. The height changes ~1.5 nm over a length of 4 μm, or 1 atomic step per 2 μm indicating a layer-by-layer growth on the top (111)B surface of the structure. Scale bars are 1 μm.

5.6.3. Atomic defect analysis

Types of possible defects that can be distinguished in selective area grown structures:

1. Misfit dislocations at the interface between the substrate and the wire. These arise due to a mismatch in lattice constant of the two materials. Their location is confined to the interface.

2. An antiphase boundary, which is formed if two nuclei, in which one of them has a twinned orientation with respect to the (111) B growth substrate, merge. This results in a charged plane between the two nuclei, leading to detrimental effects on the transport in the channel. (The orientation of a possible anti-phase boundary is vertical or inclined to the substrate.)

3. Inclined twin planes (being introduced during growth of a single nucleus rather than by the merging of two nuclei). These have been shown to increase the resistance of the channel,[41] and have been observed in literature.[13,19]

4. Horizontal twin planes, as observed in our structures, a few nm above the substrate/ wire interface.

In our structures, we observe misfit dislocations at the interface **(1.)**, which is unavoidable due to the large lattice mismatch of 10.4 % in our material system. Just above the plane with misfits we observe a horizontal twin plane **(4.)** in most of our structures. This twin plane is parallel to the electronic transport direction and therefore does not negatively affect the transport properties – as a matter of fact, the horizontal twin electrically isolates the transport channel from the misfits. The electron wavefunction is located near the InSb/Al interface at the top of the wire. This transport channel is free of defects since we do not observe defects **(2.)** and **(3.)** in our structures. The detrimental effects on electronic transport reported in [15] were not observed in our structures. The conductance could be effectively pinched off and the charge carrier density fully depleted.

5.6.4. Quantum transport data

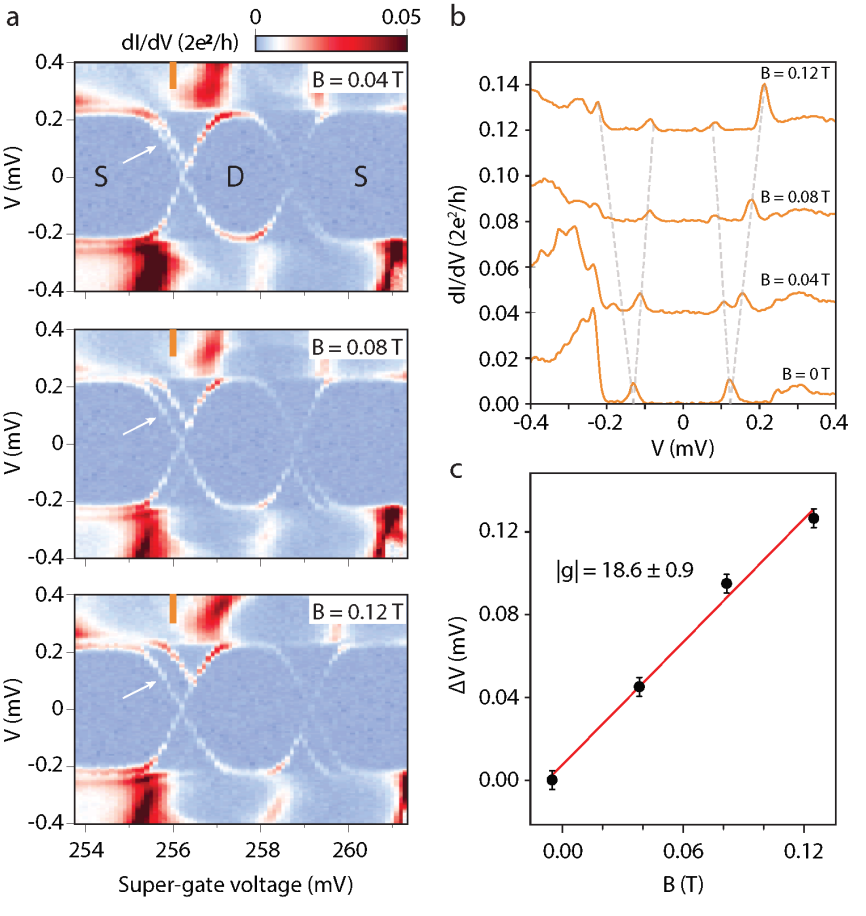

Figure 5.16 | Extraction of the g-factor in the N-NW-S device
a: Differential conductance of the N-NW-S device measured as a function of bias voltage V and super-gate voltage at different magnetic fields (0.04 T, 0.08 T and 0.12 T from top to bottom) along the nanowire. Andreev levels corresponding to the transitions between the singlet and doublet states (indicated with S/D respectively) are observed.[42] Note that the Andreev levels corresponding to singlet ground states have Zeeman splitting (white arrows). **b**: Line traces from panel (**a**) at the super-gate voltage of 256 mV (at orange lines in a), plus the line trace at the same super-gate voltage at zero magnetic field. Offset between lines is $0.04 \times 2e^2/h$. Zeeman splitting is indicated by the dashed lines. **c**: The spacing between the split peaks (black dots) of **b** (positive side) as a function of B. The slope of the linear fit (red line) is used to extract the g-factor. The error bars are given by the uncertainty of peak-finding, simply taking the bias interval of data.

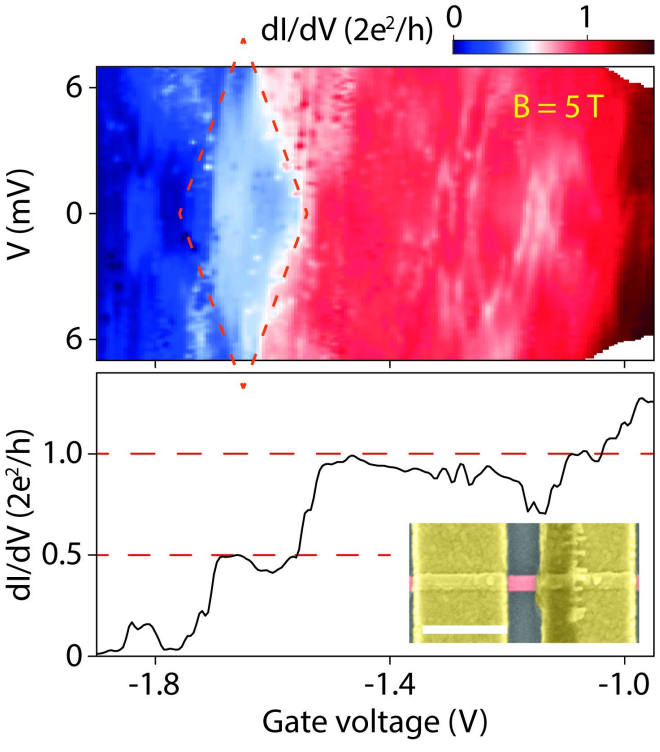

Figure 5.17 | Quantized conductance of an in-plane InSb nanowire
Upper panel: differential conductance measured as a function of bias voltage V and gate voltage at a magnetic field of 5 T perpendicular to the substrate. Conductance plateaus are visible, and the plateau of e^2/h is indicated with red dashed lines. A g-factor of around 57 can be roughly extracted. **Lower panel**: horizontal line cut of the upper panel at V=0. Conductance at e^2/h and $2e^2/h$ is marked with red dashed lines. We note the plateau quality is expected to be worse than VLS InSb nanowires,[43] probably due to the facts that 1) the nanowire was heavily etched by argon plasma before contact deposition; 2) near the pinch-off region, the top gate pushes the electron wavefunction towards the nanowire bottom (substrate with large lattice mismatch). Both introduce extra disorders which degrade the plateau quality. Inset: SEM image of the quantum point contact device. A nanowire segment (red) is contacted by Cr/Au (yellow) with 200 nm spacing. Global dielectric and top gate are not shown in this image. Scale bar is 500 nm. A minimum smoothing was applied together with a series resistance of 2.5 kΩ subtracted following the method in Ref [43].

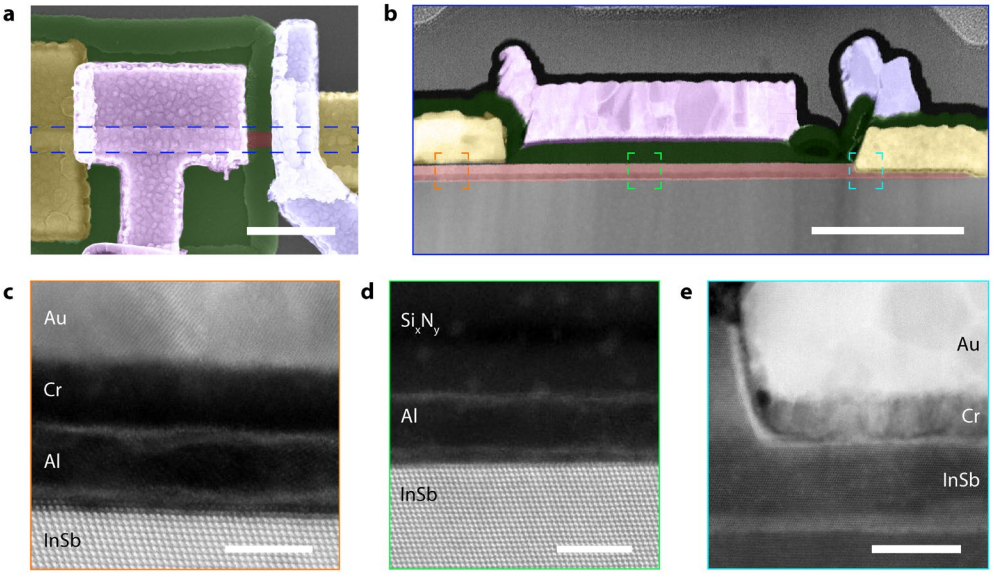

Figure 5.18 | Cross-section TEM images of a N-NW-S device
a: Scanning electron microscopy (SEM) image of a normal-nanowire-superconductor (N-NW-S) device. The InSb nanowire (red) is covered by an Al layer (green, covered by the etch mask). Contacts are Cr/Au (yellow). The tunnel- (blue) and super- (purple) gates are Ti/Au, deposited on top and separated from the wire by a Si_xN_y dielectric layer. Scale bar is 500 nm. The area indicated with blue dotted lines shows where the TEM specimen is made. **b**: Cross-section HAADF-STEM image of the device. The structures have the same colours as those of the corresponding structures in **(a)**, except for the Si_xN_y dielectric coloured in green together with Al. Scale bar is 500 nm. **c**: High-resolution STEM image of the orange region in **(b)**, showing the structure of the super contact. Note that the Cr/Au can contact the nanowire from the facet not covered by Al even though the AlO_x layer (between Al and Cr) on top of Al is not sufficiently removed by a milling process. Scale bar is 5 nm. **d**: High-resolution scanning TEM (STEM) image of the green region in **(b)**, showing the structure of the InSb-Al-Si_xN_y dielectric stack. Scale bar is 5 nm. **e**: High-resolution STEM image of the cyan region in **(b)**, showing the structure of the normal contact. Note that the milling process before depositing Cr/Au has etched into the InSb sufficiently to form an oxygen-free contact interface. Scale bar is 20 nm.

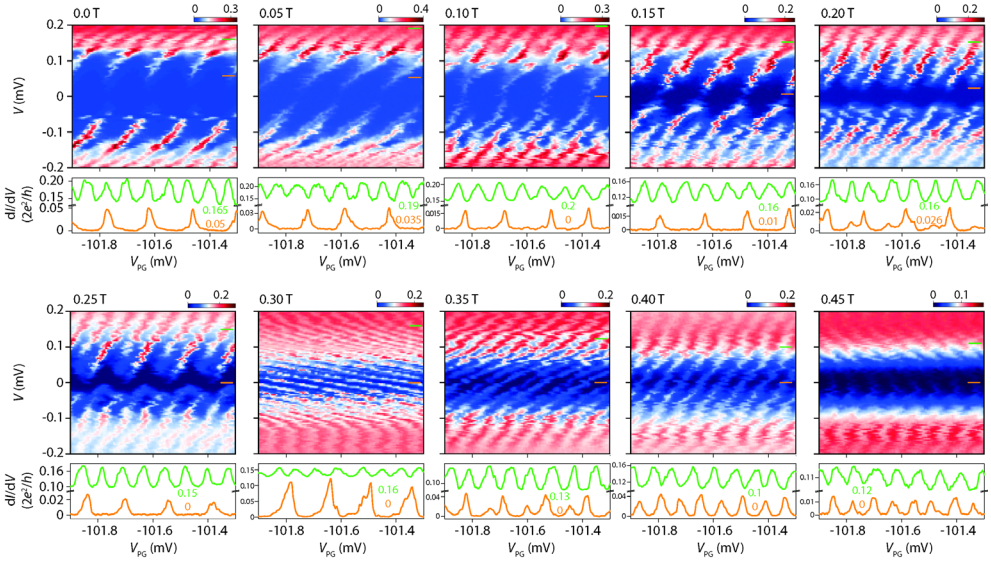

Figure 5.19 | Coulomb diamond of InSb-Al island device: transition from 2e-periodic to 1e-periodic

Differential conductance as a function of plunger gate V_{PG} and bias voltage V at different fixed parallel magnetic fields (from 0 T to 0.45 T, with 0.05 T step). The Coulomb diamond is not symmetric due to the asymmetric tunnelling strength of the two barriers. The panels below show line cuts at low bias (orange lines) and high bias (green lines) with the bias voltage indicated (in units of mV). The transition from 2*e*-periodic to 1*e*-periodic oscillations can be observed at low bias voltages.

5.7. References

1 Lutchyn, R. M. *et al.* Majorana zero modes in superconductor–semiconductor heterostructures. *Nature Reviews Materials* **3**, 52-68, doi:10.1038/s41578-018-0003-1 (2018).

2 Poerschke, R. & Madelung, O. Semiconductors Group IV Elements and III-V Compounds. *Data in Science Technology*, 124 (1991).

3 van Weperen, I. *et al.* Spin-orbit interaction in InSb nanowires. *Physical Review B* **91**, 201413, doi:10.1103/PhysRevB.91.201413 (2015).

4 Vurgaftman, I., Meyer, J. R. & Ram-Mohan, L. R. Band parameters for III–V compound semiconductors and their alloys. **89**, 5815-5875, doi:10.1063/1.1368156 (2001).

5 Bommer, J. D. S. *et al.* Spin-Orbit Protection of Induced Superconductivity in Majorana Nanowires. *Physical Review Letters* **122**, 187702, doi:10.1103/PhysRevLett.122.187702 (2019).

6 Plissard, S. R. *et al.* From InSb Nanowires to Nanocubes: Looking for the Sweet Spot. *Nano Letters* **12**, 1794-1798, doi:10.1021/nl203846g (2012).

7 Car, D., Wang, J., Verheijen, M. A., Bakkers, E. P. A. M. & Plissard, S. R. Rationally Designed Single-Crystalline Nanowire Networks. *Advanced Materials* **26**, 4875-4879, doi:10.1002/adma.201400924 (2014).

8 Gazibegovic, S. *et al.* Epitaxy of advanced nanowire quantum devices. *Nature* **548**, 434-438, doi:10.1038/nature23468 (2017).

9 Chang, W. *et al.* Hard gap in epitaxial semiconductor–superconductor nanowires. *Nature Nanotechnology* **10**, 232, doi:10.1038/nnano.2014.306 (2015).

10 Zhang, H. *et al.* Quantized Majorana conductance. *Nature* **556**, 74, doi:10.1038/nature26142 (2018).

11 Karzig, T. *et al.* Scalable designs for quasiparticle-poisoning-protected topological quantum computation with Majorana zero modes. *Physical Review B* **95**, 235305, doi:10.1103/PhysRevB.95.235305 (2017).

12 Fadaly, E. M. T. *et al.* Observation of Conductance Quantization in InSb Nanowire Networks. *Nano Letters* **17**, 6511-6515, doi:10.1021/acs.nanolett.7b00797 (2017).

13 Schmid, H. *et al.* Template-assisted selective epitaxy of III–V nanoscale devices for co-planar heterogeneous integration with Si. **106**, 233101, doi:10.1063/1.4921962 (2015).

14 Aseev, P. *et al.* Selectivity map for molecular beam epitaxy of advanced III-V quantum nanowire networks. *Nano Letters*, doi:10.1021/acs.nanolett.8b03733 (2018).

15 Krizek, F. *et al.* Field effect enhancement in buffered quantum nanowire networks. *Physical Review Materials* **2**, 093401, doi:10.1103/PhysRevMaterials.2.093401 (2018).

16 Fahed, M., Desplanque, L., Troadec, D., Patriarche, G. & Wallart, X. Selective area heteroepitaxy of GaSb on GaAs (001) for in-plane InAs nanowire achievement. *Nanotechnology* **27**, 505301, doi:10.1088/0957-4484/27/50/505301 (2016).

17 Friedl, M. *et al.* Template-Assisted Scalable Nanowire Networks. *Nano Letters* **18**, 2666-2671, doi:10.1021/acs.nanolett.8b00554 (2018).

18 Desplanque, L., Bucamp, A., Troadec, D., Patriarche, G. & Wallart, X. Selective area molecular beam epitaxy of InSb nanostructures on mismatched substrates. *Journal of Crystal Growth* **512**, 6-10, doi:10.1016/j.jcrysgro.2019.02.012 (2019).

19 Lee, J. S. *et al.* Selective-area chemical beam epitaxy of in-plane InAs one-dimensional channels grown on InP(001), InP(111)B, and InP(011) surfaces. *Physical Review Materials* **3**, 084606, doi:10.1103/PhysRevMaterials.3.084606 (2019).

20 Plugge, S., Rasmussen, A., Egger, R. & Flensberg, K. Majorana box qubits. *New Journal of Physics* **19**, doi:10.1088/1367-2630/aa54e1 (2017).

21 Aasen, D. *et al.* Milestones Toward Majorana-Based Quantum Computing. *Physical Review X* **6**, 031016, doi:10.1103/PhysRevX.6.031016 (2016).

22 Straumanis, M. E. & Kim, C. D. Lattice Parameters, Thermal Expansion Coefficients, Phase Width, and Perfection of the Structure of GaSb and InSb. **36**, 3822-3825, doi:10.1063/1.1713955 (1965).

23 Gül, Ö. *et al.* Ballistic Majorana nanowire devices. *Nature Nanotechnology* **13**, 192-197, doi:10.1038/s41565-017-0032-8 (2018).

24 Aseev, P. *et al.* Ballistic InSb Nanowires and Networks via Metal-Sown Selective Area Growth. *Nano Letters* **19**, 9102-9111, doi:10.1021/acs.nanolett.9b04265 (2019).

25 Borg, M. B. & Wernersson, L.-E. Synthesis and properties of antimonide nanowires. *Nanotechnology* **24**, 202001, doi:10.1088/0957-4484/24/20/202001 (2013).

26 Oh, J. E., Bhattacharya, P. K., Chen, Y. C. & Tsukamoto, S. Molecular-beam epitaxial growth of high-quality InSb on InP and GaAs substrates. **66**, 3618-3621, doi:10.1063/1.344069 (1989).

27 Schroer, M. D. & Petta, J. R. Correlating the Nanostructure and Electronic Properties of InAs Nanowires. *Nano Letters* **10**, 1618-1622, doi:10.1021/nl904053j (2010).

28 Badawy, G. *et al.* High Mobility Stemless InSb Nanowires. *Nano Letters* **19**, 3575-3582, doi:10.1021/acs.nanolett.9b00545 (2019).

29 de Moor, M. W. A. *et al.* Electric field tunable superconductor-semiconductor coupling in Majorana nanowires. *New Journal of Physics* **20**, 103049, doi:10.1088/1367-2630/aae61d (2018).

30 Vaitiekėnas, S., Deng, M. T., Nygård, J., Krogstrup, P. & Marcus, C. M. Effective g Factor of Subgap States in Hybrid Nanowires. *Physical Review Letters* **121**, 037703, doi:10.1103/PhysRevLett.121.037703 (2018).

31 Mikkelsen, A. E. G., Kotetes, P., Krogstrup, P. & Flensberg, K. Hybridization at Superconductor-Semiconductor Interfaces. *Physical Review X* **8**, 031040, doi:10.1103/PhysRevX.8.031040 (2018).

32 Antipov, A. E. *et al.* Effects of Gate-Induced Electric Fields on Semiconductor Majorana Nanowires. *Physical Review X* **8**, 031041, doi:10.1103/PhysRevX.8.031041 (2018).

33 Woods, B. D., Stanescu, T. D. & Das Sarma, S. Effective theory approach to the Schrödinger-Poisson problem in semiconductor Majorana devices. *Physical Review B* **98**, 035428, doi:10.1103/PhysRevB.98.035428 (2018).

34 Vijay, S. & Fu, L. Teleportation-based quantum information processing with Majorana zero modes. *Physical Review B* **94**, 235446, doi:10.1103/PhysRevB.94.235446 (2016).

35 Albrecht, S. M. *et al.* Exponential protection of zero modes in Majorana islands. *Nature* **531**, 206, doi:10.1038/nature17162 (2016).

36 Das Sarma, S., Sau, J. D. & Stanescu, T. D. Splitting of the zero-bias conductance peak as smoking gun evidence for the existence of the Majorana mode in a superconductor-semiconductor nanowire. *Physical Review B* **86**, 220506, doi:10.1103/PhysRevB.86.220506 (2012).

37 Chiu, C.-K., Sau, J. D. & Das Sarma, S. Conductance of a superconducting Coulomb-blockaded Majorana nanowire. *Physical Review B* **96**, 054504, doi:10.1103/PhysRevB.96.054504 (2017).

38 Shen, J. *et al.* Parity transitions in the superconducting ground state of hybrid InSb–Al Coulomb islands. *Nature Communications* **9**, 4801, doi:10.1038/s41467-018-07279-7 (2018).

39 Cao, Z. *et al.* Decays of Majorana or Andreev Oscillations Induced by Steplike Spin-Orbit Coupling. *Physical Review Letters* **122**, 147701, doi:10.1103/PhysRevLett.122.147701 (2019).

40 Zhang, H., Liu, D. E., Wimmer, M. & Kouwenhoven, L. P. Next steps of quantum transport in Majorana nanowire devices. *Nature Communications* **10**, 5128, doi:10.1038/s41467-019-13133-1 (2019).

41 Thelander, C., Caroff, P., Plissard, S., Dey, A. W. & Dick, K. A. Effects of Crystal Phase Mixing on the Electrical Properties of InAs Nanowires. *Nano Letters* **11**, 2424-2429, doi:10.1021/nl2008339 (2011).

42 Lee, E. J. H. *et al.* Spin-resolved Andreev levels and parity crossings in hybrid superconductor–semiconductor nanostructures. *Nature Nanotechnology* **9**, 79, doi:10.1038/nnano.2013.267 (2013).

43 Kammhuber, J. *et al.* Conductance Quantization at Zero Magnetic Field in InSb Nanowires. *Nano Letters* **16**, 3482-3486, doi:10.1021/acs.nanolett.6b00051 (2016).

Chapter 6

Universal Platform for Scalable Semiconductor-Superconductor Nanowire Networks

Based on Jason Jung, Roy L.M. Op het Veld et al., Universal platform for scalable semiconductor-superconductor nanowire networks, Under review

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Abstract

Semiconductor-superconductor hybrids are commonly used in research on topological quantum computation. Traditionally, top-down approaches involving dry or wet etching are used to the define the device geometry. These often-aggressive processes bear the risk of causing damage to material surfaces, giving rise to scattering sites particularly problematic for quantum applications. Here, we propose a method that maintains the flexibility and scalability of selective area grown nanowire networks while omitting the necessity of etching to create hybrid segments within the network. Instead, it takes advantage of directional growth methods and uses bottom-up grown InP structures as shadowing objects to obtain selective metal deposition. The ability to lithographically define the position and area of these objects, and to grow a predefined height, ensures precise control of the shadowed region. We demonstrate the approach by growing InSb nanowire networks with well-defined Al and Pb islands. Cross-section cuts of the nanowires reveal a sharp, oxide-free interface between semiconductor and superconductor. By growing InP structures on both sides of in-plane nanowires, a combination of Pt and Pb can be shadow deposited, enabling scalable and reproducible in-situ device fabrication. The semiconductor-superconductor nanostructures resulting from this approach are at the forefront of material development for Majorana based experiments towards topological quantum computation.

6.1 Introduction

Material science is a major impetus for developments in topological quantum computation. This active research field aims at using non-Abelian anyons, predicted to provide a basis for naturally fault-tolerant quantum computing.[1,2] A major step towards the first practical realization was the discovery that these quasiparticles can form in a one-dimensional semiconductor with strong spin-orbit Rashba interaction, coupled to a conventional s-wave superconductor.[3-5] This system is predicted to undergo a topological phase transition under a suitable magnetic field, with non-Abelian quasiparticles emerging in the form of Majorana bound states at the ends of the heterostructure.[6] Several proposals have emerged on how these heterostructures can be used to build a fully functioning topological qubit, most of which are based on branched nanowire networks with topological segments.[7,8] This sets the fabrication of these networks as one of the major challenges for material scientists in the field.

In conventional semiconductor microfabrication, top-down approaches involving dry or wet etching are used to define device geometries.[9] These often-aggressive processes bear the risk of causing etching-damage to the semiconductor surface, giving rise to scattering sites. This is particularly problematic for quantum applications, where these scattering sites negatively impact carrier mobility and coherence length. The preferred alternative is the bottom-up approach, in which the device structure is built from its individual atoms self-arranging into the desired pattern. A prototype of bottom-up synthesis is the growth of out-of-plane nanowires. The small contact area allows monocrystalline nanowire growth with pristine crystal quality and side facets, even on highly lattice-mismatched substrates. This can lead to ballistic transport over several microns and has been used in many successful Majorana based experiments.[10-17] The downside of out-of-plane synthesis is the limited geometric flexibility. Elaborate fabrication methods allow the synthesis of simple networks and have yielded impressive transport results.[18] Even so, there is no straightforward way to expand them to more complex structures. Recently, a more scalable approach was developed based on the selective-area growth technique (SAG). In this method, an amorphous mask is deposited on the growth substrate into which the network

pattern is etched. The right growth conditions confine the subsequent nanowire synthesis to the mask openings, allowing for scalable and highly flexible growth of complex in-plane selective area networks.[19-21] But the difficulty of creating semiconductor-superconductor segments remains. Until now, Al was subsequently evaporated and selectively wet etched, a method frequently used on out-of-plane nanowires.[19,22] Experiments show however, that even highly selective etchants inflict damage on the semiconductor surface, lowering the device performance.[23,24]

The alternative method proposed here omits the necessity of etching. Instead, it takes advantage of directional growth methods and uses bottom-up selective area grown structures as shadowing objects to obtain selective deposition. Similar concepts have been successfully used on out-of-plane nanowires but are limited in flexibility and achievable complexity.[18,23-25] In this article we present the integration of shadow deposition with SAG, allowing for a reproducible and scalable bottom-up approach. We demonstrate the growth of branched, in-plane InSb nanowire networks and full control over number, size, and position of its superconducting segments. Furthermore, our method is suitable for the directional deposition of any material. To show this, we epitaxially grow thin films of Al, the most established superconductor choice within the field, as well as Pb. The latter possesses the highest bulk critical field and temperature of all elemental type-I superconductors, and has shown high promise in recent experiments.[26] Taking the same approach to shadow networks from multiple sides allows for the combination of several shadow deposited materials. We demonstrate this through several examples, including a full device consisting of an InSb nanowire, Pb islands, and shadow deposited Pt leads. Altogether, this method provides an ideal basis for the next wave of Majorana based experiments.

6.2 Shadow deposition

Figure 6.1 illustrates the principle of the technique. As an example, we show the fabrication of an InSb Aharonov-Bohm interferometer with an embedded Al island. This type of device has raised significant interest due to its predicted non-local phase-coherent electron transfer.[27-29] The schematics in Figure 6.1a-e give an overview of the fabrication steps. The starting point is a semi-insulating InP (111)A substrate covered by a 20 nm amorphous Si_xN_y mask. Lithographically defined openings are dry etched into the mask along the $\langle 10\bar{1} \rangle$ and $\langle 11\bar{2} \rangle$ crystal directions, allowing access to the underlying crystalline substrate. The subsequent metalorganic vapor-phase homoepitaxy forms InP nanostructures, herein referred to as *walls*.[30] Confining the mask openings to these crystal directions allows for high control over the lateral dimensions of the walls (see Figure 6.5). A second Si_xN_y mask is deposited, and the same method is used to first etch the mask opening and then selectively grow the InSb nanowire network using MOVPE.[19,20] The initially grown InP walls act as shadowing objects during the subsequent superconductor deposition and allow for selective growth on the InSb network.

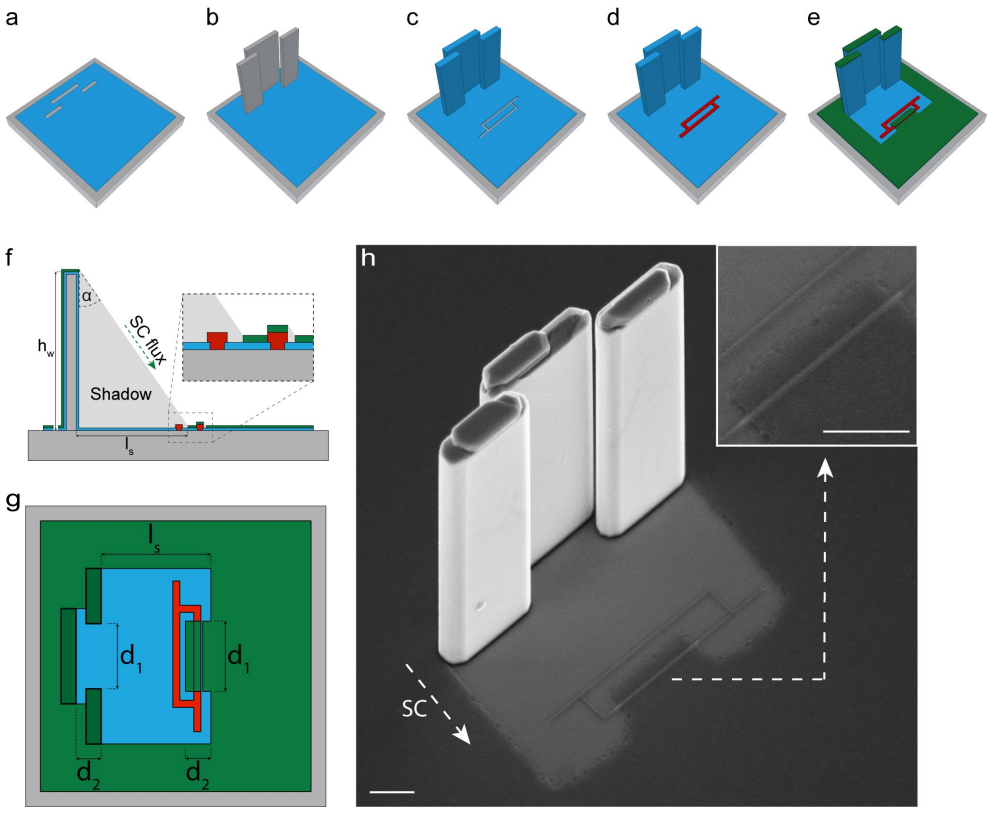


Figure 6.1 | Shadow deposit networks using InP walls.
a-e: Illustration of the growth principle. Lithographically defined openings are etched into a Si_xN_y mask (light blue) on an InP (111)A substrate (grey), followed by selective-area growth of InP walls (grey). The same approach is used to selectively grow the semiconductor (red) network after depositing and etching a second mask. The InP walls act as shadowing objects during the directional superconductor (green) deposition to allow its selective growth on the nanowire network. **f:** A cross-section of the design shows the dependency of the shadow length l_s on wall height h and deposition angle α. The inset shows a zoom-in of the partially covered network. **g:** Top-view schematic, indicating the design flexibility of the approach due to the precise control over position and size of walls and network. **h:** Tilt-view SEM image of an in-plane InSb nanowire network with a superconducting Al island created through shadow deposition using InP walls. The arrow indicates the direction of the superconductor flux (SC) during deposition. The Al is deposited at α = 25°. Scale bars are 500 nm.

The angle α under which the superconductor is deposited, and the height h of the InP nanostructure determine the length $l_s = h\sin(\alpha)$ of the shadow, as depicted in Figure 6.1f. The ability to lithographically define the lateral dimensions and position of the InP nanostructures and network, combined with the control of the wall height during MOVPE growth, gives precise control over the shadowed region. This is indicated in Figure 6.1g, where the distances d_1 and d_2 between the nanostructures define the length and position of the metal island, ensuring that the shadow falls between the two arms of the interferometer. A scanning electron microscopy (SEM) image of a device created using this technique is shown in Figure 6.1h. The result is a single-crystalline InSb nanowire interferometer with a well-defined ~1.2 µm long Al island on one arm. In addition to this, many other networks were fabricated to demonstrate the flexibility, accuracy, and scalability of the approach (see Figure 6.6 and Figure 6.7). This includes the basis of a proposed four-qubit device consisting of twelve superconducting segments connected into a branched network.[8]

A transmission electron microscopy (TEM) image of the cross-section of the Aharonov-Bohm interferometer is shown in Figure 6.2a. The partial shadowing of the network is visible, with a ~8 nm thick Al film covering only the right nanowire. This is confirmed through an energy-dispersive x-ray spectroscopy (EDX) elemental mapping of the same region, as displayed in Figure 6.2b. A more detailed EDX mapping of the right wire in Figure 6.2c shows an uninterrupted Al film from the top of the nanowire to the Si_xN_y mask. This allows to contact the superconducting segment of the network without fabricating directly on the nanowire itself, thereby preventing subsequent damage. Other designs specifically require disconnecting the metal layer on the network from the layer on the mask to electrically isolate superconducting segments within the network. This can be achieved by growing the nanowire tall enough to enable self-shadowing (see Figure 6.8).

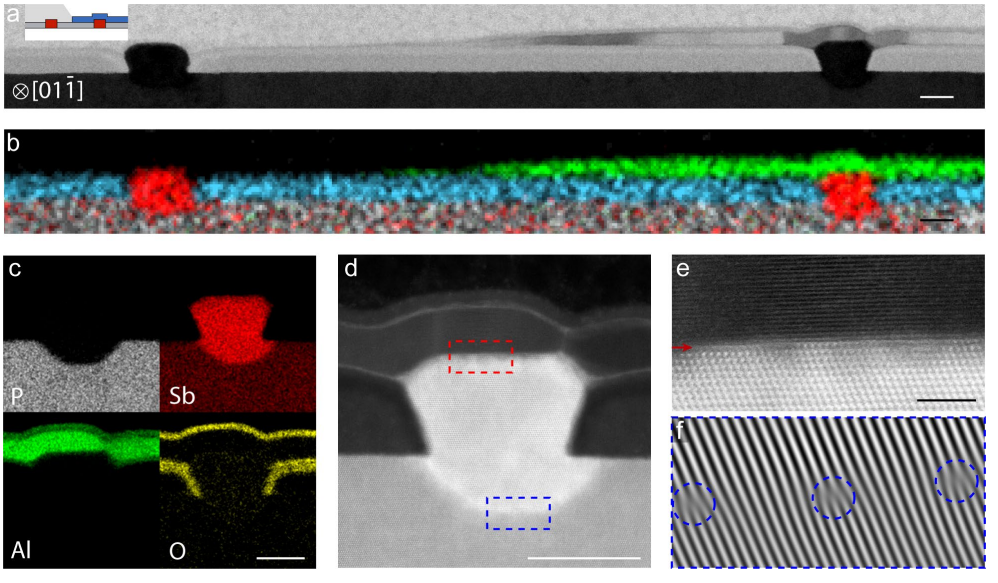


Figure 6.2 | Partial shadowing.
a: Transmission electron micrograph from a cross-section cut of the device shown in Figure 6.1. The partial shadowing of the network is visible with only the right wire being covered by the Al superconductor. The inset refers back to the schematic of Figure 6.1f. **b:** EDX elemental mapping of the same region with Sb (red), Si (light blue), P (grey) and Al (green). **c:** EDX elemental mapping of P (grey), Sb (red), Al (green), and oxygen (yellow) of the covered nanowire showing that the Al layer is continuous from the nanowire to the mask. **d:** HAADF STEM image of the covered nanowire. **e:** High resolution HAADF STEM of the region marked with a red rectangle in (**d**) depicting a uniform, oxide free InSb/Al interface. **f:** IFFT of the region marked with a blue rectangle in (**d**) reveals the atomic columns at the InP substrate to InSb nanowire interface. The lattice mismatch between InP and InSb is compensated by misfit dislocations directly at the interface (blue circles). Scale bars are 20 nm (**a-d**) and 3 nm (**e**).

A high-angle annular dark-field (HAADF) scanning TEM image of the covered nanowire is shown in Figure 6.2d. A gentle removal of the native InSb oxide using a directional flow of atomic hydrogen radicals prior to the superconductor deposition ensures the clean semiconductor-superconductor interface,[31] as seen in Figure 6.2e. A crucial requirement for the ability to grow InP by selective-area-epitaxy is the polarity of the substrate. As a consequence, this is the first reported growth of in-plane InSb nanowires on InP (111)A (see Figure 6.9), with the 10.4% lattice mismatch between the substrate and nanowire compensated by misfit dislocations directly at the interface.

These dislocations can be revealed through an inverse fast Fourier transformation (IFFT) of the TEM image, as depicted in Figure 6.2f.

6.3 Pb deposition and characterization

The presented technique is not limited to the use of Al. Any directionally deposited material can be shadowed. One particularly promising superconductor alternative is Pb, due to its expected large superconducting gap, and high critical field and critical temperature.[26] The SEM micrographs in Figure 6.3a-b show an in-plane InSb nanowire with ~22 nm thick shadow deposited Pb forming two superconducting islands. This design is based on an experiment suggested to investigate Majorana fusion rules.[32,33] The film growth is governed by an interplay of thermodynamics and kinetics. It is therefore highly dependent on the crystallography of the underlying layer. This is exemplified by the Pb forming a smooth crystalline closed film on the crystalline InSb nanowire, while exhibiting a still continuous but rougher poly-crystalline morphology on the amorphous mask, with crevices at the grain boundaries. The morphology is determined by the minimization of the overall excess energy.[34] Since Pb adatoms are more strongly bound to each other than to the Si_xN_y mask they follow the Vollmer-Weber growth mode. In this mode, three-dimensional islands nucleate directly on the surface after reaching a critical number of adatoms. Longer deposition increases the island size until they coalesce and percolate, eventually forming a closed film. Figure 6.3c demonstrates the formation of the closed film with increasing film thickness. Creating a continuous superconducting layer reaching from the nanowire to the mask can be crucial for certain experiments, as previously indicated in the context of the Aharonov-Bohm interferometer. A nanowire with a single connected superconducting island (see Figure 6.7), could for instance serve as a material basis for three-terminal nonlocal conductance measurements.[35,36] An EDX elemental mapping of a cross-section cut of a comparable deposition is shown in Figure 6.3d. It exhibits a continuous Pb layer with a sharp oxide free interface to the nanowire, as visible in the HAADF scanning TEM image depicted in Figure 6.3e. The Pb crystal is expected to orient itself to the bi-crystal interface with the smallest bulk residual mismatch, while simultaneously maintaining a low interfacial domain. This is confirmed by an IFFT in Figure 6.3f that reveals the 3:4 ratio of

the epitaxially matched InSb/Pb interface with a bulk residual mismatch of 1.9%.

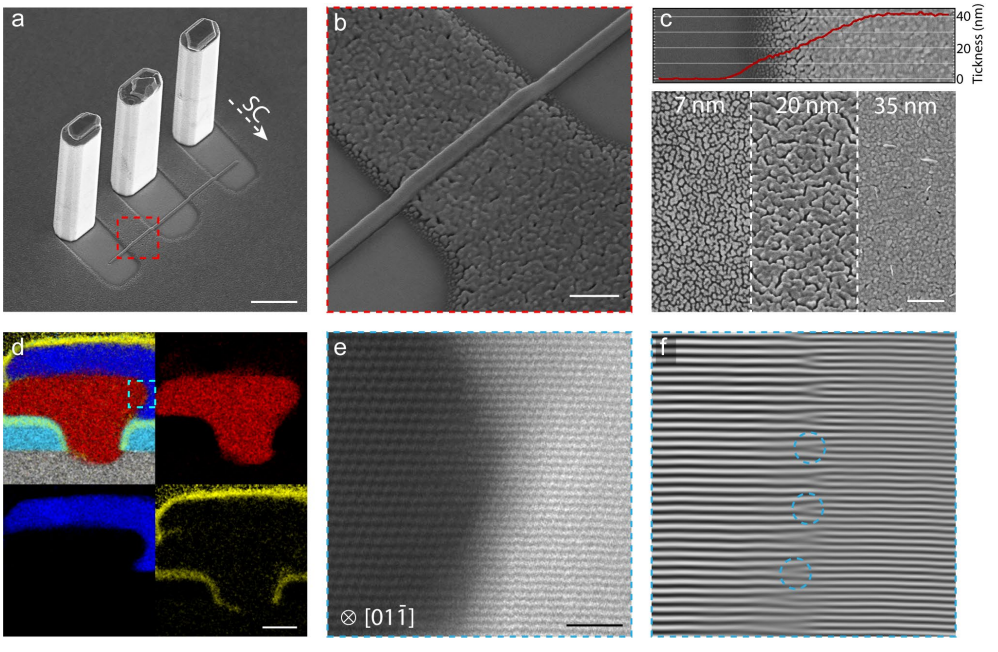


Figure 6.3 | Epitaxial Pb on InSb.
a: Tilt-view SEM image of an InSb nanowire with two shadow deposited ~22 nm thick Pb islands. The arrow indicates the direction of the superconductor flux during deposition. The Pb is deposited at $\alpha = 25°$. Scale bar is 1 µm. **b:** Close up of the left island showing a smooth, closed Pb film on the crystalline InSb nanowire and a rough poly-crystalline topography on the amorphous Si_xN_y mask. Scale bar is 200 nm. **c:** Layer morphology of Pb on the Si_xN_y mask. With increasing thickness, the film transitions from separate islands to a continuous rugged layer, to eventually forming a closed film. Scale bar is 200 nm. **d:** EDX elemental mapping of a cross-section cut imaged along the $[1\bar{1}0]$ zone axis with P (grey), Sb (red), Pb (blue), Si (light blue) and oxygen (yellow). Scale bar is 20 nm. **e:** HAADF scanning TEM image of the region marked with a blue rectangle in panel (**d**) showing the oxide free InSb/Pb interface. Scale bar is 3 nm. **f:** IFFT of the same region reveals the 3:4 ratio of the epitaxially aligned InSb/Pb interface with an expected bulk residual mismatch of 1.9 %. Three exemplary edge dislocations are indicated by cyan circles.

6.4 Two-sided metal deposition

Finally, the shadowing approach is taken further by placing InP walls on both sides of the nanowire, allowing for the combination of multiple shadow deposited materials. An example to showcase the principle is sketched in **Figure 6.4a**. Here, the Pb island device introduced in **Figure 6.3** is expanded by shadow depositing Pt on both ends of the nanowire. This creates a junction between normal metal, semiconductor, and superconductor, which reduces the steps for fabrication processing after the sensitive semiconductor-superconductor interface is created. A SEM micrograph of such a device is shown in **Figure 6.4b-c**. It exhibits sharp shadows with a clear separation between the Pt and Pb covered segments and the bare InSb nanowire. The dimensions of these segments can be accurately controlled through the position of the InP walls. Some applications require the bare InSb segments to be kept small in order to avoid the unintentional formation of quantum dots.[12,37] To validate the accuracy of this approach, a Pt/Pb junction is created with a bare InSb segment of a lateral dimension as short as ~15 nm (see **Figure 6.10**). The EDX analysis of the device is shown in **Figure 6.4d**, with the Si signal indicating the etched mask openings for walls and nanowire. The detected Pt and Pb signal reveal the deposition shadows and their relative position to the nanowire (also see **Figure 6.11** for the combination of Al and Pt). Next to combining normal metals with superconductors, this approach could also be used to combine two different superconductors for sensitive tunnel probing of the density of states (see **Figure 6.12**).[38,39] Shadow deposition is currently the only known way to create combinations of ultra-high vacuum deposited superconductors without involving processing. Alternatives would require either the ability to selectively etch one superconductor without damaging the other or the use of lift-off processes, leading to potential material contamination.

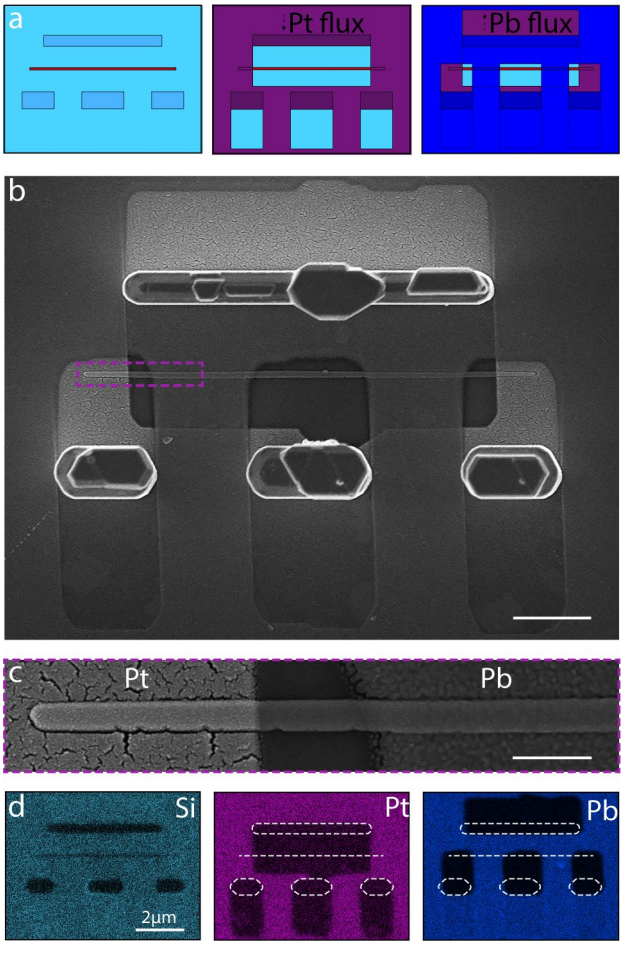


Figure 6.4 | Double-sided shadow deposition.
a: Schematic of double-sided shadow deposition. InP walls are placed on both sides of the nanowire. This allows for the consecutive shadow deposition of ~10 nm Pt at α = 35° and ~22 nm Pb at α = 25°. **b:** Top-view SEM micrograph depicting the resulting InSb nanowire with two superconducting Pb islands and normal Pt segments on both ends of the wire. Scale bar is 1 µm. **c:** Close-up of the normal-semiconductor-superconductor junction marked by a purple rectangle in panel (**b**). It shows a sharp shadow with clear separation of the Pt and Pb covered segments by the bare InSb nanowire. Scale bar is 200 nm. **d:** SEM-EDX elemental mapping of the full device. The Si (light blue) signal shows the etched wall and nanowire openings. The Pt (purple) and Pb (blue) signals show the shadow deposited metals. Scale bar is 2 µm.

6.5 Conclusion

In conclusion, we demonstrate selective shadow deposition to in-plane nanowire networks. The technique is fully based on SAG, making it highly flexible, accurate, reproducible, and scalable. Fully omitting etching of the networks avoids damaging the semiconductor surface, which would lower the device performance. Additionally, it allows for the use of materials to which no selective etchant is currently known. The approach is used for the selective deposition of Al, as well as the first reported growth of epitaxial Pb on InSb nanowires. Shadowing from two sides permits for the combination of multiple materials. This is exemplified in two ways: First, by combining Al as well as Pb with Pt for a complete device fabrication without processing of the nanowire, and second through the combination of Pb with Al for density of states (DOS) tunnel probing. We believe this approach presents an ideal large-scale platform for the next wave of Majorana based experiments.

6.6 Appendix

6.6.1 Methods

Substrate fabrication

Fabrication of substrates for SAG shadow deposition is a three-step lithography process.

- Markers: 70 nm Si_xN_y layer is deposited by plasma-enhanced chemical vapour deposition (PECVD) on an undoped semi-insulating (111)A InP substrate. AR-P 6200.13 resist is spun at 2000 rpm, baked at 150 °C for 1 min, rinsed in IPA for 30 s, blow dried. Electron-beam lithography (EBL) is used to write marker patterns and developed in AR 600-546 for 1 min. The pattern is transferred into the mask by reactive ion etching (RIE) using CHF_3 with added O_2. 5 minutes of 50 W O_2 plasma ashing is used to clean the wafer of polymers. Inductively coupled plasma etching (ICP) using CF_4/H_2 etches the marker pattern ~1.5 µm into the substrate. A 3 min buffered hydrofluoric (BHF) etch (NH_4F:HF = 7:1) removes the mask.
- InP: 20 nm Si_xN_y by PECVD. AR-P 6200.13 resist at 4000 rpm, baked at 150 °C for 60 s. The InP wall openings are written by EBL and developed in AR 600-546 for 60 s, rinse in IPA for 30 s, blow dry. RIE, using pure CHF_3 RIE to transfer the pattern into the Si_xN_y mask. Overnight AR 600-71 stripper to remove the resist, ultrasonic rinse in IPA for 30 s, blow dry. O_2 plasma ashing to clean the substrate. A phosphoric acid wet etch (H_2O:H_3PO_4 = 10:1) removes the native substrate oxides, after which the InP walls are grown using a horizontal flow MOVPE reactor. Subsequently the Si_xN_y mask is removed by a 3 min BHF etch.
- InSb: Analogous to InP processing. 20 nm Si_xN_y by PECVD. AR-P 6200.04 at 2000 rpm, baked at 150 °C for 60 s. The InSb network openings are written by EBL and developed in AR 600-546 for 60 s, rinse in IPA for 30 s, blow dry. CHF_3 RIE to transfer the pattern. Overnight AR 600-71 stripper to remove the resist, ultrasonic rinse in IPA for 30 s, blow dry. O_2 plasma ashing to clean the substrate. A phosphoric acid wet etch (H_2O:H_3PO_4 = 10:1) removes the native substrate oxides, after which the InSb networks are grown using MOVPE.

InP homoepitaxy

Growth takes place in an Aixtron 200 MOVPE horizontal flow reactor with infrared lamp heating. The InP walls are grown at 700 °C using tri-methyl-indium (TMIn) and phosphine (PH_3) with precursor molar fractions Xi (TMIn) = 3.5×10^{-6} and Xi (PH_3) = 1.33×10^{-2}, for 20-50 minutes depending on the desired wall height. The reactor pressure is 100 mbar, with a total flow of 12000 sccm, using H_2 as the carrier gas.

InSb heteroepitaxy

The same reactor is utilised for the InSb growth. An annealing step under phosphine (PH_3) overpressure at 570 °C is used for surface reconstruction of the etched openings and to remove possible oxide residuals from the exposed substrate surface. InSb nanowires were grown at 470 °C using tri-methyl-indium (TMIn) and tri-methyl-antimony (TMSb) with precursor molar fractions Xi (TMIn) = 8.4×10^{-8} and Xi (TMSb) = 3.7×10^{-3}, for 20-40 min depending on the network size and desired nanowire height. For both processes, the reactor pressure is 50 mbar, with a total flow of 12000/6000 sccm, respectively, and H_2 as the carrier gas.

Metal deposition

Nanowire networks are transferred ex-situ to a molecular beam epitaxy (MBE) chamber. An atomic hydrogen clean (20 min under continuous rotation, 400 °C thermocouple, 5×10^{-6} mbar chamber pressure) is performed to remove the native oxide from the InSb nanowire surface. Subsequently, samples are cooled down to about 110 K by active liquid-nitrogen cooling. Careful alignment of nanowires relative to the metal source is important for well-controlled shadowing of the networks. Al and Pt are deposited at a growth rate of ~5.5 Å min^{-1}, Pb at ~24 Å min^{-1}. Immediately after growth, samples are transferred in-situ to an MBE chamber equipped with an ultrahigh-purity O_2 source where they are exposed to 10^{-4} mbar of O_2 for 15 min. This step is important to form an oxide layer to 'freeze-in' the metal film. This prevents it from diffusing, while the sample warms up to room temperature in ultrahigh vacuum.

Focused Ion Beam TEM lamella preparation

TEM lamellas are prepared in a FEI Nova Nanolab 600i. First, an electron-beam induced C and Pt layer are deposited to minimize the ion beam damage in the following step. After removal of the InP walls using a nanomanipulator, the networks are embedded by an ion-beam induced Pt deposition used as a sacrificial layer for the thinning procedure. A TEM lamella is cut and transferred to a half-moon TEM grid for thinning. Finally, thin windows are cut into the lamella using Ga-ion milling in steps at 30 kV, 16 kV and finally 5 kV to create windows with a thickness of less than 100 nm, while minimizing damage induced by the ion beam. It should be noted, that particularly Pb deposited on InSb nanowires suffered from heavy interface intermixing during the thinning procedure. Ion beam milling under cryogenic conditions could possibly solve this.

TEM studies

TEM studies were performed using a probe-corrected JEOL ARM 200F, equipped with a 100 mm^2 Centurio SDD Energy dispersive X-ray spectroscopy detector. Misfit dislocations at the InP-InSb interface were visualised by creating an FFT of an atomic resolution image, applying a filter to only include one set of (111) spots and then creating an inverse FFT.

6.6.2 Supporting figures

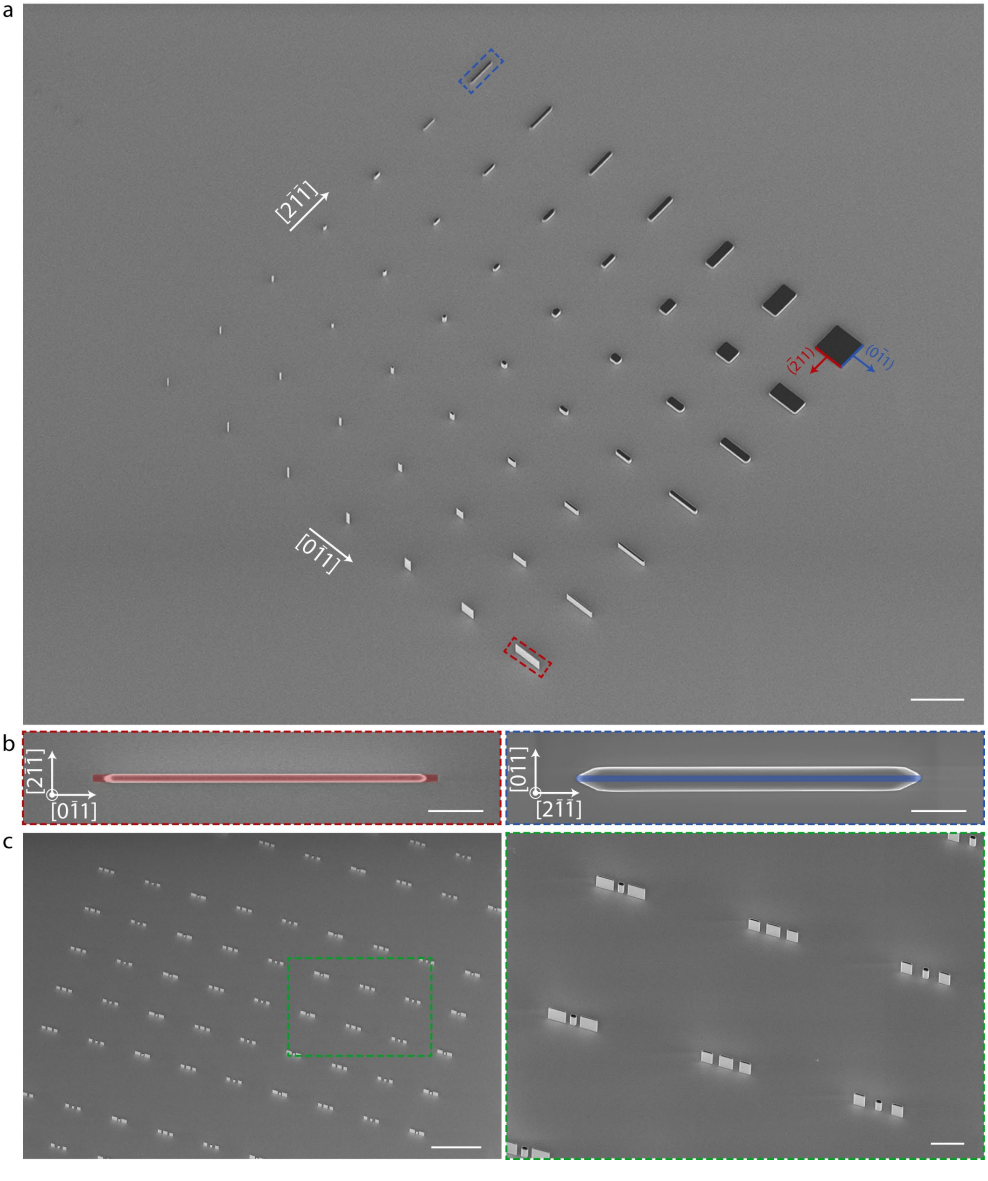


Figure 6.5 | Control over InP wall growth.
a: Tilted SEM micrograph of an array of InP walls. Mask openings patterned along the $\langle 0\bar{1}1\rangle$ and $\langle 2\bar{1}\bar{1}\rangle$ crystal directions form stable structures bound by $(\bar{2}11)$ and $(0\bar{1}1)$ side facets. The walls are grown in a variety of lateral dimensions ranging from 100 nm - 6 µm. Scale bar is 20 µm. **b:** Top-view SEM micrographs of InP walls grown along the $[0\bar{1}1]$ and $[2\bar{1}\bar{1}]$ in-plane direction

marked in panel (**a**). We note that the former is thinner, reflecting a preferential formation of $(0\bar{1}1)$ over $(2\bar{1}\bar{1})$ facets. This is likely a result of a lower surface energy of the former facet dictated by the V/III precursor ratio and growth temperature (see methods Section 6.6.1).[30] The coloured area indicates the underlying etched mask opening. Scale bars are 1 µm. **c**: Large array of InP shadow walls with an enlarged image of the area marked in green. Along one axis, the length of the walls is varied demonstrating the flexibility of the approach. Along the other axis, a copy of the same design was grown indicating the reproducibility of the approach. Scale bars are 20 µm and 4 µm, respectively.

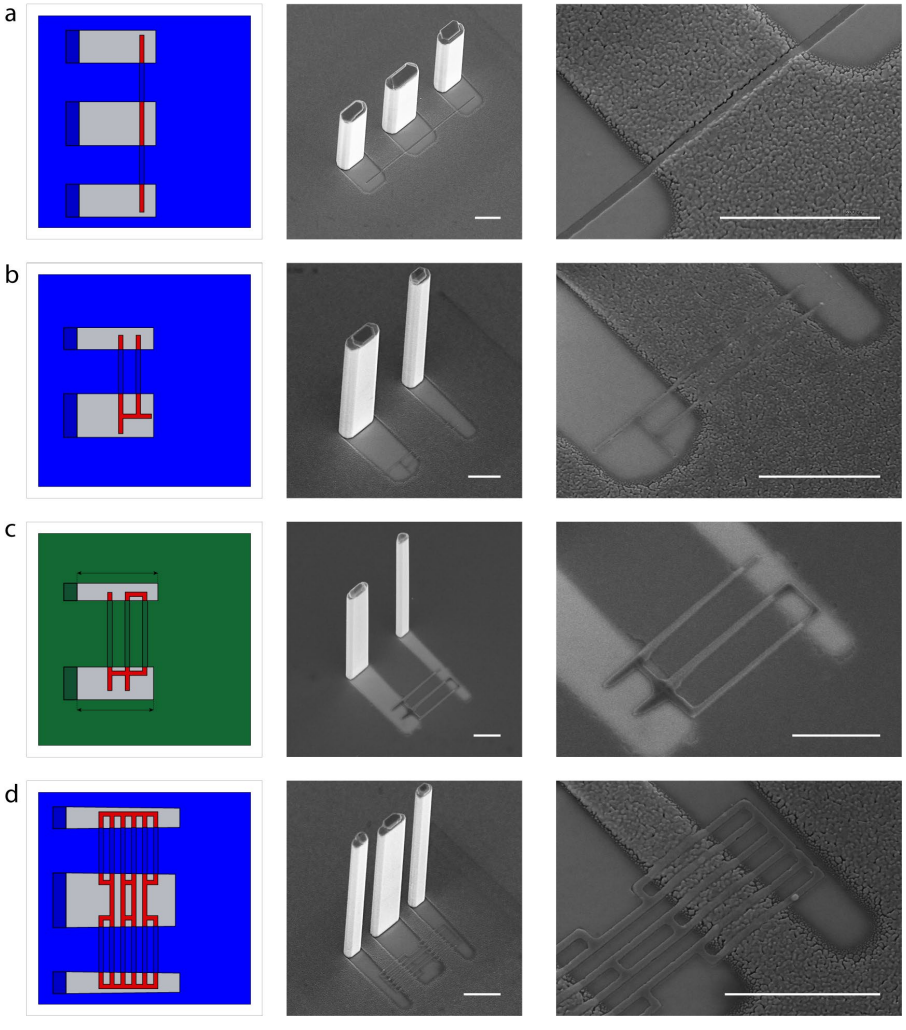
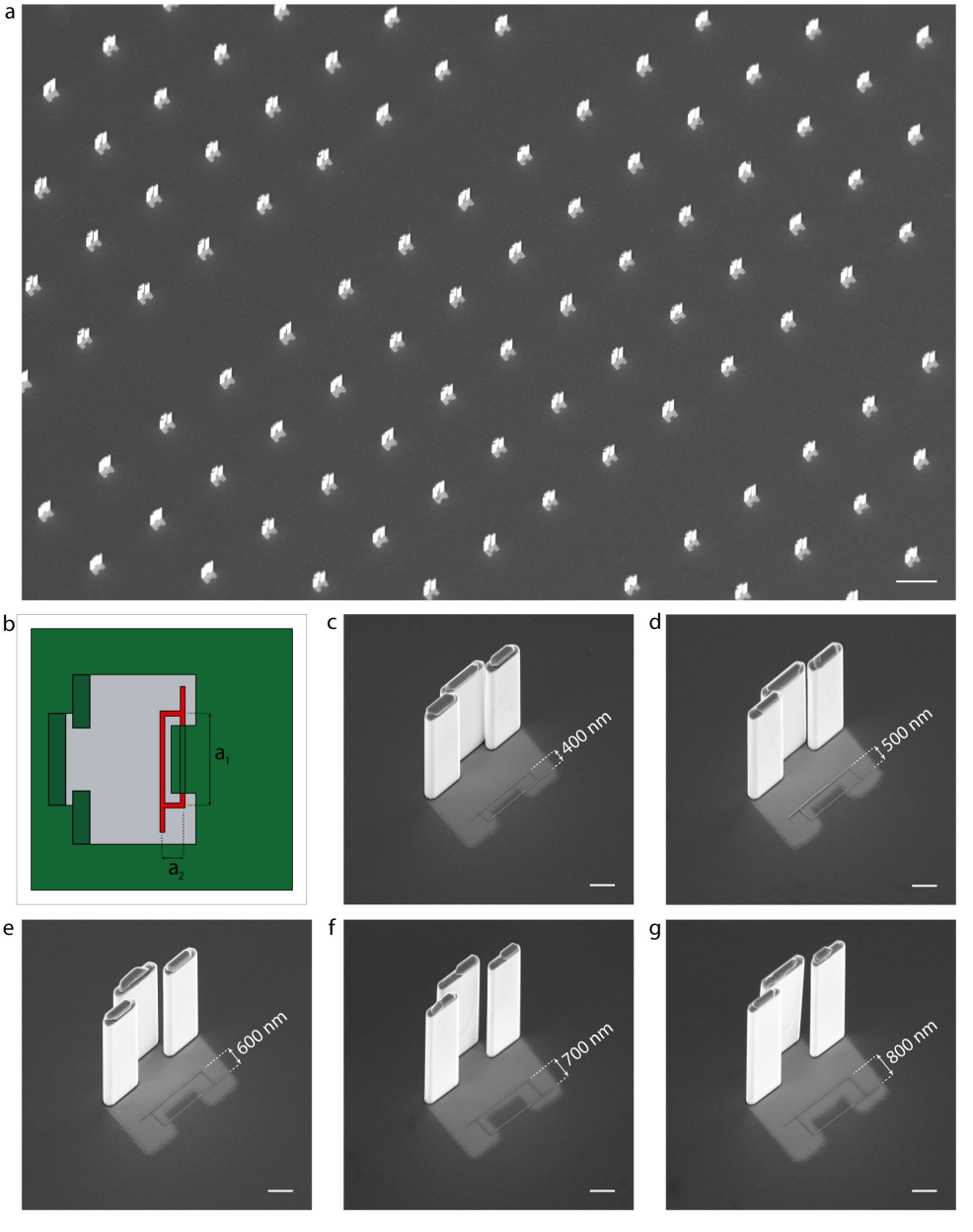


Figure 6.6 | Design flexibility.
a-d: Top-view schematic overview, accompanying tilt-view SEM and close-up SEM images of an InSb semiconductor network with shadow-deposited superconducting islands for various designs. **a:** Single nanowire with double superconducting (Pb) island design to investigate Majorana fusion rules.[33,40] The wire is substantially lower than the one shown in the main text, leading to a continuous superconducting film from wire to mask. **b:** Network based on Majorana teleportation experiments with two superconducting islands (Pb) on two separate network arms.[8] **c:** Single-qubit nanowire network design with superconducting islands (Al) on all three arms.[8] **d:** Four-qubit design with superconducting islands (Pb) on all horizontal arms, demonstrating the scalability of the growth technique.[8] Scale bars are 1 µm and 200 nm (tilt-view and close-up, respectively).



6.7 | Scalability and accuracy.
a: Tilted SEM micrograph of an array of shadow-deposited Aharonov-Bohm interferometer. Scale bar is 10 µm. **b:** Illustration of the design indicating the length of the two arms a_1 and a_2. **c-g:** A series of devices taken from the sample shown in panel a. The length a_1 is kept constant at 2 µm, while varying a_2 from 400 - 800 nm. The network shown in panel (**c**) has the same design as **Figure 6.1h** but is not the same device. Scale bars are 500 nm.

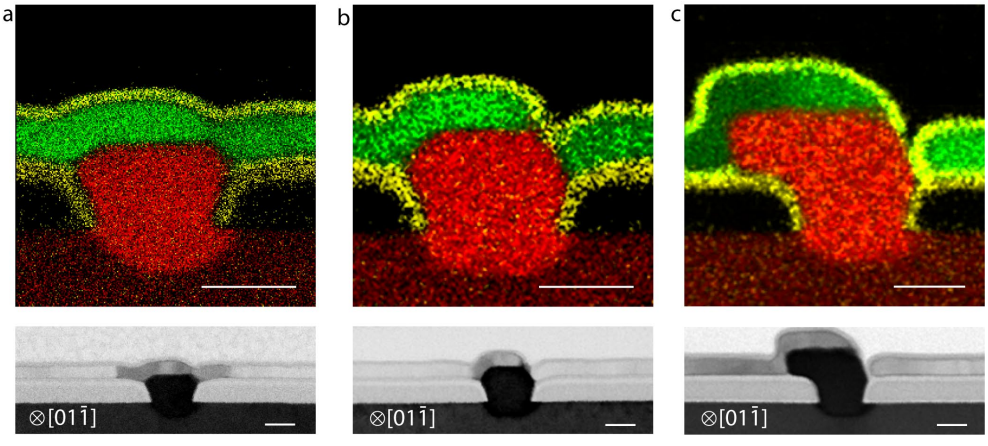


Figure 6.8 | Self-shadowing.
a: EDX elemental mapping of a cross-section of an InSb nanowire (Sb, red) with a superconducting thin film of aluminium (green) deposited on top. In this case, the nanowire is grown to approximately the height of the mask, leading to a continuous aluminium film on both sides of the nanowire to the mask. No oxide (yellow) interruptions are present in the aluminium layer. The HAADF scanning TEM image below shows the continuous film on the mask. **b:** The nanowire is grown slightly higher than the mask, allowing for self-shadowing during the superconductor deposition under an angle. In this case, two separate aluminium segments are created, while both still connect to the wire with an oxide-free interface. This creates the smallest shadow practically possible. **c:** The nanowire grows out of the mask and the aluminium film is interrupted. The self-shadowing causes the Al film on the right side of the nanowire to completely disconnect from the nanowire. A thin oxide layer between the InSb and Al further electrically isolates the Al from the nanowire. Scale bars are 20 nm.

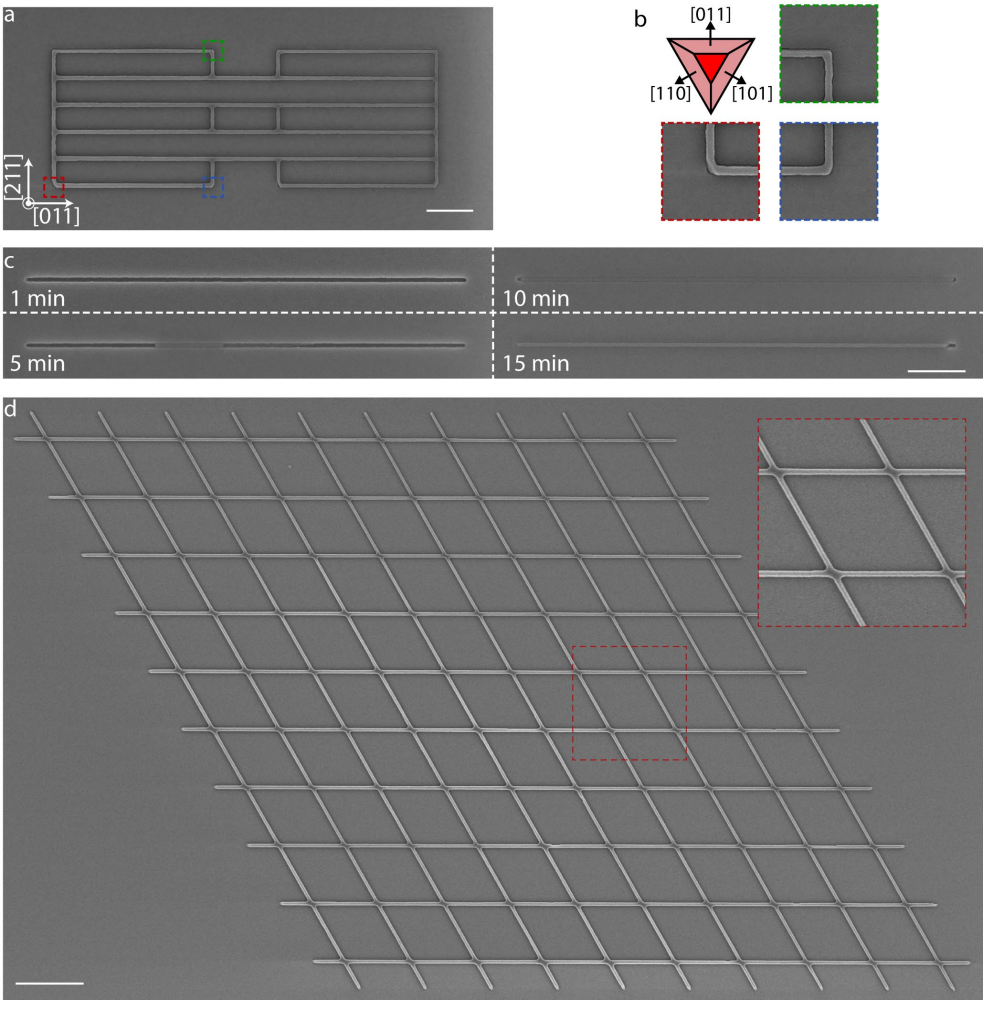


Figure 6.9 | InSb SAG on InP 111A.
a: SEM micrograph of a four-qubit design InSb nanowire network grown on an InP (111)A substrate using a Si_xN_y selective area mask. Terminating growth facets are still visible at the corners of the design (**b**), which are {110} planes. Scale bar is 400 nm. **c:** Growth as a function of time. The nanowire is fully grown in the mask after 10 minutes and exceeds it at 15 minutes. Scale bar is 400 nm. **d**: Fully grown ten-by-ten nanowire network demonstrating the scalability. Scale bar is 1 µm.

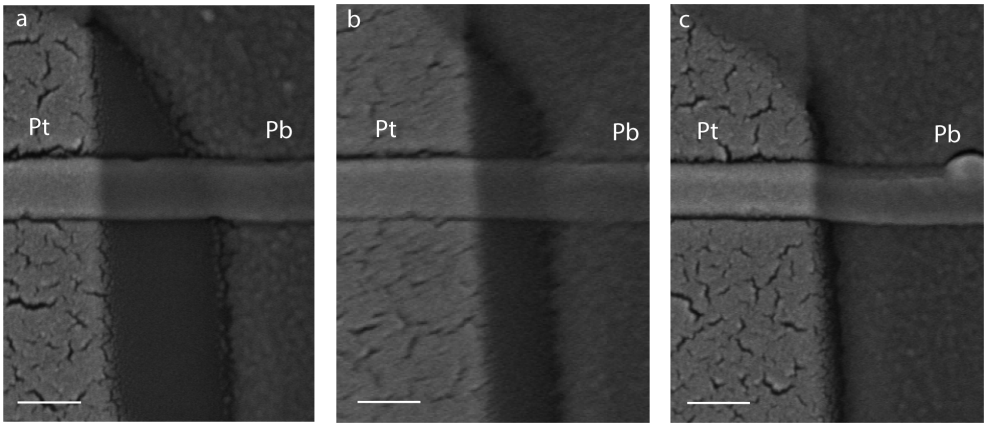


Figure 6.10 | Accuracy of double-sided shadow deposition.
a-c: Close-up SEM images of an in-plane grown InSb nanowire with a metal (Pt) selectively deposited on the left side and a superconductor (Pb) selectively deposited on the right side. The shadow between the metals is ~150 nm (**a**), ~100 nm (**b**), and ~15 nm (**c**). Scale bar is 100 nm.

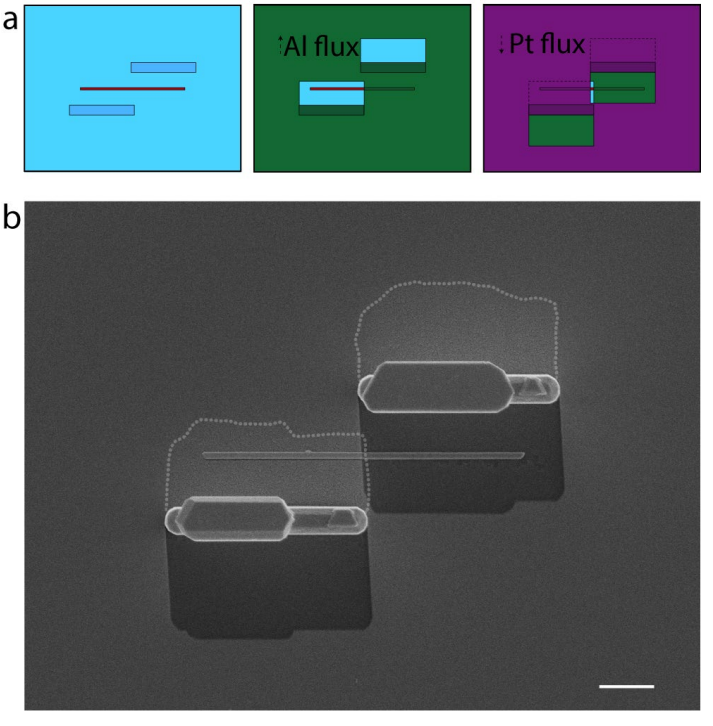


Figure 6.11 | Shadow deposition of Al and Pt.
a: Schematic top-view of two-sided metal deposition on an InSb nanowire (red) using InP walls. The aluminium (green) and Pt (purple) are deposited from opposite sides, creating a normal-nanowire-superconductor device. **b**: Top-view SEM micrograph of such a device. Scale bar is 1 µm.

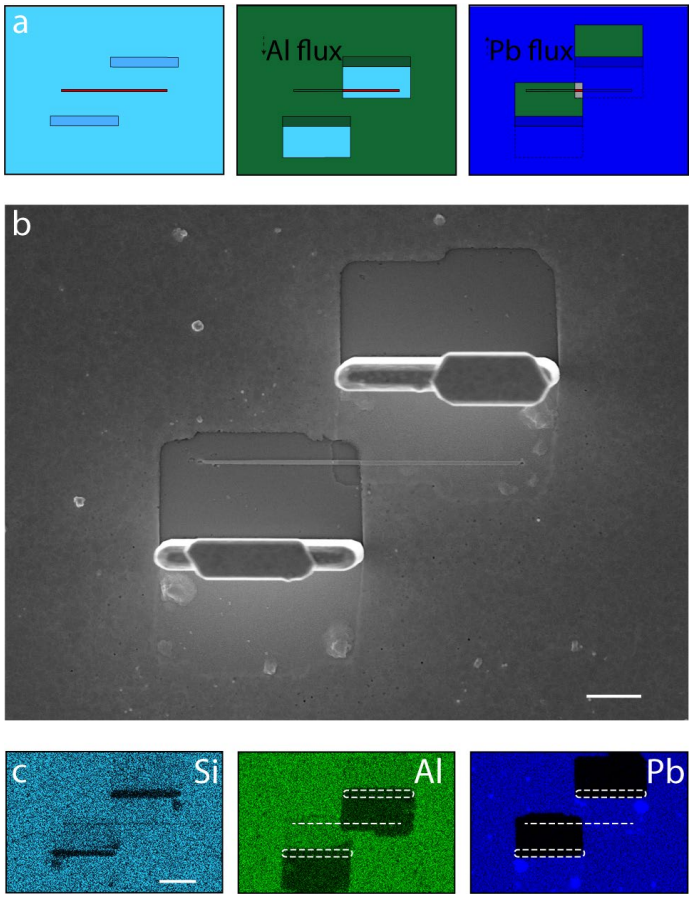


Figure 6.12 | Shadow deposition of Al and Pb.
a: Schematic top-view of two-sided superconductor deposition on an InSb nanowire (red) using InP walls. The aluminium (green) and Pb (blue) are deposited from opposite sides, creating two separated superconducting islands. **b**: Top-view SEM micrograph of such a device. Scale bar is 1 µm. **c**: SEM-EDX elemental mapping of the device shown in (**b**). The silicon signal (light blue) shows the position of the walls and nanowire in the mask. Al (green) and Pb (blue) covered regions show the respective shadowed region. Some Pb accumulation can be observed on the mask. Scale bar is 2 µm.

6.7 References

1 Nayak, C., Simon, S. H., Stern, A., Freedman, M. & Das Sarma, S. Non-Abelian anyons and topological quantum computation. *Reviews of Modern Physics* **80**, 1083-1159, doi:10.1103/RevModPhys.80.1083 (2008).

2 Kitaev, A. Y. Fault-tolerant quantum computation by anyons. *Annals of Physics* **303**, 2-30, doi:10.1016/S0003-4916(02)00018-0 (2003).

3 Oreg, Y., Refael, G. & von Oppen, F. Helical liquids and Majorana bound states in quantum wires. *Phys Rev Lett* **105**, 177002, doi:10.1103/PhysRevLett.105.177002 (2010).

4 Lutchyn, R. M., Sau, J. D. & Das Sarma, S. Majorana fermions and a topological phase transition in semiconductor-superconductor heterostructures. *Phys Rev Lett* **105**, 077001, doi:10.1103/PhysRevLett.105.077001 (2010).

5 Sarma, S. D., Freedman, M. & Nayak, C. Majorana zero modes and topological quantum computation. *Npj Quantum Inform* **1**, doi:10.1038/npjqi.2015.1 (2015).

6 Kitaev, A. Y. Unpaired Majorana fermions in quantum wires. *Physics-Uspekhi* **44**, 131 (2001).

7 Karzig, T. *et al.* Scalable designs for quasiparticle-poisoning-protected topological quantum computation with Majorana zero modes. *Physical Review B* **95**, 235305, doi:10.1103/PhysRevB.95.235305 (2017).

8 Plugge, S., Rasmussen, A., Egger, R. & Flensberg, K. Majorana box qubits. *New Journal of Physics* **19**, doi:10.1088/1367-2630/aa54e1 (2017).

9 Hobbs, R. G., Petkov, N. & Holmes, J. D. Semiconductor nanowire fabrication by bottom-up and top-down paradigms. *Chemistry of Materials* **24**, 1975-1991 (2012).

10 Mourik, V. *et al.* Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices. *Science* **336**, 1003-1007, doi:10.1126/science.1222360 (2012).

11 Albrecht, S. M. *et al.* Exponential protection of zero modes in Majorana islands. *Nature* **531**, 206-209, doi:10.1038/nature17162 (2016).

12 Deng, M. T. *et al.* Majorana bound state in a coupled quantum-dot hybrid-nanowire system. *Science* **354**, 1557-1562, doi:10.1126/science.aaf3961 (2016).

13 Gul, O. *et al.* Ballistic Majorana nanowire devices. *Nat Nanotechnol* **13**, 192-197, doi:10.1038/s41565-017-0032-8 (2018).

14 Vaitiekėnas, S., Liu, Y., Krogstrup, P. & Marcus, C. Zero-field Topological Superconductivity in Ferromagnetic Hybrid Nanowires. *arXiv preprint arXiv:2004.02226* (2020).

15 Vaitiekenas, S. *et al.* Flux-induced topological superconductivity in full-shell nanowires. *Science* **367**, doi:10.1126/science.aav3392 (2020).

16 van Weperen, I., Plissard, S. R., Bakkers, E. P., Frolov, S. M. & Kouwenhoven, L. P. Quantized conductance in an InSb nanowire. *Nano Lett* **13**, 387-391 (2013).

17 Kammhuber, J. *et al.* Conductance quantization at zero magnetic field in InSb nanowires. *Nano Lett* **16**, 3482-3486 (2016).

18 Gazibegovic, S. *et al.* Epitaxy of advanced nanowire quantum devices. *Nature* **548**, 434-438, doi:10.1038/nature23468 (2017).

19 Op het Veld, R. L. M. *et al.* In-plane selective area InSb–Al nanowire quantum networks. *Communications Physics* **3**, 59, doi:10.1038/s42005-020-0324-4 (2020).

20 Krizek, F. *et al.* Field effect enhancement in buffered quantum nanowire networks. *Physical Review Materials* **2**, 093401, doi:10.1103/PhysRevMaterials.2.093401 (2018).

21 Aseev, P. *et al.* Selectivity Map for Molecular Beam Epitaxy of Advanced III-V Quantum Nanowire Networks. *Nano Lett* **19**, 218-227, doi:10.1021/acs.nanolett.8b03733 (2019).

22 Vaitiekenas, S. *et al.* Selective-Area-Grown Semiconductor-Superconductor Hybrids: A Basis for Topological Networks. *Phys Rev Lett* **121**, 147701, doi:10.1103/PhysRevLett.121.147701 (2018).

23 Khan, S. A. *et al.* Transparent Gatable Superconducting Shadow Junctions. *arXiv preprint arXiv:2003.04487* (2020).

24 Carrad, D. J. *et al.* Shadow lithography for in-situ growth of generic semiconductor/superconductor devices. *arXiv preprint arXiv:1911.00460* (2019).

25 Heedt, S. *et al.* Shadow-wall lithography of ballistic superconductor-semiconductor quantum devices. *arXiv preprint arXiv:2007.14383* (2020).

26 Kanne, T. *et al.* Epitaxial Pb on InAs nanowires. *arXiv preprint arXiv:2002.11641* (2020).

27 Fu, L. Electron Teleportation via Majorana Bound States in a Mesoscopic Superconductor. *Physical Review Letters* **104**, 056402, doi:10.1103/PhysRevLett.104.056402 (2010).

28 Vijay, S. & Fu, L. Teleportation-based quantum information processing with Majorana zero modes. *Physical Review B* **94**, 235446, doi:10.1103/PhysRevB.94.235446 (2016).

29 Whiticar, A. M. *et al.* Coherent transport through a Majorana island in an Aharonov-Bohm interferometer. *Nat Commun* **11**, doi:10.1038/s41467-020-16988-x (2020).

30 Wang, N. *et al.* Shape Engineering of InP Nanostructures by Selective Area Epitaxy. *Acs Nano* **13**, 7261-7269, doi:10.1021/acsnano.9b02985 (2019).

31 Webb, J. L. *et al.* Electrical and surface properties of InAs/InSb nanowires cleaned by atomic hydrogen. *Nano Lett* **15**, 4865-4875 (2015).

32 Alicea, J., Oreg, Y., Refael, G., von Oppen, F. & Fisher, M. P. A. Non-Abelian statistics and topological quantum information processing in 1D wire networks. *Nat Phys* **7**, 412-417, doi:10.1038/Nphys1915 (2011).

33 Aasen, D. *et al.* Milestones toward Majorana-based quantum computing. *Phys Rev X* **6**, 031016 (2016).

34 Oura, K., Lifshits, V., Saranin, A., Zotov, A. & Katayama, M. *Surface science: an introduction*. (Springer Science & Business Media, 2013).

35 Pan, H., Sau, J. D. & Sarma, S. D. Three-terminal nonlocal conductance in Majorana nanowires: Distinguishing topological and trivial in realistic systems with disorder and inhomogeneous potential. *Phys Rev B* **103**, 014513 (2021).

36 Rosdahl, T. Ö., Vuik, A., Kjaergaard, M. & Akhmerov, A. R. Andreev rectifier: A nonlocal conductance signature of topological phase transitions. *Physical Review B* **97**, 045421, doi:10.1103/PhysRevB.97.045421 (2018).

37 Liu, C.-X., Sau, J. D., Stanescu, T. D. & Das Sarma, S. Andreev bound states versus Majorana bound states in quantum dot-nanowire-superconductor hybrid structures: Trivial versus topological zero-bias conductance peaks. *Physical Review B* **96**, 075161, doi:10.1103/PhysRevB.96.075161 (2017).

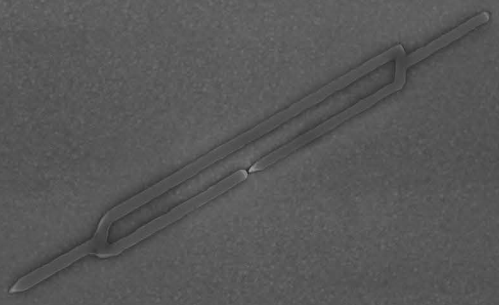
38 Su, Z. *et al.* Mirage Andreev Spectra Generated by Mesoscopic Leads in Nanowire Quantum Dots. *Phys Rev Lett* **121**, 127705, doi:10.1103/PhysRevLett.121.127705 (2018).

39 Ruby, M., Heinrich, B. W., Pascual, J. I. & Franke, K. J. Experimental demonstration of a two-band superconducting state for lead using scanning tunneling spectroscopy. *Phys Rev Lett* **114**, 157001 (2015).

40 Alicea, J., Oreg, Y., Refael, G., Von Oppen, F. & Fisher, M. P. Non-Abelian statistics and topological quantum information processing in 1D wire networks. *Nat Phys* **7**, 412-417 (2011).

Chapter 7

Summary



Summary

Quantum technologies are considered to be the tools for the next big leap forward in the evolution of human society. Specifically, quantum computing, is expected to open a new avenue to tackle problems that have so far been difficult or even impossible to solve. There are many ideas for a physical implementation of a quantum computer, each with their own advantages and disadvantages. One such idea is the use of topological quantum computations by using Majorana fermions.

This thesis describes the progress in the field of developing semiconductor networks for Majorana based topological quantum computation starting with an introduction to the field, followed by a theoretical background description of what has been achieved thus far. The results described in this thesis begin with the development of InSb nanowire networks using an out-of-plane approach. Here, the InSb nanowires are grown using a gold catalyst and specially designed InP substrates such that the nanowires can grow towards each other under a defined angle with the substrate. This enables the possibility of wires merging and creating nanowire networks. Alternatively, by precisely tuning the position of the nanowires on the substrate, the wires can cross each other without merging, making it possible to use one nanowire as the shadowing object in front of another nanowire when a directional flux of metal is used to deposit a superconductor, eliminating the need for a metal etchant. Although this technique has a lot of advantages, there are some inherent limitations when it comes to scalability for larger networks. To overcome this problem, another approach is used for the next generation of devices.

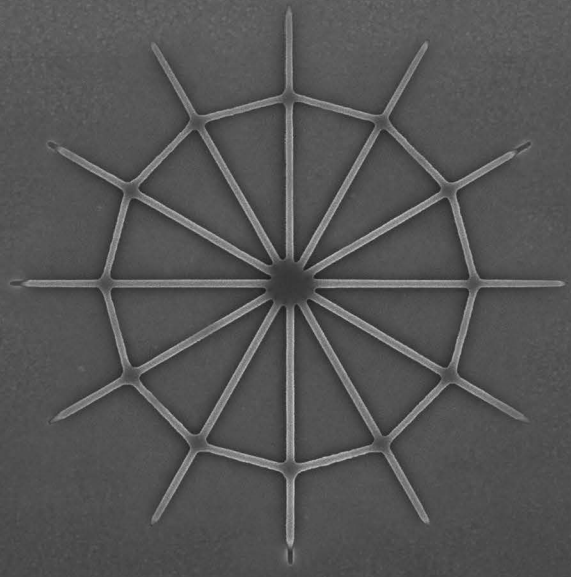
In-plane Selective Area Networks (InSANe) of InSb nanowires on InP substrates is described in detail in the next chapter of this thesis. By depositing an amorphous mask on an InP substrate and creating predefined openings in this mask using lithography, scalable one-dimensional nanowire networks can be grown using metalorganic vapor-phase epitaxy (MOVPE). The growth kinetics are investigated by studying the effect of growth parameters on the nucleation of the InSb on the substrate. Material characterization is performed using scanning electron microscopy (SEM), tunneling electron microscopy (TEM) and atomic force microscopy (AFM). Transport measurements on InSb loop

structures show coherent electron transport by observing Aharonov-Bohm (AB) oscillations, a measure for the material quality. Superconducting aluminum is deposited on the InSb nanowires using molecular beam epitaxy (MBE) at liquid nitrogen (LN_2) temperatures (~110 K) followed by electron transport characterization to demonstrate the quality of the semiconductor-superconductor hybrid device.

In order to get closer to the full in-situ fabrication of a device, unleashing the full potential of the scalable in-plane platform, selective metal-on-semiconductor deposition is achieved by using grown InP walls as shadowing objects. This eliminates the need for any metal etchant and enables the possibility for the in-situ deposition of two different metals selectively on different parts of the InSb nanowire network. This allows for the fabrication of an in-situ device with a high quality of the material near the active region and the interface of the active region. Finally, an outlook is given on preliminary results and future suggestions for the fabrication of tunnel gates underneath the InSb nanowires, called bottom gates, and a buffer layer for electrically insulating the nanowire from the bottom gates completing the goal for the full in-situ device fabrication.

Chapter 8

The Future is InSANe



The future is InSANe

This thesis has shown the advantages and disadvantages of both the out-of-plane grown InSb nanowires as well as in-plane selective area grown nanowire networks (InSANe). Although the research on in-plane nanowires has made serious advancements over the last years,[1-3] there are still a number of challenges to be addressed before it can be used as a platform for scalable topological qubits: **1.** Superconductor properties. Most studies have been performed with aluminium as a superconductor. Being able to sustain a larger critical field, however, would allow for investigating larger Zeeman energies. In addition, the chemical properties of the material are important since interfacial reactions may introduce disorder at the semiconductor/superconductor interface. See Section 8.1 for more details. **2.** Semiconductor properties. Disorder in the nanowire may break up the topological phase into subsegments. By measuring the electron mobility, the level of disorder can be estimated, and should be at least around 10^5 cm^2/Vs. The mobility may be limited by scattering at the nanowire surface, which could be improved upon by adding a capping (surface passivation) layer. See Section 8.2 for more details. The topological gap is determined by the g-factor of the semiconductor, and a larger gap results in a lower sensitivity for disorder. Therefore, a different semiconductor, PbTe, which has a very high g-factor could be a very promising material. See Section 8.6 for more details. **3.** Device tunability. It is very important to have precise control of the chemical potential in the overall device, to tune it within the topological gap, which is in the order of 100 μeV. The topside of the nanowire is already crowded with the superconductor, shielding electrostatic fields, and contacts. We, therefore, propose to develop bottom gates to use the volume underneath the NW effectively. See Section 8.3 for details. **4.** Scalability. In order to profit from the highly mature Si-technology, the InSANe nanostructures should be realized on Si substrates (see Section 8.4).

The current status of the InSANe platform allows for growth of complicated nanowire networks with the addition of selective deposition of superconductors/metals. This enables *in-situ* fabrication of a nanowire device with superconducting islands and superconducting or normal contacts for quantum transport experiments. Figure 8.1 shows a simple flowchart overview of the

interesting aspects that can be studied in the future. The six proposed research directions for 2nd and 3rd generation InSANe devices will be discussed separately below.

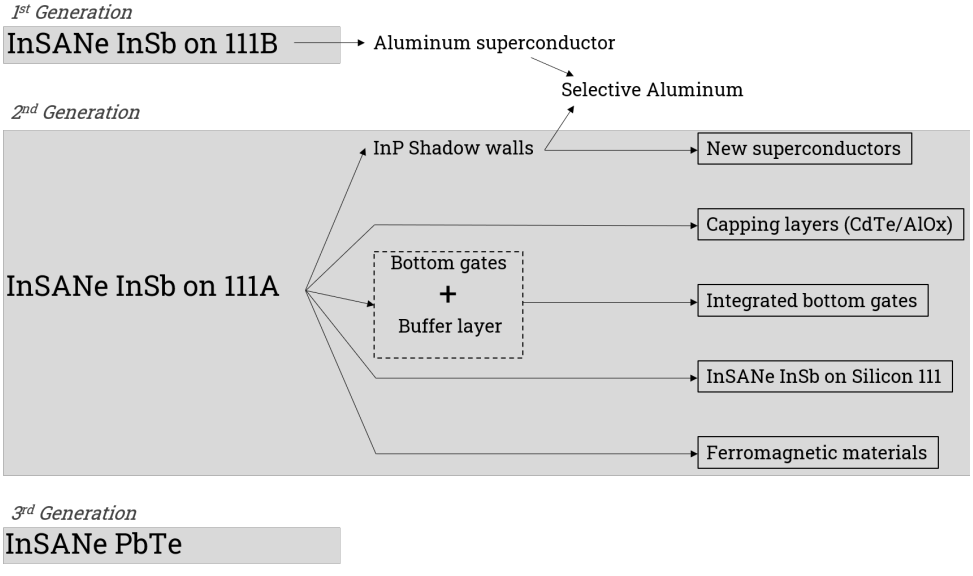


Figure 8.1 | Overview InSANe project
Flowchart of InSANe project history ('1st generation') and ideas for future generations of experiments (2nd and 3rd generation).

In this chapter, an outline is drafted for the next steps in the development of the InSANe platform, the interesting aspects of this platform and its opportunities from a scientific perspective.

8.1. Superconductors

The shadow wall geometry allows investigation of new material combinations without the need to optimize selective etching processes for each metal separately. With this platform a (rather) quick scan can be made to explore several different superconductors. Important parameters for the suitability of a superconductor are, of course, the superconducting properties, like gap size, critical field, and critical temperature, but also its material properties, such as lattice constant, diffusivity on a surface, and chemical reactivity. Finally, the band alignment between the metal (when not in the superconducting state) and the semiconductor is an important ingredient determining the proximity effect. Although there is a plethora of superconductors available, for the specific combination of InSb and the goal of creating a Majorana device, only a few superconductors seem promising based on their properties: Al, Pb, Sn, V, In (see Chapter 2, Table 2.1 for more details). For a material scientist, the InSANe InSb platform might be particularly interesting to use for the growth and characterization of α-tin, which is predicted to be a topological insulator,[4] and is lattice matched to the top surface InSb {111} plane of the InSANe InSb nanowires.

8.2. Capping layers

In-plane grown InSb networks exhibit a relatively low electron mobility compared to their VLS counterparts and bulk InSb.[5] Since the defect density in the in-plane wires is low and the level of incorporated impurities is similar as in VLS wires, the mobility is probably limited by scattering at one of the interfaces: the bottom of the wire (wire/substrate interface), the sides of the nanowire (wire/mask interface), or the top of the nanowire (wire/vacuum interface). A buffer layer, for example $In_xAl_{1-x}Sb$, could be used to reduce the scattering at the substrate side of the wire (see Section 10.3 for more details). The irregularity of the sidewalls of the mask openings prohibits the nanowire to form large stable side facets and leaves tiny pockets (voids), where nanowire material did not grow, which can lead to oxidation of the sidewalls when exposed to ambient air. The top of the nanowire also oxidizes when exposed to air, which negatively impacts the electronic properties. To address this, the surfaces can be passivated by a capping material. A viable way to increase the electron mobility is thus by

capping the InSb to prevent any surface oxides from forming and to passivate the nanowire surface, effectively removing any dangling bonds and reducing possible electron scattering sites. There are two general approaches to this passivation. One is by depositing an amorphous and insulating dielectric on top of the nanowire, like AlOx. This can be done *in-situ* in an MBE system, avoiding any surface oxidation or contamination from ambient air. If the nanowires are grown in a different system, like an MOVPE, and transferred *ex-situ* to another system, then an atomic hydrogen clean can be performed to remove the surface oxides from the nanowires prior to depositing the AlOx layer.

Another option to cap the InSb is to grow a crystalline semiconductor with a much higher bandgap on top of the nanowire surface. A suitable candidate for this is cadmium telluride (CdTe) which is almost lattice matched to InSb.[6] The advantage of this approach would be that there are no dangling bonds at the InSb nanowire surface and there is no strain induced on the nanowire lattice, possibly leading to a better passivation and therefore higher electron mobility in the nanowire. A CdTe layer can also be used as a tunnel barrier between the semiconductor and the superconductor to tune their coupling by the thickness of the layer.

8.3. Bottom gates and buffer layers

A major bottleneck for InSANe nanowires compared to out-of-plane grown nanowires is the possibility to spatially control the chemical potential in the channel by gates. VLS nanowires can be placed on a prefabricated chip with metallic finger gates covered with a dielectric layer (see **Figure 8.2a**). This allows spatial electrostatic control in the channel also underneath the normal and superconducting contacts, which is important to tune the position of the wavefunction and the coupling between the semiconductor and the superconductor. This is, unfortunately, not possible with InSANe nanowires, because a semiconductor cannot be grown crystalline with the right crystallographic orientation on a metallic layer covered by an amorphous dielectric. Hence, gates can either be designed afterwards on top of the network (top gating) or on the sides (side gating), leading to space issues as the ohmic contacts also need to be accommodated on top of the nanowires (see **Figure 8.2b**). Additionally, gating under the

ohmic and superconducting contacts is nearly impossible with gates on top or at the sides of the contact due to screening.

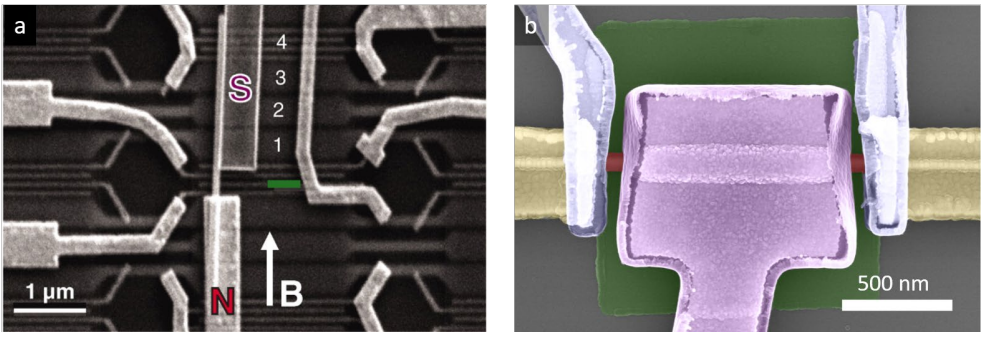


Figure 8.2 | Comparison between functioning devices with VLS and InSANe InSb nanowires
a: Scanning electron microscope (SEM) image of an InSb nanowire device with pre-fabricated metallic bottom gates.[7] **b**: False-coloured SEM image of an in-plane selective area grown InSb nanowire (horizontal, middle left to right in red) contacted with two normal contacts (yellow) and a superconducting aluminium island (middle underneath purple gate) with three top gates fabricated on top of the device (blue and purple). The gates are electrically isolated from the nanowire using a selectively deposited dielectric (green area).

These limitations can be overcome by growth of crystalline bottom gates underneath the nanowire channels. There have been a lot of studies on the stacking of different III-V semiconductors, also known as heterostructures, as in-plane layers or in nanowires, either axially or radially.[8-11] Here, the idea is to create an InSANe InSb device with integrated epitaxial bottom gates. The gates are grown by selective area growth using a mask. After growth of the gate structure, the first mask is removed and a second mask is defined, with line openings, for instance, orthogonal to the bottom gates. An insulating buffer layer is first grown selectively followed by the InSANe nanowires on top of that. See Figure 8.3 for a schematic overview of the idea.

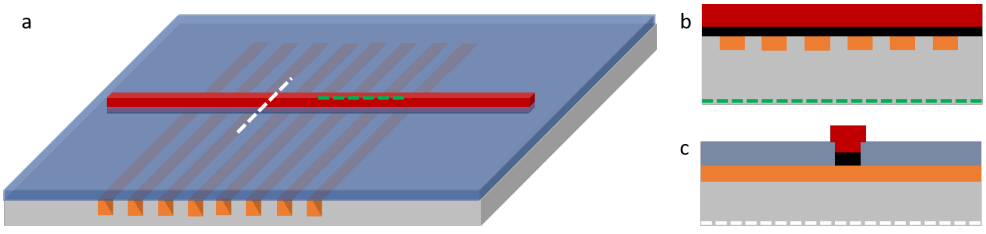


Figure 8.3 | Schematic of integrated bottom gates for in-plane nanowires
a: Perspective view of the final growth chip with an InP 111A substrate (grey), grown bottom gates (orange), the Si_xN_y mask (blue) and the InSb nanowire (red) with a buffer layer below (black). **b**: Cross-section view along the nanowire (green dashed line) showing the stacking of the materials. **c**: Cross-section cut perpendicular to the nanowire (white dashed line).

A few critical challenges should be noted. First, the crystal quality of the bottom gate material is important to avoid any defect propagation into the InSb network grown on top. Therefore, the bottom gate material is ideally lattice matched to the substrate material reducing the chance of defects. Possible materials for this are heavily doped InP or $In_xGa_{1-x}As$, with x at 0.53 such that it lattice matches with InP.[12] Second, the bottom gates should be grown to only fill the trenches in the substrate with the top surface of the gates and surrounding substrate in the same plane, making the subsequent growth easier and ensuring more uniform gating from all gates. Thirdly, the buffer layer needs to be insulating enough to avoid any leakage from the gates into the wire or vice versa during transport measurements.

A possible candidate for the buffer layer is InP. It is already known that InSb nanowires can grow on InP substrates (see Chapter 5), but this would unavoidably cause defects at the interface between InP and InSb and possibly horizontal twin planes in the bottom part of the nanowire. A more suitable alternative is $In_xAl_{1-x}Sb$ as this is more lattice matched to InSb, but still has a relatively large bandgap (2.386 eV for AlSb versus 0.235 eV for InSb, respectively).[13,14] The concentration of aluminium in the buffer layer can be tuned for finding an optimal middle ground between band offset (more aluminium content) and lattice mismatch (lower aluminium content).

The advantage that can be gained in the InSANe platform is the ease of lithographic alignment of the different layers in the stack. This would enable the possibility to create bottom gate designs dedicated to

a specific transport experiment (see Figure 8.4). For example, if an "island" device is desired (so normal contact - superconducting island - normal contact), a gate structure can be made to have two tunnel barrier gates (finger gates on the left and right of the island region) and a gate underneath the island to tune the chemical potential there. This would significantly reduce the screening effect of the superconductor on the gates.

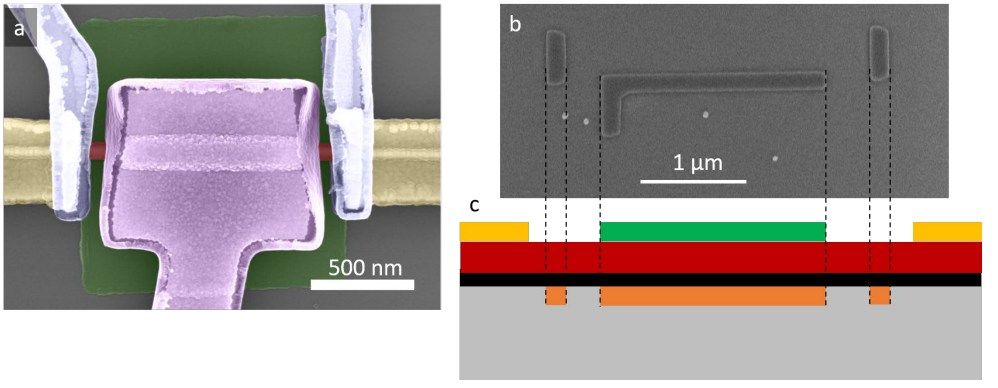


Figure 8.4 | Experiment specific bottom gate design
a: Top view scanning electron microscope (SEM) image of an island device that uses top gates to tune the chemical potential in the nanowire (see Figure 8.2b for details). **b**: Top view SEM image of a bottom gate design selectively grown on InP 111A by using a SixNy mask. The two small vertical segments replace the tunnel gates (blue) in (**a**), and the long horizontal segment will be the gate underneath the superconducting island (purple in **a**). **c**: Cross-section schematic of how the final device would look like, with the substrate in grey, bottom gates (orange), buffer layer (black), InSb nanowire (red), superconducting island (green) and normal contacts (yellow).

8.4. Silicon substrate

One of the most important requirements for a large-scale application is the possibility to integrate the new technology with silicon, the standard for the semiconductor industry. There has been a lot of research on the integration of III-V semiconductors on silicon.[15-17] InSb has been grown on silicon substrates as far back as 1988,[18] as a layer with GaAs as a buffer layer. More recently, InAs quantum dots and out-of-plane nanowires have been grown successfully on silicon,[19-21] while InSb quantum wells have been realized on silicon substrates using a stack of GaAs/InAlSb buffer layers.[22] Growing InSANe InSb

nanowires on silicon has, however not yet been achieved. Expected challenges include the significant lattice mismatch between silicon and InSb (5.43 Å and 6.48 Å),[13,14] and the non-polar Si (111) substrate surface, potentially causing anti-phase boundaries at the interfaces between different InSb nuclei. Another problem is the removal of surface oxides on the substrate surface without damaging the masking layer (Si_xN_y or SiO_x generally). The advantage of using this in-plane technique directly on silicon (over established methods of vertical nanowires on silicon or in-plane wires on other III-V substrates) is the scalability and the direct integration on silicon, making it easier to combine with existing electronics. Many of the processes described in Chapter 5 and optimized for InSANe growth on InP can be applied here as well, like crystal direction knowledge, lithography, mask material and dry etching processes. Some steps are however very specific to the substrate material and require their own optimization, like oxide removal, surface annealing and possible growth parameters.

8.5. Ferromagnetic materials

External magnetic fields are currently being used in quantum transport measurements for the detection of Majorana fermions. It would be interesting to investigate possibilities to incorporate a material in the device to create a magnetic field locally. Theoretical models and some experimental observations hint at the existence of Majorana fermions by using ferromagnetic materials combined with a superconductor.[23-25] Here, the idea is to use ferromagnetic materials as a source for local magnetic fields. An interesting material to try is EuS, which has been grown epitaxially on InAs before.[26] Other possibilities are EuSe or EuTe or their ternaries for their good magnetic properties and their relatively small lattice mismatch with InSb (EuSe: 6.2 Å (-4%), EuTe: 6.6 Å (+2%)) compared to InSb/Al (Al: 4.05 Å (-38%)).[27,28] The main difficulties will be in finding the proper material with a balance between good magnetic properties and reasonable growth quality on InSb nanowires.

Another idea is synthetic spin-orbit coupling by applying a keyboard of magnetic strips underneath the wire channel. This could maybe be realized with SAG growth of EuSe, for instance, similar to the bottom gates.

8.6. InSANe PbTe

The hunt for Majorana fermions in condensed matter goes well beyond InAs and InSb. There have been multiple proposals to find Majorana's in topological materials[29-31] and even by using ferromagnetic nanowires.[24] For the standard semiconductor-superconductor hybrid system, as currently being studied experimentally using InAs or InSb nanowires, most studies are oriented towards trying different superconductors (see Chapter 6). There is, however, also the possibility to change the semiconductor material to a more promising candidate, like PbTe, which is supposed to have a higher spin-orbit coupling and larger Landé g-factor.[32] PbTe is a IV-VI material with a rock salt crystal lattice (like NaCl) where the atoms align periodically in a simple cubic lattice. Integrating PbTe nanowires with Pb as a superconductor is particularly interesting, since Pb is the strongest type I superconductor and will not chemically react with PbTe at the interface. Out-of-plane PbTe nanowires have been grown before, mainly because of their promising thermoelectric applications.[33-36] The reports show, however, that the growth of PbTe nanowires is still in its infancy compared to the high quality and well-controlled growth of III-V nanowires (e.g. InAs, InSb, GaAs, InP). Growing InSANe PbTe nanowires is therefore an interesting challenge from a growth point of view and may combine all the advantages of the in-plane system as mentioned above.

8.7. Conclusion

To conclude, the in-plane platform is particularly suitable to create scalable nanowire networks and potentially even fully integrated devices, gates, semiconductor, and superconductor all grown epitaxially on top of each other with oxide free interfaces. So, in conclusion, it can be stated that for a more scalable and commercially viable solution to topological quantum computing, the future is InSANe!

8.8. References

1 Desplanque, L., Bucamp, A., Troadec, D., Patriarche, G. & Wallart, X. In-plane InSb nanowires grown by selective area molecular beam epitaxy on semi-insulating substrate. *Nanotechnology* **29**, 305705, doi:10.1088/1361-6528/aac321 (2018).

2 Desplanque, L., Bucamp, A., Troadec, D., Patriarche, G. & Wallart, X. Selective area molecular beam epitaxy of InSb nanostructures on mismatched substrates. *Journal of Crystal Growth* **512**, 6-10, doi:10.1016/j.jcrysgro.2019.02.012 (2019).

3 Krizek, F. *et al.* Field effect enhancement in buffered quantum nanowire networks. *Physical Review Materials* **2**, 093401, doi:10.1103/PhysRevMaterials.2.093401 (2018).

4 Fu, L. & Kane, C. L. Topological insulators with inversion symmetry. *Physical Review B* **76**, 045302, doi:10.1103/PhysRevB.76.045302 (2007).

5 Badawy, G. *et al.* High Mobility Stemless InSb Nanowires. *Nano Letters* **19**, 3575-3582, doi:10.1021/acs.nanolett.9b00545 (2019).

6 Golding, T. D. *et al.* Molecular beam epitaxial growth and magneto-transport studies of the InSb/CdTe material systems. *Semiconductor Science and Technology* **5**, S311-S314, doi:10.1088/0268-1242/5/3s/070 (1990).

7 Mourik, V. *et al.* Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices. *Science* **336**, 1003-1007, doi:10.1126/science.1222360 (2012).

8 Friedl, M. *et al.* Template-Assisted Scalable Nanowire Networks. *Nano Letters* **18**, 2666-2671, doi:10.1021/acs.nanolett.8b00554 (2018).

9 Lauhon, L. J., Gudiksen, M. S., Wang, D. & Lieber, C. M. Epitaxial core–shell and core–multishell nanowire heterostructures. *Nature* **420**, 57-61, doi:10.1038/nature01141 (2002).

10 Lind, E., Memišević, E., Dey, A. W. & Wernersson, L. III-V Heterostructure Nanowire Tunnel FETs. *IEEE Journal of the Electron Devices Society* **3**, 96-102, doi:10.1109/JEDS.2015.2388811 (2015).

11 Thelander, C. *et al.* Electron transport in InAs nanowires and heterostructure nanowire devices. *Solid State Communications* **131**, 573-579, doi:10.1016/j.ssc.2004.05.033 (2004).

12 Sweeney, S. J., Eales, T. D. & Adams, A. R. The impact of strained layers on current and emerging semiconductor laser systems. *Journal of Applied Physics* **125**, 082538, doi:10.1063/1.5063710 (2019).

13 Borg, M. B. & Wernersson, L.-E. Synthesis and properties of antimonide nanowires. *Nanotechnology* **24**, 202001, doi:10.1088/0957-4484/24/20/202001 (2013).

14 Vurgaftman, I., Meyer, J. R. & Ram-Mohan, L. R. Band parameters for III–V compound semiconductors and their alloys. *Journal of Applied Physics* **89**, 5815-5875, doi:10.1063/1.1368156 (2001).

15 Duan, G. *et al.* Hybrid III--V on Silicon Lasers for Photonic Integrated Circuits on Silicon. *IEEE Journal of Selected Topics in Quantum Electronics* **20**, 158-170, doi:10.1109/JSTQE.2013.2296752 (2014).

16 Halioua, Y. *et al.* Hybrid III-V semiconductor/silicon nanolaser. *Opt. Express* **19**, 9221-9231, doi:10.1364/OE.19.009221 (2011).

17 Semond, F. *et al.* Molecular Beam Epitaxy of Group-III Nitrides on Silicon Substrates: Growth, Properties and Device Applications. *phys. stat. sol.* **188**, 501-510, doi:10.1002/1521-396x(200112)188:2<501::Aid-pssa501>3.0.Co;2-6 (2001).

18 Rao, T. S. *et al.* Heteroepitaxy of InSb on silicon by metalorganic magnetron sputtering. *Journal of Applied Physics* **53**, 51-53, doi:10.1063/1.100123 (1988).

19 Björk, M. T., Schmid, H., Breslin, C. M., Gignac, L. & Riel, H. InAs nanowire growth on oxide-masked 〈111〉 silicon. *Journal of Crystal Growth* **344**, 31-37, doi:10.1016/j.jcrysgro.2012.01.052 (2012).

20 Cirlin, G. E. *et al.* Formation of InAs quantum dots on a silicon (100) surface. *Semiconductor Science and Technology* **13**, 1262-1265, doi:10.1088/0268-1242/13/11/005 (1998).

21 Liu, A. Y. *et al.* Reliability of InAs/GaAs Quantum Dot Lasers Epitaxially Grown on Silicon. *IEEE Journal of Selected Topics in Quantum Electronics* **21**, 690-697, doi:10.1109/JSTQE.2015.2418226 (2015).

22 Ashley, T. *et al.* Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications. *Electronics Letters* **43**, 1 (2007).

23 Alicea, J. New directions in the pursuit of Majorana fermions in solid state systems. *Rep Prog Phys* **75**, 076501, doi:10.1088/0034-4885/75/7/076501 (2012).

24 Dumitrescu, E., Roberts, B., Tewari, S., Sau, J. D. & Das Sarma, S. Majorana fermions in chiral topological ferromagnetic nanowires. *Physical Review B* **91**, 094505, doi:10.1103/PhysRevB.91.094505 (2015).

25 Nadj-Perge, S. *et al.* Observation of Majorana fermions in ferromagnetic atomic chains on a superconductor. *Science* **346**, 602-607, doi:10.1126/science.1259327 (2014).

26 Liu, Y. *et al.* Coherent Epitaxial Semiconductor–Ferromagnetic Insulator InAs/EuS Interfaces: Band Alignment and Magnetic Structure. *ACS Applied Materials & Interfaces* **12**, 8780-8787, doi:10.1021/acsami.9b15034 (2020).

27 Van Houten, S. Magnetic interaction in EuS, EuSe, and EuTe. *Physics Letters* **2**, 215-216, doi:10.1016/0031-9163(62)90231-7 (1962).

28 Wachter, P. in *Handbook on the Physics and Chemistry of Rare Earths* Vol. 2 507-574 (Elsevier, 1979).

29 Akhmerov, A. R., Nilsson, J. & Beenakker, C. W. J. Electrically Detected Interferometry of Majorana Fermions in a Topological Insulator. *Physical Review Letters* **102**, 216404, doi:10.1103/PhysRevLett.102.216404 (2009).

30 Fu, L. & Kane, C. L. Superconducting Proximity Effect and Majorana Fermions at the Surface of a Topological Insulator. *Physical Review Letters* **100**, 096407, doi:10.1103/PhysRevLett.100.096407 (2008).

31 Fu, L. & Kane, C. L. Probing Neutral Majorana Fermion Edge Modes with Charge Transport. *Physical Review Letters* **102**, 216403, doi:10.1103/PhysRevLett.102.216403 (2009).

32 Oliveira Jr, N. & Ueta, A. Spin-orbit coupling in n-type PbTe/PbEuTe quantum wells. *Acta Physica Polonica A.* **119**, 602-605 (2011).

33 Liang, H.-W., Liu, S., Wu, Q.-S. & Yu, S.-H. An Efficient Templating Approach for Synthesis of Highly Uniform CdTe and PbTe Nanowires. *Inorganic Chemistry* **48**, 4927-4933, doi:10.1021/ic900245w (2009).

34 Roh, J. W. *et al.* Size-dependent thermal conductivity of individual single-crystalline PbTe nanowires. *Journal of Applied Physics* **96**, 103101, doi:10.1063/1.3352049 (2010).

35 Yan, Q. *et al.* A Simple Chemical Approach for PbTe Nanowires with Enhanced Thermoelectric Properties. *Chemistry of Materials* **20**, 6298-6300, doi:10.1021/cm802104u (2008).

36 Dziawa, P. *et al.* Defect Free PbTe Nanowires Grown by Molecular Beam Epitaxy on GaAs(111)B Substrates. *Crystal Growth & Design* **10**, 109-113, doi:10.1021/cg900575r (2010).

Acknowledgments

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Publications

Publications

In-plane selective area InSb–Al nanowire quantum networks
Roy L.M. Op het Veld*, Di Xu*, Vanessa Schaller, Marcel A. Verheijen, Stan M.E. Peters, Jason Jung, Chuyao Tong, Qingzhen Wang, Michiel W.A. de Moor, Bart Hesselmann, Kiefer Vermeulen, Jouri D.S. Bommer, Joon Sue Lee, Andrey Sarikov, Mihir Pendharkar, Anna Marzegalli, Sebastian Koelling, Leo P. Kouwenhoven, Leo Miglio, Chris J. Palmstrøm, Hao Zhang, Erik P.A.M. Bakkers. 2020, *Nature Communications Physics, 3: 59*

Universal platform for scalable semiconductor-superconductor nanowire networks
Jason Jung*, **Roy L.M. Op het Veld***, Rik Benoist, Orson A.H. van der Molen, Carlo Manders, Marcel A. Verheijen, Erik P.A.M. Bakkers. 2021, *Under review*

Parity-preserving and magnetic field–resilient superconductivity in InSb nanowires with Sn shells
Mihir Pendharkar, Bomin Zhang, Hao Wu, Azarin Zarassi, Po Zhang, Connor P. Dempsey, Joon Sue Lee, Sean D. Harrington, Ghada Badawy, Sasa Gazibegovic, **Roy L. M. Op het Veld**, Marco Rossi, Jason Jung, An-Hsi Chen, Marcel A. Verheijen, Moira Hocevar, Erik P. A. M. Bakkers, Chris J. Palmstrøm, Sergey M. Frolov. 2021, *Science*, 372:6541

Large zero-bias peaks in InSb-Al hybrid semiconductorsuperconductor nanowire devices
Hao Zhang, Michiel W.A. de Moor, Jouri D.S. Bommer, Di Xu, Guanzhong Wang, Nick van Loo, Chun-Xiao Liu, Sasa Gazibegovic, John A. Logan, Diana Car, **Roy L. M. Op het Veld**, Petrus J. van Veldhoven, Sebastian Koelling, Marcel A. Verheijen, Mihir Pendharkar, Daniel J. Pennachio, Borzoyeh Shojaei, Joon Sue Lee, Chris J. Palmstrøm, Erik P.A.M. Bakkers, S. Das Sarma, Leo P. Kouwenhoven. 2021, *ArXiv*:2101.11456v1

A full parity phase diagram of a proximitized nanowire island
J. Shen, Georg W. Winkler, Francesco Borsoi, Sebastian Heedt, Vukan Levajac, Ji-Yin Wang, David van Driel, Daniel Bouman, Sasa Gazibegovic, **Roy L.M. Op het Veld**, Diana Car, John A. Logan, Mihir Pendharkar, Chris J. Palmstrøm, Erik P.A.M. Bakkers, Leo P. Kouwenhoven, and Bernard van Heck. 2021, *ArXiv*:2012.10118v2

Transmission phase read-out of a large quantum dot in a nanowire interferometer
Borsoi, Francesco, Kun Zuo, Sasa Gazibegovic, **Roy L. M. Op het Veld**, Erik P. A. M. Bakkers, Leo P. Kouwenhoven, and Sebastian Heedt. 2020, *Nature communications*, 11: 3666.

*equal contribution

Crossed Andreev reflection in InSb flake Josephson junctions
Folkert K. de Vries, Martijn L. Sol, Sasa Gazibegovic, **Roy L. M. Op het Veld**, Stijn C. Balk, Diana Car, Erik P. A. M. Bakkers, Leo P. Kouwenhoven, and Jie Shen. 2019, *Physical Review Research*, 1: 032031.

Electric field tunable superconductor-semiconductor coupling in Majorana nanowires
Michiel W. A. de Moor, Jouri D. S. Bommer, Di Xu, Georg W. Winkler, Andrey E. Antipov, Arno Bargerbos, Guanzhong Wang, Nick van Loo, **Roy L. M. Op het Veld**, Sasa Gazibegovic, Diana Car, John A. Logan, Mihir Pendharkar, Joon Sue Lee, Erik P. A. M Bakkers, Chris J. Palmstrøm, Roman M. Lutchyn, Leo P. Kouwenhoven, and Hao Zhang. 2018, *New Journal of Physics*, 20: 103049.

Mirage Andreev Spectra Generated by Mesoscopic Leads in Nanowire Quantum Dots
Zhaoen Su., Azarin Zarassi, Jen-Feng Hsu, Pablo San-Jose, Elsa Prada, Ramon Aguado, Eduardo J. H. Lee, Sasa Gazibegovic, **Roy L. M. Op het Veld**, Diana Car, Sebastien R. Plissard, Moira Hocevar, Mihir Pendharkar, Joon Sue Lee, John A. Logan, Chris J. Palmstrøm, Erik P. A. M. Bakkers, and Sergey M. Frolov. 2018, *Physical Review Letters*, 121: 127705.

Parity transitions in the superconducting ground state of hybrid InSb–Al Coulomb islands
Jie Shen, Sebastian Heedt, Francesco Borsoi, Bernard van Heck, Sasa Gazibegovic, **Roy L. M. Op het Veld**, Diana Car, John A. Logan, Mihir Pendharkar, Senja J. J. Ramakers, Guanzhong Wang, Di Xu, Daniël Bouman, Attila Geresdi, Chris J. Palmstrøm, Erik P. A. M. Bakkers, and Leo P. Kouwenhoven. 2018, *Nature communications*, 9: 4801.

Epitaxy of advanced nanowire quantum devices
Sasa Gazibegovic, Diana Car, Hao Zhang, Stijn C. Balk, John A. Logan, Michiel W. A. de Moor, Maja C. Cassidy, Rudi Schmits, Di Xu, Guanzhong Wang, Peter Krogstrup, **Roy L. M. Op het Veld**, Kun Zuo, Yoram Vos, Jie Shen, Daniël Bouman, Borzoyeh Shojaei, Daniel Pennachio, Joon Sue Lee, Petrus J. van Veldhoven, Sebastian Koelling, Marcel A. Verheijen, Leo P. Kouwenhoven, Chris J. Palmstrøm, and Erik P. A. M. Bakkers. 2017, *Nature*, 548: 434-38.

InSb Nanowires with Built-In $Ga_x In_{1-x}Sb$ Tunnel Barriers for Majorana Devices
Diana Car, Sonia Conesa-Boj, Hao Zhang, **Roy L. M. Op het Veld**, Michiel W. A. de Moor, Elham M. T. Fadaly, Önder Gül, Sebastian Kölling, Sebastien R. Plissard, Vigdis Toresen, Michael T. Wimmer, Kenji Watanabe, Takashi Taniguchi, Leo P. Kouwenhoven, and Erik P. A. M. Bakkers. 2017, *Nano Letters*, 17: 721-27.

Observation of Conductance Quantization in InSb Nanowire Networks
Elham M. T. Fadaly, Hao Zhang, Sonia Conesa-Boj, Diana Car, Önder Gül, Sébastien R. Plissard, **Roy L. M. Op het Veld**, Sebastian Kölling, Leo P. Kouwenhoven, and Erik P. A. M. Bakkers. 2017, *Nano Letters*, 17: 6511-15.

InxGa1−xAs nanowires with uniform composition, pure wurtzite crystal phase and taper-free morphology
Amira S. Ameruddin, H. Aruni Fonseka, Philippe Caroff, Jennifer Wong-Leung, **Roy L. M. Op het Veld**, Jessica L. Boland, Michael B. Johnston, Hark Hoe Tan, and Chennupati Jagadish. 2015, *Nanotechnology*, 26: 205604.

Patents

Method of forming shadow walls for fabricating patterned structures
Roy L. M. Op het Veld, Jason Jung.
Patent number: PCT/EP2020/061144, 22-April-2020

Method of fabricating gates
Jason Jung, **Roy L. M. Op het Veld**, Petrus J. van Veldhoven.
Patent number: PCT/EP2020/059002, 30-March-2020

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