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Model and Verification of a Plasma Etching Reactor with a Switched-Mode Power Converter

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Abstract—**For reaching a high selectivity in plasma etching, it is required to precisely control the plasma ion energy. This can be realized by applying a tailored pulse-shape voltage waveform to the reactor table. Recent research has shown that switched-mode power converters can be used to generate this kind of waveform, with the benefit of increased efficiency compared to the traditional linear amplifier. However, the equivalent electric circuit model of the plasma etching reactor is required in order to do circuit simulation and make an optimized electronic design of such switched-mode power converters. Although several circuit models of the reactor have been presented in previous research, they can not be directly adopted in tailored pulse-shape biasing.**

In this paper, a modified equivalent electric circuit model of the reactor is proposed. The plasma behaviour is modelled using the equivalent electric circuit and it is suitable for electric circuit simulation together with the power converter. Both the electrical waveforms and the normalized ion energy distribution can be obtained from the simulation, which are in line with the experimental results.

Index Terms—**equivalent electric circuit, ion energy distribution, plasma etching, switched-mode power converter, tailored pulse-shape biasing**

I. INTRODUCTION

Plasma consists of positive ions, negative electrons and neutral particles with an approximately neutral net charge [1]. It plays an important role in semiconductor manufacturing, such as using plasma etching to manipulate the silicon wafer. Fig. 1 shows a schematic representation of a typical inductively coupled plasma (ICP) etching reactor. In the etching process, the goal is to remove the surface material of the substrate wafer on the table by chemical reactions or physical sputtering. Plasma helps to accelerate this process by providing extra energy to the wafer surface.

As shown in Fig. 1, while gas is infused from the top, plasma is ignited and sustained in the chamber by an external radio-frequency (RF) power supply through a matching network. The pressure in the chamber is kept low to reduce the particle collisions. It must be noted that parasitic capacitors are present between the material surfaces, which influence the reactor electrical response. A power converter is connected to the table, which generates a negative bias voltage on the substrate surface. As a result, the ions in the bulk plasma are
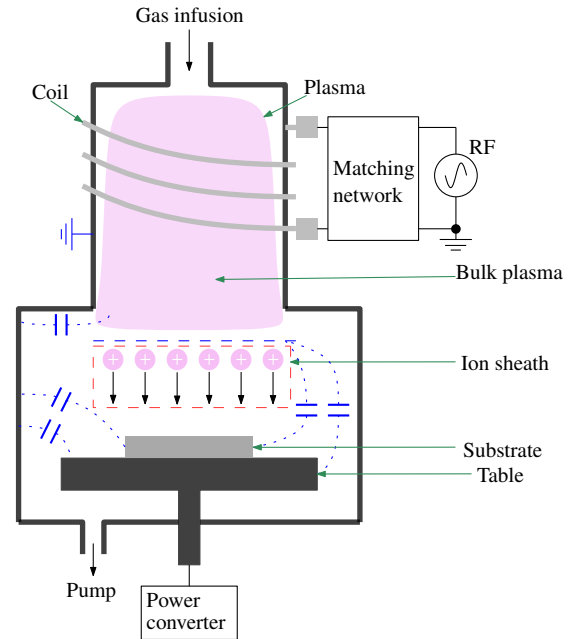
Fig. 1: A typical setup of an inductively coupled plasma etching reactor.

attracted, accelerated and as a result bombard the substrate surface. The bombarding ions provide extra energy for the chemical reaction or introduce physical sputtering on the substrate surface for material removal. Additionally, the normal direction of ion bombardment to the substrate surface also enhances the anisotropy of the etching.

In order to obtain etching with high selectivity, the ion energy should be precisely controlled. This is normally done by controlling the substrate voltage with a power converter. For a typical dielectric substrate, the tailored pulse-shape voltage waveform has proved to be a proper output waveform for the converter [2]–[5]. A switched-mode power converter (SMPC) is proposed in [6] to generate this waveform, which has significant higher efficiency compared to the traditionally used linear amplifier. Besides, it omits the requirement of matching network since the converter is quasi-dc.

However, an equivalent electric circuit (EEC) model of the reactor is needed to enable circuit simulation and optimize

Fig. 2: The schematic of a parallel plate system. u_A and u_B are the voltage potential of surface A and B respectively, and u_P is the plasma potential.

Fig. 3: (a) The traditional EEC model and (b) the modified EEC model of the parallel plate system

the design of SMPC. Although some reactor models have been derived in previous research, they are typically used for RF biasing [1], [7]–[10] or are a steady-state simplification in tailored pulse-shape biasing [11], [12]. These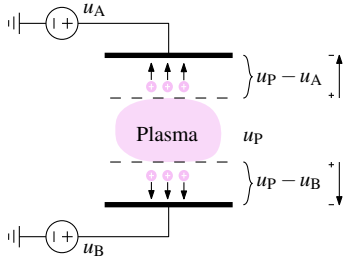 models can not be directly used for transient simulation in tailored pulse-shape biasing due to the different operating condition. In this research, a modified EEC model is formed by modelling the plasma behaviour with electric components. The proposed circuit model can be applied in circuit simulation together with the converter. The ion energy distribution (IED) can also be obtained from the model.

II. REACTOR MODEL

A. Parallel plate system

In order to derive the model of the plasma reactor, firstly the plasma sheath should be introduced. The sheath is a region where the ion density is larger than the electron density and is formed near the material surface. In plasma, the electrons move more rapidly than the ions due to the significantly lower mass. Therefore, for an initially neutral plasma close to a surface, the electrons get lost in the surface and the ion density becomes larger than the electron density in the region near the surface. As a result, the surface is negatively charged, forming an electric field which attracts ions and repels electrons [13].

In the plasma reactor, there are multiple surfaces close to the bulk plasma, including the reactor wall, wafer and reactor table. For simplicity, plasma confronted with two surfaces can be modelled as a parallel plate system, as shown in Fig. 2. The two surfaces are biased by the voltage sources and two sheaths are formed between the bulk plasma and each surface. Due to the existence of the sheath, the voltage potential of the bulk plasma is always higher than the that of the confronted surfaces. The plasma potential u_P is determined by the more positive one between u_A and u_B as represented by

$$u_P = \max\{u_A, u_B\} + V_P, \tag{1}$$

where V_P is the voltage over the Debye sheath [14]. The magnitude of V_P is determined by the plasma condition, including the plasma type, temperature, pressure, etc. and is usually $20 \sim 40$ V in typical etching applications [1]. In the equilibrium, plasma ions are attracted to both surfaces due to the electric field in the sheath, generating an equivalent
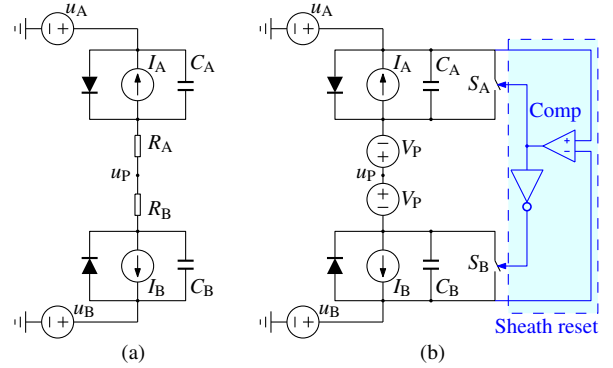
ion current. The energy of the ions bombarding the surface is equal to $e\Delta V$, where e is the element charge and ΔV is the voltage drop over the corresponding sheath.

The traditional EEC model can be built to describe the steady-state of this parallel plate system [1], [8], as shown in Fig. 3(a). Each sheath is modelled by a current source, a sheath capacitor and a diode in parallel with an equivalent resistor in series. The current source in each sheath is the equivalent current generated by the bombarding ions, the direction of which is always towards the surface. Under a fixed plasma condition, the ion current can be treated as a constant dc current, which is independent on the surface potential [14]. The diode controls the voltage direction of the sheath so that the voltage potential of the plasma is always higher than the surface. The equivalent resistor generates a power dissipation in the plasma and leads to a higher voltage potential of the plasma compared to the surface.

This model is able to depict the steady-state properties of the parallel plate system but can not be used for transient analysis. Once the higher potential between u_A and u_B is determined, for instance $u_A > u_B$, the voltage over C_B is charged to $u_P - u_B$. If the potential comparison is reversed, C_B should be discharged. In practice, the sheath experiences a restructuring and reforming process, in which the fast-moving electrons are attracted by the positive voltage thus instantly decreasing the voltage of the sheath [3]. However, there is not a fast discharge path for the sheath capacitor in the model so it can not represent the dynamic behaviour of the plasma.

In order to include the transient response of the parallel plate system in the model, a modified model is proposed as plotted in Fig. 3(b). A virtual sheath reset circuit is added to provide a discharge path for the sheath capacitor. The voltage comparator in the reset circuit compares the voltage potential of the both surface and turns on the active switch corresponding to the higher surface potential. As a result, the capacitor voltage corresponding to the higher surface potential becomes zero while the voltage of the other capacitor changes according to the plasma potential. Moreover, the equivalent resistor is replaced by a fixed dc voltage source representing the Debye sheath voltage V_P.
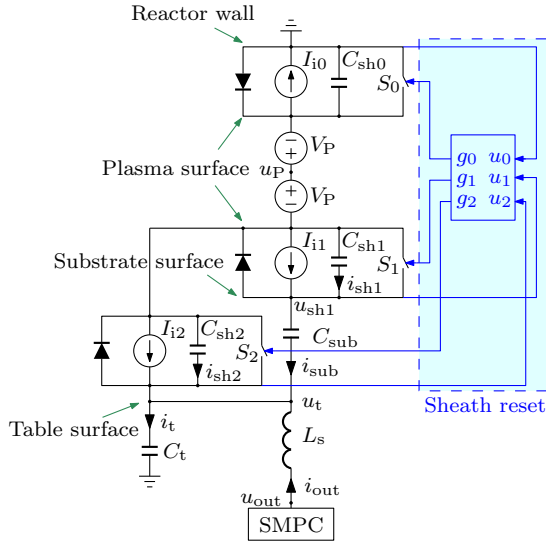
Fig. 4: The EEC model of a plasma etching reactor system.

TABLE I: The status of the sheath reset circuit

Highest voltage	Output		
	g_0	g_1	g_2
u_0	1	0	0
u_1 or u_2	0	1	1

B. Plasma reactor model

Similar to the parallel plate system, the equivalent electric model of the plasma reactor system can be derived as depicted in Fig. 4. The substrate is placed on the conductive table and the table is connected to the power converter. Usually the substrate material, such as a silicon dioxide wafer, is dielectric, so it can be modelled as C_{sub}. The reactor wall and the substrate, the reactor wall and the table each form a parallel plate system as shown in Fig. 4. Therefore, the system consists of three plasma sheaths in total. There exist parasitic capacitors between the table and the reactor wall, the substrate and the reactor wall, as also shown in Fig. 1. Those capacitors are modelled as a lumped table capacitor C_t. L_s is the stray inductance in the power converter and the table loop.

The sheath reset circuit shown in Fig. 4 is a virtual circuit to emulate the transient response of the plasma as previously explained. The reset circuit detects the surface voltage potential of each sheath and control the active switches. The status of the sheath reset circuit is described in Table I. Since the substrate and the table are on the same side, either the substrate or the table has a higher voltage potential than the reactor wall, both surfaces are attracting electrons and the both sheaths are reset at the same time.

The plasma ions are bombarding the substrate surface with an energy governed by

$$E_i = e\left(u_P - u_{sh1}\right) = e\left(V_P + u_{C_{sh1}}\right). \quad (2)$$

During etching, the plasma ions should be accelerated to a

certain velocity, so that they can provide sufficient energy to the substrate surface. Therefore, the table should be negatively biased and u_{sh1} should be negative. Ions with too low energy cause a slow reaction rate while ions with too high energy can remove the material desired to be retained, thus degrading the selectivity. The ion energy is required to remain in a narrow range. Therefore, u_{sh1} is desired to be quasi-constant. According to the EEC model, u_{sh1} is determined by

$$C_{sub}\frac{d\left(u_{sh1} - u_t\right)}{dt} = I_{i1} + C_{sh1}\frac{d\left(u_P - V_P - u_{sh1}\right)}{dt}. \quad (3)$$

During etching when the reactor table is negatively biased, the reactor wall has a higher voltage potential than the other surfaces. As a result, u_P is determined by the reactor wall and is equal to V_P. Therefore, a constant u_{sh1} leads to

$$\frac{du_t}{dt} = -\frac{I_{i1}}{C_{sub}}. \quad (4)$$

In other words, the table voltage u_t should linearly decrease with a slope rate of $-\frac{I_{i1}}{C_{sub}}$ during etching to exactly compensate the ion charge accumulation on the substrate surface for a constant ion energy [15]. In this paper, this condition is defined as the optimal operating point.

For a linearly decreasing u_t during etching, the plasma etching reactor can be generalized by

$$i_{out} = \left(\frac{C_{sh1}C_{sub}}{C_{sh1} + C_{sub}} + C_{sh2} + C_t\right)\frac{du_t}{dt}$$
$$- \frac{C_{sub}}{C_{sub} + C_{sh1}}I_{i1} - I_{i2}. \quad (5)$$

In this model, all capacitances and currents are assumed to be constant within a reasonable range around the optimal operating point. Therefore, a linearly decreasing u_t leads to a dc output current. u_t can then be approximated by u_{out} despite the existence of L_s. Consequently, the EEC model in Fig. 4 can be simplified as shown in Fig. 5(a) during etching.

Because C_{sub} is continuously charging during etching, it is required to discharge it periodically to avoid over-voltage on the substrate. By applying a positive discharge voltage
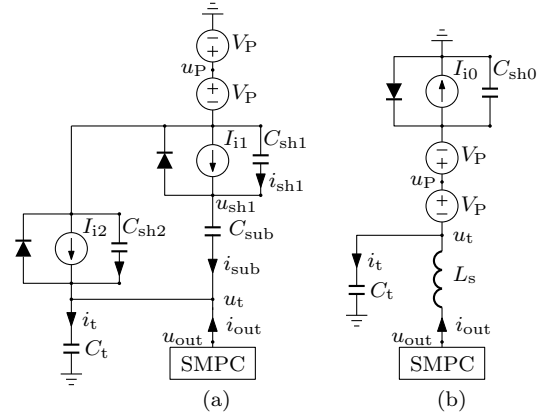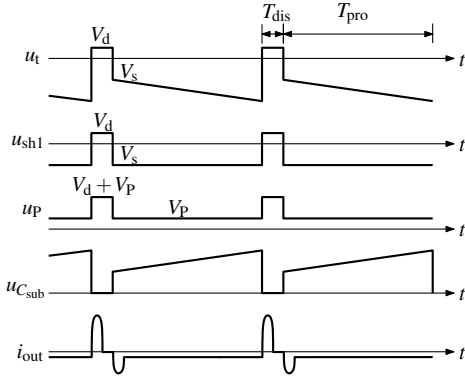

Fig. 5: The simplified EEC model of a plasma etching reactor system during (a) etching phase, (b) discharge phase.

Fig. 6: The typical waveforms of u_t, u_{sh1}, u_P, $u_{C_{sub}}$ and i_{out}. T_{dis} and T_{pro} are the time duration of the discharge phase and etching phase respectively.
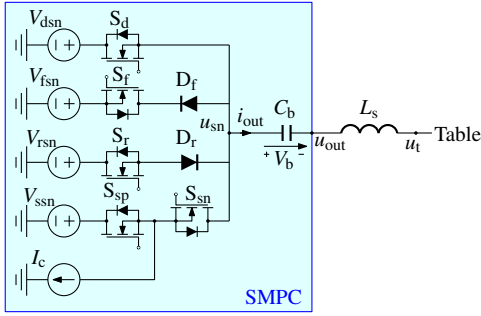

Fig. 7: The topology of the switched-mode power converter.

V_d to the table, both the substrate and table sheath are restructured and reformed. The capacitor C_{sh1}, C_{sh2} and C_{sub} are discharged by attracting the electrons instantly, which is realized by the discharge path through S_1 and S_2 in the circuit model. This process is defined by discharge phase. The EEC model can be simplified as shown in Fig. 5(b) during discharge.

The discharge phase should be short to increase the time percentage of the etching process. After C_{sub} is fully discharged, a negative voltage pulse should be applied to the table to restart the etching phase. The magnitude of this voltage pulse determines the ion energy. Assuming u_t changes to a negative value V_s, due to the capacitive voltage divider formed by C_{sh1} and C_{sub}, u_{sh1} obtains a initial value governed by

$$u_{sh1} = \frac{C_{sub}}{C_{sub} + C_{sh1}} V_s. \qquad (6)$$

Since C_{sub} is typically much larger than C_{sh1}, u_{sh1} can be approximate by V_s. As a result, the typical waveforms of the system can be drawn as shown in Fig. 6. The waveform of u_t is the so-called tailored pulse-shape voltage waveform.

III. Switched-mode Power Converter

An SMPC was designed and applied to deliver the tailored pulse-shape voltage waveform with a controlled voltage slope, the topology of which is shown in Fig. 7. The power converter consists of four controllable dc voltage levels V_{dsn}, V_{fsn}, V_{rsn}
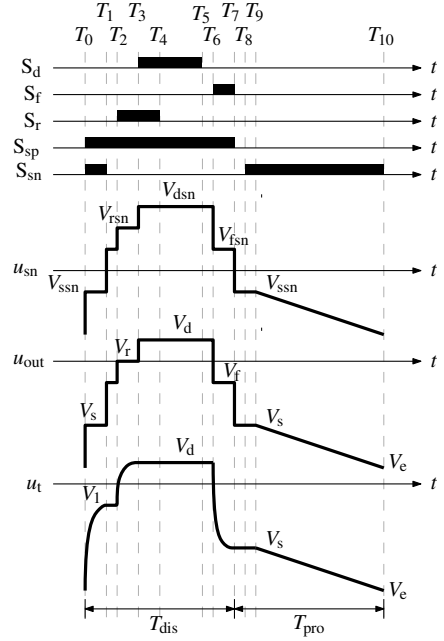

Fig. 8: The operation of the switched-mode power converter.

and V_{ssn} and a controllable dc current source I_c. V_{dsn} and V_{ssn} are utilized to generate V_d and V_s at the output, respectively. Since the reactor is a capacitive load, the stray inductor L_s is utilized to resonantly charge and discharge the load capacitor with the dc voltage sources. V_{fsn} and V_{rsn} are two intermediate voltage levels used to reduce the resonance during charge and discharge, respectively. The dc current source I_c is realized by an inductor in series with a voltage source. During etching phase, $i_{out} = -I_c$.

A blocking capacitor C_b is used at the switch-node in order to produce an equal current flowing into both side of the converter [16]. A self-biasing dc offset voltage V_b is then formed over C_b, the value of which is determined by the plasma condition and the output waveform. The value of C_b should be much larger than C_t and C_{sub} such that V_b can be assumed constant during steady state operation. In this case, the voltage level V_d, V_r, V_f and V_s of u_t are governed by

$$\begin{pmatrix} V_d \\ V_r \\ V_f \\ V_s \end{pmatrix} = \begin{pmatrix} V_{dsn} \\ V_{rsn} \\ V_{fsn} \\ V_{ssn} \end{pmatrix} - \begin{pmatrix} V_b \\ V_b \\ V_b \\ V_b \end{pmatrix}. \qquad (7)$$

The operation of the converter is described by Fig. 8. A more concrete description of the converter is provided in [6].

IV. Experimental Verification

Experiments were conducted with the power converter in an Oxford Instruments FlexAL 2 plasma reactor, which is an atomic layer etching and deposition (ALE/D) machine, as shown in Fig. 9. An eight-inch silicon dioxide wafer was used as a substrate. Argon plasma was excited and sustained with an RF power of 200 W and the pressure inside the reactor was kept at 2.2 mTorr. In the case of measuring IED,
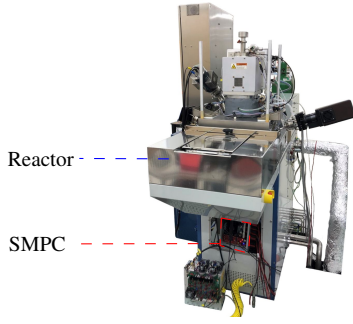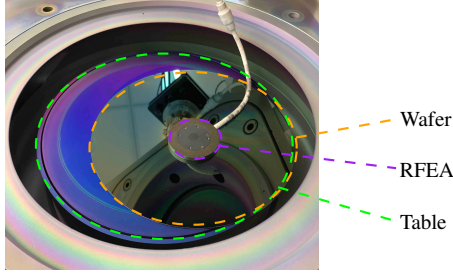
Fig. 9: The FlexAL 2 ALE/D machine.

Fig. 10: The reactor table, wafer and RFEA.

TABLE II: The parameters of the EEC

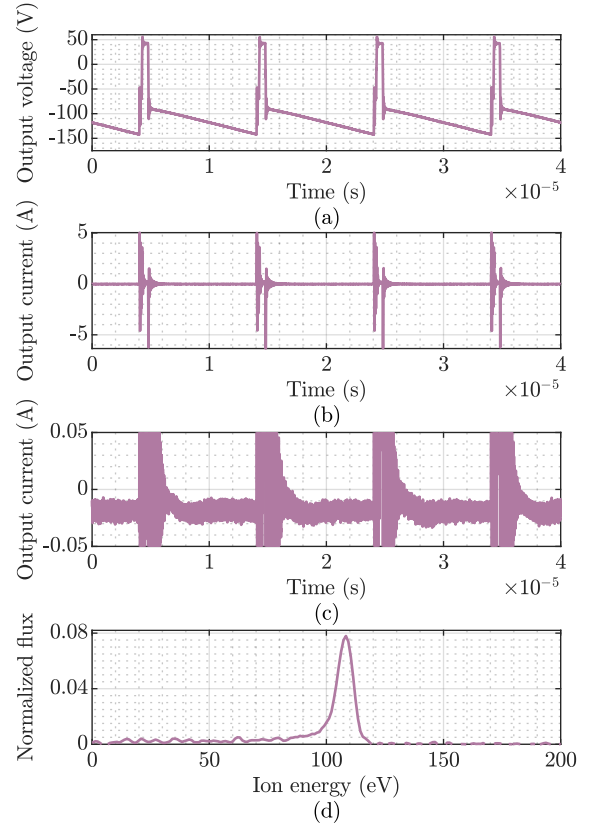| Parameter	Value	Unit	Description
V_P	30	V	Debye sheath voltage
I_{i0}	12	mA	Sheath current (0)
I_{i1}	12	mA	Sheath current (1)
I_{i2}	0	mA	Sheath current (2)
C_t	2.3	nF	Table capacitance
C_{sub}	2.84	nF	Substrate capacitance
C_{sh0}	0.41	nF	Sheath capacitance (0)
C_{sh1}	0.41	nF	Sheath capacitance (1)
C_{sh2}	0	nF	Sheath capacitance (2)
L_s	50	nH	Stray inductance
R_s	6	Ω	Loop resistance

Fig. 11: The measured (a) output voltage, (b) output current, (c) zoomed-in output current, (d) normalized ion energy distribution.

a retarding-field energy analyser (RFEA) was placed on top of the substrate, as shown in Fig. 10. It should be noted that RFEA measurement is intrusive and can disturb the plasma and the EEC model. In this paper, the EEC model and its parameters are based on the case without RFEA. Moreover, it is assumed that RFEA causes minor difference to the IED compared to the case without RFEA.

Fig. 11 gives an illustration of the experimental results at the optimal operating point. The measured waveform of the output voltage and current are plotted in Fig. 11(a) and(b). Fig. 11(c) shows a zoomed-in view of the output current at the dc value. As can be seen, the output current is quasi-dc in etching phase. The measured IED is normalized and plotted in Fig. 11(d). In this case $\frac{\mathrm{d}u_{out}}{\mathrm{d}t} = -5.958 \times 10^6$ V/s leads to the narrowest IED.

By applying the same voltage waveform as the experiment to the EEC model in simulation, the correctness of the EEC can be verified by comparing the simulated and measured waveform. In this paper, the electric simulation is conducted in MATLAB/Simulink with SimScape toolbox. A series of empirical parameter values was adopted in the simulation model, as listed in Table II. In the simulation, $V_P = 30$ V based on the empirical value. In order to further emulate the behaviour of the plasma, a random noise is added to V_P, the magnitude of which is between -5 to 5 V, so that V_P is 25 to 35 V. Moreover, I_{i2} and C_{sh2} are assumed to be zero for simplicity since the effect of them are typically minor.

Fig. 12 shows the simulated waveforms by applying the measured u_{out} waveform to the EEC model. As can be seen, the simulated i_{out} matches the measured i_{out} generally. The plasma potential u_P is determined by the grounded reactor wall in etching phase while determined by the discharge voltage in the discharge phase. The ion energy is quasi-constant in the etching phase, illustrating it is the optimal operating point. The waveform of u_1 and u_P can not be measured with this experimental setup but they are in line with the measured results demonstrated in [2].

Additionally, the simulated E_i is a rough estimation of the transient energy at the moment when the ions are reaching the substrate surface. In practice, ions respond more slowly to the
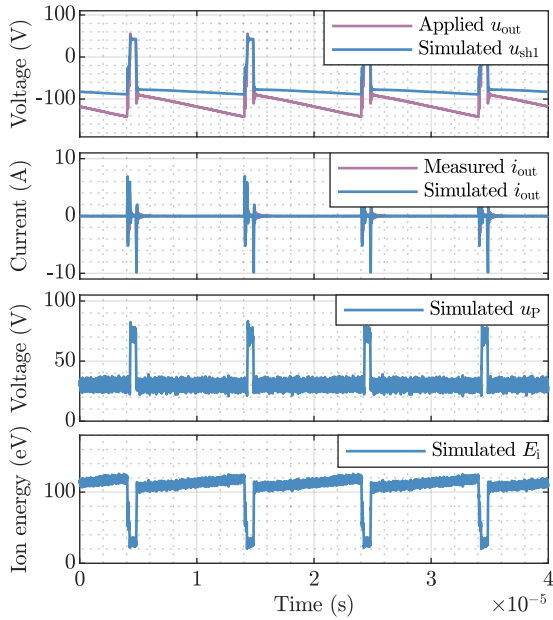
Fig. 12: The simulated waveforms of the equivalent circuit model of the reactor system.
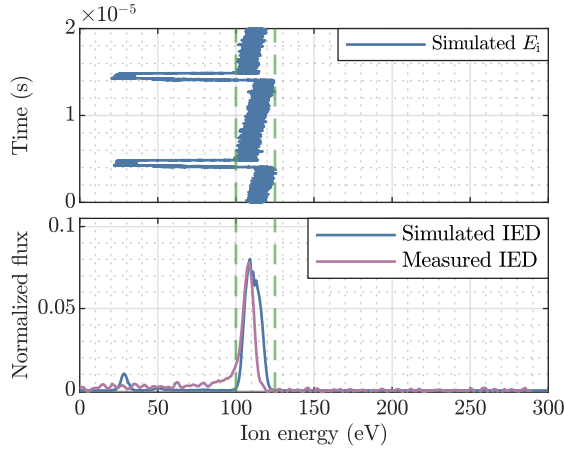

Fig. 13: The comparison of the simulated and measured normalized IED.

discharge phase due to their large mass and short duration of the discharge voltage pulse. Therefore, the practical E_i should be more smooth. On the other hand, by calculating the distribution of the ion energy based on the simulated E_i with a resolution of 1 V, the normalized IED can be obtained, which emulates the function of the RFEA [17]. The simulated normalized IED is compared to the measured normalized IED, as shown in Fig. 13. As can be seen, the simulation result aligns with the measurement.

V. CONCLUSION

In this research, a modified EEC model of the plasma etching reactor biased by tailored pulse-shape voltage waveform is introduced. The model enables circuit simulation and accurate IED estimation of the plasma reactor, which can not

be realized by the state-of-the-art models. The proposed model can be used for accurate electrical and plasma behavioural analysis. A switched-mode power converter has been used to deliver the required waveform for model verification. The introduced EEC model is simulated and compared to the experimental measurement. The simulated waveforms correspond to the measured ones well and the simulated IED matches the measured IED accurately. The results demonstrate the effectiveness of the proposed EEC model, which provides a basis for design of the switched-mode power converters used for plasma etching application.

REFERENCES

[1] M. A. Lieberman and A. J. Lichtenberg, *Principle of plasma discharges and materials processing*, 2nd ed. John Wiley & Sons, Inc., 2005, no. 1.

[2] S.-B. Wang and A. E. Wendt, "Control of ion energy distribution at substrates during plasma processing," *J. Appl. Phys.*, vol. 88, no. 2, pp. 643–646, Jul. 2000.

[3] P. Kudlacek, R. F. Rumphorst, and M. C. M. van de Sanden, "Accurate control of ion bombardment in remote plasmas using pulse-shaped biasing," *J. Appl. Phys.*, vol. 106, no. 7, p. 073303, Oct. 2009.

[4] I. T. Martin, M. A. Wank, M. A. Blauw, R. A. C. M. M. van Swaaij, W. M. M. Kessels, and M. C. M. van de Sanden, "The effect of low frequency pulse-shaped substrate bias on the remote plasma deposition of a-si : H thin films," *Plasma Sources Sci. Technol.*, vol. 19, no. 1, p. 015012, Jan. 2010.

[5] T. Faraz, Y. G. Verstappen, M. A. Verheijen, N. J. Chittock, J. E. Lopez, E. Heijdra, W. J. Van Gennip, W. M. Kessels, and A. J. MacKus, "Precise ion energy control with tailored waveform biasing for atomic scale processing," *J. Appl. Phys.*, vol. 128, no. 21, p. 213301, 2020.

[6] Q. Yu, E. Lemmen, K. Wijnands, and B. Vermulst, "A switched-mode power amplifier for ion energy control in plasma etching," in *2020 IEEE Energy Convers. Congr. Expo.*, 2020.

[7] Z. L. Dai and Y. N. Wang, "Dynamic sheath model at pulsed-biased insulating substrates," *J. Appl. Phys.*, vol. 92, no. 11, pp. 6428–6433, 2002.

[8] D. Gahan, S. Daniels, C. Hayden, P. Scullin, D. O'Sullivan, Y. T. Pei, and M. B. Hopkins, "Ion energy distribution measurements in rf and pulsed dc plasma discharges," *Plasma Sources Sci. Technol.*, vol. 21, no. 2, p. 8, 2012.

[9] H. B. Profijt, M. C. M. van de Sanden, and W. M. M. Kessels, "Substrate-biasing during plasma-assisted atomic layer deposition to tailor metal-oxide thin film growth," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 31, no. 1, p. 01A106, Jan. 2013.

[10] Z. Liu, Z. Dai, C. He, and Y. Wang, "Effects of tailed pulse-bias on ion energy distributions and charging effects on insulating substrates," *Plasma Sci. Technol.*, vol. 17, no. 7, pp. 560–566, Jul. 2015.

[11] D. K. Victor Brouk, Daniel J. Hoffman, Daniel Carter, "Wide dynamic range ion energy bias control; fast ion energy switching; ion energy control and a pulsed bias supply; and a virtual front panel," Aug. 2013.

[12] Q. Yu, E. Lemmen, and B. J. D. Vermulst, "Determining an optimal ion energy for plasma processing of a dielectric substrate," Patent WO2 021 064 110, Apr. 8, 2021.

[13] D. J. Economou, "Tailored ion energy distributions on plasma electrodes," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 31, no. 5, p. 050823, 2013.

[14] F. F. Chen and J. P. Chang, *Lecture Notes on Principles of Plasma Processing*. Boston, MA: Springer US, 2003.

[15] E. V. Barnat and T.-M. Lu, "Calculated sheath dynamics under the influence of an asymmetrically pulsed dc bias," *Phys. Rev. E*, vol. 66, no. 5, p. 056401, Nov. 2002.

[16] S.-H. Song and M. J. Kushner, "Role of the blocking capacitor in control of ion energy distributions in pulsed capacitively coupled plasmas sustained in ar/cf4/o2," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 32, no. 2, p. 021306, Mar. 2014.

[17] D. Gahan, B. Dolinaj, C. Hayden, and M. B. Hopkins, "Retarding field analyzer for ion energy distribution measurement through a radio-frequency or pulsed biased sheath," *Plasma Process. Polym.*, vol. 6, no. SUPPL. 1, pp. S643–S648, Jun. 2009.