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Integrated Circuits for Wearable Systems based on Flexible Electronics

Mohammad Zulqarnain

The work in this thesis was carried out in the Integrated Circuits (IC) group of the Department of Electrical Engineering at the Eindhoven University of Technology in collaboration with imec-NL/Holst Centre under the framework of the project “Integrated Circuits for Conformal Wearable Systems”.

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Integrated Circuits for Wearable Systems based on Flexible Electronics

PROEFSCHRIFT

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To my beloved parents

“Hum to mā.il-ba-karam haiñ koī saa.il hī nahīñ

Raah dikhlā.eñ kise rah-rav-e-manzil hī nahīñ

Koī qābil ho to hum shān-e-ka.ī dete haiñ

Dhūñdne vāloñ ko duniyā bhī na.ī dete haiñ”

— Allama Iqbal

[Behold, my hands are full of gifts, but no one comes seeking here,

And whom shall I show the right path, when there is no traveller,

On him who merits well, I bestow the brightest diadem,

And those who truly come questing, I unveil even a new world to them.]

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Chapter 1

Introduction

1.1 Introduction

The electronics field has witnessed a transformation phase in the recent years, due to the rapid rise of wearables and ubiquitous sensors, thanks to the advent of the Internet of Things (IoT). There are applications which do not suit traditional electronics such as displays, imagers, photovoltaic cells, NFC tags, wearable sensors for biomedical signals monitoring etc.

Indeed, applications that require a large surface to be covered with electronics are difficult or costly to achieve with conventional Silicon-based Integrated Circuits (ICs). However, advancements in the technology of thin-film transistors (TFTs) have paved the way to fabricate devices over large areas and have opened the possibility, thanks to a low process temperature budget, to use plastic foils as flexible substrates, enabling what is called "flexible and large area electronics". This type of devices not only result in electronics distributed over a large area, but also leads to lower cost per unit area compared to conventional ICs. The inherent flexible nature of the substrates in these technologies can be leveraged in applications requiring conformability, bendability, foldability and stretchability. A specific category of applications that can strongly benefit from flexible electronics is the domain of flexible and comfortable wearable devices for wellness and healthcare monitoring.

The dimensions of the transistors in flexible technologies are in micrometre regime, that leads to low cost solutions. Although these devices do not perform on par with conventional Silicon technologies, these devices are useful in the applications where high performance is not required. Thus, the driving requirements are flexible form factor, large surface area and reduced system cost. The ultimate purpose of flexible electronics is to enable electronic platforms that are not feasible and/or not cost-efficient with existing Silicon-based technologies. Besides, it should be noted here that the goal of flexible electronics is not to replace mainstream Silicon technologies, but rather to implement those functions that are not well addressed by conventional Silicon technologies. The main enablers of flexible

electronics include its mechanical flexibility, large-area manufacturing and potential low-cost in volume. Hence, the focus of flexible electronics is on those applications where properties such as flexibility, conformability and light weight are demanded, or for applications where a large area is required.

1.1.1 Flexible electronic technologies

Flexible electronic technologies can be divided in the following categories depending on the nature of the semiconductor material used.

Amorphous Silicon

Amorphous Silicon (a-Si:H or a-Si) is the most well-known thin-film semiconductor [1], generally used in display backplanes. The fabrication process of a-Si based TFTs requires only 4-5 mask steps and it results in n-type only devices. The standard process temperature for a-Si is about 250°C-350°C. The amorphous nature of a-Si gives it a good uniformity but the charge carrier mobility is very low ranging between 0.5-1 $cm^2V^{-1}s^{-1}$. Moreover, the electrical stability of a-Si based devices is poor, which results in threshold voltage shifts of as large as 10 V [2, 3].

Low temperature polycrystalline Silicon

Low temperature polycrystalline Silicon (LTPS) can be used as an alternative semiconductor for high-performance display backplanes. LTPS transistors exhibit mobility in the range of 50-100 $cm^2V^{-1}s^{-1}$ due to the polycrystalline nature of the semiconductor, with the additional possibility of fabrication of both p-type and n-type transistors. However, the small crystals give rise to grain boundaries resulting in device-to-device non-uniformity. A higher process temperature (around 500°C) is one other drawback while the more complex process flow with additional mask steps [4] results in larger cost and lower yield compared to a-Si.

Organic semiconductors

Organic semiconductors have been explored to overcome the limitations, concerning the processing temperature, of a-Si and LTPS [5, 6, 7, 8]. The maximum processing temperature for organic semiconductor based TFTs is about 100°C. Typical mobility values for organic semiconductors lie in the range of 1-10 $cm^2V^{-1}s^{-1}$. The organic semiconductors are mostly p-type, but n-type organic materials are also available nowadays. Environmental factors affect organic semiconductors much more than a-Si or LTPS due to their chemical nature, which makes proper encapsulation necessary for standard use, as it has been shown, for instance, in organic light emitting diodes (OLED) displays.

Metal-oxide semiconductors

Metal-oxide semiconductors are a class of materials exhibiting excellent semiconducting behaviour at low processing temperature (around 250°C). Although, the first metal-oxide transistor was reported in 1964 [9] using semiconducting SnO_2, it was the work by Hosono's group that gave a fundamental contribution to the field of flexible TFTs demonstrating for the first time amorphous Indium Gallium Zinc Oxide (a-IGZO) TFTs deposited on a flexible substrate at room temperature [10]. The most prominent metal-oxides are oxides of In, Zn, Ga and Sn. These semiconductors exhibit comparatively high electron mobility in the range of 1-50 $cm^2V^{-1}s^{-1}$. The amorphous nature of these oxides give them good uniformity. These metal oxides show good operational stability as well, making them an attractive choice for a variety of applications. Generally, metal oxides are electron-conducting semiconductors, hence, resulting in n-type TFTs.

It is clear from the ongoing discussion that amorphous metal-oxide TFTs exhibit overall a better performance trade-off compared to other semiconducting materials in terms electron carrier mobility, operational stability and low thermal budget. For these reasons, from now on, our focus in this thesis will be limited to a-IGZO tech-

nology which is available at imec-NL/TNO (Holst Centre), Eindhoven and imec, Leuven.

1.1.2 Design challenges

The physical properties of flexible electronic materials and their processing give rise to many design challenges at circuit and system level, which are summarized below:

Low frequency noise

The low quality interface between dielectric and semiconductor, together with mobility fluctuation results in large low-frequency noise (1/f or flicker noise) in thin film transistors [11]. Moreover, the 1/f noise component is the dominant noise contribution for bio-signal acquisition front-ends owing to the low frequency content of biomedical signals. Hence, low-frequency noise mitigation is the foremost challenge in designing bio-signal acquisition front-ends. Flicker noise can be suppressed by using chopping [12], but at the cost of larger bandwidth requirements. It can be decreased by increasing device area as well, which exacerbates the negative role of the amplifier input parasitic capacitance, reducing input impedance. Discrete time circuit techniques such as auto-zeroing and correlated double sampling can also be exploited to mitigate 1/f noise [12]. However, such techniques require large capacitors which are difficult to integrate in TFT technologies with acceptable yield, at the state-of-the-art.

Low efficiency

One of the main limitations of TFTs is their mobility, which is one to two orders of magnitude smaller than mainstream Silicon field effect transistors. Low mobility results in low transconductance (g_m) of the devices, which consequently limits the small-signal intrinsic gain ($g_m r_o$) and transition frequency (f_T). Moreover, the large oxide thickness typically available in TFTs results in limited electrostatic control

over the channel, which ultimately leads to larger supply voltages. From the circuit design perspective, this results in low gain-bandwidth product (GBW) and low efficiency in terms of speed versus needed power.

Variability

The low process temperature and low-cost manufacturing of TFTs result in large parameter variability. Apart from that, the low process temperature, which is the enabler of mechanical flexibility, is also responsible for limited control of device characteristics, resulting in poor intrinsic matching between identical neighbouring devices [13]. For instance, analogue to digital conversion in presence of variability and poor matching becomes extremely challenging.

Unipolar nature of devices

The unipolar nature of the devices in a-IGZO technology makes it impossible to use well-known CMOS circuit techniques. Consequently, active loads with simple configuration and low transistor count are not available in unipolar technologies. The low intrinsic gain and the absence of complementary devices limit the gain attainable with unipolar flexible TFT based amplifiers, which makes structures based on feedback less useful in stabilizing the closed-loop performance compared to standard CMOS solutions.

Interfacing with Silicon

Circuits consisting of TFTs generally require a high supply voltage in the range of 10-20 V due to thicker dielectrics used in flexible TFTs, while state-of-the-art Silicon based circuits are operated at supply voltages around 1 V. This inherent difference in supply voltage domains makes interfacing of flexible circuits with Silicon based circuits in hybrid systems quite challenging.

1.1.3 Applications

The research in the field of flexible electronics, in its nascent phase, focused primarily on applications related to digital circuits, due to considerable challenges in realizing analogue functions. There has been an immense research and industrial effort in applications related to large area displays, Radio Frequency Identification (RFID) and Near Field Communication (NFC) tags in the last decade. However, in recent years, there has been a paradigm shift, thanks to advancements in the processing technology. Now, many novel applications are being envisioned using flexible electronics including: physiological monitoring by wearable flexible health patches, epidermal electronics, flexible implants, flexible e-tattoos and wearable electronics for wellness. With the advent of IoT, flexible electronics is expected to make an even bigger impact in many diverse fields.

1.1.4 State-of-the-art flexible wearable biomedical sensors

Wearable biomedical devices have witnessed a growing interest in the recent years. Biomedical wearables typically aim at measuring vital signs of different organs, such as the brain, the muscles and the heart. Biomedical signal monitoring requires wearable devices to be conformable to the shape of the body, in order to improve the quality of signal monitoring and to ensure maximum comfort of use. Advancements in fabrication techniques and new materials that make it possible to build flexible and conformal electronics are thus an important enabler to build wearables for biomedical applications [14, 15, 16]. In the last few years, many research groups have focused on system integration. These efforts have resulted in the development of hybrid flexible electronics systems consisting of flexible electronics systems integrated with rigid conventional Silicon based systems, as well as the realization of fully flexible platforms.

Present flexible wearable biomedical sensors can be broadly classified in three categories:

1. Wearable devices in which all active components are rigid Silicon ICs. These devices are built by encapsulation and packaging techniques exploiting flexible or elastic layers, by integration in fabrics and/or by using flexible interconnects. These wearables can implement complex electronic functionality thanks to the Silicon ICs, at the cost of a reduced comfort level for the user, due to the presence of many rigid parts. Examples of such IC-based wearables include electrocardiogram (ECG) sensors with electrodes integrated into a cotton T-shirt [17], cardiac sensors where a rigid IC is encapsulated in elastic layers [18, 19], stretchable "e-tattoos" for ECG and temperature monitoring [20], and a portable electrocorticography (ECoG) system with a flexible microelectrodes array [21]. Multimodal bio-signal acquisition has been demonstrated too, with stretchable sensors capable of monitoring several combinations of electroencephalograpgy (EEG), ECG, electromyography (EMG), electrooculography (EOG) and photoplethysmography (PPG) [22, 23, 24].

2. Wearable devices in which sensors and/or front end elements are based on flexible materials/substrates while the rest of the system is implemented with rigid Silicon ICs. In this type of hybrid solutions, flexible electronic devices and sensors are used for interfacing with the human body, while rigid electronics (conventional Silicon ICs) are used for signal processing and communication functions such as amplification, filtering, digitization and data transmission. In this way, the flexibility and conformability of the flexible substrate are combined with the good signal acquisition and processing capability of rigid components. In this approach, however, the manufacturing steps and costs increase, due to the processing required to integrate flexible and rigid parts. Besides, the rigid components may result in reduced patient comfort and disturbance to the measurements due to movements. Examples of this category of wearable sensors include screen-printed electrodes for ECG [25, 26], electrophysiological sensing arrays [27], self-powered ultra-flexible electronics using organic electrochemical transistors [28], implantable sen-

sors for the brain [29], flexible printed electrodes for EEG [30], a pulse oximeter based on organic materials compatible with flexible substrates [31], an ultrasonic device conformable to the skin and capable of monitoring blood pressure [32] and epidermal electronics for multimodal physiological monitoring [33].

3. Wearable devices in which all components are built using flexible electronics. The materials exploited in these flexible devices are lightweight and fully conformable to the human body, ensuring at least in principle maximum user comfort. Examples of such wearable sensors include flexible ECG monitoring devices [32, 34, 35], a prosthetic skin with stretchable multi-electrode arrays for nerve stimulation [36], organic electrochemical transistors for ECoG monitoring [37], large-area flexible or stretchable sensors able to detect arterial pulses [32, 38] and an epidermal electronic system capable of monitoring ECG and EMG [39]. Although, all these examples show the feasibility of flexible or conformable wearable devices, the inherently poor electric performance of flexible TFT technologies results in limited electronic functionality for this class of wearables. For instance, all smart bio-signal sensors based only on flexible components, at the state-of-the-art lack digitization of the measured signals and data transmission capability.

1.2 Problem statement

There are many challenges, as discussed in Section 1.1.2, in realizing flexible wearable devices. Therefore, simple, innovative and non-conventional approaches at circuit and system level, along with exploring the integration and form factor possibilities, need to be researched to come up with solutions, where conformable wearable devices provide sufficient performance to be used in real case applications.

1.3 Aim of the thesis

The aim of this thesis is to advance the state-of-the-art of flexible electronics with specific focus on wearable bio-signal measurement systems. The research described in this thesis is carried out mainly focusing on the following aspects:

- Design of analogue and mixed signal building blocks in flexible TFT technologies
  - Design single stage and multi stage amplifiers with different topologies to get an insight into performance trade-offs and maximum gain architectures in unipolar flexible technologies.
  - Design of voltage-to-time converters, to translate voltage-domain signals to the time domain, in order to provide a robust method for quantization in the presence of variability.
- Design of wearable bio-signal measurement systems using only flexible electronics
  - Design wearable bio-signal measurement systems composed of flexible electronics only, enhancing user comfort due to the conformability of flexible foil and reducing cost due to low cost of large area electronics.
- Design of a multichannel wearable bio-signal measurement system using flexible hybrid electronics integrating flexible TFTs on foil and a Silicon IC
  - Design a multichannel wearable hybrid flexible electronics system exploiting together the large area character of flexible technologies and the better performace/efficiency of Si ICs, with emphasis on system partitioning and on interfacing of different supply voltage domains of Silicon and flexible technologies.

1.4 Scope of the thesis

The work presented in this thesis focuses on the design and characterization of wearable bio-potential systems, manufactured using a-IGZO TFTs fabricated at imec-NL/TNO (Holst Centre), Eindhoven and imec, Leuven. The specific applications targeted are given below:

- Wearable bio-signal measurement systems based exclusively on flexible electronics
  - A heart-rate readout patch manufactured with flexible a-IGZO TFTs
  - A flexible ECG patch compatible with NFC RF communication

  In the above application cases, the full signal chain has been chosen to be implemented by flexible TFTs, as the ultimate goal is to develop an NFC enabled health patch that can be read by a smart phone, which will lead to an ultra-low cost solution.
- Flexible hybrid wearable multichannel bio-potential system
  - A multichannel hybrid flexible electronics EOG patch consisting of front ends on flexible foil and data processing using custom Silicon IC

  In this application case, the hybrid system approach has been chosen, as the goal is to explore the large area character of flexible TFTs with a more generic radio option which ultimately would require a Silicon based custom IC at the state-of-the-art.

1.5 Original contributions

The work presented in this manuscript advances the state-of-the-art in flexible unipolar technologies for bio-potential systems by introducing novel configurations at circuit and system level. The author's main contributions are highlighted as follows:

- In Chapter 3, the key design metrics in bio-signal front-end architectures, highlighting the trade-offs that are specifically relevant to a-IGZO TFT circuits, are discussed. Different front-ends for bio-signal sensing systems are designed and fabricated using a-IGZO TFT technology. The front-ends are characterized and compared in terms of different performance metrics, including power efficiency factor (PEF) (noise and power), input impedance and area. Based on this comparison, an insight into performance trade-offs in bio-signal front-ends in flexible technologies is obtained and optimum front-end architectures for different specific applications are highlighted.

- In Chapter 4, a novel idea of voltage to pulse width conversion with a simple and power minimalistic implementation is presented. A switched capacitor load has been exploited, in a modified single slope reset integrator circuit. The idea is further elaborated by implementing a heart-rate measurement interface for wearable applications, fabricated on a flexible foil with a-IGZO TFTs.

- In Chapter 5, we report for the first time (to the best of the authors' knowledge) a flexible ECG sensor which exploits TFT-based circuits on a flexible foil for the full chain of signal acquisition, amplification and digitization, and is capable to measure ECG signals. Additionally, a 105.9 kb/s Manchester encoded bit stream compatible with the NFC standard is generated at the output. The reported noise efficiency factor (NEF) and PEF are 109.81 and 1.20×10^5 respectively, which are the best values reported in literature for a-IGZO TFT circuits to date.

- In Chapter 6, a multichannel acquisition system for EOG is presented. The system, consisting of a frontend based on a-IGZO TFTs manufactured on flexible substrate, is interfaced with a Silicon based custom IC for digitization of the acquired signal. In this way the low cost, flexible form factor and the large area character of the flexible TFT technology are leveraged, while

utilising the complex computational capabilities of Si IC with low power dissipation. A tunable hybrid HPF has been integrated in the system which is used to block DC electrode offset and allows low high-pass cut-off frequency. The system is designed in a novel way to reduce the number of interconnects from the flexible system to the Silicon IC. There is basically only one differential signal and a reference interconnect required between TFT and Si IC, which reduces the area needed for interconnections on the Si chip, and thus cost.

- In Chapter 7, a novel digitally assisted tunable high pass filter for biomedical applications, using unipolar a-IGZO TFTs is presented. The proposed system is based on a master-slave approach. It takes advantage of the signal attenuation experienced in a high pass filter when a reference sinusoidal signal with a frequency lower than the cut off frequency is applied. The signal attenuation is monitored and a feedback loop automatically controls the small-signal resistance in the master and slave filters to obtain a specific signal attenuation, which in turn sets the passband frequency of the high pass filter. The presented approach is not only useful for setting a sub Hz cut off frequency but it is shown to be effective in counteracting parameter and supply voltage variations. The presented method can also be applied to Silicon-based circuits.

1.6 Outline of the thesis

The manuscript is organized in the following fashion: Chapter 2 presents the description of the technology with detailed TFT device structure, fabrication steps and device modelling. In Chapter 3, the design trade-offs in bio-signal sensing front-ends based on a-IGZO TFTs are presented. The front-ends are characterized and compared in terms of different performance metrics, giving insight into performance trade-offs in bio-signal front-ends in flexible technologies. Chapter

4 presents the design and characterization of a heart-rate measurement interface for wearable applications using a time domain reset integrator circuit. Chapter 5 focuses on the design and characterization of a flexible ECG patch implemented completely on foil, which is capable to acquire the ECG signals, amplify them and convert them to a sequence of bits. Chapter 6 shows the design and characterization of an EOG hybrid system composed of multichannel acquisition system on flexible foil, while digitization is done using a Silicon IC. In Chapter 7, a digitally assisted tunable high pass filter for biomedical applications, implemented using unipolar a-IGZO TFTs is presented. Finally, Chapter 8 draws the main conclusions of the thesis.

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Chapter 2

a-IGZO TFT Technology

In this Chapter, the a-IGZO TFT fabrication process developed at imec-NL/TNO (Holst Centre), Eindhoven and imec, Leuven, used in this thesis, is presented. Further, the details about the device stack of the TFTs are described. Finally, a brief overview of the physical-based compact models, used to describe channel current and noise of the TFTs, is given.

2.1 Introduction

The chosen technology in the work described in this thesis, uses TFTs fabricated with a-IGZO as semiconductor. Amorphous IGZO is a relatively new semiconducting material, which got international recognition from Hosono's work [1] in 2004. Since then, it has been extensively used in commercial applications such as active-matrix displays etc.

2.2 Device stack

The device stack here refers to the order in which different thin film layers are processed to fabricate a device. During the entire course of the work presented in this thesis, many variants of a-IGZO TFTs evolved in imec-NL/TNO (Holst Centre), Eindhoven and imec, Leuven. Out of those variants, depending on the availability, Etch-Stop Layer (ESL) TFTs and Dual-Gate Self Aligned (DUGA) TFTs were used for this work and will be discussed in detail below.

2.3 Etch stop layer TFT technology

The cross section of a typical device based on Etch Stop Layer (ESL) technology [2] is shown in Figure 2.1. It can be seen from the cross section that it has a staggered bottom-gate top-contact structure. All the layers are processed on top of a flexible polyimide substrate, with a maximum temperature of 250^{o}C.

In this device, a 100 nm Molybdenum-Chromium (MoCr) metal film, which acts as the gate layer (M1), is sputtered on top of the substrate. Next, a 200 nm SiO_2 gate dielectric is deposited by a plasma enhanced chemical vapor deposition (PECVD) process, which is followed by DC sputtering of a 12 nm thick IGZO layer. This is followed by spin coating a photoresist layer on top.

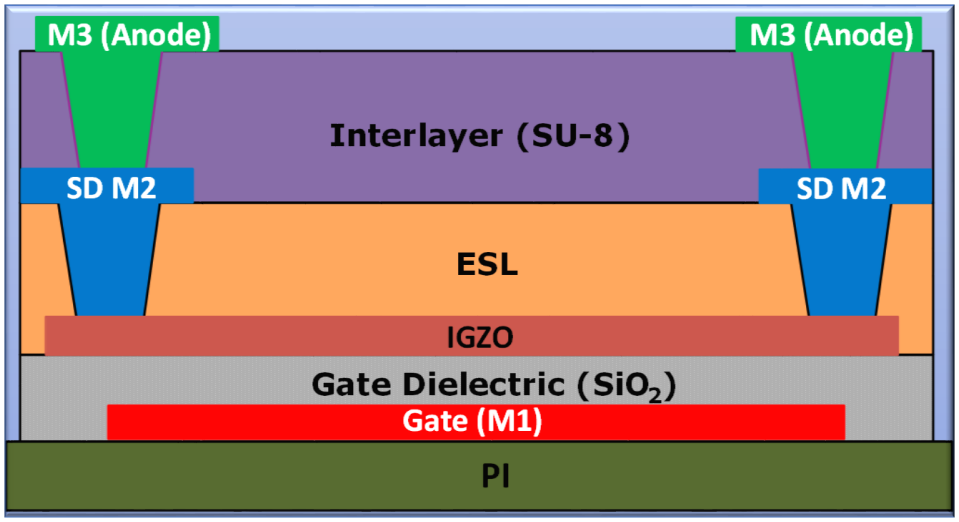

Figure 2.1: *Cross section of an a-IGZO TFT based on ESL flow.*

Next, a 100 nm SiO_2 layer is patterned on top of the semiconductor, using PECVD at 200°C. This layer, known as ESL, prevents damage of the semiconductor when processing the other layers. The contact openings are created using dry etching in the ESL layer, which is followed by sputtering of a second metal layer (M2) using MoCr target, resulting in formation of the source drain (SD) contacts. The next step is the deposition of a 2 μm thick SU-8 passivation layer (interlayer) on top of the second metal layer. This layer provides a low-capacitance insulation for the third metal, planarization and some protection from environmental influence.

Finally, a third metal layer (M3) (anode) can be optionally sputtered. This third metal layer can be very useful in wearables, e.g. to form integrated electrodes that pick up bio-potential signals on the surface of the TFT stack.

The TFTs based on the ESL technology suffer from two major drawbacks. Firstly, the accuracy in the processing steps necessitates margin between the transistor contact holes in the ESL layer and the source drain/metal layer, which results in a minimum channel length of 15 μm for single gate devices, whereas the minimum

feature size of this technology is 5 μm. The other drawback is the added parasitic capacitance due to the large overlap between gate and source/drain.

2.4 Dual-gate self aligned TFT technology

To achieve better speed performance and to solve the problems associated with the ESL TFT technology, the Dual-Gate Self Aligned (DUGA) stack [3] was developed. The cross-sectional view of a DUGA a-IGZO TFT is shown in Figure 2.2. The layer stack consists of a plastic substrate, a barrier layer, back gate (BG) metal M0, back gate dielectric, a-IGZO, top gate dielectric SiO_2, top gate (TG) metal M1, interlayer dielectric and source drain (SD) metal M2. The fabrication process starts with the deposition of a buffer layer on a polyimide plastic substrate. Then a BG metal (MoCr) is deposited by physical vapor deposition (PVD). This step is followed by deposition of the back gate dielectric (SiO_2) by PECVD at 350°C. The next step involves the deposition of the a-IGZO layer (20 nm with 10% ratio of O_2/Ar) by DC sputtering and patterning with wet etching.

After that, the top gate dielectric (SiO_2) is deposited using PECVD at 250°C, which is followed by TG metal (Mo) layer deposition. Afterwards, the top gate stack including metal layer and dielectric is patterned using wet and dry etch in a combined step. Then an interlayer dielectric (SiN_x) is deposited by PECVD at 250°C. Patterning of contact vias using dry etch follows. In the same step BG, TG and SD are contacted. The last step involves the deposition of SD (Ti-Al-Ti) metal using PVD and patterning by dry etching. Finally, annealing of the samples takes place at 240°C in N_2 for 1 hour.

The flexible polyimide substrate for the TFT process is hold on glass during manufacturing and released afterwards. The circuits realized in this way can be bent without significantly modifying their electrical characteristics [2].

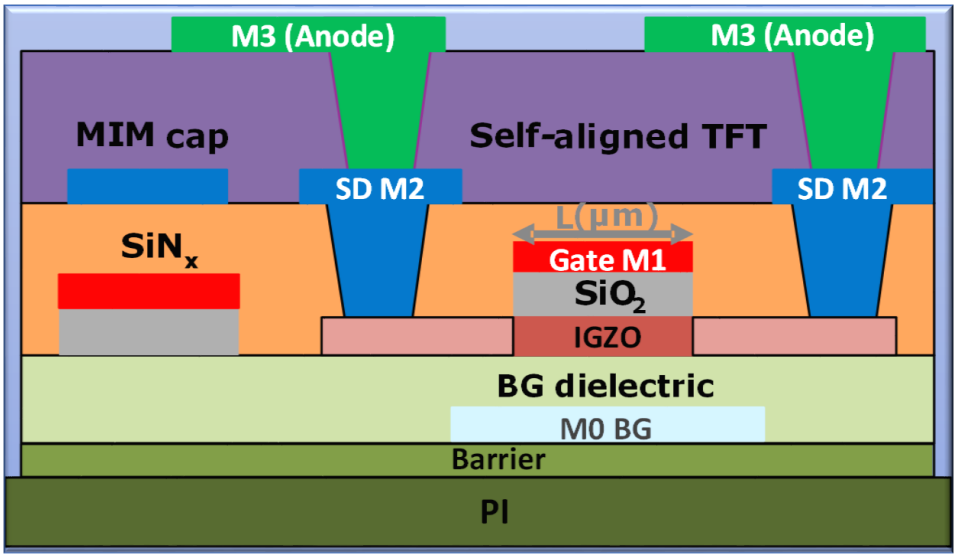

Figure 2.2: *Cross section of an a-IGZO TFT based on DUGA flow.*

2.5 Device channel current modelling

2.5.1 ESL channel current modelling

The analytical physical-based model described in [4] has been used to model channel current in ESL TFTs. The drift-diffusion drain current integral [5, 6] in the TFT can be modelled as

$$I_{DS} = \frac{W}{L}\int_{V_S}^{V_D}\int_{0}^{\varphi_s}\frac{q\mu_b n_b(\varphi, V_{ch})}{\sqrt{F_{xt}^2(\varphi, V_{ch}) + F_{xb}^2(\varphi, V_{ch})}} d\varphi dV_{ch} \tag{2.1}$$

where W is the channel width, L is the channel length, V_S and V_D are the source and the drain voltages, respectively, V_{ch} is the channel potential, φ is the electrostatic potential, φ_s is the surface potential at the insulator-semiconductor interface, n_b is the free charge carrier concentration, μ_b is the band mobility, F_{xt} and F_{xb}, are the electric fields calculated accounting for the trapped and the free charges, respectively. Solving Equation 2.1, taking into account both conduction regimes, the

drain current can be written as:

$$I_{DS} = \frac{W}{L} \frac{\Gamma_t \Psi_t \times \Gamma_b \Psi_b}{\Gamma_t \Psi_t + \Gamma_b \Psi_b} \tag{2.2}$$

where:

$$\Gamma_t = \frac{\varepsilon_s \mu_b N_b}{C_{ox}} k_B T \frac{T}{2T_t - T} \left[\frac{C_{ox}^2}{2\varepsilon_s N_t \theta_t k_B T_t} \right]^{\frac{T_t}{T}} \tag{2.3}$$

$$\Gamma_b = \frac{\mu_b C_{ox}}{2} \tag{2.4}$$

$$\Psi_t = \left[\phi_{GS}^{\frac{2T_t}{T}} - \phi_{GD}^{\frac{2T_t}{T}} \right] \tag{2.5}$$

$$\Psi_b = \left[\phi_{GS}^2 - \phi_{GD}^2 \right] \tag{2.6}$$

$$\phi_{GX} = V_G - V_{fb} - \varphi_{sX} \tag{2.7}$$

where μ_b is the band mobility, ε_s is the a-IGZO permittivity, N_b is the total number of delocalized (band) states, N_t is the total number of localized (trapped) states, T_t is the characteristic temperature of the localized states, θ_t accounts for the dependence of free and trapped charge concentrations on both T and T_t, $\mathrm{V_G}$ and $\mathrm{V_{fb}}$ are the gate and the flatband voltage, respectively, C_{ox} is the gate capacitance per unit area, φ_{sX}, with $X \in \{S, D\}$ is the surface potential at the source or drain.

Furthermore, it has been observed that the model overestimates the drain current due to contact effects. Hence, the contact model presented in [7] has been added to the model, which describes the contact effect as a reverse biased Schottky-gated diode as shown in Figure 2.3, and can be written as:

$$I_c = W \times I_0 \times \exp\left(\sqrt[4]{\frac{V_c}{V_0}} \right) \times \left[\exp\left(-\frac{qV_c}{\eta k_B T} \right) - 1 \right] \tag{2.8}$$

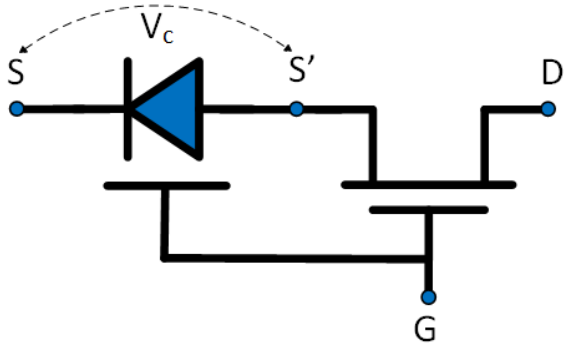

Figure 2.3: *Schematic device model including a reverse biased Schottky-gated diode.*

$$I_0 = I_{00} \times \left\{ \log \left[1 + \exp \left(\frac{V_G - V_{fb}}{V_{00}} \right) \right] \right\}^{\gamma} \tag{2.9}$$

where V_0 accounts for the Schottky barrier lowering effect, η is the quality factor, I_{00} is the reverse current prefactor, $V_{00} = 1$ and it is introduced to keep the dimensionality of the pre-factor I_{00} and γ is a fitting parameter.

Figure 2.4 shows the typical transfer characteristics of an ESL TFT with comparison between the model and the measurements. It can be seen that the model is in good agreement with the measurements.

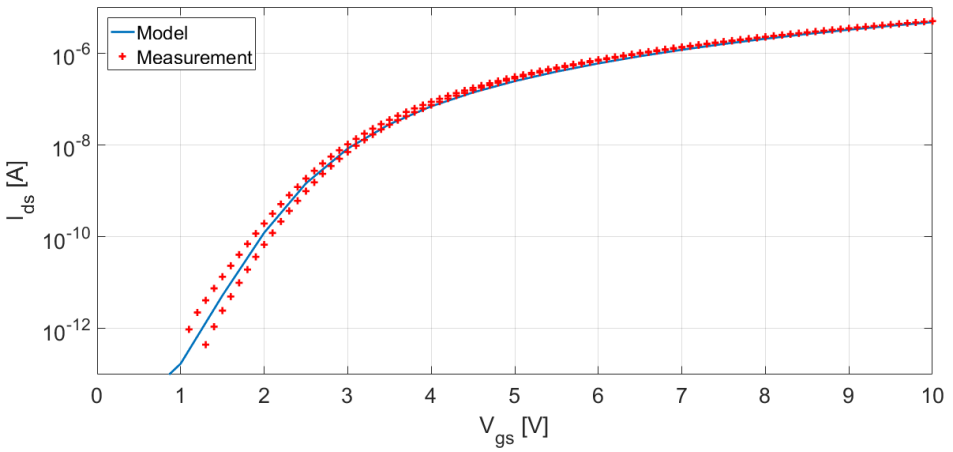

Figure 2.4: *Measured transfer characteristics of ESL TFT (in hysteresis mode) compared to model simulations.*

2.5.2 DUGA channel current modelling

The channel current model for DUGA TFTs developed by the Large Area Electronics group of imec, Leuven has been used in this thesis [8]. The channel current for a single TFT can be described as [9]:

$$I_{DS} = \frac{\mu_0 C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^{2+\gamma} \tag{2.10}$$

Equation 2.10 can be further written as:

$$I_{DS} = \frac{\mu_0 C_{ox}}{2} \frac{W}{L} [(V_{GS} - V_T)^{2+\gamma_S} - (V_{GD} - V_T)^{2+\gamma_D}] \tag{2.11}$$

The model represented by Equation 2.11 is further modified to incorporate sub-threshold behaviour and back gate model to finally obtain a complete DC model, described by the following Equations :

$$I_{DS} = \frac{\mu_{0S} C_{ox}}{2} \frac{W}{L} V_{GSTe}^{2+\gamma_S} - \frac{\mu_{0D} C_{ox}}{2} \frac{W}{L} V_{GDTe}^{2+\gamma_D} \tag{2.12}$$

$$V_{GXTe} = (2+\gamma_X) SS_X \log_{10} \left(1 + 10^{(\frac{V_G - V_X - V_{TX}}{(2+\gamma_X) SS_X})} \right) \tag{2.13}$$

$$V_{TX} = V_{T0} - \zeta (V_{BG} - V_X) \tag{2.14}$$

$$\gamma_X = \gamma_0 + \gamma_1 (V_{BG} - V_X) \tag{2.15}$$

$$\mu_{0X} = \mu_{00} + \mu_{01} (V_{BG} - V_X) + \mu_{02} (V_{BG} - V_X)^2 \tag{2.16}$$

$$SS_X = SS_0 + SS_1 (V_{BG} - V_X) \tag{2.17}$$

Equation 2.12 represents channel current behavior, Equation 2.13 describes subthreshold behavior while Equations 2.14, 2.15, 2.16 and 2.17 represents the shift caused by the backgate in V_T, γ, μ_0 and subthreshold slope (SS) respectively.

Figure 2.5 shows the transfer characteristics of a DUGA TFT with a comparison between the model and the measurements, when V_{BG} is varied between -5 V to 5 V. Also in this case, a good fit between the measurements and the model of the TFT is observed.

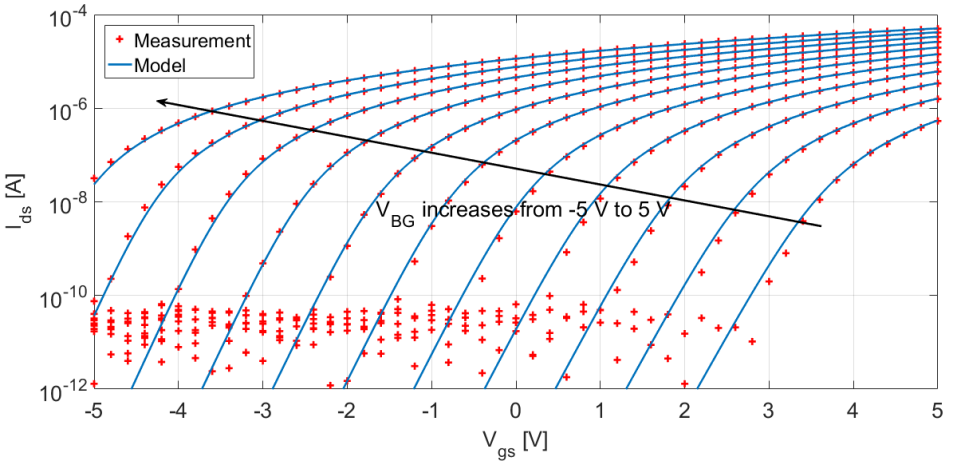

Figure 2.5: *Measured transfer characteristics of DUGA TFT compared to model simulations when V_{BG} is varied between -5 V to 5 V. Note that the points under 10^{-10} A are dominated by noise [8].*

2.6 Device noise modelling

The current noise behavior in field effect transistors can be modelled with two main contributions, which are related to the thermal and flicker noise. The power spectral density (PSD) of the drain current associated to the thermal noise contribution can be written as:

$$S_{I_D,thermal}(f) = 4k_BT\left(\frac{2}{3}\right)g_m \tag{2.18}$$

where k_B is the Boltzmann constant, T is the temperature, and g_m is the transconductance of the device.

However, the noise contribution in a-IGZO TFTs is generally dominated by flicker noise [10]. It has been shown in [10] that the mobility fluctuation model describes well the noise behaviour of a-IGZO TFTs. The flicker noise PSD in the a-IGZO TFTs' current can be modelled [11] as:

$$S_{I_D,flicker}(f) = \frac{\alpha_H q I_D^2}{fWLC_{ox}(V_{GS} - V_T)} \tag{2.19}$$

where α_H is the Hooge coefficient, I_D is the bias current, WL is the area of the device, C_{ox} is the channel capacitance per unit area and $V_{GS} - V_T$ is the overdrive voltage.

2.7 Conclusions

The a-IGZO TFT fabrication process used in this thesis has been presented in this Chapter. Furthermore, the a-IGZO TFTs based on etch stop layer and self aligned dual-gate stacks have been shown. Finally, compact models used to describe channel current and noise of the TFTs are described. The channel current models have been shown to be in good agreement with measurements.

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Chapter 3

Design Trade-offs in a-IGZO TFT based Bio-signal Front-ends

In this Chapter, four different bio-signal front-end circuits based on a-IGZO TFTs are designed, fabricated, measured and compared, focusing on three performance indicators which are in a trade-off: power efficiency factor (PEF), area occupation and input impedance.

The contents of this Chapter have been published in Flexible and Printed Electronics [1].

3.1 Introduction

A typical implementation of a bio-signal acquisition system requires sensors/electrodes, amplifiers, analogue signal processing blocks and analog-to-digital converter circuits in the full acquisition chain. The front-end amplifier is probably the most fundamental analogue building block that is inevitably present in every system. This Chapter deals with front-end amplifiers manufactured with a-IGZO TFTs on a flexible substrate.

As discussed in detail in Chapter 1, bio-signal acquisition systems on flexible substrates are inferior to mainstream Silicon technology in terms of performance, due to the low intrinsic gain, large parasitics and high flicker noise typical of flexible TFTs. However, it has been shown that bio-signal acquisition systems using TFTs on flexible substrate can achieve the accuracy required even for demanding biomedical applications such as electroencephalography (EEG) [2]. To implement bio-signal front-ends using flexible technologies, a technology-aware circuit design approach that takes into account the technology's peculiar characteristics, optimizing circuit functionality, is a must.

In this Chapter, we first discuss the key metrics in bio-signal front-end architectures, highlighting the trade-offs that become especially important when a-IGZO TFTs are used. We then discuss the realization of different front-ends for bio-signal sensing systems, designed and fabricated using a-IGZO TFT technology. The front-ends are characterized and compared in terms of different performance metrics, including noise, power, input impedance and area. Based on this comparison, we get insight into performance trade-offs in bio-signal front-ends in flexible technologies and highlight optimum front-end architectures for different specific applications.

The Chapter is organized as follows: in Section 3.2 design constraints for bio-signal front-ends are discussed together with the relevant trade-offs. Section 3.3 presents several bio-signal front-end architectures based on representative state-of-the-art designs, discussing their advantages and disadvantages. Section 3.4 gives a brief overview of the limitations of a-IGZO TFTs and the impact of their properties

on the design of bio-signal front-ends. Section 3.5 presents the chosen front-end topologies implemented with a-IGZO TFTs. Measurement results are presented and discussed in Section 3.6, and Section 3.7 gives the conclusions.

3.2 Design constraints for bio-signal front-ends

Bio-signal front-ends are mostly used to amplify weak bio-signals generated by muscular and neural tissues, in the typical range of 10 μV–10 mV, in the presence of DC electrode offset which may be as large as $\pm$300 mV, as well as motion artefacts. The bandwidth of bio-signals typically lies in the range of 0.5 Hz–5 kHz [3]. The bio-signal front-ends should meet many challenging requirements to extract the weak bio-signals with such a large DC offset. These requirements can be listed as follows:

- sufficient signal to noise ratio;
- low power dissipation for longer battery life;
- high input impedance to minimize signal attenuation from electrode to front-end;
- reduced area occupation for low cost and high spatial resolution depending upon the bio-signal monitoring application;
- removal of DC electrode offset to prevent saturation of the front-end;
- high common mode rejection ratio (CMRR) to reject interferers.

Low noise is required for an accurate measurement. In the low-frequency bio-signal band, 1/f noise is dominant, and thus circuit techniques such as chopping are used to suppress it below the thermal noise level. Consequently, the main noise contribution in Silicon front-end circuits becomes thermal noise. The input referred

spectral density of thermal noise in a transistor is given by:

$$\overline{v_n^2} = 4kT\gamma/g_m \tag{3.1}$$

where parameter γ depends on the bias point of the transistor and is typically assumed to be 2/3 in a transistor above threshold and in saturation. It can be seen from Equation 3.1 that the thermal noise spectral density in a transistor is inversely proportional to its transconductance g_m. The transconductance increases with a larger bias current. For this reason, a fundamental trade-off exists between noise and bias current, which is especially relevant to biomedical front-ends. This trade-off is typically characterized in amplifiers by a figure of merit called the noise efficiency factor (NEF) [4]:

$$\text{NEF} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi.U_T.4kT.\text{BW}}}, \tag{3.2}$$

where $V_{ni,rms}$ is the total input referred noise, I_{tot} is the total supply current of the amplifier, BW is the amplifier -3 dB bandwidth, and U_T is the thermal voltage. As it can be seen from Equation 3.2, the NEF does not take into account the supply voltage. For this reason, to compare circuits having a different supply voltage V_{DD}, the power efficiency factor (PEF) was introduced in [5]:

$$\text{PEF} = \text{NEF}^2 V_{DD}, \tag{3.3}$$

The PEF can be used to characterize the trade-off between noise and power consumption, and will be used in the later Sections of this Chapter to compare different a-IGZO front-ends. Another important requirement is that bio-signal front-ends should have a large input impedance Z_{in}, to minimize the signal attenuation from the electrodes to the front-end. Indeed, the input signal is partitioned between the electrode impedance and Z_{in}, and thus a large input impedance is desired, especially in ambulatory applications. We will use Z_{in} as a second figure of merit

to compare different a-IGZO front-ends. A third important parameter in the design of biomedical front-ends is their area occupation: a compact front-end may be cheaper to fabricate and enables higher spatial resolution, which in applications like e.g. electromyography (EMG), EEG and recordings of the neural cortex can be useful to improve diagnostic accuracy [6, 7]. The large DC electrode offset is another pressing problem often encountered in bio-signal front-ends. One obvious solution is to use AC coupled architectures, which inherently removes offset at the cost of large area to implement the input capacitors. CMRR is another important parameter in the design of bio-signal front-ends. It should be as large as possible to suppress coupling from the mains and other sources of interference.

From the above discussion, it is clear that PEF, input impedance and area are important parameters when designing biomedical front-ends. From now on in this Chapter, we will focus on these three parameters to compare different circuits for bio-signal sensing. The DC offset and CMRR are not considered to simplify the comparison. Section 3.3 will present a few typical biomedical front-end architectures, while Section 3.4 will discuss the trade-offs existing between these parameters when designing bio-signal front-ends using a-IGZO TFTs.

3.3 Bio-signal front-end architectures

Three most representative power efficient approaches for the design of biomedical front-ends in the recent literature, are illustrated in Figure 3.1. The architecture in Figure 3.1(a) uses an open-loop amplifier, A_1, to amplify the input signal. Given the low frequency range of biomedical signals (as low as 0.5 Hz), a very low high-pass corner $(1/(2\pi R_{in}C_{in}))$ is required, implying the need for a large $R_{in}C_{in}$. In addition, thanks to the low frequencies of bio-signals, chopping is a widely used technique to modulate the signal at higher frequencies and suppress the amplifier flicker noise and offset. In Figure 3.1, this is shown with CH_{in} and CH_{out} representing input and output chopper, respectively. In Figure 3.1(a), CH_{in} is placed

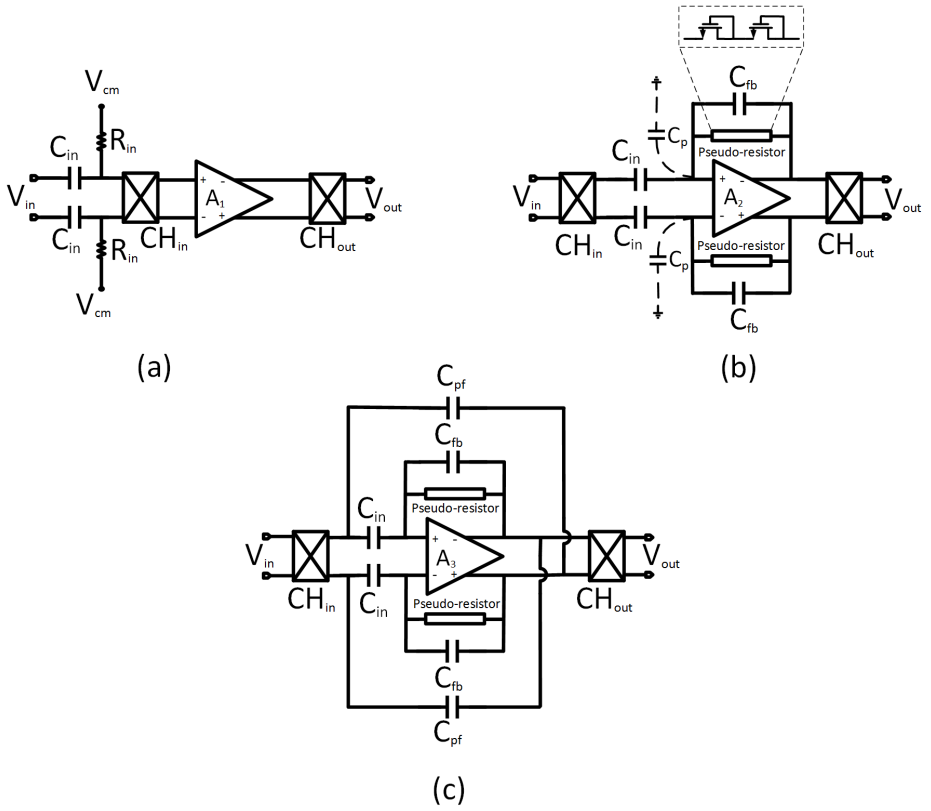


Figure 3.1: *Bio-signal front-ends implemented with (a) an open loop amplifier (b) an amplifier in capacitive feedback (c) an amplifier in capacitive feedback with additional impedance-boosting positive feedback loop.*

after the high-pass filter, to ensure the effectiveness of electrode offset blocking. However, using this approach, any mismatch in the capacitors C_{in} will affect the CMRR. In addition, this circuit exacerbates the negative role of the amplifier input parasitic capacitance C_p. Calling the chopping frequency f_{chop} and the input signal frequency f_{in}, the switched-capacitor resistor seen at the input of the amplifier due to the chopping of its input parasitic capacitance is $1/\left(2f_{\text{chop}}C_P\right)$ and, assuming that R_{in} is very large, the amount of input signal V_{in} coupled to the input of the amplifier can be approximated to be $V_{\text{Ain}} = \frac{j2\pi f_{\text{in}}C_{\text{in}}}{j2\pi f_{\text{in}}C_{\text{in}}+2f_{\text{chop}}C_p}V_{in}$. One should notice that typically $f_{\text{chop}} \gg f_{\text{in}}$. According to this equation thus, a very large C_{in} is needed to ensure negligible signal attenuation. To provide a numerical example, assuming

that f_{in} = 0.1 Hz, f_{chop} = 1 kHz, and C_p = 100 pF, to ensure 10% attenuation one would need C_{in} = 664 nF. This capacitance is so large that it cannot be integrated on foil with acceptable yield, at the state-of-the-art, and needs to be implemented using a discrete capacitor. In addition, the in-band input impedance of the overall front-end using chopping, $Z_{\text{in}} \approx 1/\left(2f_{\text{chop}}C_P\right)$, is limited due to the relatively high chopping frequency needed to ensure noise suppression. Discrete capacitors are often used in state-of-the-art reports of bio-signal front-ends implemented with TFTs [2]. Considering for example commercial ceramic SMD solutions, a 1 μF capacitor rated up to 50 V DC can be implemented in a 1.6×0.8 mm^2 footprint, with 0.8 mm height. These dimensions might still be compatible with flexible wearable solutions, provided that the capacitors are covered with a suitable e.g. silicone layer that covers the discrete components, smoothening the foil surface. Monolithic solutions, which are obviously more attractive from an integration and user-comfort perspective, would require adding a dedicated dielectric to the technology stack, which should offer a capacitance density significantly higher than the $\sim$ 10 nF mm^{-2} presently available with our technology.

Figure 3.1(b) depicts the use of an amplifier (A_2) in capacitive feedback, resulting in an accurate gain set by the ratio of passive elements C_{in}/C_{fb} [8, 9, 10]. Capacitors are preferred to resistors to realize the feedback because they do not introduce additional noise sources to the circuit. As the input capacitors in this case are behind the input chopper, their mismatch does not contribute to loss of CMRR. However, this architectural choice results in a DC-coupled amplifier, which is affected by a large output signal due to the input offset up-converted to the chopping frequency and amplified. This might jeopardize the linearity of the front-end. The effect of the electrode offset can be suppressed at the cost of increased circuit complexity using DC servo-loops (DSL), as proposed in [9, 10]. The highly resistive pseudo-resistors shown the inset of Figure 3.1(b) ensure biasing of the amplifier input pair. They should be large enough to ensure that the chopped signal is in the band pass of the closed-loop amplifier. The use of pseudo-resistors, which are

largely variable and bias dependant, results in a very inaccurate high-pass pole. Besides, the linearity of this stage might be jeopardized by the bias sensitivity of the pseudo-resistors. Instead of exploiting pseudo-resistors, a DSL can be used to implement the high-pass response in the closed-loop amplifier [9].

Obviously, noise and gain considerations are very important in determining the size of the capacitors. The input referred noise of the bio-signal front-end in Figure 3.1(b) is given by:

$$\overline{v_{ni}^2} = \left(\frac{C_{in}+C_{fb}+C_p}{C_{in}}\right)^2 \overline{v_{ni,A_2}^2} \tag{3.4}$$

where C_p is the input parasitic capacitance and $\overline{v_{ni,A_2}^2}$ the input referred noise of the main amplifier A_2. Equation 3.4 shows that the input referred noise of this front-end is an amplified version of the input referred noise of the amplifier. To minimize the total input referred noise, C_p must be minimized, and the mid-band gain, given by C_{in}/C_{fb}, should be as large as possible. For the front-end depicted in Figure 3.1(b), C_{in} can typically be integrated on foil, but still, according to Equation 3.4, it must be much larger than C_p and C_{fb}, resulting in large area occupancy and a limited input resistance. Indeed, the switching of C_{in} between positive and negative input every clock cycle requires a charging and discharging current from the signal source. Thus, the combination of input chopper and capacitors C_{in} results in the formation of a switched capacitor resistor offering an input impedance:

$$Z_{in} = \frac{1}{2f_{\text{chop}}C_{in}} \tag{3.5}$$

In the architecture of Figure 3.1(c), the input impedance is increased using a positive feedback loop (PFL) [10], realized by C_{pf}. The PFL supplies part of the current needed to charge the input capacitors at the chopping frequency. This current does not need to flow anymore from the input port, and thus the input impedance is increased. A drawback of this approach is that implementing the PFL results in area overhead due to the capacitors C_{pf}. Moreover, stability concerns in

the presence of parametric variability must be taken into account in this circuit. The condition for infinite input impedance [10] can be found to be:

$$C_{pf} = \frac{C_{in}}{G-1}, \tag{3.6}$$

where

$$G = \frac{A_3}{1+A_3\frac{C_{fb}}{C_{in}}}, \tag{3.7}$$

where A_3 is the open loop gain of the op-amp. Hence, the condition for stability from Equation 3.6 is:

$$C_{pf} < \frac{C_{in}}{G-1}, \tag{3.8}$$

Considering the analysis of the circuit in Figure 3.1(c), it can be observed that when A_3 is strongly variable and is not very large (as it will be the case in a-IGZO front-ends), a trade-off exists between improving input impedance and the risk of instability.

3.4 Limitations of a-IGZO TFT technology

In this Section, we discuss some of the limitations of a-IGZO TFTs and their impact on bio-signal measurement front-ends, with special focus on the trade-offs between PEF, input impedance and area occupation.

Considering the PEF, the fundamental difference between standard Silicon front-ends and a-IGZO TFT based front-ends is the noise corner frequency. In standard Silicon implementations, the noise corner frequency is lower than the bandwidth of the core amplifier and thus chopping frequencies larger than the noise corner frequency (f_c) can be used i.e. $f_{chop} > f_c$. This results in a front-end noise being defined by the thermal contribution only, and in an effective cancellation of the flicker noise. In contrast, a-IGZO TFT based front-ends have a noise corner frequency which is generally larger than the bandwidth of the amplifier. As a consequence, a-IGZO front-ends can only be chopped with $f_{chop} < f_c$, which means that

a-IGZO front-ends are 1/f noise dominated at the state-of-the-art: this additional flicker contribution to noise greatly degrades the PEF.

The input referred flicker noise voltage spectral density for a single TFT can be written as:

$$S_{n,in}(f) = \frac{2\alpha_H q}{C_i(\gamma+2)^2 W^{\frac{\gamma+3}{\gamma+2}} L^{\frac{\gamma+1}{\gamma+2}} f} \sqrt[\gamma+2]{\frac{I_{DS}}{\beta}} \tag{3.9}$$

The factor $\gamma+2$ is typically higher than 3 [11], which implies that a change in I_{DS} will not result in large change in 1/f noise, while an increase in device area will result in significant noise reduction. As the most effective strategy to alleviate 1/f noise in a-IGZO amplifiers is to increase the area of the input devices, a trade-off exists between noise level (thus PEF) and area. Another important point in a-IGZO TFT based front-ends is the fact that most a-IGZO technologies currently do not offer a self-aligned TFT stack, and thus a-IGZO TFTs are characterized by a large gate-drain overlap capacitance C_{gd}. In a gain stage as the ones depicted in Figure 3.1, the C_{gd} of the input TFTs will create Miller effect. This means that the actual parasitic capacitance from the input node to ground can be found to be:

$$C_p \approx (1+a)C_{gd} \tag{3.10}$$

where a is the gain between gate and drain of the input TFTs. In a single-stage amplifier the gain a will be equal to the total amplifier gain A_i, introduced in Section 3.3.

When using an amplifier in a closed-loop bio-signal front-end of the type introduced in Figures 3.1(b) and (c), according to Equation 3.4, the input equivalent noise increases due to the large C_p, and this effect must be counteracted by an increase of C_{in} (and C_{fb}), aggravating the trade-off between noise and area. On top of this, increasing C_{in} results in a decreased input impedance according to Equation 3.5, causing a trade-off between noise (and thus PEF) and input impedance.

To alleviate this trade-off, circuit techniques like impedance boosting introduced in Section 3.3 (Figure 3.1(c)) can be used, but this results in a consider-

able additional area overhead, in order to implement the capacitor banks needed to provide an accurate input impedance compensation. In summary, focusing on the main performance indicators PEF, area and input impedance, we can conclude that in bio-signal front-ends based on non-self-aligned a-IGZO TFTs the following trade-offs exist :

1. A trade-off between noise (PEF) and area due to:
    - the large TFTs needed to counteract 1/f noise;
    - the detrimental effect on noise of the large TFT parasitic capacitances C_p (exacerbated by the Miller effect) which can only be alleviated by larger C_{in}.
2. A trade-off between noise (PEF) and input impedance, due to the need to select large input capacitors C_{in} in the presence of a large parasitic TFT input capacitance C_p to ensure good noise performance.
3. A trade-off between input impedance and area, due to the area overhead needed to implement impedance boosting techniques such as the positive feedback described in Section 3.3.

As discussed before, the a-IGZO technology is unipolar. For this reason, specific amplifiers topologies must be used, taking inspiration from the work done in Silicon technology in the late 1970s when only NMOS devices were available. In the next Section, a set of bio-signal front-ends based on a-IGZO TFTs will be presented and analysed.

3.5 Bio-signal front-ends based on a-IGZO TFTs

Four biomedical front-ends exploiting the architectures shown in Figures 3.1(a) and (c) have been designed and implemented using a-IGZO TFTs. The first front-end (FE) uses a typical robust core amplifier architecture, the second one uses a

core amplifier similar to the first, but optimized for lower 1/f noise. The third and fourth FEs exploit amplifiers with a larger gain per stage. We explore three variants of core amplifiers using the open loop front-end architecture (Figure 3.1(a)), obtaining front-ends FE-I, FE-II and FE-III; and one topology of the core amplifier using the capacitive feedback front-end with impedance boosting (Figure 3.1(c)), obtaining FE-IV. The front-end schematics, including the topologies of the core amplifiers and the most relevant design parameters, are summarized in Figure 3.2 and Table 3.1 respectively. All front-ends are described in detail in the next Section. One should notice that all open-loop front-ends (FE-I, II and III) use discrete components to embody C_{in} and R_{in} ($R_{in} = 1\ M\Omega$ and $C_{in} = 4.7\ \mu F$). The bias current (I_{bias}) in FE-I, FE-II and FE-IV is implemented using n-type a-IGZO TFT based current mirror with an external current source.

3.5.1 FE-I and FE-II

As a first option for the implementation of a biomedical front-end, we explore the open-loop architecture of Figure 3.1(a) with a core amplifier A_1 based on a diode-connected load topology, as shown in Figure 3.2. As the gain of one stage is not sufficient for most of the applications, two stages are cascaded to obtain higher gain. Due to the moderate total gain and the fact that the gain is defined by a ratio of transconductances of matched devices $\left(A = \frac{g_{m1}}{g_{m3}}\right)$, this architecture is rather insensitive to general parameter variability, which is especially useful in the context of large area electronics due to its large variability. Two variants of the cascaded diode-connected load amplifier are considered: in the first front-end (FE-I), the input TFT pair is $\frac{500\ \mu m}{15\ \mu m}$, where the length is the minimum available in our technology to enable double-gate, and the width is chosen relatively small, to minimize C_P and its negative impact on input impedance. In the second front-end (FE-II), the input pair is made larger, $\frac{4000\ \mu m}{15\ \mu m}$, in order to reduce 1/f noise at the cost of increased C_p, resulting in $< 100\ \mu V_{rms}$ simulated integrated noise in the bio-signal frequency band.

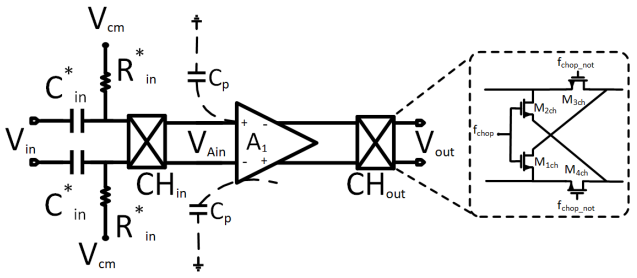
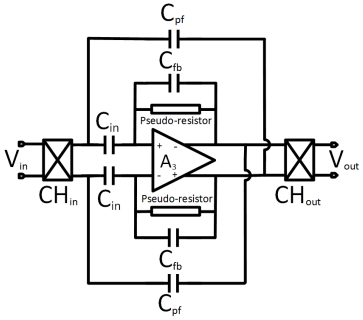
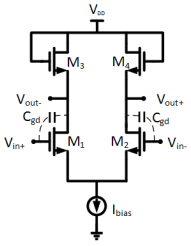
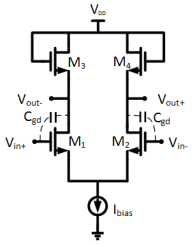
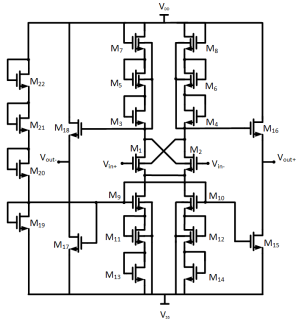
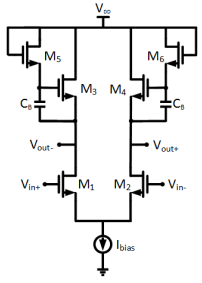
FE Architecture				
Core Amplifier	 2x in cascade ; $\left(\frac{W}{L}\right)_{M_1,M_2} = \frac{500\mu m}{15\mu m}$	 2x in cascade ; $\left(\frac{W}{L}\right)_{M_1,M_2} = \frac{4000\mu m}{15\mu m}$		
	FE-I	FE-II	FE-III	FE-IV

Figure 3.2: *Architectural schematics of the presented front-ends with structural details of the core amplifiers.*

3.5.2 FE-III

The next front-end is still an open-loop topology, where the core amplifier A_1 is based on an enhanced diode-connected load and positive feedback techniques to increase the amplifier gain, according to the topology reported in [11] and shown in Figure 3.2. This amplifier uses a modified diode-connected load consisting of series diodes M_3, M_5 and M_7 with the top gate of diode M_5 and M_7 connected to the source of M_3. In this configuration, the output resistance of M_5 is increased by a factor of $(1+\eta)$ and the output resistance of M_3 is increased by $(1+\eta)^2$ where η is the threshold modulation coefficient due to the presence of the top gate [11], which is typically larger than 2 for this technology. As the output resistance increases with this load arrangement, the DC gain also increases. The top gates of input transistors M_1 and M_2 are cross-coupled, creating a partial positive feedback which increases transconductance and, thus, gain.

At the output stage, a buffer, implemented with a source follower configuration (M_{16} and M_{18}), is used to interface the amplifier with the measurement setup. The supply voltage is divided by four through a voltage divider composed of M_{19} to M_{22}. This voltage is then used to bias the gates of M_9, M_{10}, M_{15} and M_{17}, which are used as tail current source for the amplifier stage and the buffers.

Although this topology effectively enhances gain, it is sensitive to mismatch and variations. Indeed, the introduction of positive feedback in presence of large mismatch and variability may result in instability. Besides, as this amplifier has a low-pass response and large gain, the input DC offset of the amplifier, due to the large mismatch present in a-IGZO TFT technology can be amplified enough to saturate the stage. Another drawback of this architecture is limited available output swing which often necessitates higher supply voltages.

3.5.3 FE-IV

The last front-end is designed according to the impedance-boosting capacitive feedback architecture of Figure 3.1(c). The core amplifier A_3 is implemented with the

Table 3.1: *Relevant design parameters of the presented front-ends.*

	FE-I	FE-II	FE-III	FE-IV
C_{in} [pF]	4.7x10^{6}[a]	4.7x10^{6}[a]	4.7x10^{6}[a]	10
C_{fb} [pF]	-	-	-	1
C_{pf} [pF]	-	-	-	0.8
C_B [nF]	-	-	-	1
W_1/L_1 [$\mu m/\mu m$]	500/15	4000/15	5000/15	500/15

[a]These capacitors are implemented using discrete components.

bootstrapped load amplifier shown in Figure 3.2. This topology, proposed in [12] uses a load consisting of M_3 and M_5 with a bootstrapping capacitor C_B. At low frequencies, M_3 behaves as a diode-connected load which is less sensitive to threshold variations due to its low gain, while at high frequencies it behaves as a zero-V_{GS} load which provides higher gain. This topology has, thus, a characteristic band pass response, which is desirable to avoid saturation of the core amplifier due to the TFT mismatch.

3.6 Measurement results

The front-ends presented in the previous Section have been designed and fabricated using a-IGZO TFTs on foil. The foil micrographs of the presented circuits are shown in Figure 3.3.

In this Section, the measurements of these circuits are discussed. Figure 3.4 shows the measured frequency response of the bio-signal front-ends, using the whole FE architectures as shown in Figure 3.2, keeping the chopping off. Figures 3.4(a) and (b) show the gain plots of the two-stage cascaded diode-connected load amplifier in FE-I and FE-II respectively. The gain of the amplifier in FE-I is 22.9 dB with a -3 dB frequency of 6.8 kHz, while for the amplifier with larger input TFTs, the gain is 26.9 dB with a -3 dB frequency of 4 kHz. Figure 3.4(c) plots the frequency response of the enhanced diode-connected load amplifier. It shows a gain of 25.2 dB in a single stage, with a -3 dB frequency of 400 Hz. The GBW

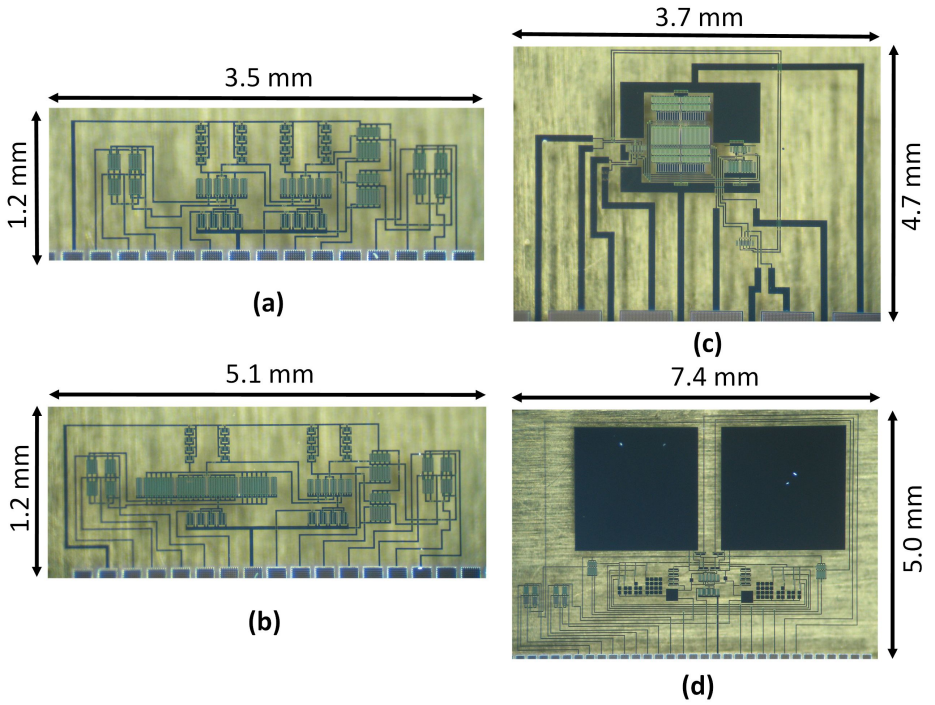


Figure 3.3: *Foil micrograph of the fabricated front-ends (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV.*

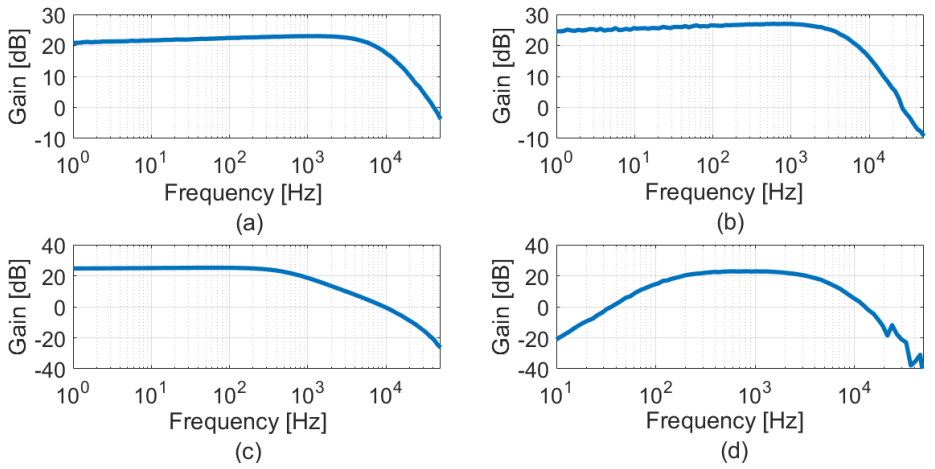


Figure 3.4: *Frequency response of the amplifiers (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV.*

is reduced compared to the conventional diode-connected load due to the stronger Miller effect on the input devices observed in this single-stage topology. The last

plot of Figure 3.4(d) shows the frequency response of the bootstrapped amplifier with feedback network again without chopping. The lower and upper cut off frequency are 185 Hz and 3.3 kHz respectively with a mid-band gain of 22.8 dB. This value is slightly different from the theoretical one, C_{in}/C_{fb}, due to the parasitic TFT capacitances. Owing to the rather small capacitances C_B (1 nF) used in the design and the limited output resistance of the diode-connected devices M_5 and M_6, the high-pass corner of the bootstrapped amplifier is at a rather high frequency (185 Hz). Such a high-pass is not compatible with low frequency biomedical signals like EMG and ECG. To cope with these signals, larger C_B capacitors, and/or a biasing of $M_{5/6}$ ensuring higher output resistance should be used.

As mentioned earlier, it should also be noted that the first two amplifiers are two-stage while the last two are single stage. Besides, the last front-end is measured in closed-loop and thus its bandwidth is enhanced at the expense of gain.

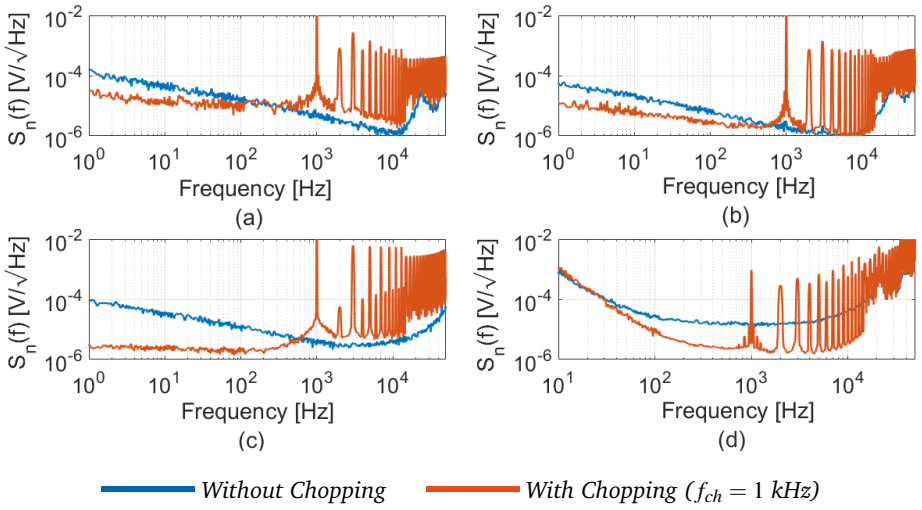


Figure 3.5: *Input referred noise density of the different front-ends (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV.*

Figure 3.5 represents the input referred noise spectral density of the front-ends discussed, with choppers deactivated (in blue), and activated (in red). Figure 3.5(a) shows the input noise density of FE-I (based on the diode-connected load amplifier). The input noise density without chopping shows a 1/f behaviour start-

ing from 147 $\mu V/\sqrt{Hz}$ at 1 Hz and reaching 5 $\mu V/\sqrt{Hz}$ at 1 kHz. When chopping at 1 kHz is applied, the noise spectral density becomes almost flat with a floor of around 14 $\mu V\sqrt{Hz}$ until 1 kHz (Figure 3.5(a), red line). The total equivalent input referred integrated noise in a bandwidth of 1–200 Hz with chopping at 1 kHz is 176.9 μV_{rms}. Figure 3.5(b) shows the input noise density of FE-II (based on a diode-connected load amplifier with large input devices). As expected, the noise density without chopping (blue line) follows the same trend as in the previous case, but with a 2.5x reduction in the noise, thanks to increased area of the input pair. In this case, the input noise density without chopping is 58 $\mu V/\sqrt{Hz}$ at 1 Hz reducing to around 2 $\mu V/\sqrt{Hz}$ at 1 kHz. The total equivalent input referred integrated noise of FE-II in a bandwidth of 1–200 Hz with chopping at 1 kHz is 51.2 μV_{rms} (Figure 3.5(b), red line).

Figure 3.5(c) shows the input noise spectral density of FE-III, built with the modified diode-connected load amplifier. The noise spectral density at 1 Hz is 92.4 $\mu V/\sqrt{Hz}$. The application of 1 kHz chopping results in a total equivalent input referred integrated noise of 29.2 μV_{rms} in a bandwidth of 1–200 Hz. The improved noise behaviour offered by the modified diode-connected load amplifier compared to the normal diode-connected load amplifiers is due to the 10x larger size of the input pair. The last plot, Figure 3.5(d), shows the input noise spectral density of FE-IV, based on the bootstrapped load amplifier. The measurement without chopping shows a trend decreasing in frequency until the lower cut off frequency of 185 Hz and almost a flat floor of 15 $\mu V/\sqrt{Hz}$ till the upper cut off frequency of 3.3 kHz. The total equivalent input referred noise integrated in a bandwidth of 400–600 Hz (a 200 Hz bandwidth in the maximum gain region for comparison with the other FEs), applying chopping at 1 kHz, is 34.7 μV_{rms}.

Figure 3.6 shows the input impedance vs frequency for the presented front-ends with (red line) and without (blue line) chopping. Figures 3.6(a) and (b) show the input impedance plots of FE-I and FE-II, respectively. The input impedance of the version 1 diode-connected load amplifier at 1 Hz in absence of chopping is 540

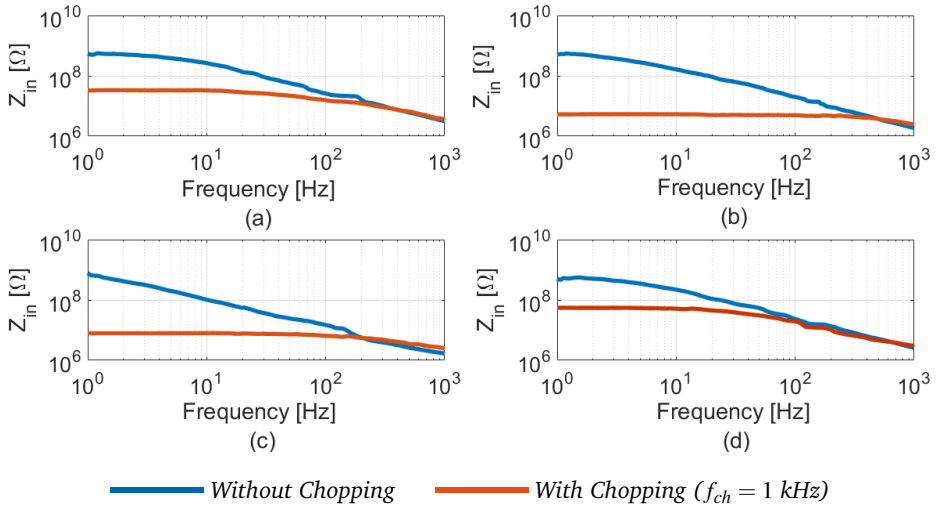


Figure 3.6: *Input impedance of the different front-ends (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV.*

$M\Omega$ while application of 1 kHz chopping reduces the input impedance to 33.1 $M\Omega$. In case of the version 2 diode-connected load amplifier, the input impedance at 1 Hz reduces from 499 $M\Omega$ to 5.3 $M\Omega$ with the application of chopping at 1 kHz, which is expected due to the large input pair and its large parasitic capacitance. Figure 3.6(c) shows the input impedance vs frequency plot of the modified diode-connected load FE-III. In this case, the input impedance at 1 Hz reduces from 791 $M\Omega$ to 7.9 $M\Omega$ with the application of chopping at 1 kHz, owing to the large parasitic capacitance due to Miller effect and due to the large input pair. The last plot of Figure 3.6(d) shows the input impedance versus frequency for FE-IV. The input impedance at 1 Hz without chopping is 508 $M\Omega$, which decreases to 55.3 $M\Omega$ when chopping at 1 kHz is applied. In this front-end, the input impedance after chopping is better compared to the other cases thanks to the PFL impedance boosting.

All the parameters measured in the front-ends presented in this work are summarized in Table 3.2 along with a comparison with the state-of-the-art bio-signal front-ends in similar flexible technologies, where the three main performance indicators: PEF, area, and input impedance are highlighted. These three parameters

which, as explained in Section 3.4, are in trade-off, are also shown in a radar plot in Figure 3.7 for the front-ends discussed here. As the best PEF is the lowest, the PEF axis is plotted in inverse order, so that the best front-end would cover the largest surface in the radar plot. For the sake of comparison, one should remember that FE-I, FE-II and FE-III use external discrete capacitors.

Clearly, FE-I with the cascaded diode-connected load amplifier version 1 has the worst PEF performance, while FE-II and FE-III, with diode-connected load version 2 and modified diode-connected load amplifier respectively, are similar. In fact, the former has a higher noise (due to the fact that its gain is divided in two cascaded stages and thus more TFTs contribute to noise) but lower power consumption compared to the latter (which stacks many TFTs between the rails and thus needs larger supply voltage).

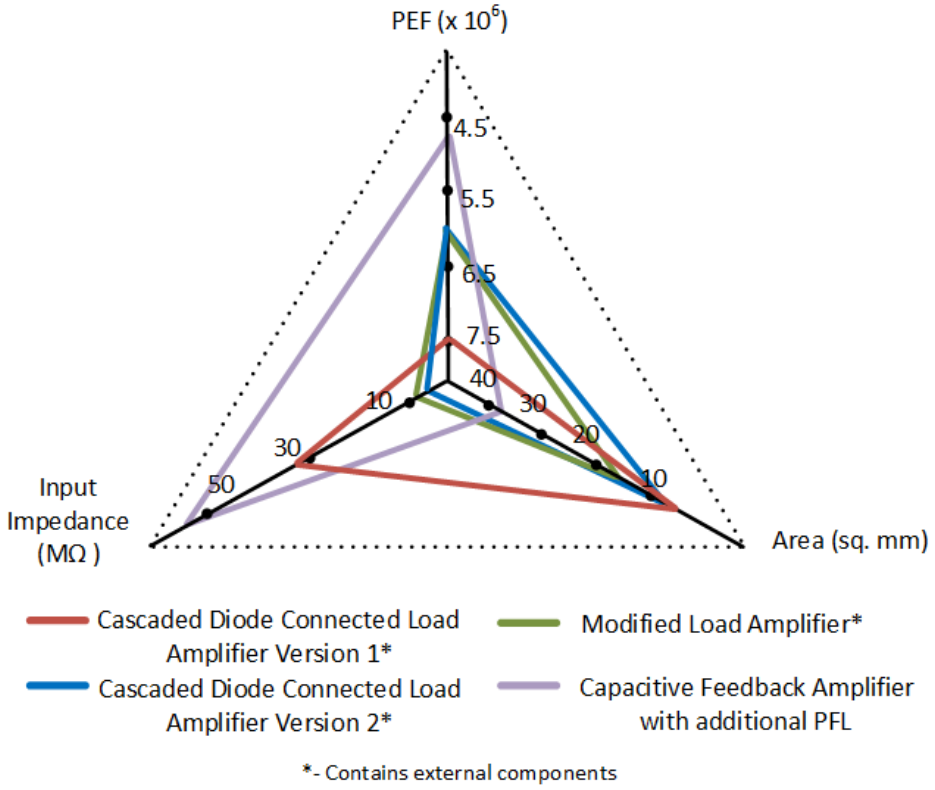


Figure 3.7: *Performance comparison of the presented front-ends.*

The capacitive feedback FE-IV with input impedance boosting and bootstrapped amplifier achieves the best PEF. This is due to the fact that the bootstrapped amplifier provides high maximum gain in one stage (minimizing the noise contributions of the TFTs after the input pair) using only two stacked TFTs, and thus with no need for a high voltage supply. When it comes to input impedance, FE-IV with the capacitive feedback amplifier with impedance boosting again demonstrates the best performance, thanks to the impedance-boosting positive feedback technique employed, albeit, at the expense of area for the positive feedback network. It should be noted that the use of positive feedback in a technology that suffers from high parametric variability requires extra attention to stability issues. The area consumption of FE-IV is exacerbated by the use of the bootstrapped amplifier, which needs large capacitors C_B (1 nF) to shorten gate and source of the load TFT at the signal frequency. Still, this FE is the only one which is fully integrated on foil. The other FEs need external discrete capacitors to implement C_{in}. Finally, our work is compared to relevant the state-of-the-art bio-signal measurement solutions implemented on foil [2, 13, 14, 15] and listed in Table 3.2. The NEF measured in our front-ends is in line with other a-IGZO references, while the NEF of [2] is better thanks to the lower 1/f noise offered by that technology. The PEF of our front-ends is actually lower than the one reported in all previous art. FE-III achieves this result exploiting a moderate supply voltage and a design that reduces 1/f noise by increasing the size of the input devices. FE-II and FE-IV use an even lower power supply (enabled by the simple structure of the amplifiers used in these FEs) and a noise-optimized sizing of the input TFTs. Also, all our FEs use a limited bias current, as their thermal noise is not dominant, and benefit from the better mobility of a-IGZO compared to the technologies used in [2] and [13].

3.7 Conclusions

For applications where area is not a critical factor because only few bio-signal measurement channels are required, the capacitive feedback architecture with impedance boosting based on the bootstrapped load amplifier represents an attractive solution, due to better PEF and high input impedance. One of the obvious disadvantages of this solution is guaranteeing stability of the front-end in presence of variability and mismatch. However, when high resolution electrode matrices are necessary, the minimum required electrode pitch sets a strict requirement on area. In such applications, e.g. high resolution surface EMG, other options should be explored, like the front-ends II and III discussed in this Chapter. These front-ends, based on diode-connected load amplifiers with and without output impedance enhancement, should be carefully optimized for the noise, power and input impedance requirements, based on the characteristics of the flexible technology employed and based on the specifications of the envisaged application. Also, they need two discrete capacitors each, which might add to the cost and decrease the flexibility of the final solution. In conclusion, the diode-connected load amplifiers with cascaded stages offer a good compromise between performance and robustness. Hence, this topology has been chosen to be implemented in full system architectures, presented in the following Chapters of this thesis.

Table 3.2: *Performance comparison of the presented front-ends with the state-of-the-art.*

Parameter	This work				[2]	[13]	[14]	[15]
	FE- I	**FE-II**	**FE-III**	**FE-IV**				
Technology	a-IGZO				a-Si	DNTT	a-IGZO	a-IGZO
Amplifier maximum gain [dB]	22.9	26.9	25.2	22.8	20	27	22	24.9-23.1
Amplifier bandwidth	6.8 kHz	4 kHz	400 Hz	185 Hz-3.3 kHz	200 Hz	90 Hz	3 kHz	5.4 kHz-5.2 kHz
Chopping frequency [kHz]	1	1	1	1	5	-	0.5	5-8
Input referred noise [μV_{rms}] with chopping (BW)	176.9 (1–200 Hz)	51.9 (1–200 Hz)	29.2(1–200 Hz)	34.7(400–600 Hz)	2.3(1–100 Hz)	-	92.5(1–200 Hz)	125–31.4 (1–500 Hz)
Z_{in} with chopping [MΩ]	33.1	5.3	7.9	55.3	-	-	-	29.6-23
Bias current [μA]	3.2	2.6	3.1	5.2	200	15	3.2	50
Supply voltage [V]	10	10	±13	10	55	2	10	±13
NEF	868.8	226.6	141.1	217.2	126.3	-	454.3	385.5[a]
PEF	7.5 x 10^6	5.1 x 10^5	5.1 x 10^5	4.7 x 10^5	8.7 x 10^5	-	2.0 x 10^6	3.8 x 10^{6a}
Area [mm^2]	4.2	6.1	17.4	37.0	-	100.0	5.4	11.2
External components required	Yes	Yes	Yes	No	Yes	Yes	Yes	No

[a] Considering 31.4 μV_{rms} in 500 Hz bandwidth.

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Chapter 4

A Heart-Rate Measurement Interface on a Flexible Foil

This Chapter deals with two time based interfaces based on a reset integrator, for bio-signal acquisition using a-IGZO TFTs. The initial part of the Chapter presents a heart-rate measurement interface for wearable applications, fabricated on a flexible foil, that requires a moderate SNR (as low as 6 dB). The output is provided as a PWM waveform. Voltage to pulse-width conversion is achieved with a simple and power minimalistic approach, using a reset integrator.

This approach can be further refined to serve applications that are more demanding in terms of SNR. In the later part of this Chapter, SNR is improved by applying correlated double sampling (CDS) to enable ECG monitoring. A low power flexible ECG interface incorporating CDS has been studied in simulations.

The contents of this Chapter have been published in ESSCIRC 2018 [1] and IWASI 2019 [2] conference proceedings.

4.1 Introduction

Wearable electronic devices are gaining a growing research interest and popularity. Wearable devices should be flexible and conformable to the human body, to increase user comfort. Amorphous Indium Gallium Zinc Oxide (a-IGZO) Thin Film Transistors (TFTs) technologies are very suitable platforms to develop electronic devices for these kind of applications due their flexibility, robustness to mechanical stress and low manufacturing cost.

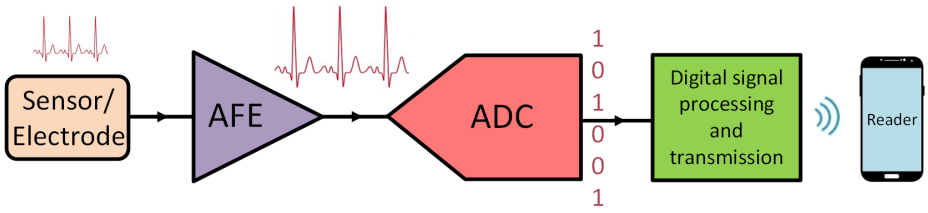

Figure 4.1: *General bio-signal acquisition system architecture.*

Figure 4.1 shows the general architecture of a bio-signal acquisition system. The system typically consists of a sensor/electrode, an analogue front-end (AFE), an analogue to digital converter (ADC), a digital signal processing and transmission block, and a reader. The sensor/electrode converts an external analogue quantity into either a current or a voltage signal. The output signal of the sensor/electrode is generally low in amplitude, hence, it is amplified through an AFE. Conversion to digital representation is essential before transmitting signals to a reader device (e.g. smart phone), to increase noise immunity during transmission. This analogue-to-digital conversion and transmission process is performed by an ADC and a digital signal processing and transmission block.

In Chapter 3, we have already discussed analogue front-ends. This Chapter deals with conversion of an input signal to a binary pulse width modulated (PWM) representation, which can further be quantised in time to get a digital representation (to be discussed in Chapter 5). In Silicon-based bio-signal acquisition systems, the digitization of the input data is generally done in the voltage domain, as stable

voltage references are available. But, it is difficult to make a voltage reference in a-IGZO at the state-of-the-art. Hence, we prefer to digitize the input data in time domain, as a time reference can be easily generated in a-IGZO [3], for instance based on a received NFC carrier. Besides, in this technology, the time domain conversion of an analogue signal to the digital representation is much simpler to implement than the voltage domain conversion. Thus, after the AFE, a reset integrator is used to transform the signal amplitude in duty cycle information i.e. PWM representation. The binary PWM representation can be transformed to a digital representation by counting the number of clock cycles the integrator output is high every period (to be discussed in Chapter 5).

Bio-signal acquisition systems designed and fabricated using flexible TFT technologies have been presented in [4, 5] but the signals in these works are not digitized within the system on foil. Moreover, the power consumption reported in [4] is 11 mW, which is quite high for wearable applications. The input signal is transformed to analogue PWM representation in [6] but power consumption is still 2 mW, and the circuit does not provide a voltage, but a current input, making it inconvenient to measure bio-potentials. In this Chapter, the analogue output from a voltage-sensitive front-end is converted to an analogue PWM representation with low power consumption and using a hardware minimalistic approach.

The rest of the Chapter is organized as follows: In Section 4.2, an introduction to the reset integrator is provided, together with the experimental characterization of a first implementation. Section 4.3 discusses the system architecture and circuit design of the heart-rate measurement interface on flexible foil, that is based on the reset integrator circuit, and presents its experimental measurement results including *in-vivo* characterization. Section 4.4 presents an improved version of the previous system with better noise performance, analyzing its performance through simulations. Finally, Section 4.5 concludes the Chapter.

4.2 Single slope reset integrator

4.2.1 Principle of operation

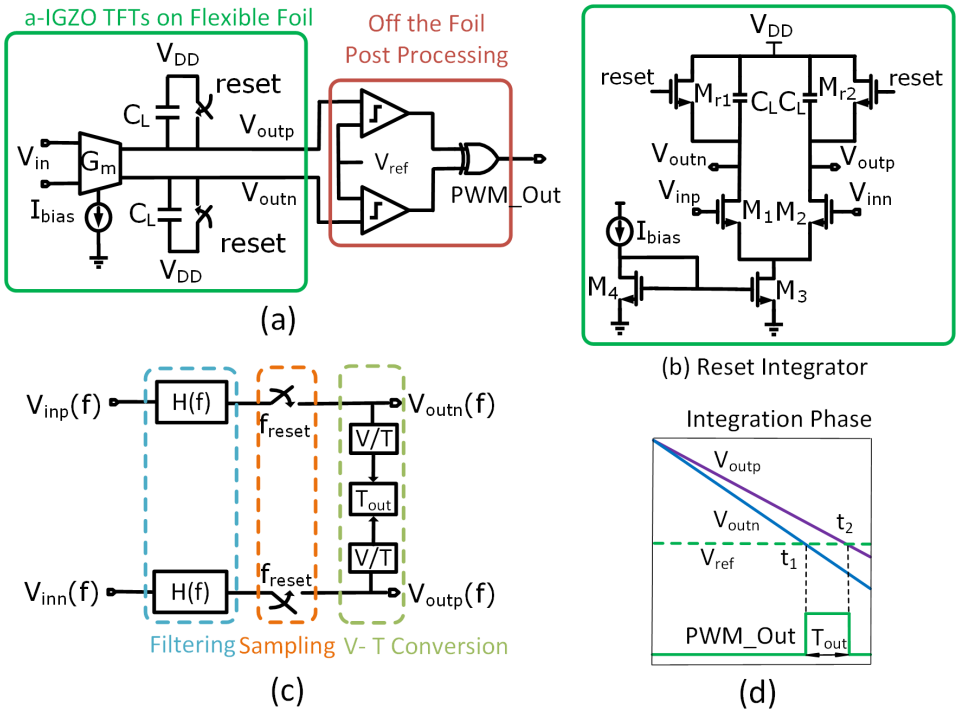

Figure 4.2: *(a) Architecture of the single slope reset integrator, (b) Circuit schematic of the single slope reset integrator, (c) Functionality of the reset integrator in terms of signal processing operations, (d) Principle of operation.*

The unavailability of active loads in unipolar technologies, as discussed in Chapter 1, motivated us to investigate a switched capacitor load in this technology. The basic idea is shown in Figure 4.2. Figure 4.2(a) shows the conceptual schematic of a reset integrator, which uses a switched capacitor load. The circuit schematic is presented in Figure 4.2(b), while the principle of operation is shown in Figure 4.2(d). The output drain currents are integrated on load capacitors C_L during the integration phase. The moments in which the integrator outputs (V_{outn}, V_{outp}) are discharged below a given threshold V_{ref} can be detected by comparators. The integrator outputs are periodically reset to V_{DD}. The time delay in threshold crossing

between both branches of the integrator output, T_{out}, is proportional to the input signal. Thus, the reset integrator circuit transforms a voltage input signal (V_{in}) to a PWM output signal (T_{out}).

The voltage to pulse width conversion produces a PWM waveform which can have variable pulse widths depending on the sampled input signal with a fixed sampling frequency. Hence, the output PWM representation is a continuous-amplitude version of the input signal, but sampled in time. So, the output PWM representation discussed in this Chapter is still not a digital representation. The sampling in the integrator will result in aliasing but, as there is no digitization, there will be no quantization noise.

The basic operation of the reset integrator can be represented by three subsequent signal processing operations as shown in Figure 4.2(c): filtering due to integration of the signal current within a integration period, followed by output voltage sampling at a rate f_{reset} and finally voltage to time conversion.

Assuming ideal integration of the input currents on the load capacitors (C_L), the time-domain output voltage of the reset integrator at the n^{th} sampling moment (considering G_m as the transconductance, $f_{reset} = f_s = 1/T_s$ and integration time = T_{int}) can be written as:

$$V_{out}(t = nT_s) = V_{DD} - \frac{1}{C_L} \cdot \int_{nT_s - T_{int}}^{nT_s} I_{int}(\tau) d\tau = V_{DD} - \frac{G_m}{C_L} \cdot \int_{nT_s - T_{int}}^{nT_s} V_{in}(\tau) d\tau \qquad (4.1)$$

The integration of current samples within an integration window results in a sinc LPF response as shown in Figure 4.3. The ideal magnitude transfer function of this response can be expressed as:

$$H(f) = \left| \frac{V_{out(f)}}{V_{in(f)}} \right| = \frac{G_m}{C_L} \left| \frac{\sin(\pi f T_{int})}{\pi f} \right| \qquad (4.2)$$

As shown in Figure 4.3, the periodic integration of the current produces notches in the frequency response, which are at multiples of the inverse of the integration

period ($1/T_{int}$). It can be seen that with equal -3 dB bandwidths and equal voltage gains, the sinc lowpass response attenuates out of band frequency components more than a first order RC lowpass response. The ideal -3 dB bandwidth of the low-pass sinc response is approximately $0.44/T_{int}$ [7]. It should be noted that the -3 dB bandwidth in this case is ideally determined only by T_{int}.

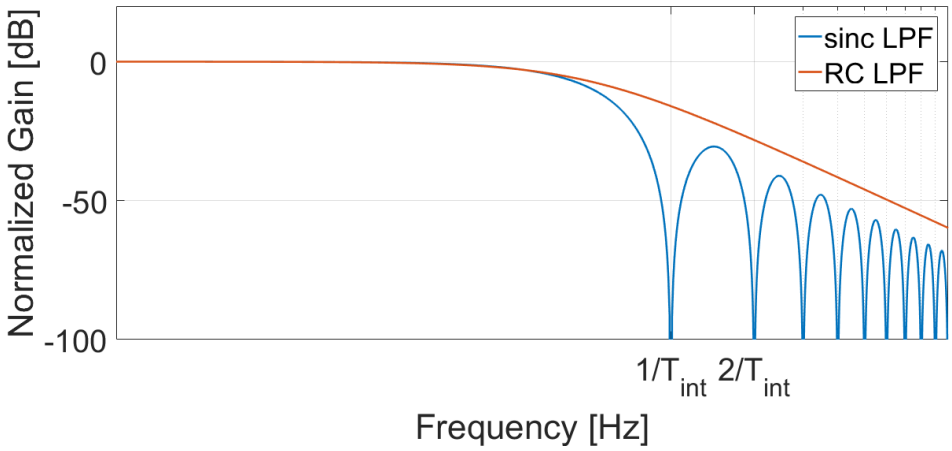

Figure 4.3: *Comparison of sinc LPF response with RC LPF response.*

The relationship between T_{out} and V_{in} can be obtained as (Figure 4.2(d)):

$$V_{\text{outn}} = V_{DD} - \frac{\frac{I_{bias}}{2} + \frac{g_m V_{in}}{2}}{C_L} t_1 \tag{4.3}$$

$$V_{\text{outp}} = V_{DD} - \frac{\frac{I_{bias}}{2} - \frac{g_m V_{in}}{2}}{C_L} t_2 \tag{4.4}$$

$$\text{At } V_{ref} : V_{\text{outn}} = V_{\text{outn}} = V_{ref} \tag{4.5}$$

$$V_{DD} - \frac{\frac{I_{bias}}{2} + \frac{g_m V_{in}}{2}}{C_L} t_1 = V_{DD} - \frac{\frac{I_{bias}}{2} - \frac{g_m V_{in}}{2}}{C_L} t_2 \tag{4.6}$$

$$\frac{I_{\text{bias}}}{2} (t_2 - t_1) = \frac{g_m V_{in}}{2} (t_1 + t_2) \tag{4.7}$$

Considering, $CV = It$ and taking the average of t_1 and t_2, we obtain:

$$C_L\left(V_{DD} - V_{ref}\right) = \frac{I_{\text{bias}}}{2}\left(\frac{t_1 + t_2}{2}\right) \tag{4.8}$$

$$t_1 + t_2 = \frac{4C_L}{I_{\text{bias}}}\left(V_{DD} - V_{ref}\right) \tag{4.9}$$

Using the value of $t_1 + t_2$ from Equation 4.9 in Equation 4.7, we can write:

$$\frac{T_{out}}{V_{in}} = \frac{4g_m C_L(V_{DD} - V_{ref})}{I_{bias}^2} \quad [\text{s/V}] \qquad (where,\ T_{out} = t_2 - t_1) \tag{4.10}$$

where T_{out} is the output pulse width, V_{in} is the differential input signal, g_m is the transconductance of the input transistor in the integrator, C_L is the load capacitor, V_{DD} is the supply voltage of the integrator and I_{bias} is the tail bias current in the integrator. It should be noted that Equation 4.10 is only valid in pass-band, as the input is assumed to be constant.

The presented idea is inspired by the integrating amplifier (dynamic amplifier) introduced in [8], which has become very popular in the last 10 years especially in the application as a residue amplifier for ADCs. A differential dynamic amplifier using a common-mode voltage detection technique is proposed in [9], with further improvements in [10, 11, 12, 13, 14, 15]. However, all of the mentioned approaches used the dynamic amplifier in the voltage domain only, while we use it as a voltage to pulse width converter.

4.2.2 Circuit characterization

This Section presents measured results of the single slope reset integrator. Figure 4.4 shows the micrograph of the single slope reset integrator. The total area of the circuit on foil is 4.4 mm^2. Table 4.1 depicts some design parameters of the circuit shown in Figure 4.2(b). Figure 4.5 shows the linear relationship between T_{out} and V_{in}. Figure 4.6 shows the residual error in T_{out} with respect to a linear fit.

Table 4.1: *Circuit parameters of the single slope reset integrator*

Parameter	Value
$\left(\frac{W}{L}\right)_{M_1,M_2}\left[\frac{\mu m}{\mu m}\right]$	$\frac{2000}{15}$
$\left(\frac{W}{L}\right)_{M_{r1},M_{r2}}\left[\frac{\mu m}{\mu m}\right]$	$\frac{100}{15}$
$\left(\frac{W}{L}\right)_{M_3}\left[\frac{\mu m}{\mu m}\right]$	$\frac{500}{15}$
V_{DD} [V]	10
C_L [pF]	10
I_{bias} [μA]	5.5

It can be observed that this error is less than $\pm 2\,\mu s$ in a $\pm 150\,mV$ input range. The time domain gain as expressed in Equation 4.10 is 0.59 ms/V, while the measured gain is 0.5 ms/V. Figure 4.7 shows the variation of gain with change in V_{ref}. It can be observed that the analytical variation in gain with change in V_{ref} closely matches with the measured variation in gain with change in V_{ref}. Figure 4.8 shows the histogram of the output jitter measured from the circuit in absence of an input signal. The total output rms jitter is 0.76 μs, which translates to 1.5 mV_{rms} input referred noise. As, it can be seen, this integrated noise is not suitable for practical applications, thus, gain stages should be added before the reset integrator.

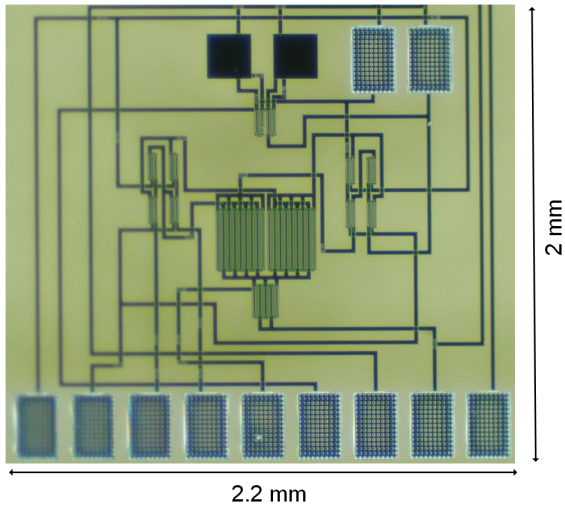

Figure 4.4: *Micrograph of the single slope reset integrator on foil.*

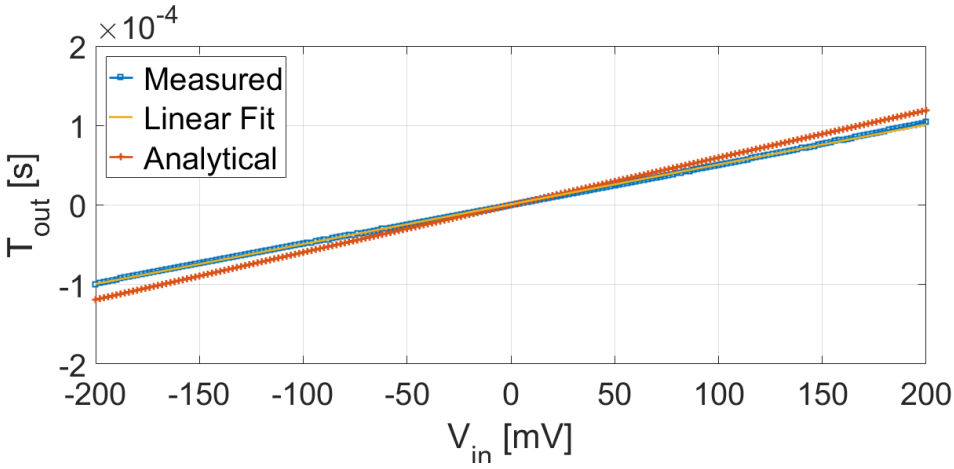

Figure 4.5: *DC transfer characteristics.*

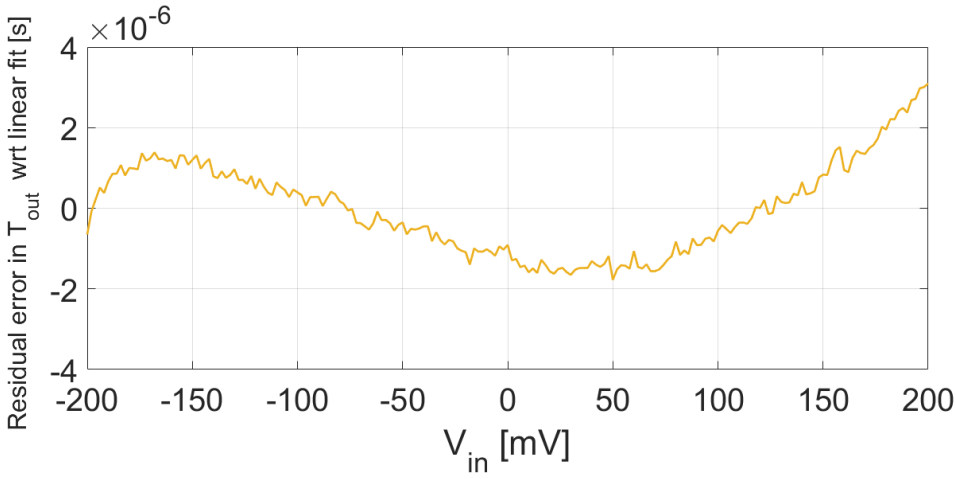

Figure 4.6: *Residual error in measured T_{out} with respect to linear fit.*

4.3 Heart-rate measurement interface

4.3.1 System architecture

The architecture of the heart-rate (HR) measurement interface which is developed based on the idea of the reset integrator is shown in Figure 4.9. The analogue front-end is integrated on foil using a-IGZO ESL TFT technology. It consists of an

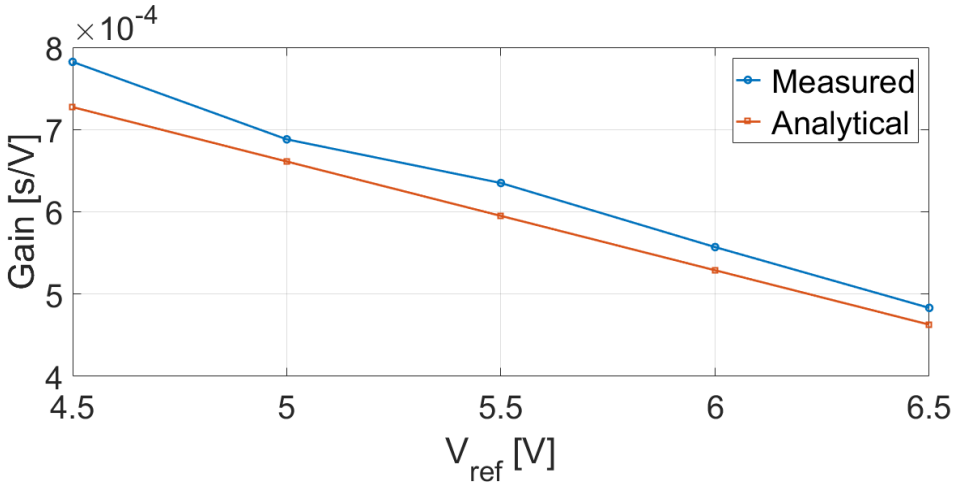

Figure 4.7: *Variation of gain with V_{ref}.*

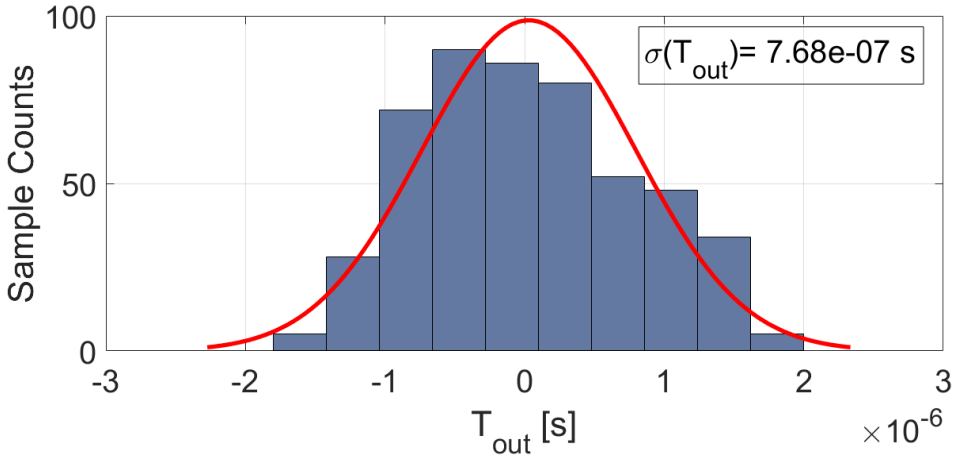

Figure 4.8: *Measured output jitter.*

input chopper, a 2-stage preamplifier featuring two cascaded diode-connected load differential gain stages and a reset integrator with de-chopper (Figure 4.9). The input signal of the conditioning chain is AC-coupled with discrete components before the input chopper ($R_{in} = 1\ M\Omega$ and $C_{in} = 4.7\ \mu F$). The output of the preamplifier is fed to the reset integrator, where the signal current discharges the load capacitors. The moments in which the integrator outputs are discharged below a given threshold V_{ref} is detected by two comparators. The time delay in threshold crossing between both branches of the integrator output, T_{out}, is proportional to the input

signal. The comparator outputs are then fed to an XOR to obtain a PWM output having a pulse width equal to T_{out} (and thus proportional to the differential input signal), with an additional sign bit, that provides information on which of the two signals crossed the reference voltage first.

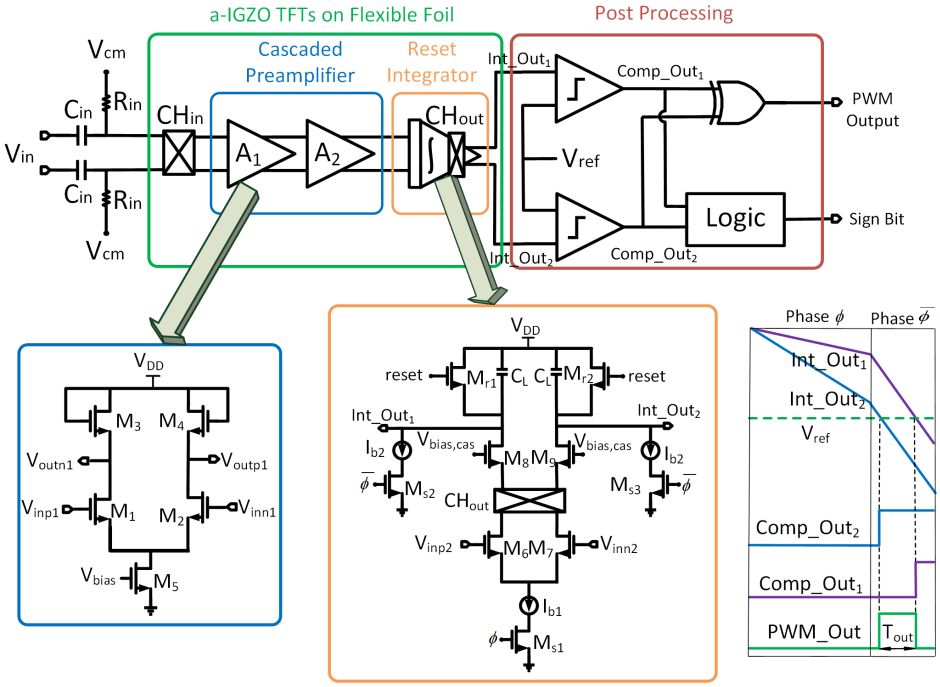

Figure 4.9: *General system architecture.*

4.3.2 Circuit design

The preamplifier is a conventional diode-connected load differential gain stage (Figure 4.9). Two stages are cascaded to obtain higher gain and lower input referred noise. The input TFTs in the preamplifier have large area (60000 μm^2) to reduce the 1/f noise. Chopping at 500 Hz is also used to mitigate the effect of 1/f noise. The reset integrator (Figure 4.9) consists of a differential input pair, output chopper and load capacitors C_L, and includes cascode transistors to enable de-chopping on low-impedance nodes. In the first phase ϕ, which will be called as the integration phase, a signal-dependent discharging of the output capacitors

occurs via the differential pair, while in the second phase $\bar{\phi}$, a constant current discharging takes place, as shown in Figure 4.9. If only an integration phase would be used for the voltage to pulse width conversion, then the comparator delay would be different for different input slopes, and this would result in non-linearity in the voltage to pulse width conversion. This effect is removed by adding the constant slope phase $\bar{\phi}$. The delay between the moments in which the two outputs reach the same voltage level (and thus the duration of the output pulse produced by the XOR, T_{out}) is proportional to the differential input voltage. This technique has an obvious penalty of reduced gain due to lesser integration time. The relationship between T_{out} and input voltage can be derived, by inspection of Figure 4.10, as follows:

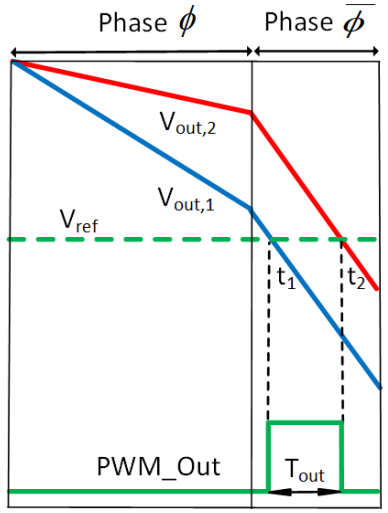

Figure 4.10: *Principle of operation.*

During the integration phase (phase ϕ):

$$v_{\text{out}_{1,\phi}} = V_{DD} - \frac{\frac{I_{b1}}{2} + \frac{g_m v_{in}}{2}}{C_L}\phi \tag{4.11}$$

$$v_{\text{out}_{2,\phi}} = V_{DD} - \frac{\frac{I_{b1}}{2} - \frac{g_m v_{in}}{2}}{C_L}\phi \tag{4.12}$$

During the constant current discharge phase (phase $\bar{\phi}$):

$$\text{At } V_{ref} : v_{\text{out}_{1,\bar{\phi}}} = v_{\text{out}_{2,\bar{\phi}}} = V_{ref} \tag{4.13}$$

$$v_{\text{out}_{1,\bar{\phi}}} = v_{\text{out}_{1,\phi}} - \frac{I_{b_2} t_1}{C_L} \tag{4.14}$$

Using value of $v_{\text{out}_{1,\phi}}$ from Equation 4.11 in Equation 4.14, we obtain:

$$V_{ref} = V_{DD} - \frac{\frac{I_{b1}}{2} + \frac{g_m v_{in}}{2}}{C_L}\phi - \frac{I_{b_2} t_1}{C_L} \tag{4.15}$$

$$\frac{I_{b_2} t_1}{C_L} = V_{DD} - V_{ref} - \frac{\frac{I_{b1}}{2} + \frac{g_m v_{in}}{2}}{C_L}\phi \tag{4.16}$$

$$t_1 = \frac{C_L}{I_{b2}}\left[V_{DD} - V_{ref} - \frac{\frac{I_{b1}}{2} + \frac{g_m v_{in}}{2}\phi}{C_L}\right] \tag{4.17}$$

Similarly, we can express t_2 as:

$$t_2 = \frac{C_L}{I_{b2}}\left[V_{DD} - V_{ref} - \frac{\frac{I_{b1}}{2} - \frac{g_m v_{in}}{2}\phi}{C_L}\right] \tag{4.18}$$

$$t_2 - t_1 = \frac{g_m v_{in}}{I_{b2}}\phi \tag{4.19}$$

$$\frac{T_{out}}{v_{in}} = \frac{g_m \phi}{I_{b2}} \quad [\text{s/V}] \quad (where,\ T_{out} = t_2 - t_1) \tag{4.20}$$

where T_{out} is the output pulse width, v_{in} is the differential input signal, g_m is the transconductance of the input transistor in the integrator, ϕ is the integration period and I_{b2} is the discharging current during the phase $\bar{\phi}$.

The first design parameter to be chosen is the reset frequency, which is similar to the sampling frequency of an ADC, and is dictated by the application. Then, from

Table 4.2: *Optimized design parameters of the system shown in Figure 4.9*

Parameter	Value
$\left(\frac{W}{L}\right)_{Input\ pair\ of\ A_1}\left[\frac{\mu m}{\mu m}\right]$	$\frac{4000}{15}$
$\left(\frac{W}{L}\right)_{Input\ pair\ of\ Integrator}\left[\frac{\mu m}{\mu m}\right]$	$\frac{2000}{15}$
V_{DD} [V]	10
C_L [pF]	100
Reset frequency [Hz]	250
Reset duration [μs]	200
Integration phase [ms]	1.8
Constant current discharge phase [ms]	1.8

Equation 4.20, we get the dependency of the other parameters. We would like to maximize the g_m/I_D ratio of the transistors in the integration phase, since the constant bias current in phase ϕ, I_{b1} does not carry information, while g_m amplifies the signal. So, it is a good choice to make W/L of these transistors large enough to bias them in subthreshold, resulting in $W \gg L$. In general, we would like to have the phase ϕ (the integration phase) to last most of the time, but we need to make sure that during the phase $\bar{\phi}$ (the constant current discharge phase), both the voltages cross the reference voltage V_{ref}. Then, the load capacitor (integrating capacitance), C_L is chosen in such a way to have the integration phase of the desired duration. In ideal conditions, the reset of the integrator should be instantaneous, as it does not bring any information, but since the switches have limited conductivity, the reset duration has to be chosen, so that the voltages settle to V_{DD}. The optimized design parameters are shown in Table 4.2.

4.3.3 Experimental results

Circuit characterization

Figure 4.11 shows the micrograph of the flexible foil integrating preamplifier and reset integrator. The total area of the circuits on foil is $10.5\ mm \times 5\ mm$. Figure 4.12

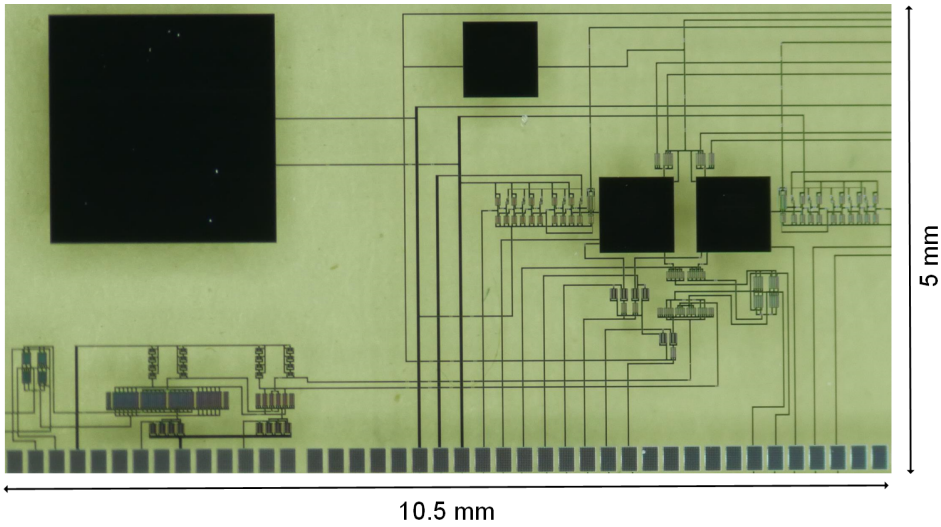

Figure 4.11: *Micrograph of the preamplifier and reset Integrator on foil.*

shows the measured frequency response of the cascaded preamplifier. It achieves a gain of 22 dB in a 3 kHz bandwidth with 3.2 μA current consumption from a 10 V supply. The integrated input referred noise of the stand alone preamplifier is 220.2 μV_{rms} without chopping and 92.5 μV_{rms} with chopping at 500 Hz in a 1-200 Hz band. Figure 4.13 shows the CMRR of the cascaded preamplifier. The CMRR is 42 dB at 100 Hz with chopping at 500 Hz. Figure 4.14 shows the input impedance of the cascaded preamplifier. The input impedance is 16.6 $M\Omega$ at 100 Hz without chopping and it reduces to 6.6 $M\Omega$ at 100 Hz with chopping at 500 Hz. Figure 4.15 shows the transfer curve of the full chain, including the reset integrator. The low frequency gain is 25 ms/V. The notches appear at integer multiples of the inverse of the integration time. The integration period is 1.8 ms and hence the first notch appears at 555 Hz. Figure 4.16 shows the measured histogram of the output jitter for the full chain, in absence of an input signal. The total output rms jitter is 4.79 μs while chopping at 500 Hz, which translates to 186.3 μV_{rms} input referred noise for the full system. The increase in the input referred noise of the full system compared to the preamplifier can be explained by considering the effect of noise folding in the baseband due to periodic reset as well as the noise of the

reset integrator itself. The current consumption in the integrator during the first phase ϕ is 1 μA while in the phase $\bar{\phi}$ it is 1.5 μA in each branch. The total power consumption is 52 μW with 10 V supply voltage.

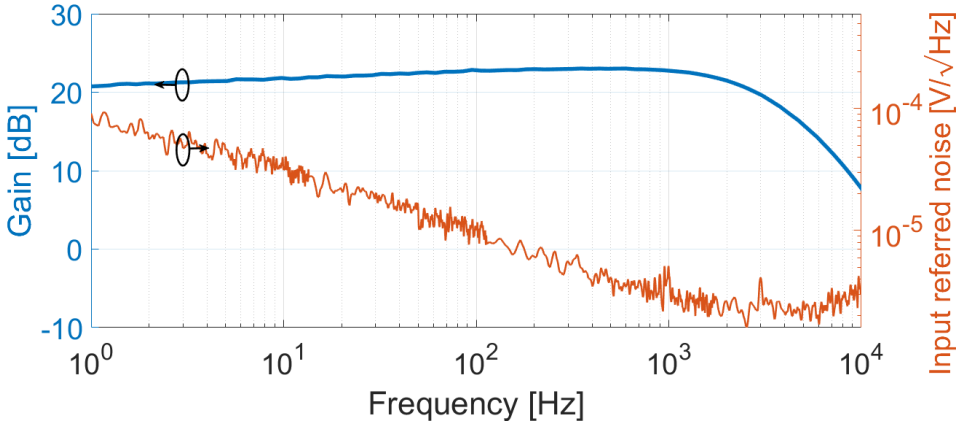

Figure 4.12: *Measured preamplifier frequency response and input-referred noise.*

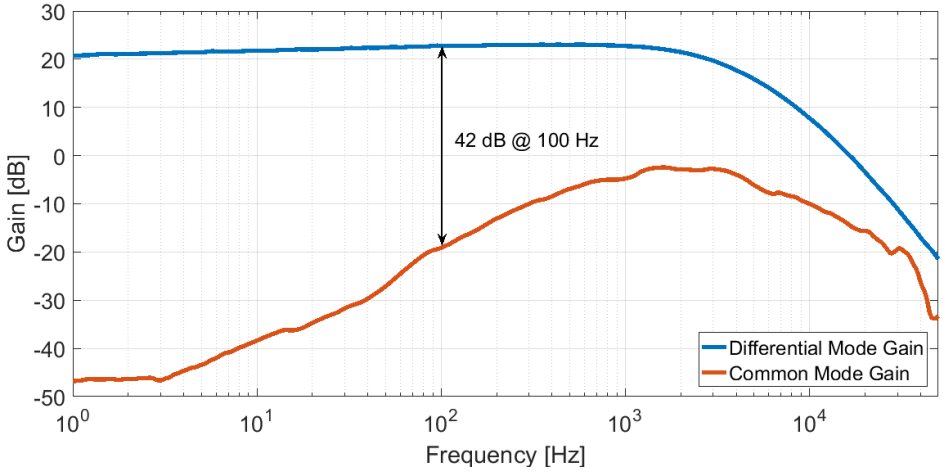

Figure 4.13: *Measured CMRR of the preamplifier.*

Signal reconstruction

The signal is reconstructed in the voltage domain from the PWM output signal. The reset frequency and its harmonics are removed from the PWM output by low-pass filtering. Figure 4.17 shows the reconstruction of a 20 mV_{pp} ECG signal applied

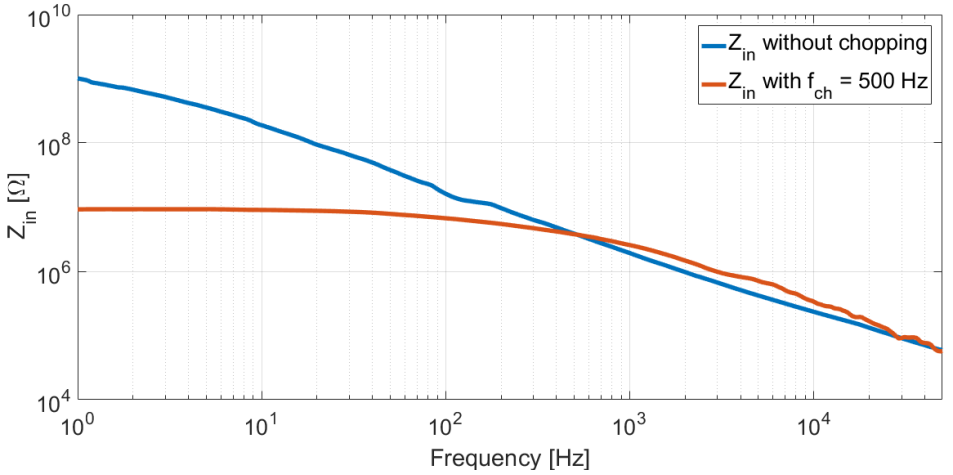

Figure 4.14: *Measured input impedance of the preamplifier.*

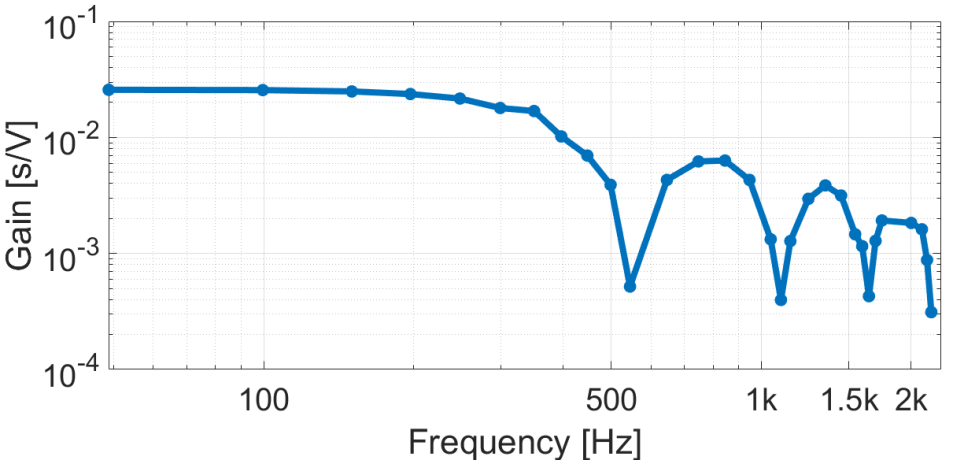

Figure 4.15: *Measured frequency response of the full chain.*

from a signal generator. A 200 Hz LPF is used to filter the reset frequency and its harmonics. As the amplitude of the input signal provided from the generator in this case is quite high, one can appreciate the QRS complex and PR and ST segments too, although corrupted by noise. However, to accurately measure ECG signals an integrated noise of 20 μV_{rms} in 100 Hz bandwidth would be needed [16]. For this reason, the present circuit is only used to measure *in-vivo* heart-rate. For heart-rate, indeed, an SNR of even 6 dB is sufficient [17]. Assuming a typical cardiac signal amplitude of 1 mV, the SNR provided by this circuit is sufficient to measure

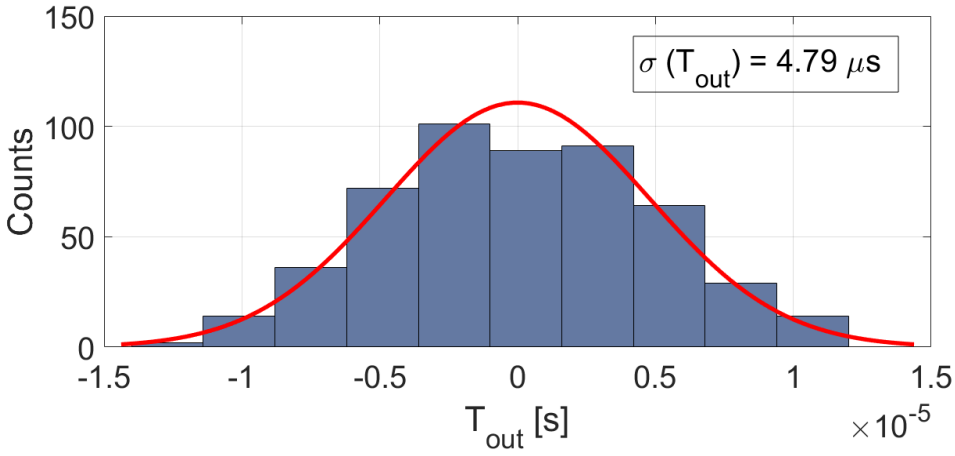

Figure 4.16: *Measured output jitter in absence of an input signal.*

HR. The signal bandwidth is further reduced to 10 Hz, to limit the in band noise and achieve sufficient SNR.

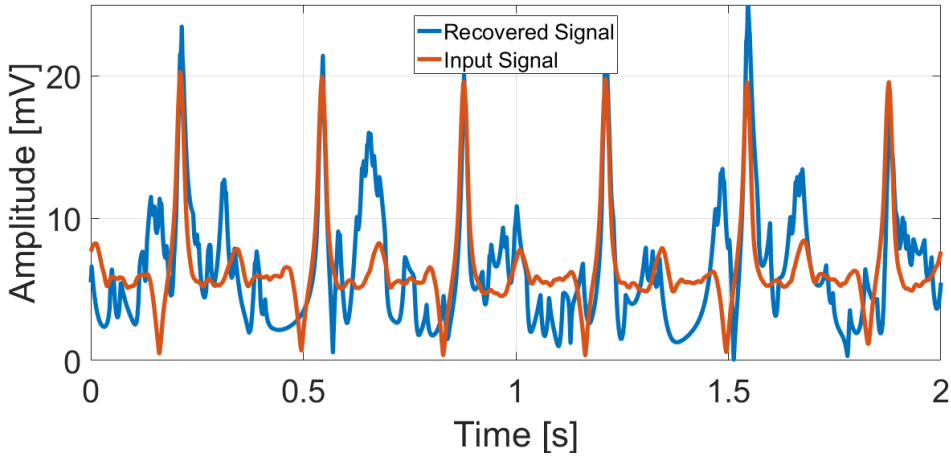

Figure 4.17: *Response of the measurement interface to an ECG signal provided by a signal generator.*

In-vivo measurement

Figure 4.18 shows an *in-vivo* experiment measuring the heartbeat of a person, obtained by connecting our system to the test subject using standard wet electrodes (Kendall's H124SG) placed on the chest. The threshold crossing of the recovered

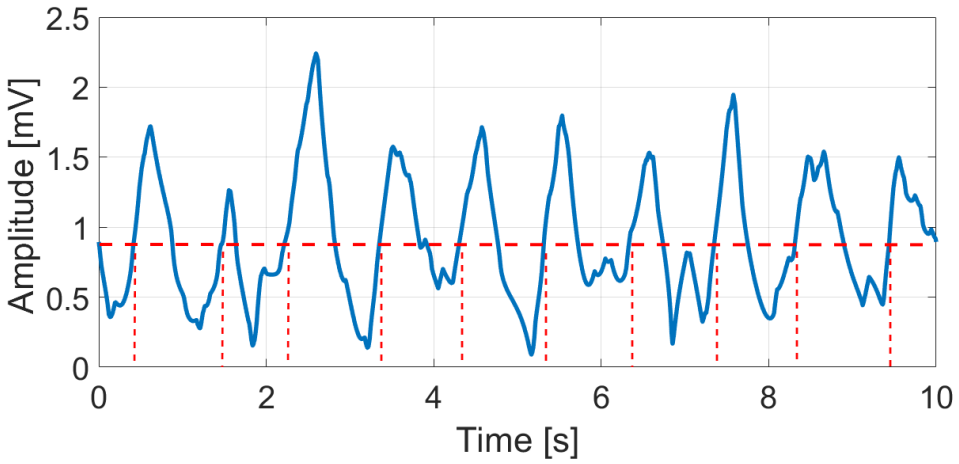

Figure 4.18: *Reconstructed signal from PWM waveform showing heartbeat from in-vivo measurement.*

signal shown in Figure 4.18 indicates the heartbeat rhythm. As discussed, a 10 Hz LPF is used to filter the reset frequency and its harmonics and to limit the in band noise. The detected heartbeat is 60 bpm which is well in the range of a normal heartbeat for a person at rest. In this case the shape of the output waveform is less recognizable, due to the strong low-pass filtering applied, but the peaks of the heart activity are clearly recognizable. An overview of the main circuit performance of our HR measurement interface and a comparison to prior-art is given in Table 4.3.

Table 4.3: *Comparison to the state-of-the-art*

	JSSC'17[4]	ISSCC'17[6]	**HR Measurement Interface**
Technology	a-Si	a-IGZO	a-IGZO
Architecture	Chopped Amplifier	ADSM	Chopped Amplifier + Reset Integrator
Input domain	Voltage	Current	Voltage
Output type	Analogue	PWM	PWM
Application	EEG	Temp. sensor	HR
Chopping frequency	5 kHz	-	500 Hz
Integrated noise [μV_{rms}] (BW)	2.3 (100 Hz)	-	186.3 (200 Hz)
Current consumption [μA]	200	100	5.2
Supply voltage [V]	55	20	10
Power dissipation [mW]	11	2	0.052
Area [mm^2]	-	27.9	52.5

4.4 Time based ECG interface

4.4.1 Improved system architecture

The integrated input noise in the system presented in Section 4.3.3 is 186.3 μV_{rms} which is too high for ECG standards, thus, enabling only HR measurements. In this Section we present an improved version of the system with better noise performance, designed and simulated using DUGA TFT models. The improved system architecture is shown in Figure 4.19. The improved performance compared to the system shown in Figure 4.9 is due to better TFT technology, circuit improvements and correlated double sampling (CDS) at system level. The front-end consists of an input chopper, a 2-stage preamplifier consisting of cascaded diode-connected load differential amplifiers (Figure 4.20(a)), a reset integrator (Figure 4.20(b)) and additionally two pseudo CMOS inverters with controllable hysteresis to implement the comparators (Figure 4.20(c)).

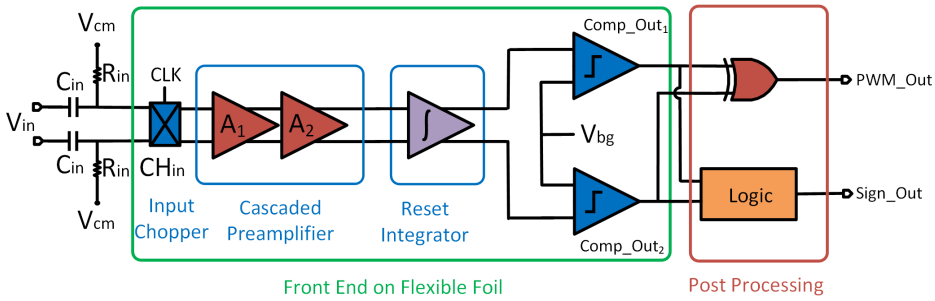

Figure 4.19: *System architecture of the improved version of the system shown in Figure 4.9.*

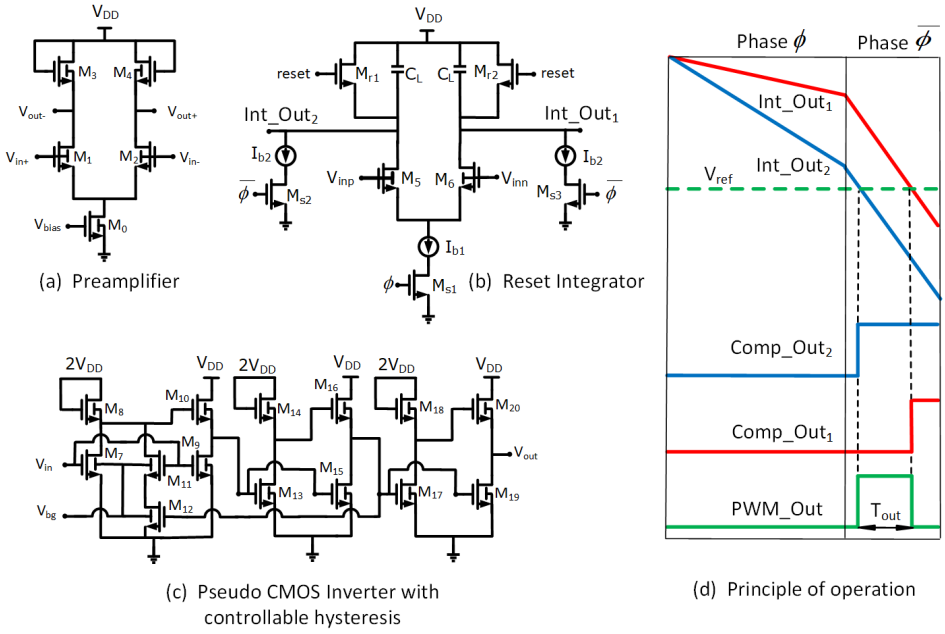

Figure 4.20: *Schematics of (a) the preamplifier, (b) the reset integrator, (c) pseudo CMOS inverter and (d) working principle of the reset integrator.*

4.4.2 Principle of operation

The preamplifier consists of a diode-connected load differential amplifier (Figure 4.20(a)). The back gates of the current-source TFT M_0 and the load TFTs $M_{3,4}$ are connected to the source to increase the output resistance (Figure 4.20(a)). Moreover, the back gates of the input TFTs $M_{1,2}$ are connected to the front gates to increase transconductance. The reset integrator (Figure 4.20(b)) consists of a differential input pair $M_{5,6}$ and load capacitors C_L. The outputs of the integra-

tor are connected to comparators which consist of three pseudo CMOS inverters connected in cascade. The output of the second inverter (Figure 4.20(c)) in the cascade is also connected to the gate of M_{12} to provide positive feedback. This introduces hysteresis in the inverter, while the switching threshold of the inverter can be controlled through the back gate biasing V_{bg} of $M_{7,11,12}$ as shown in the next Section. The hysteresis is beneficial to suppress kickback noise from the integrator outputs.

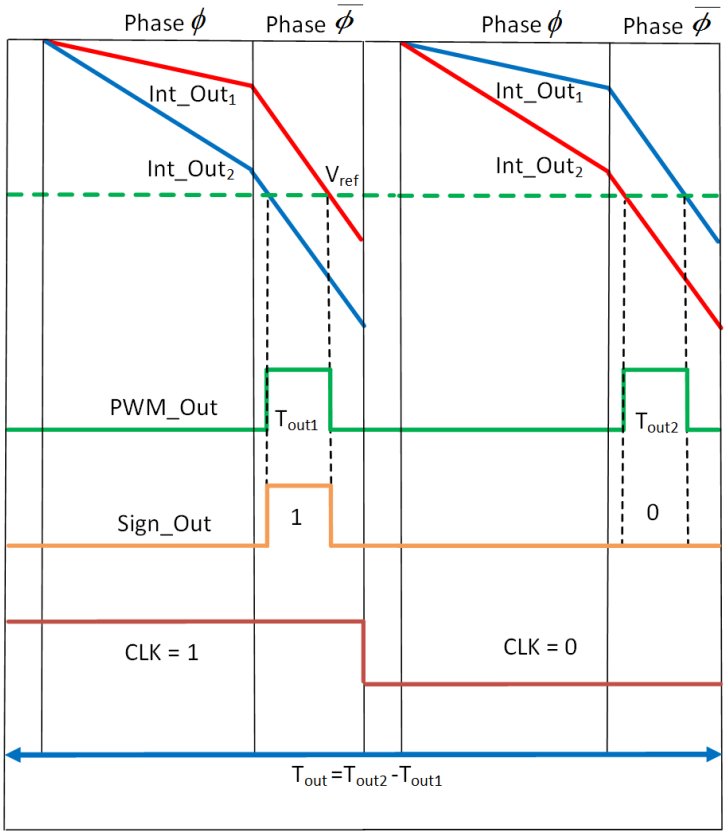

Figure 4.21: *Principle of system level CDS.*

The low-frequency noise is suppressed using CDS at system level. An input chopper (CH_{in}) is used to alternate the connection between the inputs of the preamplifier periodically with a low frequency. The output signal is extracted by subtract-

ing in the digital domain two consecutive samples, while taking into account the sign bit, as shown in Figure 4.21. When CLK is high, the inputs of the preamplifier are connected in the usual way and a PWM output of pulse width T_{out1} is obtained. In the next phase, CLK goes low, the inputs of the preamplifier are reversed, and the PWM output of pulse width T_{out2} is obtained. By subtracting T_{out2} from T_{out1} (while keeping the sign bit in consideration), a final pulse T_{out} is obtained. This approach cancels the quantities that have high correlation between two consecutive samples, i.e. offset and flicker noise, while the signal is doubled.

4.4.3 Simulation results

Circuit characterization

The system is simulated using the a-IGZO DUGA TFT model, introduced in Chapter 2. Figure 4.22 shows the simulated frequency response of the cascaded preamplifier. It achieves a gain of 35.8 dB in 1.1 kHz bandwidth with 2 μA current consumption from 10 V supply. Figure 4.23 shows the input referred noise spectrum of the system with and without system level CDS. The interface presented in this work achieves in simulation 52.5 μV_{rms} integrated input referred noise in the 1-100 Hz band without application of CDS at system level. With 250 Hz system level CDS, an input referred noise of 18.3 μV_{rms} is simulated in the 1-100 Hz band.

The current consumption in the integrator during the first phase is 250 nA while in the second phase, it is 500 nA in each branch. Fig. 6 shows the simulated DC transfer curve of the pseudo CMOS inverter. It can be seen from Figure 4.24 that the trip point of the inverter can be controlled through the back gate voltage V_{bg} applied to $M_{7,11,12}$.

Signal reconstruction

The reset frequency and its harmonics can be removed from the PWM output by low-pass filtering in a 100 Hz band, which passes only the input signal and thus

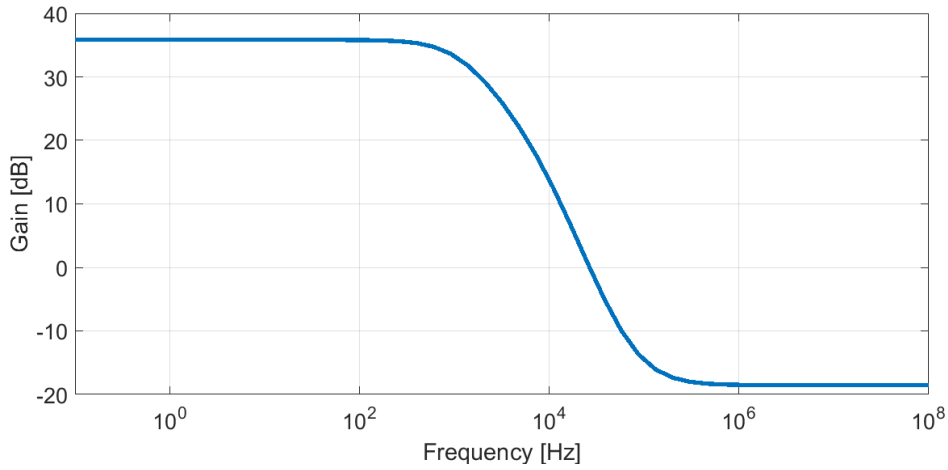

Figure 4.22: *Simulated frequency response of the preamplifier.*

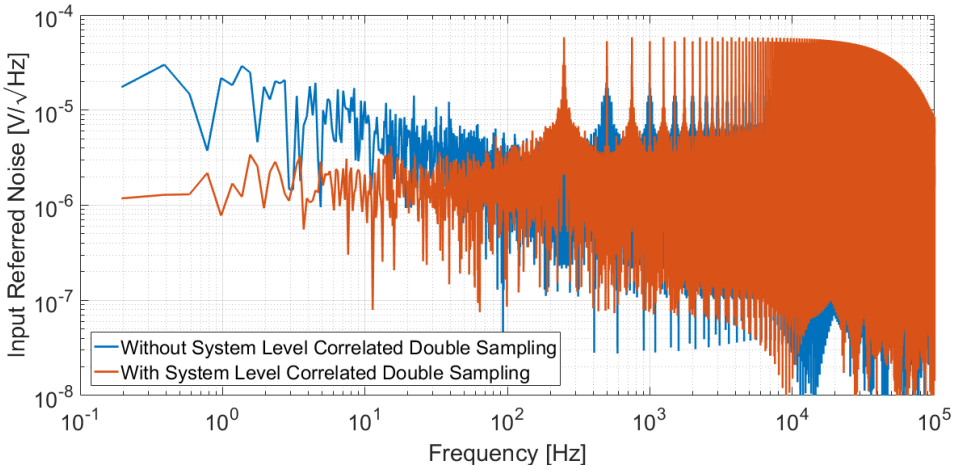

Figure 4.23: *Simulated noise spectrum of the proposed system.*

allows its reconstruction in the analogue domain. The reset frequency is 500 Hz while the CLK signal is half of the frequency of the reset signal. Figure 4.25 shows the reconstruction of a 1 mV_{pp} ECG signal obtained in simulation using this method. The simulation includes a noise model including 1/f noise as described in Chapter 2, and the ECG signal is still well recognizable.

An overview of the main circuit performance of our ECG interface and some relevant publications is given in Table 4.4. The better performance compared to the HR measurement interface described in the beginning of this Chapter [1], is

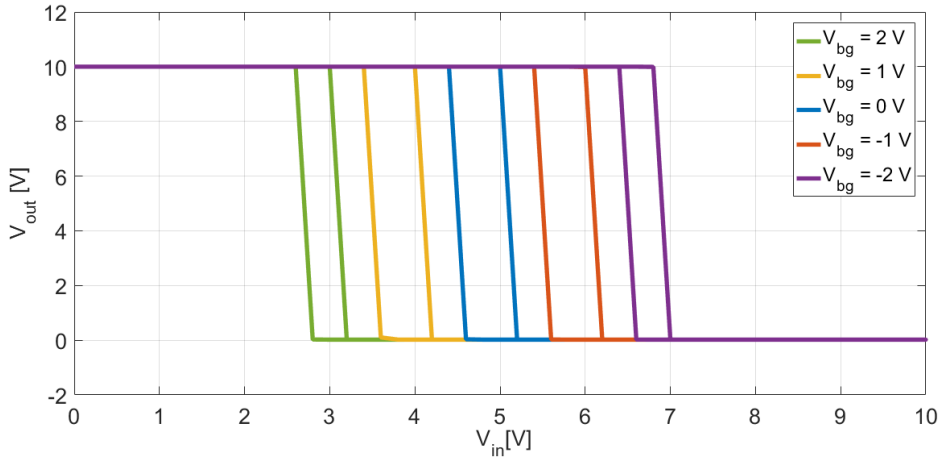

Figure 4.24: *Simulated DC transfer curve of the inverter with cascading three pseudo-CMOS inverters.*

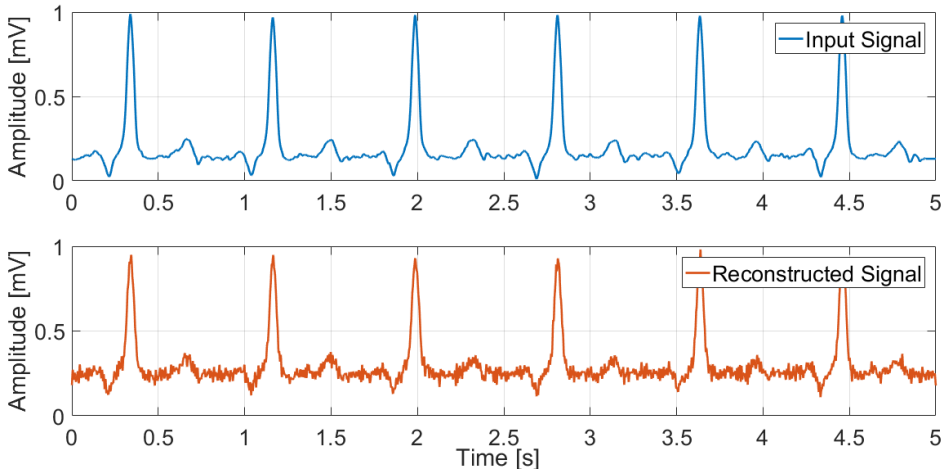

Figure 4.25: *Simulated response of the full system to an ECG source signal.*

due to both, better TFT technology and circuit improvements. From the technology perspective, the self-aligned a-IGZO technology used in this work has a Hooge factor which is significantly better than the a-IGZO technology used in [1] and thus contributes less 1/f noise. From the circuit perspective, in this work a system level CDS has been used, which reduces the total input referred noise of the whole system. The conventional chopping used in [1], on the contrary, was only applied to the preamplifier and the input of the integrator. Besides, the higher amplifier gain

and larger input transconductance, both obtained thanks to the double gate TFT architecture, benefit the noise efficiency of the interface. The simulated noise with system level chopping results in a NEF of 115.12. The total power consumption is 26.25 μW with 10 V supply voltage. This makes the simulated PEF of the presented interface 6.64$\times$ better than [4].

Table 4.4: *Comparison to prior literature*

	JSSC'17[4]	SSCL'18[18]	ESSCIRC'18[1]	ISSCC'17[6]	**Time based ECG Interface**[a]	
Technology	a-Si	a-IGZO	a-IGZO	a-IGZO	Dual Gate Self Aligned a-IGZO	
Architecture	Chopped Amplifier	Chopped Amplifier with Frequency Division Multiplexing	Chopped Amplifier + Reset Integrator	ADSM	Preamplifier + Reset Integrator + Pseudo CMOS Inverter	
Input domain	Voltage	Voltage	Voltage	Current	Voltage	
Output type	Analogue	Analogue	PWM	PWM	PWM	
Application	EEG	EMG	HR	Temp. Sensor	ECG	
Chopping frequency	5 kHz	5 kHz	500 Hz	-	-	250 Hz
Integrated noise (BW)	2.3 μV_{rms} (100 Hz)	125 μV_{rms} (500 Hz)	186.3 μV_{rms} (200 Hz)	-	52.5 μV_{rms} (100 Hz)	18.3 μV_{rms} (100 Hz)
Current consumption [μA]	200	50	5.2	100	2.6	
Supply voltage [V]	55	26	10	20	10	
Power dissipation [mW]	11	1.3	0.052	2	0.026	
NEF	126.29	1534.80	1166.4	-	330.26	115.12
PEF	8.77×10^5	6.12×10^7	1.36×10^7	-	1.09×10^6	1.32×10^5
Area [mm^2]	-	11.2	52.5	27.9	19.5	

[a] Simulated results.

4.5 Conclusions

This Chapter presents two time based interfaces for bio-signal acquisition systems for wearable applications developed with a-IGZO TFT technologies. The proposed time based interfaces perform a voltage to pulse width conversion. The proposed system architectures exploit conventional chopping and system level CDS to improve the noise performance, respectively.

The initial part of the Chapter presents an application scenario that requires a moderate SNR. A heart-rate measurement interface for wearable applications, fabricated on a flexible foil, is presented. The output is provided as a PWM representation. Voltage to pulse-width conversion is achieved with a simple and power minimalistic approach, using a reset integrator. The presented solution is compact, low cost and adds to user comfort, thanks to its mechanical flexibility. However, this approach achieves an SNR that is insufficient for most biomedical monitoring applications.

The approach presented in the first part of this Chapter is further improved for applications that require higher SNR. In the later part of this Chapter, the SNR is improved by applying CDS at system level to enable ECG monitoring using a low power flexible ECG interface. The improved performance compared to the system shown in Figure 4.9 is due to better TFT technology, circuit improvements and the CDS at system level. It can be concluded that for high SNR applications like ECG monitoring, DUGA a-IGZO TFT technology appears to be a promising solution.

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Chapter 5

A Flexible ECG Patch Compatible with NFC RF Communication

This Chapter presents a flexible ECG patch implemented on foil with self-aligned a-IGZO TFTs, which is capable to acquire ECG signals, amplify them and convert them to a sequence of bits. The presented approach provides a digitization strategy using a time reference rather than a voltage reference, and is particularly attractive for implementation with a-IGZO TFTs on foil. The analogue frontend has a measured input-referred noise of 8 μV_{rms} in the 1-100 Hz band. The system achieves experimentally 67.4 dB CMRR, 58.9 dB PSRR and 16.5 MΩ input impedance at 50 Hz, while using 1 kHz chopping. The signal from the electrodes is transformed to a 105.9 kb/s Manchester encoded serial bit stream which could be sent wirelessly to a smart phone according to the Near Field Communication (NFC) standard for further post processing.

The contents of this Chapter have been published in Nature's npj Flexible Electronics [1].

5.1 Introduction

As discussed in Chapter 1, wearable biomedical devices have witnessed a growing interest in recent years. Indeed, these devices allow long-term non-invasive monitoring of people in the comfort of their daily routine [2, 3, 4], providing information that is valuable to enable early diagnosis and effective treatment of patients, or that can be used to support a healthy lifestyle. Biomedical wearables typically aim at measuring vital signs or the bioelectric activity of different organs, such as the brain, the muscles and the heart. These signals will be named in the context of this Chapter as "bio-signals".

Cardiovascular diseases are worldwide the first cause of death, causing 31% of all fatalities every year [5]. A valuable tool to diagnose these diseases is the electrocardiogram (ECG), a non-invasive surface measurement of the heart's electrical potentials. Traditionally, to perform ECG measurements, patients are generally connected with wires to a bulky bio-potential acquisition system. This makes long-term monitoring impossible. More recently, portable and wearable ECG monitoring systems became available. These solutions are particularly valuable to diagnose various cardiovascular diseases in an early stage. For this reason, the focus of this work is on a wearable patch to measure ECG.

Continuous monitoring of physiological signals requires wearable devices to be conformable to the shape of the body, in order to improve the quality of physiological signal monitoring and to ensure maximum comfort of use. Advancements in fabrication techniques and new materials made it possible to build flexible and conformal electronics. Thus, these advancements are an important enabler to build wearables for biomedical applications [6, 7, 8].

In an effort to advance the state-of-the-art of wearable bio-signal monitoring devices exclusively based on flexible electronics, we report here for the first time

(to the best of the authors' knowledge) a flexible ECG sensor which exploits TFT-based circuits [9, 10, 11, 12, 13, 14, 15, 16] on flexible foil for the full chain of signal acquisition, amplification and digitization, and which is capable to measure ECG signals captured by a pair of electrodes with sufficient signal to noise ratio [17] (Figure 5.1). Additionally, the digital output is provided as a serial 105.9 kb/s Manchester encoded bit stream compatible with the NFC wireless transmission standard, so that the measured data could be sent to a smart phone for further elaboration and presentation. The absence of any rigid active component makes the system conformable to the human body and comfortable to use. Moreover, the implementation of the full system with flexible TFTs reduces the extra processing steps and the cost required for the integration of rigid and flexible electronic components, enabling a solution that could become compatible with single use.

The rest of the Chapter is organized as follows: Section 5.2 discusses the system architecture. In Section 5.3, circuit design of the implemented system is presented. The experimental measurement results including *in-vivo* characterization are shown in Section 5.4. Finally, Section 5.5 concludes the Chapter.

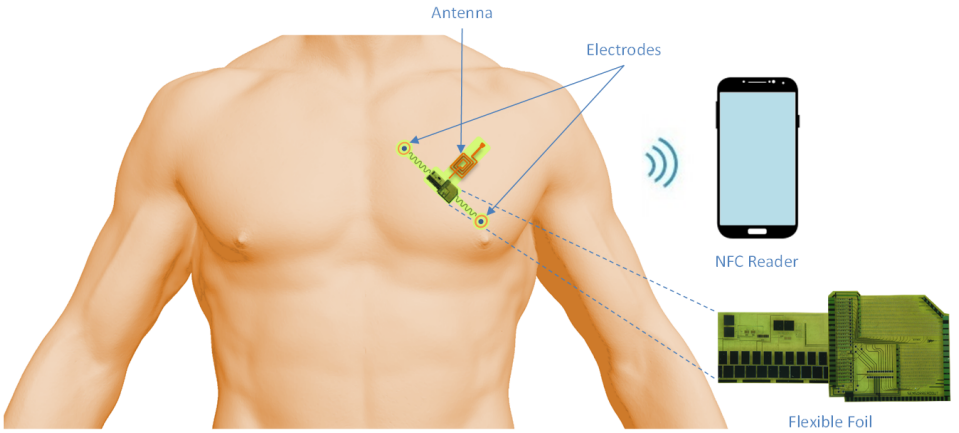

Figure 5.1: *Representative application scenario of the presented ECG patch.*

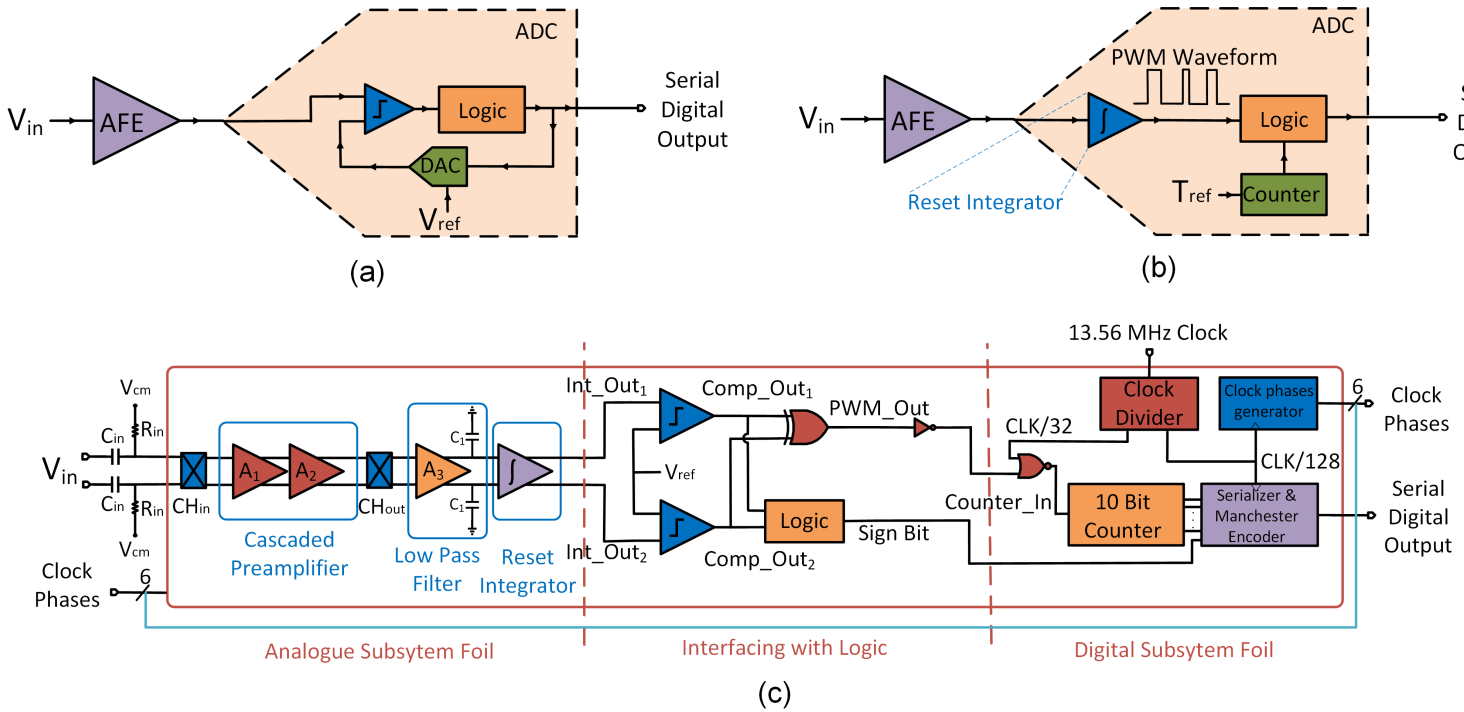

Figure 5.2: *System architecture. (a) Conventional bio-potential acquisition system, (b) System-level diagram of the presented ECG acquisition system, (c) Detailed architecture of the presented system.*

5.2 System architecture

A bio-potential acquisition system typically consists of two main blocks (Figure 5.2(a)): an analogue frontend (AFE) amplifies the signal while ensuring a suitable noise level, to preserve the shape of the signal, and provides sufficiently high impedance to enable reading the ECG signal with appropriate electrodes placed on the skin. An analogue to digital converter (ADC) follows, to convert the bio-potential signal to a digital representation, enabling robust wireless transmission and/or further signal processing. As shown in Figure 5.2(a), several ADC architectures consist typically of a comparator, a digital to analogue converter (DAC) and suitable logic. To minimize the influence of temperature and technology variability, both the AFE and the ADC are typically designed so that their signal transfer function is determined by the ratio of similar components (e.g. resistors). If variations affect all components proportionally to their value (e.g. the resistance per square increases by a given amount), these ratios tend to stay unchanged. Moreover, in typical Silicon designs, the DAC uses a reference voltage generator (Figure 5.2(a)). This reference voltage is very stable against process, supply and temperature (PVT) variations. The DAC uses this reference to produce output voltages that are also stable against PVT. At the state-of-the-art, it is difficult to make a voltage reference in a-IGZO, because the main components used for this purpose (diodes and bipolar junction transistors) are not available in a-IGZO processes.

For this reason, the design presented in this Chapter takes a radically different approach, and digitizes the input data in the time domain. The concept is shown in Figure 5.2(b). After the AFE, a reset integrator (as presented in Chapter 4) is used to transform the signal amplitude in duty cycle information (Pulse-Width Modulated, i.e. PWM representation). This means that the duty cycle of the signal produced by the reset integrator is proportional to the input signal. Digitization is then simply achieved by counting, for how many clock cycles the integrator output is high every period. In this case a time reference is needed for digitization, as

Table 5.1: *Specifications of ECG recording systems as dictated by the ANSI AAMI standard*

Electrical Parameter	ANSI AAMI EC11 Standard
Input Dynamic Range	$\pm$ 5 mV
Input Referred Noise	$< 20\ \mu V_{rms}$ (100 Hz)
Input Impedance	$> 2.5\ M\Omega$
CMRR	$>$ 60 dB

shown in Figure 5.2(b). A time reference can be easily generated in our system, which is meant to communicate to a smart phone via NFC, by using the 13.56 MHz NFC carrier as time reference, after suitable division in the digital domain [18]. The approach described here, provides a digitization strategy, without the need for a voltage reference, and thus, is particularly suited to implementation with a-IGZO TFTs on foil.

5.3 Circuit design

The electrical performance specifications of systems dedicated to ECG recording applications are regulated by the ANSI-AAMI standard [19]. Table 5.1 presents the target specifications according to this ECG standard. The input referred noise should be less than 20 μV_{rms} in a bandwidth of 100 Hz. The input impedance should be greater than 2.5 $M\Omega$. The common mode rejection should be at least 60 dB.

A more detailed schematic of the proposed flexible patch is provided in Figure 5.2(c). The system consists of two plastic foils (Figure 5.1) on which a-IGZO TFTs are fabricated. The first foil (analogue subsystem) is connected to the electrodes. The AFE captures the ECG signals, and the reset integrator transforms them to a PWM representation. The second foil (digital subsystem), connected to the first foil (analogue subsystem), digitizes the PWM signal and serializes the output bits, so that they can be sent to a receiver using radiofrequency (RF) NFC communication. The system is divided in two foils for yield optimization. Technically, at the

state-of-the-art, it is possible to have the full system on a single foil. Essentially, the middle part shown in Figure 5.2(c) (interfacing with logic) is designed on the foil, but in practice for the measurements shown in Section 5.4, it is implemented with discrete components due to some functionality issues.

The analogue frontend (AFE) consists of an input chopper (Figure 5.2(c), CH_{in}), a 2-stage cascaded diode connected load preamplifier (Figure 5.2(c)), a de-chopper (Figure 5.2(c), CH_{out}), and a low pass filter (Figure 5.2(c), LPF). The input signal is AC-coupled before the input chopper, to cancel the large DC electrode offsets. Due to the low frequency bio-signals, chopping is used to suppress the amplifier flicker noise and offset. The chopping frequency is chosen as a trade-off between noise, preamplifier bandwidth (which has an impact on power consumption) and input impedance. The preamplifiers are designed to have a bandwidth larger than the target chopping frequency, which is 1 kHz. They are built using diode-connected load TFTs, so that their gain is mainly dependent on the ratio of the transconductance of input and load devices, improving the robustness to process variations. The detailed schematic of each preamplifier is shown in Figure 5.3(a). The input TFTs $M_{1,2}$ in A_1 have a large area (15000 μm^2) to bring the 1/f noise corner close to the chopping frequency. For the diode-connected load transistors M_3 and M_4 (Figure 5.2(a)), the back gates are connected to the output nodes to increase the output resistance, while the input transistors M_1 and M_2 have back gates connected to their front gates to increase transconductance and improve noise efficiency. The second amplifier, A_2, has the same topology as A_1, with different aspect ratios of the input pair. To avoid excessive noise aliasing, the output after the chopper is low-pass filtered by another differential amplifier with diode connected load, with a 100 pF load capacitor, which has a nominal 100 Hz bandwidth.

The AFE is followed by the reset integrator (Figure 5.3(b)). The latter consists of a differential input pair $M_{5,6}$ with load capacitors C_L. The principle of operation

is similar as explained in Chapter 4: a two-phase integration is used, where in the first phase ϕ, the capacitor discharge is signal-dependent, and in the second phase $\bar{\phi}$, the capacitors are discharged by a constant current (Figure 5.3(c)). The instants at which the integrator outputs are discharged below a given threshold V_{ref} is detected by two external comparators. Thanks to the constant slope observed in phase $\bar{\phi}$, the time walk difference between the two comparators is minimized and the linearity of the voltage to duty-cycle transformation is improved. The time delay in threshold crossing between the two branches of the integrator output, T_{out}, is proportional to the input signal (Figure 5.3(c)). The comparator outputs are then fed to a XOR gate to obtain a PWM representation of the input signal with an additional sign bit. The entire analogue subsystem is extremely minimalistic in terms of transistor count, which benefits to the circuit yield and to the power consumption.

In the digital subsystem (Figure 5.2(c)), a clock divider is used to generate timing signals from a 13.56 MHz source (CLK). The PWM output is clock gated (and thus quantized in time) with a clock of frequency CLK/32 and then fed to an asynchronous counter which creates a digital multi-bit representation of the PWM output.

A 10 bit counter is required by the design constraints as shown below: The relation between output jitter and counter frequency can be given as:

$$\Delta t_{rms}^2 = \frac{1}{12 f_c^2} \tag{5.1}$$

where, Δt_{rms} is the quantization effect (in the time domain) of the counter. The above Equation 5.1 can be translated to input referred noise as:

$$v_{in,rms}^2 > \frac{1}{12 f_c^2 G^2} \tag{5.2}$$

where, $v_{in,rms}$ is the rms input referred quantization noise and G is the gain of the full chain. The targeted input referred noise is less than 20 μV_{rms} and the gain is

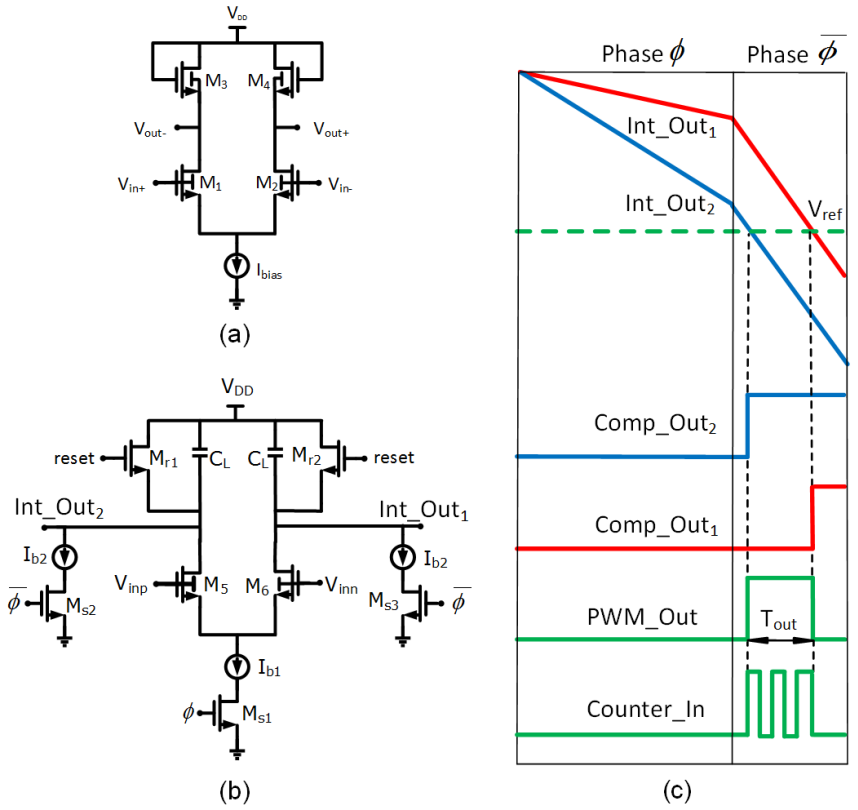

Figure 5.3: *Circuit schematics and working principle. (a) Schematic of each of the two cascaded diode-load amplifiers in the preamplifier, (b) Reset integrator, (c) Reset integrator working principle.*

35 ms/V. Substituting these values in Equation 5.2 results in $f_c > 412.4\,kHz$. The chosen f_c is:

$$f_c = \frac{13.56\ \text{MHz}}{32} = 423.75\ \text{kHz} \tag{5.3}$$

$$\mathrm{t}_c = \frac{1}{f_c} = 2.36\ \mu s = t_{\min} \tag{5.4}$$

The maximum period which has to be counted by the counter is $\bar{\phi}$ (the constant current discharge phase) i.e.:

$$\bar{\phi} = 1.8\ ms = t_{\max} \tag{5.5}$$

The number of bits (n) of the counter can be obtained as:

$$2^n = \frac{t_{\max}}{t_{\min}} \tag{5.6}$$

Equation 5.6 results in n > 9 and hence a 10 bit counter has been selected for our first prototype. The counter outputs are then serialized and Manchester encoded, generating a 32 bit serial stream including a 12 bit preamble, 10 counter bits and other fixed payload. The serializer and Manchester encoder are driven with a clock of frequency CLK/128, to provide the 105.9 kb/s output bit stream which is compatible with NFC RF transmission. The clock phases needed to drive the analogue subsystem are also generated on foil (Clock Phase Generator). The timing diagram of the clock phases is shown in Figure 5.4. It can be seen from Figure 5.4, that the reset period is 4 ms (indicated by T_4), phase ϕ (the integration phase) is 1.8 ms (indicated by $T_2 - T_1$), phase $\bar{\phi}$ (the constant current discharge phase) is 1.8 ms (indicated by T_3) and the chopping period is 1 ms. The digital subsystem is designed by the imec Leuven team leaded by Kris Myny.

5.4 Measurement results

5.4.1 Electrical characterization

To characterize the preamplifier (Figure 5.5), this circuit has been connected via a suitable mechanical connector (Yokowo DS CCNL-050-47-FRC) to off-the-shelf voltage buffers (TI OPA445AP), followed by an instrumentation amplifier (TI INA-111AP) for differential to single ended conversion. The output of the instrumentation amplifier is connected to the HP35670A Dynamic Signal Analyser to measure the frequency response and the output noise. A 10 mV_{p-p} sine wave with 5 V DC bias, and a 5 V DC reference were applied to the positive input (V_{in+}) and negative input (V_{in-}) of the preamplifier (Figure 5.3(a)), respectively. The supply voltage is 10 V. Figure 5.5 shows the measured transfer curve of the cascaded preamplifier. It

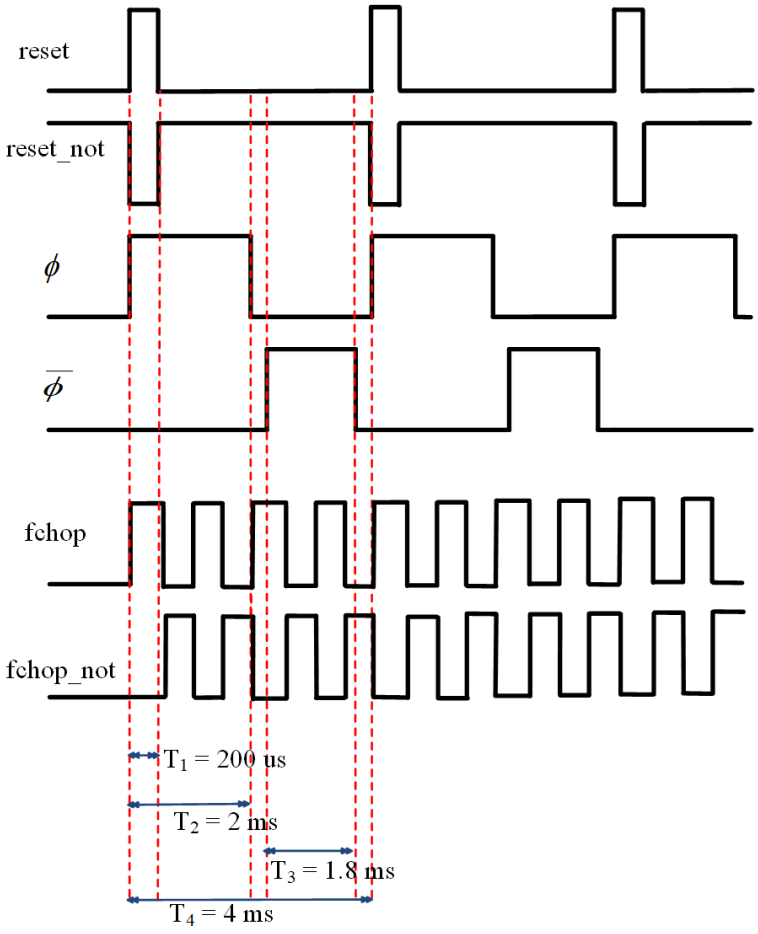

Figure 5.4: *Timing diagram of the clock phases.*

achieves a gain of 23.5 dB in a 3.7 kHz bandwidth with 12.5 μA current consumption from 10 V supply. The integrated input-referred noise in the 1-100 Hz BW is 8 μV_{rms} with a chopping frequency of 1 kHz. For the full analogue chain characterization (Figure 5.6), a 10 mV_{p-p} sine wave with varying frequency was applied to the input of the system and the output PWM was observed. The output data are acquired using a Digilent® Analog Discovery 2 board. The ratio between the fundamental harmonic of the of the filtered output PWM and the applied input signal has been calculated for each point of the frequency response recorded from the full analogue chain (from input to output PWM). Figure 5.6 shows the measured

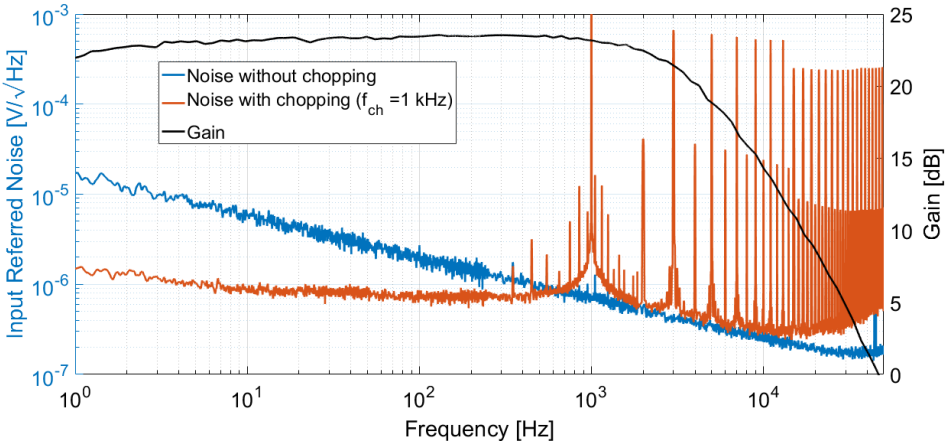

Figure 5.5: *Measured frequency response and input-referred noise of the cascaded preamplifier.*

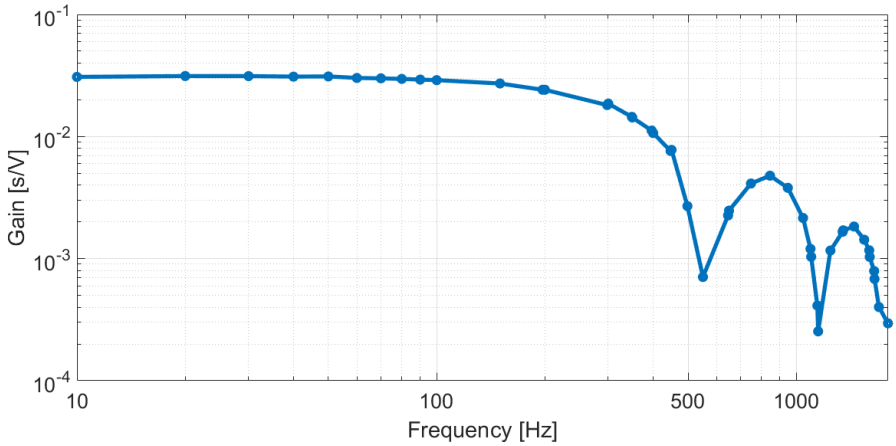

Figure 5.6: *Measured transfer function of the full analogue chain (from input to output PWM).*

transfer curve of the full analogue chain, including the reset integrator and PWM generation. The low frequency gain is 31.3 ms/V. Notice that the notches are, as expected, at multiples of the inverse of the integration period ($\frac{1}{1.8\text{ ms}} = 555.5$ Hz) and thus do not affect the target signal bandwidth. The total power consumption of the analogue subsystem is 280 μW from a 10 V supply. The digital subsystem consumes 15.4 mW from a 5 V supply. The system achieves experimentally 67.4 dB CMRR, 58.9 dB PSRR and 16.5 $M\Omega$ input impedance at 50 Hz with 1 kHz chopping.

5.4.2 *In-vivo* characterization

The *in-vivo* measurements are performed connecting our system to the test subject using wet electrodes (Kendall's H124SG) placed on the chest with a spacing of about 5 cm. A third body electrode acts as the ground electrode (which for simplicity is not shown in Figure 5.1). The output data are acquired using a Digilent® Analog Discovery 2 board for a period of 10 s. The output spectrum is filtered using MATLAB® with a Butterworth filter in the band 1-100 Hz. The ECG signal is reconstructed by dividing the output signal by the previously recorded full chain gain, to obtain the input referred ECG signal. Figure 5.7 (top panel in blue) shows an *in-vivo* experiment measuring the cardiac activity of a person. These data in the PWM output format is stored and is given as input to the digital subsystem. Figure 5.7 (bottom panel in red) shows the reconstructed signal obtained by the Manchester encoded serial digital output.

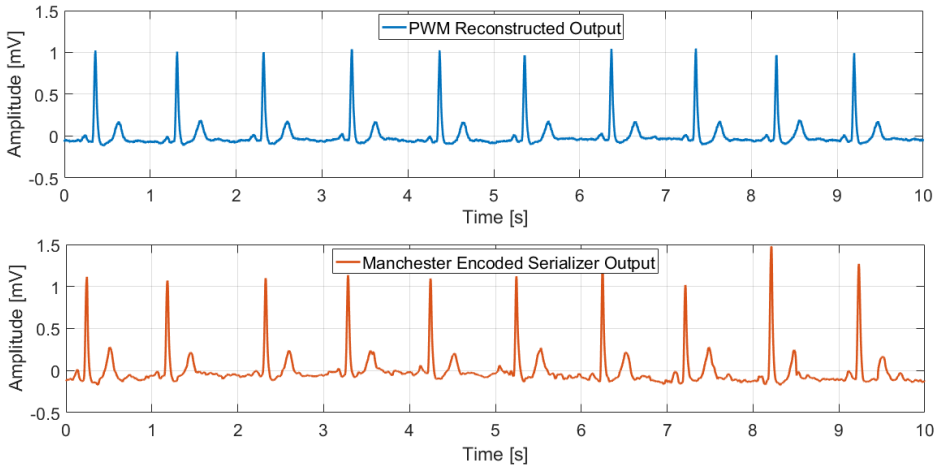

Figure 5.7: *(Top panel) In-vivo ECG measured signal reconstructed from the output PWM, (Bottom panel) In-vivo ECG measured signal reconstructed from Manchester encoded output.*

In Figure 5.8, a segment of the 105.9 kb/s Manchester encoded bit stream corresponding to the *in-vivo* measurement is displayed. The bit stream corresponding to the digitization of one sample is repeated three times in order to reduce errors in the NFC transmission. The sampling frequency of the input signal is 250 Hz,

while the Manchester encoded bit stream is generated at 105.9 kb/s, hence, there is sufficient time to repeat each sampled value three times. Figure 5.9 shows the foil micrograph of the presented system. The total area of the foil is 123.4 mm^2.

Figure 5.8: *Manchester encoded output corresponding to three samples of the in-vivo measurement and a zoom-in of the Manchester encoding of the output bits.*

Table 5.2 provides a performance summary and comparison to prior literature. This work is the first reported circuit on foil to date capable to convert a bio-potential input signal to the digital domain. Additionally, it generates a 105.9 kb/s Manchester encoded bit stream compatible with the NFC standard. Some of the initial steps taken in the direction of bio-signal acquisition systems using flexible TFT technologies have been published in literature for EEG [20], EMG [21, 22], ECG [23] and Heart-Rate (HR) [24] measurements. Comparing our contribution to existing literature on flexible TFTs circuits, in references [20, 21, 22, 23] the signal is not digitized. A recently published frontend [23] is able to acquire ECG

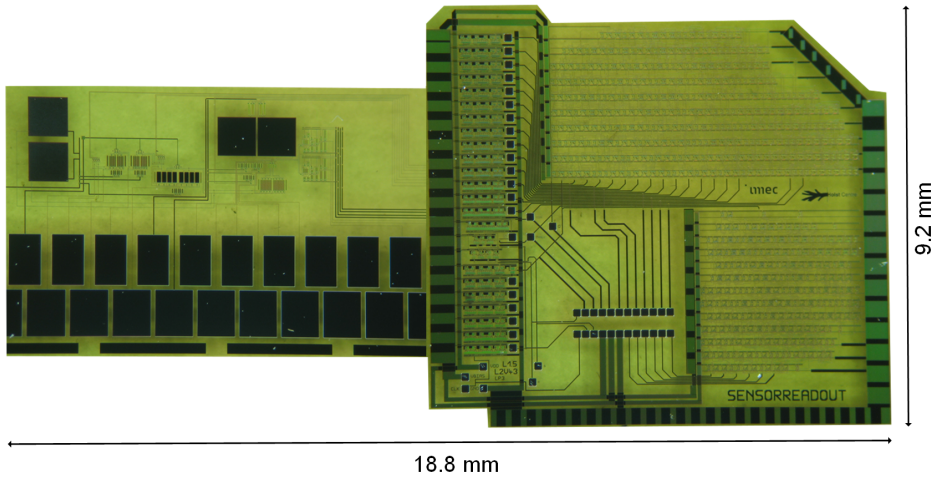

Figure 5.9: *Foil micrograph of the presented system.*

using a flexible TFT based amplifier, but it also does not digitize the signal. An HR readout on flexible foil [24] was able to convert the signal to binary levels, encoding it in the transition times (i.e. PWM output representation), but was lacking a time-sampled digital output representation (i.e. in bits), which is needed to be compatible with most modern wireless transmission systems. Compared to [24] (described in Chapter 4), we have included in this work a digital subsystem (consisting of a 10 bit counter, serializer with Manchester encoder, clock divider and digital phase generator) which transforms the PWM to a time-sampled digital format. The digital clock signals needed to operate the full system are also generated on the foil. Apart from this, the integrated input referred noise in [24] is 186.3 μV_{rms}, which is too high to perform ECG measurements, enabling only HR measurements. Within the analogue frontend we have, thus, implemented in the present work a low pass filter after the cascaded preamplifier, which limits in band noise and noise aliasing, and enables 8 μV_{rms} input equivalent noise in the 1-100 Hz bandwidth: a performance that is now compatible with ECG measurements. The input signal is transformed to PWM without digitalization in [25] too, and that circuit does not provide a voltage, but rather a current input, making it unsuited to measure bio-potential signals. The flexible ECG patch described in this

Chapter achieves experimentally NEF and PEF equal to 109.81 and 1.20x10^5 respectively. These figures provide an improvement of 13% and 86% in NEF and PEF respectively, compared to the best NEF and PEF reported for previous bio-signal acquisition front-ends implemented using flexible TFTs [20]. These advancements are obtained due to both, a better TFT technology and circuit improvements. The self-aligned a-IGZO technology used in this work has indeed a better Hooge factor, thus providing less 1/f noise. Besides, the larger input transconductance obtained, thanks to the use of the double gate TFT architecture, benefits the noise and power efficiency of the front-end.

5.5 Conclusions

This Chapter presents the first, fundamental steps to demonstrate intelligent plasters for biomedical applications based on flexible electronics which are compatible with the NFC standard. The presented approach provides a digitization strategy using a time reference, without the need for a voltage reference, and thus is particularly suited to implementation with a-IGZO TFTs on foil. The analogue frontend has a measured input-referred noise of 8 μV_{rms} in the 1-100 Hz band, which is the lowest input-referred noise reported in a-IGZO TFT circuits so far [6, 7, 8, 22, 24, 25, 26]. The system achieves experimentally 67.4 dB CMRR, 58.9 dB PSRR and 16.5 $M\Omega$ input impedance at 50 Hz with 1 kHz chopping. The output is transformed to the digital domain and provided as a 105.9 kb/s Manchester-encoded serial bit stream. To the best of authors' knowledge, this is the first demonstrated ECG acquisition system in flexible a-IGZO TFTs on foil providing a digital serial output bit stream compatible with the NFC standard [6, 7, 8, 20, 21, 22, 23, 24, 25, 26]. The power consumption is 15.4 mW for the digital and 280 μW for the analogue part. The NEF and PEF are 109.81 and 1.20x10^5 respectively, which are the best values reported in literature for a-IGZO TFT circuits to date [6, 7, 8, 20, 21, 22, 23, 24, 25, 26].

Table 5.2: *Comparison with the state-of-the-art*

	JSSC'17[20]	ISSCC'17[25]	ESSCIRC'18[24]	SSCL'18[22]	Nature Electronics'19[23]	**Flexible ECG Patch**
Technology	a-Si	a-IGZO	a-IGZO	a-IGZO	DNTT	Dual Gate Self Aligned a- IGZO
Architecture	Chopped Amplifier	Asynchronous Sigma Delta Modulator	Chopped Amplifier + Reset Integrator	Chopped Amplifier with Frequency Division Multiplexing	Amplifier with AC Coupled Load	Chopped Amplifier + Low Pass Filter + Reset Integrator + 10 Bit Counter + Serializer + Manchester Encoder + Clock Divider + Digital Phase Generator
Minimum Channel Length [μm]	6	15	15	15	10	1.5
Input Domain	Voltage	Current	Voltage	Voltage	Voltage	Voltage
Output Type	Analogue	PWM	PWM	Analogue	Analogue	Digital
Application	EEG	Temp. Sensor	HR	EMG	ECG	ECG
Chopping Frequency [kHz]	5	-	0.5	5	-	1
Integrated Noise [μV_{rms}](BW)	2.3 (100 Hz)	-	186.3 (200 Hz)	125 (500 Hz)	-	8 (100 Hz)
CMRR [dB]	<50 @ 50 Hz	-	-	-	44 @ 50 Hz	67.4 @ 50 Hz
PSRR [dB]	-	-	-	-	-	58.9 @ 50 Hz
Input Impedance [$M\Omega$]	-	-	-	29	-	16.5 @ 50 Hz
NEF (Frontend)	126.29	-	454.29	1534.80	-	109.81
PEF (Frontend)	8.77×10^5	-	2.06×10^6	6.12×10^7	-	1.20×10^5
Supply Voltage [V]	55	20	10	26	4	10^a 5^d
Power Dissipation [mW]	11	2	0.052	1.3	-	0.28^a 15.4^d
Area [mm^2]	-	27.9	52.5	11.2	-	24^a 99.3^d

[a] Analogue [d] Digital

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Chapter 6

A Multichannel EOG Acquisition System based on Flexible TFTs and CMOS Technologies

This Chapter demonstrates a fully integrated 8 channel Electro-oculography (EOG) acquisition system that exploits a front-end in a-IGZO technology, interfaced with a custom Si IC that supports the frontend and provides conversion of the acquired signals to the digital domain. In this way the low cost, flexible form factor and the large area character of the flexible TFT technology are leveraged, while exploiting the accuracy, computational capability and energy efficiency of the Si IC. More specifically, the Si IC controls a high pass filter, which is implemented with TFTs, providing a very low high-pass frequency. Also, the Si IC enables conversion to the digital domain with much higher efficiency compared to the TFT solution previously discussed in Chapter 5. Thus, from the circuit perspective, we have enabled an integrated high pass filter, while from the system perspective, we explore the combination of TFT and Si technologies to decrease power consumption.

6.1 Introduction

Wearable devices using flexible technologies for health monitoring have become a topic of growing research interest, with applications including Electroencephalography (EEG) [1], Electromyography (EMG) [2, 3, 4] and Electrocardiography (ECG) [5]. This Chapter presents a multichannel Electro-oculography (EOG) acquisition system based on a-IGZO TFTs and Si IC Technology.

The flexible form factor of TFTs can be used to improve interfacing with the human body, resulting in better signal-to-noise ratio and improved user comfort. However, the inherently poor device performance of flexible TFT technologies results in limited electronic functionality. On the other hand, Si ICs can provide superior computational functionality at a comparatively lower power than flexible electronic devices. Hence, conventional Si ICs are well suited for the signal processing and data transmission. Thus, to optimize the performance of bio-signal acquisition systems, the flexibility, conformability and large area character of the flexible devices should be combined with the better signal processing capability and higher efficiency of conventional Si ICs to realize flexible hybrid electronics (FHE) systems.

FHE systems are especially well suited for applications where large area coverage or high channel count for signal acquisition is required, such as in EEG and EMG acquisition systems. If these applications are implemented using only Si ICs, the bond pad area for input connections to the electrodes can dominate the total chip area. Thus, implementation of a large number of channels leads to higher costs. Using TFTs for the front-end allows concentration of the signals from many channels on a small number of interconnects and thus enables smaller Si ICs. The added cost of TFT electronics is typically negligible, given the very low price per unit area that these technologies offer. Therefore, a hybrid solution combining flexible and rigid electronics is attractive in terms of patient comfort, performance and cost, where flexible devices are used for soft interfaces and hard electronics are used for computation, signal processing, and data transmission as shown in

a representative scenario depicted in Figure 6.1. One point to be taken into consideration while dealing with FHE systems is that they might not offer the lowest cost solution compared to flexible only systems, but they provide a very interesting tradeoff between performance and cost.

This Chapter presents a fully integrated 8 channel FHE EOG acquisition system based on double gate self aligned a-IGZO technology, interfaced with a custom Si IC used for backend operations.

EOG is a well known approach of non-invasively monitoring eye movement activity [6]. The EOG measurements are based on electrical signals that are generated due to cornea-retina dipole when the eye moves. These bio-signals can be acquired by attaching pairs of electrodes across the eyes. The primary applications of EOG are related to ophthalmological diagnosis and eye movement recording. The EOG acquisition systems can be further used for various applications e.g. cognitive and perception studies in neuroscience [7], mental health monitoring [8], quantitative evaluation of neurodegenerative diseases [9], sleep studies [10], human-computer interaction (HCI) [11] etc.

The rest of the Chapter is organized as follows: Section 6.2 discusses the system architecture and circuit design of the implemented system. The experimental measurement results are shown in Section 6.3. Finally, Section 6.4 concludes the Chapter.

6.2 System architecture

The specifications of systems dedicated to EOG recording applications are regulated by the ISCEV standard [12]. In human beings, the EOG signal ranges from 0.05 mV to 3.5 mV, with a typical bandwidth of DC to 50 Hz [6]. However, the main signal bandwidth of eye movement is located in the range of 0.1 Hz to 30 Hz. In practice, the high cut off frequency should be preferably above 70 Hz to acquire all the signal details [13]. For a 30^{o} eye movement, the typical EOG ampli-

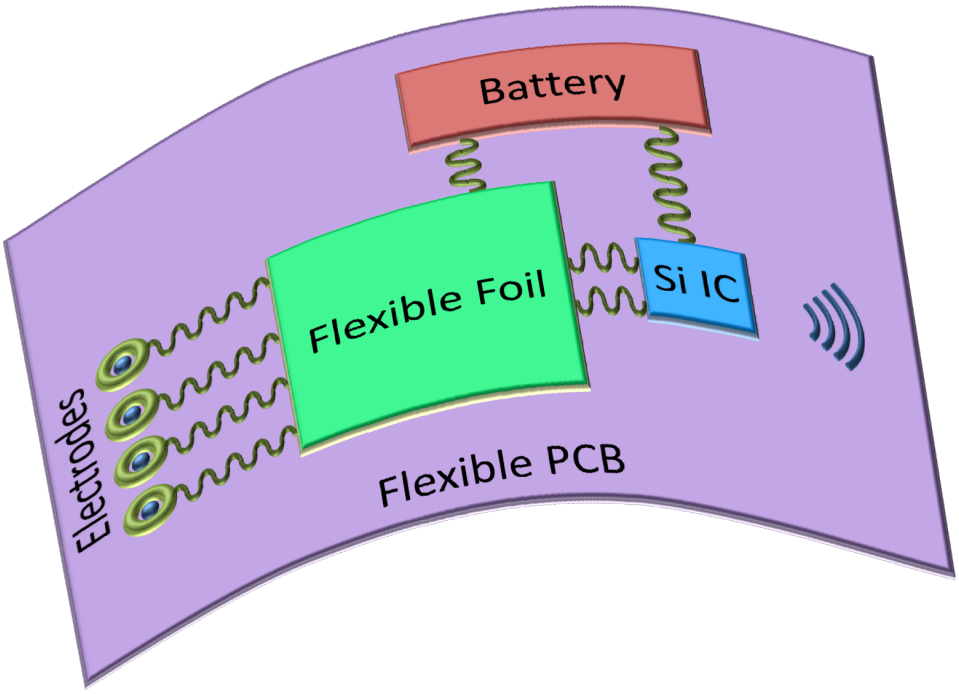

Figure 6.1: *Representative integration of the flexible hybrid system.*

tude is between 250 μV and 1000 μV, with an essential frequency content in the band 0.1–30 Hz. The electrode–skin contact impedances should be below 5 $k\Omega$ as measured between 20 and 40 Hz [12].

The full system architecture is shown in Figure 6.2. It consists of 8 channels for signal acquisition. Each channel of the analogue frontend (AFE) consists of an input chopper (CH_{in}), a 2-stage cascaded diode connected load preamplifier ($A_{1,2}$), a de-chopper (CH_{out}), and a low pass filter, A_3, loaded by C_i. The channels are AC coupled through a tunable hybrid high pass filter (HPF). All the channels are time-multiplexed through a multiplexer (MUX) to a reset integrator. The outputs of the reset integrator are fed to the gates of TFTs which act as transconductors. The output currents of these TFTs along with a reference current, are interfaced to the Si backend. The clock phases required for the analogue subsystem functional-

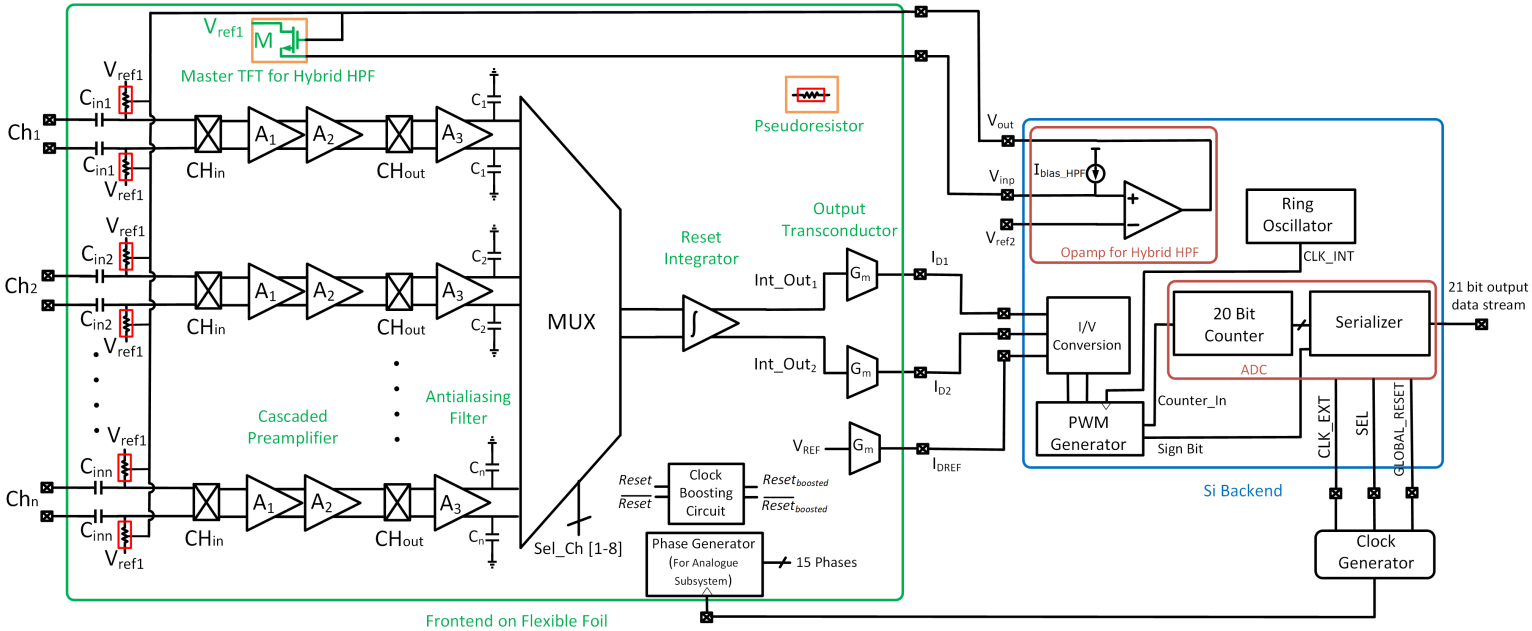

Figure 6.2: *System architecture of the flexible hybrid system.*

ity are generated on the foil by a Phase Generator, while a Clock Boosting circuit provides voltage boosted reset signals ($0- \sim 2V_{DD}$) for the integrator reset. The Si backend input consists of an I/V conversion block to interface the TFT and Si subsystems. There is basically only one differential signal and a reference interconnect (I_{D1}, I_{D2} and I_{DREF}) required between TFT and Si subsystems, which reduces the area needed for interconnections on the Si chip, and thus cost. After conversion to the voltage domain in the Si IC, the output is fed to a PWM Generator where a PWM representation of each channel (PWM_Out) is generated with an additional Sign Bit. The result of an AND between the internal clock (CLK_INT) and PWM_Out, called Counter_In, is used as input for a 20 bit Counter. The output bits of the Counter along with the Sign Bit are serialized to generate a 21 bit digital serial output bit stream. More details on the main sub-blocks are provided in the following Sections.

6.2.1 Hybrid high pass filter

In biomedical applications, HPF at the input of the signal processing chain are typically used to reject the electrode offset and provide a suitable signal filtering. Due to the very large times constants required, these filters are often implemented with capacitors and pseudoresistors. This is even more the case in TFT technologies, where no highly resistive layer is typically available, and capacitors have a low capacitance per unit area. The problem of pseudoresistors, however, is their high sensitivity to process variations, and the lack of a simple way to tune their value. To solve these problems, we propose here a novel approach that exploits the presence of Si components in the system.

The proposed hybrid HPF consists of TFT based pseudoresistors and integrated on-foil capacitors with a feedback loop, using a CMOS based op-amp in the Si IC, to tune the gate voltages of the pseudoresistors as shown in Figure 6.3. An on-chip bias current I_{bias_HPF}, generated using the current reference described in Section

6.2.3, flows through the master TFT consisting of M TFTs T_{m_1-M} in parallel. The output of the op-amp tunes the gate voltages of the master TFTs, which in turn are used to tune the gate voltages of the pseudoresistors used in the signal chain, consisting of N TFTs T_{chi_p/n_s_1-N} in series. The op-amp is implemented with a standard folded cascode topology. The equivalent resistance of the pseudoresistor is given by:

$$R_{eq} = \frac{(V_{\text{ref2}} - V_{\text{ref1}})}{I_{\text{bias\_HPF}}} \cdot M \cdot N \tag{6.1}$$

where $V_{\text{ref2}} - V_{\text{ref1}}$ is the voltage difference across the master TFT, I_{bias_HPF} is the on-chip bias current, M is the number of parallel TFTs in the master TFT, while N is the number of TFTs in series in the pseudoresistor. For illustration, if $V_{\text{ref2}} - V_{\text{ref1}}$ is chosen to be 100 mV, I_{bias_HPF} is 1 nA, M is 10 and N is 10, R_{eq} of 10 $G\Omega$ is achieved.

The obvious advantage of the hybrid HPF with tunable pseudoresistor is its robustness to parameter variations. A CMOS based op-amp is more robust compared to its TFT counterparts under variations due to process, supply voltage and temperature (PVT). The feedback loop will tune the gate voltages of the TFT based pseudoresistors across a wide range of parameter variations to match the desired value. Obviously, a residual cause of variability will be the mismatch between the unity elements of the pseudoresistors. In order to counteract this final variability source, the backgate voltages of the master TFTs (V_{BG0}) and pseudoresistors ($V_{BG\_chi\_p/n}$) are individually tunable.

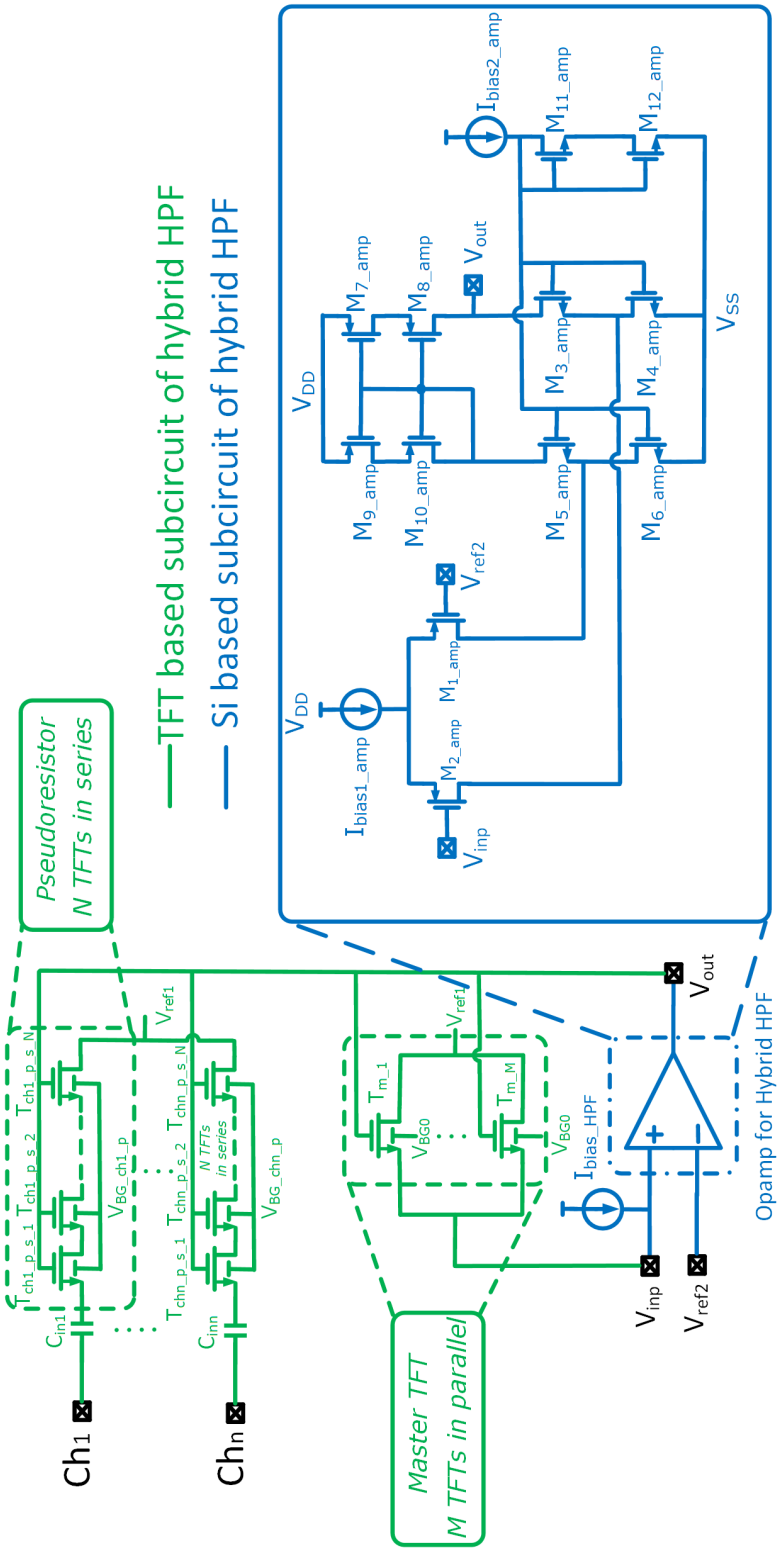

Figure 6.3: *Architecture of the flexible hybrid HPF.*

6.2.2 Frontend on flexible foil

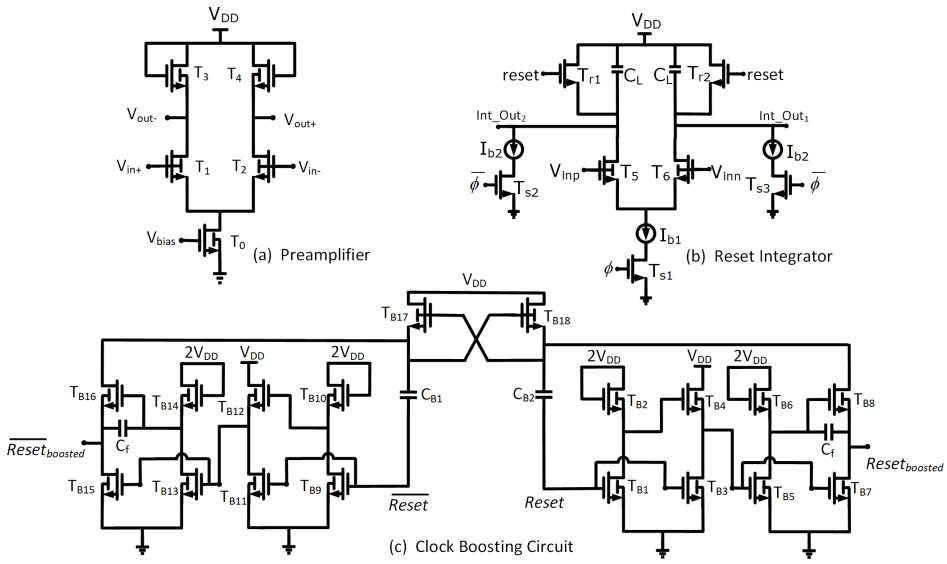

Figure 6.4: *Circuit schematic of analogue frontend (a) Schematic of the diode-connected load amplifier, (b) Reset integrator, (c) Clock boosting circuit.*

The preamplifier is a 2-stage cascaded diode-connected load preamplifier, built using diode-connected load TFTs, as shown in Figure 6.4(a). The input TFTs $T_{1,2}$ in A_1 have a large area to reduce 1/f noise. The second amplifier A_2 has the same topology as A_1 with different aspect ratios of the input pair. The output after the de-chopper is low-pass filtered by another differential amplifier, A_3, with diode connected load, which includes load capacitors to limit the bandwidth and noise folding in the reset integrator. All the 8 channels in the AFE are time multiplexed using a MUX, followed by the reset integrator (Figure 6.4(b)). The principle of operation of the reset integrator is the same as explained in Chapter 4. The integrator outputs are fed to gates of TFTs, functioning as transconductors (G_m) (Figure 6.2). The output currents ($I_{D1,2}$) from the integrator outputs along with a reference current (I_{DREF}) are interfaced to the Si backend. Circuits consisting of TFTs generally require a high supply voltage due to thicker dielectrics used in flexible TFTs, while Silicon based circuits are operated at lower supply voltages. This inherent difference in supply voltage domains makes interfacing (especially in voltage domain)

of flexible circuits with Silicon based circuits in hybrid systems quite challenging. Hence, the interfacing between TFT and Si IC in this system has been implemented in the current domain.

The reset switches ($T_{r1,2}$) in the reset integrator (Figure 6.4(b)) need to pull $Int\_Out_{1,2}$ nodes to V_{DD}. As these are NMOS TFTs, they need to be switched on by clocks higher than V_{DD}. For this reason, these clocks are generated by the Phase Generator and then fed to the Clock Boosting circuit to get output voltage boosted clocks. The schematic of the Clock Boosting circuit is shown in Figure 6.4(c). This circuit uses two clock phases *Reset* and $\overline{Reset}$ and operates as follows: during the on time of $\overline{Reset}$, TFT T_{B18} turns on and capacitor C_{B2} charges to V_{DD}. During *Reset*, TFT T_{B17} turns on and capacitor C_{B1} charges to V_{DD}. Capacitor C_{B2}, which was charged to V_{DD} during the previous clock phase, is now connected between V_{DD} and the drain of TFT T_{B8}, lifting the voltage at drain of TFT T_{B8} to $2V_{DD}$. Thus, the output pulse ($Reset_{boosted}$) at the source of TFT T_{B8} is between $V_{SS}- \sim 2V_{DD}$.

The clock phases required for the functionality of the analogue frontend are also generated on-foil using the Phase Generator. The timing diagram for the frontend functionality is shown in Figure 6.5. It can be seen from Figure 6.5, that the reset period is 500 μs (indicated by T_4), phase ϕ (the integration phase) is 245 μs (indicated by $T_2 - T_1$) and phase $\bar{\phi}$ (the constant current discharge phase) is 245 μs (indicated by T_3). Each channel is active for 495 μs and after one complete cycle (when all channels have been multiplexed), the Ch1_flag signal is activated to indicate the start of a new acquisition cycle. The Phase Generator block is designed by the imec Leuven team leaded by Kris Myny.

6.2.3 Silicon backend

Current reference

The current reference is a standard beta multiplier reference circuit, as shown in Figure 6.6. It consists of a current mirror composed of $M_{1,2}$ and $M_{3,4}$. The start up circuit consists of M_{5-7} with $M_{pc,nc}$ acting as MOS capacitors to V_{DD} and V_{SS}

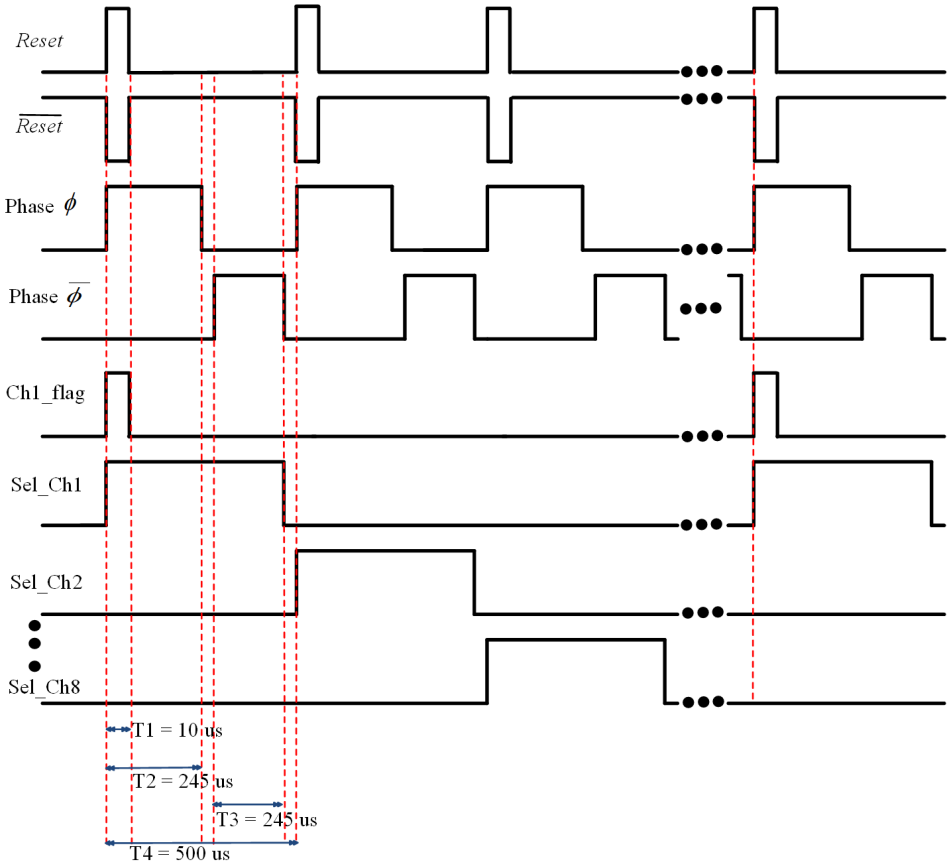

Figure 6.5: *Timing diagram of the frontend on flexible foil.*

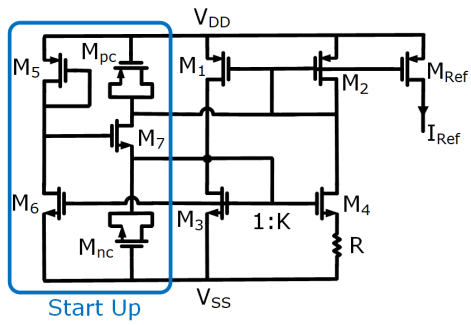

Figure 6.6: *Circuit schematic of the current reference.*

respectively. The reference current I_{Ref} can be written as:

$$I_{\text{Ref}} = \frac{V_t \ln K}{R} \tag{6.2}$$

where V_t is kT/q, R = 1.06 $M\Omega$, K = 50, which results in a nominal $I_{Ref} = 100\,nA$.

I/V conversion for TFT-Si interface

Figure 6.7a shows the circuit diagram of the current to voltage conversion block used at the TFT-Si interface. The PMOS based current mirrors $M_{ls\_1,2}$ and $M_{ls\_3,4}$ copy the TFT output currents $I_{D1,2}$ (which are periodically reset ramp signals) and I_{DREF} inside the Si IC. The NMOS based current mirror formed by $M_{ls\_5,6}$, then performs a current comparison between $I_{D1,2}$ and I_{DREF}, and a conversion to the voltage domain at its output. An over-voltage protection is provided at the TFT-Si interface terminals in the Si IC, to avoid potential over-voltages generated on the TFT side. This signal is then fed to 3 cascaded current-starved inverters, followed by inverters with gradually increased sizes. The input and output of the last stage inverter are finally fed to a latch to get the rail to rail outputs V_{OUT1} and V_{OUT2}. The delay time of the starved inverters is controlled by the bias current (I_{bias_LS}). This op-amp-less current to voltage conversion architecture is chosen for its power efficiency. Indeed, its simulated power consumption, for operation with TFT outputs at the nominal frequencies, is 69.3 μW.

Ring oscillator

Figure 6.7b shows the simplified circuit diagram of the ring oscillator. It comprises of an odd number of current-starved inverter stages followed by inverters with gradually increased sizes to drive the connected the feedback loop. The propagation delay time of a single inverter stage is controlled by the bias current (I_{bias_RO}). The ring oscillator is designed to provide a nominal clock frequency (CLK_INT) of 10 MHz.

PWM generator

The block diagram of the PWM Generator and 20 bit Counter and Serializer is shown in Figure 6.8. The PWM Generator consists of two D flip flops clocked by

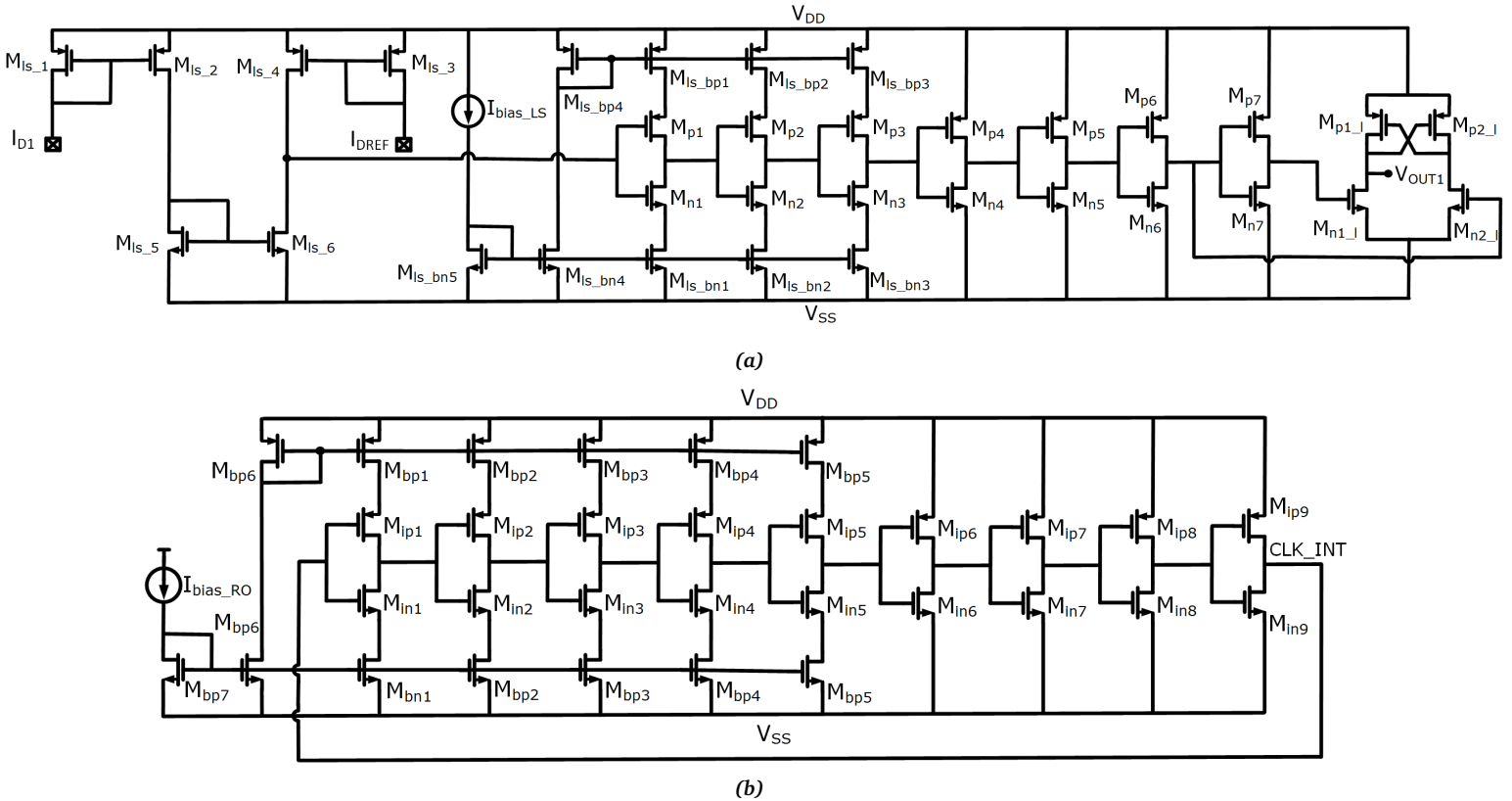

Figure 6.7: *(a) Circuit schematic of the I/V conversion (single ended version shown for illustration), (b) Circuit schematic of the ring oscillator.*

V_{OUT1} and V_{OUT2}. The outputs of both the flip flops are ORed to get PWM_Out (as shown in Figure 6.9) which is ANDed with CLK_INT to finally get Counter_In. GLOBAL_RESET is used to periodically reset both the flip flops.

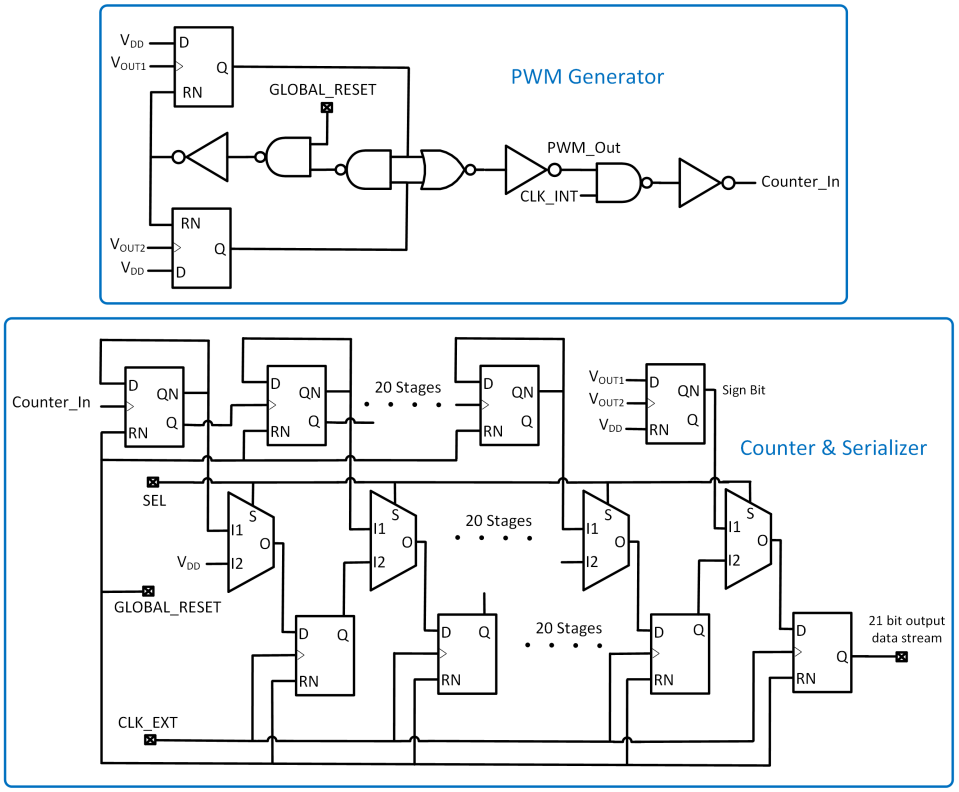

Figure 6.8: *Circuit schematics of the PWM generator, counter and serializer.*

Counter and serializer

The output of the PWM Generator, Counter_In is used as input to a 20 bit asynchronous ripple counter based on D flip flops. The SEL signal passes the counter output bits and additional Sign Bit to the Serializer to obtain a 21 bit output data stream. The Counter and Serializer are also periodically reset by the GLOBAL_RESET.

The main timing waveforms of the Si backend are shown in Figure 6.10. After a channel is selected by Sel_Ch*i* signal, a PWM waveform (PWM_Out) is generated as

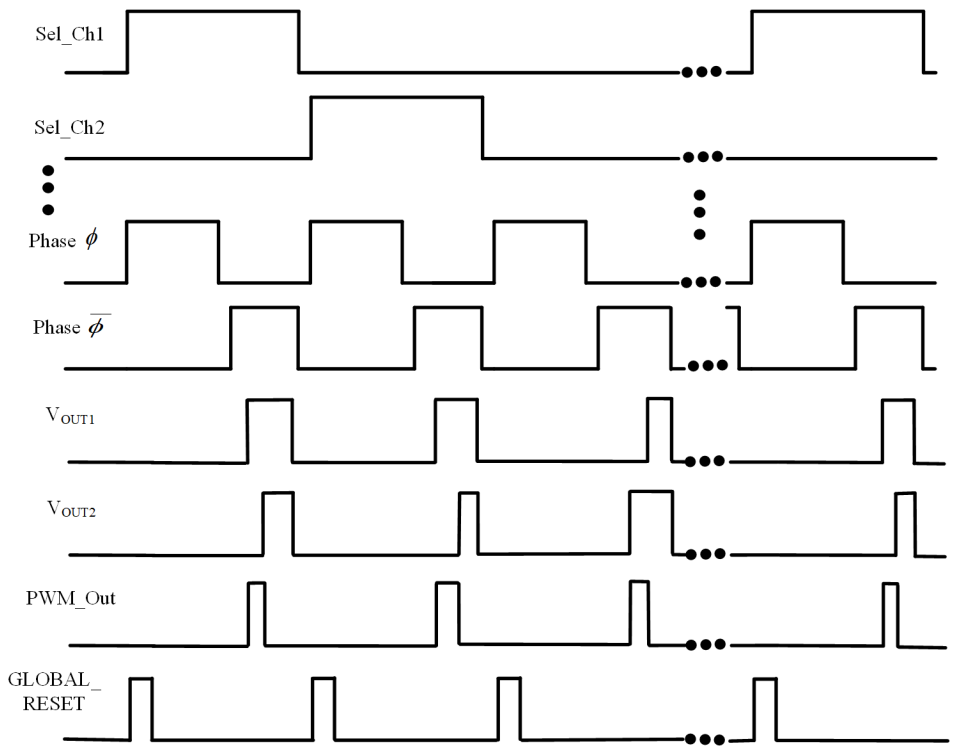

Figure 6.9: *Timing diagram for the PWM generator block.*

explained in Figure 6.9, which in turn is clock gated to get Counter_In, which goes to a counter. After the constant current discharge phase in the reset integrator (as explained in Chapter 4) for each channel, the SEL signal gets activated to push the bits stored in the counter to the serializer and obtain the serial output bit stream. Once a single channel is read out, the GLOBAL_RESET signal gets activated to reset all the flip flops.

6.3 Measurement results

The frontend on flexible foil is fabricated using dual gate self aligned a-IGZO TFT technology from imec, Leuven while the Si backend is fabricated with a standard commercial 180 nm CMOS technology. The system micrograph is shown in Figure 6.11. The total area of the frontend on flexible foil is 602.7 mm^2 (24.4 $mm \times$

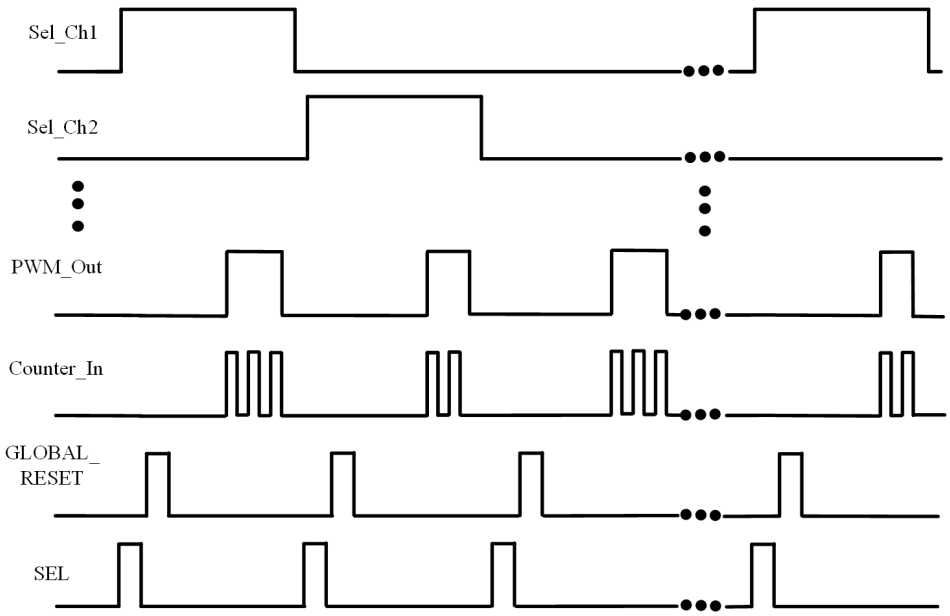

Figure 6.10: *Timing diagram for the Silicon backend.*

24.7 *mm*), while the Si backend takes 1.44 mm^2 (1.2 $mm \times 1.2$ *mm*) of area.

6.3.1 Preamplifier chain characterization

The preamplifier chain (A_{1-3}) along with chopper and de-chopper has been characterized first stand-alone, connecting its output to voltage buffers (TI OPA445AP), followed by an instrumentation amplifier (TI INA111AP) for differential to single ended conversion. The supply voltage is 10 V. Figure 6.12 shows the measured transfer curve of the cascaded preamplifier A_{1-3}. It achieves a gain of 23.3 dB in a 510 Hz bandwidth with 3.1 μA current consumption from 10 V supply. It should be emphasized here, that for this measurement, the capacitors at the output of A_3 are 120 pF each, which results in rather large bandwidth. For the full system architecture, the A_3 stage has been loaded with much higher capacitors to reduce the bandwidth and prevent aliasing in the reset integrator. From this measurement, the integrated input-referred noise in the 1-30 Hz signal BW is 5.8 μV_{rms} with a chopping frequency of 1 kHz. The preamplifier chain achieves experimentally 70.6

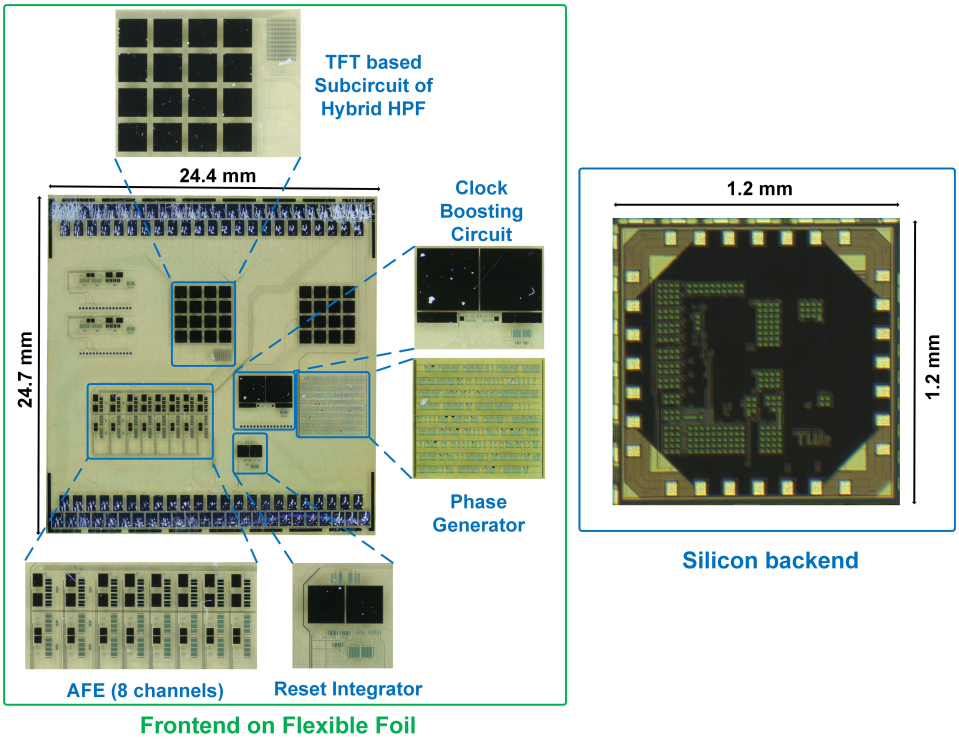

Figure 6.11: *Micrograph of the full system including frontend on flexible foil and Silicon backend.*

dB CMRR and 68.5 dB PSRR with 1 kHz chopping.

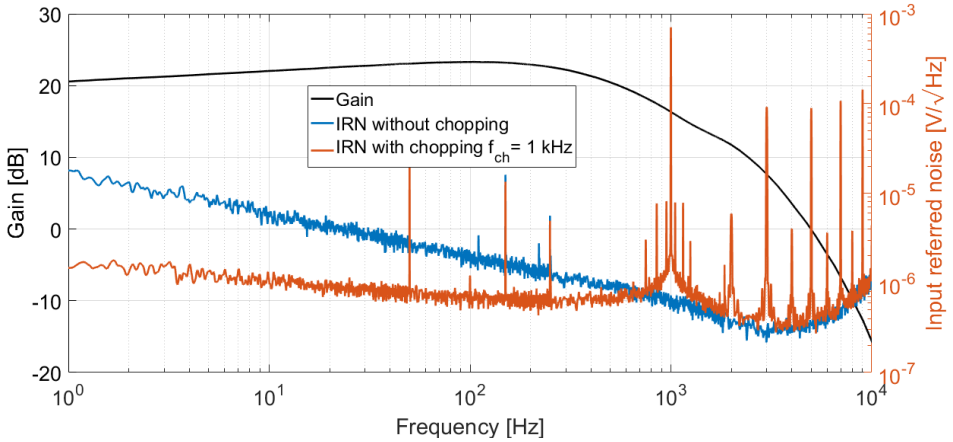

Figure 6.12: *Measured frequency response and input-referred noise of the preamplifier chain (A_{1-3}).*

6.3.2 Full system characterization

The supply voltage (V_{DD}) for the TFT based subsystem is 10 V w.r.t. V_{SS} of 0 V. The supply voltage (V_{DD}) for the Si backend is 8.3 V w.r.t. V_{SS} of 5 V (i.e. 3.3 V operation). A 3.3 V Si technology (which has higher threshold voltage) has been chosen due to increased reliability and robustness required for interfacing with high voltage TFT technology. The V_{SS} of the Si IC has been selected to be equal to the half-rail voltage of the TFT foil (V_{ref1}), to enable direct connection of the HPF control voltages generated on the Si IC to the TFT circuitry, avoiding any level shifting.

For the full system characterization, a 5 mV_{p-p} sine wave with varying frequency was applied to the input of a single channel of the system and the output digital bit stream was observed. The output capacitors on the A_3 stage in the full system are increased to 675 pF each on-foil, to reduce the signal bandwidth before the reset integrator. The midband gain is 25.9 ms/V with 0.035-75 Hz bandwidth as shown in Figure 6.13. The integrated input referred noise for the full system in 1-30 Hz BW is 6.45 μV_{rms} with a chopping frequency of 1 kHz as shown in Figure 6.14. Figure 6.15 shows the measured channel crosstalk, when a 5 mV_{p-p} 10 Hz sine wave input is applied to channel 1. The outputs of channels 2-8 at the signal frequency are between 26.7 dB and 35.9 dB below the output of Channel 1.

It can be seen from the measurement in Figure 6.13 that the lower cut off frequency is as low as 0.035 Hz, thanks to the pseudoresistor and its control loop, including the Si IC. The integrated on-foil input capacitor C_{in} in hybrid HPF in each channel is 520 pF, which results in a pseudoresistor impedance of 17.5 $G\Omega$ at 0.035 Hz. Indeed, the input impedance of the system is dominated by the impedance of pseudoresistor. The power consumption for the frontend on flexible foil is 352 μW (including all channels) from a supply voltage of 10 V, while the Si backend consumes 321.5 μW from 3.3 V. Thus, the resulting total power consumption per channel is 84 μW.

Table 6.1 presents a comparison between the FHE EOG system in this Chapter

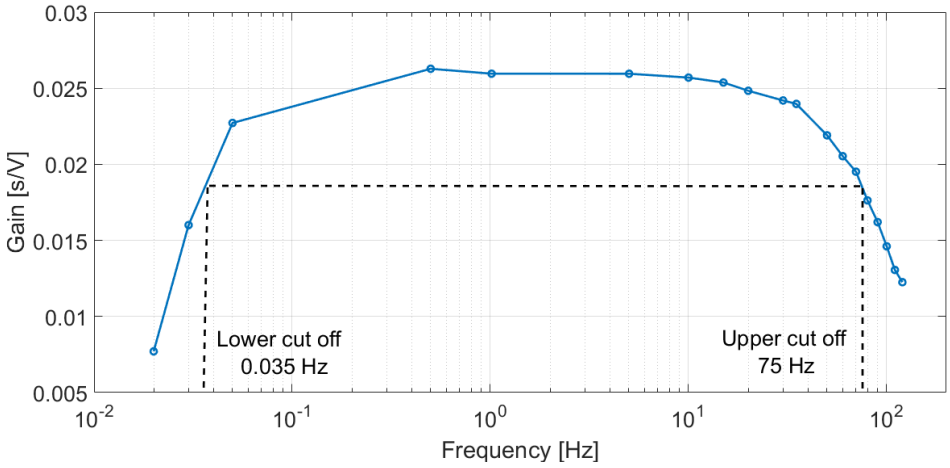

Figure 6.13: *Measured transfer function of the full system.*

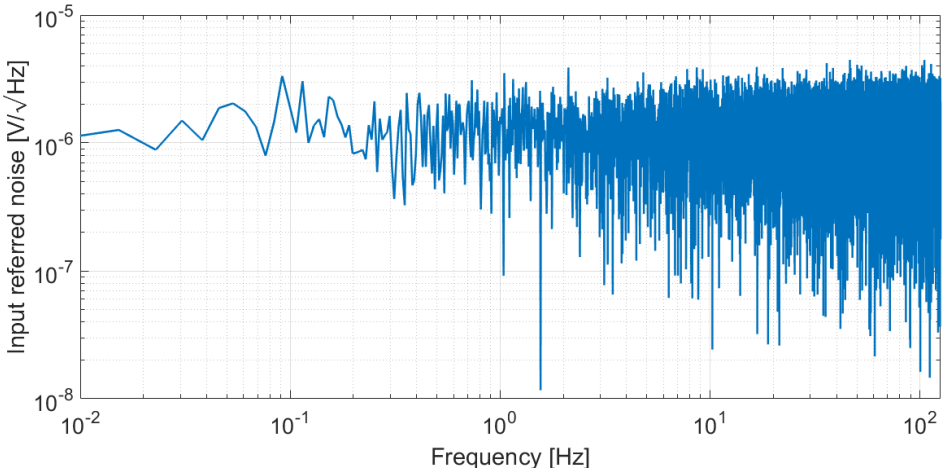

Figure 6.14: *Measured input referred noise of the full system.*

with previous state-of-the-art systems in flexible technologies. In [1, 2, 3, 4] digital signal processing is not performed on the chip. [5] has digital signal processing on flexible foil which increases the overall power dissipation of the system. Moreover, [5] presents a single channel system which does not fully leverage the large area character of flexible technologies. In [1], external discrete components are used to realize the HPF and the power dissipation of the flexible system is higher than other works. The system presented in [2] has still a large power consumption, needed to provide high input impedance. The system in [3], provides a rather low input

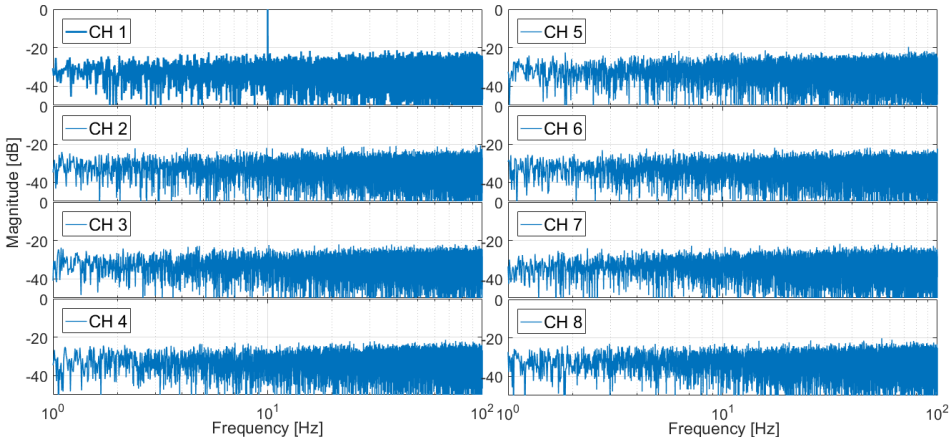

Figure 6.15: *Measured crosstalk of the full system.*

impedance, which can cause problems when using actual electrodes to capture signals. In our system, the frontend on flexible foil is integrated with a minimum number of interconnections with a Si IC for backend computation, which results in low cost, enhanced user comfort, better computational capability and low power dissipation.

6.4 Conclusions

We demonstrate a fully integrated 8 channel FHE EOG acquisition system fabricated in a-IGZO technology, interfaced with a custom Si IC used for backend operations. In this way the low cost, flexible form factor and large area character of the flexible TFT technology are leveraged, while exploiting at the same time the complex computational capabilities of Si ICs with low power dissipation. A tunable hybrid HPF has been integrated in the system which is used to block DC electrode offset and results in low high-pass cut-off frequency. The EOG signals can be acquired from multiple channels using time division multiplexing. The acquired signals are converted to PWM using a reset integrator which is interfaced to a Si IC in the current domain. The current domain interface enables the functionality of the full system, where both the subsystems use very different supply voltages. The

custom Si IC is used to quantize the PWM and provide output as a serial digital output bit stream. The use of a custom Si IC reduces total system power considerably compared to previously published flexible counterparts.

Table 6.1: *Comparison with the state-of-the-art*

	[1]	[2]	[3]	[4]	[5]	**EOG Acquisition System**
Technology	a-Si	a-IGZO	DNTT	a-IGZO	a-IGZO	a-IGZO + 180 nm CMOS
Architecture	Chopped Amplifier	Chopped Amplifier with Frequency Division Multiplexing	Amplifier with AC Coupled Load	Amplifier with Diode Connected Load	Chopped Amplifier + Low Pass Filter + Reset Integrator + DSP on foil	Hybrid High Pass Filter + Chopped Amplifier + Low Pass Filter + Multiplexer + Reset Integrator + DSP using Si IC
Integrated DSP	No	No	No	No	Yes (DSP on foil)	Yes (DSP on Si IC)
Output Type	Analogue	Analogue	Analogue	Analogue	Digital	Digital
Number of Channels	7	4 x 4	8 x 8 (16 Amplifiers in sharing)	16 (Single Ended)	1	8
Application	EEG	EMG	EMG	EMG	ECG	EOG
Chopping Frequency [kHz]	5	5	-	-	1	1
Integrated Noise [μV_{rms}](BW)	2.3 (100 Hz)	125 (500 Hz)	-	-	8 (100 Hz)	6.45 (30 Hz)
CMRR [dB]	<50 @ 50 Hz	-	-	-	67.4 @ 50 Hz	70.6 @ 30 Hz
PSRR [dB]	-	-	-	-	58.9 @ 50 Hz	68.5 @ 30 Hz
Input Impedance [$M\Omega$]	0.26	29.6	0.032 @ 100 Hz	2500[a]	16.5 @ 50 Hz	17500 @ 0.035 Hz
Supply Voltage [V]	55	26	2	5	10 & 5	10 & 3.3
Power Dissipation/Channel [mW]	11	1.3	0.03	0.008	0.28 + 15.4	0.044[b] + 0.040
Total Area [mm^2]	5776	205.4	1800	900[c]	24 + 99.3	602.7 + 1.44

[a] Capacitive impedance is given without mentioning frequency.
[b] Phase generation block not included.
[c] Estimated.

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Chapter 7

A Digitally Assisted Tunable High Pass Filter

This Chapter presents a method to build a digitally assisted tunable high pass filter for biomedical applications. The principle is tested in simulations, using a circuit designed with unipolar a-IGZO TFTs. The presented approach is useful not only for setting a sub Hz cut off frequency, but it is also shown to be effective in counteracting parameter and supply voltage variations. The method presented in this Chapter can also be applied to Silicon-based circuits.

The contents of this Chapter have been published in ISCAS 2020 [1] conference proceedings.

7.1 Introduction

High pass filters are widely used in bio-signal acquisition systems to block electrode DC offset. The cut off frequency of these filters is typically in sub Hz range, needing large resistor and/or capacitor values that are difficult and expensive to implement in integrated circuits due to the large area required. This high-pass pole is, thus, generally implemented with pseudo-resistors [2, 3, 4, 5], that suffer from very large variations due to process, supply voltage and temperature (PVT). While temperature is not a major concern in wearables, due to the close contact with the constant-temperature human body, TFT technologies are typically characterized by large transistor variations, which make even more compelling the need for TFT parameter-insensitive solutions to implement the high-pass filter. This issue is addressed here presenting a novel idea to implement a tunable high pass filter, which ensures good robustness to process and supply variations and can be applied to a-IGZO as well as to Silicon-based circuits.

The rest of the Chapter is organized as follows: The system architecture is discussed in Section 7.2, while Section 7.3 discusses the circuit principle. Simulation results are presented in Section 7.4 and Section 7.5 concludes the Chapter.

7.2 System architecture

The general architecture of master-slave [6, 7, 8, 9] digitally assisted filters is shown in Figure 7.1a. The master filter is a replica of the slave filter. In this scheme a reference voltage signal V_{ref} (a sinusoid digitally synthesized locally with the help of a digital to analogue converter) is applied to the master filter. The output response of the master filter is applied to the control circuitry, which generates a control signal that is fed back to the master filter, tuning it towards the desired frequency response. The control signal is applied to the slave filter too. After some

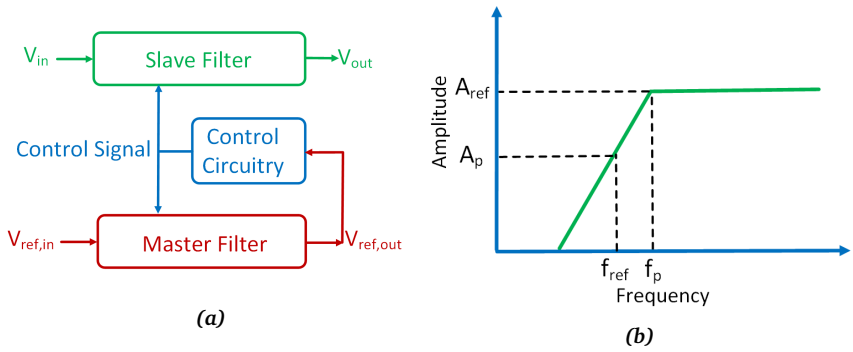

Figure 7.1: *(a) General system architecture and (b) General high pass filter response.*

iterations, the loop locks to the desired tuning point. Once the loop has stabilized, the control circuitry and the reference generator can be turned off to save power and avoid any digital switching on the foil, minimizing interference. However, this part of the system can be turned on periodically to recalibrate the slave filter. One of the factors which affects accuracy in this approach is matching between master and slave filters. Nevertheless, layout matching techniques can be used to mitigate this problem.

7.3 Circuit principle

The approach proposed in this Chapter exploits the attenuation that a reference sinusoidal signal experiences when its frequency is lower than the cut off of a high pass filter. If a sinusoidal signal, V_{ref}, with amplitude A_{ref} and frequency f_{ref} is applied to a first-order high pass filter, having a cut off frequency f_p higher than f_{ref}, then (as shown in Figure 7.1b) the attenuated filter output amplitude A_p and the passband frequency f_p are related by the expression:

$$f_p = \frac{f_{ref} A_{ref}}{A_p} \tag{7.1}$$

which is valid as long as $f_{ref} << f_p$ (and $A_p << A_{ref}$). In this way, for a given amplitude A_{ref} and frequency f_{ref}, monitoring the attenuated signal, A_p, at the output of the high pass filter can be used to tune the high pass filter for a desired passband frequency f_p.

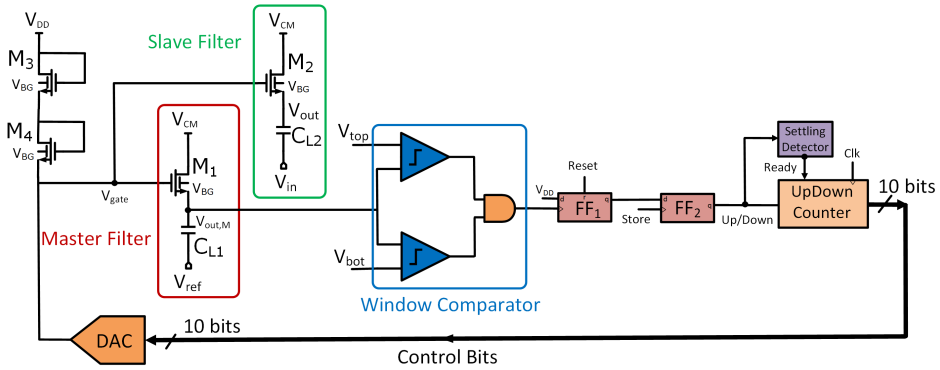

Figure 7.2: *Circuit schematic of the proposed system.*

A high-level circuit schematic of the proposed approach is shown in Figure 7.2, while Figure 7.3 shows the voltage waveforms at the most relevant nodes. The master filter consists of TFT M_1 and capacitor C_{L1}, while the slave filter consists of TFT M_2 and capacitor C_{L2}. Both TFTs are driven in deep subthreshold to implement very large small-signal equivalent resistances in the linear regime. The input of the master filter is fed with a sinusoidal signal having frequency f_{ref} and amplitude A_{ref}. The attenuated output of the master filter ($V_{out,M}$) is monitored by a window comparator (having V_{top} and V_{bot} as the upper and lower threshold for the window, so that $V_{top} - V_{bot} = 2 \times A_p$). A Reset signal consisting of short pulses at frequency equal to half f_{ref} is generated, so that the flip-flop FF_1 observes the output of the window comparator for about two periods of the input sinusoidal signal. If the output filter amplitude exceeds the target size A_p during this time FF_1 is set, otherwise it remains reset. The state of FF_1 is stored in FF_2 just before resetting the first flip-flop. The output of FF_2 (Up/Down) controls the counting direction of a 10 bit up/down counter, which generates control bits for the current-domain digital

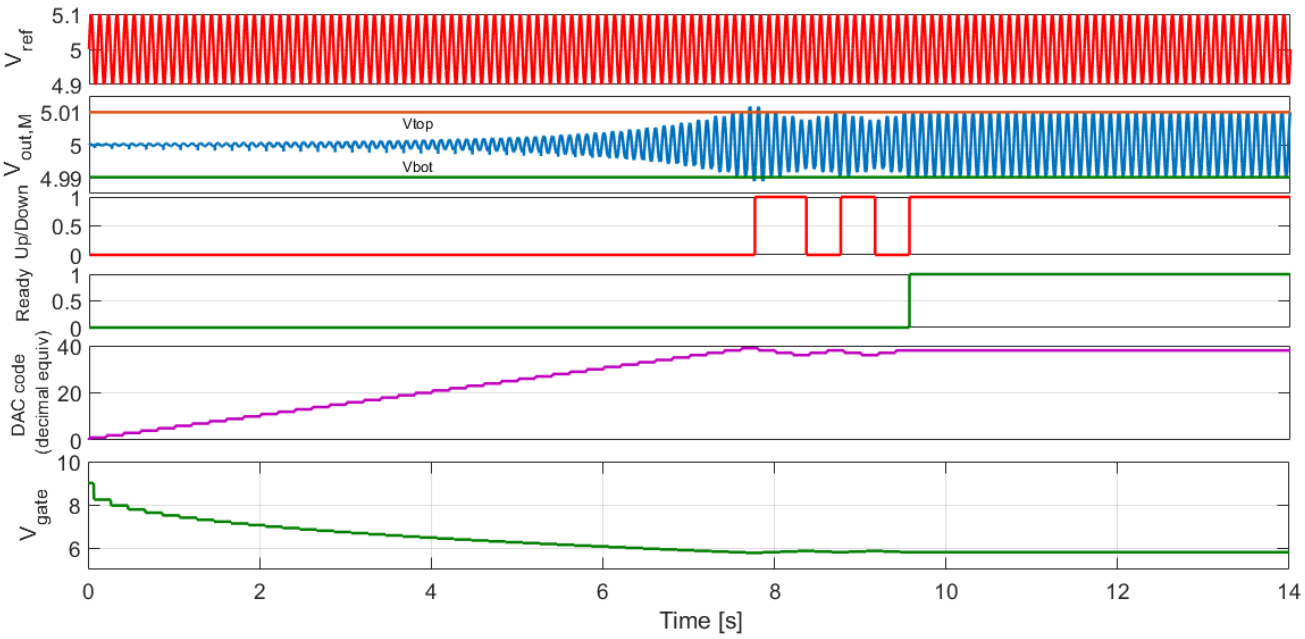

Figure 7.3: *Waveforms at different nodes of the system depicting operation of the system. To show more clearly how the system works, an 8 bit counter and DAC are used to generate this figure.*

to analog converter (DAC). If FF_2 is in reset state the counter goes up, otherwise it counts down. The output current of the DAC flows in the diode connected TFTs M_3 and M_4, controlling the gate biasing of the transistors M_1 and M_2 to achieve the desired passband frequency of the filter and the target attenuated amplitude A_p. After convergence of the feedback loop, the system would continue toggling the amplitude of the master filter output around the value of A_p determined by the threshold voltages of the window comparator. This is not needed, thus a settling detector can be used to monitor the settling behaviour of the loop. Once the output of FF_2 has toggled a certain number of times, the filter bias point has settled to the desired value, and a ready flag can be generated (Ready) to freeze the counter and the DAC output to the target code value. At this instant the DAC code can be preserved in a register, while the controlling circuitry and the reference generator could be turned off to reduce power dissipation.

The design Equation 7.1 can be further modified by incorporating scaling factors between the master and slave filters as shown below:

$$f_p = \frac{f_{ref} A_{ref}}{n_1 n_2 A_p} \tag{7.2}$$

where, $n_1 = \frac{C_{L2}}{C_{L1}}$ and $n_2 = \frac{(W/L)_{M_1}}{(W/L)_{M_2}}$.
Hence, a wide tuning range of f_p can be achieved by appropriately choosing the parameters shown in Equation 7.2.

7.4 Simulation results

The system is simulated using models of the a-IGZO TFTs provided by the TFT foundry for the filters and the DAC, together with behavioural models of the other building blocks in the control circuitry. To show a proof of the concept introduced in the previous section, a high pass filter for a passband frequency of 0.5 Hz has been designed. The optimized design parameters are f_{ref} = 10 Hz, n_1 = 10, n_2 = 20 and A_{ref}/A_p = 10. One of the most variable parameters in TFT circuit design

is the threshold voltage, V_T. The threshold voltage varies from wafer to wafer and also changes with TFT bias stress or aging. If no tuning scheme would be applied, the sensitivity to threshold variations in the proposed filter circuit would be especially strong, as the transistors M_1 and M_2 are driven in subthreshold to realize large time constants.

Figure 7.4 shows the relative error in passband frequency obtained from sim-

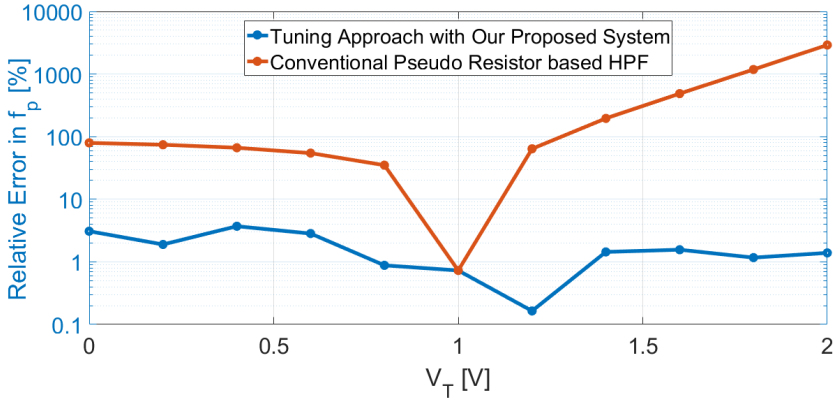

Figure 7.4: *The effect of threshold voltage variation on the relative error in f_p.*

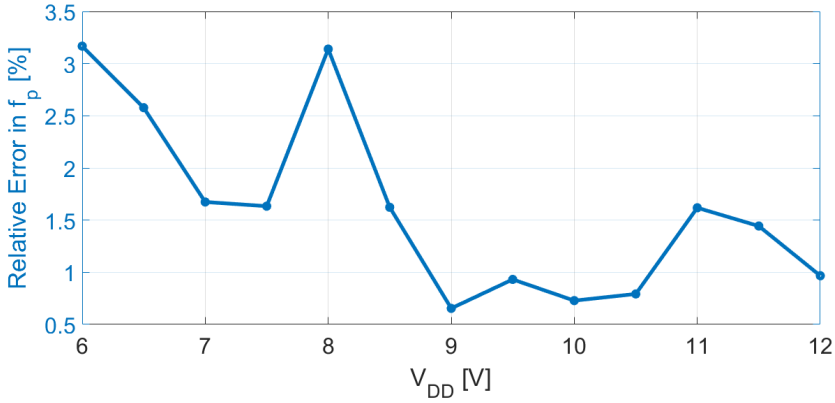

Figure 7.5: *The effect of V_{DD} variation on the relative error in f_p.*

ulations with respect to the value obtained from Equation 7.2, when varying V_T by 2 V and using the proposed tuning approach. Results are also compared to a conventional high pass filter based on pseudo-resistors. It can be seen that the rel-

ative error in the realized passband frequency using the proposed tuning scheme is within 4%, while the error is very large for the conventional pseudo-resistor approach. Figure 7.5 shows the effect of V_{DD} variation on the relative error in f_p. It can be seen from the plot that f_p remains within 3.5% of its theoretical value for a V_{DD} variation as large as 6 V, confirming a good robustness of the proposed approach to supply voltage variations. Figure 7.6 shows the behaviour of f_p and of the relative error in f_p when changing f_{ref} from 1 Hz to 100 Hz. It can be seen from the plot that a tuning range of f_p spanning two decades from 0.05 Hz to 5 Hz can be achieved while keeping a maximum 1% relative error. Figure 7.7 shows the effect of A_{ref}/A_p ratio variation on f_p and the relative error in f_p. It can be observed that the relative error in f_p remains less than 3% for a wide range of of A_{ref}/A_p ratios. Figure 7.8 shows the relative error in f_p when varying A_p while keeping $A_{ref}/A_p = 10$, to maintain the target passband frequency constant. It can be seen from the plot that the relative error in passband frequency increases linearly in a staircase pattern and remains less than 5% till 30 mV A_p amplitude, when the input reference amplitude is thus 300 mV. The fact that input signals of several hundreds of millivolt can still be tolerated shows the robustness of the proposed approach for the application to input filters (where typical signal amplitudes are small).

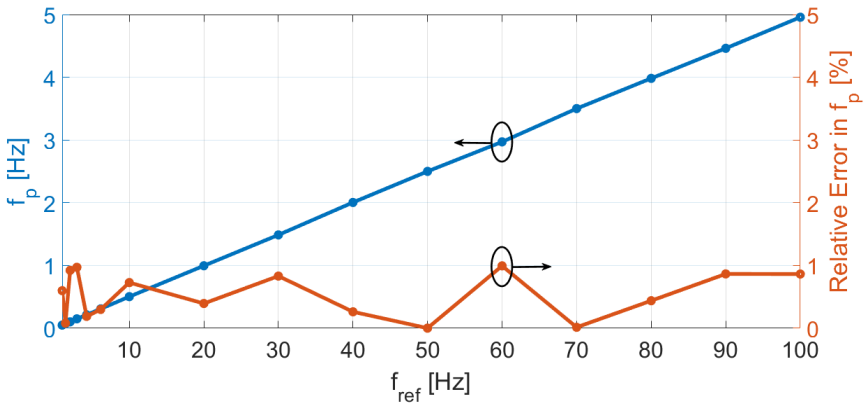

Figure 7.6: *The effect of f_{ref} variation on f_p and the relative error in f_p.*

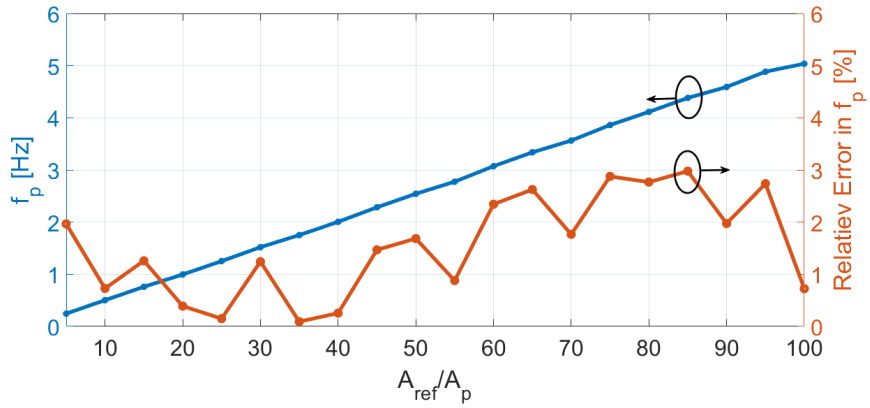

Figure 7.7: *The effect of A_{ref}/A_p ratio variation on f_p and the relative error in f_p.*

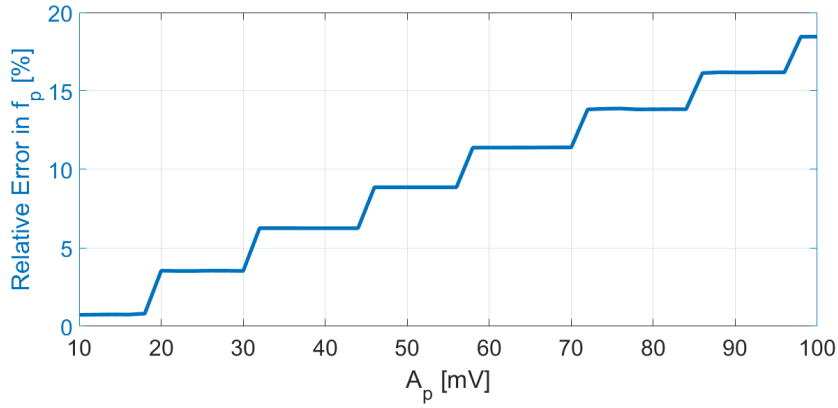

Figure 7.8: *The effect of A_p variation in f_p (keeping the A_{ref}/A_p ratio constant).*

It can be observed that the relative error in f_p is limited by the finite resolution of the DAC, the loop settling and matching of the master and slave filters. The inaccuracy in f_p caused by mismatch and scaling of the master and slave filters can be minimised by unary element layout.

7.5 Conclusions

A method to build a digitally assisted tunable high pass filter for biomedical applications is discussed in this Chapter, and is simulated using unipolar a-IGZO TFTs. The presented system leverages the signal attenuation by the high pass filter when

a reference sinusoidal signal with a frequency lower than the cut off frequency is applied, to tune a master-slave filter structure. The results presented in this Chapter show that sub Hz cut off frequencies can be obtained with less than 5% relative error in presence of large TFT parameter and supply variations. The proposed tuning scheme can be applied to improve the precision of high pass filters for biomedical applications implemented in a-IGZO and also in Silicon.

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Chapter 8

Conclusions

8.1 Conclusions

This dissertation illustrates various circuit design and system level solutions to enable bio-signal monitoring on a flexible foil. The results presented in this thesis are the first steps towards building a low cost health patch with flexible electronics capable of monitoring vital signs.

After an introduction to a-IGZO TFT technology in Chapter 2, in Chapter 3, the key design trade-offs in bio-signal front-end architectures that are especially relevant to a-IGZO TFT circuits, are discussed. The diode-connected load amplifiers with cascaded stages offer a good compromise of performance and robustness. For this reason, they have been chosen as preamplifiers for the system architectures presented in this thesis.

Chapter 4 presents a voltage to pulse width conversion technique using a reset integrator with a switched capacitor load. This technique is especially suitable for unipolar technologies which do not offer complementary loads. Additionally, the input is transformed to the time domain which paves the way to a radically different analogue to digital conversion approach. The analogue to digital conversion for bio-signal acquisition systems is performed in two steps. In the first step, as presented in Chapter 4, the input signal is transformed to a binary pulse width modulated (PWM) representation, using a time based reset integrator. In the second step, the output PWM is quantised in time to get a digital representation (discussed in Chapter 5). The proposed technique is utilised to realize a time based heart-rate measurement interface, that requires a moderate SNR. The presented solution is compact, low cost and adds to user comfort, thanks to its mechanical flexibility. However, this approach achieves an SNR that is insufficient for most biomedical monitoring applications. It has been shown that SNR could be improved by applying CDS at system level to enable applications that are more demanding in terms of SNR, e.g. ECG monitoring. It can be concluded that the transformation of an input signal from the voltage domain to the time domain in a simple, minimalistic and energy efficient manner opens an arena of opportunities

in unipolar technologies, where high gain amplifiers are not easily available.

In Chapter 5, we present the fundamental steps to demonstrate intelligent plasters for biomedical applications based on flexible electronics which are compatible with the NFC standard. The presented approach provides a digitization strategy using a time reference, without the need for a voltage reference, and thus is particularly suited to implementation with a-IGZO TFTs on foil. The output is transformed to the digital domain and provided as a 105.9 kb/s Manchester encoded serial bit stream. To the best of author's knowledge, this is the first demonstrated ECG acquisition system in flexible a-IGZO TFTs on foil providing a digital serial output bit stream compatible with the NFC standard. The circuit improvements (e.g. implementation of anti-aliasing filtering before the reset integrator) and better TFT technology used for this design (the DUGA technology which is faster and has better 1/f noise performance), results in the best NEF and PEF values reported in literature for a-IGZO TFT circuits to date.

In the context of the reset integrator, which has been the core circuit block used in this thesis, the following conclusions can be drawn:

- The single slope integrator is optimal in terms of gain but not linearity. Linearity can be improved by adding a constant current discharge phase that improves linearity at the cost of gain.
- The voltage to time conversion gain of a single reset integrator is not sufficient to use in practical applications. Hence, a gain stage is required in front of the reset integrator.
- In order to reduce noise folding, a low pass filter acting as an anti aliasing filter should be used in front of the reset integrator.

In Chapter 6, a multichannel hybrid flexible electronics system for EOG application is presented. The system, consisting of a multichannel frontend acquisition system based on a-IGZO TFTs manufactured on flexible substrate, is interfaced

with a Silicon-based custom IC for digitization of the acquired signal. In this way, low cost, flexible form factor and the large area character of the flexible technology are leveraged, while exploiting at the same time the complex computational capabilities and low power dissipation of Silicon ICs. The system is designed in a novel way to reduce the number of interconnects from the flexible system to the Silicon IC. A tunable hybrid HPF has been integrated in the system which is used to block DC electrode offset and results in low high-pass corner frequency. The use of a custom Si IC reduces the total system power considerably considering flexible counterparts.

In Chapter 7, a digitally assisted tunable high pass filter for biomedical applications is presented. We can conclude from the presented results that sub Hz cut off frequencies can be obtained with good accuracy in presence of large TFT parameter and supply variations. The proposed tuning scheme can be applied to improve the precision of high pass filters for biomedical applications implemented in a-IGZO and also in Silicon.

8.2 Future work

From the circuit design perspective, many innovations could be added to the core reset integrator circuit e.g. instead of adding a voltage gain stage in front of the reset integrator, a time domain gain stage can be added, which will result in energy efficient and completely time domain operation of the circuit.

From the technology perspective, DUGA a-IGZO TFT technology appears to be a promising solution to implement a wearable bio-signal acquisition system. However, scaling of the feature size would be required to not only reduce circuit footprint, but also to increase the transition frequency of the TFTs. Moreover, advancements of the technology process will be required to push the performance of the TFTs in terms of transconductance and 1/f noise.

Although the models presented in Chapter 2 describe the TFT behaviour quite

well, a more sophisticated model is required to incorporate variability, mismatch and other second order effects such as a better description of the dynamic behavior, to design complex variability-insensitive circuits and systems.

The availability of a Process Design Kit (PDK), in order to design complex systems on foil is of uttermost importance. However, Electronic Design Automation (EDA) tools for flexible technologies are still in their nascent phase. Hence, in order to enable the design of complex systems on foil, a PDK specifically developed for flexible technologies is required.

Summary

Integrated Circuits for Wearable Systems based on Flexible Electronics

Electronics has witnessed a transformation in recent years, due to the rapid rise of wearables and ubiquitous sensors, fostering the advent of Internet of Things (IoT). There are applications which are not trivial to be implemented by traditional electronics such as displays, imagers, photovoltaic cells, near field communication (NFC) tags, wearable sensors for biomedical signals monitoring etc. These applications require a large surface to be covered with electronics and are difficult or costly to achieve with the conventional Silicon-based Integrated Circuits (ICs). However, advancements in the technology process of thin-film transistors (TFTs) have paved the way to fabricate devices over large areas and have opened the possibility to use plastic foils to provide mechanically flexible substrates. This type of devices not only result in electronics distributed over a large area, but also leads to lower cost per unit area compared to conventional ICs. The inherent flexible nature of the substrates has been leveraged in applications requiring conformability, bendability, foldability and stretchability. A specific category of applications that can strongly benefit from the flexible electronics is the domain of flexible and comfortable wearable devices for wellness and healthcare monitoring.

The aim of this thesis is to advance the state-of-the-art of flexible electronics with specific focus on wearable bio-signal measurement systems. A bottom-up design approach is used to design wearable bio-signal interfaces.

After an introduction to a-IGZO TFT technology in Chapter 2, in Chapter 3, we demonstrated the design of single stage and multi-stage amplifiers with different topologies to get an insight into performance trade-offs and maximum gain architecture in unipolar flexible technologies.

Moving up in the design approach, we present a novel voltage to pulse width conversion technique using a reset integrator with a switched capacitor load, exploiting a simple and power minimalistic implementation. This technique is especially advantageous in unipolar technologies, which do not offer complementary loads. Additionally, the signal can be easily transformed to a binary pulse width modulated (PWM) representation, paving the way to a radically different analogue to digital conversion (ADC) approach. Indeed, to perform ADC, the PWM signal is simply quantized in time and transformed to a digital word using a counter. The transformation of the input signal from voltage to time domain in a simple, minimalistic and energy efficient way enables a wide spectrum of opportunities in unipolar technologies, where high gain amplifiers cannot be easily implemented.

This proposed technique is used first to realize a time-based heart-rate measurement interface, presented in Chapter 4. Then, it has been shown that the signal to noise ratio (SNR) can be improved by applying correlated double sampling at system level, enabling applications that are more demanding in terms of SNR.

In Chapter 5, we report on a flexible electrocardiogram (ECG) sensor which exploits TFT-based circuits on flexible foil and the reset integrator approach to implement the full chain of signal acquisition, amplification and digitization and is capable to measure ECG signals for the first time on foil (to the best of the author's knowledge). The presented approach provides digitization using a time reference, with no need for a voltage reference, and thus, is particularly suited to implementation with a-IGZO TFTs in the framework of an NFC system, where a precise clock can be generated based on the received carrier. Additionally, a 105.9 kb/s Manchester encoded bit stream compatible with the NFC standard is generated at the output.

Further, Chapter 6 presents a multichannel EOG acquisition system based on flexible TFTs and CMOS technologies. The system, consisting of a frontend acquisition system based on a-IGZO TFTs manufactured on flexible substrate, is interfaced with a Silicon based custom IC for digitization of the acquired signal. In this way the low cost, flexible form factor and the large area character of flexible TFT technology are leveraged, while utilising at the same time the complex computational capabilities and low power dissipation of Silicon ICs. The system is designed in a novel way to reduce the number of interconnects from the flexible system to the Silicon IC. A tunable hybrid HPF has been integrated in the system which is used to block DC electrode offset and results in low high-pass corner frequency. The use of a custom Si IC reduces the total system power considerably compared to flexible counterparts.

Chapter 7 presents a digitally assisted tunable high pass filter for biomedical applications. HPFs are widely used in bio-signal acquisition systems to block electrode DC offset. The cut off frequency of these filters is typically in sub Hz range, needing large resistor and/or capacitor values that are difficult and expensive to implement in integrated circuits due to the large area required. The proposed architecture provides a solution to this issue. It is shown that accurate sub Hz cut off frequencies can be obtained in presence of large TFT parameter and supply variations. The proposed tuning scheme can be applied to improve the precision of high pass filters for biomedical applications implemented both in a-IGZO and in Silicon.

List of publications

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Acknowledgments

They say the important thing in life isn't the destination, it's the journey...
The challenges you face along the way...
The unexpected twists and turns...
The disappointments you overcome...
— Modern Family S3:E21

... So, here it goes. One of the finest journeys of my life comes to an end. During the last five years, I have had the opportunity to work with some of the smartest people around. Each of them has taught me something new, either directly or indirectly. This thesis would be incomplete without an expression of deep gratitude towards these people and others who have helped and supported me during the brightest and the darkest times. I would like to acknowledge as many of them as I can in the following paragraphs.

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Curriculum Vitae

Mohammad Zulqarnain was born on 15-08-1990 in Aligarh, India. After finishing his senior secondary school in 2007, he enrolled in Bachelor of Technology (B.Tech) in Electronics Engineering at Zakir Husain College of Engineering and Technology, A.M.U., Aligarh. In 2015, he graduated in Master of Technology (M.Tech) with specialization in Electronic Circuits and System Design with University Medal for standing first in all branches of M.Tech. In October 2015, he started a PhD project at Eindhoven University of Technology, The Netherlands in collaboration with imec-NL/Holst Centre. The results from his research are presented in this thesis.