Area-selective atomic layer deposition for bottom-up fabrication of nanoelectronics

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Ever since Richard Feynman's lecture on nanotechnology entitled *There is plenty of room at the bottom*, one of the main challenges in nanoscience has been to develop reliable approaches for bottom-up processing of materials. Despite this vision, the miniaturization of electronics in the past few decades according to Moore's law relied completely on innovations in top-down processing. In this article, the alternative of using area-selective ALD for bottom-up fabrication is discussed. The approaches that currently exist for achieving area-selective ALD are reviewed, together with their merits and limitations.

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Motivation for area-selective ALD

The multilayered devices at the heart of every integrated circuit are fabricated by repeating deposition, lithography and etching steps for each device layer, as illustrated in figure 1. Area-selective deposition (ASD) focuses on the deposition of material only where it is needed, and thereby eliminates the need for a lithography and an etching step after the deposition [1,2]. Because of the atomic-level control of ALD and its strong dependence on the surface chemistry of the substrate, it has been considered as an ideal starting point for the development of ASD processes.

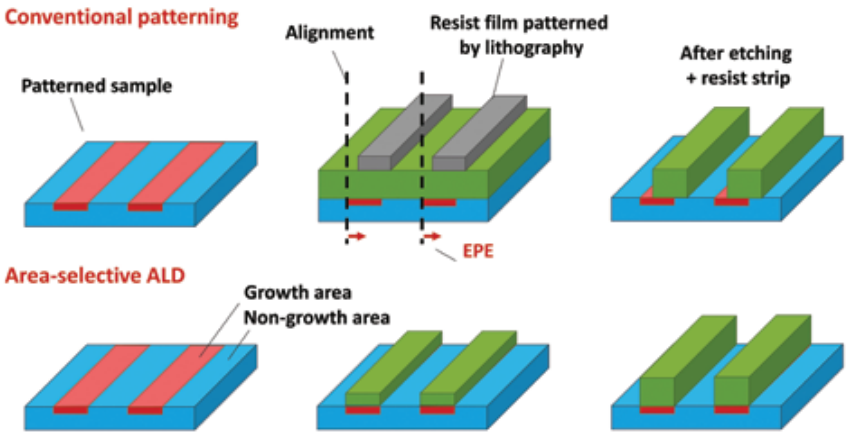


Figure 1 Conventional patterning relies on repetition of deposition, lithography and etching steps for every layer in a multilayered device. At the small dimensions of current and future devices, it is often difficult to align features on top of each other, which results in an edge placement error (EPE). Area-selective ALD solves alignment issues, and eliminates etching and lithography steps.

There are several different motivations for working on area-selective ALD. The early work on area-selective ALD aimed at reducing the complexity of nanofabrication and at dealing with compatibility issues [1]. When working with materials that are not compatible with conventional etching or lift-off steps, it is desired to process the material in a bottom-up fashion. These initial studies predominantly focused on the development of methods that involve patterning steps. For instance, our previous work aimed at the patterning of contacts on sensitive nanomaterials such as carbon nanotubes and graphene by a combination of e-beam patterning and ALD [3,4].

In recent years, most work on area-selective ALD is motivated by challenges in alignment for sub-5nm technology nodes [2,5]. With the downscaling of nanoelectronics, it becomes more and more difficult to align structures relative to one another during the fabrication of multilayered device structures. The alignment is typically described by referring to the parameter *edge placement error* (EPE), which is allowed to be roughly a quarter of the size of the structure (i.e. ~2nm for a critical dimension of 10nm). Area-selective ALD is currently explored for applications in *self-aligned* fabrication schemes. For these applications, a partially processed device structure fabricated using conventional top-down

fabrication is considered that consists of different materials (figure 1). Performing ALD selectively on only one of these materials results in a perfectly aligned structure, while the costly lithography and etching steps are eliminated.

An example of such an application is the fabrication of *fully self-aligned vias* (FSAV) [6]. Currently, EPEs in interconnects or VIAs are a limiting factor in device reliability, for example by introducing shorts. Area-selective ALD processes for dielectric-on-dielectric deposition, considering a metal as the non-growth area, are currently being explored for the deposition of a topographical barrier that reduces the chance of shorting.

Besides the focus on nanoelectronics, also some work has been performed that aims at applications in catalysis [7]. The most prominent example is to synthesize core/shell nanoparticles by area-selective deposition of a shell material on a metallic nanoparticle, with the general aim to improve the catalytic activity of the nanoparticle. Work in this direction focused predominantly on noble metals and led to the synthesis of for example Pd/Pt, Pt/Ru and Pt/FeO_x core/shell particles [8].

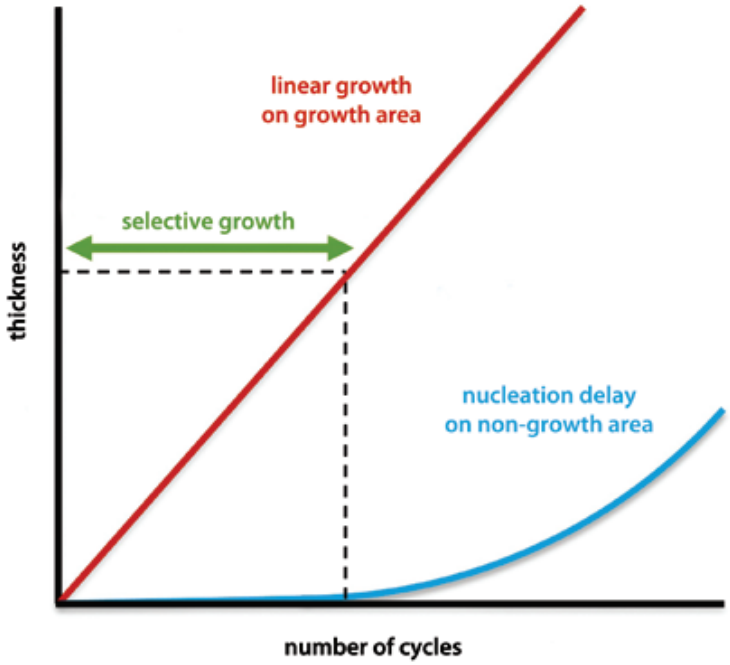


Figure 2 Differences in ALD nucleation on the growth and non-growth areas are exploited to obtain area-selective ALD.

Approaches to area-selective ALD

When considering the applications of area-selective ALD in self-aligned fabrication, the ALD process needs to distinguish between starting surfaces of different materials. Generally, the material on which ALD is desired is referred to as the *growth area*, whereas the material(s) on which no ALD is allowed to occur is described as the *non-growth area* (figure 1). In order to characterize an area-selective ALD process, experiments are typically conducted to investigate the nucleation behavior of an ALD process on different starting surfaces. In case an ALD process results in immediate growth on one material, while there is a nucleation delay on another material, this difference can be exploited to achieve area-selective ALD on the first material, as shown in figure 2 [5]. In ASD, selectivity is defined as the ratio of the amounts of material deposited on the growth and non-growth areas.

If only a thin layer needs to be deposited selectively, in some cases it is possible to make use of chemical differences between the surfaces of the growth and non-growth areas. For example, if an ALD precursor adsorbs readily on the growth area and experiences a significant energy barrier for adsorption on the non-growth area, such a difference can be the exploited for achieving area-selective ALD. In practice, this approach only works for relatively thin layers of only a few nanometers thick, which is often not sufficient for the applications. The most common approach to obtain area-selective is ALD is to functionalize the non-growth area in such a way that the ALD is deactivated on the functionalized surface. A large part of the field focuses on the use of molecules that can form a self-assembled monolayer (SAM) for functionalization of the non-growth area [9]. The general idea is to form a barrier for the ALD precursor to interact with the surface. The preparation of a SAM typically involves immersion of the substrate in solution for > 24 hours.

Advanced ALD cycles

While there are several approaches to achieve area-selective ALD, in general the limitation is that they do not offer sufficient selectivity to allow for area-selective deposition of films with the desired thickness. In practice, there are always unintended side reactions that lead to a loss of selectivity, i.e. the initiation of ALD on the non-growth area. For example, SAMs are often not thermally stable at the temperature of deposition and degrade over time. This implies that it is not adequate to only functionalize the non-growth area *before* the ALD process. In our research, the strategy is to implement vapor-phase correction steps *during* the ALD process, as illustrated in figure 3 [5]. Instead of using conventional two-step ALD processes, ABC-type ALD or supercycle ALD recipes are designed that involve the repetition of surface functionalization or cleaning steps. The focus is on using vapor-phase dosing for the correction steps, in order to develop methods that are very compatible with semiconductor processing flows.

An example of such an approach is to use small molecules as inhibitor [10]. While this approach relies on deactivation of

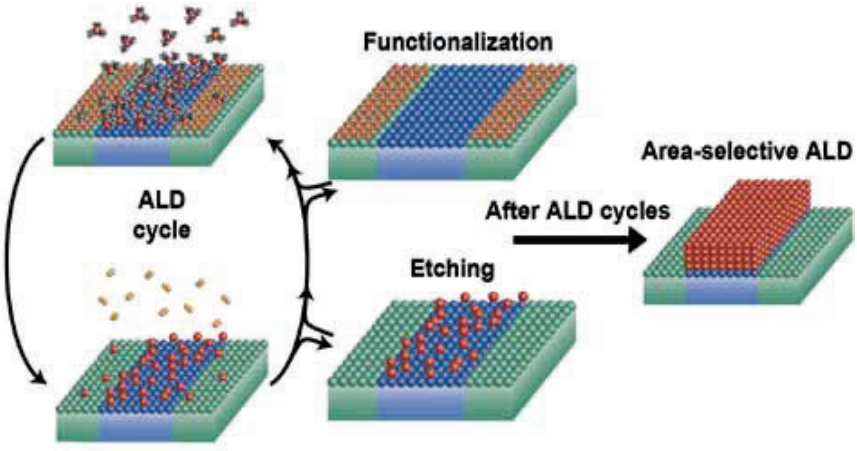
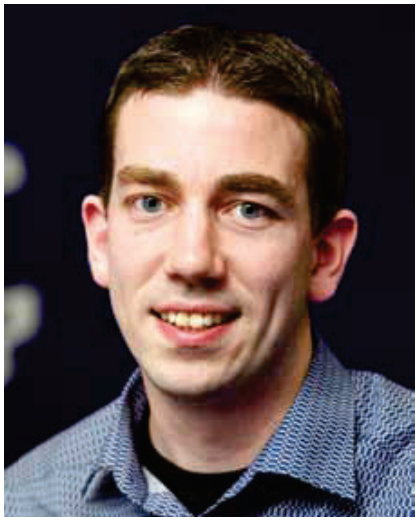


Figure 3 Our strategy for area-selective ALD involves the implementation of vapor-phase corrections steps in an advanced ALD cycle [5].



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the non-growth area similar to previous work involving SAMs, the main difference is that these inhibitor molecules can be dosed during the ALD cycle instead of soaking the sample in solution before the deposition. Because of the re-application of the inhibitor molecules every cycle in an ABC-type recipe, this approach is not sensitive to degradation of the molecules, while it can also be used for a broader range of ALD processes involving for example ozone or a plasma as the co-reactant. Another example of employing an advanced ALD cycle for area-selective ALD is the combination with selective etching to improve the selectivity of ALD [11]. The implementation of an etching step (or an ALE cycle) after a certain number of ALD cycles in a supercycle recipe enables the deposition of thicker films with a high selectivity [5].

Although area-selective ALD has already been researched for over two decades, it appears that the semiconductor industry is now ready for implementing the technique. The fabrication of fully self-aligned vias is likely the first application that will be employed in high volume manufacturing [6], but there are many other applications in nanoelectronics that are currently being explored [2]. With that we are entering a new era in which the fabrication of nanoelectronics relies on both top-down and bottom-up processing.

References

1 A.J.M. Mackus, A.A. Bol, W.M.M. Kessels, *Nanoscale*, **6** (2014) 10941.
2 R. Clark, K. Tapily, K.-H. Yu, T. Hakamata, S. Consiglio, D.O. Meara, C. Wajda, J. Smith, G. Leusink, *APL Mater.*, **6** (2018) 058203.
3 A.J.M. Mackus, N.F.W. Thissen, J.J.L. Mulders, P.H.F. Trompenaars, Z. Chen, W.M.M. Kessels, A.A. Bol, *Appl. Phys. Lett.*, **110** (2017) 013101.
4 N.F.W. Thissen, R.H.J. Vervuurt, A.J.M. Mackus, J.J.L. Mulders, J.W. Weber, W.M.M. Kessels, A.A. Bol, *2D Mater.*, **4** (2017) 025046.
5 A.J.M. Mackus, M.J.M. Merkx, W.M.M. Kessels, *Chem. Mater.*, **31** (2019) 2.
6 *Fully Self-Aligned Vias: The Killer Application for Area-Selective ALD? – A Discussion of the Requirements for Implementation in High Volume Manufacturing.* [online], www.atomiclimits.com/2019/07/18/fully-self-aligned-vias-the-killer-application-for-area-selective-ald-a-discussion-of-the-requirements-for-implementation-in-high-volume-manufacturing
7 K. Cao, J. Cai, X. Liu, R. Chen, *J. Vac. Sci. Technol. A*, **36** (2018) 010801.
8 A.J.M. Mackus, M.J. Weber, N.F.W. Thissen, D. Garcia-Alonso, R.H.J. Vervuurt, S. Assali, A.A. Bol, M.A. Verheijen, W.M.M. Kessels, *Nanotechnology*, **27** (2016) 034001.
9 R. Chen, S.F. Bent, *Adv. Mater.*, **18** (2006) 1086.
10 A. Mameli, M.J.M. Merkx, B. Karasulu, F. Roozeboom, W.M.M. Kessels, A.J.M. Mackus, *ACS Nano*, **11** (2017) 9303.
11 M.F.J. Vos, S.N. Chopra, M.A. Verheijen, J.G. Ekerdt, S. Agarwal, W.M.M. Kessels, A.J.M. Mackus, *Chem. Mater.*, **31** (2019) 3878.