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# High Data Rate W-Band Balanced Schottky Diode Envelope Detector for Broadband Communications

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**Abstract**— This article reports on a W-Band (75-110 GHz) Schottky diode based balanced envelope detector in microstrip technology, featuring a transition from WR-10 to microstrip. The manufactured detector provides 20 GHz of input RF bandwidth within the W-band. A video bandwidth between 4 GHz and 6 GHz is achieved for input RF frequencies between 75 GHz and 88 GHz, allowing error free transmission of signals up to 12 Gbit/s.

**Keywords**— Envelope detectors, millimeter wave communications, Schottky diodes, broadband communications.

## I. INTRODUCTION

Future communication networks need to support the large bandwidth that new mobile and wireless communication services require, e.g., 8k video streaming, holographic conferencing and e-health care, which cannot be supported by the existing 4G networks. Thus, new spectrum assignments in the W-band (75-110GHz) are being considered to achieve peak user data rates in the Gbit/s range [1]–[3]. Furthermore, these wireless links need to be designed using cost effective receiving devices capable of detecting high data-rate signals while minimising the number of components used for detection. Envelope detectors (ED) can be used for demodulating amplitude modulated signals taking advantage of their lower cost and complexity over heterodyne architectures [2]–[4]. EDs are able to demodulate signals without the need for a local oscillator, simplifying the receiver structure at the cost of reducing receiver sensitivity and losing information on the signal phase.

Table 1 summarises the state of the art of W-band EDs when demodulating ASK signals at bitrates between 7.6 Gbit/s and 26 Gbit/s, at carrier frequencies ( $f_c$ ) between 80 GHz and 108 GHz. Although these EDs can demodulate high bitrate ASK signals, they are designed to operate at a fixed  $f_c$ .

In this work we use a detector based on a balanced architecture, reducing common mode noise and canceling the output fundamental harmonic, which loosens the requirements on the output filter. As a tradeoff, balanced detectors can present behaviour mismatch between the two diodes, making the matching of the ED more complex. This paper presents the experimental results of a Schottky diode based ED which demodulates up to 14 Gbit/s ASK signals, while the  $f_c$  can be selected between 78 GHz and 92 GHz.

Table 1. W-Band Envelope Detectors – State Of The Art

| Ref              | $f_c$ [GHz]  | Bitrate [Gbit/s] | Technology            | Architecture    |
|------------------|--------------|------------------|-----------------------|-----------------|
| [5]              | 101          | 26               | 35 nm mHEMT           | Balanced        |
| [6]              | 108          | 24               | 50 nm mHEMT           | n/a             |
| [7]              | 84           | 20               | 65 nm CMOS            | Single Ended    |
| [8]              | 93           | 20               | n/a                   | n/a             |
| [9]              | 80           | 12               | 65 nm CMOS            | Single          |
| [10]             | 85.5         | 10               | InP HEMT              | Single          |
| [11] (a)         | 80           | 12.5             | 65 nm CMOS            | Balanced        |
| [11] (b)         | 100          | 7.6              | 65 nm CMOS            | Balanced        |
| <b>This work</b> | <b>75–92</b> | <b>14</b>        | <b>Schottky Diode</b> | <b>Balanced</b> |

## II. CIRCUIT DESIGN AND BENCHMARKS

### A. Circuit design

The circuit tested in this paper is composed by a hollow waveguide WR-10 to microstrip transition described in [12] and an ED.

The ED's architecture combines a balun, rectifying Schottky diodes and a low pass filtering structure. The balun is based on a rat-race hybrid coupler using the high-pass compensation principle modified into a three port structure by neglecting the isolated port [13].

Figure 1 shows the schematic of the ED, which is designed using two Schottky diodes, a transmission line with an

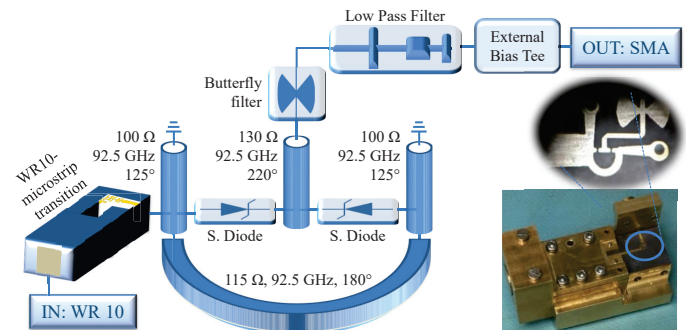


Figure 1. Schematic of the envelope detector and manufactured circuit.

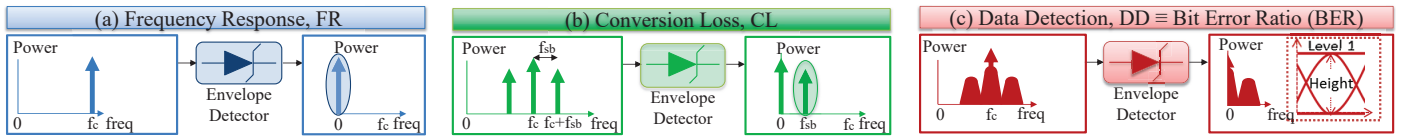


Figure 2. Benchmarks used to test the ED: (a) frequency response (FR); (b) conversion loss (CL); (c) data detection (DD).

electrical length of  $180^\circ$  at 92.5 GHz, i.e., the central frequency of the W-Band, and two shorted-stubs. A butterfly and a stepped impedance low pass filter (LPF) filters, connected to the cathode of the two diodes, reject the W-band component from the fundamental harmonic that is not cancelled through the balanced principle of the balun. An external bias tee is connected to the output of the ED in order to provide a DC path to the two diodes. The reason for choosing an external bias tee over a built-in one is to be able to experimentally measure the ED's DC output as described in subsection II-B.

The ED was fabricated in microstrip technology on a 10 mil RO5880 substrate with a  $35\ \mu\text{m}$  top copper layer. ACST GmbH provided the Schottky diodes used in this work. The ED simulations and design were conducted with Keysight's Advance Design System's (ADS) harmonic balance and transient analysis, using electromagnetic (EM) circuit simulations [14]; while the transition was designed using CST Microwave Studio simulations [12].

### B. Envelope Detector Benchmarks

The ED's performance is analysed using three different benchmark schemes depicted in figure 2: frequency response (FR), conversion loss (CL) and data detection (DD).

The FR is obtained by feeding the ED with a tone at frequency  $f_c$ , which is swept from 75 GHz to 110 GHz. The ED's DC output is measured with a voltmeter when connected to a  $50\ \Omega$  load. In this benchmark, the DC path is provided by the connection of the load to ground, therefore, the external bias tee is not needed. The CL defines the output ED's video bandwidth. As shown in figure 2, the ED is fed with a tone at  $f_{sb}$ , modulated onto a carrier at  $f_c$ .

The CL is the difference between the obtained downconverted signal at  $f_{sb}$  and the input power at  $f_c \pm f_{sb}$ . A broad FR and low CL over a large video bandwidth are needed to demodulate high data rate ASK signals without introducing distortions. Both benchmarks are calculated using harmonic balance analysis in ADS.

Finally, after confirming a broad FR and CL, we can obtain the demodulated signal's eye diagram through the DD setup shown in figure 2, where the modulating tone from the CL setup is substituted by a data signal. The external bias tee is connected to the ED output in the CL and DD cases. In ADS, a transient analysis is used in the DD benchmark.

## III. EXPERIMENTAL CHARACTERISATION

This section describes the experiments accomplished to evaluate the ED using the benchmarks described in section II-B.

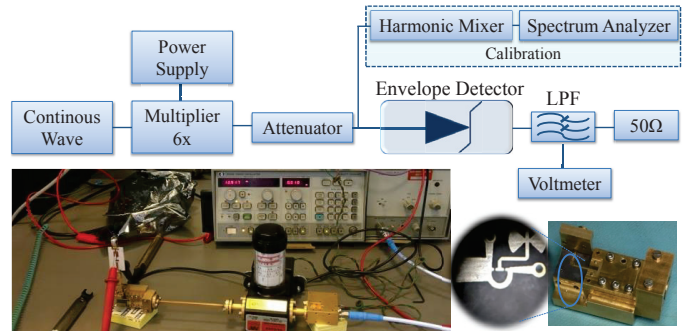


Figure 3. Experimental setup used for measuring the frequency response.

### A. Frequency Response

Figure 3 displays the setup used to measure the FR. The continuous wave (CW) signal, which provides a tone at a single frequency that is swept from 12 GHz to 18.33 GHz, was connected into the  $6\times$  multiplier to generate an output tone at W-band fed into the ED. The ED's output is connected to a  $50\ \Omega$  load through a low pass filter to be able to measure the voltage on the microstrip without damaging either the ED board (PCB) or the diodes.

The results are shown in figure 4, where the power of the ED's input signal was set to  $-6\ \text{dBm}$  and  $-10\ \text{dBm}$ . Experimental results match the simulation for both input powers up to 92.5 GHz, where the FR rolls off more abruptly in the experiment than in simulations. Nevertheless, the manufactured ED provides 20 GHz of input bandwidth within W-band.

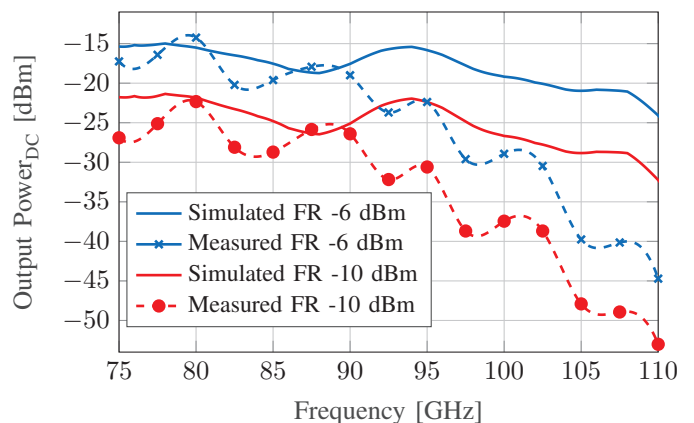


Figure 4. Frequency response results.

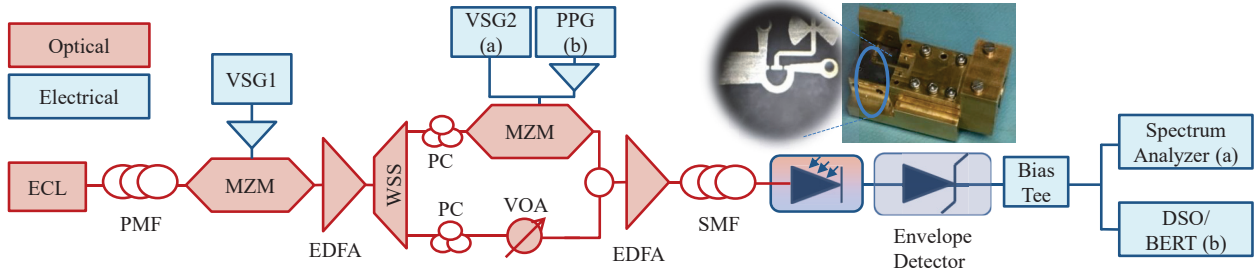


Figure 5. Experimental setup used for measuring the Conversion Loss (a) and the Data Detection (b).

### B. Conversion Loss and Data Detection Measurement Setup

Figure 5 shows the setup used to measure the CL and the DD. Two optical tones separated by a frequency distance of  $f_c$  are generated when modulating the signal from an external cavity laser (ECL) with a Mach-Zehnder modulator (MZM) biased at its minimum transmission point and driven with a tone at  $f_c/2$  from a vector signal generator (VSG). An erbium doped fiber amplifier (EDFA) boosts the two tones and a wavelength selective switch (WSS) separates them.

One of the tones is modulated with either the output of a second VSG (VSG2) in the CL benchmark, or with a non-return-to-zero (NRZ) signal in the DD at a second MZM. The NRZ signal is generated by a pulse pattern generator (PPG) based on a pseudo-random bit sequence of  $2^{31}-1$  bits (PRBS31).

At the second output of the WSS, a variable attenuator (VOA) regulates the power and polarisation of the second co-propagating tone (CT) which is recombined with the modulated optical signal through a 3 dB coupler. Then, the total signal is amplified by another EDFA before being launched into a fiber span of 2 km which is connected to a high-speed photodiode (PD) with 90 GHz of bandwidth, where the RF signal is generated by heterodyne beating.

The resulting RF signal at a carrier frequency of  $f_c$  is fed to the envelope detector (ED) and the detected envelope passes through a bias tee, removing the DC component. The baseband NRZ signal is then amplified by a power amplifier with 29 dB gain in the DD experiment. The output is recorded on the spectrum analyser in the CL benchmark or fed to a bit-error-rate tester (BERT) in the DD, to calculate the BER. As the main focus of this experiment is the characterisation of the ED in communication systems, the clock of the PPG was directly synchronised to the BERT.

### C. Conversion Loss and Data Detection Measurement Results

The results of the CL experiment and its comparison with simulations are depicted in figure 6, where figure 6a displays the CL measurements from the ED, finding a minimum CL of 11.1 dB. The ED provides a 3 dB video bandwidth up to 4 GHz. Additionally, it maintains CL values below 24 dB at video bandwidths up to 16 GHz except for  $f_{sb} = 7$  GHz and 8 GHz at  $f_c = 81$  GHz and 82 GHz.

Figure 6b further presents the difference between the simulation and experimental results. At carrier frequencies

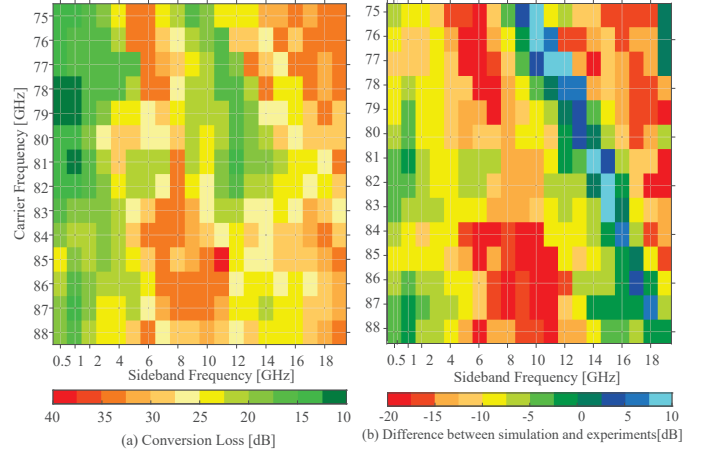


Figure 6. Conversion Loss results: (a) experimentally; (b) comparison with simulation.

below 79 GHz there is no good agreement between simulations and experiments for  $f_{sb} > 4$  GHz, as the  $f_{sb}$  quickly falls outside the W-band, and the simulation results do not provide a good estimate. At  $f_c = 80-83$  GHz the simulation and experimental results match accurately within a range between 5 to 10 dB of difference for  $f_{sb} < 8$  GHz. At higher frequencies, they match for  $f_{sb} < 5$  GHz. We consider 5 dB a good match, since it is the average difference between simulation and experimental results across all values of  $f_c$  when modulated by a signal with  $f_{sb} = 0.5$  GHz. This difference is expected to stem from the losses in the waveguide to microstrip transition or a possible misalignment of the PCB inside the block cavity, which could not be precisely measured.

To measure the DD, we substituted VSG2 with a PPG and the spectrum analyser with a BERT for real-time BER measurement. Figure 7 shows the BER versus the input power and the bitrate at carrier frequencies between 78 GHz and 92 GHz. Error free demodulation (defined as  $BER < 10^{-9}$ ) is achieved up to 12 Gbit/s for an ASK signal with  $f_c = 82$  GHz. At  $f_c = 90$  GHz and 92 GHz, the ED demodulates up to 14 Gbit/s with a BER of  $2 \cdot 10^{-5}$  and  $8.4 \cdot 10^{-7}$  respectively, i.e. below the limit of 7% overhead forward error correction (FEC) [15]. This higher video bandwidth is achieved because the ED's design frequency is at 92.5 GHz. Even if transmission is not error free, due to the lower frequency response in this frequency range (figure 4), the ED demodulates higher



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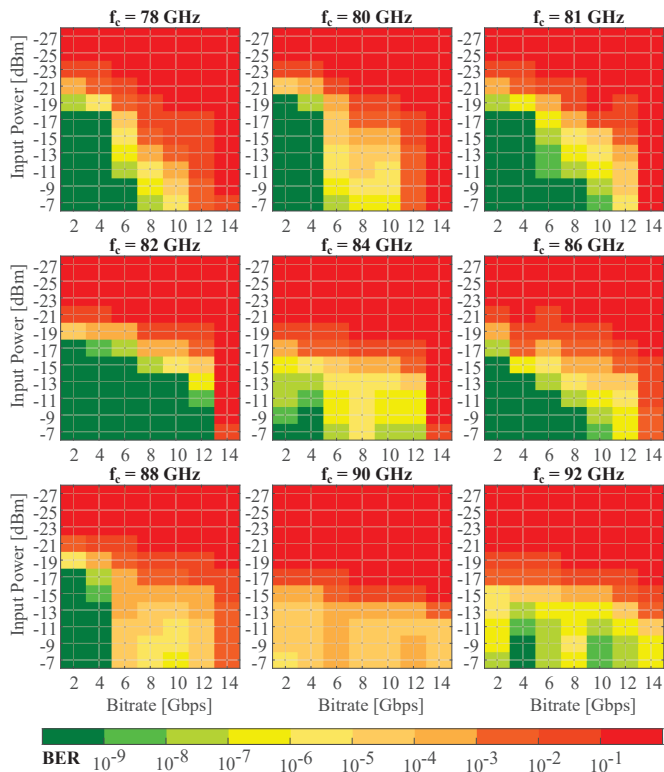


Figure 7. Experimental BER results for different carrier frequencies, data rates and input powers.

data rates at these two frequencies because it works using the balanced principle and the output fundamental harmonic is cancelled. Meanwhile, at lower carrier frequencies the ED works following a single ended architecture.

At the same time we must consider that the PD, with up to 90 GHz bandwidth, limits the experiment performance. The RF signal at its output has lower power at the upper half of the W-band, and therefore, we have not measured signals with carrier frequencies above 92 GHz. Similarly, not reaching error free at 90 GHz and 92 GHz could have been influenced by this limitation as well.

## IV. CONCLUSION

This article shows the experimental performance of a manufactured W-band Schottky diode based balanced envelope detector (ED) built in microstrip planar technology. The prototype was tested using three benchmarks, analysing its input bandwidth by measuring frequency response; its output video bandwidth by measuring conversion loss; and data transmission performance by measuring real-time BER at different carrier frequencies and data rates.

The ED provides an input bandwidth of 20 GHz within W-band and a conversion loss of 11 dB. Furthermore, the ED allows error free transmission of signals up to 12 Gbit/s on a 82 GHz carrier. Moreover, for carriers at 90 GHz to 92 GHz a BER below the limit for 7% overhead FEC for 14 Gbit/s signals was measured.