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Approaching Quantization in Macroscopic Quantum Spin Hall Devices through Gate Training

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Quantum spin Hall edge channels hold great promise as dissipationless one-dimensional conductors. However, the ideal quantized conductance of $2e^2/h$ is only found in very short channels-in contradiction with the expected protection against backscattering of the topological insulator state. In this Letter we show that enhancing the band gap does not improve quantization. When we instead alter the potential landscape by charging trap states in the gate dielectric using gate training, we approach conductance quantization for macroscopically long channels. Effectively, the scattering length increases to 175 μm, more than 1 order of magnitude longer than in previous works for HgTe-based quantum wells. Our experiments show that the distortion of the potential landscape by impurities, leading to puddle formation in the narrow gap material, is the major obstacle for observing undisturbed quantum spin Hall edge channel transport.

Over a decade ago, the quantum spin Hall (QSH) effect was found in HgTe quantum wells (QWs) [1], which have become the prototype two-dimensional topological insulator [2–7]. For QW thicknesses larger than 6.3 nm, the band structure of unstrained HgTe becomes topologically nontrivial, and a pair of counterpropagating, spin-polarized [8] channels emerge on the edge of the sample [1]. In the ideal edge mode picture, the chemical potentials of a multi-terminal device can be calculated with the Landauer-Büttiker formalism [9]. Thus, a four-probe longitudinal resistance measurement on a six-terminal Hall bar device yields a quantized conductance of $2e^2/h$.

This value, however, is only observed for channels of a few μm length [1]. For longer channels, the observed conductance drops considerably. This is a fundamental puzzle in the field, and a serious problem for potential device applications that require fully transmitting channels. Various explanations for the reduced conductance are discussed in literature [10–21]. Scattering on small charged islands (puddles) [17,20,21] captures best the observed weak temperature dependence [1,5], and is supported by scanning-gate measurements [22]. In devices of the narrow-gap system HgTe, such puddles form mainly due to charged defects at the semiconductor-insulator interface and within the polycrystalline insulator itself. The charge state of the defects determines the potential landscape.

A schematic sketch of the potential landscape along the edge of a device is given in Fig. 1(a). It is obvious that the edge channel conductance can be improved by increasing the band gap (right figure) or by flattening the potential landscape (left figure). In both cases the distance between areas where backscattering may be possible increases
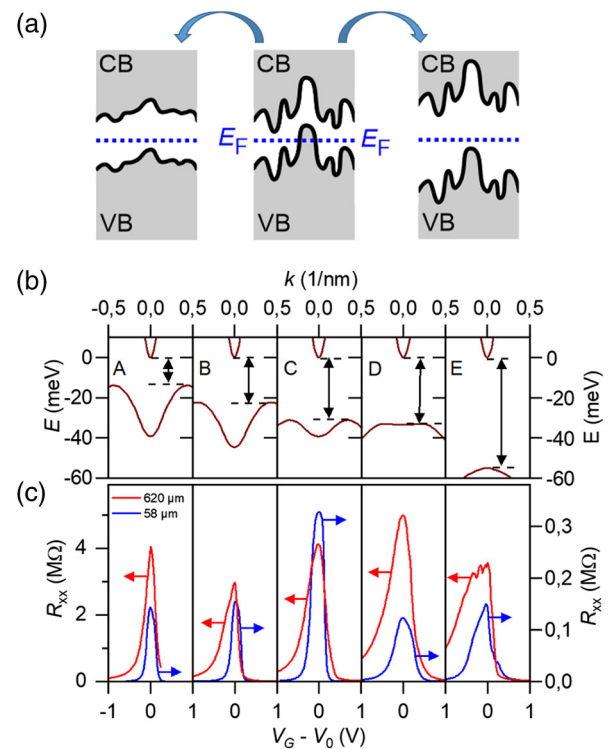
FIG. 1. (a) Schematic sketch of the potential landscape along the edge channel for small (left) and large fluctuations (center), and an enlarged band gap (right). CB and VB denote the conduction and valence band, respectively. (b) Calculated band dispersions around the Γ point of samples A through E. The arrow indicates the band gaps. (c) Longitudinal resistance as a function of the gate voltage for samples A through E for large (red, $l_{\text{edge}} = 620$ μm) and small devices (blue, $l_{\text{edge}} = 58$ μm) at $T \approx 2$ K. The gate voltages V_G are shifted by V_0 corresponding to the resistance maximum.

TABLE I. Sample parameters. Indicating the insulator (d_{ins}), top barrier (d_b), and quantum well thickness (d_{QW}), the deduced strain ($\varepsilon < 0$: tensile; $\varepsilon > 0$: compressive), and the related band gap (E_G). The last column gives the composition of the top barrier.

	d_{ins} (nm)	d_b (nm)	d_{QW} (nm)	ε (%)	E_G (meV)	Barrier material
A	110	17	8.8	−0.2	14	$Hg_{0.3}Cd_{0.7}Te$
B	110	17	8.4	0.0	21	$Hg_{0.3}Cd_{0.7}Te$
C	110	17	9.0	0.4	31	$Hg_{0.3}Cd_{0.7}Te$
D	110	16	9.8	0.6	33	$Hg_{0.3}Cd_{0.7}Te$
E	110	18	7.5	1.4	55	$Hg_{0.3}Cd_{0.41}Zn_{0.29}Te$
F	110	140	8.0	0.5	37	$Hg_{0.3}Cd_{0.57}Zn_{0.13}Te$

effectively. We study both mechanisms experimentally and find that for HgTe quantum well structures the flattening of the potential landscape provides a successful approach to achieve quantized conductance even in macroscopically large devices.

First, we investigate the influence of the band gap size on the QSH conductance. Väyrynen *et al.* [17,20] predict an exponential decay of scattering from charge islands with increasing band gap and consequently a channel conductance that approaches the expected quantized value. We study this dependence on a set of five QWs A to E with band gaps ranging from 14 to 55 meV, respectively. The QW thicknesses vary between 7.5 and 9.8 nm. A variation of the band gap is achieved by growing the HgTe QW layer on substrates with different lateral lattice constant imposing either tensile or compressive strain. The strain level is determined by high resolution x-ray diffraction. This method of band gap engineering is explained in more detail in Ref. [23]. Each QW exhibits a $Cd_{0.7}Hg_{0.3}Te$ top barrier of 16 to 18 nm. The relevant sample parameters are summarized in Table I.

For transport experiments, the samples are lithographically structured into six-terminal Hall bar devices equipped with a gold top gate. The top gate is separated from the semiconductor by a 110 nm thick amorphous SiO_2/Si_3N_4 alternating multilayer stack of five periods. Figure 1(b) shows the band dispersion for the samples A through E obtained from an eight band $k \cdot p$ calculation for all samples [24]. The size of the gap is confirmed experimentally by temperature activated transport measurements (cf. Supplemental Material Fig. S1 [25]).

For each sample we investigate two devices with different distances between two neighboring voltage probes. The effective edge channel length l_{edge} between those contacts is either 620 or 58 μm. For the transport characterization we perform four-terminal measurements at 2 K using standard ac techniques.

The gate-dependent longitudinal resistance is shown in Fig. 1(c) for each sample comparing the two device sizes. Note that for easier comparison the gate voltages V_G are
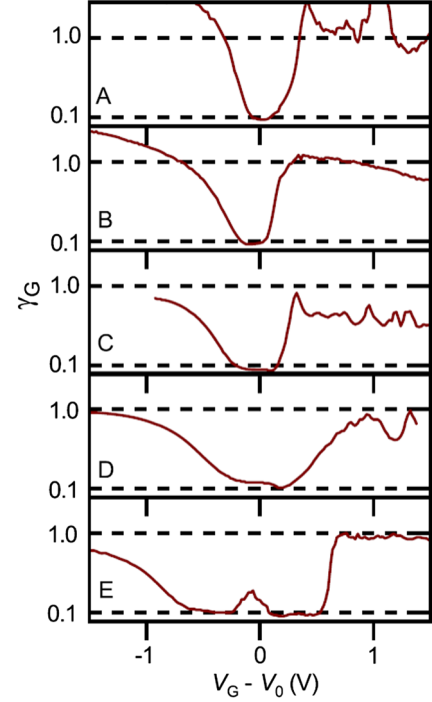

FIG. 2. Resistance ratio $\gamma_G = R_{xx58}/R_{xx620}$ as a function of gate voltage. Dashed lines indicate ideal values for pure sheet conductance ($\gamma_G = 1$) and pure edge conductance ($\gamma_G = 0.1$).

listed with respect to the voltage V_0 where the resistance exhibits a maximum. This maximum characterizes the transition regime between n-type and p-type conductance for positive and negative V_G, respectively.

From the measurement of the longitudinal resistance [Fig. 1(c)] it is not possible to draw any conclusion on the effect of an increased band gap on the conductance inside the band gap. The variations of maximum value in R_{xx} are random and independent of the gap size. Thus, we conclude that an increase of the band gap is not a determining factor for the scattering length in our devices.

Even though the conductance in the devices of Fig. 1 is much smaller than the expected conductance quantum, one can still make an argument that the current is carried by the edge states. Evidence can be found from comparing the resistance ratio, $\gamma_G = R_{xx58}/R_{xx620}$, between small and large device for each sample. Since the aspect ratio of length to width ($l/w = 3$) is the same for both device sizes, the resistance ratio would yield $\gamma_G = 1$ if the current is carried solely by bulk modes. However, if one expects an edge mode conductance where the existence of charge puddles introduces an Ohmic behavior, the channel length would determine γ_G, which yields an approximately 10 times lower value: $\gamma_G \approx 58/620 \approx 0.1$. In Fig. 2 γ_G is plotted for all samples ($A \ldots E$). One can clearly distinguish two regimes: First, the bulk conducting regime for large positive and negative V_G where γ_G ranges around unity, and second, the band gap regime where γ_G approaches 0.1, indicating a one-dimensional Ohmic behavior. Note that the

gate voltage region where $\gamma_G = 0.1$ represents the regime where edge channel transport dominates over bulk transport which not necessarily implies that the Fermi energy is located within the band gap over the entire voltage range.

Another approach to improve the edge channel conductance is to modify the potential landscape. In a study on hysteretic effects in gate-dependent transport experiments we have previously established that in our devices surface defects and the polycrystalline insulator layer are the source for charge trap states in the vicinity of the semiconductor-insulator interface [26]. As soon as V_G exceeds a certain threshold, for positive or negative gate voltage, charges may tunnel from or into the QW and charge or discharge these trap states, respectively, which modifies the effective screening and thus the electrostatic potential landscape. The charging effect is hysteretic and determines the dependence of n on V_G. We now use this memory effect to perform a controlled gate training to achieve an optimally homogeneous electrostatic potential landscape. In order to enhance the potential smoothening we use sample F, which has a thick top barrier (140 nm). A thick barrier moves the charged trap states further away from the QW, but should still allow for sufficient gating. Note that in order to avoid strain relaxation in the HgTe QW due to the thick top barrier layer, Zn was added to reduce the strain (cf. Table I). For comparison, we perform the same gate training on sample D with a much thinner HgCdZnTe top barrier (16 nm). For sample F, we additionally fabricated a microstructured Hall bar with a 13 μm channel length between neighboring voltage probes, a device size which is still larger than the largest so far where we observed quantized edge channel conductance [27]. Note that for the devices in Ref. [27] a special wet-etching technique was applied to achieve to reduce the potential roughness in the vicinity of the edge channels.

The gate training consists of the following procedure: Starting at zero gate voltage, V_G is increased up to a certain negative voltage V_{max} and then decreased back to zero. During both V_G sweeps, the longitudinal resistance of the sample is monitored. This step is then repeated, scanning to a slightly more negative V_{max}. A sequence of resistance traces obtained in this manner is shown for three device sizes of sample F in Fig. 3. The figure shows R_{xx} separated into the two sweep directions, zero to negative V_{max} in the left and the reverse direction in the right panel. The maximum negative V_{max} for each sequence step is indicated by a colored bar.

The measurement shows that there is a minimum in the sequence of resistance maxima for each sweep direction (indicated by a black dot in Fig. 3). Because of charging and discharging of charge puddles the traces for both sweep directions differ from each other. For our samples we find that a sweep back to zero exhibits the lowest values for R_{max}, i.e., values that are closest to the expected $h/2e^2$. In Fig. 4(a) we plot the minimum conductance values

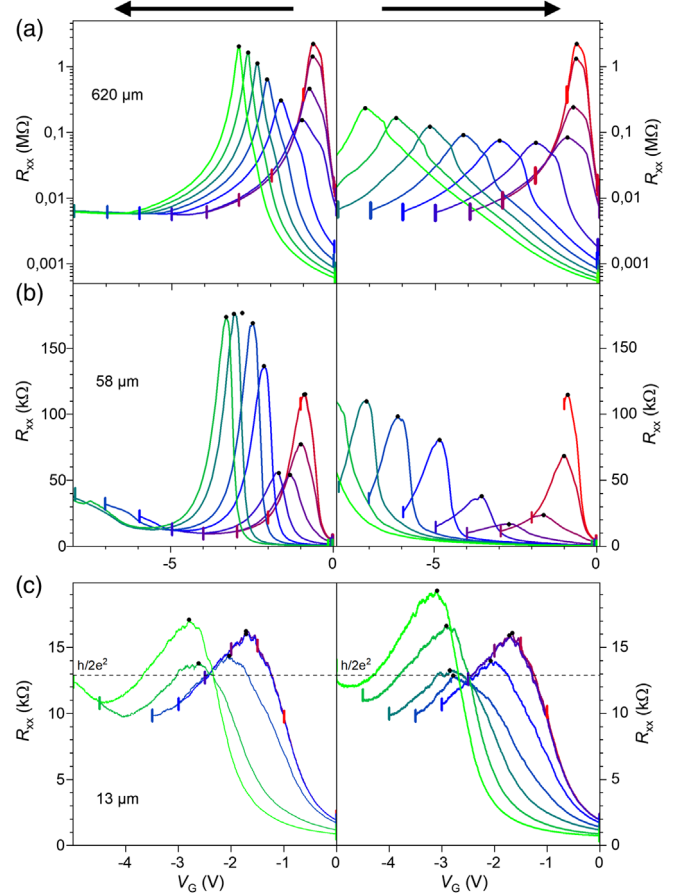FIG. 3. Gate training. Longitudinal resistance R_{xx} as a function of gate voltage at $T = 2$ K for (a) the large device ($l_{edge} = 620$ μm), (b) the small ($l_{edge} = 58$ μm), and (c) the microdevice ($l_{edge} = 13$ μm). The left and right panel represent different sweep directions, from zero to V_{max} (indicated by a colored bar) and V_{max} back to zero, respectively. Black dots mark the resistance maximum for each training sequence.

$G_{min} = 1/R_{max}$ as a function of the V_{max} value for which they were obtained.

For the large device the minimum conductance reaches a value of approximately 0.4 e^2/h at $V_{max} = -5$ V after optimal training, which is the largest observed so far for such a large device. The training effect is even more apparent for smaller devices. The conductance for the 58 μm device reaches 80% off of the expected conductance value, and training establishes successfully the expected quantized minimum conductance for the smallest device. We have repeated the gate training for different cooling cycles and find that the minimum conductance reproduces very well [open and closed dots in Fig. 4(a)]. All together, these results indicate that with a controlled gate training an optimized potential landscape can be established, which minimizes the scattering probability along an edge channel. Further charging again roughens the potential.

Increasing the thickness of the top barrier turns out to be essential for effective gate training. In Fig. 4(a) we also
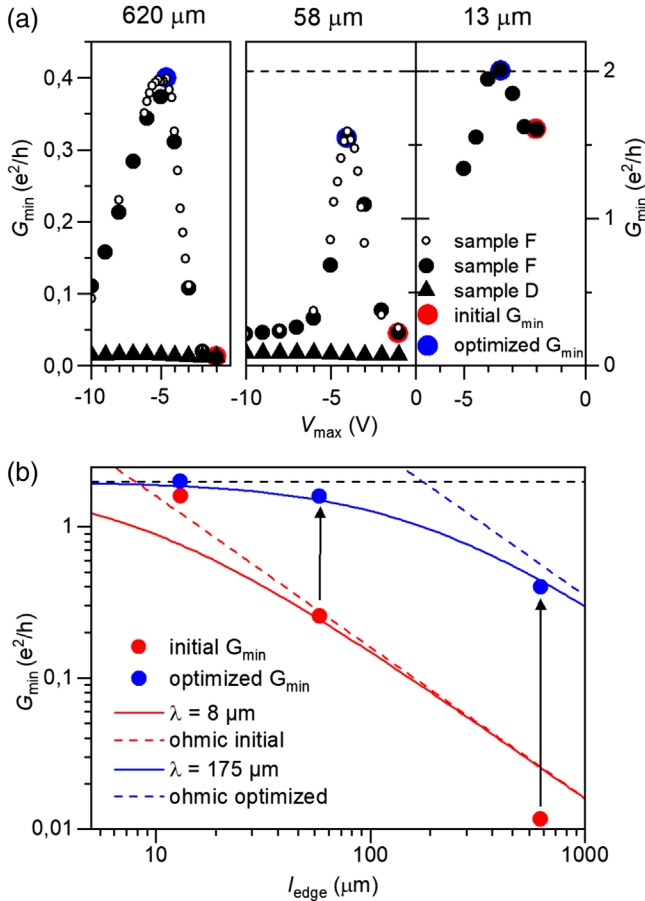
FIG. 4. (a) Minimum conductance values of the corresponding maximum resistance (dots in Fig. 3) as a function of V_{max} for all three channel lengths. Open and closed dots represent sample F and triangles sample D. Open dots are obtained from a second cool-down. The dashed line marks the expected quantized conductance value of $2e^2/h$. (b) shows the conductance closest to the expected value of $2e^2/h$ as a function of channel length for initial (red) and optimized (blue) minimum conductance (extracted from (a)). The solid line corresponds to a fit of the average scattering length within the edge channel, which yields $\lambda = 8$ (red) and 175 μm (blue). The dashed line represents the Ohmic behavior with $G_{min} \propto 1/l_{edge}$.

show gate training results for sample D which has a thin (16 nm) top barrier. Even though the charging effect is observable for both devices (cf. the plot of the same data on a smaller scale in Fig. S2 of the Supplemental Material [25]), the effect is hardly recognizable for sample D on the presented scale. We conclude that the close vicinity of individual trap states to the QW influences the roughness of the potential landscape significantly and makes gate training much less efficient.

We now use the results of the gate training to estimate the average distance between charge puddles which lead to backscattering. We consider an edge channel as a perfectly conducting one-dimensional channel, which is intersected by charge puddles responsible for backscattering. Thus, we

express the edge channel resistance as $R_{edge} = h/e^2(1 + l_{edge}/\lambda)$, where λ is the average distance between two fully dephasing scattering events. For small λ, the resistance is proportional to l_{edge} (Ohmic), while, when λ exceeds the device size, the channel resistance saturates at h/e^2 (non-Ohmic).

In Fig. 4(b) we plot the observed minimal conductance as a function of channel length before (red dots) and after gate training (blue dots). To extract λ, we fit these data points using the above expression [$G = 1/R = 2/R_{edge} = 2e^2/h(1 + l_{edge}/\lambda)^{-1}$]. The red line, fitted to the initial minimum conductance (red dots), yields an average puddle distance of $\lambda \approx 8$ μm while after training λ increases to 175 μm (fit parameter for the blue line, optimized minimum conductance), with an error of ± 25 μm, determined by the accuracy of the fitting. For small λ, the data points can still be well represented by an Ohmic behavior (dashed red line). However, as λ exceeds the device size, saturation to the expected quantized value becomes apparent, an observation which additionally demonstrates the occurrence of dominant edge channel transport. Our data points are in good agreement with our trial function, which indicates that our assumptions are reasonable. We interpret the cutoff of the blue dashed line at 175 μm as reflecting the intrinsic crystalline quality which limits the device size for the observation of quantized edge channel conductance.

In comparison, recent work on the large-gap material WTe$_2$ [28] finds saturation to $2e^2/h$ only for channels of a few hundred nm, which gives rise to a λ only of about 500 nm. This again demonstrates that even for materials with a large band gap (WTe$_2$: 100 meV) potential fluctuations are the dominant factor that limits the conductance quantization.

In conclusion, we have achieved optimized edge channel conductance for HgTe QW structures by controlled gate training. With this technique the long awaited use of quantized helical edge channel transport becomes feasible in macroscopic devices. Additionally, these results demonstrate the evidence for puddles as the major obstacle for the observation of quantized conductance in topologically protected helical edge channels.

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