

Low-power BPSK inductive data link for an implanted intracortical visual prosthesis

Citation for published version (APA):

Omisakin, A., Mestrom, R., & Bentum, M. (2019). Low-power BPSK inductive data link for an implanted intracortical visual prosthesis. In *2019 41st Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBC 2019* Article 8857225 Institute of Electrical and Electronics Engineers. <https://doi.org/10.1109/EMBC.2019.8857225>

DOI:

[10.1109/EMBC.2019.8857225](https://doi.org/10.1109/EMBC.2019.8857225)

Document status and date:

Published: 07/10/2019

Document Version:

Accepted manuscript including changes made at the peer-review stage

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

Low-Power BPSK Inductive Data Link for an Implanted Intracortical Visual Prosthesis

Adedayo Omisakin, Rob Mestrom, and Mark Bentum

Abstract—In making visually impaired people see again, for most cases the only option is to stimulate the visual cortex. In building such a system, it is desired that the communication to/from the implant and powering be done wirelessly to avoid infections. For the downlink, which is sending stimulation data to the implanted electrode, bandpass-sampled binary phase shift keying (BPSK) is chosen due to its potential for low-power consumption at its digital receiver. However, since an inductive link is most suited, designing practical inductive links with a flat band region to avoid poor phase transition and also refining the reset timing for imperfect transition times as well as designing low-power custom 1-bit Analog-to-digital converter is crucial. The bandpass-sampled BPSK system is designed and simulated at circuit level in Cadence using 180 nm CMOS technology at data rates of 0.5-4 Mbps and carrier frequency of 5-12 MHz. The improved bandpass-sampled BPSK system meets the requirements on data-rate, low-power consumption and robustness and is an integral part of the overall wireless communication and powering of the implanted intracortical visual prosthesis.

I. INTRODUCTION

Roughly 0.5% of the world population is visually impaired [1]. For nearly 90% of visual impairment, the only option is to stimulate the visual cortex directly. Building such a system, requires a camera, advanced image processing, and thousands of electrodes stimulating the visual cortex. It is essential communication to and from the implanted electrode array be done wirelessly to avoid infections and to enable free body movement. Therefore, an uplink communication system for reading the brain and downlink system for writing the brain is needed. The selected system layout is shown in Figure 1. The implanted transceiver is placed between the skull and the skin. This layout has more safe space and a relatively shorter distance for the signal to propagate through as compared to when the implanted transceiver is placed beneath the skull. This work focuses on the low-power system design at an integrated circuit-level of the downlink system, which is the link for sending the stimulation data from the external transmitter to the implanted receiver. Since the receiver side will be implanted, it needs to be low-power due to battery constraints. The implanted system will be powered wirelessly, and research work is on-going on that but it will not be addressed in this paper.

* This research is supported by the Dutch Technology Foundation STW, which is part of the Netherlands Organization for Scientific Research (NWO), project 5 of the NESTOR program (P15-42)

Adedayo Omisakin, Rob Mestrom and Mark Bentum are with the Department of Electrical Engineering, Eindhoven University of Technology, Eindhoven, The Netherlands. (e-mail [a.e.omisakin, r.m.c.mestrom, m.j.bentum]@tue.nl)

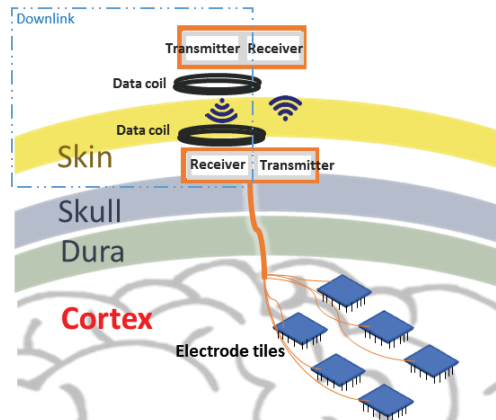


Fig. 1. An illustration of the system layout for wireless communication in the visual prosthesis.

For low-power consumption at the receiver, in [2], [3] bandpass-sampled binary phase shift keying (BPSK) is proposed. This is because its demodulator uses digital components. This fits the overall goal of low-power consumption and data rate required for the visual prosthesis [4]. However, to further enhance its robustness to errors, we propose the following three novelties to in the system. 1) Designing a practical inductive link with a flat band to improve sharp phase transition in the received BPSK signal for robust demodulation by the digital receiver. 2) Building a low power analog-to-digital front end for the digital receiver by deriving its clock from the digital demodulator. 3) Fine-tuning the reset timing region to ensure robust signal demodulation.

In this work, the transmitter, the inductive link and the receiver are designed and simulated (see Figure 2 for system block diagram). A low-power front end 1-bit analog to digital converter (ADC) in the digital receiver that derives its clock from the digital demodulator is presented. A practical guide in designing a nearly flat band for the communication through the inductive link which improves the phase transition in the received signal is discussed. The counter of the digital demodulator is raised to count up to 7 compared to the count of up to 4 in reported literature [2], [3], ensuring fine range on the reset timing signal to improve robustness. The overall downlink system is designed at integrated circuit level in Cadence simulator using 180 nm CMOS technology, demonstrating low power consumption and robustness at data rates of 0.5-4 Mbps and carrier frequency of 5-12 MHz (0-5 MHz is used for wireless power transfer). The remainder of the paper is organized as follows. Section II describes the

circuit design of the individual system blocks. In Section III, distinguishing system aspects are covered, including the idea of using a higher count for a more precise range of timing, and efficient use of clock signals. Section IV presents the simulation results and describes variable data rate depending on the skin depth at 5 mm and 10 mm. The implanted receiver is robust to imperfect transition errors while keeping its power consumption below 1 mW.

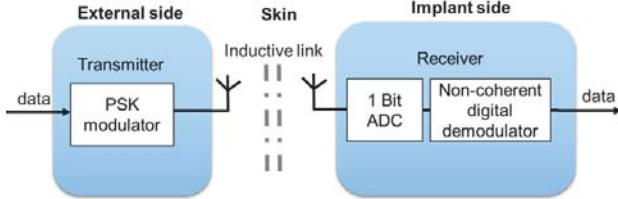


Fig. 2. Bandpass-sampled BPSK system block diagram.

II. SYSTEM BLOCKS

A. Transmitter

The transmitter comprises of the oscillator and the mixer. The BPSK mixer designed is shown in Figure 3. It is similar to the reported mixer in [5], except that a resistor and a common mode feedback structure is not used to convert the transconductance current to a voltage level. Two inverters act as switch pairs, switching between signal paths to generate the BPSK signal as currents. The BPSK currents are passed directly to the inductive link because this essentially transfers the current on one side to the other side by the coupling factor. The subsystem is simulated in the data rate range of 0.5-4 Mbps and carrier frequency in the range of 5-12 MHz.

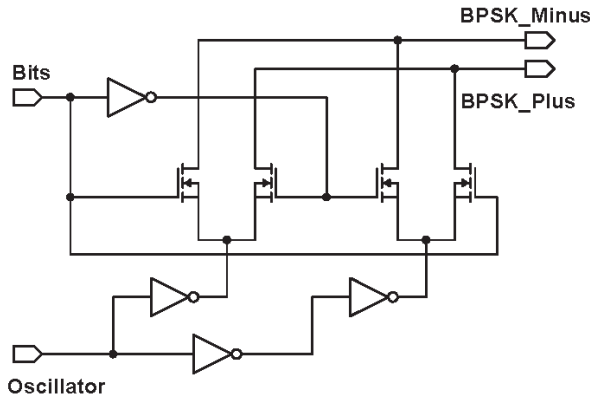


Fig. 3. Circuit schematic of the BPSK mixer.

B. Receiver

The implanted receiver comprises of a 1-bit ADC and the digital demodulator.

1) *The 1-bit Analog-to-Digital converter:* The received signal voltage level is expected to be in the range of 0.5 - 3 V. This may sometimes be lower than the digital logic level of the digital receiver, for example, if 1.8 V is used.

Traditionally, low noise amplifiers are usually used as the first stage of receivers, but they consume several milliwatts of power. Instead, a dynamic latch comparator is proposed, which consumes well below a milliwatt at low frequencies on the order of 10 MHz [6]. Dynamic latch comparators can have an offset voltage of hundreds of millivolts, so to keep the offset voltage low [7], a Lewis-Gray comparator is used [8]. This has a fair balance between complexity and power consumption. After the Lewis-Gray comparator, a single-ended output differential pair is used to convert the output of the 1 bit ADC to single-ended. Next, a D-flip-flop is used to derive the digital output from its clock and output signal. However, the clock is first delayed before entering the D-flip-flop to ensure proper alignment. Figure 4 shows the circuit schematic of the 1 bit ADC.

2) *The digital demodulator:* The digital demodulator comprises mainly of an edge detector and a reset generator to reset the edge detector before the next symbol. The edge detector consists of a rising edge and falling edge flip-flop. With an AND and OR logic gate, the type of edge and when the edge occurred is derived. Through a D-flip-flop, the sent bits are recovered from the edge type and edge detected. The detected edge is delayed to ensure alignment before entering the recovery D- flip-flop. Figure 5 shows the circuit schematic of the digital demodulator. Theoretically, the reset generator must reset at a time after present edge detection $t = 0$, between $t = T_{PSK}$ and $t = 0.5T_{PSK}$. Where T_{PSK} is the period of the carrier frequency. With a count up number N , the range of clock frequency is given by

$$Nf_{PSK} < f_{OSC} < 2(N-1)f_{PSK}, \quad (1)$$

where f_{PSK} is the carrier frequency and f_{osc} is the oscillator frequency. A practical reset timing constraint will be discussed in Section III.

C. Inductive link design

The desired data rate is in the range of 0.5-4 Mbps for the visual prosthesis. Since the communication range from beneath the skin to above the skin is below 10 mm [9], an inductive link is the most suited type of link. To keep power consumption low, the carrier frequency is chosen to be below 20 MHz. Squeezing out bandwidth for the desired data rate can be challenging, especially in inductive links. This is generally attempted by greatly reducing the quality factor of the coil which leads to more power dissipation [10]. The transition region of the PSK modulated signal can be distorted if the transmission in the pass-band of the inductive system is not flat enough. However, a practical guide for creating a flat band without lowering the quality factor of the coils is presented next.

Creating a flat band region can be done by making both the transmit and receive coil resonate at the same frequency. When two coils resonate at the same frequency, the resulting coupled response gives two resonance peaks away from the resonance frequency of the individual coils, thereby creating a 'well' between peaks. This well has a relatively flat pass-band to fit the data rate bandwidth. Extensive treatment of

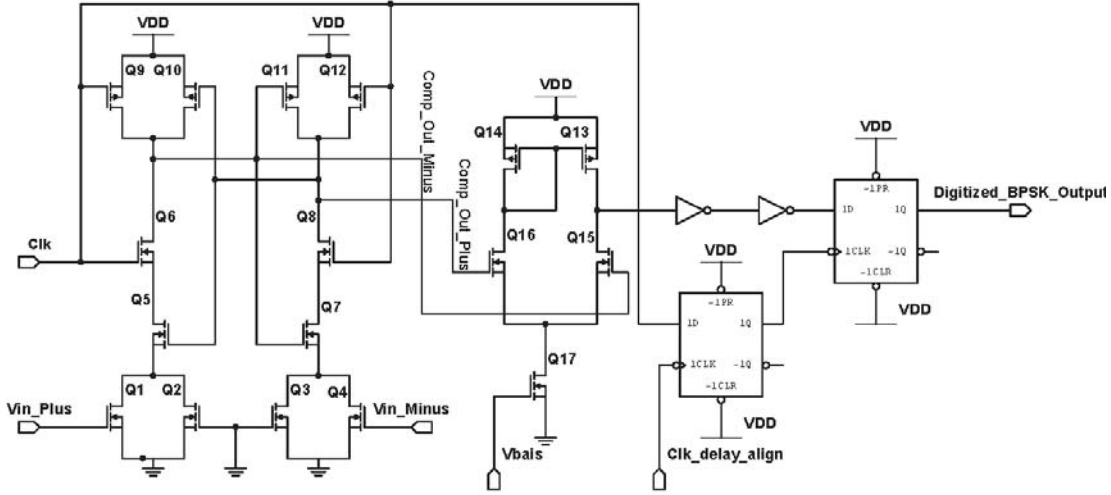


Fig. 4. Circuit schematic of the 1-bit-ADC.

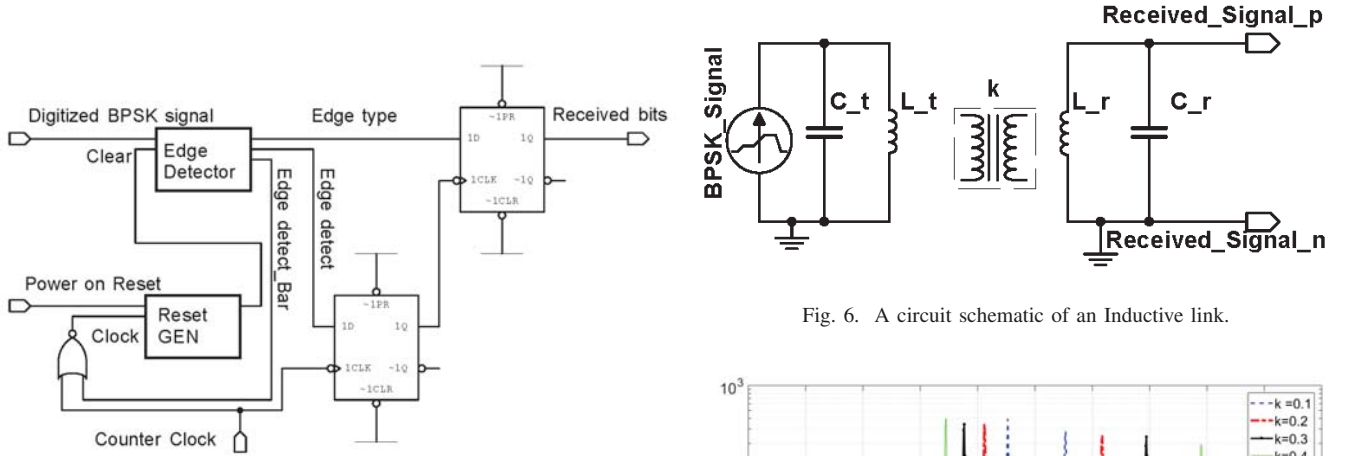


Fig. 5. Circuit schematic of digital demodulator.

this phenomena is found in [11], and is observed to occur if the coupling factor is high enough. If the inductance is high enough (tens of microhenries) and the coupling factor is in range of 0.1-0.4, with the carrier frequency range of 0.1-30 MHz, and coil-resistances in the order of a few ohms, the frequency gap between both peaks is linearized and empirically given by:

$$\Delta f_{peak2-peak1} \sim k f_{res}, \quad (2)$$

where k is the coupling factor between coils and f_{res} is the resonance of one side uncoupled. For example, for a k -factor of 0.3, which is feasible at 5 mm separation distance [12], it follows that at 10 MHz, a flat band of 3 MHz is available. Figure 6 and 7 show the circuit schematic and frequency response of two coils of 27 μ H and the resonance frequency of 10 MHz at various k -factor values, respectively. From Figure 7, it is seen that the frequency separation (flat band) is roughly proportional to the k -factor with the constraints mentioned previously.

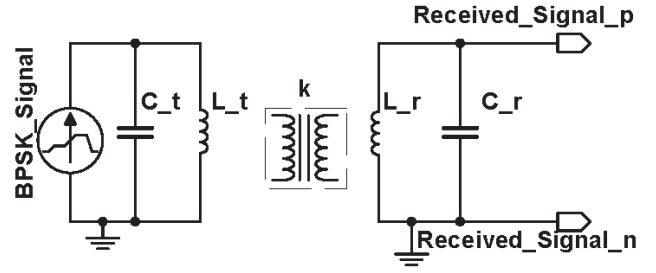


Fig. 6. A circuit schematic of an Inductive link.

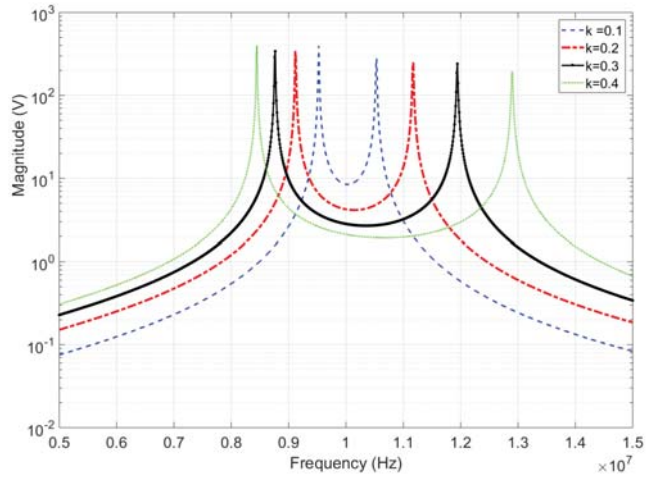


Fig. 7. Varying k for two coils of the same resonance.

III. SYSTEM ASPECTS

A. Timing of the reset signal

Theoretically, the reset time t should be between $0.5T_{PSK} < t < T_{PSK}$ to ensure that no two successive symbols are detected as a phase change. A count-up number N of 4 was used in [2], but however, in the presence of realistic inductive links, the phase transition is sometimes

not instantaneous as it drags before phase reversal. Figure 8 illustrates this. Therefore, a finer range of timing is required, for example $0.65T_{PSK} < t < 0.8T_{PSK}$. This results in a more general form of (1):

$$\frac{N}{c_{upper}} f_{PSK} < f_{OSC} < \frac{N-1}{c_{lower}} f_{PSK}, \quad (3)$$

where c_{upper} and c_{lower} are the set limits on the reset timing. From (3), it is observed that a higher count up number N is needed if the range is to be made finer. For example, the commonly used $N = 4$ in [2], [3] does not satisfy the equation for $0.65T_{PSK} < t < 0.8T_{PSK}$, but $N = 7$ does. This fine-tuning of reset timing will allow the reset timing not to occur in the imperfect transition area, giving more robustness to errors.

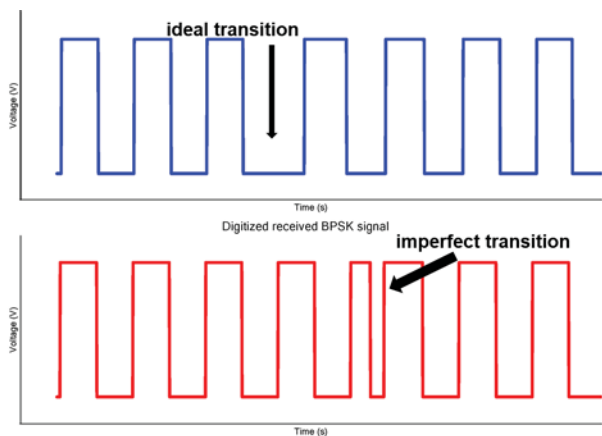


Fig. 8. Illustrating an imperfect transition on the digitized received BPSK signal due to the inductive link. (a) ideal transition. (b) imperfect transition.

B. Efficient use of clocks

For the designed implanted receiver, 4 clocks are needed: 1) The clock for the comparator f_{comp} 2) Clock for delay to align signals in the comparator $f_{comp-align}$ 3) Clock for the reset generator $f_{counter}$ 4) Clock for delay to align signal in the digital demodulator $f_{signal-align}$. It would be area-efficient to minimize the number of independent clocks used. This would also reduce power consumption. The constraints on the 4 clock frequencies are as follows: $f_{comp} > 2f_{PSK}$ for proper sampling at the comparator, $f_{comp-align} > 2f_{comp} = 4f_{PSK}$ to avoid overdelay when delaying the comparator clock during alignment, $f_{counter} > (5-30)f_{PSK}$ is a typical range of clock frequency of the reset generator counter, and $f_{signal-align} > 2f_{PSK}$ to avoid overdelay when delaying the edge detect signal during alignment.

This follows that $f_{counter} > 6f_{PSK}$ or multiples above can be used to drive $f_{signal-align}$ and f_{comp} and multiplying the frequency by 2 to drive $f_{comp-align}$. Figure 9 shows a block diagram of the receiver with the clock sharing. For example, if $c_{upper} = 0.8$ and $c_{lower} = 0.65$ at $N = 7$, using (3), the resulting constraint is $8.8f_{PSK} < f_{counter} < 9.2f_{PSK}$. This means that if $f_{comp-align} = 18f_{PSK}$ is taken and $f_{signal-align} = f_{counter} = f_{comp} = 9f_{PSK}$, the system

uses only one clock fed to $f_{comp-align}$, divided by 2 and then fed as the rest 3 remaining clocks required.

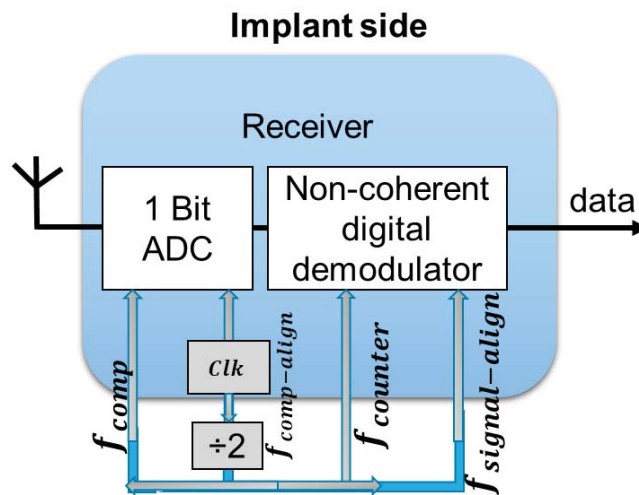


Fig. 9. Efficient use of clocks.

TABLE I
CIRCUIT PARAMETERS OF THE WIRELESS LINK.

Parameters	Value	Comment
f_{psk}	12 MHz	Carrier frequency
r_{bit}	3,4 Mbps	Data rate
L_t	27 μ H	Transmit Coil Inductance
L_r	27 μ H	Receive Coil Inductance
C_t	6.5 pF	Transmit Parallel capacitor
C_r	6.5 pF	Receiver Parallel capacitor
c_{osc}	9	$f_{counter}$ - factor of f_{psk}

IV. RESULTS AND DISCUSSION

The entire system described in Section II and III, which is the novel BPSK inductive link system, is simulated in Cadence using 180 nm CMOS technology at 1.8 V supply voltage. Table I shows the key parameters of the simulation. The skin is usually about 5 mm thick [9]. Therefore the target coil separation distance is 5 mm, and it is extended to a coil separation distance of 10 mm for extreme cases. Coils of 30-40 mm diameter are physically compatible with the system as it is not too bulky. At this coil diameter, an inductance of a few tens of μ H is feasible with ferrite backing. In an electromagnetic simulation of coils using CST Microwave Studio, the coupling factor is determined which is used in subsequent circuit simulations in Cadence. At 10 mm coil distance, a coupling factor of about 0.3 was reached, and at 5 mm a coupling factor of about 0.5 was reached.

When the system is simulated at a carrier frequency of 12 MHz, a data rate of 4 Mbps was achieved at $k = 0.5$ but not at $k = 0.3$. However, when the data rate was lowered to 3 Mbps, it was successful at $k = 0.3$. The failure of 4 Mbps at $k = 0.3$ agrees well with empirical bandwidth calculation $0.3 \times 12 = 3.6$ MHz (see (2)). In that case, there was insufficient flat bandwidth. The trend of the simulation follows that with a data-to-carrier ratio of 1/3 the coupling

factor needs to be higher than $k = 0.3$ for more bandwidth. Furthermore, with a data-to-carrier ratio of 1/4 with $k = 0.3$, the system is successful.

On CMOS 180 nm technology, a supply voltage of 1.8 V, $f_{counter} = 9f_{PSK}$, a carrier frequency of 12 MHz, and a data rate of 4 Mbps, Cadence simulations show that the 1-bit ADC consumed 0.26 mW, the digital demodulator consumed 0.14 mW while the ring oscillator and frequency-divider for clock generation and distribution consumed 0.55 mW. The overall receiver thus consumes 0.95 mW. This power consumption can be much lower with a smaller CMOS technology such as CMOS 65 nm technology and optimised clock generation and distribution.

Comparing the system with state of the art links is not straightforward due to incomplete system reportings in literature and due to reported solutions being very specific for applications. However, it remains below 1 mW compared to other systems that used analog techniques reported in [13] and [14] which consumed above 5 mW at achieving 2 and 4 Mbps, respectively.

V. CONCLUSION & FUTURE WORK

A bandpass-sampled BPSK inductive link system is designed and simulated at an integrated circuit level. The implanted receiver remains below 1 mW power consumption while using a low-power 1-bit ADC which features a dynamic comparator instead of power-hungry amplifiers. A guide to designing inductive links which have a relatively flat pass-band region to fit the data rate bandwidth was discussed. This improved the phase transition of the received modulated signal without lowering the quality factor of the coils, which leads to increased power dissipation. The count-up number of the reset generator in the digital demodulator was increased to 7 to enable fine-tuning of the reset constraints to avoid resetting at imperfect transition regions. The overall system at 12 MHz could work successfully with a data rate of 4 Mbps (data-to-carrier ratio of 1/3) at a coil separation of 5 mm which corresponds to $k \sim 0.5$, and at 10 mm with a data rate of 3 Mbps (data-to-carrier ratio of 1/4) while consuming 0.4 mW at implanted receiver (excluding the clock generator). The system is scalable in frequency although the self-resonant frequency of the coils poses a constraint.

The next step is to build a demonstrator, and later on, develop the design further for IC manufacturing and experimental verification. The overall system meets the specifications

of the downlink system which sends stimulation data to the implanted electrode which is an integral part of the wireless enabled visual prosthesis.

ACKNOWLEDGEMENT

This research is supported by the Dutch Technology Foundation STW, which is part of the Netherlands Organization for Scientific Research (NWO), project 5 of the NESTOR program (P15-42).

REFERENCES

- [1] D. Pascolini and S. P. Mariotti, "Global estimates of visual impairment: 2010," *British Journal of Ophthalmology*, vol. 96, no. 5, pp. 614–618, 2012. [Online]. Available: <http://bjo.bmj.com/content/96/5/614>
- [2] F. Asgarian and A. M. Sodagar, "A high-data-rate low-power BPSK demodulator and clock recovery circuit for implantable biomedical devices," in *2009 4th International IEEE/EMBS Conference on Neural Engineering*, apr 2009, pp. 407–410.
- [3] A. Ghenim, D. Daoud, M. Ghorbel, A. B. Hamida, and J. Tomas, "A dual band wireless power and DPSK data telemetry for biomedical implants," in *ICM 2011 Proceeding*, dec 2011, pp. 1–5.
- [4] Omisakin A; Mestrom R; Bentum M, "Low-Power Communication for an Implanted Intracortical Visual Prosthesis," in *2019 13th European Conference on Antennas and Propagation EuCAP*. IEEE, 2019.
- [5] L. D. Xing, S. Shafie, and H. Ramiah, "Low power BPSK modulator for the application of capsule endoscope," in *2011 Fourth International Conference on Modeling, Simulation and Applied Optimization*, apr 2011, pp. 1–4.
- [6] S. K. Arya and Neelkamal, "A Comparative Study of Dynamic Latch Comparator," in *International journal of Advances in Electronics Engineering*, vol. 1, no. 1, 2011, pp. 313–317.
- [7] P. Uthaichana and E. Leelarasmee, "Low power CMOS dynamic latch comparators," in *TENCON 2003. Conference on Convergent Technologies for Asia-Pacific Region*, vol. 2, 2003, pp. 605–608 Vol.2.
- [8] A. Rabiei, A. Najafizadeh, A. Khalafi, and S. M. Ahmadi, "A new ultra low power high speed dynamic comparator," in *2015 23rd Iranian Conference on Electrical Engineering*, 2015, pp. 1266–1270.
- [9] J. Delbeke and C. Veraart, "Visual Prostheses," *Encyclopedia of Medical Devices and Instrumentation, Second Edition*, pp. 530–549, 2006.
- [10] Farzad Asgarian and Amir M. Sodagar, "Wireless Telemetry for Implantable Biomedical Microsystems, Biomedical Engineering," *Trends in Electronics, Anthony N. Laskovski, IntechOpen*, 2011.
- [11] F. E. Terman, *Radio engineers' handbook*. New York.: McGraw-Hill Book Company, 1943.
- [12] E. Waffenschmidt, "QI Coupling Factor." [Online]. Available: <https://www.wirelesspowerconsortium.com/knowledge-base/magnetic-induction-technology/how-it-works/coupling-factor.html>
- [13] J. Kim, M. S. Chae, L. Wu, and W. Liu, "A fully integrated DPSK demodulator for high density biomedical implants," in *2008 IEEE Biomedical Circuits and Systems Conference*, nov 2008, pp. 93–96.
- [14] M. Zhou and W. Liu, "A Non-Coherent PSK Receiver with Interference-Canceling for Transcutaneous Neural Implants," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, feb 2007, pp. 156–593.