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Design Trade-Offs in a-IGZO TFT based Bio-Signal Sensing Front-Ends

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Abstract

With the advent of the Internet of Things (IoT) wearable sensing devices are gaining importance in our daily lives for applications like vital signal monitoring during sport and health diagnostics. Amorphous Indium Gallium Zinc Oxide (a-IGZO) Thin Film Transistors (TFTs) fabricated on flexible large-area substrates are a very interesting platform to build wearable sensing devices due to their flexibility, conformability to human body, and low cost. For this paper four different bio-signal sensing frontend circuits based on a-IGZO TFTs are designed, fabricated, measured and compared, focusing on three performance indicators which are in trade-off: Power Efficiency Factor (PEF), area occupation and input impedance. Considering a 200 Hz bandwidth, the measured PEF varies between 4.7×10^5 and 7.5×10^6. The area occupation spans from 4.2 to 37 mm^2, while the input impedance at 1 Hz varies from 5.3 MΩ to 55.3 MΩ. The front-ends based on diode-load amplifiers are compact but have the lowest input impedance and need external capacitors; a front-end exploiting positive feedback impedance boosting has the highest input impedance and is fully integrated on foil, but occupies the largest area.

1) Introduction

Wearable sensing devices are gaining significant importance in our daily lives not only for applications like vital parameters monitoring during sport, but also for health diagnostics (e.g. glucose monitors, impedance tomography, and bio-signal monitors to measure electromyograms, electrocardiograms and electroencephalograms). Ideally, these devices should be flexible and conformable to the human body, to provide user comfort and good adhesion to the skin, ensuring minimum disturbance to the measured signals when moving (i.e. minimizing motion artefacts). In addition, they should be power-efficient for longer battery life, while achieving the required measurement accuracy (i.e. noise performance). Amorphous Indium Gallium Zinc Oxide (a-IGZO) based Thin Film Transistors (TFTs) fabricated on flexible large-area substrates are attractive for such type of applications because of their low cost, compatibility with large area and mechanical flexibility.

Bio-signal measurement systems on flexible substrates are inferior to mainstream silicon technology in terms of performance, due to the low intrinsic gain, large parasitics and high flicker noise typical of flexible electronic devices like a-IGZO TFTs. However, it has been shown that bio-signal acquisition systems using TFTs on flexible substrate can achieve the accuracy required even for demanding biomedical applications such as Electroencephalography (EEG) [1]). To implement bio front-ends using flexible technologies, a technology-aware circuit design approach that takes into account the technology's peculiar characteristics, optimizing circuit functionality, is a must.

In this paper, we first discuss the key metrics in bio-signal frontend architectures, highlighting the trade-offs that become especially important when a-IGZO TFTs are used. We then discuss the realization of different front-ends for bio-signal sensing systems, designed and fabricated using a-IGZO TFT technology. The front-ends are characterized and compared in terms of different performance metrics, including PEF (noise and power), input impedance and area. Based on this comparison, we get insight into performance trade-offs in bio-signal front ends in flexible technologies and highlight optimum front-end architectures for different specific applications.

The paper is organized as follows: In section 2 design constraints for bio-signal front-ends are discussed together with the relevant trade-offs. Section 3 presents few bio-signal front end architectures based on representative state-of-the-art designs, discussing their advantages and disadvantages. Section 4 gives an overview of the properties of IGZO TFTs and the impact of their properties on the design of bio-signal front-ends. Section 5 presents the chosen front-end

topologies implemented with IGZO TFTs. Measurement results are presented and discussed in section 6 and section 7 gives some conclusions.

2) Design Constraints for Bio-signal Acquisition Front-Ends

Bio-signal sensing front-ends are mostly used to amplify weak bio-signals generated by muscular and neural tissues, in the typical range of 10 µV- 10 mV, in the presence of DC electrode offset which may be as large as ±300 mV. The bandwidth of bio-signals typically lies in the range of 0.5 Hz- 5 kHz. The bio-signal front-ends should meet many challenging requirements to extract the weak bio-signals with such a large DC offset. Among these requirements can be listed:

i)   Low noise to maintain signal quality;

ii)   Low power dissipation for longer battery life;

iii)   High input impedance to minimize signal attenuation from electrode to front-end;

iv)   Reduced area occupation for low cost and high spatial resolution;

v)   Removal of DC electrode offset to prevent saturation of the front-end;

vi)   High common mode rejection ratio (CMRR) to reject interferers;

Low noise is required for an accurate measurement. The main noise contribution in silicon front-ends circuits is typically thermal noise. The input-referred spectral density of thermal noise in a transistor, $\overline{v_n^2} = 4kT\gamma/g_m$,[1] is inversely proportional to its transcoductance g_m. The transcoductance increases with a larger bias current I. For this reason, a fundamental trade-off exists between noise and bias current, which is especially relevant to biomedical front-ends. This trade-off is typically characterized in amplifiers by a figure of merit called Noise Efficiency Factor - NEF [2]:

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi.U_T.4kT.BW}} \qquad (1)$$

where $V_{ni,rms}$ is the total input-referred noise, I_{tot} is the total supply current of the amplifier, BW is the amplifier -3 dB bandwidth, and U_T the thermal voltage. As it can be seen from (1) the NEF does not take into account the supply voltage. For this reason, to compare circuits having a different supply voltage V_{DD}, the Power Efficiency Factor PEF was introduced in [3]:

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[1] The parameter γ depends on the bias point of the transistor and is typically assumed to be 2/3 in a transistor above threshold and in saturation.

$$PEF = NEF^2 V_{DD} \qquad\qquad (2)$$

The PEF can be used to characterize the trade-off between noise and power consumption, and will be used in the later sections of this paper to compare different IGZO front-ends.

Another important requirement is that bio-signal front-ends should have large input impedance Z_{in}, to minimize the signal attenuation from electrode to the front-end. Indeed the input signal is partitioned between the electrode impedance and Z_{in}, and thus a large input impedance is desired, especially in ambulatory applications. We will use Z_{in} as a second figure of merit to compare different IGZO front-ends.

A third important parameter in the design of biomedical front-ends is their area occupation: a compact front-end may be cheaper to fabricate and enables higher spatial resolution, which in applications like e.g. electromyography (EMG); electroencephalography (EEG) and recordings of the neural cortex can be useful to improve diagnostic accuracy [4,5].

The large DC electrode offset is another pressing problem often encountered in bio-signal front-ends. One of the obvious solution is to use AC coupled architectures, which inherently remove offset at the cost of large area to implement the input capacitors.

CMRR is another important parameter in the design of bio-signal front-ends. It should be as large as possible to suppress coupling from the mains and other sources of interference.

From the above discussion it is clear that PEF, input impedance and area are important parameters when designing biomedical front-ends: in this paper we will focus on these performance indicators to compare different circuits for bio-signal sensing. Section 3 will present a few typical biomedical front-end architectures, while Section 4 will discuss the trade-offs existing between these parameters when designing bio-signal front-ends using IGZO.

3) Bio-signal Front-End architectures

Three main approaches to biomedical front-ends based have been described in literature and are illustrated in Fig. 1. The architecture in Fig.1(a) uses an open-loop amplifier, A_1, to amplify the input signal. Given the low frequency range of biomedical signals (as low as 0.5 Hz), a very low high-pass corner ($1/(R_{in}C_{in})$) is required, implying the need for a large $R_{in}C_{in}$. In addition, due to the low frequency bio-signal, chopping is a widely used technique to modulate the signal at higher frequencies and supress the amplifier flicker noise and offset. In Fig. 1, this is shown with CH_{in} and CH_{out} representing input and output chopper, respectively. In Fig.1(a), CH_{in} is

placed after the high pass filter, to ensure the effectiveness of electrode offset blocking. However, using this approach, any mismatch in the capacitors C_{in} will affect the CMRR. In addition, this circuit exacerbates the negative role of the amplifier input parasitic capacitance C_P. Calling the chopping frequency f_{chop} and the input signal frequency f_{in}, the switched-capacitor resistor seen at the input of the amplifier due to the chopping of its input parasitic capacitance is $1/(2f_{chop}C_P)$ and, assuming that R_{in} is very large, the amount of input signal V_{in} coupled to the input of the amplifier can be approximated to be $V_{Ain} = \frac{j2\pi f_{in}C_{in}}{j2\pi f_{in}C_{in}+2f_{chop}C_P}V_{in}$.

One should notice that typically $f_{chop} \gg f_{in}$. According to this equation thus, a very large C_{in} is needed to ensure negligible signal attenuation. To provide a numeric example, assuming that $f_{in} = 0.1Hz, f_{chop} = 1kHz$, and $C_P = 100\,pF$, to ensure 10% attenuation one would need $C_{in} = 664nF$. This capacitance is so large that cannot be integrated on foil with acceptable yield, at the state of the art, and needs to be implemented using a discrete capacitor. In addition, the input impedance of the overall front-end using chopping, $Z_{in} \approx 1/(2f_{chop}C_P)$, is limited due to the relatively high chopping frequency needed to ensure noise suppression. Discrete capacitors are often used in state of the art reports of bio-signal frontends implemented with TFTs [1]. Considering for example commercial ceramic SMD solutions [2], a 1μF capacitor rated up to 50V DC can be implemented in a 1.6×0.8 mm^2 footprint, with 0.8 mm height. These dimensions might still be compatible with flexible wearable solutions, provided that the capacitors are covered with a suitable e.g. silicone layer that covers the discrete components, smoothening the foil surface. Monolithic solutions, which are obviously more attractive from an integration and user-comfort perspective, would require adding a dedicated dielectric to the technology stack, which should offer a capacitance density significantly higher than the ~10nF/mm^2 presently available in our technology. Smaller input capacitors can also be used when choosing different circuit schematics, like the ones discussed in the rest of this section.

Fig. 1(b) depicts the use of an amplifier (A$_2$) in capacitive feedback, resulting in an accurate gain set by ratio of passive elements C_{in}/C_{fb} [6-8]. Capacitors are preferred to resistor to realize the feedback because they do not introduce additional noise sources to the circuit. As the input capacitors in this case are behind the input chopper, their mismatch does not contribute to CMRR. However, this architectural choice results in a DC-coupled amplifier, which is affected by a large output signal due to the input offset up-converted to the chopping frequency

and amplified. This might jeopardize the linearity of the front-tend. The effect of the electrode offset can be suppressed at the cost of increased circuit complexity using DC servo-loops (DSL), as proposed in [7,8]. The highly resistive pseudo-resistors shown the inset of Fig. 1(b) ensure biasing of the amplifier input pair. They should be large enough to ensure that the chopped signal is in the bandpass of the closed-loop amplifier. The use of pseudo-resistors, which are largely variable and bias-dependant, results in a very inaccurate high-pass pole. Besides, the linearity of this stage might be jeopardized by the bias sensitivity of the pseudo-resistors. Instead of exploiting pseudo-resistors, to realize the high-pass corner in the closed-loop amplifier, a DSL can be used to implement the high pass response [7].
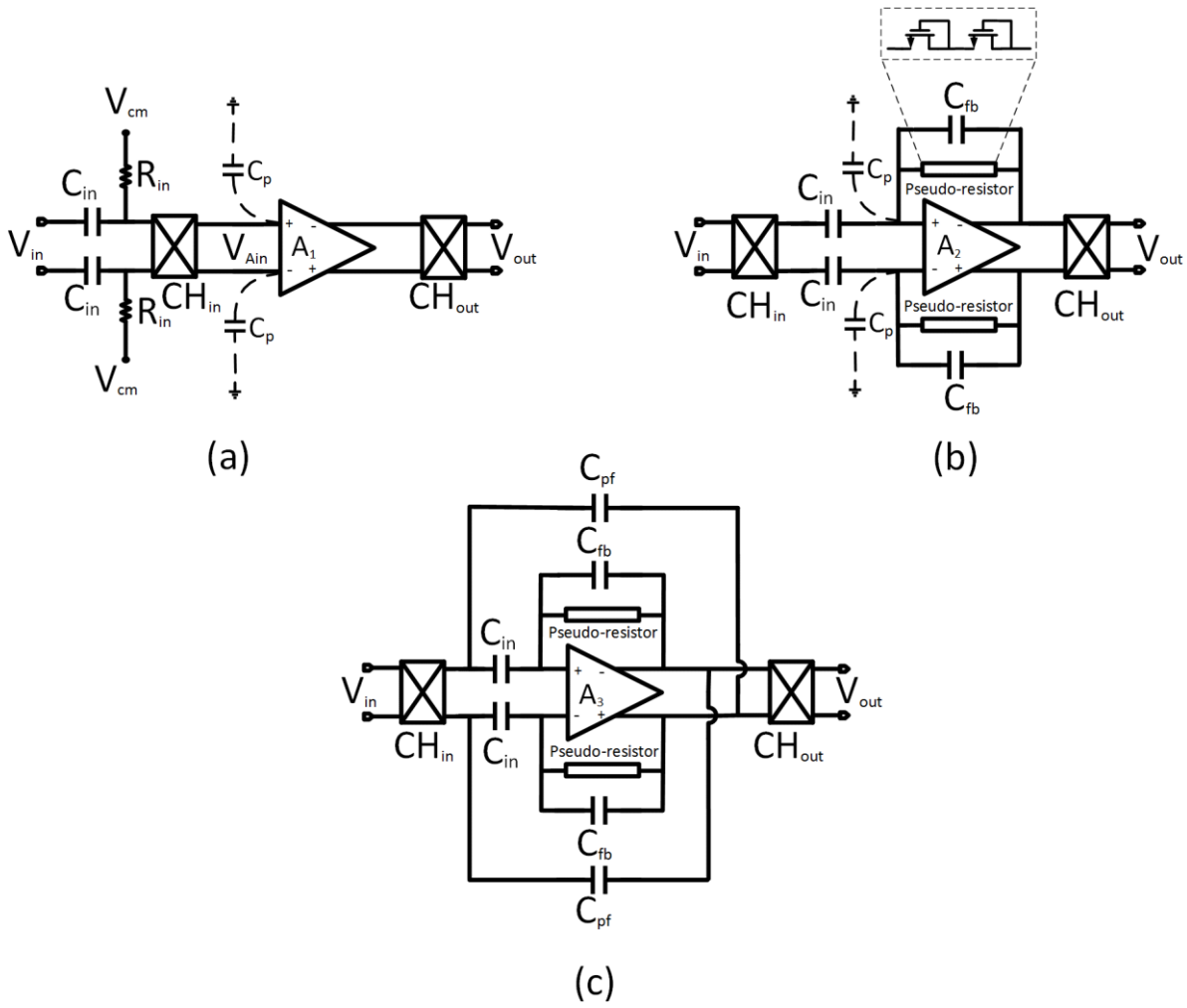

Fig. 1 Bio-signal front-ends implemented with (a) an open loop amplifier (b) an amplifier in capacitive feedback (c) an amplifier in capacitive feedback with additional impedance-boosting positive feedback loop

Obviously, noise and gain considerations are very important in determining the size of the capacitors. The input referred noise of the bio-signal front-end in Fig. 1(b) is given by

$$\overline{v_{ni}^2} = \left(\frac{C_{in} + C_{fb} + C_p}{C_{in}} \right)^2 \overline{v_{ni,A_2}^2} \tag{3}$$

where, C_p is the input parasitic capacitance and $\overline{v_{ni,A_2}^2}$ is the input referred noise of the main amplifier A_2. Equation (3) shows that the input referred noise of this front-end is an amplified version of the input referred noise of the amplifier. To minimize the total input referred noise C_p must be minimized, and the mid-band gain, given by C_{in}/C_{fb}, should be as large as possible. For the front-end depicted in Fig. 1(b) C_{in} can typically be integrated on foil, but still, according to (3), it must be much larger than C_p and C_{fb}, resulting in large area occupancy and a limited input resistance. Indeed, the switching of C_{in} between positive and negative input every clock cycle requires a charging and discharging current from the signal source. Thus, the combination of input chopper and capacitors C_{in} results in the formation of a switched capacitor resistor offering an input impedance:

$$Z_{in} = 1/(2 f_{chop} C_{in}) \tag{4}$$

In the architecture of Fig.1(c) the input impedance is increased using a positive feedback loop (PFL) [8], realized by C_{pf}. The PFL supplies part of the current needed to charge the input capacitors at the chopping frequency. This current does not need to flow anymore from the input port, and thus the input impedance is increased. A drawback of this approach is that implementing the PFL results in area overhead due to the capacitors C_{pf}. Moreover, stability concerns in the presence of parametric variability must be taken into account in this circuit. The condition for infinite input impedance [8] can be found to be:

$$C_{pf} = \frac{C_{in}}{G-1} \tag{5}$$

where,
$$G = \frac{A_3}{1 + A_3 \dfrac{C_{fb}}{C_{in}}} \tag{6}$$

and A_3 is the open loop gain of the op-amp. Hence, the condition for the stability from (5) is:

$$C_{pf} < \frac{C_{in}}{G-1} \tag{7}$$

Considering the analysis discussed till now of the circuit in Fig. 1(c), when A_3 is not very large and is strongly variable (as it will be the case in IGZO implementations) a trade-off exists between improving input impedance and the risk of instability.

4) a-IGZO TFT Technology

In this section, we discuss some of the properties of a-IGZO TFTs and their impact on bio-signal measurement front-ends, with special focus on the trade-offs between PEF, input impedance and area occupation.

The main limitation of metal oxide TFTs is their mobility, which is around 10-20cm^2/Vs, i.e. more than an order of magnitude smaller than what measured in mainstream monocrystalline Si Field Effect Transistor (FETs). The small-signal intrinsic gain ($g_m r_o$) is also limited as it directly depends on mobility. There are only n-type devices in this technology, which makes impossible to use the well-known complementary circuit techniques (CMOS). The low intrinsic gain and the absence of complementary devices limit the gain attainable with a-IGZO amplifiers, which makes structures based on feedback less useful in stabilizing the close-loop performance compared to standard Si CMOS solutions.

Considering the PEF, the fundamental difference between standard silicon front-end and IGZO TFT based front-ends is the noise corner frequency. In standard silicon implementations the noise corner frequency is lower than the bandwidth of the core amplifier and thus chopping frequencies larger than the noise corner frequency (f_c) can be used i.e. $f_{chop} > f_c$. This results in a front-end noise being defined by the thermal contribution only, and in an effective cancellation of the flicker noise. In contrast, IGZO TFT based front-ends have a noise corner frequency which is generally larger than bandwidth of the amplifier. As a consequence, IGZO front-ends can only be chopped with $f_{chop} < f_c$, which means that IGZO frontends are 1/f noise dominated at the state of the art: as a consequence, the additional flicker contribution to noise greatly degrades the PEF.

The flicker noise power spectral density in the IGZO TFTs current can be modelled [9] as:

$$S_{ID}(f) = \frac{\alpha_H q I_D{}^2}{f W L C_i (V_{GS} - V_{TH})} \tag{8}$$

where, α_H is Hooge coefficient, I_D is bias current, WL is the area of the device, C_i is the channel capacitance per unit area and $V_{GS} - V_{TH}$ is the overdrive voltage.

The TFT channel current in the saturation region can be described [10] according to:

$$I_D = \beta \frac{W}{L} \left(V_{GS} - V_{TH} \right)^{\delta} \tag{9}$$

where δ and β are suitable coefficients. The input referred flicker noise voltage spectral density for a single TFT can be then calculated, combining (8) and (9) to be [11]:

$$S_{n,in}(f) = \frac{2\alpha_H q}{C_i \delta^2 W^{\frac{\delta+1}{\delta}} L^{\frac{\delta-1}{\delta}} f} \sqrt[\delta]{\frac{I_D}{\beta}} \tag{10}$$

The parameter δ is typically higher than three [11], which implies that a change in I_D will not result in large change in 1/f noise, while an increase in device area will result in significant noise reduction. As the most effective strategy to alleviate 1/f noise in IGZO amplifiers is to increase the area of the input devices, a tradeoff exists between noise level (thus PEF) and area. Another important point in IGZO TFTs front-ends is the fact that most IGZO technologies do not offer a self-aligned TFT stack, and thus IGZO TFTs are characterized by a large gate-drain overlap capacitance C_{gd}. In a gain stage as the ones depicted in Fig. 1, the C_{gd} of the input TFTs will suffer from Miller effect. This means that the actual parasitic capacitance from the input node to ground can be found to be

$$C_p \approx (1+a)C_{gd} \tag{11}$$

where a is the gain between gate and drain of the input TFTs. In a single-stage amplifier the gain a will be equal to the total amplifier gain A_i, introduced in Section 3.

When using an amplifier in a close-loop bio-signal frontend of the type introduced in Fig. 1(b) and (c), according to equation (3) the input equivalent noise increases due to the large C_p, and this effect must be counteracted by an increase of C_{in} (and C_{fb}), aggravating the tradeoff between noise and area. On top of this, increasing C_{in} results in a decreased input impedance according to (4), causing a trade-off between noise (and thus PEF) and input impedance.

To alleviate this tradeoff, circuit techniques like the impedance boosting introduced in Section 3 (Fig. 1(c)) can be used, but this results in a considerable additional area overhead, in order to implement the capacitors banks needed to provide an accurate input impedance compensation. In summary, focusing on the main performance indicators PEF, area and input impedance, we can conclude that in bio-signal front-ends based on non-self-aligned IGZO TFTs there exist:

1) A tradeoff between noise (PEF) and area due to:
   - the large TFTs needed to counteract 1/f noise and
   - the detrimental effect on noise of the large TFT parasitic capacitances C_p (exacerbated by Miller effect) which can only be alleviated by larger C_{in};

2) A tradeoff between noise (PEF) and input impedance, due to need to select large input capacitors C_{in} in presence of large parasitic TFT input capacitance C_p to ensure good noise performance; and

3) A tradeoff between input impedance and area, due to the area overhead needed to implement impedance boosting techniques as the positive-feedback one described in Section 3.

As discussed before, the IGZO technology is unipolar. For this reason specific amplifiers topologies must be used, taking inspiration from the work done in silicon technology in the late 1970's when only NMOS devices were available. In next Section a set of bio-signal front-ends based on IGZO TFT will be presented and analysed.

5) Bio-signal sensing front-ends based on IGZO TFTs

Four biomedical front-end exploiting the architectures shown in Fig. 1(a) and Fig. 1(c) have been designed and implemented using IGZO transistors. We explore three variants of the core amplifier in the open loop front-end architecture (Fig. 1(a)), obtaining front-ends (FE-I, FE-II and FE-III) and one topology of core amplifier for the capacitive feedback front-end with impedance boosting (Fig. 1(c)), obtaining FE-IV. The front-ends schematics, including the topologies of the core amplifiers and the most relevant design parameters, are summarized in Table I and II respectively. All front-ends are described in detail here below. One should notice that all open-loop front-ends (FE-I, II and III) use discrete components to embody C_{in}.

FE-I and II)

As a first option for the implementation of a biomedical front-end we explore the open-loop architecture of Fig 1(a) with a core amplifier A₁ based on a diode-load topology, as shown in Table I. As the gain of one stage is not sufficient for most of the applications, two stages are cascaded to obtain higher gain. Due to the moderate total gain and the fact that gain is defined by a ratio of transconductances ($A = \dfrac{g_{m1}}{g_{m3}}$), this architecture is rather insensitive to mismatch and variability. Two variants of the cascaded diode connected load amplifier are considered: in the first (FE-I) the input TFT pair is $\dfrac{500\,\mu m}{15\,\mu m}$, where the length is the minimum available in our technology to enable double-gate, and the width is chosen relatively small, to minimize C_P and its negative impact on input impedance. In the second front-end (FE-II) the input pair is made

larger, $\dfrac{4000\,\mu m}{15\,\mu m}$, in order to reduce 1/f noise, resulting in $< 100\ \mu V_{rms}$ simulated integrated noise in the bio-signal frequency band.

FE-III)

The next front-end is still an open-loop topology, where the core amplifier A_1 is based on an enhanced diode-load and positive feedback techniques to increase the amplifier gain, according to the topology reported in [11] and shown in Table I. This amplifier uses a modified diode-load consisting of series diodes M_3, M_5 and M_7 with top gate of diode M_5 and M_7 connected to the source of M_3. In this configuration, the output resistance of M_5 is increased by a factor of $(1+\eta)$ and the output resistance of M_3 is increased by $(1+\eta)^2$ where η is the threshold modulation coefficient due to the presence of the top gate [11]. As the output resistance increases with this load arrangement, the DC gain also increases. The top gates of input transistors M_1 and M_2 are cross-coupled, creating a partial positive feedback which increases transconductance and, thus, gain.

Although this topology effectively enhances gain, it is sensitive to mismatch and variations. Indeed, the introduction of positive feedback in presence of large mismatch and variability may result in instability. Besides, as this amplifier has a low pass response and large gain, the input DC offset due to the large mismatch present in IGZO technology can be amplified enough to saturate the stage. Another drawback of this architecture is the higher supply voltage which is needed due to the many stacked transistors.

FE-IV)

The last front-end is designed according to the impedance-boosting capacitive feedback architecture of Fig. 1(c). The core amplifier A_3 is implemented with the bootstrapped load amplifier shown in Table I. This topology, proposed in [12] uses a load consisting of M_3 and M_5 with a bootstrapping capacitor C_B. At low frequencies, M_3 behaves as a diode load which is less sensitive to threshold variations due to its low gain, while at high frequencies it behaves as a zero-V_{GS} load which provides higher gain. This topology has thus a characteristic band pass response which is desirable to avoid saturation of the core amplifier due to the TFT mismatch.

Table I

	FE-I	FE-II	FE-III	FE-IV
Architecture				
Core Amplifier	 2X in cascade	 2X in cascade		

Table II

	FE-I	FE-II	FE-III	FE-IV
C_{in} [pF]	4.7×10^6 *	4.7×10^6 *	4.7×10^6 *	10
C_{fb} [pF]	-	-	-	1
C_{pf} [pF]	-	-	-	0.8
C_B [nF]	-	-	-	1
W_1/L_1 [μm /μm]	500/15	4000/15	5000/15	500/15

* These capacitors are implemented using discrete components

Table III

Parameter	This work				[1]	[13]	[14]	[15]
	FE- I	FE-II	FE-III	FE-IV				
Technology	a-IGZO				a-Si	DNTT	a-IGZO	a-IGZO
Amplifier max. Gain [dB]	22.9	26.9	25.2	22.8	20	27	22	24.9-23.1
Amplifier Bandwidth	6.8 kHz	4 kHz	400 Hz	185 Hz-3.3 kHz	200 Hz	90 Hz	3 kHz	5.4 kHz-5.2 kHz
Chopping Frequency [kHz]	1	1	1	1	5	-	0.5	5-8
Input referred noise [μV_{rms}] with chopping (BW)	176.9 (1- 200 Hz)	51.2 (1-200 Hz)	29.2 (1-200 Hz)	34.7 (400- 600 Hz)	2.3 (1-100)	-	92.5 (1-200)	125-31.4 (1-500)
Zin with chopping [MΩ]	33.1	5.3	7.9	55.3	-	-	-	29.6-23
Bias Current [μA]	3.2	2.6	3.1	5.2	200	15	3.2	50
Supply Voltage [V]	10	10	±13	10	55	2	10	±13
NEF	868.8	226.6	141.1	217.2	126.3	-	454.3	385.5**
PEF	7.5×10^6	5.1×10^5	5.1×10^5	4.7×10^5	8.7×10^5	-	2.0×10^6	3.8×10^6 **
Area [mm²]	4.2	6.1	17.4	37.0	90*	100.0	5.4	11.2

* Estimated   ** Considering 31.4 μV_{rms} in 500 Hz bandwidth

6) Measurement Results

The front-ends presented in previous section have been designed and fabricated using IGZO TFTs on foil. The foil micrographs of the presented circuits are shown in Fig. 2. In this section the measurement of these circuits are discussed. The main measurement results are presented in Table III. They include the key performance indicators on which this study focuses, i.e. PEF, input impedance and area occupation, besides information on supply voltage, power consumption and bandwidth.
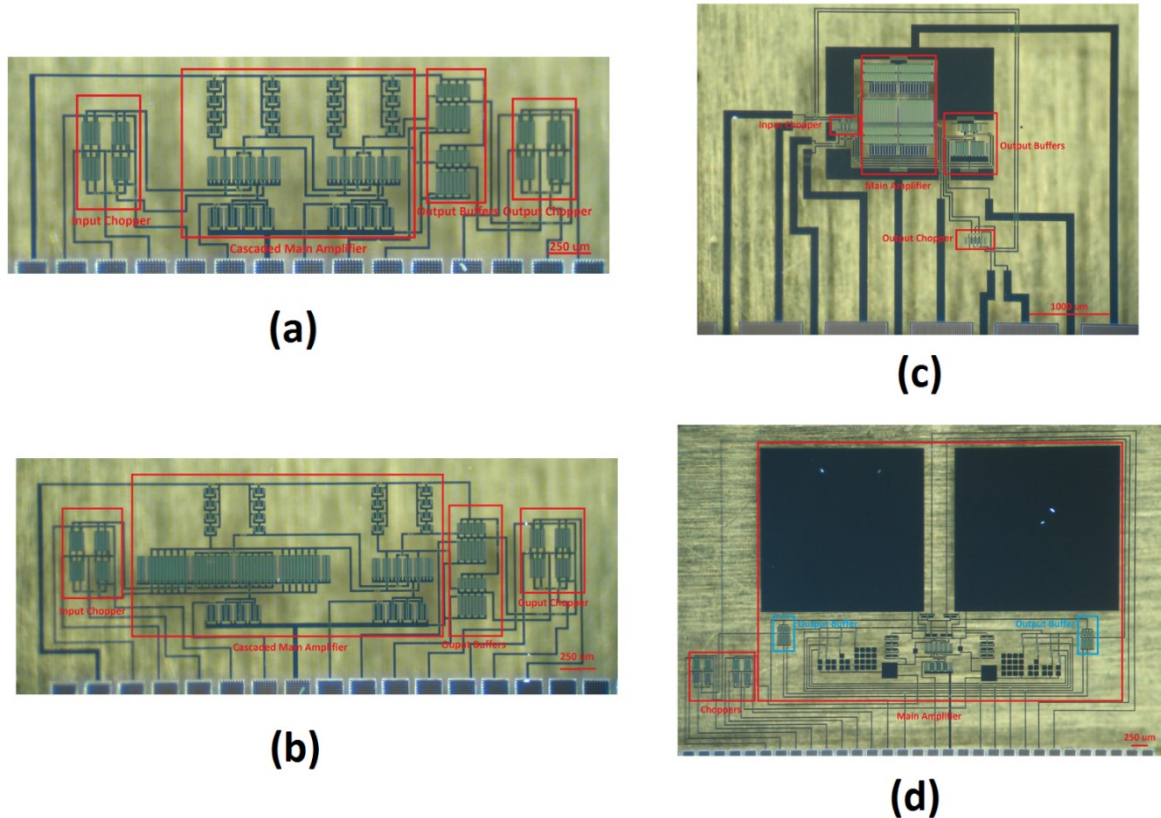

Fig.2 Foil micrograph of the fabricated front-ends (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV.

Fig. 3 shows the frequency response of the bio-signal front-ends, measured deactivating the choppers. Fig. 3 (a) and (b) show the gain plots of the two-stage cascaded diode-load amplifier in FE-I and FE-II respectively. The gain of the amplifier in FE-I is 22.9 dB with -3 dB frequency of 6.8 kHz while for the amplifier with larger input TFTs, the gain is 26.9 dB with a -3 dB frequency of 4 kHz. Fig. 3 (c) plots the frequency response of the enhanced diode-load amplifier. It shows a gain of 25.2 dB in a single stage, with -3 dB frequency of 400 Hz. The GBW is reduced compared to the conventional diode-load due to the stronger Miller effect on the input devices observed in this single-stage topology. The last plot of Fig. 3 (d) shows the

frequency response of the bootstrapped amplifier with feedback network and no chopping. The lower and upper cut off frequency are 185 Hz and 3.3 kHz respectively with a mid-band gain of 22.8 dB. This value is slightly different from the theoretical one, C_{in}/C_{fb}, due to the parasitic TFT capacitances. Owing to the rather small capacitances C_B (1 nF) used in the design and the limited output resistance of the diode-connected devices M_5 and M_6, the high-pass corner of the bootstrapped amplifier is at rather high frequency (185Hz). Such high-pass is not compatible with slow biomedical signals like EMG and ECG. To cope with these signals larger C_B capacitors, and/or a biasing of $M_{5/6}$ ensuring higher output resistance should be used.

As mentioned earlier, it should also be noted that the first two amplifiers are 2-stages while the last two are single stage. Besides, the last front-end is measured in closed-loop and thus its bandwidth is enhanced at the expenses of the maximum gain.
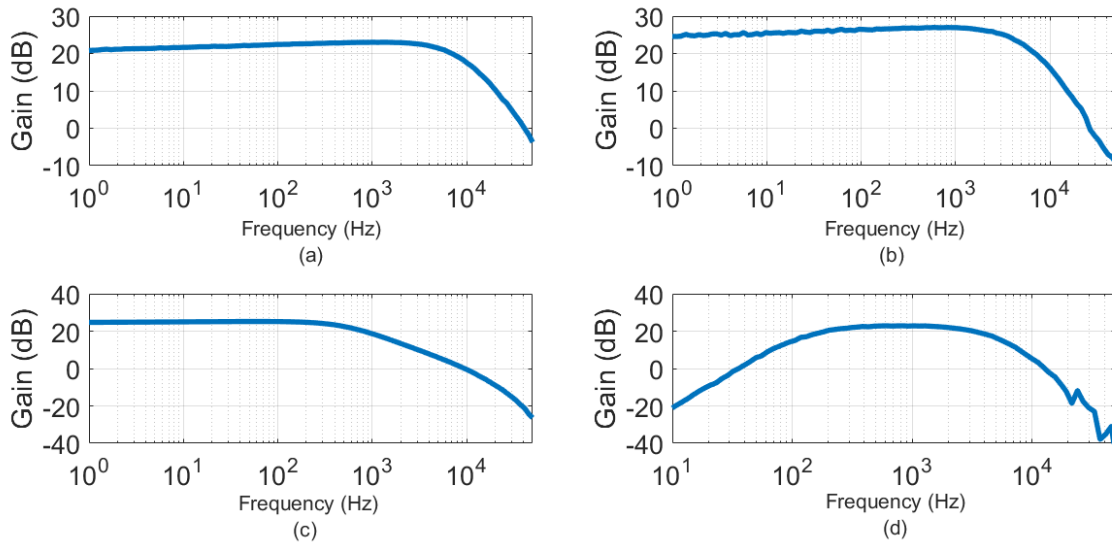

Fig. 3 Frequency response of amplifiers (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV

Fig. 4 represents the input-referred noise spectral density of the front-ends discussed, with choppers deactivated (in blue), and activated (in red). Fig. 4 (a) shows the input noise density of the FE-I (based on the diode-load amplifier). The input noise density without chopping shows a 1/f behaviour starting from 147 $\mu V/\sqrt{Hz}$ at 1 Hz and reaching 5 $\mu V/\sqrt{Hz}$ at 1 kHz. When chopping at 1 kHz is applied, the noise spectral density becomes almost flat with a floor of around 14 $\mu V/\sqrt{Hz}$ till 1 kHz (Fig. 4 (a) – red line). The total equivalent input referred integrated noise in a bandwidth of 1-200 Hz with chopping of 1 kHz is 176.9 μV_{rms}. Fig. 4 (b) shows the input noise density of the FE-II (based on a diode-load amplifier with large input devices). As expected the noise density without chopping (blue line) follows the same trend as

in the previous case, but with considerable reduction in the noise thanks to increased area of the input pair. In this case the input noise density without chopping is 58 $\mu V / \sqrt{Hz}$ at 1 Hz reducing to around 2 $\mu V / \sqrt{Hz}$ at 1 kHz. The total equivalent input referred integrated noise in a bandwidth of 1-200 Hz with chopping of 1 kHz in the complete FE-II is 51.2 μV_{rms} (Fig. 4(b) – red line).

Without Chopping
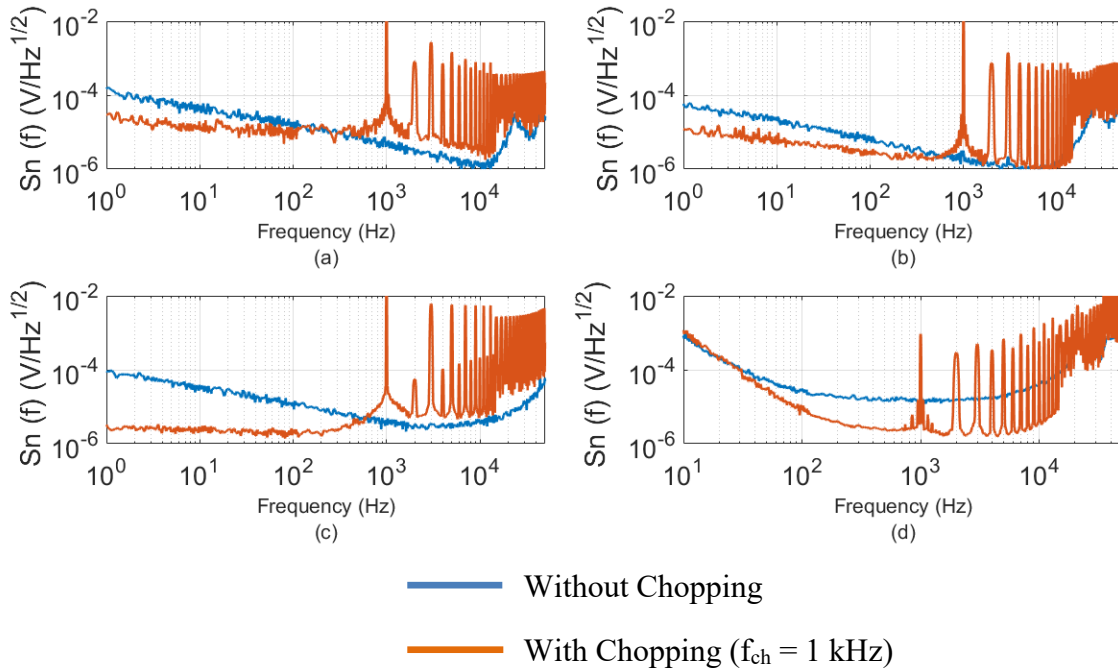
With Chopping (f_{ch} = 1 kHz)

Fig. 4 Input referred noise density of the different front-ends (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV

Fig.4 (c) shows the input noise spectral density of the FE-III, built with the modified diode-load amplifier. The noise spectral density at 1 Hz is 92.4 $\mu V / \sqrt{Hz}$. The application of 1 kHz chopping results in a total equivalent input referred integrated noise of 29.2 μV_{rms} in a bandwidth of 1-200 Hz. The improved noise behaviour offered by the modified diode-connected load amplifier compared to the normal diode-load amplifiers is due to the larger gain realized in a single-stage structure, which decreases the noise contribution of the TFTs after the input pair. The last plot, Fig.4 (d), shows the input noise spectral density of FE-IV, based on the bootstrapped load amplifier. The measurement without chopping shows a trend decreasing in frequency till the lower cut off frequency of 185 Hz and almost a flat floor of 15 $\mu V / \sqrt{Hz}$ till the upper cut off frequency of 3.3 kHz. This is a result of the interplay between the noise transfer function of this front-end and the 1/f noise behaviour of its TFTs. The total equivalent

input-referred noise integrated in a bandwidth of 400-600 Hz, applying chopping at 1 kHz, is $34.7\,\mu V_{rms}$.
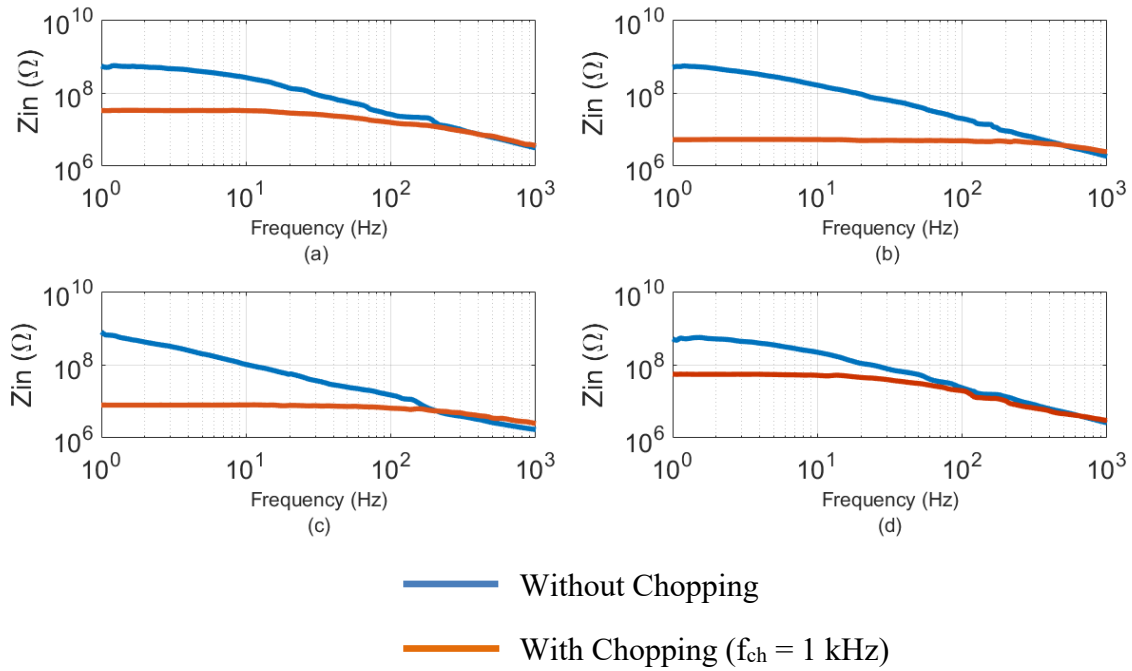

Fig. 5 Input impedance of the different front-ends (a) FE-I, (b) FE-II, (c) FE-III and (d) FE-IV

Fig. 5 shows the input impedance vs frequency for the presented front ends with (red line) and without (blue line) chopping. Fig. 5 (a) and (b) show the input impedance plots of FE-I and FE-II, respectively. The input impedance of the version 1 diode-load amplifier at 1 Hz in absence of chopping is 540 $M\Omega$ while application of 1 kHz chopping reduces the input impedance to 33.1 $M\Omega$. In the case of the version 2 diode-load amplifier, the input impedance at 1 Hz reduces from 499 $M\Omega$ to 5.3 $M\Omega$ with the application of chopping of 1 kHz, which is expected due to the large input pair and its large parasitic capacitance. Fig. 5 (c) shows input impedance vs frequency plot of the modified diode-load FE-III. In this case the input impedance at 1 Hz reduces from 791 $M\Omega$ to 7.9 $M\Omega$ with the application of chopping at 1 kHz, owing to the large parasitic capacitance due to the Miller effect. The last plot of Fig. 8 (d) shows the input impedance vs frequency for the FE-IV. The input impedance at 1 Hz without chopping is 508 $M\Omega$, which decreases to 55.3 $M\Omega$ when chopping of 1 kHz is applied. In this front-end the input impedance after chopping is better compared to the other cases thanks to the PFL impedance boosting.

All the parameters measured in the front-ends presented in this work are summarized in Table III along with comparison with state of the art bio-signal front-ends in similar flexible

technologies, where the three main performance indicators: PEF, area, and input impedance are highlighted. These three parameters which, as explained in section 4, are in trade off, are also shown in a radar plot in Fig. 6 for the front-ends discussed here. As the best PEF is the lowest, the PEF axis is plotted in inverse order, so that the best front-end would cover the largest surface in the radar plot. For the sake of comparison, one should remind that FE-I, II and III use external discrete capacitors.
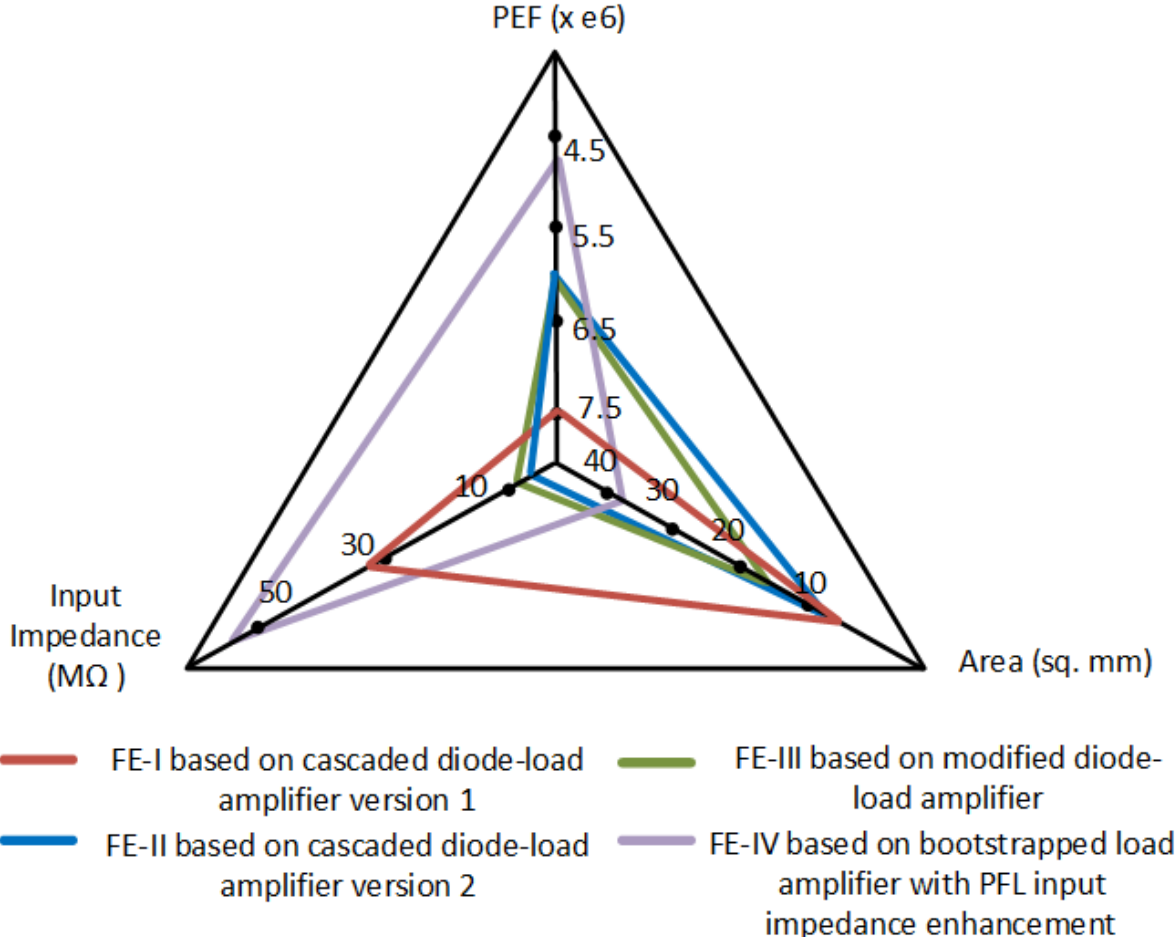

Fig. 6 Performance comparison of the presented front-ends

Clearly, the FE-I with the cascaded diode-load amplifier version 1 has the worst PEF performance, while FE-II and III, with diode-load version 2 and modified diode-load amplifier respectively, are similar. In fact, the former has a higher noise (due to the fact that its gain is divided in two cascaded stages and thus more TFT contribute to noise) but lower power consumption compared to the latter (which stacks many TFTs between the rails and thus needs larger supply voltage). The capacitive feedback FE-IV with input impedance boosting and bootstrapped amplifier achieves the best PEF. This is due to the fact that the bootstrapped amplifier provides high maximum gain in one stage (minimizing the noise contributions of the

TFT after the input pair) using only two stacked TFTs, and thus with no need for high voltage supply. When it comes to input impedance, FE-IV with the capacitive feedback amplifier with impedance boosting again demonstrates the best performance, thanks to the impedance-boosting positive feedback technique employed, albeit at the expense of area for the positive feedback network. It should be reminded that the use of positive feedback in a technology that suffers from high parametric variability requires extra attention to stability issues. The area consumption of the FE-IV is exacerbated by the use of the bootstrapped amplifier, which needs the large capacitors C_B (1 nF) to shorten gate and source of the load TFT at the signal frequency. Still, this FE is the only one which is fully integrated on foil. The other FEs need external discrete capacitors to implement C_{in}.

Finally, our work is compared to relevant state of the art bio-signal measurement solutions implemented on foil ([1], [13], [14], [15]) and listed in Table III. The NEF measured in our front-ends is in line with other a-IGZO references, while the NEF of [1] is better thanks to the lower 1/f noise offered by that technology. The PEF of our front-ends is actually lower than the one reported in all previous art. FE-III achieves this result exploiting a moderate supply voltage and a design that reduces 1/f noise increasing the size of the input devices. FE-II and IV use an even lower power supply (enabled by the simple structure of the amplifiers used in these FEs) and a noise-optimized sizing of the input TFTs. Also, all our FEs use a limited bias current, as their thermal noise is not dominant, and benefit of the better mobility of a-IGZO compared to [1] and [13].

7) Conclusions

In conclusion, for applications where area is not a critical factor because only few bio-signal measurement channels are required, e.g. in heart rate measurements, the capacitive feedback architecture with impedance boosting based on the bootstrapped load amplifier represents an attractive solution, due to better PEF and high input impedance. However, when high resolution electrode matrices are necessary, the minimum required electrode pitch sets a strict requirement on area. In such applications, e.g. high resolution surface EMG, other options should be explored, like the front-ends II and III discussed in this paper. These front-ends, based on diode-load amplifiers with and without output impedance enhancement, should be carefully optimized for the noise, power and input impedance requirements, based on the characteristics of the flexible technology employed and on the specifications of the envisaged application. Also, they need two discrete capacitors each, which might add to cost and decrease the flexibility of the final solution.

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