The testing of generator circuit-breakers

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The Testing of SF_6 Generator Circuit-Breakers

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Abstract - **Generator circuit-breakers face much higher current and voltage stress than distribution switchgear. This has led to a special standard (ANSI C37.013). Strictly in accordance with this standard's requirements, test circuits and -parameters for a 100 kA and 120 kA (25.3 kV) SF_6 generator circuit-breaker have been defined. The circuit-breaker is equipped with capacitors at both sides of the extinction chambers. The effect of these is to reduce the TRV severity and this is quantified for the relevant switching duties. Adequate test-circuits are described. Also, the optional verification of interruption of generator-fed faults with very large dc components has been demonstrated. Herein, delayed current zero can extend arcing time. The importance of arc voltage in reducing the longer arcing time is illustrated in a calculated example.**

I. INTRODUCTION

Generator circuit-breakers are commonly located between generator and step-up transformer in power generating units. Usually, generator circuit-breakers (GenCBs) are single phase integrated into the busduct connecting generator and step-up transformer.

The GenCB's location puts special requirements to the stresses to which these devices are exposed, thermally, electrically and mechanically. The high power flow and the vicinity of the current and voltage generating main components at either side of the GenCB cause the severity of the (short circuit) current interruption to be higher than in distribution networks of similar voltage, both from current and voltage point of view. This has led to the establishment of a IEEE/ANSI standard for GenCBs by an IEEE working group [1], [2]. Traditionally, the interruption of current in GenCB was accomplished in pressurized air arc extinction chambers assisted by a high-pressure air blast. Since pressurized air as an arc extinguishing medium has a relatively long time constant to recover to its non-conducting state, special means had to be applied to drastically reduce the rate of rise of transient recovery voltage (RRRV) in order to facilitate the interruption. Very often, a resistor (in the order of 1 Ω) parallel to the extinction chamber is mounted. The disadvantage of this principle is that a second interrupting chamber is needed to interrupt the resistor-current. A new generation of GenCB's uses SF_6 as arc extinction medium as well as for internal insulation. Exploiting the thermal energy of the arc combined with a puffer action, high breaking capacity can now be realized with low operating energy, the so-called self-blast technology. In SF_6, the reduction of transient recovery voltage (TRV) severity by capacitors parallel to the interrupting chamber is sufficient for succesful current interruption.

Adequate facilities are required to test generator circuit breakers. In most cases the available short-circuit power of test laboratories is insufficient to perform the test in a direct circuit, and synthetic test methods have to be applied. If the GenCB is equipped with a resistor shunting the extinction chamber, the energy in the HV (capacitor-) part of the synthetic circuit is usually insufficient to produce the TRV waveshape that a direct circuit would yield. Two-part test methods are then unavoidable, i.e. separate testing of the interruption behaviour during the thermal and dielectric period of post-arc recovery [3], [4], [5], [6]

In this contribution, the actual (single part) testing is described of a modern SF_6 GenCB equipped with parallel capacitors. The special requirements and measures with regard to current interruption both from the test-laboratory as well as from the user's point of view are emphasized.

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II. CURRENT INTERRUPTION REQUIREMENTS

In this section, the attention is focused to the main points of distinction between generator circuit-breakers and conventional distribution circuit-breakers as far as the interrupting duties are concerned. Herein, a distinction must been made between normal operation and fault situations.

a. Load current. Load currents for large generation units can rise up to 50 kA, often demanding forced cooling. Following interruption of the load current, the two circuits at both sides of the GenCB oscillate independently, creating a TRV that is a sum of two independent waveshapes. First, at the generator side a waveshape appears with a relatively low rate of rise of voltage (RRRV) because both the distributed capacitances and the ac impedance is high compared to the values at transformer side where the higher RRRV appears.

b. System fed faults. In this situation, the fault current is supplied by the step-up transformer. The magnitude of this current has the highest value of all the possible fault situations because the short circuit reactance from transformer and HV system is usually smaller than the generator reactances. Unlike the situation for conventional high-voltage circuit-breakers, the maximum voltage (TRV) stress for GenCB now coincides with the maximum short circuit current stress. The high RRRV originates from the

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low distributed capacitance of the step up - and auxiliary transformer.

c. Generator fed faults. In this case the fault current is fed by the generator causing a dc component that may be higher than the symmetrical short circuit current and may lead to delayed current zero. However, thanks to the arc voltage of the fault and of the circuit-breaker arc, the circuit time constant is reduced by effective arc series resistances added to the circuit resistance. The values of these additional series resistances are expected to be high enough to force an accelerated decay of the dc component.

TABLE I
TEST PROGRAM FOR CERTIFICATION OF 120 kA GENCB

Test-duty		current		asym-metry	RRRV	TRV peak	test circuit
		make	break				
		kA_p	kA_RMS	%	kV/µs	kV_p	(see fig. 1)
load			24	< 20	1.6	23.3	3Ph-D
out of phase	1	115	60	< 20	5.2	65.9	1Ph-T (+synth)
	2	160	60	75	5.2	65.9	1Ph-T (+synth)
short circuit	1	370	120	< 20	5.5	46.6	3Ph-D + synth
	2	370	-	< 20	-	-	3Ph-D
	3	300	120	< 20	5.5	46.6	3Ph-D + synth
	4A	360	-	< 20	-	-	3Ph-D
	4B	-	120	75	5.5	46.6	3Ph-D + synth

The moderate value of the generator reactance limits the short circuit current to values below the system fed case. The same can be said of the associated TRV stress. Dictated by the inherent capacitance of the generator, the TRV rate of rise (RRRV) is about half the value of the system fed fault.

d. Out-of-phase faults. The characteristics of this interruption can be compared with the load current interruption, only the TRV amplitude is considerably higher (proportional to the current). The severity of this interruption depends on the out-of-phase angle δ. Since the generator is at risk at values of $\delta > 90°$, this situation is excluded by protective relaying. For the out-of-phase angle $\delta = 90°$, current is about half the system fed fault current. On the voltage side, the GenCB experiences a RRRV which is roughly in the same order as in the system fed fault case, but with a crest value being $\sqrt{2}$ times higher.

The out-of-phase current, specified in [1] is half the system-fed fault current.

Since the generator neutral is essentially floating, after interruption of the first phase the system neutral will take up mid-potential of the non-interrupted phases so that the first pole to clear is interrupting against a power frequency recovery voltage of 1.5 the system phase-to-ground voltage.

III. THE TEST PROGRAM AND TEST CIRCUITS

In this section, test circuits are described for the testing of two generator circuit-breakers designed for 1000 MVA class power stations with the following rated values:

manufacturer	*ABB, Switzerland*
type	*100 kA and 120 kA*
rated voltage (ANSI)	*27.5 kV*
rated frequency	*60 Hz*
maximum service voltage	*25.3 kV*
maximum rated current	*24 kA*
rated short circuit breaking current	*100 kA and 120 kA*

A test program covering the certification for the 120 kA GenCB was carried out with the interruption parameters from table I. For the 100 kA GenCB, current values are roughly 17% smaller, TRV parameters are the same as with 120 kA.

For the most severe situation to be tested - the system fed fault case - this implies the availability of a test circuit producing current levels equal to the maximum asymmetrical peak in a circuit with X/R = 50 (time constant 133 ms for 60 Hz) of 2.74*I, here 274 and 328 kA_p.

From the voltage side, rate of rise of voltages up to 5.5 kV/µs are required with a crest value of 47 kV, largely exceeding those normally needed in testing of distribution switchgear. For comparison, the maximum

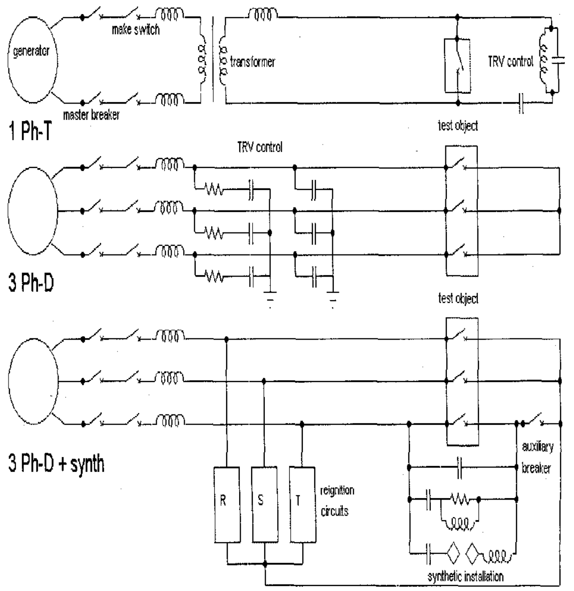

Fig. 1. Test-circuits for testing various switching duties

required RRRV for conventional 36 kV distribution circuit-breakers is 2.8 kV/µs (IEC 56, test-duty 2; short-circuit current reduced to 30% of its rated value) - see fig. 8.

The combination of extreme values of current and voltage makes the use of a synthetic test circuit necessary, combined with a very high current circuit and special measures for prolonging the arcing time. The particular design of the GenCB (three separate poles with activation by a common shaft energized by one stored-energy mechanism) requires three phase fault current testing.

Three different types of test circuits (referred to in table I) were used to cover all the necessary test-duties (see fig.1):

a. *1 Ph-T:* This circuit is the conventional single-phase direct circuit, in which the output voltage of the short-circuit generators is transformed to the desired voltage level. Having a total available power of 4800 MVA single phase (8400 MVA three-phase), KEMA's test facility is able to supply current up to 120 kA_{RMS} at the required voltage level of 31 kV. TRV requirements are met through suitable LRC networks.

b. *3 Ph-D.* This circuit is necessary for very high current values. In this three-phase direct circuit, the output of the generators is directly fed into the test-bay (without transformer) through a 17 kV busbar system designed for 400 kA_{RMS}. This circuit was necessary for the high-current making tests firmly keeping within KEMA's limiting short time current I^2t value of 6.7 10^{10} A^2s.

c. *3Ph-D + synth.* In this case KEMA's synthetic installation is added to the high-current circuit. Hereby, the appropriate values of TRV can be produced using the current injection method. KEMA's synthetic installation is a double LC (energy 2*1.7 MJ) circuit, designed for three phase synthetic testing. In these test series, only one LC circuit was used to produce the injection current (frequency 711 Hz, peak value 14.4 kA_p), in separate tests on the first and last poles to clear respectively. The other LC unit was needed for deliberate arc reignition (see section V) on foregoing current zero. The auxiliary breaker for isolation of the current source from the HV-source, was a commercial airblast generator circuit-breaker with parallel resistor.

TABLE II

EFFECT OF BUILT-IN CAPACITANCE ON TRV PARAMETERS

duty	$U_{c,i}$	$RRRV_i$	$t_{d,i}$	I	Z	C_p	$U_{c,m}$	$RRRV_m$	$t_{d,m}$
	kV	kV/µs	µs	kA	Ω	nF	kV	kV/µs	µs
	inherent values					modified by GenCB			
load	23.3	1.6	< 1	24	124	86	28	1.03	3.8
out-of-phase	65.9	5.2	< 1	60	162	86	79	2.72	4.1
generator fed	46.6	2.2	< 0.5	85	48	130	56	2.22	3.5
system fed	46.6	5.5	< 1	120	86	260	56	1.86	4.2

IV. TRV - MODIFICATION BY THE GENCB

The GenCB is equipped with two capacitors (phase to ground) per phase in order to facilitate arc interruption. At the transformer side C_t = 260 nF is installed, at generator side C_g = 130 nF. The asymmetry arises from the fact that faults on generator side produce a steeper TRV than on transformer-side, so that the natural frequency of the transformer-side circuit needs more reduction than the generator side. This is illustrated in fig. 2, where for the out-of-phase test-duty 1 the (calculated) inherent TRV is compared with the TRV modified by the GenCB. As can be seen, the inherent RRRV has been reduced by approx. a factor of two thanks to the capacitance in parallel to the interrupting gap with a value of 86 nF (series capacitance of 130 nF and 260 nF). On the other hand, the crest value of the TRV modified by the breaker, is higher than the inherent TRV, as listed in table I.

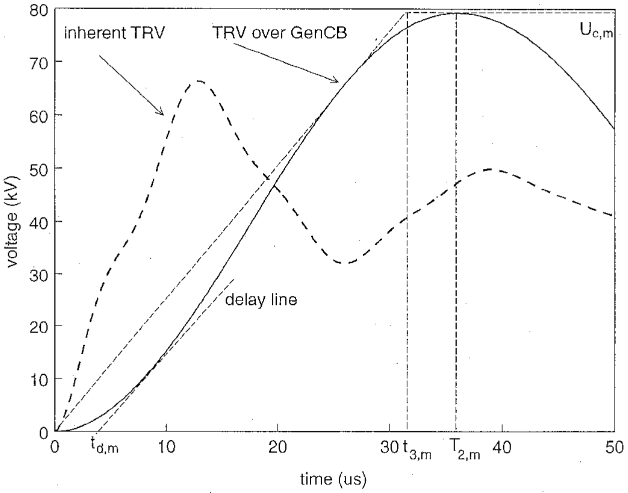

Fig. 2: Calculated inherent and GenCB-modified TRV for out-of-phase switching duty. For symbols see text.

Apart from the more intuitive description of TRV waveshape in terms of frequency and amplitude, a characterisation in terms of rate of rise of TRV (RRRV), crest-value (U_c), time to peak (T_2) time-delay (t_d) is more common in the world of testing. These quantities (indexed 'm' referring to 'circuit-breaker modified') are explained in fig. 2. In this approach, surge impedance (Z) is defined as the ratio of the initial rate of rise of TRV (RRRV) and slope of interrupted current.

RRRV is normally approximated by: RRRV = U_c/t_3, with t_3 the time at which the TRV envelope reaches its maximum (see fig. 2). The importance of the value of the time delay lies in the pause before TRV rises, during which the circuit-breaker gap is allowed to pass through the thermal post-arc period without significant voltage stress.

In table II, the inherent TRV (indicated by index i) based on the ANSI C37.013 standard are compared with the expected TRV parameters (index m) modified by the specific GenCB. The value C_p is the effective capacitance seen *from the* source side of the current in question.

V. TEST EXPERIENCES

a. Circuit design. The circuit reactance is directly obtained from rated voltage and rated (short-circuit) current. Using the prescribed values of (inherent) RRRV and the rated (short circuit) current values, the surge impedance (Z) of the test-circuit can be calculated in a straightforward manner.

Time delay control presents certain problems, since the capacitance normally present in testing laboratories is considerably higher than in the actual system. Given the unusally high values of Z (see table II), a principal difficulty is the realization of the inherent time delay.

This time delay is given as: $t_{d,i} = ZC_d$, with C_d the (usually parasitic) capacitance parallel to the test-object. By subdividing the total short-circuit impedance in a section before and after the GenCB, the series connection of the parasitic capacitances at both sides of the GenCB realizes the necessary very low values of C_d in critical situations.

b. Prolongation of arcing time. Because the current in a synthetic set-up is supplied by a low-voltage source (in our case maximum 15.4 kV), the arc has the tendency to extinct at the first current zero, unlike the case in a circuit offering the full rated voltage. Therefore, special circuits are applied to force reignition of the arc by injection of a short RC current pulse (few kA) very shortly before current zero in any of the three phases. In this way, the arcing time is prolonged to realistic values. In the realization of three reignition circuits for three-phase tests, the power of three standard reignition circuits is insufficient. Therefore, the first phase was reignited by three standard circuits in parallel. For the other two phases reignition circuits were applied by using the second half of the synthetic installation. In this way, two high-power RC current pulses were created, able to force the arc current through zero with a much higher (approx. 10 times) di/dt value than in usual tests, see fig. 3 inset).

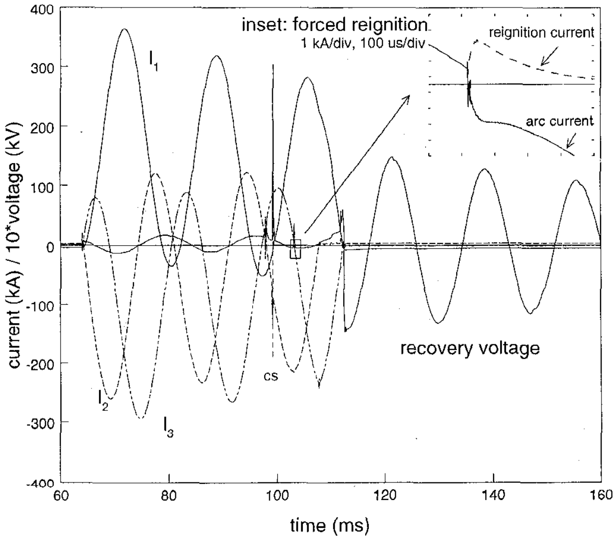

Fig. 3: Interruption of 120 kA three-phase asymmetrical current and reignition current. cs: contact separation

c. Actual tests. During the tests, the metal enclosures of the three extinction chambers were not interconnected at either side, thus creating the most onerous condition of electrodynamic phase-to-phase interaction.

An overview of the three-phase asymmetrical current test (test-duty 4B synthetic, current injection in last phase-to-clear) is given in fig. 3. The period of 2 ms around interruption of a system-fed symmetrical 120 kA fault current (test-duty 1, first phase to clear) is given in fig. 4. After extinction of the arc, the current continues in a high-frequency oscillation, reflecting the non-zero impedance of the parallel capacitor path.

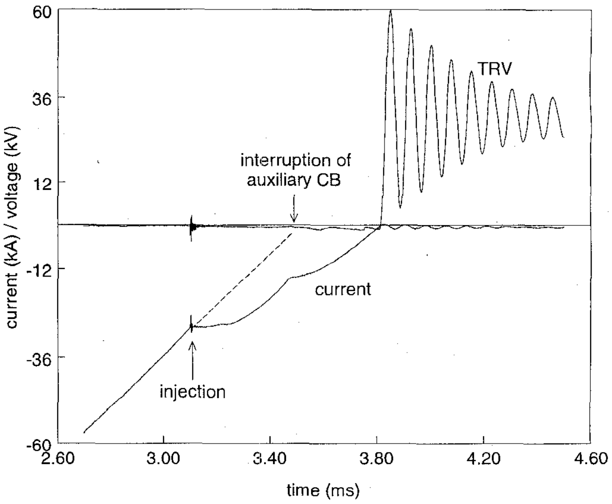

Fig. 4: Interruption of 120 kA system-fed fault

As a result of the test-series, certificates were issued for both test-objects.

VI. GENERATOR-FED FAULT TESTING

Although not required for certification according to ANSI, the 100 kA GenCB was tested for interruption of generator-fed fault current. Under such conditions the subtransient behaviour of the generator may cause dc components larger than the symmetrical current amplitude, leading to delayed current zero.

In the high-power laboratory, a three-phase generator-fed fault test is simulated by energizing the first two phases at their line-to-line voltage zero, effectuating maximum asymmetry. When the third phase is energized 90° later (4.2 ms), the current of one of the other phases passes zero only after several cycles provided the dc time constant of the testcircuit is sufficiently large (here approx. 250 ms).

In fig. 5, an overview is provided of a typical test-result. The two oscillograms were recorded simultaneously with

100 kHz and 1 MHz (inset) sampling frequency by the digital measuring system. Due to the high degree of asymmetry, the small phase shift of current and driving voltage causes very modest TRV stresses in this switching duty.

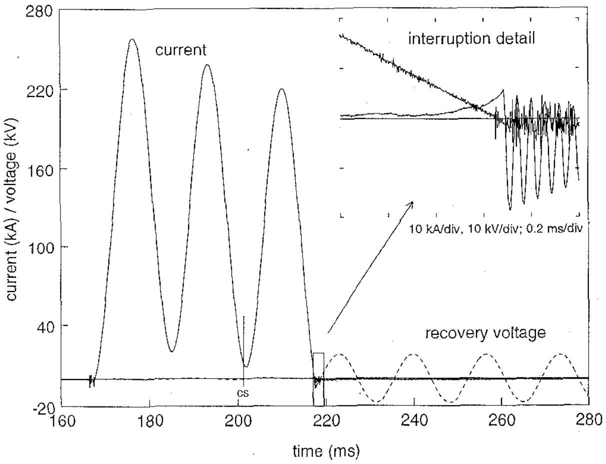

Fig. 5 :Interruption of 85 kA generator-fed current with delayed current zero. cs: contact separation

In fig. 6, (measured) current is shown of two consecutive tests - with and without opening of the GenCB - aimed at verifying the delayed-zero interrupting performance. As can be seen, the action of the arc voltage forces the arc current to zero and reduces the arcing time considerably.

It is difficult to give general guidelines of the effectiveness of arc voltage to enforce current zero. Generally speaking, SF_6 arcs have considerably lower arc voltage than arcs in air. This reduces the "current zero enforcing" ability.

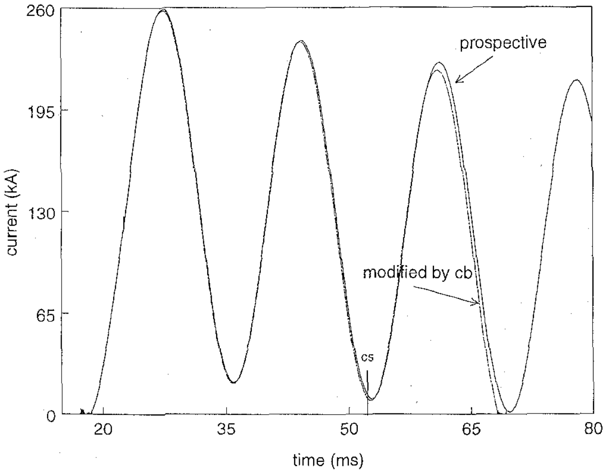

Fig. 6: Interruption of 85 kA generator-fed current with and without modification by GenCB. cs: contact separation.

A calculated example makes this clear. A simulation of a delayed zero interruption in the present test circuit (25.3 kV, 85 kA) is shown in fig. 7. In this case, the interruption of the (almost) symmetrical current I_2 causes the zero-passing current I_3 to become a zero-missing current. This is a specially onerous case, since both last clearing phases face a long arcing time. In fig.7, the cases with (average) arc voltage 250 V and 2.5 kV are compared. It is immediately clear that the higher arc voltage drastically reduces the arcing time, and thus the thermal stress of the extinction chamber. Per phase, the momentary energy stored in the circuit inductance L_c is given by:

$$E_{Lk} = 0.5 L_c i_k^2 \qquad k = 1,\ 2,\ 3.$$

When this quantity remains below a limit defined by:

$$E_{cr} = 0.5 L_c [2\sqrt{2} I_{gf}]^2 = 12.9\ MJ$$

zero missing cannot occur (I_{gf} generator-fed short circuit current). The difference $E_{Lk} - E_{crit} = E_a$ is the excess circuit energy that has to be absorbed by the arc in order to avoid zero-missing:

$$E_a = \int_{cs}^{t} u_a i_k dt$$

with u_a the arc voltage. These energies are also entered in fig 7. From this, it is clear that only the higher arc voltage case is able to absorb a significant amount of the stored magnetic energy.

The energy balance is completed by taking into account the ohmic dissipation. This natural sink of circuit energy absorption accounts (for the test-circuit under study) for approx. 5 - 10% of the energy dissipation.

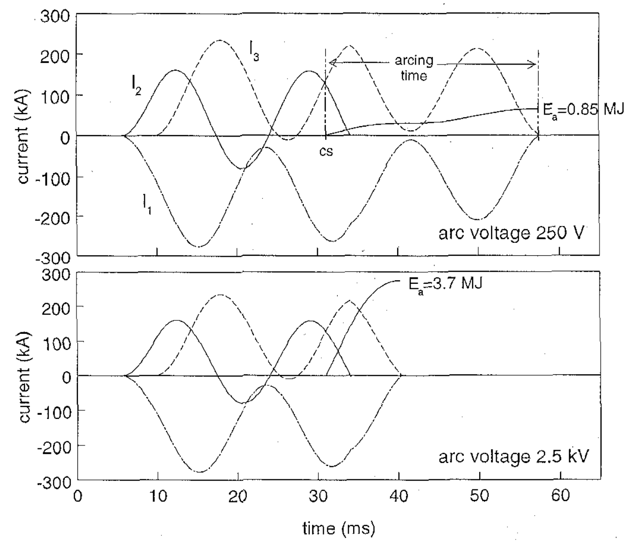

Fig. 7: Calculated effect of 250 V and 2.5 kV of average arc voltage on interruption of 85 kA generator-fed current. Cs: contact separation; E_a: arc energy

VII. SUMMARY AND CONCLUSION

Certification tests were performed succesfully with a 120 kA and a 100 kA generator circuit-breaker. The test program (see table I) was according to the ANSI C37.013

standard. The circuit-breaker has built-in capacitors at both sides of the interruption chamber in order to reduce the TRV stress. This results in a reduction of RRRV of a factor of three for the out-of-phase switching duty. Also, time delay is increased more than four times. The crest value of TRV, however, is 20% higher (see fig. 2).

The generator-circuit breaker under test was tested according to the ANSI RRRV requirements for ratings up to 1000 MVA. Fig. 8 gives an impression of the downsizing of RRRV values at lower ratings (data taken from CIGRE SC 13 [7], [8]).

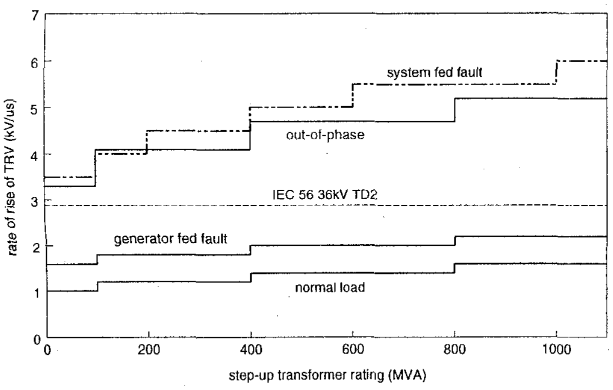

Fig. 8: RRRV values as a function of transformer rating.

Standard current-injection circuits were used for correct TRV stress of first and last clearing phases separately. Specially designed fast-triggered current injection circuits for arc prolongation were applied. The high required surge impedance called for a special circuit topology in order to realize small inherent time-delay values. Due to the presence of a single operating mechanism, all high-current tests had to be performed in a three-phase configuration.

Although strictly not part of the ANSI requirements, additional tests were performed for verification of the delayed current zero interrupting ability. The inherent low arc voltage of SF_6 circuit-breakers may lead to longer arcing time. Considering the thermal stress of the extinction chamber, the effect of the longer arcing time is compensated by the lower arc voltage, since the arc energy is proportional to both. With regard to the thermal stress of circuit components, long arcing times are undesirable. In the majority of fault situations, the fault arc should be considered as well. Therefore, the tests (as in fig. 5 & 6) and analyses (fig. 7) should be considered as a worst case.

VIII. ACKNOWLEDGMENT

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IX. BIOGRAPHIES

René Peter Paul Smeets was born in Venlo, the Netherlands in 1955. He received the M.Sc. degree in physics from the Eindhoven Univ. of Technology, the Netherlands. He obtained a Ph.D. degree for research work on vacuum arcs. From 1983 to 1995, he was an assistant professor at the Fac. of Electrical Engineering, Eindhoven University. During the year 1991 he worked with Toshiba Corporation's Heavy Apparatus Engineering Laboratory in Japan. In 1995, he joined KEMA High-Power & High-Voltage Labs. His interests are in fast processes in switching arcs and their relevance for switching. He is a member of CIGRE WG 13.04, the "Current Zero Club" and the IEEE.

Wim A. van der Linden was born in Escharen, the Netherlands in 1941. He received the B.Sc. degree for electrical engineering from the Technical College of 's-Hertogenbosch in 1963. He joined KEMA's High-Power Lab. in 1965 as a test engineer and is since 1972 employed as a senior test-engineer. He has been actively involved in the design and construction of new test equipment in KEMA High Power Laboratory. He is a member of the IEEE Working Group on synthetic testing of generator circuit-breakers.