Chip scale 12-channel 10 Gb/s optical transmitter and receiver subassemblies based on wet etched silicon interposer

Chip Scale 12-Channel 10 Gb/s Optical Transmitter and Receiver Subassemblies Based on Wet Etched Silicon Interposer

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***Abstract*—In this paper, compact optical subassemblies are demonstrated based on a novel silicon interposer, which is designed and fabricated in a wafer scale process. The interposer includes the design of optical and electrical connections. A low-cost fabrication method, wet etching, is used to define light inputs and outputs as well as create the required recesses in the interposer to embed the chips into the silicon wafer at the same time. Impedance matched traces, for the high speed signals of the CMOS and opto–electronic ICs, are designed using advanced design system software and transferred onto the interposer by photolithography and electro-plating, which are accomplished on the deeply etched topology. The whole process flow of the silicon interposer patterning is designed and demonstrated, and the challenges are discussed. After the process, the optoelectronic dies and their complimentary CMOS parts are flipped and bonded on the interposer in close proximity, and a mechanical optical interface (MOI) is mounted for light coupling. Both transmitter and receiver subassemblies provide 12 parallel optical interconnections, and are scaled down to an area measuring 6 by 8 mm. Signal integrity testing is performed on a probe station for 10 Gb/s data signal delivering clear eye patterns for all channels (in both Rx and Tx subassemblies). The performance is further characterized using bit error rate (BER) testing. Both transmitter and receiver assemblies outperform a reference SFP+, with receiver sensitivity of -10 dBm at a BER lower than 10^{-12} after compensating for the MOI insertion loss. Finally, we also test the assemblies for crosstalk and demonstrate that the current design has a maximal additional penalty lower than 0.2 and 0.8 dB for transmitter and receiver, respectively.**

***Index Terms*—Optical interconnections, optical transceiver, silicon interposer.**

I. Introduction

PRESENTLY, data centers are exponentially scaling up to support the increasing global data center IP traffic. Besides, the portion of traffic residing within the data center is still dominating [1], which means short reach interconnects are increasingly needed. To sustain the growth of traffic in the data center, the demand for bandwidth and bandwidth density for the interconnections between switch ASICs needs to follow the same growth trend. Optical communication is a promising way to propagate high speeds signals with limited distortions and it has completely taken over the data transmission over distances exceeding several hundreds of meters [2]. Currently, pluggable optical transceivers are mainly employed at the edge of the switch board [3]. Therefore, the electrical signals have to propagate from the switching ASIC, along the switch printed circuit board (PCB) to the cards edge. Increased power consumption and electrical distortion become apparent with the continuous increase in data rate. The electronic solution for signal deterioration on the PCB is the addition of re-timers but these lead to additional power consumption. Considering the tradeoffs between electrical and optical communication it is likely that optical interconnects may eventually be integrated onto the switch board, and even in the package of the switch ASIC [3], as serial bit rates continue to grow. This calls for optical transceiver sub-assemblies with an ever smaller footprint so that they can be brought and electrically connected closer to the ASIC and be manufactured at a lower cost.

Small form factor optical interconnect modules can be integrated and fabricated using CMOS platforms by silicon photonics technology [4], [5]. However, lack of light source is the barrier for full integration. In this paper, we focus on commercially available light sources and restrict our discussion mainly to multi-mode VCSEL based demonstrators since multi-mode short distance interconnects are by far the dominant technology of choice [6]. Multimode vertical-cavity surface-emitting lasers (VCSELs) and surface normal photodiodes (PDs) in the 850 nm wavelength range are often used for short reach parallel-optical interconnection as they are much cheaper on component level [7], [8]. However, the cost of a complete optical transceiver module is still high, compared to electronic variants, mainly due to the high cost of packaging of the electronics and photonics, especially for small form factor packaged modules. During packaging, both electrical and optical connections should be considered aiming for improved testing and assembly [9], [10]. The use of wafer scale processes is essential for large scale manufacturing and reduced cost of compact transceivers modules.

Three dimensional (3D) stacking is an effective way to get short connection and high bandwidth density, and it can be achieved by reflow of thick photoresist on wafer scale [11].

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However, the thermal coupling between CMOS and optoelectronics becomes a serious issue. Flexible printed circuits (FPC) and polymer waveguides have been used for optical transceivers, where the dies can be assembled on the designed layout separately [12]. However, the coefficient of thermal expansion (CTE) mismatch between the chip and the carrier represents a major issue. Besides, in order to support light in and out coupling, precise openings need to be fabricated, which is not standard technology and therefore increases the cost. Low electrical loss glass interposer is another packaging approach, where lithographic technology can be used to define traces [13], but the process on glass carrier is not a mature technology yet, and light reflections can impair performance.

Silicon may prove to be a better candidate for an interposer, since it is compatible with the standard CMOS technology. Silicon also has a similar CTE as that of CMOS and optical chips [14]. A high resistivity substrate can be chosen to reduce electrical losses too. However, one of the challenges of using silicon as an integration platform is to couple the light in and out of the flip-chipped opto-electronic dies. Deep through holes, made using extended duration reactive-ion etching of silicon, can provide path for the light through the carrier. In addition, electrical through silicon vias (TSV) can be created to allow for further connectivity [15]. However both electrical and optical TSVs need complicated and costly processing. A guided-wave silicon optical bench has also been developed on a silicon on insulator (SOI) platform for chip to chip interconnects in the 1310 nm transmission window [10], but it requires high accuracy of patterning, since light is reflected via a trapezoidal mirror onto the other side. A low cost process for a silicon interposer is desired to lower down the transceiver module costs.

Previously, we reported on a 2.5D silicon interposer for VCSEL based transmitter assembly [16]. A simple low-cost process based on anisotropic wet etching of silicon was carried out at the wafer scale and used to structure the silicon interposer. In this paper, we present the complete transmitter and receiver assemblies using this fabrication process. We show that the fabricated assemblies demonstrate clear eye patterns and that the link performance, measured for both transmitter and receiver assemblies, results in receiver sensitivity better than -10 dBm. Finally we characterize the performance of both assemblies in terms of channel cross talk and show that the penalty is below 0.2 dB and 1 dB, for transmitter and receiver assemblies respectively.

The paper is organized as follows. Firstly, we will describe in detail the concept of assembly for both transmitter and receiver assemblies. Secondly, the electrical connections (impedance matched traces) are designed, simulated and tested. The whole process for the patterning of the interposer, for both transmitter and receiver, will then be illustrated, following all the lithographic steps. After that, transmitter and receiver assembly is shown. Finally, we test the performance of the assembled subassemblies using BER and channel crosstalk measurements.

II. Concept of Assembly

The 2.5D packaging scheme, for both transmitter and receiver, based on the use of a silicon interposer is shown in Fig. 1, where both front and back side of the silicon interposer are utilized for electrical and optical connections, respectively. Optoelectronic die and CMOS IC are embedded into the recesses of the silicon interposer and are bonded side by side, using flip-chip techniques. They are connected with short impedance controlled traces patterned on the interposer itself. All of the pads for power supply and digital control on the CMOS chip are routed on the surface of the silicon interposer. Additionally, the differential pads for signal I/O are fan-out and redistributed at the edge of silicon interposer. Optical through-silicon vias for each channel are opened by another wet etching step. Then, the mechanical optical interface (MOI), which is used to focus light, is fixed at the back side, and the PRIZM LightTurn System is employed for light coupling into standard multimode fiber ribbon.

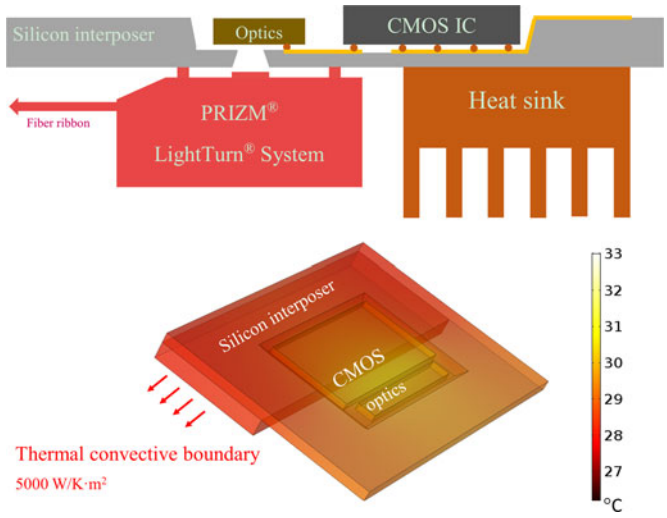

Fig. 1. (top) The 2.5D scheme of packaging of the optical die and its CMOS part on the patterned silicon interposer; (bottom) thermal simulation (by COMSOL) of the sub-assembly, with thermal dissipation area of 8 mm by 3 mm.

The resulting sub-assemblies can be flipped and soldered on a standard PCB or package for electrical connection, as the dies are embedded within the cavity and the 125 μm pads on the dies are fan out to a 250 μm pitch pads. The heatsink can also be mounted on the module as can be seen from the schematic diagram in Fig. 1 (top). Because silicon itself is a good heatsink, with high heat transfer coefficient, the side on which the heat sink is placed is less critical. A convective cooling area of 8 mm by 3 mm on silicon interposer, with the heat transfer coefficient of 5000 W/K $\cdot$ m^2 would be enough for heat dissipation, as can be seen from Fig. 1 (bottom) that the entire assembly exhibits only $\sim$3 °C temperature variation with no forced air-cooling and assuming an ambient temperature of 20 °C.

III. Design of Electrical Connections

As shown in the conceptual sketch, traditional point-to-point wire bonding for die to die connection will be replaced by impedance matched connections, utilizing standard lithography and electro-plating, which will both reduce the assembly cost and deliver improved RF performance in terms of reflections and losses. The design includes two kinds of transmission lines (TMLs), the 100 Ω differential TML for the digital signal

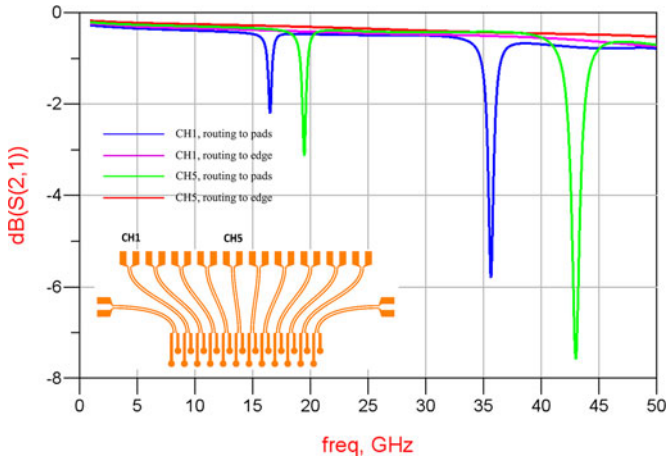

Fig. 2. Transmission parameter of channel 1 (longest trace) and channel 5 (shortest trace), actual traces routing to pads and designed differential traces. Inset: differential traces for 12 channels.

(towards the CMOS inputs) and the 50 Ω single ended TML for analog signal (from CMOS to optics). Advance design system (ADS) software is used for simulating and optimizing the traces design.

A. Differential Traces

In the design, the differential pads on the CMOS IC are routed and redistributed as a 1D array of pads at the edge of silicon interposer, with a pitch of 250 μm, which is compatible with standard PCB technology. The fan-out differential traces are used for digital signal transmission between the edge of the interposer and the IC as shown in the inset in Fig. 2.

We use a high resistivity substrate (2000 Ω·cm) to avoid any signal deterioration due to losses to the substrate. The scattering parameter on channel 1 and channel 5, which is the longest and shortest trace in the design respectively, are given in Fig. 2. The blue line and green line are the simulated results of channel 1 and channel 5, which are routed from the interposer edge to the solder bump pads on CMOS IC. They show two drops in transmission in the range of 1–50 GHz, due to the 250 μm difference in length of the two traces making up the differential pair. In addition, we have also simulated the same design removing the difference in length. The results are shown as the red and pink lines in Fig. 2. No dip in the transmission is visible and the loss is lower than −0.7 dB (channel 1) and −0.5 dB (channel 5) up to 50 GHz. While the length mismatch affects high frequency in a very narrow range, there is limited impact on digital signals. Besides, there is negligible difference among the channels, due to the small loss of the TML.

To validate the designed differential TML, we test a fabricated interposer with differential RF probes on both ends of channel 1 and channel 5.

The 28 Gbaud PAM4 signal is injected at one end of the TML and picked up at the other end. The results, as well as back to back performance, are shown in Fig. 3. Due to the insertion loss (1.2 dB at 28 GHz) of the probe, the swing amplitude is reduced from 352 mV to 293 mV, but the eyes still clearly open.

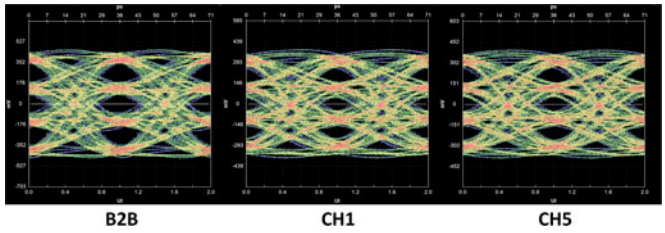

Fig. 3. The experimental results of 28 Gbaud, PAM4 signal.

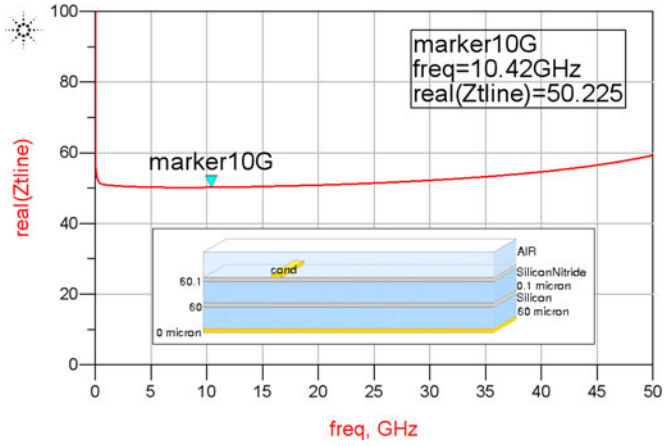

Fig. 4. Simulation result of impedance of designed traces as a function of frequency. Inset: the modelled stacked layer.

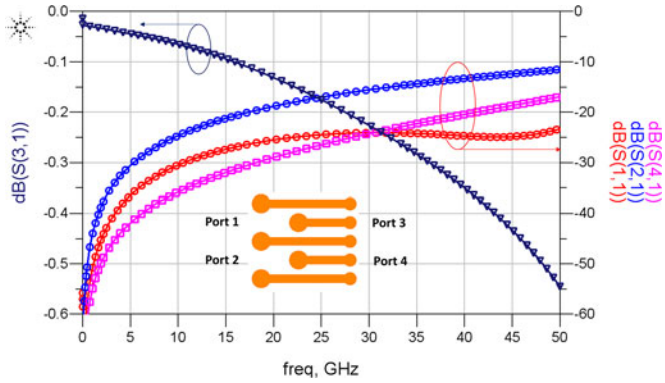

Fig. 5. The scattering parameters of two channel up to 50 GHz, shows the transmission loss (S31), reflection (S11), near end crosstalk (S21) and far end crosstalk (S41).

B. Single Ended Traces

Very short traces between opto-electronics and electronic ICs can be obtained with this 2.5D stacking approach. The single ended traces with impedance of 50 Ω are also designed and simulated in ADS to get optimized transmission parameter. As shown in the Fig. 4, the simulated impedance of the trace is 50.2 Ω at 10.4 GHz, and it slightly increases up to 59.2 Ω when moving up to 50 GHz. The inset picture is the configuration of stacked layers, according to the actual silicon interposer, which is used in the Momentum solver of ADS.

The scattering parameters are also simulated between two adjacent channels. The layout as well as the defined ports are shown in Fig. 5. From the simulation results we see that the

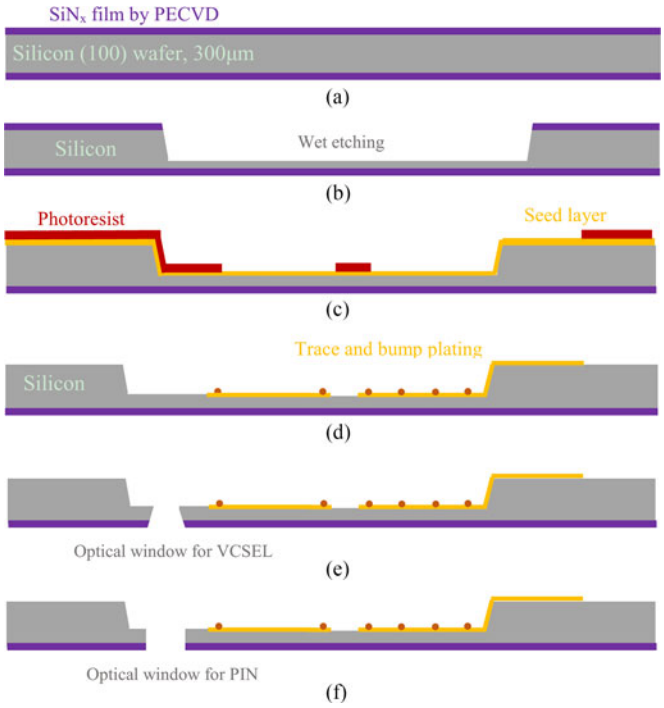

Fig. 6. Process flow of silicon interposer for transmitter and receiver, including (a) PECVD SiNx; (b) wet etching of silicon; (c) lithography on etched topology; (d) electro-plating; etching of optical TSV for VCSEL (e) and PD (f).

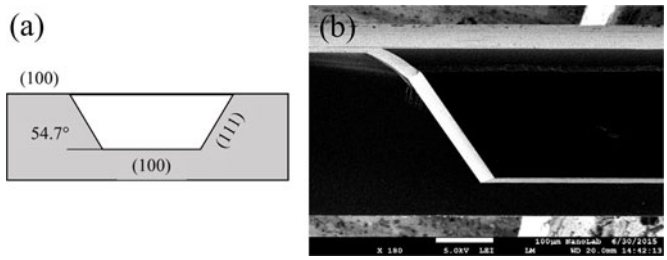

Fig. 7. (a) Principle of anisotropic wet etching of (100) silicon; (b) The SEM photo of cross section of etched sample, with smoothed corner and the etching stop face (111).

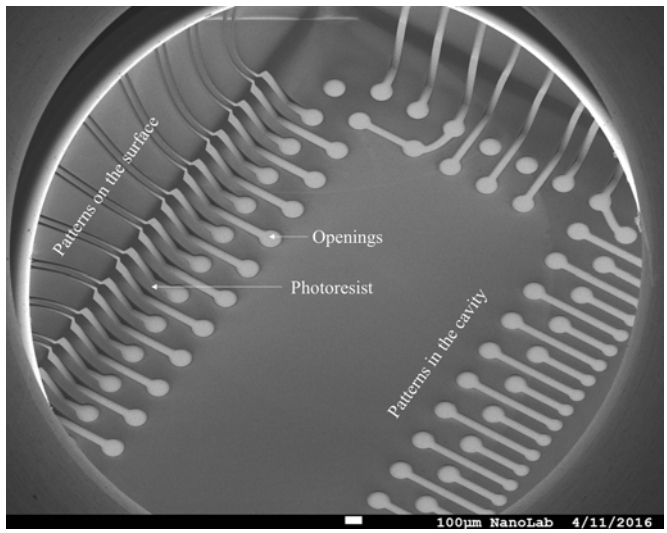

Fig. 8. SEM photo of patterned photoresist on the etched cavity. The photoresist is continous from the surface to the bottom of the cavity.

transmission loss (S31) is only −0.55 dB and the reflection (S11) is below −20 dB in the range of 0-50 GHz. Far-end crosstalk and near-end crosstalk are also calculated, named as S21 and S41 respectively and the magnitude is below −10 dB up to 50 GHz for both curves.

The simulation results indicate that the designed traces on the interposer can support high speed electrical signal transmission. When utilizing high resolution photolithography, the designed trace is precisely transferred onto the interposer, resulting in close to optimal performance. The silicon interposer with these patterned TMLs can therefore easily be used to package the next generation optical transceivers working at 25–28 Gb/s and even 56 Gb/s (using PAM-4) and beyond.

IV. Interposer Fabrication Process

The process flow of the silicon interposer, which is used for the VCSEL based transmitter, includes 4 steps of lithography [17]. Because of the larger apertures of surface normal PD, compared with VCSEL, bigger optical TSVs are needed. Therefore, the fabrication of the receiver assembly interposer includes 5 steps of lithography, with the additional step of lithography used for wet etching silicon on both sides. As a result, a vertical sidewall with a larger aperture can be obtained. The whole process flow is shown in Fig. 6, and the last two drawings are the final etching process for transmitter and receiver packaging respectively.

The fabrication starts from a double polished (100) silicon wafer with a size of 26 mm by 26 mm, which can be scaled up to 12 inch wafers. Initially, a thin layer of SiN_x is deposited by PECVD as a hard mask for wet etching, later to be selectively removed by reactive-ion etching (RIE). Before etching the surface of the wafer, this is carefully cleaned to get a uniform surface for the following processes.

The principle of anisotropic wet etching of silicon is shown in Fig. 7(a): the crystal faces of (111) act as etch stop planes. During etching, the cavity is formed by (111) and (100) faces. Deep etching of silicon is performed in the 35% (by weight) potassium hydroxide (KOH) solution at 80 °C, with an etching rate of 1.0 μm/min. In order to insure a good metal coverage, the convex corners are smoothed by etching the patterned interposer in a TMAH solution for 25 min, after removing the SiN_x mask (see Fig. 7(b) [18]). This obtained structure will be beneficial for the spin coating process which is a part of the following lithography steps.

Performing photolithography on a multilevel surface is challenging. A thick photoresist is used to ensure full surface coverage. The result of lithography on the deeply etched surface of the silicon wafer is shown in Fig. 8. The thick positive photoresist is well developed on both the top and bottom of the etched cavity. From the SEM photo it is evident that also the photoresist accumulated at the concave corner is well developed.

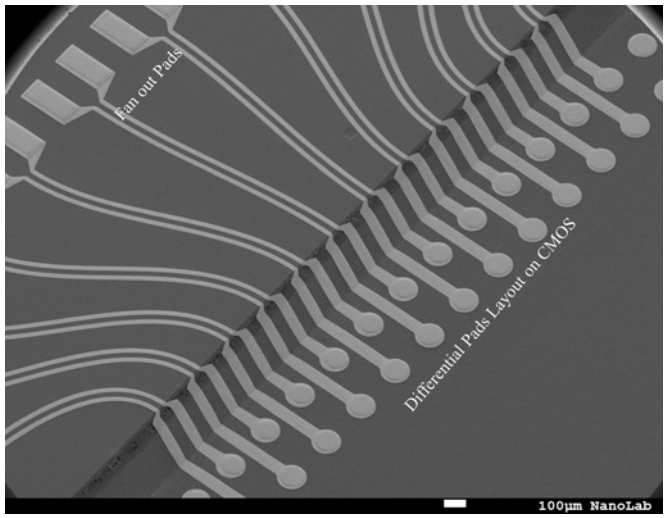

Fig. 9. SEM picture of the plated 12 pairs of differential traces.

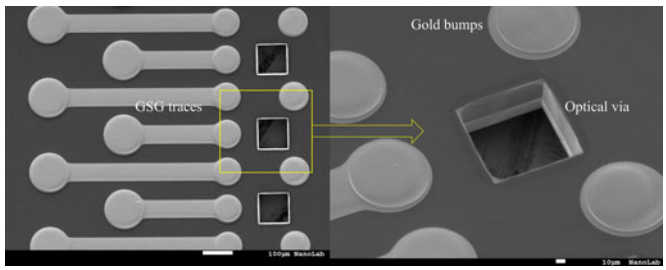

Fig. 10. (left) SEM photo of GSG traces and optial TSVs, and the mask layout is also shown in Fig. 5.; (right) zoomed-in photo shows the details of optical TSV and plated bumps.

After that, the gold is plated through the openings. In Fig. 9, the plated signal traces are shown, obtained after removing the photoresist and chemical etching of seed layer. From the photo, it is clearly visible that the traces are well formed and show no discontinuity.

Finally, in order to get optical TSV with vertical side walls, wet etching is performed in a KOH solution on both sides of the remaining thin silicon layer at the same time [19]. The side walls of the opening are etched until vertical sidewalls are formed. The optical TSV and GSG traces are shown in Fig. 10, left panel, and the zoomed SEM image, in the right panel, shows the etched vertical optical via and the gold bumps for electrical connections. The last wet etching step is also used to define cleaving lines for cleaving the processed wafer into separate interposers.

V. Assembly of Transmitter and Receiver

Flip chip bonding is performed on the FINEPLACER lambda die bonder, which is used to align the dies on the completed interposer. The alignment of the optical die is made according to the optical openings and pads, using a camera and without activating the components (passive alignment).

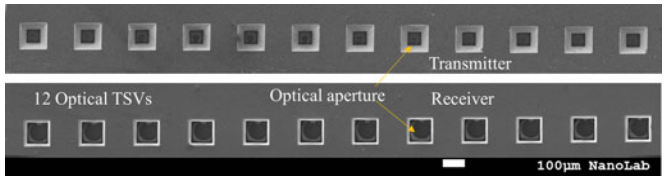

Fig. 11. SEM photos of optical TSVs and optical apertures; 12 funnel shape TSVs for transmitter (up) and 12 vertical TSVs for reveiver (down).

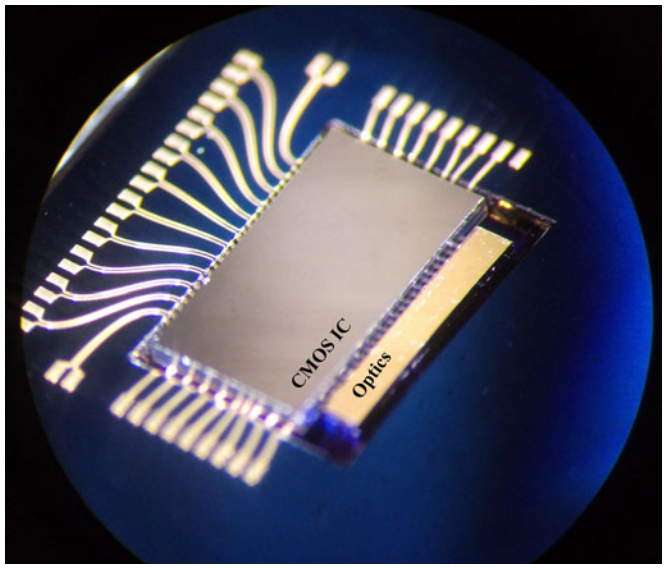

Fig. 12. Photograph of one of optical assemblies, taken under microscope.

We make the gold-gold connection between the gold pads on the VCSEL and the plated bump on silicon interposer, by using the thermal compression method. Fig. 11 includes the SEM photos of the backside of the silicon interposer, after bonding the optical dies. The different optical vias of both transmitter and receiver are shown; a one side etched funnel shape TSV and double sides etched vertical TSV for VCSELs and PDs respectively. The distance between TSVs is 250 μm, and hole dimensions are 100 μm on each side. The apertures of VCSEL and PD are visible through the TSVs.

The VCSEL driver and TIA/LA are placed and attached using a reflow process on the die bonder. The photo of the complete assembly as taken under a microscope is shown in Fig. 12. As designed, the optical die and its CMOS part are put side by side and they are embedded in the silicon interposer.

Finally, the MOI is mounted on the backside of the silicon interposer with the same pick and place tool. During passive alignment, the optical TSVs and the lenses on MOI are acting as the reference. Then, the PRIZM LightTurn ferrule, connected with standard MTP connector, can be easily coupled and reused through the latches on the MOI.

During the various assembly steps, passive alignment (with camera) is used. The pad pitch of the dies is 125 μm, and the diameter of the lenses is 250 μm. This means that standard high-throughput tools with ± 10 μm accuracy can be employed for the assembly of these sub-assemblies.

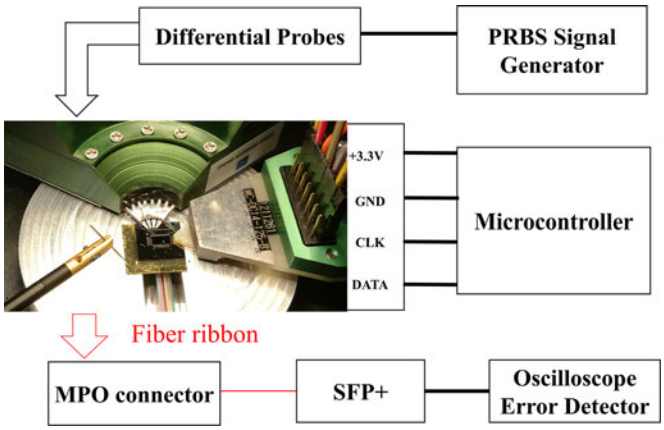

Fig. 13. Scheme of testing setup for transmitter module, inserted photo includes transmitter module, differential probes and DC probes.

VI. Testing Results and Discussion

Signal integrity tests are performed to evaluate the transmitter and receiver assemblies. The testing setup is shown in Fig. 13. The control pads on the silicon interposer from the CMOS IC are connected to a microcontroller via DC probes, and the chip is driven with a 3.3 V power supply. The internal registers of the CMOS IC, which are used to control the chip, can be programmed through two wires communication interface. Multiple differential RF probes (signal-signal) are connected to the fan-out pads of the silicon interposer. The standard MTP connector is connected to the fiber ribbon array on the other side. Finally, a multimode fiber is connected to a commercial SFP+ module (AFBR-709SMZ from Avago), through a multi-mode optical attenuator, used as a high speed light source or detector.

A. Transmitter Testing

The 12.5 Gb/s differential signal, with PRBS $2^{31}-1$ sequence, is fed into the fan out pads on the interposer through an RF probe channel by channel. The converted output electrical signal from SFP+ can be visualized on the oscilloscope. The eye patterns of 11 channels, excluding channel 7, together with SFP+ measurement, are shown in Fig. 14. Channel 7 is affected by a short circuit at its input which occurred during the reflow process on the CMOS IC. As will be shown for the receiver assembly below, by controlling the distance between CMOS and interposer during reflow, this issue can be solved. In addition, in industrial case, it will not be an issue, as soldering is often performed in a formic acid atmosphere without any pressure on top of the CMOS die.

During the bit error rate (BER) testing, all of the channels are turned on, and one input with 10 Gb/s PRBS $2^{31}-1$ sequence is fed into the channels one by one through an RF probe. The optical outputs are detected with the SFP+ receiver and fed into the error detector. The testing results, together with performance of SFP+ own transmitter, acting as a reference, are shown in Fig. 15. The deviation of the receiver sensitivity when operating the 11 VCSEL channels is 1.0 dB, with the worst performance associated with the side channels (10, 11). This may be due to the small variations in the ohmic resistance after the compression bonding of the VCSELs, which may have resulted from non-uniform force at the edges. We also test the crosstalk of three adjacent channels. Channel 1, 2, 3 at one corner of the design are selected and are all fed with a 10 Gb/s PRBS $2^{31}-1$ sequence by multi RF probes and 3 independent pattern generators. The BER curves of channel 2 are drawn in Fig. 16, comparing one channel, two channels and three channels operation mode. The results show that impact on the performance of channel 2 is below 0.2 dB in receiver sensitivity which is within the power measurement error.

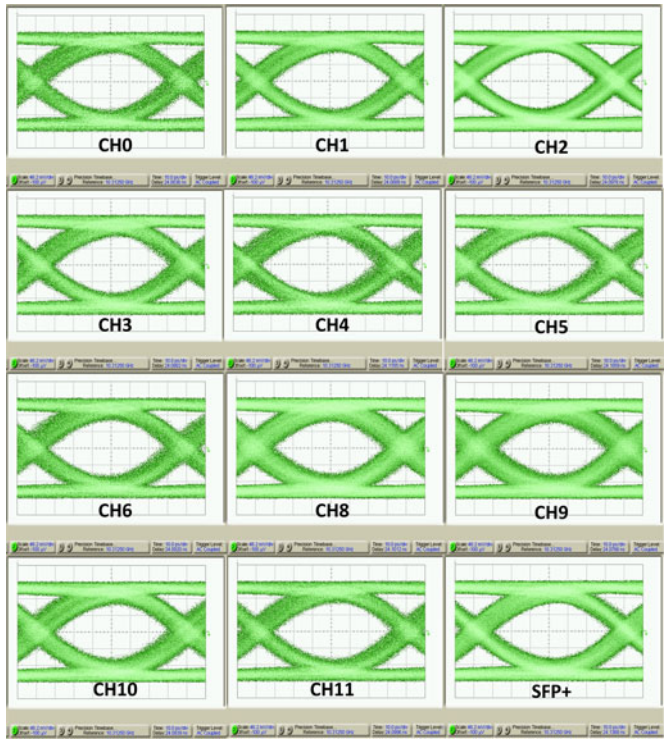

Fig. 14. Eye patterns of 11 channels and SFP+ in the transmitter test.

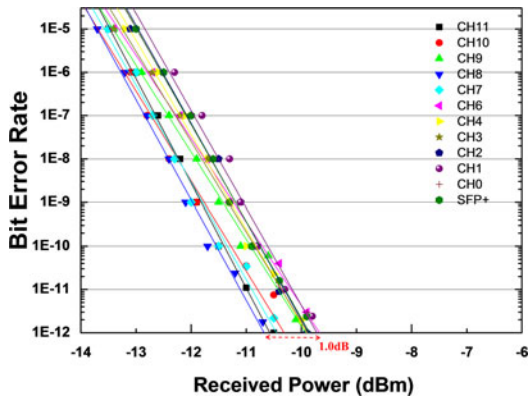

Fig. 15. The fitted BER curves for each channel and SFP+ in transmitter test.

B. Receiver Testing

For the receiver testing, we use the same setup. Optical signals with 10 Gb/s PRBS $2^{31}-1$ sequence, are generated by the transmitter of the same SFP+. The input optical power is set

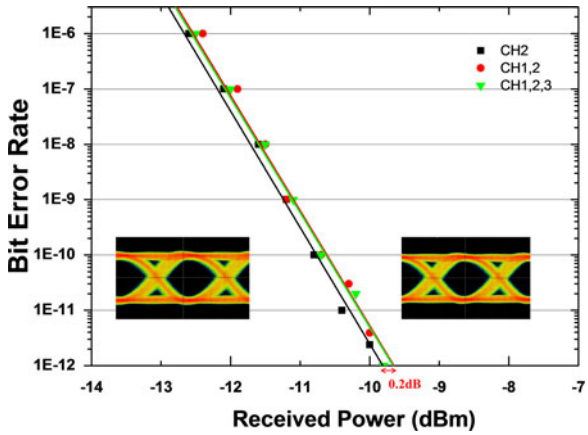

Fig. 16. The BER curves of channel 2 of transmitter module, when channel 2 alone, channel 1 and channel 2, three of channels are fed with differential signal.

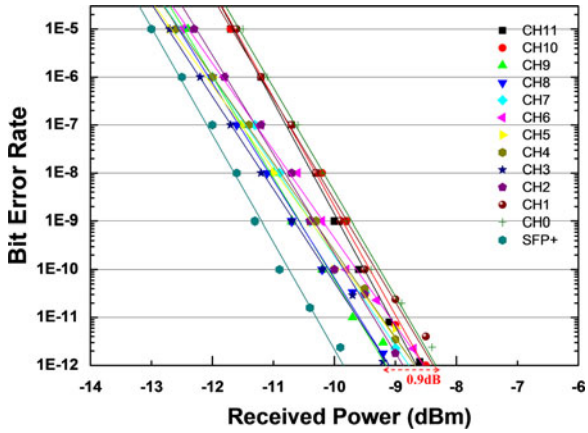

Fig. 18. The BER curves for each channel and SFP+ in receiver test.

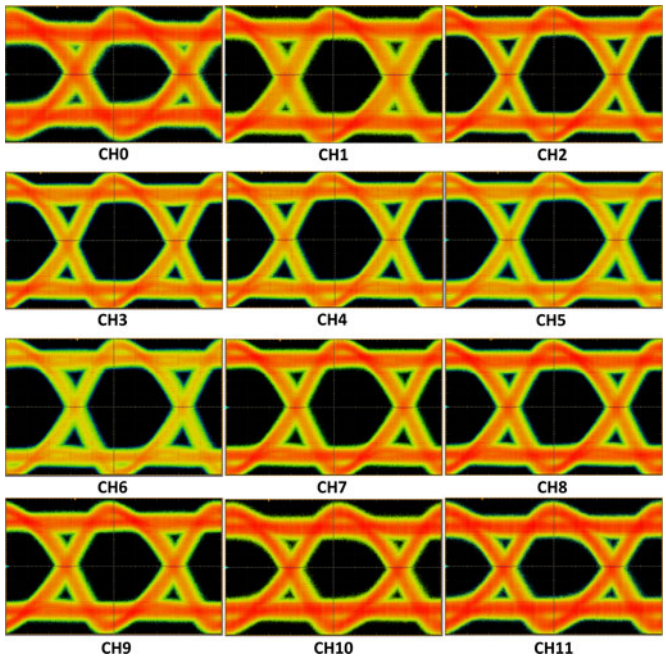

Fig. 17. Eye patterns of 12 channels of receiver working at 10 Gb/s.

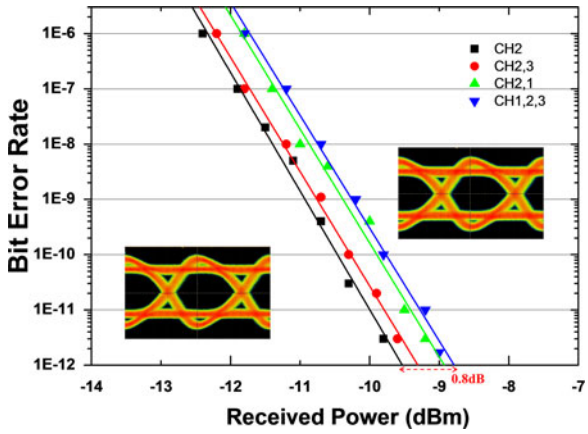

Fig. 19. The BER curves of channel 2 of receiver module, when channel 2 alone, channel 1 and channel 2, channel 2 and channel 3, three of channels are fed with optical signals.

to -6 dBm for both test module and SFP+ (back to back) to measure the eye patterns. The pre-emphasis function is enabled to optimize the differential output. The converted differential output electrical signal by receiver module is visualized on the oscilloscope, with one port terminated with 50 Ω. The eye patterns of 12 channels are shown in Fig. 17 and they are all clearly opened.

The BER testing is also performed on the receiver module, and the measured results are shown in Fig. 18. All 12 channels show a penalty distribution of only 0.8 dB. This might also be due to the higher pressure at the corner during thermal bonding. Besides, misalignment of MOI in vertical and horizontal directions may also contribute to the spread in performance. The actual receiver sensitivity value can be compensated with an additional 1.5 dB, because of the coupling losses of the light turning system, comparing with the SPF+ receiver.

Crosstalk is also tested on the receiver module. We generate 2 optical signals, with 10 Gb/s PRBS $2^{31}-1$ sequence using a CXP module connected to a 64 port 10 Gb/s switch system and feed them to the inputs of channel 1 and channel 3, while testing the performance of channel 2 using an error detector module with differential inputs. As shown in the Fig. 19, there is little impact (0.2 dB) on the performance of channel 2, if channel 3 is switched on. However, when we turn on channel 1 we see a 0.6 dB impact on receiver sensitivity. We repeat our testing on the other channels, and find that there is always 0.6 dB additional penalty on the same side, which is the longer traces side of differential trace. This suggests that the differential traces should be designed as coupled lines to maintain the desired impedance. The crosstalk can be further suppressed by adding ground planes between the differential pads. We further generated more optical signals and fed them into other non-adjacent channels, but no further impact on the performance of tested channel was observed.

We also measured receiver eye opening (often referred to as bathtub curve) for PRBS $2^{31}-1$ pattern, with the two different received power levels, at -7.0 dBm and -10 dBm, for both transmitter and receiver. As shown in Fig. 20, at -10 dBm

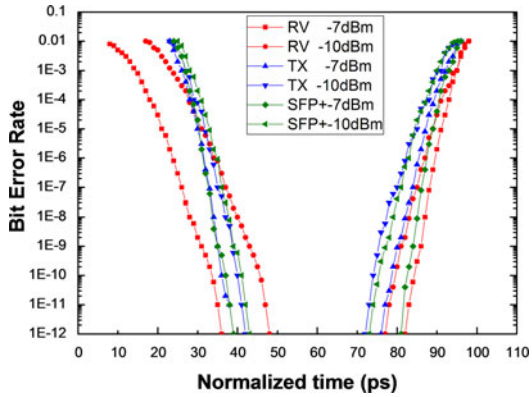

Fig. 20. Receiver eye opening (bathtub curve) at the receiver output operation for received power at −7.0 dBm and −10.0 dBm.

level, the transmitter and the receiver shows similar time margin with the SFP + (30 ps) module. At −7 dBm level, our proposed receiver sub-assembly shows a wider time margin (47 ps) thanks to the exploitation of the pre-emphasis function.

VII. Conclusion

The optical transmitter and receiver sub-assemblies have been packaged by assembling optical and electrical chips on a wet etched silicon interposer, to demonstrate a compact array of 12-channel receiver and transmitter. The impedance matched connections are designed in ADS and fabricated by lithographic processes on a large topography surface. Wet etched optical openings are designed for coupling light in and out of the VCSEL and PD dies. The design of electrical and optical connections can be used for next generation optical transceivers working at higher speed. The electrical traces have been both numerically simulated and tested and show excellent performance up to and including 50 GHz analog bandwidth and 28 Gbaud PAM-4 signaling.

The sub-assemblies have been tested. Clear transmission eye patterns up to 12.5 Gb/s and receiver eye patterns up to 10 Gb/s, as well as power penalty spread of less than 1.0 dB are demonstrated. The spread in BER curves may be caused by excessive pressure during thermal compression bonding, which can be solved by adopting ultrasonic bonding. Channel crosstalk is only observed for the receiver assembly and is lower than 0.8 dB (since measured penalty for VCSEL assembly is within power meter error). Finally the bathtub analysis is applied to both Tx and Rx sub-assemblies and performance is similar to that of a commercial SFP+ module.

In future designs, we aim to further improve the performance and bit-rate of this assembly technology by including ground planes between differential channels to further suppress the crosstalk and multiple rows of electrical fan out pads will be designed to achieve shorter redistributed traces and transmission lines with equal lengths.

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Authors' biographies not available at the time of publication.