

Exploring the PowerDAC : an asymmetric multilevel approach for high-precision power amplification

Citation for published version (APA):

Caris, M. L. A. (2016). *Exploring the PowerDAC : an asymmetric multilevel approach for high-precision power amplification*. [Phd Thesis 1 (Research TU/e / Graduation TU/e), Electrical Engineering]. Technische Universiteit Eindhoven.

Document status and date:

Published: 30/11/2016

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

Exploring the PowerDAC

An asymmetric multilevel approach for
high-precision power amplification



This research is part of and funded by the THOR project. The project is supported by two large European research support programmes: CATRENE and EURIPIDES

First edition, published 2016

Printed by Gildeprint

Cover design by Ruben Hekkens

Artwork by **The***BruceDickinson* productions

Copyright © 2016 by M.L.A. Caris. All rights reserved

A catalogue record is available from the Eindhoven University of Technology Library

ISBN: 978-90-386-4181-2

Exploring the PowerDAC

An asymmetric multilevel approach for
high-precision power amplification

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit
Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens,
voor een commissie aangewezen door het College voor Promoties, in het
openbaar te verdedigen op donderdag 30 november 2016 om 16:00 uur

door

Marcus Leonardus Anna Caris
geboren te Heythuysen

Dit proefschrift is goedgekeurd door de promotoren en de samenstelling van de promotiecommissie is als volgt:

voorzitter:	prof.dr.ir. J.H. Blom
promotor:	prof.dr. E.A. Lomonova
copromotoren:	dr.ir. H. Huisman dr.ir. J.L. Duarte
leden:	prof. M.A.E. Andersen (Technical University of Denmark) prof. P. Mattavelli (University of Padova) prof.dr.ir. E. Cantatore
adviseur:	dr.ir. J.M. Schellekens

Het onderzoek dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

Summary

Exploring the PowerDAC

An asymmetric multilevel approach for high-precision power amplification

This thesis investigates the fundamentals and principles of the PowerDAC, a new approach for improving the performance of precision power amplifiers. The justification is found in industry, as a steady demand exists for the development of ever more powerful precision amplifiers. In various application areas, such as MRI and lithography, the tendency is that the requirements set on power rating, and at the same time the requirements of the relative accuracy of the generated signals, are increasing. A related issue is that the bandwidth of the controlled amplifier needs to increase, which implies that ever higher switching frequencies are demanded. Without a breakthrough in technology, this would lead to even higher switching losses, translating into a major cooling effort and large, heavy systems.

In recent years, in power electronics research, this issue has led to the development of multilevel circuits. By connecting switching cells in series or parallel, individual device stresses are reduced. Furthermore, the resulting multicell topologies allow for the generation of a multilevel waveform. Some multilevel circuits are constructed in such a way that it is possible to use synchronous but out of phase pulse-width modulation among the devices, leading to a multilevel waveform which has a higher effective switching frequency. This high-frequency multilevel waveform results in the decrease of passive components in the output filter of the power converter, potentially increasing its performance.

Besides the development of multilevel circuits, yet another ongoing trend is the further digitization of electronic circuits. And, what is found is a fusion of the process of digital-to-analog conversion and the process of power amplification. In the PowerDAC, the line of both of these trends is followed, and the quest is continued in exploring the possibilities for creating high-level circuits. As a result, the PowerDAC can be seen as the finalization of the integration of DAC and power amplifier, hence its name.

For the PowerDAC multiple solutions may be suitable and therefore, first, for the various multilevel circuits that already exist, a classification, or taxonomy, is proposed. By means of such a classification the multicell circuits can be categorized. It is shown that dual and symmetric relations exist among the different multicell families. Additionally, in the introductory section, a gradient amplifier, being one of the applications in which the PowerDAC may eventually be applied is explored in detail and a basic simulator is realized to give an indication of how distortions in the gradient current affect image quality. Such a tool can be used to find out the most important aspects in the design of such amplifiers and to assist in setting up the specifications.

The main contribution of this thesis lies in the synthesis of a topology, including a control/modulation scheme, by which a high-level multilevel waveform can be created. This topology consists of a number of subsequent power stages, in which each cell has half the voltage and twice the switching frequency of the preceding cell. Compared to the conventional two-level approach, the power stage has been extended in such a way that the output filter can be reduced or even eliminated. Compared to a multilevel approach, the topology can be seen as an alternative solution which allows the creation of a high number of voltage levels with a limited amount of switching devices.

Other contributions of this thesis include the establishment of two control techniques for flying-capacitor power amplifiers. In this part, specific attention is given to the decoupling of the control objectives, that is, on one side the regulation or tracking of the desired output voltage reference, and on the other side the balancing of the capacitor voltages. Also, for interleaved power amplifiers that suffer from non-idealities among output inductors, a harmonic elimination technique, based on the adaption of the phase-shift, is found.

In this thesis, all theories that are proposed are fully supported by means of simulation and experimental results. Furthermore, a proof-of-concept prototype is designed and realized, which is used to demonstrate the capabilities of the PowerDAC concept.

Contents

Summary	v
I Introduction and Background	1
1 Amplifying signals by processing power	3
1.1 Background	3
1.2 Reconstructing a digital signal	5
1.2.1 Signals	5
1.2.2 Perfect reconstruction	6
1.2.3 Practical reconstruction	7
1.3 Power amplification of digital signals	8
1.4 PowerDACs	10
1.4.1 Applications	12
1.5 Outline	13
2 Effect of gradient amplifier distortion on MR images	15
2.1 Introduction	15
2.2 Nuclear Magnetic Resonance basics	16
2.2.1 Proton magnetic moment	18
2.2.2 Precession of the proton magnetic moment	19
2.2.3 Magnetization	20

2.2.4	Retrieving the MR signal	21
2.2.5	Signal demodulation	22
2.3	The elegance of MR: Spatial encoding	23
2.3.1	Slice selection	24
2.3.2	Frequency encoding and 1D imaging	24
2.3.3	Phase encoding and 2D imaging	26
2.4	Image reconstruction	27
2.4.1	Gradient echo	27
2.4.2	Image formation	29
2.4.3	k-space	30
2.5	The gradient system	30
2.5.1	Relation between current and magnetic field	31
2.6	Creating a simulation tool and results	35
2.6.1	Output current distortions	35
2.7	Conclusion	40
II	Episteme	41
3	Exploration and categorization of multicell circuits	43
3.1	Introduction	43
3.2	Basic concept of multilevel power conversion	46
3.2.1	Generation of multilevel PWM waveforms	48
3.2.2	Multilevel and quantization distortion	50
3.2.3	Multilevel and sampling distortion	51
3.2.4	Multilevel and output filter reduction	52
3.3	Taxonomy	53
3.3.1	Technological domains and fields	54
3.3.2	Classes	55
3.3.3	Families	56
3.3.4	Variants	61
3.4	Symmetric and dual relations	63
3.4.1	The duality principle and dual converters	65
3.4.2	Application of the duality principle	67
3.4.3	Simulation results	71
3.5	Summary	75
4	Synthesis of a PowerDAC	77
4.1	Introduction	77
4.2	Definitions	79
4.3	Modulation strategy - open loop	84

4.3.1	Calculation of the duty cycles	86
4.3.2	Alternative modulator	86
4.4	Modulation strategy - closed-loop balancing	87
4.4.1	Adjusting duty cycles	91
4.4.2	Adjusting phase-shift	92
4.4.3	Limiting the adjustments	93
4.5	Basic comparison with other multicell topologies	94
4.5.1	Switching devices and stress-factor	94
4.5.2	Capacitors	96
4.5.3	Discussion	96
4.6	Simulation results	97
4.6.1	The ideal PowerDAC and the influence of capacitors	99
4.6.2	Natural balancing of capacitors	101
4.6.3	Closed-loop balancing	102
4.6.4	Unipolar and bipolar switching	103
4.6.5	Dead time	104
4.7	Summary	106

III Techne 107

5	Modeling and control of series multicell converters	109
5.1	Introduction	109
5.2	Modeling	111
5.2.1	Averaging switched model	112
5.3	Input-output decoupling by feedback linearization	116
5.3.1	System transformation	116
5.3.2	Input-output decoupling	119
5.3.3	Linearizing control law	120
5.4	Decoupling by vector PWM	120
5.5	Control design	123
5.5.1	Output voltage control by full-state feedback with LQR	124
5.5.2	Linear PI control	126
5.5.3	Prevention of saturation effects	127
5.5.4	Output current singularity	127
5.6	Simulation results	128
5.7	Conclusion	130
6	Impact of asymmetries in parallel multicell converters	133
6.1	Introduction	133
6.2	Interleaving	135

6.2.1	Effect on higher number of cells	136
6.3	Theory	138
6.3.1	Fourier series of a triangular wave	138
6.3.2	Improved phase-shift - Analytic description	139
6.3.3	Improved phase-shift - Geometric visualization	141
6.3.4	Iterative phase-shift calibration	142
6.3.5	Modified Newton's method for small deviations	144
6.4	Simulation results	144
6.4.1	Results for five interleaved cells	145
6.4.2	Harmonic distortion for five interleaved cells	147
6.5	Summary	149
7	Experimental results	151
7.1	Introduction	151
7.2	Experimental results of PowerDAC	152
7.2.1	Gate signaling	153
7.2.2	Output voltage and output current	153
7.2.3	Capacitor balancing	156
7.3	Closed-loop control for flying-capacitor converters	156
7.3.1	Feedback linearization with LQR	157
7.3.2	Vector decoupling with PI control	158
7.4	Harmonic elimination in parallel converters	158
7.4.1	Results for five interleaved cells	159
7.4.2	Output current	162
7.5	Discussion	163
IV	Closing	165
8	Conclusion and discussion	167
8.1	Conclusions	167
8.2	Original contributions	168
8.3	Recommendations and future research	170
	Appendices	173
A	Nomenclature	175
A.1	Symbols	175
A.2	Subscripts	176
A.3	Notation	177
A.4	Acronyms	177

B	Definitions	179
B.1	Fourier series and transform	179
B.1.1	Fourier series	179
B.1.2	Complex Fourier series expansion	180
B.1.3	Fourier transform	181
B.1.4	Band-limited functions	182
B.2	Lie Algebra	183
B.2.1	Lie derivative	183
B.3	Nonlinear control concepts	184
B.3.1	Relative degree	184
C	Design aspects of prototype board	185
C.1	Hardware aspects	185
C.1.1	DSP and controlCARD	187
C.1.2	Power stage and output filter	188
C.1.3	Gate drivers	190
C.1.4	Floating-capacitor voltage measurement	191
C.2	Software aspects	194
C.2.1	Open-loop sound play	195
C.2.2	Closed-loop algorithm implementation	195
	Bibliography	197
	Dankwoord	211
	About the author	213

Part I

Introduction and Background

Chapter 1

Amplifying signals by processing power

"I just wondered how things were put together."

(Claude Shannon)

1.1 Background

Ancient Greek philosophers, most prominent Plato and Aristotle, were thinking about knowledge and wisdom. It is them who were the first to establish the notion of different types of knowledge. An example can be found in a dialogue "Philabus" where Plato writes about a conversation between Socrates and Protarchus, dividing knowledge into two classes: one part of knowledge is productive (Techne, art), the other has to do with education and support (Episteme, science) [101, 110]. Aristotle later extends this view in "Nicomachean Ethics", giving a broader framework, and defining episteme as the knowledge that is demonstrable. Here, with demonstrable, he meant that the knowledge can be deducted from reasoning and argumentation. Episteme is universal, invariable and context-independent. Clearly, it is episteme that is closely related to the modern understanding of what science is.

Techne, for Aristotle, is an ability to make/produce with true logos (consciousness). Etymologically, it is techne, combined with logos, which is the foundation of the English word technology (Technologie in Dutch). It means that techne involves logos, not in production of artifacts itself, but in understanding how to

make them. *Techné* is, therefore, more pragmatic, variable and context-dependent. Nowadays, technology is understood as the making and using of artifacts, and we find technology in different disciplines. These disciplines are closely related to the different physical domains or forms of energy that exist in nature. One can think of, for instance, the technological domain of electrical engineering, where mechanisms are designed in which electrical energy is used. These mechanisms are constructed by the interconnection of different types of elements, source elements, dissipative elements, storage elements or switching elements. It is the electrical energy embodied in the electromagnetic field that causes motion of electrons due to the Lorentz force, and the interaction of these charged particles with the electromagnetic field is fully described by physical laws, such as the Maxwell equations. This natural phenomenon gives rise to time-dependent voltage (effort) and current (flow) waveforms that can be observed.

One of the two main aspects for which we use electrical energy is to do the work that we are not able or not willing to do ourselves. Electrical energy in its pure form is not very useful. There exists, however, a variety of loads in which electrical energy is transformed into for example mechanical or thermal energy to provide the needs for our daily lives. Take for example the transformation into rotational or translational motion with a motor or actuator, or the transformation into motion of air molecules by using a loudspeaker, energy that can be observed as sound. Another example would be the transformation into motion of photons, electromagnetic radiation, which may be observable as visible light for a certain band of frequencies or being used to heat up food in a microwave. It should be kept in mind that conversion does not necessarily take place from one physical domain to another, sometimes it is desired to transform the electrical energy from one voltage, current, frequency into another voltage, current, frequency [100]. It is, within electrical engineering, the field of power electronics that analyzes and designs the systems that perform this function: power converters.

The other aspect for which electrical energy can be used, is the interpretation of voltage, current or power waveforms as signals. Fundamentally, signals possess information, and it gives us the possibility to use electrical energy for communication purposes. Analysis and processing of signals is, therefore, an essential element in electrical engineering, and it is covered by the field of signal processing. The Fourier transform can be seen as the most profound and versatile tool for performing the analysis. Moreover, the transformation forms the basis for one of the most astonishing and elegant theorems in electrical engineering, the sampling theorem. This theorem states that there exists a class of signals that can uniquely be represented in terms of its samples. As such, it allows for the conversion from the analogue to the digital domain and vice versa, as it is sampling that

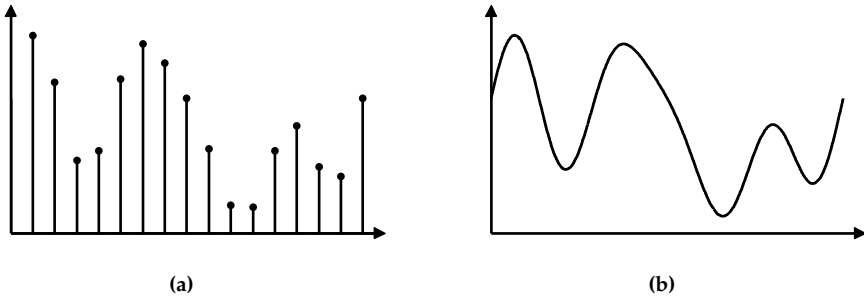


Figure 1.1: Example of (a) a discrete signal and (b) a continuous signal.

forms a crucial and first step in the digitization of signals. Nowadays, information is processed in electronic devices mostly in a digital environment, because digitization offers a number of advantages, such as the ability to transfer and store information losslessly [23]. Subsequently, it may not be a surprise that both digitization and reconstruction of analog signals are crucial and essential tasks in many electronic systems.

1.2 Reconstructing a digital signal

1.2.1 Signals

A signal, in general, is defined as a function or a sequence of values that represents information [50]. A signal, of which an example is depicted in Figure 1.1, could represent for instance a voltage or current varying in time. However, it could also represent the proton spin density varying in a certain spatial direction. Signals are, without any context, therefore, very generic. In signal processing, two types of signals can be distinguished. In Figure 1.1(a) an example is shown of a discrete signal and in Figure 1.1(b) a continuous signal is shown. Mathematically, the difference between continuous and discrete can be understood by the notion of countability, meaning that when $t \rightarrow \infty$, the discrete signal belongs to a countably infinite set, while the continuous signal belongs to an uncountably infinite set. Conceptually, it means that a discrete signal can be put in a list, or, to put it differently, that there exists a bijection or one-to-one correspondence between the signal and the set of all integers \mathbb{Z} . For a continuous signal there exists a bijection with all real numbers, \mathbb{R} .

A digital signal is a specific type of discrete signal, defined as a set of quantized

discrete samples. This implies that the signal can be represented on a computer system as a sequence of binary numbers. The most basic format for storing a digital signal on a computer system is pulse-code modulation (PCM), and the data is embodied with two parameters, bit depth n_b and sample frequency f_s (or its reciprocal the sample time T_s). These two parameters provide enough information about how the collection of binary numbers should be interpreted. A digital signal may be created in two manners, either directly on a computer by a software script or by digitizing an analog signal which involves the processes sampling (time discretization) and quantization (amplitude discretization).

The reverse process, the conversion of a digital signal into an analog physical quantity is accomplished with an electronic device called a Digital-to-Analog Converter (DAC). A DAC is fundamentally based upon the sampling theorem of Shannon, since the sampling theorem on information states that a continuous band-limited signal can be replaced by a sequence of values without loss of information [63]. The Fourier transform can be used as a tool to prove this statement (see Appendix B).

1.2.2 Perfect reconstruction

Following Shannon's theory, one of the methods by which perfect reconstruction of a discrete signal can be achieved is by using the "Whittaker-Shannon" equation [87]

$$s(t) = \sum_{k \in \mathbb{Z}} s[k] \cdot \text{sinc}\left(\frac{t - kT_s}{T_s}\right). \quad (1.1)$$

The equation is a result of a convolution of the samples with a sinc-function, the latter being the inverse Fourier transform of an ideal low-pass filter. Note that the equation is an infinite sum over all positive and negative numbers. In Figure 1.2 the reconstruction of the sample waveform from Figure 1.1 is illustrated. It can be seen that each sinc-function is placed in such a way that its maximum value exactly corresponds to a sample value, while the function is zero at all the other sample instances. In an ideal DAC the modulator outputs a pulse train of samples and an ideal low-pass demodulation filter is used to generate the original signal. It should be mentioned that such an ideal filter is non-causal, and has infinite delay. Theoretically, however, the result is identical to the reconstruction with the "Whittaker-Shannon" equation.

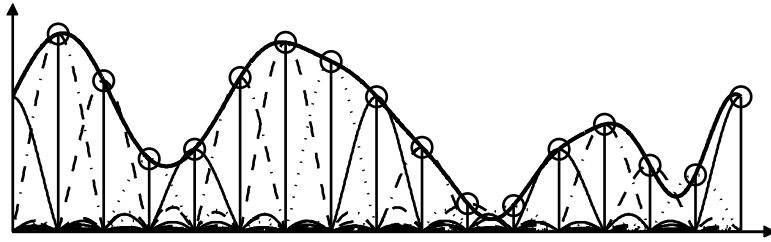


Figure 1.2: Visualization of perfect reconstruction by means of the Whittaker-Shannon equation applied to the signal shown in Figure 1.1.

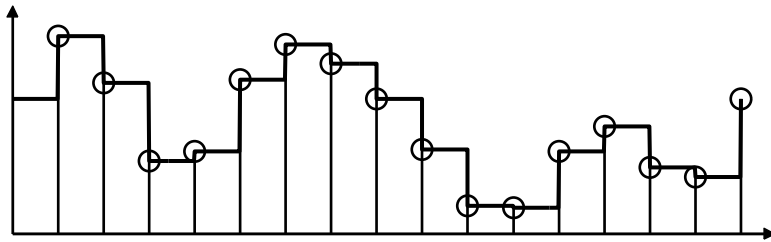


Figure 1.3: Visualization of the zero-order hold reconstruction technique as often employed in practical DACs.

1.2.3 Practical reconstruction

It is obvious that a perfect reconstruction technique cannot be realized exactly in practice. In a realization, it is tried to closely approximate the behavior of an ideal DAC. Instead of using a pulse train of samples, often a data hold approximation is applied. A data hold reconstruction is characterized by a certain order, and for a zero-order hold each sample is held exactly one sample time, as is shown in Figure 1.3. Also, in a practical application, instead of an ideal filter, a practical filter is used, which is not eliminating, but reducing the higher-frequency components. Finally, time discretization was shown to be the foundation of perfect reconstruction. Amplitude discretization or quantization, on the other hand, leads to unrecoverable noise, and it is inherently given by a digital input signal. As a result, due to quantization, an ideal discrete signal is not realizable and a limitation exists on the maximum attainable quality, expressed in signal-to-noise ratio (SNR), that can be achieved, and given by the number of bits. The signal-to-noise ratio in dB is found to be approximately six times the number of bits of the digital input signal [123]. As an example, for a 16-bit digital input signal the maximum achievable signal-to-noise ratio is approximately equal to 96 dB.

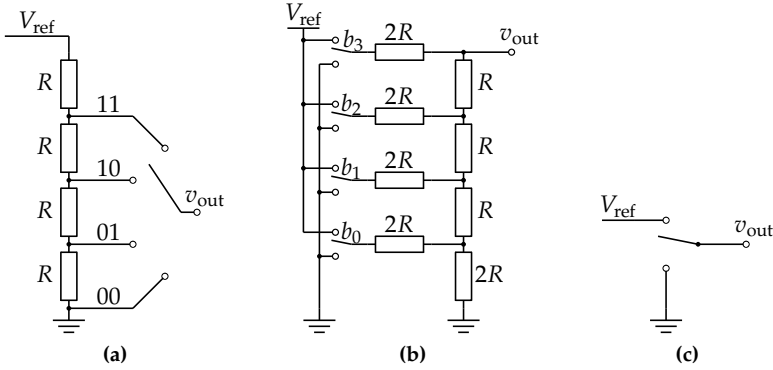


Figure 1.4: Three commonly used DAC structures: (a) A string DAC (b) an R2R DAC and (c) a 1-bit sigma-delta DAC.

One possible way of realizing a ZOH DAC in practice is by using resistors and configuring them as shown in Figure 1.4(a). This configuration is also known as a string DAC, and an arbitrary reference voltage V_{ref} is divided proportional to create the voltage levels, as all resistor values are assumed to be equal. The desired output voltage V_{out} is simply selected with an SPMT switch. Variations of this approach exist with other switch configurations or with segmented structures [68]. Other arrangements with different resistor values are also possible, such as a binary-weighted structure. A popular alternative is the R2R DAC, shown in Figure 1.4(b).

For higher power applications it is difficult to generate all the individual voltage levels. Also, resistive elements should be avoided, as resistors dissipate power. An alternative approach is to spread the noise by oversampling and use noise shaping to move the remaining noise towards higher frequencies. This technique can be extended to the limit, until eventually only one bit is left. In a 1-bit DAC no resistors are required anymore, and the output waveform is created by a single switch, as is shown in Figure 1.4(c). A DAC which uses this approach is also known as a sigma-delta DAC. Note that, due to noise shaping, an output filter becomes an essential element in a sigma-delta DAC.

1.3 Power amplification of digital signals

Very often, a DAC itself is not able to deliver sufficient power for driving a load. For this reason, a DAC is generally accompanied by a power amplifier. A power

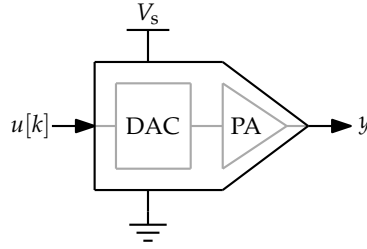


Figure 1.5: Schematic representation of a digital power amplifier in its simplest form: a system that consists of a power amplifier (PA) and a digital-analog converter (DAC). The output is defined as an analog electric signal, which can either be a current or a voltage.

amplifier is an electronic device in which a signal is amplified by using a power converter. While in most systems there is a clear distinction between the part which is performing the digital-to-analog conversion and the part which is performing the amplification, as systems evolve, the distinction between these two separate parts has become more vague. In Figure 1.5 a block diagram of a generic digital power amplifier is shown. An input signal u is defined representing a band-limited reference signal. An external power supply is connected to the power amplifier and its voltage is defined as V_s . The main goal of this system is to generate the output waveform y representing the input signal as accurately as possible.

A classical converter topology, which is commonly used in the design of a power amplifier, is based on a two-level class-D amplifier. The approach is very similar to a 1-bit sigma-delta DAC and the switch is constructed by a power stage consisting of two active switch devices (e.g. MOSFET or IGBT) which are operating in on-off mode. Consequently, the output voltage has a square waveform, because the stage switches between the positive and negative rail of the supply voltage. An idealized power converter is directly converting the pulse-density modulation (PDM) signal into an output voltage. Hence, it is necessary to carefully analyze the applied PDM as it contains information about the added harmonic distortion to the desired waveform, often a measure for the accuracy.

In practice, the switching devices require a finite time to go from the conductive to the non-conductive state, and, a certain loss is experienced during every switching action. Not surprisingly, in power-electronics research, especially those used in applications in which a high efficiency is desired, engineers search for zero-voltage or zero-current switching approaches. Similarly, the total number of switching actions within a given amount of time, which is related to the total losses of the converter in terms of switching losses, needs to be analyzed as well. As a consequence, other PDM methods than sigma-delta modulation have been

searched for, and most often a fixed-frequency PDM technique is used. The latter approach, in which a reference is compared to a carrier wave, is better known as pulse-width modulation (PWM).

The desired output voltage waveform can be obtained from the pulse-width modulated square wave by means of a demodulation process by placing a filtering part consisting of reactive elements after the power stage. The filter is used to suppress unwanted spectral components and to fulfill the requirements on EMI and on the relative accuracy of the desired waveform. Most commonly used as filter is a second-order filter which consists of a series inductor and a shunt capacitor.

Filters in power amplifiers, however, can be seen as an unwanted necessity. First, because during the design of this filter there will always be a trade-off between the transient state and steady-state requirements of the total system. And, second, besides this trade-off, filter components can contribute up to 40% of the weight or volume of such amplifier systems, adding to the total cost. For these reasons, in power-electronics research, new approaches in power amplification have been investigated. One straightforward solution is to increase the switching frequency. However, increasing the switching frequency translates into a major cooling effort and large, heavy systems. Combining these observations one finds that there exists a deliberation on finding the optimal balance between power, efficiency and accuracy for a specific design of a power converter.

The focus of attention has, therefore, been set on the extension of the power stage in such a way that the output filter can be reduced or even eliminated. By putting switching devices in series or parallel, device stresses can be reduced. When, simultaneously, "smart" modulation strategies are applied, multilevel waveforms can be created, and the full advantages of the topologies are exploited to benefit the most.

1.4 PowerDACs

The multilevel strategy features an interesting property. Namely, the ability to create a waveform analogous to the way a ZOH DAC would do. However, the conventional topologies have certain limitations, as the number of voltage levels is still low in practice. As shown in chapter 3, one of the problems is that the number of components scales linearly with the number of voltage levels. For a high number of levels, size and complexity increase, after which, at a certain point, the topology becomes unfeasible for realization.

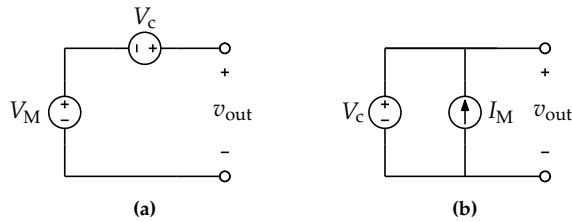


Figure 1.6: Two possible configurations for the realization of a PowerDAC with a voltage output. When the main amplifier is designed in such a way that it delivers on average the output power, then no additional supply is required for the correction amplifier.

The approach used here, in contrast to that what has already been done in the field of multilevel and interleaving, is that the creation of a multilevel circuit by interconnecting switches or sub-circuits (cells) in series or parallel is expanded by giving the sub-circuits a specific function or task. That is to say, that one amplifier system can be created by combining two amplifier stages in which one of the amplifier stages is concerned with delivering the bulk power while another amplifier stage is used for fine-tuning the output waveform. Such composite amplifiers have been investigated in the past, where the amplifier stages are called main amplifier and correction amplifier. It might be interesting to note that similar approaches are found also in other fields of engineering. As an example, in a large mechatronic system, such as a wafer scanner system, the wafer stage is built using a long- and short stroke actuator. The long-stroke actuator may have a limited precision of approximately 1 mm, while the short-stroke actuator performs at sub-nanometer precision [104].

An example of a composite amplifier is the combination of a main class-D power amplifier in combination with a linear correction amplifier. The main power amplifier is designed for delivering the power to the load and the correction amplifier is designed to correct for the remaining error. In other words, instead of focusing on one power amplifier which has to deliver all the power at a very high accuracy, the amplifier is split up into two parts. This concept has been theoretically analyzed by Yundt [152, 153] and he concluded that there are basically 4 possible implementations of such a composite amplifier. Two of them are shown in Figure. 1.6 and both of them are characterized by having a voltage output. The other two variants have a current output and can be seen as the dual version.

It is exactly this concept (composite amplifiers) in which both the main amplifier and correction amplifier are to be realized with a switched-mode amplifier that forms the basis of the PowerDAC idea. When the main amplifier is controlled in such a way that it delivers on average the power to the load, then the correction amplifier does not need to deliver any continuous power and the amplifier could

be implemented without a power source. In other words, it means that capacitors can be used for the creation of the voltage levels. When asymmetrical voltage levels are to be chosen; for instance, "binary-weighted", such as in a R2R DAC, a high number of voltage levels can be created with a relatively low amount of components. Additionally, since voltage levels in these correction amplifiers are lower, switching frequencies can be higher.

The PowerDAC can thus be seen as the finalization of the integration of a DAC and a power amplifier (as was depicted in Figure 1.5), where the power stage is extended with the intention to reduce or eliminate the output filter. With the use of a composite amplifier, a high-level correction amplifier can be designed that consists of a set of dissimilar series-connected power stages each having a different switching frequency and capacitor voltage (e.g. binary-weighted as in an R2R-DAC).

1.4.1 Applications

The PowerDAC concept can be employed in different applications. One can think of for example audio, lithography and Magnetic Resonance Imaging (MRI). In such systems the PowerDAC idea would be an alternative solution for the existing power amplifier. Although the applications share the primary task to generate a high-precision waveform, some important differences may be recognized, such as their main purpose and load characteristics. For audio, the (high-fidelity) power amplifier is required to convert the digital information into electrical energy for driving a loudspeaker to produce sounds. In actuator or motion systems a power amplifier is necessary to produce the electrical energy that is required to drive an actuator. In MRI, a power amplifier is required to spatially encode the hydrogen protons.

Another major difference between the listed applications is power rating, which translates in different power-electronics solutions that are most commonly applied. In MRI, multilevel topologies are already used, simply because a two-level approach is not feasible. In a digital audio amplifier, on the other hand, a multilevel approach is very unusual, although some first attempts have been published recently [107]. The two-level approach, here, remains still simple, cheap and over the years this approach has been optimized to the limit. Next to power rating, some applications may have the requirement to be "real-time". In other words, the reference is either predetermined (MRI) or determined by an outer closed-loop system (motor control). In such real-time systems a time delay is highly undesirable as it lowers the performance of the total system.

In all of these systems the power amplifier is an essential and crucial part of the signal chain and all its distortions influence the performance of the system. In a previous project, an interesting power circuit solution to get rid of dead-time effects has been found, implemented and evaluated [132]. The analysis and minimization of the distortions remains however a fundamental part in the development of new concepts for high-precision power amplifiers. In this thesis the quest for ever more powerful amplifiers is continued, with the evaluation of the PowerDAC concept.

1.5 Outline

This thesis consists of three main parts. The first part focuses on the introduction and background of the work. Starting with **Chapter 1**, in which an introduction of the PowerDAC concept is given. This chapter sets the context of the thesis and some applications in which the concept can be applied are listed. Therefore, in **Chapter 2**, one of these applications, the MRI system, is discussed in more detail and it is shown how distortions in a gradient amplifier influence the image quality. The chapter additionally contains a brief introduction in the fundamentals of MRI, which has led to the development of a simulation tool. At the end of the chapter the main results from this simulation tool are presented, as it provides a method by which the effect of gradient amplifier distortion can be analyzed.

Up to this point, one may have noticed that in this introduction not only we went from the sampling theorem to switched-mode amplifiers, we also went from ideal conversion methods to a more practical and realistic realization of a converter. It is these types of knowledge in which the virtues episteme and techne are recognized, and the remaining part of the thesis has been split up accordingly.

Episteme

Whenever we are thinking about the ideal, about linear systems, about no-ripple, we find ourselves in the domain of episteme. In this domain it is aimed to develop for instance generic theories, which is useful, because they give us a better understanding of fundamental principles. In this part, **Chapter 3** proposes a classification of multicell topologies. Also, it is demonstrated how (ideally) the generation of a multilevel waveform can be used to reduce the output filter. A taxonomy for multicell topologies is proposed and it is found that symmetrical and dual relations exist among different categories, which forms the remaining of

this chapter. In **Chapter 4** the main contribution of this thesis, the synthesization of the PowerDAC topology, is explained in detail. A large part of this chapter is devoted to the development of a modulation/control scheme for asymmetrical series-connected H-bridge converters.

Techne

In the third part the more technical aspects are discussed. In the domain of techne we find the theoretical aspects which are more oriented towards realization. Although we strive to achieve the ideal, we are confronted with practical limitations. In reality, non-idealities and sources of noise and distortion exist, which have to be taken into account and measures have to be taken to minimize their effects. These effects require attention for making the technology eventually successful. **Chapter 5** deals with series multicell converters in which capacitors are used for creating various voltage levels, and coupling between the balancing compensator and the output voltage controller is analyzed. Two decoupling methods are proposed. In **Chapter 6** the focus of attention is set on parallel converters, and the effect of unequal output inductors on the output current is analyzed. A solution is presented in the form of an improved phase-shift. Two approaches are proposed, either a pre-calculation, or a closed-loop adaptive optimization algorithm can be used. In **Chapter 7** the ideas which are developed in this thesis are verified on an experimental setup.

Finally, **Chapter 8** presents the overall conclusions, lists the main contributions, and proposes a number of elements for future research.

Chapter 2

Effect of gradient amplifier distortion on MR images

"I have not yet lost a feeling of wonder, and of delight, that this delicate motion should reside in all the things around us, revealing itself only to him who looks for it."

(Edward M. Purcell)

2.1 Introduction

In this chapter one of the applications in which the PowerDAC eventually can be applied, that is as an alternative topology for the gradient amplifier in a Magnetic Resonance Imaging (MRI) system, is explored in more detail. The gradient system is one of the key components of an MRI system, responsible for the creation of magnetic field gradients in x-, y- and z-direction and used to spatially encode the MR signal. The gradient amplifier is part of the gradient system and generates the current that flows through the gradient coil, by which these magnetic field gradients are created.

The aim of this chapter is to find out how distortions inside a gradient amplifier affect image quality. To be able to achieve this goal the fundamentals of Magnetic Resonance (MR), and the systems NMR and MRI, should be understood. However, MR is a complex process, and, therefore, first, the most essential aspects of this process are explained. There are numerous texts/books/articles available

that cover the subject matter [53,95,115,124]. However, most of the literature is either intended for a broad public (medical staff/users) or a specialized group of biomedical scientists, not specifically intended for electrical engineers in the field of electric power processing. As consequence, most of the material seems to be written with the philosophy that the addition of mathematical equations complicates the presentation. One notable exception to this statement, however, is the book "Magnetic Resonance Imaging: Physical Principles and Sequence Design" of Mark Haacke et al. [53]. As in this chapter only an introduction and summary is given, for further reading and more detailed information this book is warmly recommended.

Three aspects, regarding the image formation, are explained in more detail. First, the physical origin of the MR signals, the precession of the magnetic moment of a proton due to an external magnetic field resulting in the creation of a net magnetization and the "resonance" phenomenon, the excitation of the protons by means of an RF pulse. Resonance only occurs when the RF frequency matches the Larmor condition, so by superposing a gradient on the uniform field, the precession frequency and phase become spatially dependent. Secondly, it is explained how the magnetic field gradients can be used for the slice selection procedure and how the frequency encoding and phase encoding gradient can be used to encode the MR signal spatially. Subsequently, it is shown mathematically how the demodulated MR signal is the Fourier transform of the proton spin density. It is shown how an image can be retrieved from the raw signal data (k-space). The resulting equations form the basis of a simulation tool of which the results are presented at the end of this chapter.

2.2 Nuclear Magnetic Resonance basics

Nuclear Magnetic Resonance (NMR) is an important technique in the field of medical diagnosis and scientific research. NMR is used scientifically in the field of chemistry or spectroscopy to examine chemical properties of different materials. When the technique is used in medical applications, it is aimed to take cross-section images of the body displaying different types of tissue and one speaks of Magnetic Resonance Imaging (MRI). MRI has the greatest impact in the field of neurology. Apart from diagnosis of the brain, central nervous system, and spinal cord, where it has largely become the superior method, MRI also contributes to other fields, such as oncology, cardiovascular or abdominal imaging, and the investigation of musculoskeletal problems [73].

MRI is a tomography, which, as the name suggests, involves an assortment of



Figure 2.1: Example of an MRI scanner - Philips - Achieva 1.5T SE.

magnetic fields and a resonance phenomenon by which images can be constructed. The image formation technique includes the application of a magnetic field \mathbf{B} that consists of three components:

- A large static magnetic field, denoted as \mathbf{B}_m
- An RF field defined as \mathbf{B}_{rf}
- Three additional gradient fields, $G_x = \frac{\partial B_x}{\partial x}(\mathbf{0})$, $G_y = \frac{\partial B_y}{\partial y}(\mathbf{0})$, $G_z = \frac{\partial B_z}{\partial z}(\mathbf{0})$

The external magnetic static field \mathbf{B}_m results in a precession of the hydrogen proton magnetic moment with frequency ω_0 (Larmor frequency). The summation of the precessing magnetic dipole moments of these protons forms a net magnetization. In equilibrium the net magnetization coincides with the external field. However, a "resonance" phenomenon occurs by means of transmitting a radio-frequency (RF) pulse through \mathbf{B}_{rf} with a frequency equal to the Larmor frequency of the protons of interest, and thus RF energy pushes the net magnetization out of its equilibrium. The rotating net magnetization results in an oscillating magnetic field, which induces an emf (voltage) in a receive coil. This emf can be perceived as a signal, and when the protons have been spatially encoded by a gradient system, and sufficient measurements have been taken, an image can be constructed.

Figure 2.1 shows an example of an MR imaging scanner, the Philips - Achieva 1.5T SE [116]. This scanner has the typical "tunnel" shape, which is used most often. However, also other shapes are possible, such as the Philips Panorama series, where a patient lies in a more open environment and has a more comfortable experience. Most scanners, also from other manufacturers, have similar shape, where the main part is a cylindrical tube, since the magnetic field is created with

cylindrical coils.

An MRI scanner consists of several fundamental parts. The first part involves a large superconducting magnet, which is responsible for creating the large homogeneous field B_m , in the order of $(0.5 - 7)$ T. By convention, B_m is oriented along the z-direction. The second part is the RF system, that includes transmission coils to excite the protons, and receive coils to measure the resulting magnetization. The third part is the gradient system, which is, by superimposing a gradient magnetic field, used to spatially encode the protons. The gradient system can be subdivided further, and it comprises an input supply, a gradient amplifier, a gradient coil, but also cables, shielding and connectors.

2.2.1 Proton magnetic moment

Fundamentally, NMR is based upon the interaction of the magnetic moment of nuclei with an external magnetic field. This magnetic moment can be traced back to the subatomic particles, i.e. protons and neutrons, in the nucleus. An uneven number of protons or neutrons is a necessary condition for giving the atom a magnetic moment. The exact mechanisms that are responsible for causing the magnetic moment are still not yet fully understood, however, conceptually, the magnetic moment μ is created by an intrinsic angular momentum L or spin of these subatomic particles and a proportional relationship exists between the two physical quantities as

$$\mu = \gamma L. \quad (2.1)$$

Here, γ represents the gyromagnetic ratio, which is, by this equation, defined as the ratio between the magnetic moment and intrinsic angular momentum. Furthermore, the magnetic moment will in the presence of an external magnetic field cause a torque, which is found to be

$$\tau = \mu \times B. \quad (2.2)$$

Using classical mechanics (Newton's second law of motion), it can be shown that

$$\frac{dL}{dt} = \tau, \quad (2.3)$$

i.e. that change in angular momentum is equal to torque.

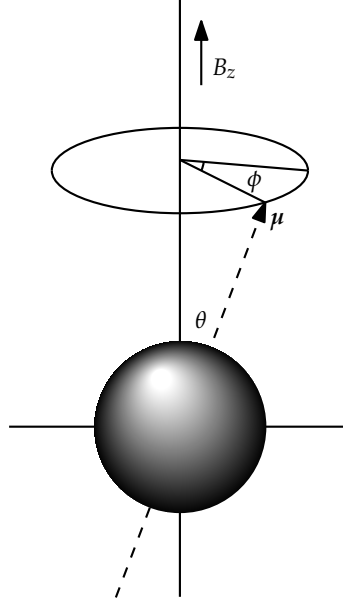


Figure 2.2: (Classical) model of a proton, illustrating the precession of the magnetic moment due to an external magnetic field.

2.2.2 Precession of the proton magnetic moment

The mathematical equations that describe the behavior of a proton in a magnetic field introduced in the previous section can be combined, resulting in

$$\frac{d\boldsymbol{\mu}}{dt} = \gamma \boldsymbol{\mu} \times \mathbf{B}, \quad (2.4)$$

which is also known as the Bloch equation in vector notation where relaxation and thermal effects are neglected. From equation (2.4) it can be derived that a change in magnetic moment $\boldsymbol{\mu}$ is, as a result of the cross product, perpendicular to the applied magnetic field \mathbf{B} and the angular momentum itself. A simplification of the equation can be made when it is assumed that i) \mathbf{B} is constant and ii) \mathbf{B} has only a z-component. This situation is depicted in Figure 2.2.

The analysis is continued further by transforming the equations into spherical coordinates. Both the magnetic field and angular momentum are then represented by their magnitude $B_r = |\mathbf{B}|$ and $\mu_r = |\boldsymbol{\mu}|$ and the line element as $d\boldsymbol{\mu} = \mu_r \sin \theta d\phi$. Solving this equation yields

$$\mu_r \sin \theta \frac{d\phi}{dt} = \gamma \cdot (|\boldsymbol{\mu}| \times |\mathbf{B}|) = \gamma \cdot (-B_r \mu_r \sin \theta). \quad (2.5)$$

By definition the angular frequency $\omega_0 = \frac{d\phi}{dt}$, and so the precession frequency f_0 in [Hz] is found to be

$$f_0 = \frac{\omega_0}{2\pi} = \frac{\gamma}{2\pi} B_r. \quad (2.6)$$

For hydrogen the gyromagnetic ratio is $267.513 \times 10^6 \text{ rad s}^{-1} \text{ T}^{-1}$, and therefore the Larmor frequency is 42.576 MHz when the external field is 1 T.

2.2.3 Magnetization

Up to this point, the analysis has only been focusing on single protons and it should be noted that classical mechanics is used to describe the proton behavior. In reality, it is quantum mechanics that predicts the behavior of single protons much better. However, it should be mentioned that classical mechanics allows us to understand the MR mechanism sufficiently [55]. This understanding is based on the correspondence principle, which was formulated by Niels Bohr [10], and which states that typically in the macroscopic limit the quantum mechanics reduces to classical physics.

A net magnetization vector is introduced as

$$\mathbf{M} = \frac{1}{V} \sum \boldsymbol{\mu}_k, \quad (2.7)$$

which is thus defined as the sum of all magnetic moments per unit volume. The volume that is to be imaged usually contains a very large number of protons. To give an impression, the number of protons in 13.15 liters of water is equal to the diameter of the observable universe in meters¹.

When an external magnetic field is applied, the net magnetization will point in the direction of this external magnetic field, which is referred to as the equilibrium state. Since the RF coils are placed perpendicular to this external magnetic field, no signal is received. When an RF pulse is sent, a "resonance" occurs when the Larmor frequency of the proton matches a frequency component of the RF

¹Calculation is based upon Avogadro's number, $6.022 \times 10^{23} \text{ mol}^{-1}$ and the assumption that the size of the observable universe is $8.8 \times 10^{26} \text{ m}$

pulse. The net magnetization flips into the transverse plane by an angle that depends on the magnitude of the RF signal and its duration τ , according to

$$\theta = \gamma B_{\text{rf}} \tau. \quad (2.8)$$

When a $\frac{\pi}{2}$ -pulse is used ($\theta = \frac{\pi}{2}$), the maximum MR signal is retrieved. Over time, a so-called relaxation takes place, and the magnetization will return back into the equilibrium state. In this thesis chapter, relaxation is not of importance, and, therefore, fully neglected. Information about relaxation times is, however, used in practice, and forms the basis for contrast in MR images. Also, in the equations to follow, it is assumed that the RF pulse is always a perfect $\frac{\pi}{2}$ -pulse. With these assumptions, a proportional relationship exists between the amplitude of the magnetization and the proton spin density, given by

$$M_0(\mathbf{r}) = \frac{\gamma^2 \hbar^2 B_m}{4kT} \cdot \rho_0(\mathbf{r}), \quad (2.9)$$

where ρ_0 is the proton spin density per unit volume, k the Boltzmann constant, T the temperature, and \hbar the Planck constant divided by 2π .

2.2.4 Retrieving the MR signal

The underlying physical principle of the creation of an MR signal (a voltage at the terminals of the receive coil) is electromagnetic induction, produced by precessing nuclear spin magnetization. It is, therefore, desired to find an equation that gives the relation between the net magnetization (or likewise, proton spin density) and the measured voltage at the receive coil. With Faraday's law of induction in combination with the principle of reciprocity it can be shown that the emf $\varepsilon(t)$ at the receive coil is equal to

$$\varepsilon(t) = -\frac{d}{dt} \int_V (\mathbf{S}(\mathbf{r}) \cdot \mathbf{M}(\mathbf{r}, t)) dV, \quad (2.10)$$

where the receive coil sensitivity $\mathbf{S}(\mathbf{r})$ is defined as the \mathbf{B} -field per unit current, or, in other words, the magnetic field the coil would produce at a point \mathbf{r} when a current of 1 A flows through the coil. The equation can be largely simplified if it is assumed that the coil sensitivity is not depending on \mathbf{r} and if the coil is placed perpendicular to the x-axis, $\mathbf{S}(\mathbf{r}) = S_x$. The magnetization after a $\frac{\pi}{2}$ -pulse is a

rotation in the x/y-plane, and a complex representation of this rotation is given by

$$\mathbf{M}(\mathbf{r}, t) = M_0(\mathbf{r})e^{-j(\omega_0 t - \phi_0)}, \quad (2.11)$$

where ϕ_0 denotes the initial magnetization phase. This expression of the net magnetization can be substituted into (2.10). Due to the dot product only the x-component is received, and the electromotive force is then

$$\varepsilon(t) = \omega_0 \int_V S_x M_0(\mathbf{r}) \sin(\omega_0 t - \phi_0) dV. \quad (2.12)$$

Note that $\|\varepsilon\| = \omega_0 S_x M_0 V$, with V the total imaged volume, reveals that the signal amplitude is approximately proportional to $(B_m)^2$, referring to equation (2.6) and (2.9).

2.2.5 Signal demodulation

The received voltage contains a high-frequency component. However, for obtaining the information that is interesting for MRI, a demodulation process is required. The term "signal" may sometimes be somewhat confusing. The reason is that there exists a signal as the voltage measured directly at the receiver coil (here denoted by $\varepsilon(t)$), and a signal after a demodulation process (here denoted by $s(t)$ or $s[k]$ when sampled). The signal is complex and denoted by

$$s(t) = s_{\text{re}}(t) + js_{\text{im}}(t). \quad (2.13)$$

The information about the amount of net magnetization is encoded in the amplitude. Spatial information is encoded in the phase/frequency, and it is retrieved if the real and imaginary component can be identified. The combined use of amplitude and phase modulation is better known as IQ modulation or Quadrature-Amplitude Modulation (QAM), and in Figure 2.3 a block diagram is shown of the demodulation process.

By means of IQ-demodulation (QAM) the high frequency component (Larmor frequency) can be removed from (2.12)

$$s(t) = \int_V \rho_{\text{eff}}(\mathbf{r}) e^{-j\phi_0} dV, \quad (2.14)$$

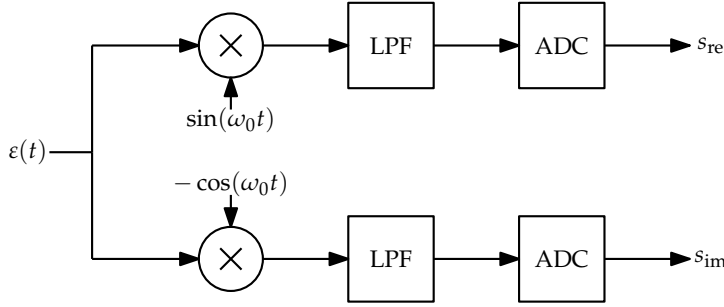


Figure 2.3: Block diagram which visualizes IQ demodulation of the received RF signal. The input signal is multiplied with two sinusoids (in-phase and quadrature) at the modulation/Larmor frequency followed by a low-pass filter. The signal is then digitized by means of an ADC.

where

$$\rho_{\text{eff}}(\mathbf{r}) = \omega_0 S_x M_0(\mathbf{r}). \quad (2.15)$$

is defined as the “effective” spin density. One may notice that the (demodulated) signal in this particular case is just a DC signal, independent of time, which is not a surprise, as all the protons saw the same magnetic field (recall equation (2.9)). Finally, since it is the demodulated signal which is of interest, often it is more convenient to perform the MR analysis in a rotating reference frame.

2.3 The elegance of MR: Spatial encoding

In the previous section it has been mentioned how protons possess a magnetic moment, and a net magnetization has been defined representing the sum of all magnetic moments within a certain volume. It has been illustrated how by means of an RF pulse the magnetization can be manipulated, resulting in an MR signal. It is only now that we will come to the essence of MR imaging, and its relation to electric power processing converters, with the addition of magnetic field gradients.

2.3.1 Slice selection

At first, it is shown how one of the gradients is used for the slice selection process (here, the z-direction gradient). The process of selecting of a slice in a patient is illustrated in Figure 2.4. Only protons that precess with a frequency within the frequency band of the RF pulse are excited, and only the protons that are excited contribute to the signal. The frequency spectrum of the RF pulse has a rectangular shape. The slice thickness depends on the applied gradient and on the bandwidth of the RF pulse.

Note that the slice selection gradient waveform has a positive and negative portion. That is because also in a single voxel, due to the gradient slight variations exist between individual protons. This effect causes the protons to dephase, and a rephasing lobe is applied directly after the slice selection gradient to counteract this effect. The areas of these lobes should be equal to each other as indicated in Figure 2.4.

The resulting signal, due to the application of an RF signal, is also shown in Figure 2.4 and known as the “echo” signal. Here, the echo signal is a “free-induction decay” (FID). The decrease in signal amplitude is a result of relaxation effects, where the net magnetization returns to equilibrium over time. When relaxation effects are ignored, as is done in the analysis to follow, the signal would last infinitely.

2.3.2 Frequency encoding and 1D imaging

After selecting a slice, two spatial dimensions remain. These two spatial dimensions are “encoded” and in this section we start with explaining imaging in one dimension. It is shown how the addition of a gradient field adapts the signal that is received after demodulation. Accordingly, the magnetic field which was assumed to be static is redefined into a linear magnetic field in the x-direction,

$$B = B_m + G_x x. \quad (2.16)$$

Application of the redefined magnetic field in (2.16) results in a spatially dependent Larmor frequency. For that reason, the applied gradient is defined as a frequency encoding gradient, because the application of the gradient results in a precessing frequency which is a function of the location on the x-axis. Therefore, while in (2.14), the accumulated phase was static and space-independent, now, the accumulated phase becomes a function of space and time according to

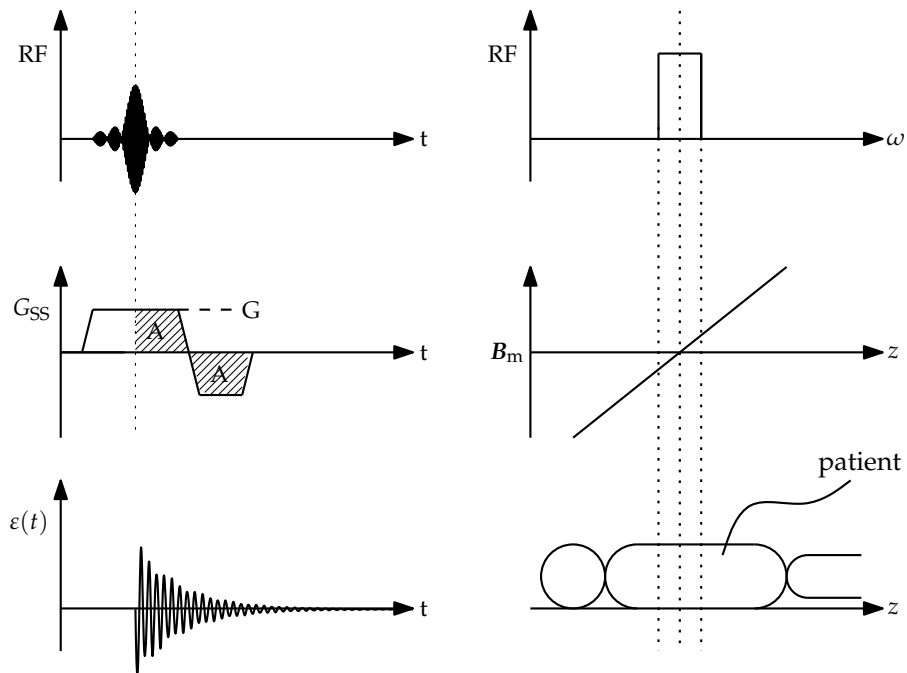


Figure 2.4: Illustration of the slice selection procedure. An RF pulse is sent simultaneously with the application of the slice-selection gradient. The measured emf (received signal) will be an FID echo. The frequency spectrum of the RF pulse has a rectangular shape, and “resonance” only occurs with protons that have a precession frequency that falls inside this band. As such, a slice is selected, because only protons from this slice contribute to the signal.

$$\phi(\mathbf{r}, t) = \int_0^t (\omega_0 - \omega(\mathbf{r}, t)) dt. \quad (2.17)$$

When redoing the calculus from the previous sections, it can be derived that (2.14) becomes

$$s(t) = \int \rho_{\text{eff}}(x) e^{-j2\pi k_x x} dx, \quad (2.18)$$

where

$$k_x(t) = \frac{\gamma}{2\pi} \int_0^t G_x(t) dt. \quad (2.19)$$

Which is a truly remarkable result, because (2.18) is in fact equivalent to a Fourier transformation (see Appendix B). In other words, these equations show that the application of a magnetic field gradient in combination with the physical laws of the receive coil and the demodulation process of a retrieved signal results in a signal which represents the Fourier transform of the proton spin density.

Note that when G_x is constant over time, (2.19) simplifies to

$$k_x = \frac{\gamma}{2\pi} G_x t, \quad (2.20)$$

which represents a linear frequency spectrum in k-space (section 2.4.3).

2.3.3 Phase encoding and 2D imaging

Without going too much into detail, it can be said, that 2D imaging is not significantly different because the same principle is used to the additional dimension. However, as frequency encoding cannot be applied again in another spatial direction during a single measurement, an ingenious solution is to observe multiple MR experiments each with a different phase in the remaining dimension. To understand this concept, refer to (2.17), showing that a difference in frequency equals an accumulated phase as function of time.

The remaining gradient, here in the y -direction, is thus defined as phase-encoding gradient, and, it might be interesting to note that the technique of phase encoding can also be used for higher dimensions in the additional dimensions. It is not a surprise that a similar result is found, and the wavenumber in the y -direction is given by

$$k_y(t) = \frac{\gamma}{2\pi} \int_0^t G_y(t) dt. \quad (2.21)$$

The total signal becomes

$$s(t) = \iint \rho_{\text{eff}}(x, y) e^{-j2\pi(k_x x + k_y y)} dx dy. \quad (2.22)$$

Equation (2.22) has the same structure as a two-dimensional Fourier transform.

2.4 Image reconstruction

2.4.1 Gradient echo

The application of gradients to spatially encode the proton spins can be done in a number of different ways. Two example sequences are gradient echo and spin echo. Here, only the basic gradient echo sequence is shown. Figure 2.5 illustrates the sequence. It can be seen that, first, a slice selection gradient is applied. Simultaneously, an RF pulse is sent to excite the protons that are to be imaged. When the slice selection process is finished, a rephasing lobe is applied to counteract dephasing. Also a rephasing lobe is applied in the frequency encoding gradient. For faster imaging, these rephasing lobes can be applied simultaneous with a phase encoding gradient. When the phase-encoding process is finished, a frequency encoding gradient is applied, and the echo signal is sampled. The number of samples needs to be at least equal to the number of pixels in one row of the image (to fulfill the Nyquist condition).

This process is repeated, each time with a different phase-encoding gradient. The total number of measurements equals the number of pixels in one column in the image. Two timing parameters are commonly used: TE (echo time), the time between an RF pulse and the resulting echo signal, and, in order to measure the total time to generate an image, TR (repetition time), which is defined as the time

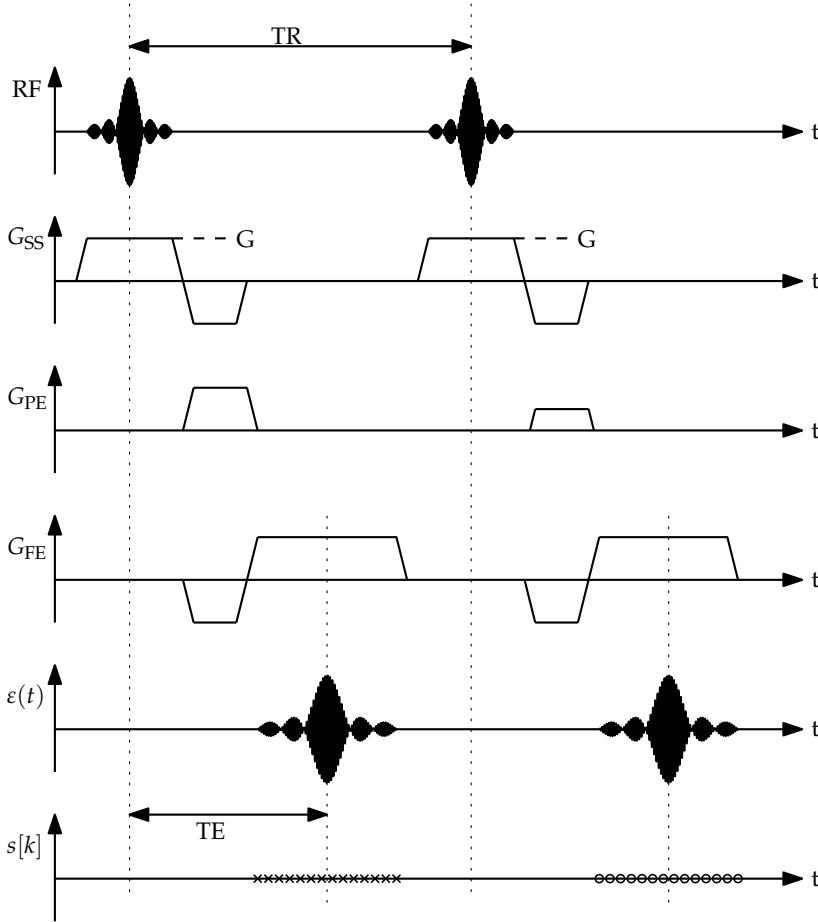


Figure 2.5: Illustration of a gradient echo sequence. First, the slice selection procedure is applied, then a phase encoding gradient is applied, and the last step is the application of the frequency encoding gradient. During this last step, read-out takes places. In other words, the receive coil and ADC are enabled, resulting in the emf $\varepsilon(t)$. After demodulation and sampling, the signal $s[k]$ is obtained, consisting of complex samples (here depicted as small crosses and small circles).

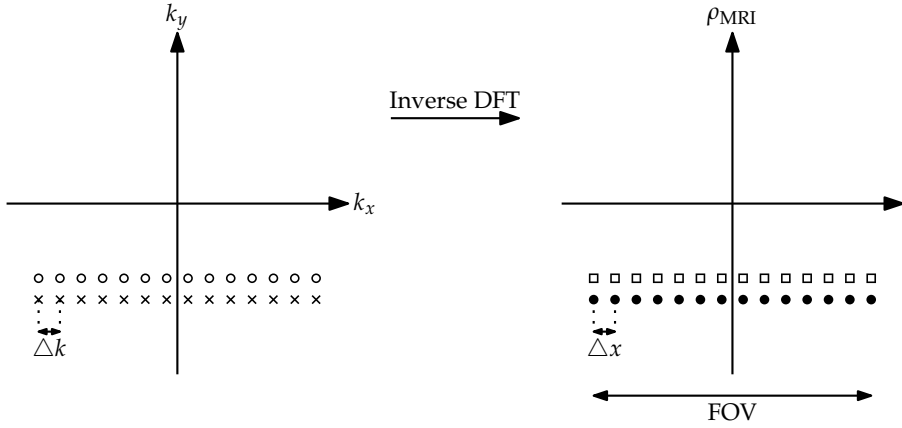


Figure 2.6: Image formation illustrated: The ADC samples obtained from a single MR experiment are directly placed in one row of k-space. When all rows are obtained, an inverse DFT is applied to generate the image.

between two consecutive RF pulses. The total time is the the repetition time multiplied by the number of measurements.

2.4.2 Image formation

As mentioned before, the signal, given by (2.14), is in practice sampled as demonstrated in Figure 2.5. Due to the demodulation process, the signal is in fact a sequence of complex numbers. These samples can be placed in an array as shown in Figure 2.6, and each MR measurement results in a row in k-space. When k-space is entirely filled up, an inverse 2D DFT can be applied to obtain the image. The image is, therefore, representing the reconstructed proton spin density.

For one dimension the inverse DFT, to obtain the reconstructed proton spin density ρ_{mri} , is given by

$$\rho_{\text{mri}}(x) = \frac{1}{\Delta x \Delta k} \cdot \sum_{p=-n}^{n-1} s[p \Delta k] e^{j2\pi p \Delta k x}, \quad (2.23)$$

where $2n$ is defined as the number of pixels in one row. Also note that for any given image, the k-space values (samples) can be reconstructed by using a DFT, by using

$$s[k] = \sum_{q=-n}^{n-1} \rho_{\text{mri}}[q\Delta x] e^{-j2\pi q\Delta x k}. \quad (2.24)$$

Note that, due to sampling, (2.20) becomes

$$\Delta k = \frac{\gamma}{2\pi} G \Delta t, \quad (2.25)$$

where Δt defines the sample time of the ADC sampling the signal.

2.4.3 k-space

It might be interesting to inspect k-space in a bit more detail, and to investigate its relation to the magnetic field gradient. The value of k can be seen as a wavenumber and Δk can be defined as the distance between two consecutive harmonics, or, as the wavenumber of the fundamental component. The reciprocal of the fundamental component defines the Field-Of-View (similarly, for a time-dependent function the reciprocal of the fundamental component would give the fundamental period), as

$$\text{FOV} = \frac{1}{\Delta k}. \quad (2.26)$$

The FOV can also be defined as the number of pixels times the size of one pixel in reality (voxel size), or as $\text{FOV} = 2n\Delta x$. Combining this equation with (2.25) and (2.26) it can be found that the following relation exists

$$G_x = \frac{\pi}{\gamma n \Delta x \Delta t}. \quad (2.27)$$

In other words, that the magnitude of the magnetic field gradient is inversely proportional with image resolution (Δx) and/or acquisition time (Δt).

2.5 The gradient system

Up to this point, the analysis has been done based on the magnetic field. One component of the magnetic field is the gradient and the gradient system is re-



Figure 2.7: Example of a gradient amplifier - The NG1800-XP by Prodrive Technologies [120].

sponsible for its creation. The gradient system comprises an input supply, a gradient amplifier, a gradient coil, but also cables, shielding and connectors. With the gradient amplifier a current is generated, that flows through the gradient coil, creating the magnetic field gradients. Such a gradient amplifier is usually placed in a different room and an example of a gradient amplifier is shown in Figure 2.7, the NG1800-XP, designed and constructed by Prodrive Technologies [120]. While in the early days of MRI linear amplifiers were used [135], at a certain moment these types of amplifiers were not suitable anymore because of the high losses and nowadays one finds mostly switched-mode power amplifiers. Still, due to the high demands for both power and accuracy, the most popular approach (i.e. Siemens, GE and Prodrive Technologies) is series-connected power stages [74, 129, 135], sometimes with an additional linear amplifier.

2.5.1 Relation between current and magnetic field

In this section we try to establish a relationship between current generated by the gradient amplifier and the magnetic field gradient. With the establishment of this relationship a simulation tool can be created which allows analyzing the

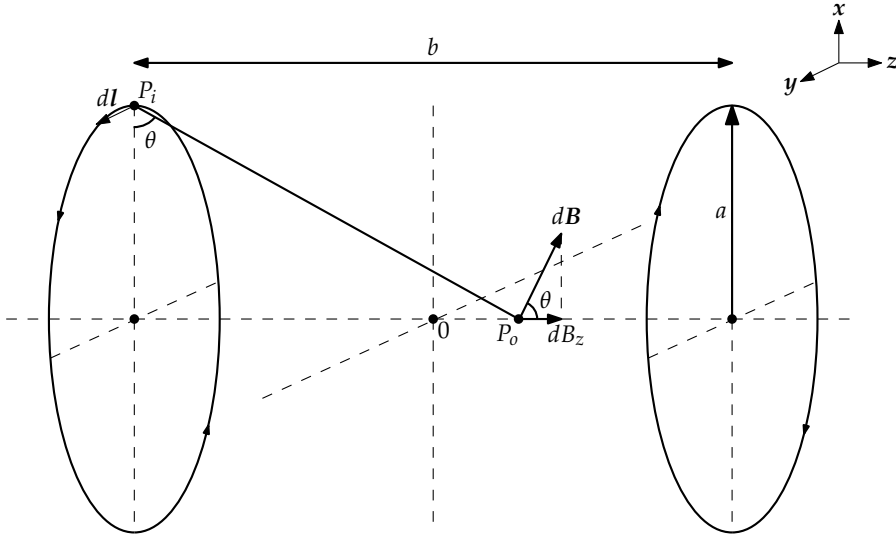


Figure 2.8: A basic coil arrangement for a gradient coil in the z-direction.

effect of a number of different current distortions. An important fact is that there is only one current component per axis, and so it can be assumed that the current in all the wires belonging to one axis is the same at all times. In other words, it is assumed that parasitic effects, such as parasitic capacitance or skin effect can be ignored. A commonly used structure for the gradient coil in the z-direction is shown in Figure. 2.8. It shows two coils with radius a , placed at a distance b from each other and placed perpendicular to the z-axis. The expression for the magnetic field at a specific point P_o in space that results from a current I in a wire located at point P_i can be calculated by applying the Biot-Savart law [82], assuming constant current (magnetostatics)

$$\mathbf{B} = \frac{\mu_0}{4\pi} \int_C \frac{I d\mathbf{l} \times \hat{\mathbf{r}}}{r^2}, \quad (2.28)$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ is the permeability of free space. The unit vector $\hat{\mathbf{r}}$ points in the direction from the source, a current-line element $I d\mathbf{l}$, to the point P_o . The distance between the two points is given by r . Due to symmetry, the magnetic field on the z-axis will only have a z-component. In the drawing it is shown that, to obtain this component, a multiplication of the magnetic field with $\cos \theta$ is required. It can be found that for a single coil

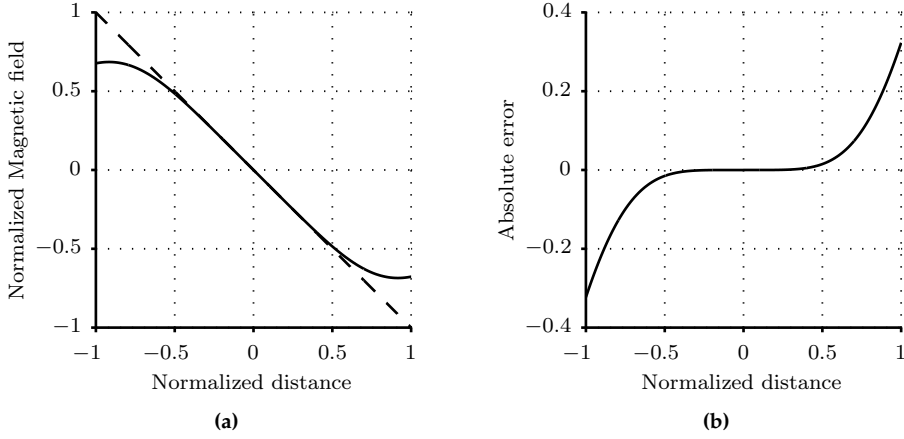


Figure 2.9: Graph of (a) normalized magnetic field in a Maxwell coil pair and (b) absolute error between desired and produced field, both graphs are plotted with respect to $\frac{z}{r}$.

$$B_z = \frac{\mu_0 I}{4\pi} \frac{2\pi a}{r^2} \cos \theta = \frac{\mu_0 I a^2}{2(a^2 + (z + \frac{b}{2})^2)^{\frac{3}{2}}}. \quad (2.29)$$

For the gradient coil, the current in both such coils is equal, but in opposite direction. Now, an analytic expression for the magnetic field along the z -axis is derived. To obtain the total field, the expression for the magnetic field of both coils in point P_0 should be summed (superposition), resulting in

$$B_z = \frac{\mu_0 I a^2}{2} \cdot \left[\frac{1}{(a^2 + (z + \frac{b}{2})^2)^{\frac{3}{2}}} - \frac{1}{(a^2 + (z - \frac{b}{2})^2)^{\frac{3}{2}}} \right]. \quad (2.30)$$

The optimal distance b between the coils for obtaining a linear field gradient on the z -axis can be found by deriving a Taylor expansion in $z = 0$ and solving the equation in such a way that the zeroth, second and third term are zero. It is found that $b = \sqrt{3}a$ satisfies these conditions, and a coil configuration with these dimensions is referred to as a Maxwell coil. The magnetic field and the error with respect to the desired field for a Maxwell coil is shown in Figure 2.9. The first term in the Taylor expansion defines the field-gradient, and it is given by

$$G_z = \frac{dB_z}{dz}(0) = \frac{48\sqrt{21}\mu_0}{343a^2}I. \quad (2.31)$$

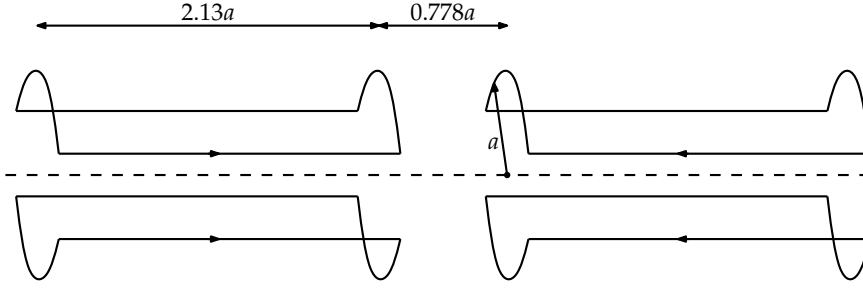


Figure 2.10: A possible arrangement for the x- and y-direction coil, a Golay coil pair.

It can be seen that there exists a linear relation between the current and gradient. In other words, the following relation can be defined

$$G = \eta I, \quad (2.32)$$

in which η is gradient coil efficiency, giving the amount of gradient per unit current. It is found that for a Maxwell coil,

$$\eta_{\text{Maxwell}} = \frac{8.058 \times 10^{-7}}{a^2} \text{ T m}^{-1} \text{ A}^{-1}. \quad (2.33)$$

A more complex description of the magnetic field can be derived, for instance, by analyzing the structure with a spherical coordinate expansion [111] [145]. However, also in these more complex descriptions (2.32) holds, but with a different value for η .

As mentioned earlier, a Maxwell coil pair can be used in the z-direction of an MR scanner. For the other two axes the basic configuration is a so called Golay pair. Similarly, it can be found that [145] the efficiency for a Golay coil pair as depicted in Figure 2.10 is equal to

$$\eta_{\text{Golay}} = \frac{9.18 \times 10^{-7}}{a^2} \text{ T m}^{-1} \text{ A}^{-1}. \quad (2.34)$$

Hence, for both coil shapes there is a one-to-one correspondence between the current and the magnetic field gradient. This holds for any current, and in particular also for any distortion in it.

2.6 Creating a simulation tool and results

A simulation tool with which the effect of gradient amplifier current distortion on image quality can be simulated and analyzed has been realized in MATLAB. The approach is as follows: First of all, the input of the simulator is an image to which an inverse MRI is applied. Then, k-space is recalculated based on the equations derived in this chapter and based on the gradient waveform which is produced by an amplifier system that is simulated with PLECS. Since original image data is not available, to be able to do an inverse MRI, it is important that the simulator is based on a reversible process. In other words, that if the produced gradients were ideal that the exact same image would be generated. For this reason, it is also assumed that all other subsystems are ideal. This means that for an ideal MRI scanner the following assumptions are made:

- The large magnet produces a magnetic field that is perfectly homogeneous.
- The RF system produces ideal RF pulses which are able to excite the protons as desired and the RF system is able to perfectly measure the echo signal. Relaxation effects are ignored.
- All other components in the gradient system are ideal, that is, the gradient coils produce an exactly linear gradient whenever a DC current flows through the coil. Also, the magnetic field gradient is proportional to the current.

It is, based on these assumptions, how the equations have been derived in this chapter. With the exception of numerical errors, the ideal MRI scanner is now a reversible process, because ideally it involves a DFT and inverse DFT. In principle there are two methods that can be distinguished which can be used for creating a simulation tool. Either the equations (2.23) and (2.24) are directly applied (method 1), or a virtual space is generated that really simulates the behaviors of individual protons (method 2). In the following, method 1 has been used to generate the results, because it is simpler and faster. It is assumed, however, that if method 2 would be applied that similar results are observed.

2.6.1 Output current distortions

Note that, from equations (2.23) and (2.24), it can be seen that an additional gradient affects the value of k , and therefore also the accumulated phase. As phase is used to spatially encode the proton spin density, errors in the gradient will

Table 2.1: Simulation parameters.

Parameter	Description	Value	Unit
MRI			
FOV	Field-of-view	0.256	[m]
Δx	Resolution	0.001	[m]
Δt	Sample time	20	[μ s]
G	Gradient	4.6	[mT m ⁻¹]
η_{coil}	Gradient coil efficiency	6.578	[μ T m ⁻¹ A ⁻¹]
Power stage			
f_{sw}	Switching frequency	50	[kHz]
V_s	Supply voltage	1000	[V]
L	Filter inductance	15	[μ H]
C_H	Filter capacitance	1	[μ F]
C_g	Filter capacitance	0.1	[μ F]

result in spatial errors. It is this kind of error that is generally referred to as image distortion [53], and here image distortion is classified in three types: Timing distortion, where the echo is not placed exactly symmetrical with respect to echo time TE (refer to Figure 2.5), also known as "echo shifting". Static distortion, such as gain errors in the amplifier or (static) background gradients that exist in other dimensions when the signal is sampled. And, lastly, dynamic distortion, such as a current ripple or a low-frequency (50-Hz) component on the supply that reflects to the output current.

Image distortion can be visualized by comparing the distorted image with the ideal image, and the distortion depends on the image. However, for quantification, distortion can better be based on the error in k-space. In other words, by combining (2.19) and (2.32), the relation between error in k-space and current is given by

$$e[k] = \frac{\gamma\eta}{2\pi} \int_0^{kT_s} \tilde{I}(t) dt, \quad (2.35)$$

where $\tilde{I}(t)$ denotes the current perturbation. In the upcoming simulation results the focus is on image distortion and the simulation parameters from Table 2.1 have been used. It must be mentioned that the parameters are somewhat arbi-

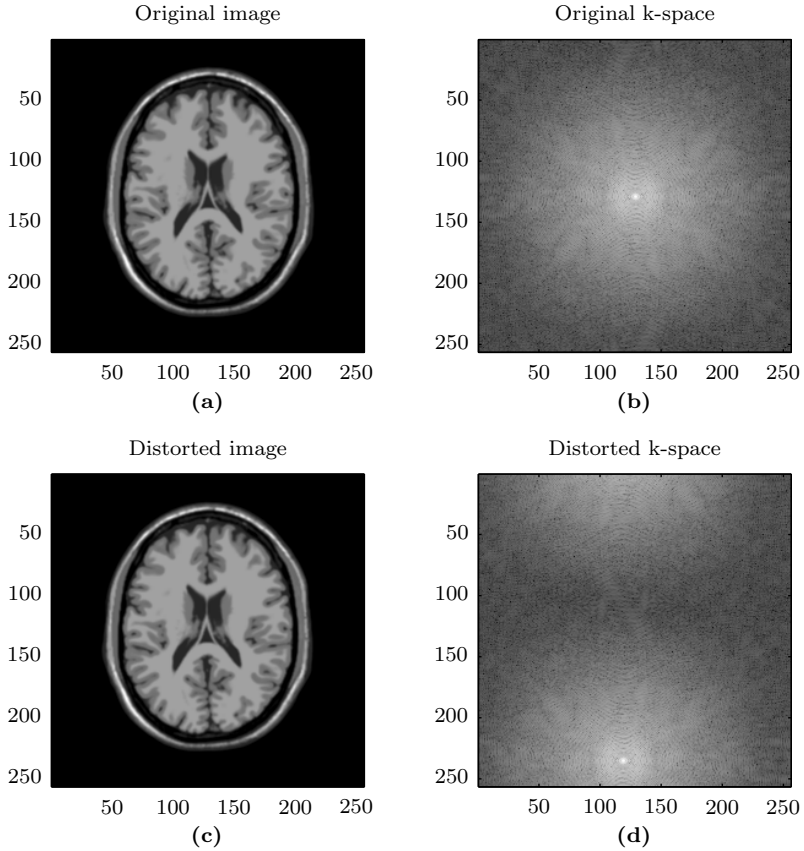


Figure 2.11: Simulation result of the effect of a timing error.

trary. It is just not known which type of scanner has been used for generating the original image nor is the original data available. The parameters are, however, linked to each other such that the equations in this chapter are valid. The current is created by an H-bridge converter with output filter and resistive load ($1\ \Omega$).

Time delay

The first simulation demonstrates the effect of the first type of distortion, timing distortion, and, a significant time delay has been added. In Figure 2.11 the result is shown, and it can be seen that k-space looks entirely different. The white spot, which was originally in the middle, has been displaced. However, when an

inverse DFT is applied to the distorted k-space, the original image is retrieved. As a result, it can be concluded that in an ideal MRI scanner, timing distortion is not influencing the image quality. It should be mentioned though that the image formation here is based solely on magnitude, and, for most MRI techniques that is also sufficient. However, the phase of the resulting image will be different, and in for instance MR thermometry or magnetic field mapping phase information is used. Also, when relaxation and dephasing are taken into account, results may also be different, as time delay will then result in signal intensity loss [53].

Gain error

In Figure 2.12(b) it is shown how the image would change if a 10% gain error would exist on the frequency-encoding gradient (x-gradient). In practice, an amplifier would most certainly not generate that much gain error, however, to be able to see the distortion, a significant error needs to be added. It can be seen that the image stretches and deforms in the vertical direction. Similarly, in Figure 2.12(c) a 10% gain error has been added on the phase-encoding gradient (y-gradient), resulting in a deformation in the horizontal direction.

Background gradient

A gain error can be seen as a background gradient, or, to put it differently, the total gradient can be written as $G + \tilde{G}$, the sum of the desired gradient and a perturbation gradient. It would also be interesting to see what would happen if a non-zero gradient exists in another dimension during read-out (application of the frequency-encoding gradient). That is, when the frequency-encoding gradient is applied, it is assumed that the slice-selecting and phase-encoding gradients are zero. Figure 2.12(d) shows the result of a non-zero phase-encoding gradient during read-out, and image distortion can be observed. The image is slightly rounder, and the white edge is thicker. Also, the image is a bit blurred and looks less sharp than the original image.

Current ripple

Both the gain error and the background gradient can be defined as static distortions, in other words, as distortions which are assumed not to change in time. However, in gradient power amplifiers also dynamic distortions can occur. For example, current ripple is inherently present in switching power amplifiers. To

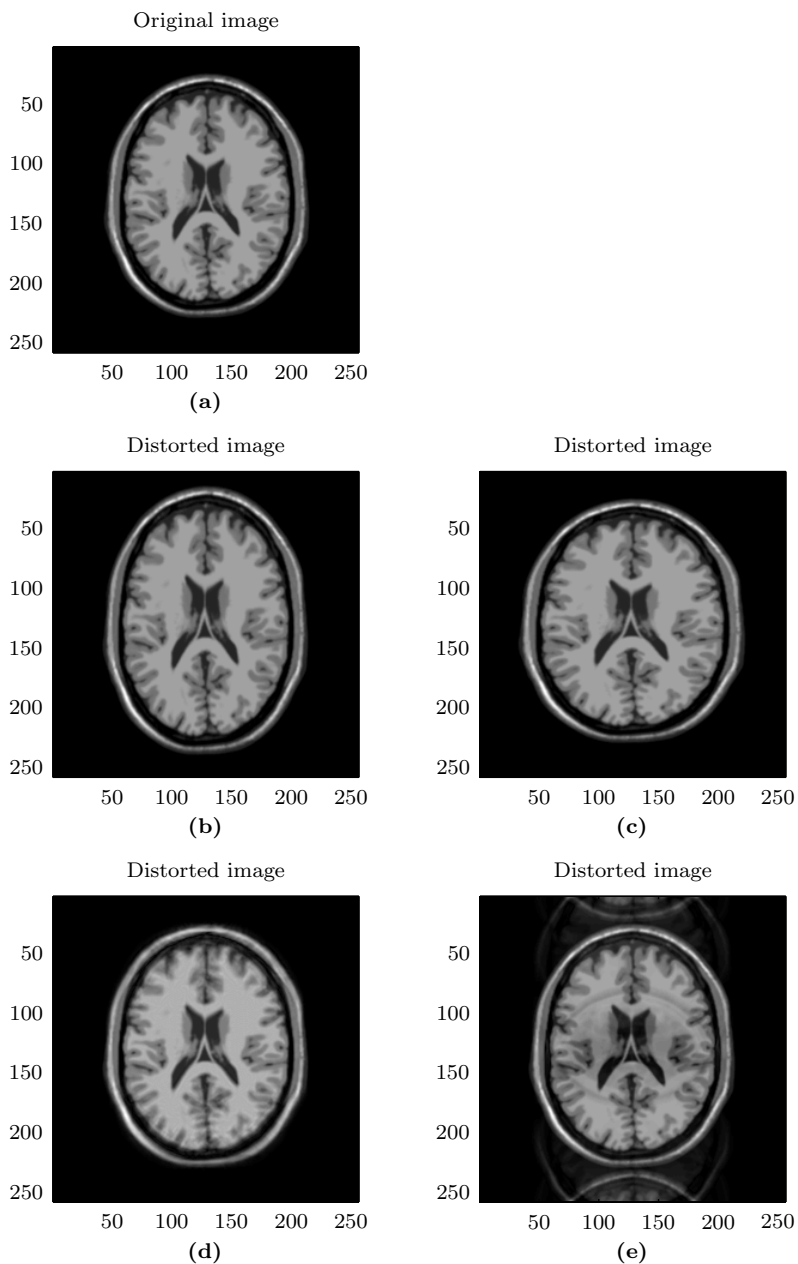


Figure 2.12: Simulation result of the effect of different types of distortion in the gradient amplifier: (a) the original image (b) gain error in the x-gradient (c) gain error in the y-gradient (d) background gradient (e) current ripple.

show this effect more clearly, for the following simulation the switching frequency has been lowered to 10 kHz. The result is shown in Figure 2.12(e) and it clearly can be seen that the image is modified.

2.7 Conclusion

In this chapter an MRI system has been explored and analyzed from a power-electronics perspective. From this perspective the question that needs to be addressed is the relation between current, generated by a gradient amplifier, and the resulting image. The analysis was required to create a simulation tool in MATLAB, where simulated current waveforms generated by a PLECS simulation can be used to generate an image. As such, it is possible to simulate specific distortions that commonly exist in amplifiers and see how they affect image quality. The presented simulator is very basic, and so far only the most essential elements of MR have been included, but other elements can easily be implemented to visualize how they correlate with gradient amplifier distortions.

From the simulation results it can be concluded that, as gradients are responsible for spatially encoding the proton spin density, not surprisingly, distortions in the current lead to spatial errors in the image. It has been shown how static distortions (gain errors) lead to a deformation of the image. Dynamic distortion, such as current ripple, has a more local distortion effect and a high current ripple leads to some sort of mirroring (ghosting) in the image. It should be mentioned that the added distortion is relatively high for the sake of clarity. Also, when there is a possibility to measure the distortions, afterwards, a correction can be applied during reconstruction.

Besides the distortion analysis done to single 2D images, it may be possible to expand the simulator such that it is also possible to analyze 3D MR experiments. When multiple images are generated, other aspects become relevant, such as repeatability. In other words, successive pulses need to be as identical as possible. This relative deviation or noise is in electrical engineering referred to as jitter. To minimize jitter, it is usually recommended to use the same clocks for both the amplifier and the rest of the MR system, such that they are fully synchronized.

Part II

Episteme

Chapter 3

Exploration and categorization of multicell circuits

“The function of electrical power processing systems is to convert electrical energy from one voltage, current, or frequency to a different voltage, current, or frequency. This function is to be achieved, ideally, with 100 per cent efficiency.”

(R.D. Middlebrook)

3.1 Introduction

For the realization of the PowerDAC a multicell topology is used. Multiple reasons can be found for which a multicell topology is applied, the first reason being the splitting of the switching device stresses. These stresses are given by the voltage the device needs to block, the current the device needs to conduct, and the number of switching actions the device needs to perform within a certain time period. These parameters determine the losses, the power dissipation at any time instant, and determine, therefore, the device temperature. The losses in combination with the number of devices play an important role in the power converter efficiency, and the device temperature plays an important role in the converter lifetime or reliability.

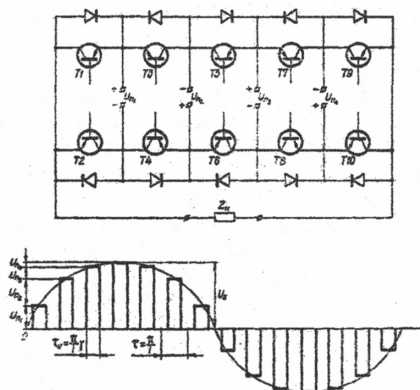
Besides the reduction of device stresses, another reason for using a multicell topology, is the possibility to control the switching devices in such a way that

a multilevel waveform is generated. Such a multilevel waveform has a lower harmonic distortion compared to a waveform created by the two-level alternative [109]. A lower harmonic distortion reduces the size of passive components in the output filter, and potentially increases bandwidth and accuracy.

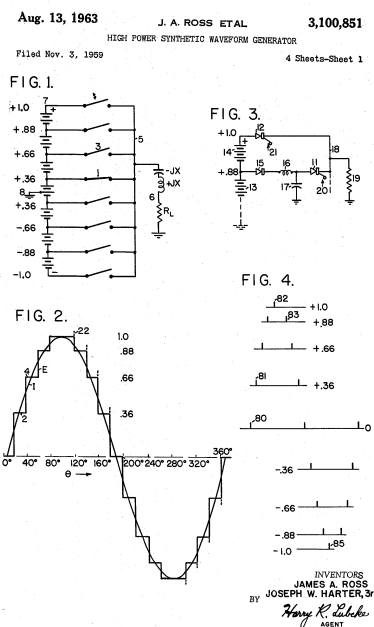
Despite these advantages, when evaluating applications in which multilevel converters are used in practice, the number of levels is still limited. That can partially be explained because a multilevel converter suffers from being more expensive, having a lower reliability and being more complex to design. An exception to this statement is found in applications for which the number of switching devices is already high due to the high power rating, which is for instance the case with HVDC power converter solutions [40].

It is already half a century ago that the first publications on ideas of multilevel approaches appeared. The basic idea is simple, instead of using only one voltage source for generating the output voltage waveform, multiple sources are introduced and an arrangement of switching devices is applied to either select a certain output voltage or to sum/subtract the voltage sources to obtain a desired output voltage level. For that reason, an intrinsic feature of multilevel converters is that in some manner the various DC voltage levels need to be created. Some multilevel structures, such as the series-connected H-bridge, make use of external sources to create the voltage levels. However, these external sources need to be floating, meaning that an isolated power supply is required for each voltage level. Such power supplies tend to be complicated and bulky, adding to the volume, weight, complexity and cost of the entire converter system. Not to mention the decrease in reliability. In other multilevel converters, such as the flying-capacitor, the neutral-point-clamped or the modular multilevel converter, capacitors are used to create the DC voltages. One of the major challenges, though, is the balancing of the capacitor voltages. Alternatively, in parallel buck-converters, interleaving can be used to create multiple voltage levels [96].

In Figure 3.1 examples are given of the first patents/publications that present the idea of multilevel circuits. In Figure 3.1(a) a picture is shown from one of the early developments (1964) in the USSR, and its existence was reported in [156]. It clearly shows a plurality of voltage sources, and a method by which different voltage levels can be created. In Figure 3.1(b) an idea is shown where voltage sources are stacked on top of each other [128]. At every time instant only one of the switches is turned on and a desired voltage level is selected. In Figure 3.1(c) an original image from a patent is shown where two H-bridge power stages are connected in series [94]. Interestingly, the first proposals on multilevel use a staircase approximation of the output voltage waveform, similar to the output waveform of a conventional DAC. However, it is only a few years later that the



(a) Example displaying an early development of the multilevel concept in the USSR (1964) [156].



(b) Patent of James A. Ross and Joseph W. Har-
ter (1963) [128].

PATENTED MAY 25 1971

3,581,212

SHEET 1 OF 5

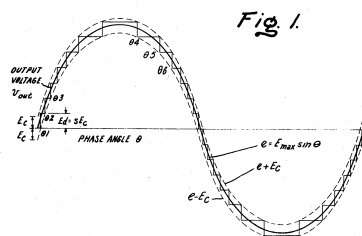
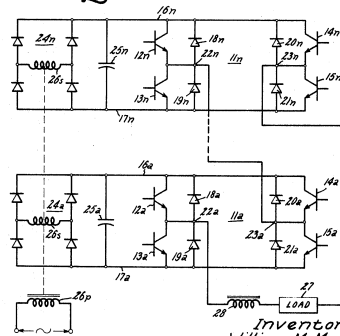


Fig. 2.



INVENTOR:
William McMurray
by *Ronald R. Rapp*
His Attorney.

(c) Patent of William McMurray (1971) [94].

Figure 3.1: Examples of early work displaying the first ideas on multilevel conversion.

first publications and patents were published in which a PWM approach was proposed [156].

In the years following, research and development lead to alternative topologies, aiming at an optimal creation of a multilevel waveform. This chapter aims to give an overview of the different multilevel topologies that are available for realizing power conversion from a DC voltage to an arbitrary waveform (static inverters). The purpose of such an overview is to demonstrate the current state-of-the-art regarding multilevel inverters. An overview of multilevel inverters can be found in, for instance, introductory sections about the subject [39, 54, 76, 142] or in overview-papers such as [1, 42, 72, 98, 126, 156]. However, here, instead of just listing the various options, as is commonly done, our intention is to find a classification. Such a classification or grouping of topologies should be based on commonalities among the topologies. It is found that these kinds of commonalities exist on different layers of abstraction. A categorization, as is proposed, is also known as a taxonomy. Interestingly, it is also found that there exist symmetry and/or dual relations between different groups, although it requires the expansion of the classical duality theorem to include non-planar circuits. This is addressed in more detail in section 3.4.

Of course, it is not our goal to rewrite the existing terminology, and it is tried to avoid introducing new terms. Much of the described material may seem familiar to many readers up to this point. Also, it is not our goal to propose a taxonomy that covers all possible power converter topologies, although the method may inspire others to do the same for their main field of expertise. Yet, it is the diversity of multilevel converters that have been proposed in the last decades that have been the inspiration for the categorization in the first place, and it is exactly this family of converters that forms the main focus of this chapter.

3.2 Basic concept of multilevel power conversion

Before giving an overview of the different multicell topologies, first, the basic concept of multilevel power converters needs to be explained in more detail. Figure 3.2(a) shows an example of a block-diagram representation of a conventional power-electronics system. Such a power-electronics system may be represented as an interconnection of various one- and two-port elements. When filters are neglected for the sake of argument, then, the hard-switched two-level converter produces a rectangular-wave current signal as well as a rectangular-wave voltage signal. These signals result in high distortion on the input as well as on the output of the converter, as shown in Figure 3.2(a). As a result, as high distortion levels

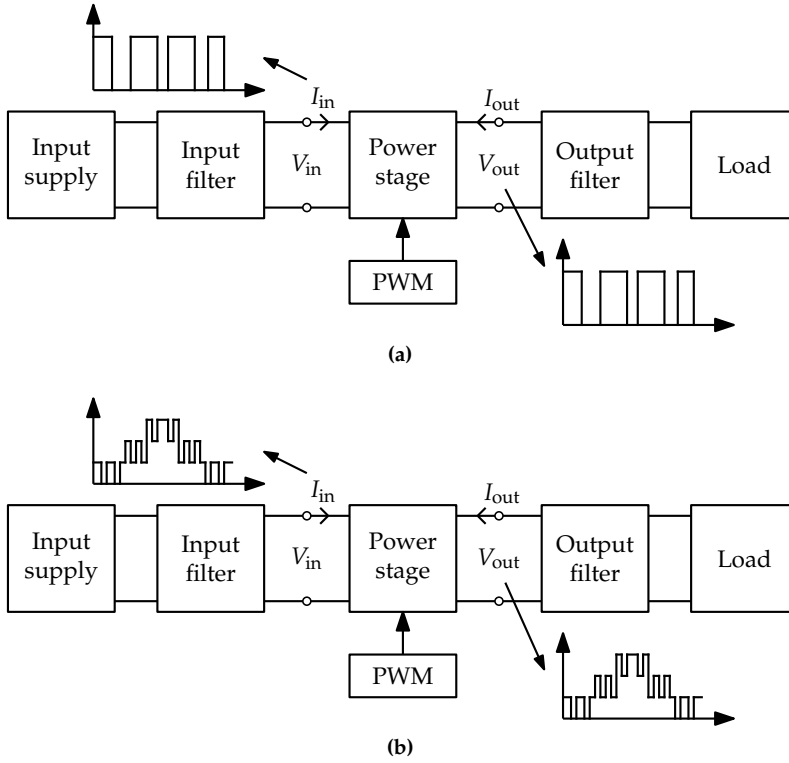


Figure 3.2: Block diagram of (a) a conventional 2-level power amplifier (b) a multilevel power amplifier.

are unacceptable in almost any application, an input filter and output filter are required to reduce the higher-order harmonic components and to ensure that the system will satisfy the requirements on electromagnetic interference (EMI) and maximum allowed distortion on input and output waveforms.

To enhance the converter topology such that the waveforms at both input and output are less distorted, a multilevel approach can be used, as it better approximates the desired waveform. This is shown in Figure 3.2(b). Note that a multilevel waveform can be created on the input or output waveform, depending on the topological configuration of the power stage.

In this section, a comparison is made between two-level and five-level PWM waveforms. Ultimately, an estimation of the filter size reduction is given, based on idealistic waveforms produced by fixed-frequency (carrier) PWM. This estimate is made under the assumption that the effective frequency of the produced waveform remains equal with respect to the number of levels. Note that this as-

sumption in multilevel PWM may result in a lower switching frequency of the individual devices. Additionally, in this section, the generation of a multilevel waveform is shortly discussed, and also the effects of sampling and quantization in multilevel PWM are examined.

3.2.1 Generation of multilevel PWM waveforms

As stated in the introduction of this chapter, two types of multilevel waveforms can be distinguished. One could choose to use a staircase modulation strategy [38], however, due to a limited amount of voltage levels in current multilevel technologies, this type of waveform is not sufficiently accurate for amplifier applications. An alternative method is based on modulation theory where a reference is encoded by means of a high-frequency carrier waveform. This reference can either be continuously varying during the PWM modulation process (natural sampling) or the (sampled) reference is kept constant during one switching cycle (regular sampling). The latter is sometimes referred to as uniform sampling.

For multilevel waveform generation, a straight-forward and basic method is the adaption of the fixed-frequency carrier-based modulation as also employed in two-level converters [19]. Two methods are visualized in Figure 3.3, where for both methods each carrier is compared to a reference (here a sinusoid of 1 kHz) resulting in a PWM waveform. The method depends on the interpretation of the multiple carriers. In the first interpretation, the carrier waveforms with amplitude 0.25 are seen as stacked on top of each other, and this interpretation is defined as phase disposition (PD) modulation. Note that the stacked carrier waveforms could have a phase-shift with respect to each other. For the waveforms displayed in the Figure 3.3(a) alternative phase opposition disposition (APOD) is applied as a carrier waveform has a phase-shift of π with respect to the carrier waveform on top of or below itself. It can be seen that with four carrier waveforms 5 levels are created. The number of levels is denoted by N .

In the second interpretation the carrier waveforms are seen, not stacked, but as being out of phase with respect to each other. This interpretation is known as phase-shifted carrier (PSC) modulation. The resulting PWM waveform of PSC is identical to APOD for natural sampling since all the switching instants occur at the same time. However, for regular sampling, the switching moments will differ, depending on the moment of updating the reference for each carrier. Note that the reference update frequency is lower for PSC than for APOD. One of the two PWM methods might have the preference in a particular multicell topology, because each carrier waveform results in one PWM signal, or switching function,

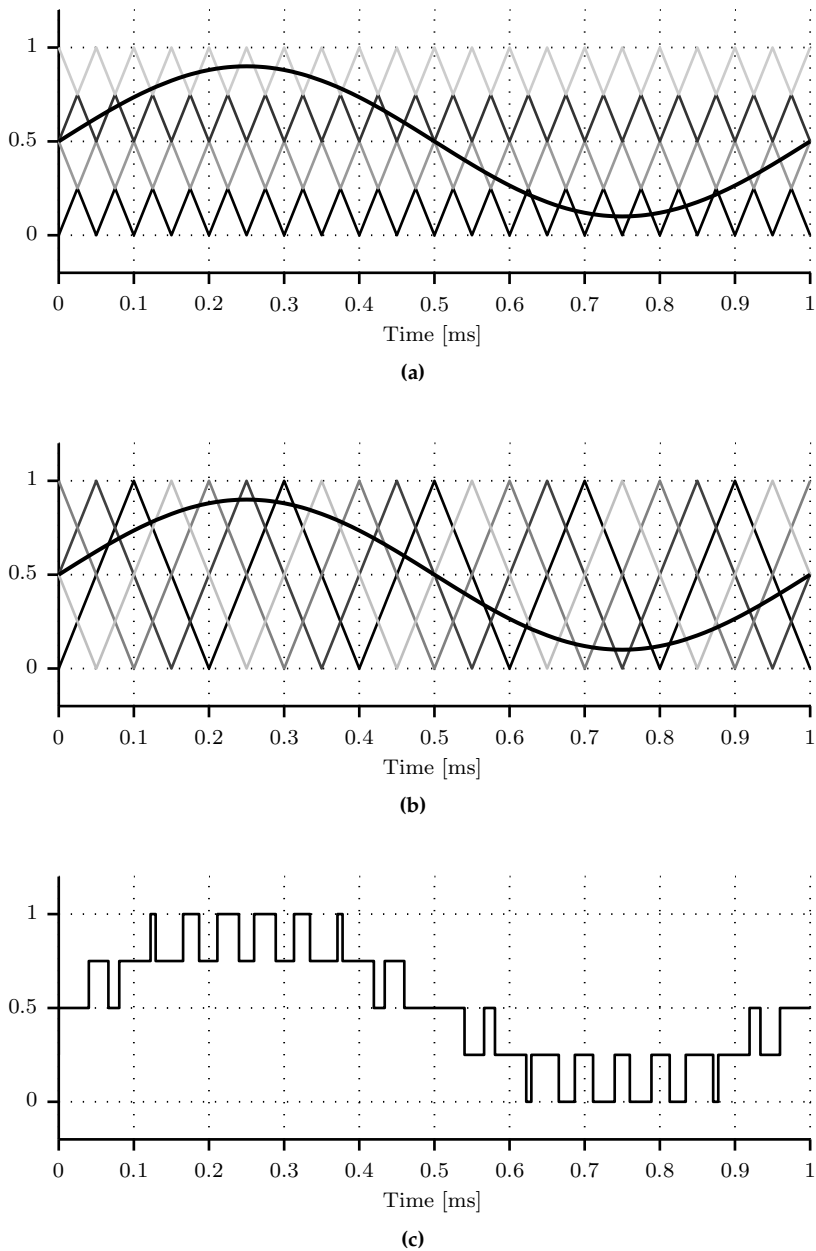


Figure 3.3: Graphical visualization of the multilevel carrier modulation process.

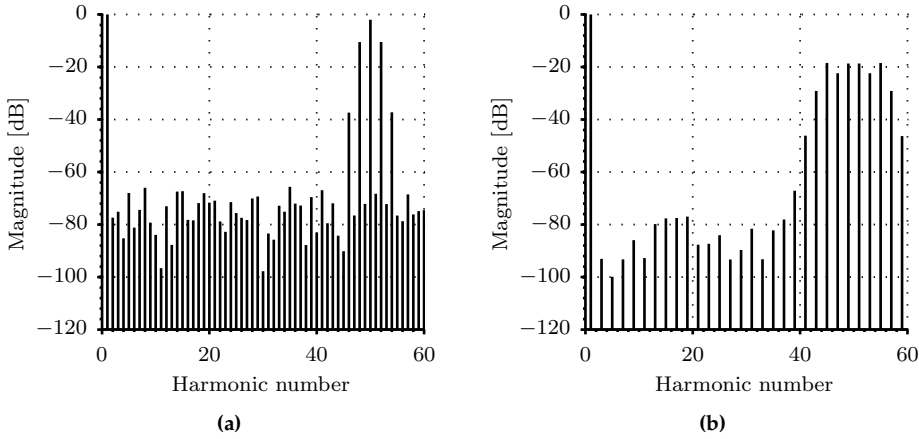


Figure 3.4: Harmonic spectrum of (a) a two-level waveform and (b) a five-level waveform, presenting the distortion effect of quantization.

which in some cases can be directly applied to a certain switch.

3.2.2 Multilevel and quantization distortion

In the time-domain, a multilevel waveform seems to be a much better approximation of a reference waveform than its two-level counterpart, as was shown in Figure 3.3. However, since switching frequency harmonics are dominant, it is difficult to see other types or sources of error/distortion. Other types of distortion (sampling and quantization) can, therefore, better be visualized and analyzed by using a harmonic spectrum. As a start, quantization distortion for two- and five-level is analyzed with ideal waveforms. In Figure 3.4 the harmonic spectrum is depicted, with the reference as shown in Figure 3.3, but with an effective switching frequency of 48 kHz. In both cases the effective switching frequency is the same, and the number of bits of the reference or PWM modulator is 8. Natural sampling is used in the PWM modulator, because we are specifically interested in quantization distortion. Both PSC and APOD yield the same results, as explained in the previous section.

When examining the results, it is interesting to note that the multilevel waveform does not have even harmonics, which is an indication of symmetry in the waveform. Since zero is a voltage level, the first half of the reference sine results in exactly the same PWM waveform as the second half of the reference period. Fur-

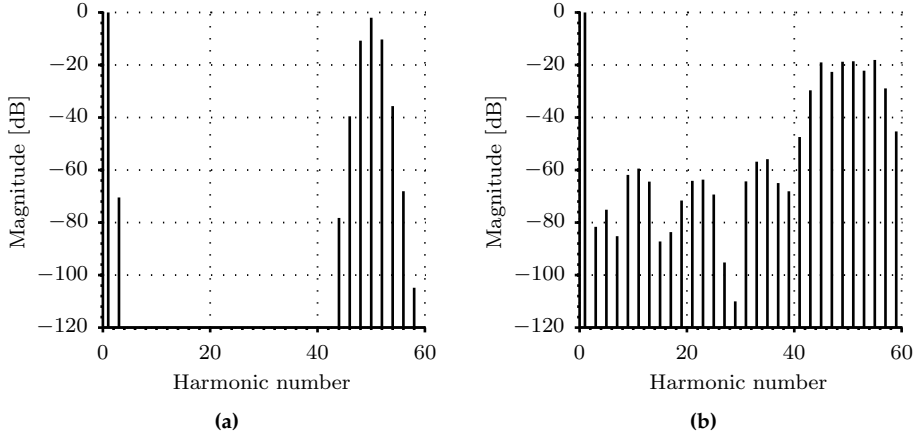


Figure 3.5: Harmonic spectrum of (a) a 2-level waveform and (b) a multilevel waveform (APOD), presenting the distortion effect of sampling.

thermore, it can be seen that due to the voltage levels the quantization distortion is lower. In other words, the voltage levels can be seen as additional bits, and it can be explained by the fact that multiple carrier waveforms are used, each contributing to the total number of bits of the total PWM waveform. Note also that switching frequency harmonics are lower, this effect is analyzed in section 3.2.4.

3.2.3 Multilevel and sampling distortion

Quantization distortion is a result of the digital representation of a reference, and of limitations of the modulator clock. Sampling noise is a result of regular-sampled PWM, in which the reference in the modulator is only updated at the start of the carrier period. Compared to natural sampling, regular sampling results in sub-optimal placement of the PWM pulses within one switching cycle.

In Figure 3.5 results of a simulation including sampling distortion are shown. Here, APOD and PSC are not producing the same harmonics and in Figure 3.5 it was chosen to show the harmonic spectrum when using APOD. The harmonic spectrum of PSC is similar to the two-level spectrum, and only the third harmonic will be higher. It can be seen from the simulation that for a given effective switching frequency a multilevel waveform is much more sensitive to sampling distortion.

3.2.4 Multilevel and output filter reduction

In the previous section it could be seen that there exists a major difference between the harmonic spectrum of a two-level and a five-level PWM waveform in terms of switching frequency harmonics. An output filter is mainly designed for reducing these components, because the switching frequency components contribute either to the distortion in the load or cause EMI issues. It is interesting to give a simple quantification of how much the filter size would reduce due to the use of a multilevel voltage waveform. Inspecting Figure 3.4 or 3.5 and comparing the two-level and five-level waveform, a difference of approximately 16 dB can be observed in the magnitude of the switching frequency (carrier) harmonic component.

Let us consider a second-order Butterworth filter which is critically damped (Quality factor $Q = \frac{1}{\sqrt{2}}$), and has transfer function

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{Q}{\omega_0}s + \omega_0^2}. \quad (3.1)$$

Then, let us find the value for the cut-off frequency ω_0 for which the worst-case switching frequency harmonic has a relative magnitude of -40 dB. This value is sometimes used as a rule-of-thumb for filter design as it represents the slope (-40 dB dec $^{-1}$) of a second-order filter at high frequencies. In other words, a factor 10 (1 decade) between the cut-off frequency of the filter and the switching frequency results in an attenuation of the switching frequency harmonic of a factor 100. The value of ω_0 for the two cases is found to be

- For two-level, $\omega_0 = 2\pi \cdot 5388$ rad s $^{-1}$
- For five-level, $\omega_0 = 2\pi \cdot 13\,598$ rad s $^{-1}$

It can be seen that the difference in cut-off frequency is quite significant, which leads, first of all, to a higher control bandwidth. Next, based on Q and ω_0 , the values of L and C in the output filter can be determined [121],

$$\begin{aligned} C &= \frac{1}{\omega_0 R_L \sqrt{2}} \\ L &= \frac{R_L \sqrt{2}}{\omega_0}. \end{aligned} \quad (3.2)$$

where R_L denotes a fictitious load resistance. Note that both the capacitance and inductance are inversely proportional to the cut-off frequency. Since current and voltage ratings are assumed to be almost equal (the magnitude of the switching frequency harmonic has been forced to be equal) in both cases, the stored energy will approximately be inversely proportional to ω_0 . For inductors which are designed with the use of the area-product method the relation between inductance and size (volume) is found to be approximately $\text{Vol}_L \propto L^{3/4}$ [93]. Interestingly, in [106] the same relation, $\text{Vol}_C \propto C^{3/4}$, has been found empirically (by comparing manufacturer datasheets) for film capacitors.

It should be emphasized that the output filter reduction presented here is only due to additional voltage levels. An even higher reduction is achieved with multilevel circuits in which the effective switching frequency is increased by a factor M , where M denotes the number of cells. The switching frequency and its sideband harmonics then shift towards Mf_{sw} , and ω_0 will shift accordingly. In that case, an additional reduction of a factor M can be achieved.

3.3 Taxonomy

The electronic circuit with which a multilevel waveform can be created is called a multilevel converter. In this section the most popular multilevel topologies are explored and categorized. The categorization is obtained by means of a taxonomy. Taxonomy is the science of classification in hierarchical ranks. Organizing by means of categorization can be very useful for many reasons. In relation to the topic of this work, one can think of, for instance, the increase in understanding the underlying operating principles at certain abstract levels by grouping power converters or amplifiers based on shared characteristics. It should be mentioned that there is no set of rules by which the shared characteristics are determined, and this is, therefore, a decision of the taxonomist.

A popular grouping for power electronics has been a single-layer classification based on function or type of input source and output load which are connected to the power converter. That is, for instance, grouping in DC-DC, AC-DC, AC-AC and DC-AC conversion [11]. Another possibility would be to group based on the applied control method, i.e. line-frequency converters, resonant converters, multilevel converters. A disadvantage of the two methods is, first, the possibility of a single topology to be classified twice. A half-bridge topology can be used for DC-DC and DC-AC purposes. A flying-capacitor converter or MMC can be operated as a multilevel or as a two-level converter. And secondly, an enormous number of variants can exist in one group, as is the case for, for instance, multilevel convert-

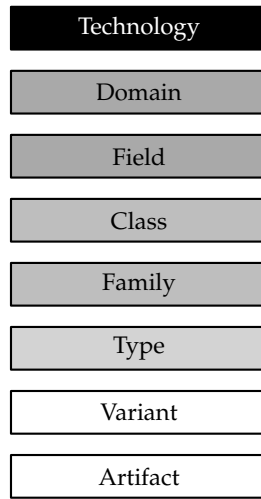


Figure 3.6: Ranks in the taxonomy of designed objects.

ers. Hence, the topology is considered to be the basic rank of the classification, and it determines the type of converter. Consequently, a third approach is proposed here, which is the use of a multi-layer topology-based classification. The shared characteristics are then mostly based on commonalities in structure and the type of components that are used. Each topology has strengths, weaknesses, possibilities and limitations. These then define a set of constraints on control and components for the eventual application.

Figure 3.6 shows the various ranks that are used as intermediate levels for the classification and these ranks are each shortly discussed in the following. One of the challenges in the classification of technology is the concept of hybrid. As an example, if one would choose to classify cars based on their fuel source, i.e. gasoline or electric, then it is always possible to create the hybrid variation of cars powered both by gasoline and an electric source. Not surprisingly, the hybrid category can be found in all ranks.

3.3.1 Technological domains and fields

A possible subdivision of technology is identical to the different disciplines or branches which exist in engineering [44]:

- Electrical
- Mechanical

- Chemical
- Civil
- System

Within the proposed taxonomy the first rank is defined as domain. Domains are very closely related to the physical energy domains that exist. The last domain "system" is devoted to all the interdisciplinary domains.

The second rank is field and it can be used to sub-categorize domains. The term field is chosen, as it is used already quite often. For instance, power electronics is the field within electrical engineering that concerns with the conversion of electrical energy. Other fields could be signal processing, control, telecommunication, embedded systems, power systems and micro-electronics.

3.3.2 Classes

The next rank in the hierarchical classification is class, and in the field of power electronics this term is already used quite frequently to classify amplifiers and power converters. It defines the different methods, at a fundamental level, that can be used to convert the energy. In other words, a class categorizes based on how the transistors are used. For power electronics there exist two major groups: the class of linear amplifiers, in which there exist certain subclasses, such as class A, B, AB and C and the class of switched-mode converters/amplifiers, of which the subclasses are class D, E, F and switched-capacitor. Additionally, classes can be used to distinguish between direct and indirect power conversion.

Composite amplifiers

Amplifiers or power converters can also be constructed as a combination of two amplifiers from a different class (hybrid). Such amplifiers, where for example a linear amplifier is combined with a switched-mode amplifier, are known as composite amplifiers and they have been grouped in [51, 153]. Multiple topologies may arise from this strategy [37], and, for instance, in [103] an example is given of a composite amplifier applied in a gradient power amplifier. In [51] the strategy is used for an AC power source.

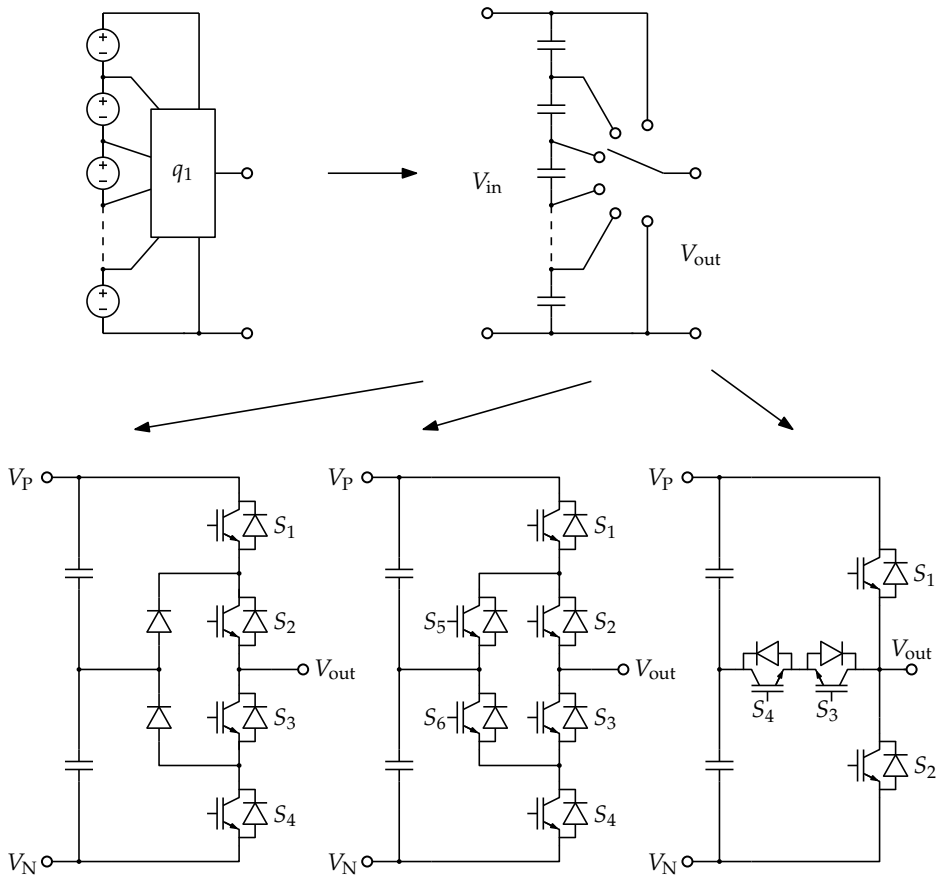


Figure 3.7: Stacked voltage source topologies (NPC, ANPC and T-type).

3.3.3 Families

As discussed in the introduction of this section, for power electronics it is the topology which defines the type. Different types of topologies can be grouped in families [78]. For instance, here, the families of multicell converters are discussed. All these families can be grouped together in a so called superfamily.

Family of stacked voltage multicell topologies

The first multicell converter family is the family of stacked voltage sources. It is based on the diode-clamped converter and the main characteristic of these types of converters is that the input voltage is shared over a set of series-connected

voltage sources. A number of switches, controlled by a switching function q , is then configured such that the desired output voltage can be selected. In Figure 3.7 this structure is depicted, and a number of types of converter topologies is shown. It can be noticed that the structure is very similar to an R-string DAC, and the structure has in the past been referred to as generalized multilevel converter [6,22,126].

One notable characteristic is that, when capacitors are used as voltage sources, the current in each branch between the capacitors should be kept zero on average, to keep the capacitor voltages balanced. As a result, these topologies have the limitation that the output waveform should be AC. And even with AC, waveforms at the nodes between the capacitors will slightly oscillate at (multiples of) the fundamental frequency. In multiphase converters, however, the common-mode current can be used as a control parameter to stabilize the voltages.

It can be seen that, from the structure shown in Figure 3.7, various multilevel topologies can be derived. For instance, the neutral-point-clamped converter or NPC, which was patented by R.H. Baker in 1978 [4] and first published by Nabae in 1981 [105]. Although the "neutral-point clamped converter" is most widely used, the name suggests that the topology has a neutral point, which is only the case for the odd-level variants. Consequently, in more recent publications the name "diode-clamped converter" is also used [13]. However, it should be mentioned that higher-level diode-clamped converters suffer from balancing limitations [119], and stable operation depends on load current and modulation index [139]. Therefore the number of levels for this type of topology is in practice limited to three. When more than three voltage levels are used, most often additional hardware is required to ensure that the voltages remain balanced [131,139].

One of the major drawbacks of the diode-clamped topology is the asymmetric loss distribution among the switching devices [125]. As a consequence, alternative topologies have been searched for, such as the Active-NPC (ANPC) [12] or the T-type topology [137] in which the distribution of the losses among the switching devices is improved. It can be seen in Figure 3.7, that these topologies can be classified as different types.

Family of series multicell topologies

The second multicell family differs from the stacked voltage source family in the sense that the voltage sources are not directly connected in series, but instead entire power stages (cells) are connected in series. In fact, there exists a large current loop, containing the load and all cells. The switching function is now

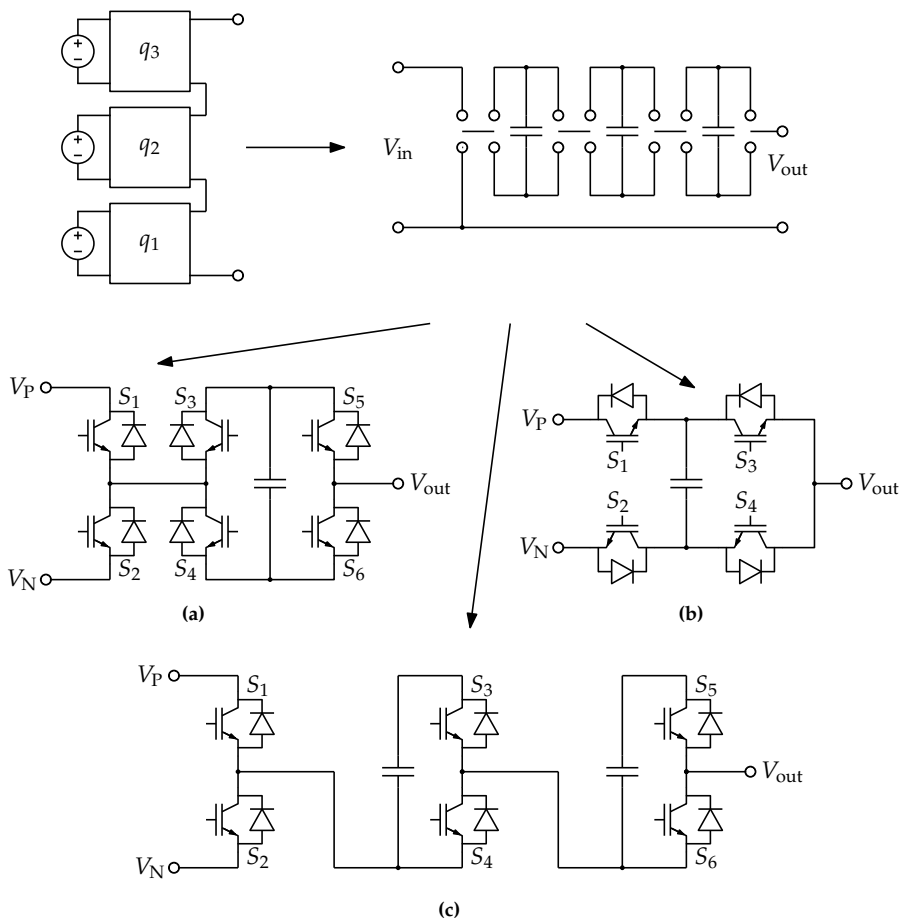


Figure 3.8: Examples of different type of topologies within the family of series multilevel converters (a) Series-connected H-bridge (b) Flying-capacitor (c) MMC arm.

such that a particular cell can be included or excluded in the chain. Also for this family a general structure can be defined, which is shown in Figure 3.8. Such an abstract general structure is very often used in papers to explain the operation of the topology. For instance, in [149, 150] the structure is used as a model for the flying-capacitor topology. The main purpose of such an abstract structure is to show the fundamental operation of various multilevel converters and to reveal similarities. In other words, in all these series multicell topologies the main function of the switches is to add or subtract a voltage source for generating a specific voltage level.

Every cell can be implemented with either a voltage source or a capacitor. However, if more than one cell is implemented with sources, then the sources need to be isolated. A disadvantage is of course the fact that in practice such sources require relatively a lot of hardware, which adds to the size and weight of the amplifier. In Figure 3.8 it is shown how with the use of a capacitor in the remaining cells the general structure leads to a different abstract structure, in which in the most generic way, the switching function is created by two SPDT switches. When implemented with capacitors the switching function should be constructed in such a way that the capacitor voltage is being balanced. In other words, a capacitor-based module will not be able to deliver any continuous active power.

A very popular series multicell topology, applied also in industry, is the flying-capacitor topology [28, 79, 98, 127, 130], which was developed at the end of the previous century [41, 97]. An interesting feature is that when phase-shifted carrier modulation (PSC PWM) is used, natural balancing [150] of the capacitor voltages is achieved. However, with other carrier-based multilevel PWM methods, such as phase-disposition (PD PWM) [140], also open-loop balancing techniques can be found. Another example is given in [154], where the balancing control method has been combined with selective harmonic elimination PWM (SHE-PWM). The natural balancing can be also improved by using external balancing booster circuits [141]. For flying-capacitor converters with a high number of voltage levels, however, closed-loop balancing is required [143].

Depending on the application, two operating modes for capacitor-based series multicell topologies can be distinguished. First, the mode (balance mode) in which the balancing, open- or closed-loop, of the capacitor voltages is handled within one switching cycle. In this mode, all capacitor based cells produce on average no voltage, and the output voltage range is limited to the supply voltage. On the other hand, the capacitance of the capacitors can be kept relatively small. The second mode (limited-balance mode) refers to applications in which the capacitor voltage balancing is handled within the fundamental period of the reference. One can think of, for instance, DC-AC converters such as the MMC.

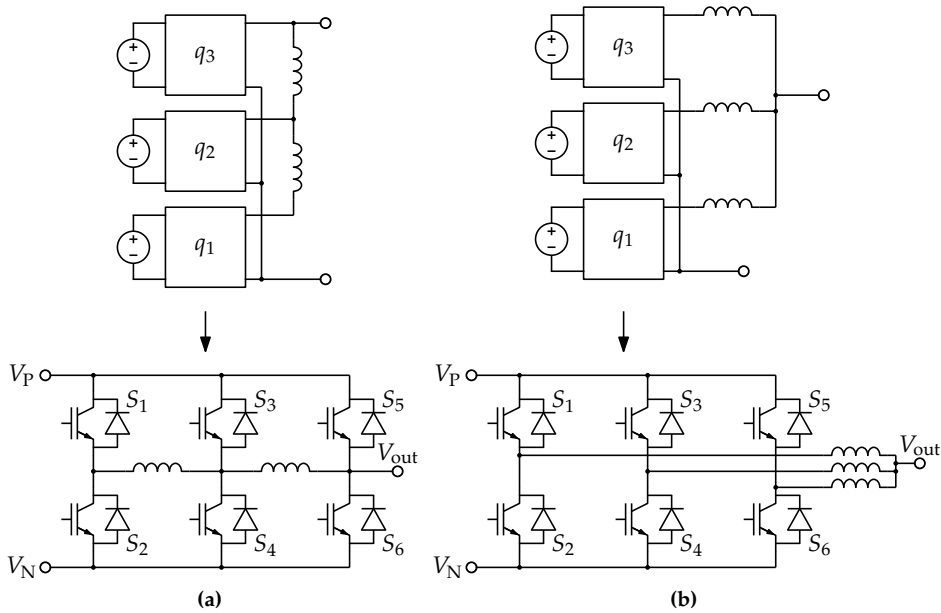


Figure 3.9: Two approaches for parallel multicell topologies, inductors are required in between the switching legs for the prevention of short circuits.

Family of parallel multicell topologies

The previous two families of multicell topologies resulted in structures in which the switching devices are placed in series. The series-connection leads to the advantage of sharing the input voltage over the multiple devices. Alternatively, one searches for approaches in which the output current is shared over the devices. In Figure 3.9 two parallel multicell alternatives are shown, in which the inductors are either star-connected or connected in between the switching legs. Usually, because a voltage is switched, a direct connection is only feasible when all switches are switched simultaneously. For out-of-phase switching, inductors are required to prevent a short circuit from one cell to another.

A more familiar name for the topology shown in Figure 3.9(b) is interleaved buck converter, where “interleaved” is referring to the PWM that is applied in such a converter. At the star-connection the ripple currents of the individual cells are summed together, and by using PSC PWM, an output current results which has a reduced ripple, due to the cancellation of harmonics.

Hybrid multicell topologies

The basic family structures can also be combined, resulting in hybrid topologies. An example is the combination of stacked voltage multicell topologies and series multicell topologies, the stacked multicell topology (SMC) [47], which can be seen as the combination of a flying-capacitor topology and a T-type topology. A combination of the ANPC and flying-capacitor topology results in either the 5L-ANPC or generalized P2 converter [112, 113]. An example of a topology in which series and parallel multicell topologies are combined is the modular multilevel (MMC) topology in which the MMC arm, from the series multilevel family is placed twice in parallel for a single phase. These multilevel alternative topologies are also shown in Figure 3.10.

3.3.4 Variants

The last rank in the proposed taxonomy is defined as variant. A variant gives us the ability to distinguish small variations of a certain type of topology. With variations it is possible to address different switching devices or other components. But also the use of additional circuitry, such as hardware used for balancing (i.e. balance boosters) or hardware to improve the switching behavior, for instance, to obtain ZVS/ZCS. Yet another interesting variant within the series multicell family is the inclusion of inductors in between cells [77]. A new cell arises, similar to a buck-boost structure by which the capacitors can be balanced. Also, because of the structure, capacitor voltages can be stacked on top of each other, resulting in higher-than the supply voltage output voltage levels.

Lastly, up to this point only single-phase half-bridge multilevel structures have been categorized and grouped. Multi-phase and full-bridge configurations are also considered as variants. In a full-bridge configuration the load phases are not connected to a fixed potential, and both sides of the load have a controlled voltage.

Balancing circuits

In both the stacked voltage as well as the series multicell topologies where capacitors are used for the creation of the voltage levels, the balancing of the capacitor voltages is a frequently discussed topic. As previously mentioned, on one hand, there is focus on the analysis of the open-loop natural balancing phenomena and the design of closed-loop balancing controllers. However, on the other hand,

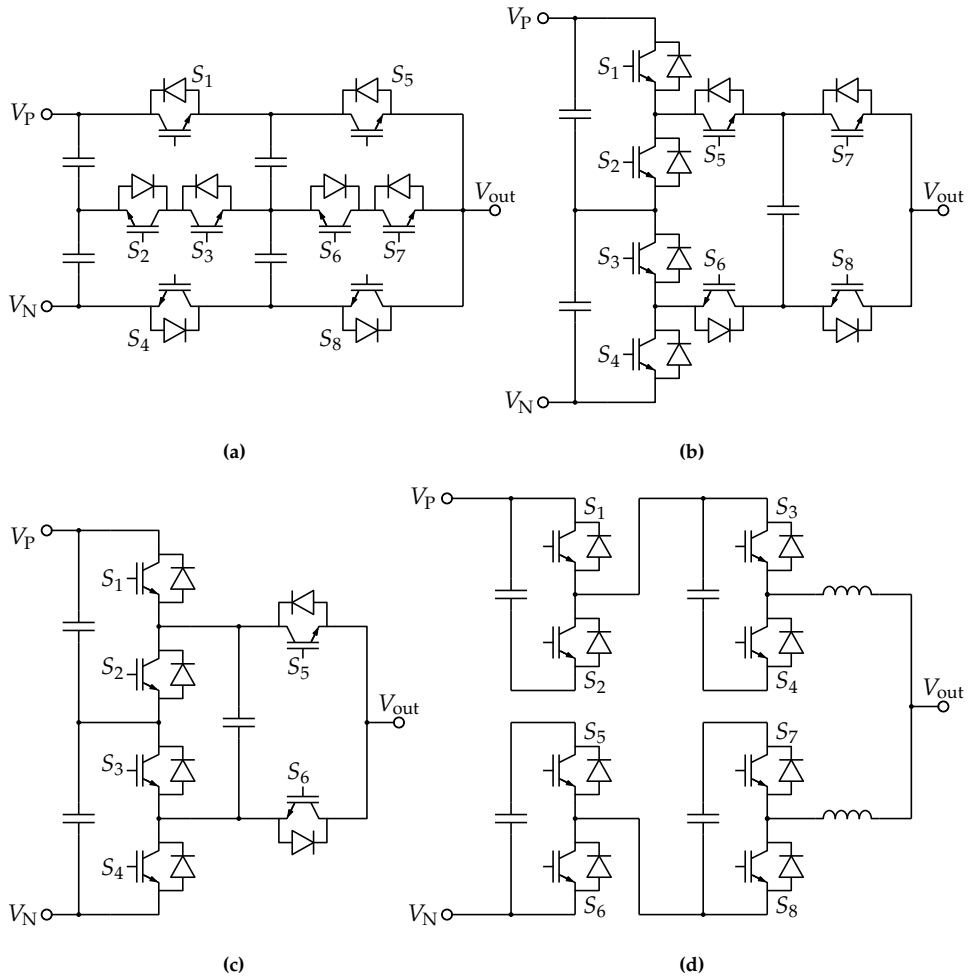


Figure 3.10: Family of hybrid multicell structures (a) Stacked Multicell Converter (SMC) (b) 5L-ANPC (c) Generalized P2 (d) MMC.

these approaches may not be sufficient or applicable, and additional hardware is then required for balancing the capacitors.

As an example, natural balancing in converters can be improved by using a so-called balance booster. A balance booster is an additional passive network, mostly connected to the output of the converter with which the natural balancing time-constants are changed. As a result faster balancing is possible. In [102] an example is given of the use of a balance booster in a stacked voltage power converter, and in [91, 141] an example of a balance booster in a flying-capacitor converter can be found.

Asymmetric voltage levels

In the late 90's the "binary" multilevel inverter [58] and "new approach" in multilevel power conversion [27] were among the first publications in which asymmetric multicell approaches were introduced. In these two papers the ratio between the voltage levels between two adjacent cells is a factor two. It should not be a surprise that shortly hereafter also a factor three was proposed [83]. With the use of different voltages for the cells also proposals arose where the switching devices and the switching frequencies are different, for which, ironically, the term hybrid was chosen [84, 92, 122]. It should be noticed that these first asymmetric proposals are based upon series-connected cells with isolated voltage sources as supply. Capacitor-based asymmetric converters are only found quite recently, such as in [32], where the topology of Figure 3.8(a) is applied with staircase modulation in limited balance mode. This strategy has been further investigated in [21, 70, 117].

Compared to an asymmetric approach, a symmetric approach has the advantage that a cell can be designed once, and that, as a result, the system is more easily extendable. It is said that the system is modular. With asymmetric approaches, however, one has the possibility to optimize each cell for the given parameters and more voltage levels and a higher effective switching frequency can be reached with fewer components.

3.4 Symmetric and dual relations

In the previous section a classification of multicell converters has been presented. Besides categorizing and grouping, equivalence and dual relations provide a powerful tool in the analysis of circuits [29], and the principle of duality has been used many times in the past in lumped-parameter modeling to provide electrical

engineers more insight into electronic circuits. This principle can also be applied to power-electronics networks. One can imagine finding a relationship between different types of converters [7] and using the technique to extend, for instance, modulation or control strategies to other converter topologies [71, 90]. As an example, in 1979 it was shown how four basic switching DC-DC converters - the boost, the buck, the buck-boost and the Ćuk converter - can be related by using the duality principle [8, 26]. Coincidentally, the concept of the canonical switching cell [75], which is itself dual, was introduced with the same intention, that is, to show the relationship between different switching topologies.

These examples show that there is a need for generalization of topologies in power electronics theory, especially as the hybrid multilevel structures become more complex. Two approaches for the generalization process in literature can be identified: First, the introduction of basic switching structures [144] or generalized topologies [112], and secondly, the search for dual and symmetric relations between topologies [3, 96]. An example of equivalent circuits is shown in Figure 3.11, and with the use of circuit analysis tools (superposition and Thévenin's theorem) it can be shown that both circuits have identical behavior at the terminals [60]. The output voltage in the equivalent circuit is given by

$$V_{\text{out}} = \left(\frac{V_1}{L_1} + \frac{V_2}{L_2} + \frac{V_3}{L_3} \right) \cdot \frac{L_{123}}{L_x}, \quad (3.3)$$

where

$$\begin{aligned} L_{123} &= L_1 \cdot L_2 \cdot L_3 \\ L_x &= L_1 \cdot L_2 + L_2 \cdot L_3 + L_1 \cdot L_3. \end{aligned} \quad (3.4)$$

The equivalence shows the close relation between series and parallel multicell topologies.

Apart from the equivalence illustrated in Figure 3.11, duality can be seen as yet another form of equivalence. Dual relations have been found between the topologies shown in Figure 3.8(b) and in Figure 3.9(a) [25], and also a dual counterpart has been found of an interleaved topology with $M = 2$. A duality transformation for $M \geq 3$ can still be seen as missing link between series and parallel topologies [25], and in this section an extension of the classical duality theorem is used for the establishment of the dual counterpart [16].

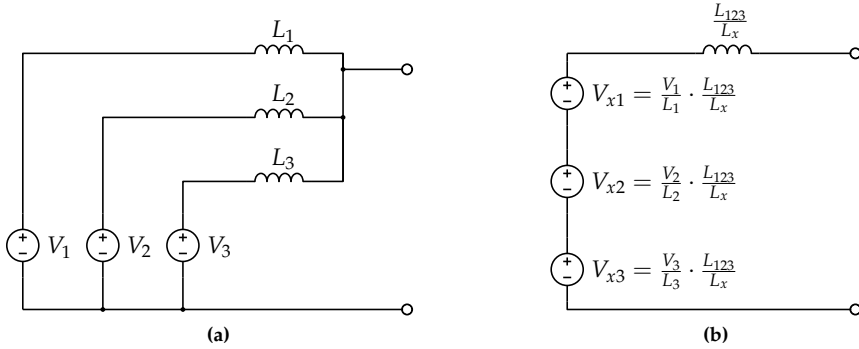


Figure 3.11: Equivalence between parallel and series multicell converters.

3.4.1 The duality principle and dual converters

A dual transformation of an electric circuit results in a circuit which has equivalent behavior, but currents and voltages are exchanged. The duality principle is not a concept which is limited to circuit theory. In many other fields such as mathematics and physics, the concept of duality is also used. However, there is no proper definition of duality and there does not exist a mathematical description which generalizes all types of duality in all fields. The fact that the exact same transformation applied twice to something leads to exactly the original again could be seen as the main characteristic of duality between two objects, equations, etc. Originals and their dual objects have a unique symmetric relationship.

It is assumed that one important constraint to find the dual counterpart of a certain topology is planarity. In other words, it is not possible to find a dual of a topology which cannot be drawn as a planar graph (i.e. cannot be drawn such that it has no crossing branches). The buck converter with more than three cells is an example of such a non-planar topology. However, it can be shown that this assumption is incorrect, and that the duality principle can be applied to non-planar circuits, such as the interleaved buck converter with $M \geq 3$ mentioned above and multi-phase voltage source converters [71, 151]. To be able to find a non-planar dual transformation the concept of electrical duality as opposed to topological duality has to be introduced. A crucial step in obtaining electrical duality is the transformation of the original circuit to a functionally equivalent planar realization, i.e. which has the same properties imposed by Kirchhoff's current and voltage laws as the original circuit.

Two methods can be used for creating an equivalent planar circuit. The first

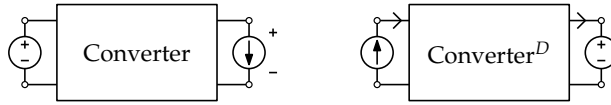


Figure 3.12: Converter shown as a two port element, and the converter dual.

method is to add ideal transformers, segregating the originally non-planar circuit into two planar circuits and thereby enforce constraints identical to Kirchhoff's laws to the new equivalent circuit [9, 151]. The second method is to evaluate each switching state of the original converter, assuming each state results in a planar circuit [71]. After obtaining a functionally equivalent planar circuit by either method, the classical method of graph transformation and interchange of elements is applied to find the topological dual of the planar equivalent circuit(s). Here, the first method is applied to a generalized interleaved topology, which is shown in Figure 3.9(b).

The interleaved buck topology has some interesting features, such as the unique characteristic that it is creating multilevel signals on both the input current as well as on the output voltage of the converter in contrast to the classical series multilevel converters, i.e. neutral-point clamped, flying-capacitor or cascaded topologies. In contrast to conventional multilevel topologies, interleaved topologies are characterized by switches connected in parallel, resulting in the property that current is equally distributed over the switching cells, instead of the property in which voltage is equally distributed over the switch devices. A circuit which has the property of a series connection of switches and the advantage of the interleaved converter will result in an interesting topology which may be useful in various applications.

Finding this topology could be accomplished by searching for the dual topology as shown in Figure 3.12. In this figure, the dual of a converter is shown and the converter is treated as a single element. One drawback in relating power amplifiers by means of duality is the restriction of handling the input and output sources and loads. If, for example, we choose our power amplifier to be in a configuration in which a voltage source is connected at the input and a current source at the output, then, consequently, a dual converter topology is found in which a current source is connected at the input and a voltage source at the output. This is a result which is based on the fact that a dual transformation of a cascaded connection of two-port elements results in a cascaded connection of the individual two-port elements [138]. For the dual transformation, here, the standard convention is used as defined in [43], which means that the current direction for all elements (also the voltage source) is always defined from the positive to the neg-

ative terminal. Care should be taken with the current/voltage directions. As can be seen, in the original circuit the elements have been placed such that the positive voltage is defined at the top nodes of the two-port elements. However, in the dual circuit this is not the case anymore and the elements are oriented such that the current is circulating through the cascaded connection. The dual topology can now be inverted, such that the topology is again a voltage-supplied current source configuration. However, it would be more convenient if the sources are uncoupled from the topology itself, because the primary interest is the converter dual. Afterwards, it is determined how sources should be connected, and it is defined what the input and output of the topology will be.

3.4.2 Application of the duality principle

Graph theory is a field within mathematics in which duality plays a major role, and it concerns all fundamental concepts related to graphs. Graphs are used to represent networks in various scientific fields; i.e. computer science, communication theory, electrical engineering etc. An electric circuit, built up from lumped elements, is an example of a network and can, therefore, be drawn as a graph. The duality principle is one of the tools in graph theory and it can also be applied to electric circuits. The dual circuit can be constructed by, first, drawing the electrical circuit as a planar graph, denoted as \mathcal{G} . After that, a transformation needs to be applied to the graph to find the dual graph $\mathcal{G}^{\mathcal{D}}$. By interchanging all the elements by their counterparts in the new graph, the dual circuit is found. This dual circuit has the property that the voltage over all the elements in \mathcal{G} is transformed into a current through the dual counterpart elements in $\mathcal{G}^{\mathcal{D}}$. The superscript letter \mathcal{D} is used to assign all terms which pertain to the dual graph. If the dual transformation is applied again to the dual circuit, then the original circuit will be found again.

The duality principle in graph theory is restricted only to planar graphs. That is because graph theory only concerns the geometrical outline of a graph and not the laws which are imposed on the network. These laws describe the behavior of the circuit, and, when taken into consideration, these laws give extra freedom. As already introduced in [9], the concept of topological duality as opposed to electrical duality needs to be defined. Topological duality refers to conventional duality as defined within graph theory, and this type of duality can only be applied to planar networks. Topological duality can be seen as exact duality between two circuits, because not only are currents and voltages dual, also the layout itself is dual. Electrical duality applies to non-planar electric circuits, as certain tools from electric circuit theory can be used to convert non-planar electric circuits into

a subset of planar circuits. In other words, electrical duality allows the conversion of a circuit to an equivalent circuit.

The duality principle applied to planar circuits

A dual transformation of an electrical circuit is explained in many textbooks about circuit theory [29] or graph theory, and a short summary and an example are given in this section. First, the concept of topological duality is defined:

Definition 3.4.1. *Two electric circuit networks \mathcal{G} and $\mathcal{G}^{\mathcal{D}}$ are each other's topological dual if*

- (a) *There is a one-to-one correspondence between all elements of \mathcal{G} and their counterparts in $\mathcal{G}^{\mathcal{D}}$ in such a way that voltages across elements in one circuit are represented as currents through their counterpart element in the other circuit.*
- (b) *There is a one-to-one correspondence between the meshes of \mathcal{G} and the nodes of $\mathcal{G}^{\mathcal{D}}$.*

The transformation consists of two steps. The first step is a so-called graph transformation. This is done by drawing the circuit as a simplified interconnection of nodes with branches, called a graph. Every branch represents an element and the element itself is not drawn. This is slightly different from the conventional way of drawing a circuit, where also nodes are sometimes drawn as an interconnection of nodes and branches. The dual graph can be found by putting nodes in every mesh, including the exterior mesh, of the original graph \mathcal{G} and interconnecting the nodes such that every branch is crossed once, which is shown in Figure 3.13(b).

Note that because often circuits have most of their elements connected to ground, a good starting point is to put the ground as the lowest node. Often, the node which is placed in the exterior mesh is used as the ground connection in the dual graph $\mathcal{G}^{\mathcal{D}}$. The second step involves the replacement of the original elements by their dual counterparts [43]. Further note that arrows have been placed in the graphs. These arrows indicate the current direction. When performing the graph transformation, the arrows should be placed counter-clockwise with respect to the original arrows. This leads to a correct current direction in the dual graph.

The duality principle applied to non-planar circuits

The application of the duality principle in graph theory only applies to planar circuits. When applied to non-planar circuits, problems occur because the graph

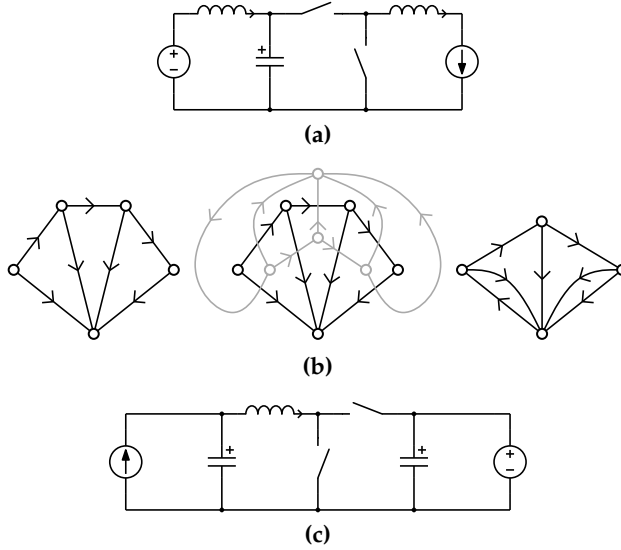


Figure 3.13: Example of a dual transformation applied to a power electronics circuit: (a) The example circuit (b) the graph transformation (c) the dual circuit.

transformation will not work properly. To verify whether a particular graph is planar or not, two specific non-planar graphs are useful to recognize. These two non-planar graphs are known as Kuratowski's graphs and are shown in Figure 3.14. K_5 is the non-planar graph with the smallest number of vertices, and $K_{3,3}$ is the non-planar graph with the smallest number of edges. The theorem of Kuratowski states that \mathcal{G} is planar iff \mathcal{G} contains no sub-graph $K_{3,3}$ or K_5 .

Methods in which duality is applied to non-planar circuits rely on the idea that the non-planar circuit first needs to be converted into a planar circuit. One can think of, for instance, the addition of elements and making certain branches unnecessary, or alternatively, by only considering the switching states. The resulting dual circuit will not be a topological dual circuit, because the graphs are not dual. However, the behavior of the circuits is still dual. Electrical duality is, therefore, defined as:

Definition 3.4.2. Two electric circuit networks \mathcal{G} and \mathcal{G}^D are each other's electrical dual if the electric circuit \mathcal{G} is equivalent to an equivalent circuit \mathcal{G}^{eq} and \mathcal{G}^{eq} is topologically dual with \mathcal{G}^D . By equivalence, here, is meant that \mathcal{G} and \mathcal{G}^{eq} have identical behavior.

Basically, this definition means that the duality principle is not applicable for all the elements in the entire circuit. Only certain voltages or currents, which are of interest, are considered. For a power electronics circuit this means that we are,

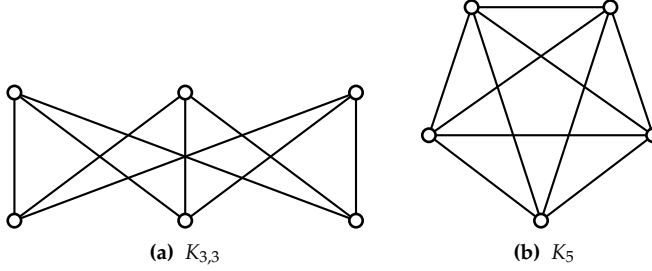


Figure 3.14: Kuratowski's graphs: \mathcal{G} is planar iff \mathcal{G} contains no sub-graph $K_{3,3}$ or K_5 .

for instance, only interested in a converter topology which has dual input and output behavior. In other words, the dual of the topology as a whole - defined as topological duality - is for these circumstances not of our interest.

Method of addition of transformers

One method of converting a non-planar electrical circuit into a planar circuit is the addition of transformers. Two types of transformers can be used, and depending on the non-planar circuit's layout a certain choice is more practical. The first type of ideal transformer is a junction transformer and it can replace a junction in a circuit. By placing one winding in each of the branches leading towards the node of interest, the junction transformer is actually enforcing Kirchhoff's current law (KCL) in that particular node. In other words, the junction transformer enforces

$$\sum i_k = 0, \quad (3.5)$$

where i_k is the k th current flowing in the node and k is the number of branches connected to the node (Note that we assume all coils having the same number of windings). The second type of transformer is the mesh transformer, and it is, obviously, the dual of the junction transformer. It enforces the Kirchhoff's voltage law on a certain mesh in the network, hence

$$\sum v_k = 0, \quad (3.6)$$

where v_k is the k th voltage in a mesh and k is the number of branches enclosing the entire mesh.

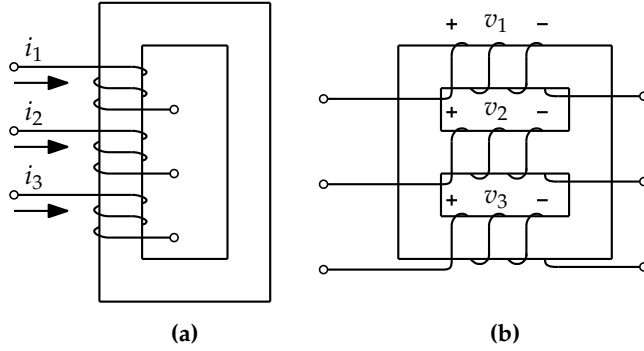


Figure 3.15: Example of (a) Junction transformer (b) Mesh transformer.

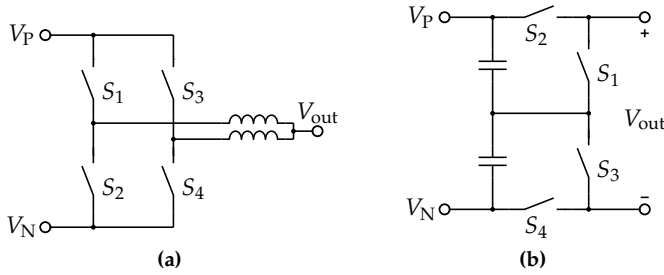


Figure 3.16: Dual transformation of interleaved topology, $M = 2$.

3.4.3 Simulation results

The most basic interleaved structure is shown in Figure 3.9(b). When M is defined as the number of cells which are connected in parallel, then $M = 1$ results in the canonical switching cell, which is self-dual. A dual transformation will, in this case, result in the exact same circuit again. The case $M = 2$ results in a planar graph, and a dual transformation can easily be applied. The result is shown in Figure 3.16. The case $M = 3$ results in Kuratowski's graph $K_{3,3}$, and, by definition, it is non-planar. In general, every interleaved converter with $M > 3$ has $K_{3,3}$ as a sub-graph and is non-planar too.

The dual of these non-planar interleaved converters can be found by adding a junction transformer in the star-connected output node, as discussed in section 3.4.2. After that, the node is connected to ground. By adding this ideal transformer the total circuit's behavior is not changing and the resulting circuit is, therefore, an equivalent circuit of the interleaved converter. This equivalent circuit is shown in Figure 3.17(a), and this equivalent circuit is actually a combina-

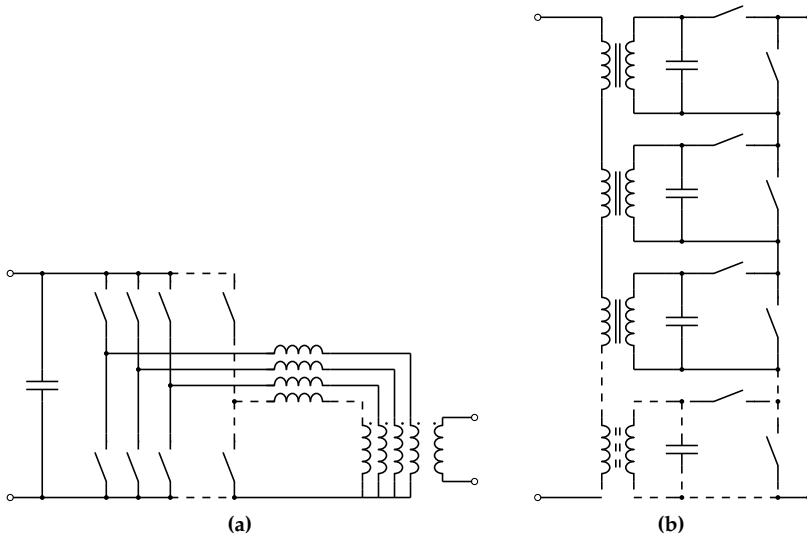


Figure 3.17: Dual transformation of interleaved topology, with (a) the equivalent circuit (b) the dual circuit.

tion of two planar circuits. As a result, these planar circuits can be transformed by using the graph transformation. The electrical dual circuit is shown in Figure 3.17(b).

Both the interleaved topology of Figure 3.9 and the dual topology of Figure 3.17(b) have been simulated in Matlab Simulink [88] by using the tool PLECS [118]. This is done by connecting a voltage source to the input of the topology and a current source to the output as shown in Figure 3.12. The voltage source is set to 100 V and the current source to 100 A. In both topologies phase-shifted carrier pulse-width modulation has been used. The reference is a sine wave of 5 kHz, and the switching frequency is 20 times higher than the reference frequency, 100 kHz. The inductance of the inductors in the interleaved topology amounts 500 μH , and the capacitance of the capacitors has the same value in Farads. The results of this simulation are shown in Figure 3.18. It can be seen that the converter is creating both multiple input and output levels, and that these waveforms are identical for the interleaved converter and the interleaved dual converter. Hence, this simulation shows that the topologies are each others electrical dual. Also the waveform of the currents through the inductors in the interleaved topology are identical to the waveform of the voltages across the capacitors in the interleaved-dual topology, as can be seen by comparing Figure 3.18(b) and Figure 3.18(d).

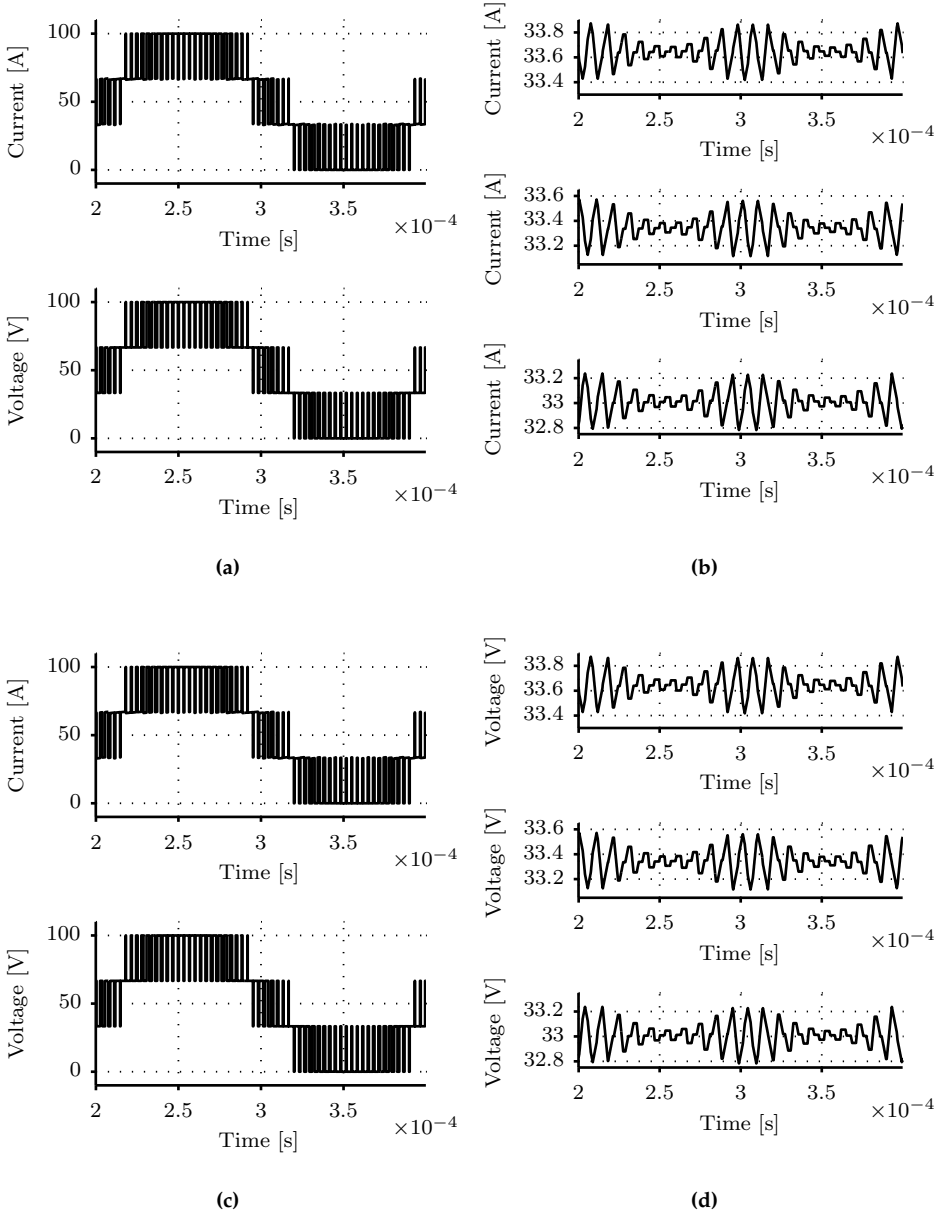


Figure 3.18: Simulation results showing dual behavior between the two topologies, for the interleaved converter: (a) The input current and output voltage (b) inductor currents and for the interleaved dual converter: (c) The input current and output voltage (d) capacitor voltages.

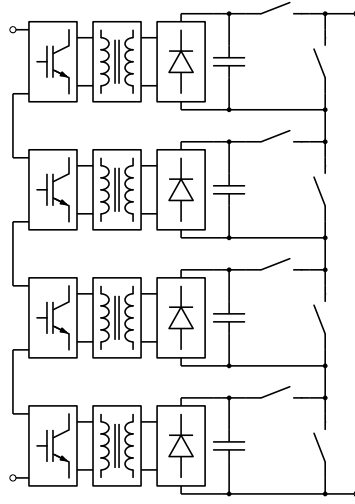


Figure 3.19: Transformers replaced by isolated DC-DC converters.

Unfortunately, the dual topology in Figure 3.17 has no direct practical use. The transformers which have been added are assumed to be ideal, whereas real transformers are not able to transfer both DC currents and voltages. It is not possible to remove the transformers in the dual circuit. Evaluation of both circuits reveals that the star-connection of the switching cells in interleaved converters results in a common voltage for all the switching cells at the output. This property has to be transformed in the dual circuit into a common current for the series cells and this can only be obtained when the switching cells are isolated from each other. The series connection of the ideal transformers ensures that all the switching cells will have the exact same current.

As a solution, the transformers could be replaced by isolated DC-DC converters. This is shown in Figure 3.19. As it was allowed to add transformers, the addition of such ideal converters does not influence the multilevel input/output behavior. However, in these type of multilevel converters usually the DC-DC converters are connected in parallel at the input side. The input-series connection of the isolated DC-DC converters (dual-active bridge) is also employed in practice, although the output is then connected directly either in series [49] or in parallel [35]. Here, each output consists additionally of a half-bridge cell which all are connected in series, and the entire output stage can be seen as an MMC arm.

3.5 Summary

In this chapter an overview was given of existing multicell topologies for the generation of multilevel waveforms, and these topologies have been categorized by means of a multi-layer taxonomy. Simulations, in which the effective switching frequency has been kept the same, have been used to demonstrate how multiple voltage levels can lower the quantization distortion. This effect becomes larger as the number of levels increases. It is also shown for $N = 5$, and with the use of APOD, how sampling distortion is significantly higher. The simulations also show a decrease of the switching frequency harmonics when increasing the number of voltage levels and an approximation is presented indicating how using voltage levels reduces the filter size. The chapter ends with the establishment and derivation of the interleaved dual circuit. For this result the duality theorem was necessary to be discussed and extended.

Chapter 4

Synthesis of a PowerDAC

“If you really want to understand how something works, build it yourself.”
(Jim Williams)

4.1 Introduction

In the previous chapter a classification of existing multilevel circuits has been proposed. Also, it was shown how composite amplifiers are constructed as a series or parallel connection of a switched class-D main amplifier and a linear correction amplifier. In this chapter the development of the series multicell topology is continued, and a composite amplifier is constructed in which both amplifiers are switched amplifiers. The proposed topology, which will be referred to in the following as the PowerDAC topology, is shown in Figure 4.1. The topology is not new and has been investigated in recent years, mostly for three-phase drive or grid-connected systems [31, 32, 85, 114, 127, 155]. The novelty, or main contribution, of this chapter is the configuration (the selection of capacitor voltage values and switching frequencies of the cells) and its associated modulation/control strategy.

The fundamental idea is as follows: One starts with a main amplifier, which is the amplifier one would like to improve, and, in series to its output, a number of subsequent correction amplifiers is connected. In this particular situation the most basic two-level switching leg is chosen, but the main amplifier itself could already be a multicell topology. Here, the correction amplifiers each have a conventional H-bridge structure, but also for the correction amplifiers alternative switching

4.2 Definitions

Main amplifier

The first half-bridge in Figure 4.1 is referred to as main amplifier, and will be denoted by c_0 , because it can be seen as the amplifier which is responsible for delivering the active power to the load. This cell is operated in such a way that the output voltage reference is tracked, that is, it is operated as if there would not be any other H-bridges connected in series. It is also the only amplifier that has a voltage source as input. This main amplifier defines the switching frequency of the PowerDAC, which is defined as f_{sw} and the amplitude of its switched output voltage $v_{sn0}(t)$ is equal to the supply voltage V_s . When the main amplifier itself is a multilevel converter, the number of levels is denoted as N_0 and the level voltage as ΔV_0 . For uniform level voltages, the following equality holds

$$V_s = (N_0 - 1)\Delta V_0. \quad (4.1)$$

Correction amplifiers

All H-bridges which are connected in series to the main amplifier are referred to as correction amplifiers, and denoted by $c_1 \dots c_M$. Again, also for the correction amplifiers different topologies can be used. Because these correction amplifiers have no power source as input, their purpose is not to deliver any continuous active power. Instead, they are operated such that the square-wave voltage $v_{sn0}(t)$ produced by the main amplifier is corrected to the desired level. The number of correction amplifiers in a PowerDAC is denoted by M , the level voltage and the number of levels that can be created by the i^{th} correction amplifier are defined as ΔV_i and N_i , respectively.

Level uniformity and redundancy

Each correction amplifier contains a capacitor and, depending on the modulation strategy that is used, these capacitors will be charged to a certain nominal voltage. In principle, for every cell any capacitor voltage-level could be chosen, however, the designer of the modulation strategy must provide a method which ensures the balanced operation of the converter based on the hardware capabilities while at the same time guarantee the ability to provide the desired output voltage [59].

Furthermore, it is desirable to have a uniform distribution of the voltage levels which can be created by the converter, as it results in symmetric behavior. Otherwise, the control algorithm will be even more complicated. Unbalanced capacitor voltages lead in fact to non-uniformity. This subject is treated separately in Chapter 5. It should be mentioned that in the analysis of PCM signals in the past, one has searched for optimal levels for quantization to maximize the signal-to-noise ratio, for instance, μ -law or Lloyd-max optimization [81,89].

It would be interesting to find a set of conditions that defines uniformity for asymmetric multicell topologies (symmetric multicell topologies obviously have uniformity). Based on the uniformity condition in combination with the output voltage range, the number of levels can be determined. Similarly, it would be interesting to find the necessary conditions for balancing, in other words, the ability to balance by providing redundancy of the voltage levels. Given the configuration as shown in Figure 4.1, different capacitor voltages can be chosen. As a start, let us define $\forall i \in \{1 \dots M\}$, without loss of generality:

$$\Delta V_i \leq \Delta V_{i-1}, \quad (4.2)$$

which is the sorting definition for the PowerDAC, based on the level step size of each cell. The level step voltage, which is simply defined as the smallest ΔV_i , is given by the sorting definition, and equal to ΔV_M . Furthermore, the following definition is proposed:

$$\Delta V_i = k \Delta V_M, \quad k \in \mathbb{N}_1, \quad (4.3)$$

by which all other voltages are defined to be either equal to or integer multiples of the level step voltage. Given these two definitions, the uniformity condition is given by [86]:

$$\Delta V_{i-1} \leq \Delta V_M + \sum_{j=i}^M (N_j - 1) \Delta V_j. \quad (4.4)$$

The uniformity condition basically sets a maximum level voltage for the i^{th} correction amplifier. At the edge of the uniformity condition, that is when all correction cells fulfill (4.4) with an equal-sign, the maximum number of levels can be achieved. As a result, for series-connected power stages where voltage balancing is not a concern, that is, when separated isolated dc voltage sources are used, it is found that a factor three between the voltage levels can be used with H-bridge

$(N_i = 3)$ correction amplifiers.

For configurations in which (4.4) yields a less-than sign, certain levels can be created in multiple manners. Such levels are called redundant voltage levels. When capacitors are used, as in the PowerDAC, redundant levels are necessary, as it is a requirement for the ability to simultaneously balance the capacitor voltages and generate an arbitrary output voltage. Balancing of capacitor voltages in a correction amplifier is possible when a redundant level translates in the ability to both charge and discharge the capacitor for a given output level. For single-phase topologies the following condition needs to be fulfilled [85]

$$\Delta V_{i-1} \leq \frac{N_i + 1}{2} \Delta V_i. \quad (4.5)$$

Since H-bridges are used, the number of levels that can be generated per cell is $N_i = 3$, and the maximum voltage ratio between two adjacent cells is a factor two. In section 4.3 a modulation strategy is explained that has this feature and allows the balancing of the capacitor voltages while creating any desired output voltage at the same time.

Switching functions

Given a PowerDAC with a main amplifier and a set of correction amplifiers, a function for the output voltage can be determined based on switching functions. This leads to the definition of total switching functions q_t and difference switching functions q_d . The total switching function is the sum of the main amplifier's switching function and the difference functions (each describing the behavior of one H-bridge).

A switched-node voltage, the voltage between cell j and cell $j + 1$, can be defined based on the switching functions and nominal capacitor voltages as

$$v_{snj}(t) = q_0 \Delta V_0 + \sum_{i=1}^j q_{di} \Delta V_i, \quad (4.6)$$

where for $M = 3$, when all correction cells are H-bridges as in Figure 4.1, the three difference functions are given by

$$\begin{aligned}
q_{d1} &= q_2 - q_1 \\
q_{d2} &= q_4 - q_3 \\
q_{d3} &= q_6 - q_5.
\end{aligned} \tag{4.7}$$

So, the produced voltage of a correction amplifier is denoted by $v_{di} = q_{di} \triangle V_i$.

Operation modes

Redundancy does not exist for all possible states of the converter. Therefore, to reduce complexity, the states are classified into two categories. The first category comprises the states that lead to an output voltage or any switched-node output voltage within the range of the supply voltage. The remaining states are put in the second category. Two modes can now be distinguished:

- Balance mode: The PowerDAC amplifier is only operated such that the output voltage does not exceed the supply voltage.
- Limited-balance mode: The PowerDAC amplifier is operated such that the output voltage exceeds the supply voltage.

Limited-balance mode may be useful in AC applications, where it is known beforehand that the waveform is in limited-balance mode only for a limited amount of time. This operation mode then allows for an output voltage which is higher than the supply voltage and also the total number of levels is higher. However, the capacitors need to be sufficiently large to keep the voltage unbalance within certain limits. Also, the switching devices within the correction amplifiers need to be able to handle this unbalance.

In this thesis, the intention is to generate arbitrary waveforms, both AC and DC. Therefore, this chapter is only focusing on balance mode.

Switching frequency

Most state-of-the-art multilevel converters are based on a single switching frequency. For instance, in a flying-capacitor topology all switching devices have the same switching frequency, and they also have the same blocking voltage. In a PowerDAC, where the voltages of two adjacent cells divide by a factor two,

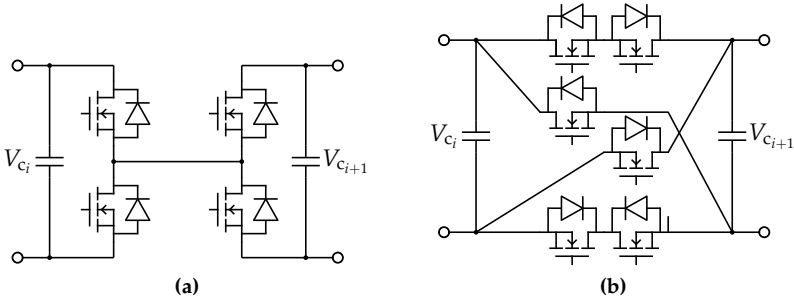


Figure 4.2: Two alternative switching cells (a) the switching cell between two H-bridges (b) alternative switching cell (cross-connected cell).

more flexibility for the synthesis of waveforms is achieved if the switching frequency increases every next cell. Like the nominal capacitor voltages, the switching frequency can also be chosen. The modulation strategy presented here results naturally in a doubling of the switching frequency in every following H-bridge. Notice that when a stress-factor for cell i is defined as

$$S_{fi} = k_1 \cdot \Delta V_i \cdot f_{swi} + k_2 \cdot I_i^2, \quad (4.8)$$

where f_{swi} is the switching frequency, I_i the current, and k_1 , k_2 constants, then this stress-factor remains constant for all cells.

Switching cells

In the PowerDAC, H-bridges are connected in series, which results in the switching cell that is shown in Figure 4.2(a). Other cell configurations are, however, also possible. An example is the so-called cross-connected cell, proposed in [20], and shown in Figure 4.2(b). Similar to the H-bridge cell, the cross-connected cell has the ability to connect the capacitors to each other in four different ways. When only two of the four ways are used, that is, when for instance the two top switches are switching simultaneously the switching cell reduces to a flying-capacitor switching cell. It shows again, as mentioned in Chapter 3, the close relation between the flying-capacitor multicell topology and the PowerDAC topology.

4.3 Modulation strategy - open loop

In this section a modulation or open-loop control method is proposed for the PowerDAC. This modulation scheme can be seen as an alternative to the already existing carrier methods (demonstrated in section 3.2.1) for the generation of a multilevel PWM waveform. For multilevel PWM, the modulation strategy is influenced by the selection of the voltage levels. For instance, when the same modulation strategy is applied which is most commonly applied in the flying-capacitor topology (PSCPWM), a natural balancing occurs, and the voltage difference between the cells will be equal to $\frac{V_s}{N}$.

Figure 4.3 shows the basic principle of the modulation strategy. In this example a waveform with a normalized voltage of 0.875 is created. As can be seen, both the voltage and time axis have been normalized with respect to the supply voltage V_s and switching period T_{sw} , respectively. In Figure 4.3(a) the output voltage waveform of the main amplifier is depicted. The square-wave of Figure 4.3(a) can be "corrected" by adding another square-wave (shown in Figure 4.3(b)), resulting in the waveform shown in Figure 4.3(c). When comparing the output waveform with the original waveform created by the main amplifier it can be seen that the possible number of levels is increased from two to three. In other words, the amplitude of the square-wave is half the amplitude of the voltage created by the main amplifier. In addition, the effective output switching frequency is twice the switching frequency of the switching devices in the main amplifier.

The modulation strategy as just described can easily be extended for additional correction amplifiers. For instance, the output waveform of the second correction amplifier is shown in Figure 4.3(e). Note that the switching frequency of this second amplifier needs to be twice the switching frequency of the first cell. Also, the capacitor voltage of this cell is one-fourth of the input voltage. It can be seen, again, that the effective frequency of the output voltage has been doubled and that the voltage amplitude has been decreased by a factor two. In other words, the number of possible voltage levels has again been doubled.

The generation of the multilevel waveform in this manner has the disadvantage that sometimes multiple switching devices need to switch simultaneous to jump from one voltage level to another. In the waveforms of Figure 4.3 it can hardly be seen, because the switching edges lie exactly on top of each other. In practice, this simultaneous switching will cause spikes, because noise, jitter and dead time cause small differences between the switching instants and switching transition waveforms will not perfectly cancel each other. This is, however, a well-known issue in asymmetric series-connected H-bridge topologies, and therefore not a

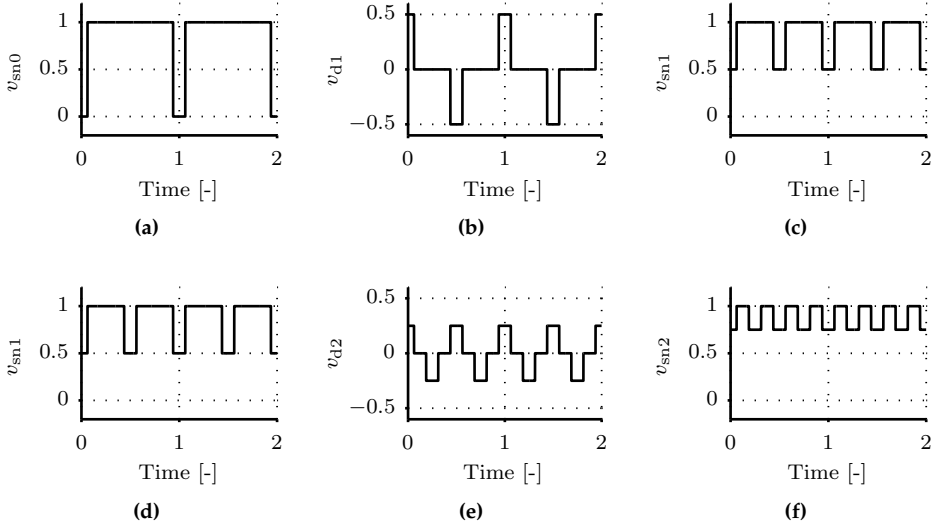


Figure 4.3: Waveforms of basic modulation scheme for a PowerDAC with 2 correction amplifiers.

direct consequence of the proposed modulation strategy.

As an aside, the creation of the three-level voltage waveform of one of the H-bridge correction cells can be done in two ways, because there are two possibilities for creating the zero-voltage vector. Either by enabling the two top switches or the two bottom switches. The difference between the two methods becomes important when the dynamic modification of the duty cycles is included in the modulation scheme. Furthermore, it should be mentioned that the switching function of the first correction cell can be set equal to the switching function of the main amplifier (refer to Figure 4.1 and set $q_0 = q_1$). As a result, these switching cells can be merged, eliminating two switching devices, and the main amplifier and first correction amplifier become a flying-capacitor cell.

The entire converter can easily be expanded by adding extra correction cells. With the proposed modulation scheme, for every extra cell the number of levels and the effective switching frequency doubles. In general, the number of levels amounts to $2^M + 1$ and the effective switching frequency is increased to 2^M . Compared to other single-source multilevel converters this is a significant advantage, as conventional multilevel converters, like the MMC or flying-capacitor converter, scale linearly in terms of number of levels and frequency when adding extra switches.

4.3.1 Calculation of the duty cycles

One may have noticed that the duty cycles (which will be denoted by d) for the various switching legs are not all the same. So, given a reference value, first, the nominal values of the duty cycles for all switching legs need to be calculated. The nominal value of the duty cycle of the main amplifier is simply the reference value, and its control is similar to a conventional two-level amplifier. For the correction amplifiers different duty cycles are required. Since the correction amplifier consists of two switching legs, two duty cycles need to be calculated. When no balancing is applied these duty cycles will be the same, such that the H-bridge on average creates zero voltage. However, when balancing is required, these duty cycles will be slightly different. Furthermore, the carriers of the PWM of the two switching legs are always 180° out of phase. This phase is not changed, because it defines the symmetry axis of the PWM waveforms.

In the previous subsection it has been mentioned how there are two methods by which the H-bridge cells can be controlled. For the first correction cell one can either choose to use the duty cycle d again or to use $(1 - d)$. For the second cell, the duty cycle needs to be doubled, because the cycle time has been halved. As a result, for the second amplifier $2d$ or $2(1 - d)$ is used. When the duty cycle exceeds 1, the modulo operation is used. So, in general, the nominal duty cycle for the n^{th} correction amplifier is $d_n \bmod (nd, 1)$ or $d_n = \bmod(n(1 - d), 1)$.

It should be mentioned that the modulator of the correction amplifiers has a different configuration in different sections. Therefore, first, the different areas should be recognized for each cell. As an example, when two correction amplifiers are used, two sections can be defined: $d_0 > 0.5$ and $d_0 < 0.5$. Then, for each section the phase-shift of the carriers is either 0° or 180° . Another possibility is to invert the output in the different sections instead of changing the phase-shift. A special case is the situation in which $d_0 = 0.5$. Since the first correction amplifier is already exactly canceling the voltage, creating an approximate dc voltage, the correction of other amplifiers is not necessary anymore. Therefore, for these cells $d = 0$ or $d = 1$ holds.

4.3.2 Alternative modulator

To overcome the determination of sections, an alternative method for the creation of the PWM is to use alternate phase-disposition PWM (see section 3.2.1). That is, not to change the duty cycle or phase-shift, but to modify the carrier and to define multiple carriers stacked on top of each other. To be more specific, for each

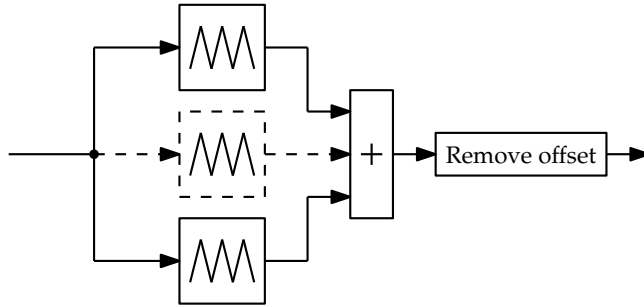


Figure 4.4: Generic modulator for the correction cells.

cell multiple carriers (carrier modulators) are introduced, of which the number depends on the cell number. For the second correction cell two carrier modulators with double frequency and half amplitude should then be used, for the third correction cell four carrier modulators are used and so on. A generic modulator results, which is shown in Figure 4.4. It should be noted that the output of even modulators (counting from top to bottom) is inverted.

When applying this method, the same duty cycle is applied to all modulators, and the resulting PWM waveforms are summed together. The resulting (sum) PWM waveform will have an offset which needs to be removed, assuming that it is desired to have a PWM waveform that switches between 0 and 1. An additional advantage of this alternative modulator is that it allows a continuous reference and also a natural-sampled PWM output can, therefore, be created.

4.4 Modulation strategy - closed-loop balancing

One of the major challenges in series multicell topologies is the balancing of the capacitor voltages. The proposed single-source multilevel topology and its modulation scheme can only be successful if the converter is able to balance its capacitors under all load conditions and for all modulation indexes. Similar to a flying-capacitor topology, the open-loop modulation scheme described in the previous section shows a natural balancing behavior when a resistive load is used. With an inductive load, both the balancing time-constants and steady-state capacitor voltages are changed. For the PowerDAC, the capacitor voltages can even become unstable with a high-inductive load. Closed-loop balancing is, therefore, for this topology and modulation scheme a requirement.

For now, two possible balancing fixed-frequency modulation schemes are distin-

guished. Either the modulation sequence or the switching transitions are fixed for any given reference. When the transitions are fixed, the optimal state of the converter at each transition is determined by a controller. This can be implemented in multiple ways. One method would be by selecting the optimal switching state given the sign of the voltage error of all the capacitors. Another method would be a space-vector based modulation algorithm, in which the optimal switching states are also chosen given the voltage error. Such balancing controllers have a very heuristic or hysteresis-like behavior.

In the method proposed here, the modulation sequence is fixed, and the transitions are not. Fundamentally, the approach of all methods is identical, because they are all based on using redundant states of the converter. In other words, under nominal conditions, the switching patterns of these methods is identical. It should be stressed, however, that in this case the redundant states are not selected to correct for voltage deviation, instead, the pattern is designed in such a way that these states are always applied. Slight modifications in the duty cycle cause an internal energy flow among the correction amplifiers, and this flow is used to balance the capacitor voltages. It is this second method, and the basic calculations for the duty cycles to control the unbalance, which is explained in the following sections.

As a start, the nominal waveforms which are created by the correction amplifiers are investigated. These are shown in Figure 4.3(b) and Figure 4.3(e). Every switching cycle the waveform is symmetric around zero and, therefore, the mean of this waveform is also always zero, independent of modulation index or capacitor voltage. This is an important observation, as an unbalanced capacitor voltage is not influencing the average output voltage. In contrast to, for instance the supply voltage or supply voltages in symmetric series-connected H-bridges, of which an unbalance will influence the average output voltage.

Note that the same reasoning can be applied to any other distortion that is symmetrical within one switching cycle. An exception, however, is for instance distortion due to dead time, which results in a voltage error that is depending on the output current polarity. For the main amplifier the distortion due to blanking-time results in similar distortion as in conventional two-level power amplifiers and its effects and solutions are well-described [132, 134]. For the correction amplifiers the blanking-time distortion leads to two negative effects. First, since the current, during the blanking time, can flow through both the diode as well as through the dc-link capacitor of that particular correction cell, the correction amplifier will produce a non-zero average output voltage. As a result, this non-zero voltage affects the output voltage. The second effect is that the capacitor can get unbalanced. Interestingly, a closed-loop balancing controller compensates for the

unbalance, thereby, also compensates for the error created by blanking time.

Furthermore, with a constant output current, the average capacitor voltage remains constant. However, if the current is not constant and contains harmonics of the switching frequency, the capacitor voltage can become unbalanced. To be more precise, uneven harmonics of the current through the capacitor will not affect the capacitor voltage, but even harmonics will. These even harmonics can lead to a different equilibrium point up to the case that the system becomes unstable. Consequently, it is required to measure the capacitor voltage and slightly adjust the duty cycle of the various switching cells to keep the capacitor voltages balanced.

To illustrate this, first, it is demonstrated what happens with the output voltage if one of the capacitors is unbalanced. Two situations are now investigated for the PowerDAC configuration with two correction amplifiers:

- Case 1: Correction amplifier 1 slightly unbalanced
- Case 2: Correction amplifier 2 slightly unbalanced

Additionally, it is explained what the corrective action should be. When multiple capacitors are unbalanced the corrective action is simply the superposition of the individual corrective actions.

Suppose the (normalized) capacitor voltage of the first correction cell is slightly unbalanced and amounts to, for instance, 0.4 instead of 0.5, then this unbalance will have its effect on the output voltage waveform. As a result, the voltage will jump from 1 to 0.6 back to 1 and then to 0.4 in one switching cycle, as shown in Figure 4.5(c). Despite the unbalance of the capacitor, still, the right amount of volt-seconds is created. However, the fundamental switching frequency harmonic will be present in the output voltage.

To adjust the unbalance of 0.1, during one switching cycle, or more switching cycles, the positive pulse of the H-bridge waveform should be made slightly shorter and the negative pulse slightly longer, such that on average the cell has created a negative voltage and absorbed power. Inevitably, this change will have its consequences on the output voltage. Therefore, an adjustment of the duty cycle of the main amplifier is also required. Furthermore, for the minimization of the distortion in the output voltage waveform, it is desired that when a transition between two voltage levels requires multiple switching transitions, that these transitions occur simultaneously. In Figure 4.5 an unbalance in correction amplifier 1 and the applied correction is visualized, in Figure 4.6 similar waveforms are shown for the situation that the capacitor in correction amplifier 2 is unbalanced.

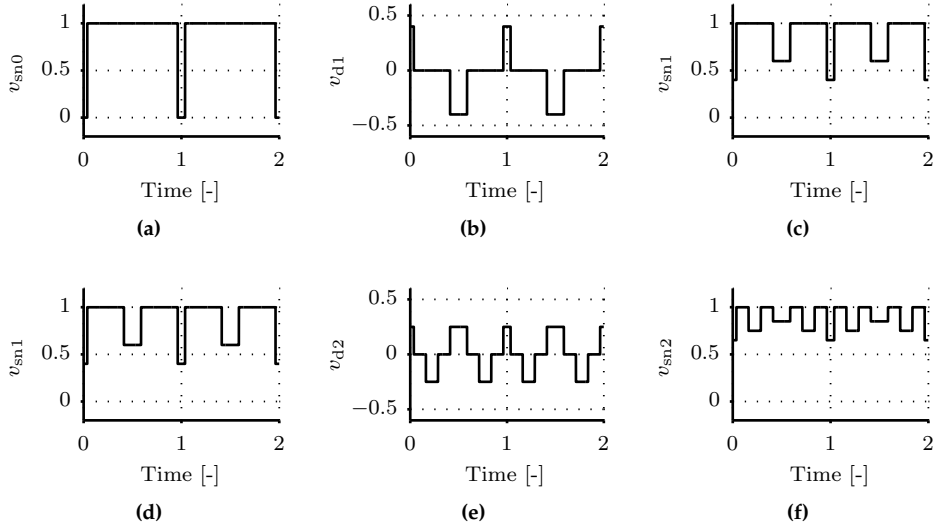


Figure 4.5: Waveforms of basic modulation scheme for a PowerDAC with 2 correction cells and in which the capacitor voltage of correction amplifier 1 is slightly unbalanced.

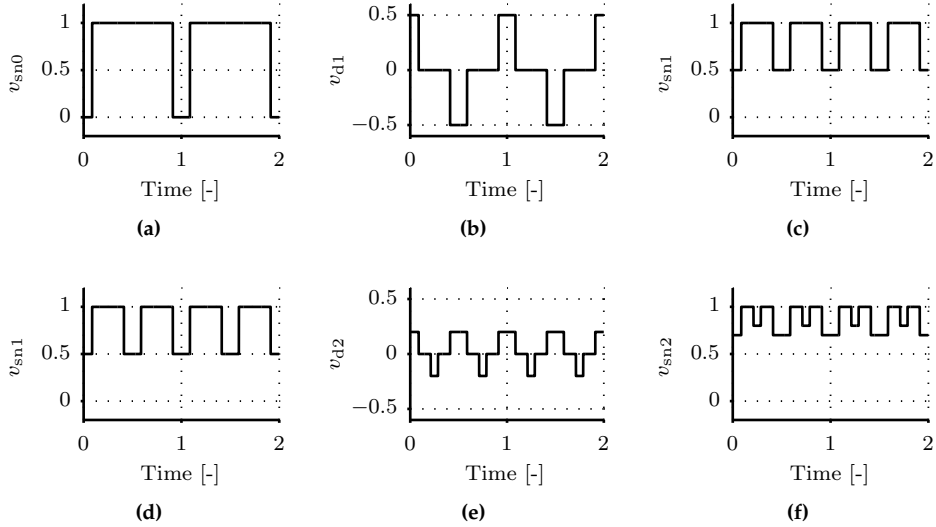


Figure 4.6: Waveforms of basic modulation scheme for a PowerDAC with 2 correction cells and in which the capacitor voltage of correction amplifier 2 is slightly unbalanced.

When implementing the balancing algorithm, and adjusting the duty cycles, some limitations need to be addressed. As has been mentioned before, an unbalance has in principle no effect on the output voltage (that is, the volt-seconds of one cycle of the fundamental switching frequency remains unchanged). However, when the PWM is adjusted for correction, this statement is not valid anymore. As a starting point, here, the balancing PWM adjusts only in such a way that this feature remains true assuming nominal constant voltages. It means, for instance, that limits have to be set on how much the duty cycles can be changed. In chapter 5 a more detailed analysis of unbalanced capacitor voltages is performed, where the focus of attention will be on the decoupling of the controllers.

4.4.1 Adjusting duty cycles

The balancing method is a closed-loop control method. It means that the voltages are measured, the error (i.e. the voltage with respect to its nominal value) is calculated and a compensator is used to bring this error to 0. The compensator is thus generating a setpoint u (defined between $[-1, 1]$) and here it is described how the PWM modulator adjusts the PWM waveforms. The explanation starts with Figure 4.5 and 4.6, where it is shown how an unbalance in the capacitor voltage influences the output voltage. Also, the pulse pattern is shown that is required to compensate for this error. As a result of the compensation, the resulting intermediate sum voltage changed, as it is not symmetrical anymore. Therefore, it is necessary that all the following correction amplifiers slightly change their pulse patterns.

This problem can be solved in two ways, either one chooses to calculate two duty cycles, one for the first cell and one for the second cell, or one calculates a phase-shift for the carrier. Both methods have the same result and it depends on the implementation environment which method is the most suitable. First, a duty cycle adjustment is explained, then, in the next section a phase-shift correction is described.

The duty cycle for the main amplifier d_0 can be calculated with

$$d_0 = \frac{1}{2} + \frac{1}{2}u_{v_{out}} - u_{V_{C_1}} - u_{V_{C_2}}, \quad (4.9)$$

where $u_{V_{C_1}}$ and $u_{V_{C_2}}$ denote the requested correction of the compensator. From 4.9 it can already be seen that there is a limit on the values of $u_{V_{C_1}}$ and $u_{V_{C_2}}$, because the duty cycle value d_0 is limited to $[0, 1]$. For that reason, an additional

algorithm is required to prevent exceeding the maximum borders. The duty cycle of the first correction amplifier can be calculated by using

$$\begin{aligned} d_{11} &= \frac{1}{2} + \frac{1}{2}u_{v_{out}} - u_{V_{C_1}} - u_{V_{C_2}} \\ d_{12} &= \frac{1}{2} + \frac{1}{2}u_{v_{out}} + u_{V_{C_1}} - u_{V_{C_2}}, \end{aligned} \quad (4.10)$$

where d_{11} refers to the duty cycle of the left leg of the correction amplifier. Note that this duty cycle is identical to the duty cycle of the main amplifier. For the second correction cell 4 duty cycles can be defined:

$$\begin{aligned} d_{311} &= \|u_{v_{out}}\| + u_{V_{C_1}} - u_{V_{C_2}} \\ d_{312} &= \|u_{v_{out}}\| - u_{V_{C_1}} - u_{V_{C_2}} \\ d_{321} &= 1 - (\|u_{v_{out}}\| + u_{V_{C_1}} + u_{V_{C_2}}) \\ d_{322} &= 1 - (\|u_{v_{out}}\| - u_{V_{C_1}} + u_{V_{C_2}}), \end{aligned} \quad (4.11)$$

then alternately the duty cycle is d_{311} / d_{312} for the right switching leg and d_{321} / d_{322} for the left switching leg. With the definition of the duty cycles as such, the value for the right switching leg needs to be inverted.

4.4.2 Adjusting phase-shift

While a slight deviation of the capacitor voltage results in a slight modification of the duty cycle in that particular cell, it will result in phase-shifted pulses in the other cells. To counteract this phase-shift the most logical solution is to apply a phase-shift correction in the other correction cells (instead of alternating the duty cycles). This can be seen as an alternative solution for ensuring simultaneous switching. Instead of alternating the duty cycles as in (4.11) of the faster stages, the phase-shift is alternated. The equations in (4.11) change into

$$\begin{aligned} d_{31} &= \|u_{v_{out}}\| - u_{V_{C_2}} \\ d_{32} &= 1 - (\|u_{v_{out}}\| + u_{V_{C_2}}), \end{aligned} \quad (4.12)$$

and an offset is defined as

$$\begin{aligned}\phi_1 &= 2\pi u_{V_{C_1}} T_s \\ \phi_2 &= -2\pi u_{V_{C_1}} T_s.\end{aligned}\tag{4.13}$$

The modulator of the second correction amplifier changes, because a phase-shift ϕ needs to be applied. Also in this case ϕ alternates between ϕ_1 and ϕ_2 . The calculation for the duty cycle of the main amplifier and the first correction amplifier are the same as described in the previous section.

4.4.3 Limiting the adjustments

The amount of correction which can be applied to the duty cycles is limited. That is because the first priority of the generated PWM signals is to generate the correct amount of volt-seconds of the output voltage. The reference controller may not be influenced by the balancing controllers. As mentioned before, it should be prevented that the duty cycles become too large or too small. For $0.5 \leq u_{v_{out}} \leq 1$ the following conditions hold

$$\begin{aligned}\|u_{V_{C_1}}\| + \|u_{V_{C_2}}\| + u_{v_{out}} &\leq 1 \\ \|u_{V_{C_1}}\| + \|u_{V_{C_2}}\| &\leq u_{v_{out}} - 0.5,\end{aligned}\tag{4.14}$$

and for $0 \leq u_{v_{out}} \leq 0.5$,

$$\begin{aligned}\|u_{V_{C_1}}\| + \|u_{V_{C_2}}\| - u_{v_{out}} &\leq 0 \\ \|u_{V_{C_1}}\| + \|u_{V_{C_2}}\| &\leq 0.5 - u_{v_{out}}.\end{aligned}\tag{4.15}$$

If the output of the compensator is too high, the corrective actions should be limited, otherwise, unwanted phenomena could appear. Limiting or saturating the corrective actions basically results in a temporarily lower gain. These equations show that a duty cycle of 0.5 is problematic, because at this duty cycle the capacitors cannot be balanced. The equations force the corrective action to be 0. The same holds for duty cycles of exactly 0 or 1.

These equations also show that when multiple corrections are requested a problem occurs, as an additional equation is required to choose how to saturate or limit. This problem can be solved in multiple ways, for instance, by setting priorities. In other words, first, capacitor 2 is balanced, then capacitor 1. Another solution is to limit by ratio, although the calculation of this solution contains a division, of which the calculation time can be costly.

4.5 Basic comparison with other multicell topologies

Comparing two power converter topologies is often seen as a difficult task, since many aspects are involved. Here, the purpose of the comparison is to reveal the strengths and weaknesses of the PowerDAC approach with respect to other multicell approaches. For this purpose a basic comparison is sufficient and a fully detailed comparative analysis is only necessary to find out the exact numbers of certain performance criteria (i.e. efficiency, size, cost etc.). The PowerDAC topology will be compared to a flying-capacitor topology, as the flying-capacitor topology is most similar to the PowerDAC topology, and the focus of attention is set on the most relevant differences, the stress of the switching devices and the size of the capacitors.

When comparing two topologies one aspect or parameter needs to be set equivalent. Here, it is chosen to fix the characteristics (the number of levels and the effective switching frequency) of the output voltage waveform. In other words, we pretend that the converter is a "black box" and define the behavior at the output terminals to be as close as possible. Subsequently, two aspects are highlighted. First, the number of switching devices and the stress that is experienced by these devices. And, secondly, the total capacitance and stored energy of the capacitors.

4.5.1 Switching devices and stress-factor

In the PowerDAC topology the voltage levels have been chosen in such a way that a high number of levels can be created. With the addition of only four switching devices the number of levels is doubled. Not surprisingly, compared to a flying-capacitor topology, the number of switching devices is significantly lower, especially for a high number of levels. In Figure 4.7(a), the number of switching devices is plotted with respect to the number of voltage levels.

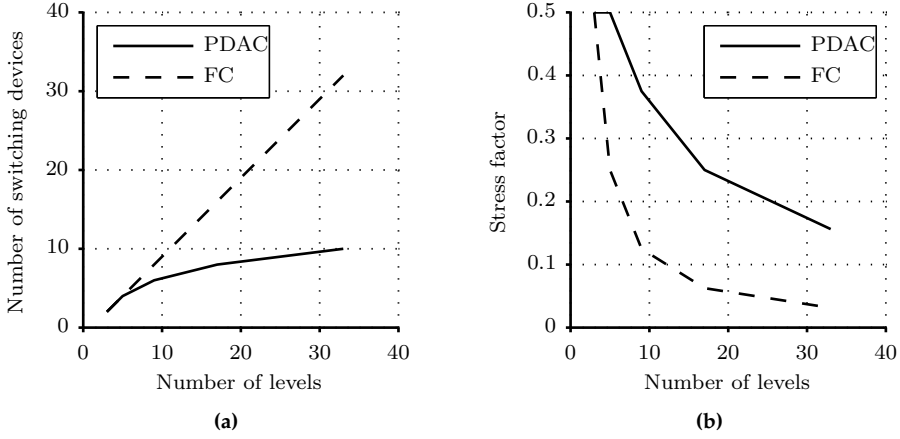


Figure 4.7: Graph of comparison between (a) number of switching devices and (b) stress factor as function of the number of levels for a flying-capacitor topology and the PowerDAC topology.

It should be noted that only looking to the number of devices can be misleading. For a more realistic comparison, a compensation is added for the voltage the switch needs to block, the current the device needs to conduct and the switching frequency of the device. Therefore, for a fair comparison, for each of the switching devices in both topologies the switch stress should be calculated. This stress has been defined in (4.8) and it gives an approximate indication for the total amount of losses in the switching devices, hence it is defined as “stress”. Since the current has to flow in all states either through the top or bottom switch in each switching leg, this component is, in this comparison, not relevant, and is therefore neglected. The total switch stress in the converter is then given by

$$S_{ft} = \frac{1}{(N_t - 1)f_{sw}V_s} \sum f_{swi} V_{bli}, \quad (4.16)$$

where V_{bli} denotes the blocking voltage of the switch. It can be seen that the total switch stress is normalized with respect to the supply voltage and the effective output frequency. The total switch stress is plotted in Figure 4.7(b) for $(N_t - 1)f_{sw} = 40 \text{ kHz}$ and $V_s = 100 \text{ V}$. From this graph the comparison gets a very different perspective. This result can be explained by “ineffective switching”. While in the flying-capacitor topology each switching actions leads to a transition to an adjacent voltage level, in the PowerDAC sometimes two or more switches need to switch simultaneously (as was explained in section 4.3).

4.5.2 Capacitors

Also the applied capacitors experience a stress and the resulting stress translates into the total capacitance which is required in the converter. Again, simply comparing the number of capacitors leads to a dubious result. The total capacitance of both converters can be compared in terms of the total energy storage of the capacitors which is required to guarantee a certain voltage ripple. First, the size of the required capacitive storage of the various cells is calculated. For the PowerDAC topologies the capacitance can be calculated by using

$$C_i = \frac{I_{\text{out}}}{2\tilde{V}_{C_i}f_{\text{swi}}}. \quad (4.17)$$

For the flying-capacitor

$$C_i = \frac{I_{\text{out}}}{(M+1)\tilde{V}_{C_i}f_{\text{swi}}}, \quad (4.18)$$

in which \tilde{V}_{C_i} denotes the worst-case peak-to-peak voltage ripple. Note that by using (4.18) the required capacitance for all capacitors in the flying capacitor topology is the same, while the capacitance in the PowerDAC topology has different values in each cell, because of the different switching frequencies. In Figure 4.8(a) the total capacitance in both converters is shown, which is approximately equal for both topologies. The resulting capacitance can now be used to estimate the total capacitor energy, which is related to the total volume of capacitors in the converter. The sum of the stored energy of all capacitors is

$$E = \sum \frac{1}{2}CV^2. \quad (4.19)$$

The total energy storage is shown in Figure 4.8(b). As shown, the stored energy for the PowerDAC is approximately two times smaller than for the flying-capacitor converter.

4.5.3 Discussion

Based on the basic comparison it can be concluded that the strength of the PowerDAC compared to the flying-capacitor topology is that it requires fewer components (switching devices/capacitors) to generate a certain waveform. However, fewer

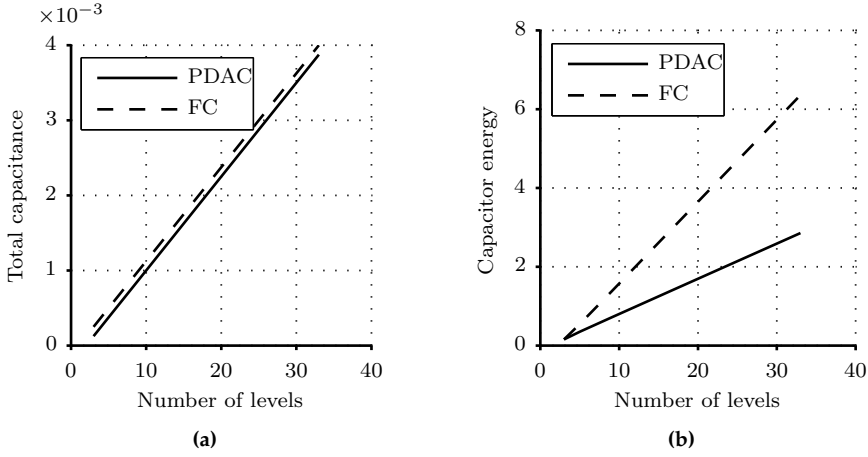


Figure 4.8: Graph of comparison between (a) total capacitance and (b) total stored energy in the capacitors as function of the number of levels for a flying-capacitor topology and the PowerDAC topology.

devices comes at the cost of “ineffective” switching in the PowerDAC. This “ineffective” switching can be qualified as resulting in a higher total switch stress in the converter. On the other hand, the higher switching frequency is beneficial internally, as the total energy in the capacitors is lower.

4.6 Simulation results

In this section the modulation method for the PowerDAC as proposed in this chapter is demonstrated. The circuit diagram of the simulated topology is shown in Figure 4.9 and the main parameters are shown in the Table 4.1. The topology consists of one main amplifier and two correction amplifiers, and, as explained in section 4.3, the main amplifier and first correction amplifier can be combined into a single stage. This simulated topology is the one that is also used to obtain the experimental results in Chapter 7. Detailed information about the experimental setup can be found in Appendix C.

All simulation models are built in Matlab/Simulink [88] in combination with the tool PLECS [118]. With the exception of the first simulation result, the simulation models have been set up in such a way as if they were implemented on a micro-controller. It means, for instance, that in the simulation C-scripts are used, which are identical to the C-code that is implemented on the experimental setup. The

following aspects are, therefore, taken into account:

- Resolution or time-quantization of the PWM and measured signals (9-bit).
- Sampling of the reference with an update frequency of 96 kHz.
- A one-cycle delay on both the reference and measured signals.

The topology itself and other hardware components, however, are considered ideal. No nonlinear effects, such as blanking time or parasitic components have been added.

4.6.1 The ideal PowerDAC and the influence of capacitors

In the first simulation the PowerDAC in combination with natural-sampled PWM and a purely resistive load is presented. It aims to demonstrate the influence of using capacitors for creating the voltage levels on the harmonic spectrum and a comparison is made between a PowerDAC with capacitors and a PowerDAC with ideal voltage sources. In this simulation the reference is a 1 kHz sine-wave and in Figure 4.10(a) the ideal (multilevel) voltage waveform of a PowerDAC is shown. Usually, when simulating, spikes occur at some of the switching events, due to simultaneous switching. In a simulation that is because of numerical errors, however, for the sake of clarity, these spikes have been removed. In practice, these spikes occur more often as the switching devices are not ideal and rise-times are finite. In Figure 4.10(c) the spectrum of this waveform is shown. For an ideal PowerDAC the first harmonics occur at the effective switching frequency (in this case 384 kHz), which is outside the scope of this graph.

In Figure 4.10(b) the voltage waveform is shown when capacitors (100 μF) are used. It is very hard to notice any difference in the time domain, although a ripple is present on the voltage levels. The difference is better visualized when evaluating the spectrum, and the result is shown in Figure 4.10(d). It can be seen that harmonics are now present at the (internal) switching frequency. Also, some baseband harmonics appear, because the ripple magnitude is correlated with the input reference. A solution for reducing these harmonics is to increase the capacitance of the correction amplifiers, and thereby lowering the peak-to-peak ripple.

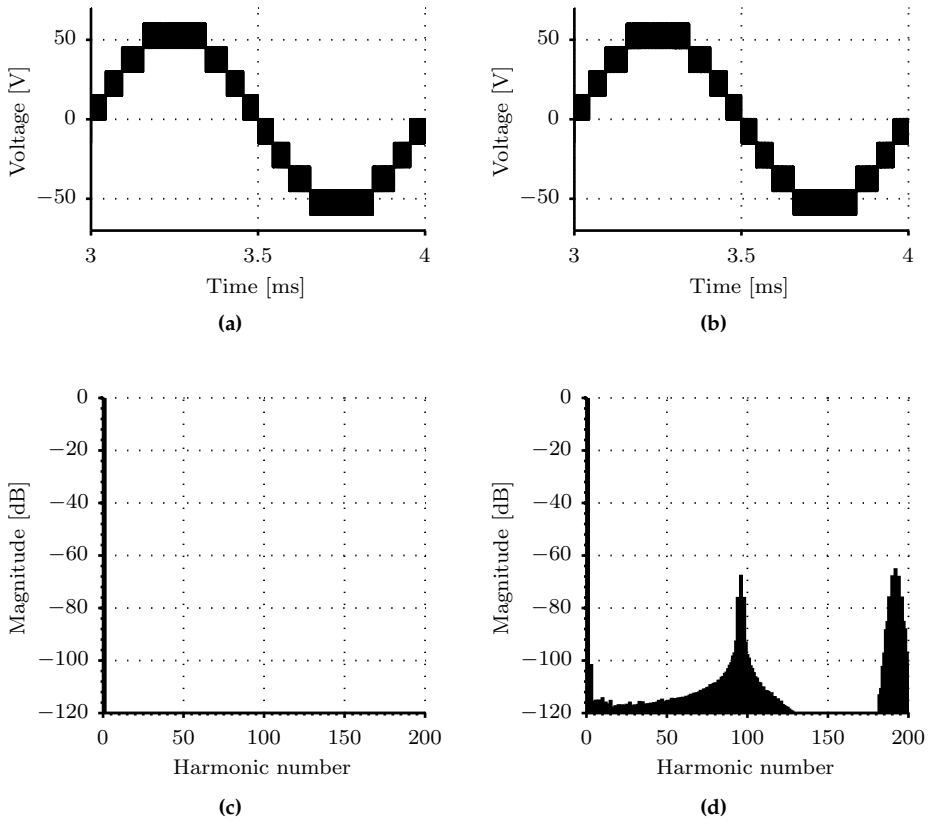


Figure 4.10: The switched output voltage and its spectrum (natural-sampled): (a) Voltage waveform with sources (b) Voltage waveform with capacitors (c) Spectrum of voltage waveform with sources (d) Spectrum of voltage waveform with capacitors.

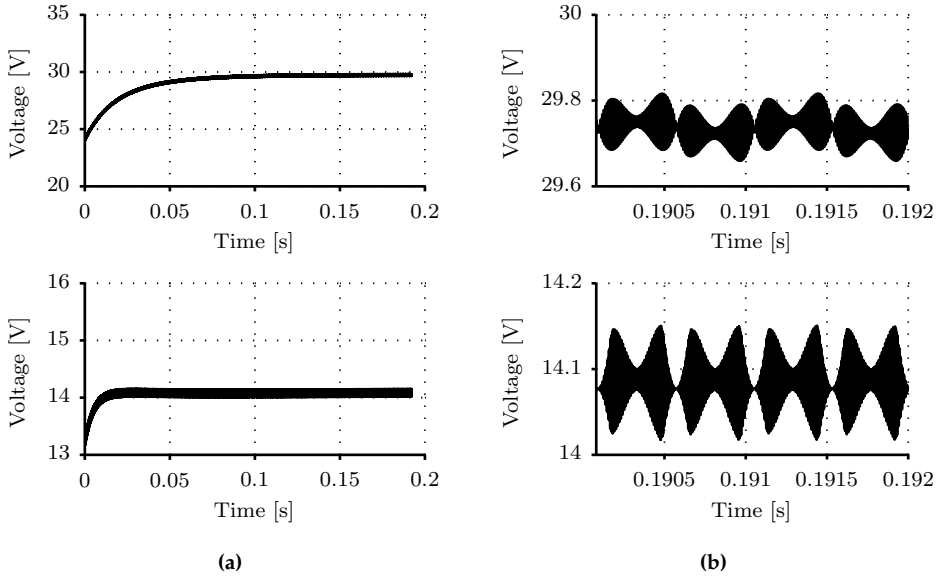


Figure 4.11: Simulation result of capacitor natural balancing showing (a) capacitor (C_{A1} and C_{A2}) voltage with initial offset, and (b) capacitor (C_{A1} and C_{A2}) voltage in steady-state (zoomed).

4.6.2 Natural balancing of capacitors

For the next simulation regular-sampled PWM is used (i.e. to obtain a more realistic simulation of the digital implementation). The purpose of this simulation is to demonstrate the behavior of the capacitor voltages when using open-loop modulation. With the filter and load parameters of Table 4.1 the PowerDAC shows, similar to flying-capacitor converters, a natural balancing phenomenon. In other words, with an initial offset in the capacitor voltages, over time, the voltages tend to go to a certain steady-state value. From Figure 4.11 it can be seen that the time-constants however are quite long. Also, the steady-state voltage is not the desired nominal voltage and a considerable offset is noticed, especially in the capacitor voltage of correction amplifier 2. It should be mentioned that when an inductive load is used (or when the parasitic inductance of the output resistor is taken into account), the offset can be worse and it is even possible to destabilize the converter such that the capacitor voltage in a correction amplifier keeps rising.

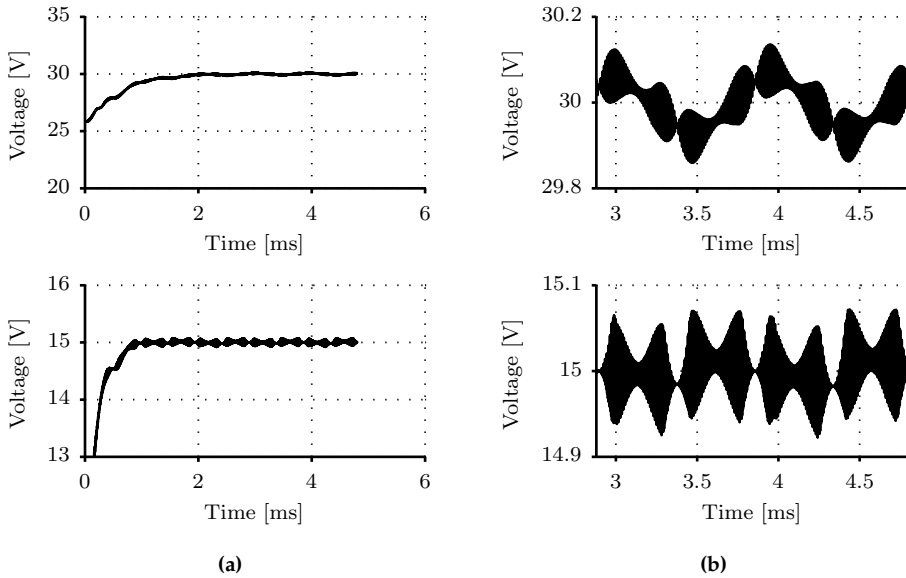


Figure 4.12: Simulation result of capacitor closed-loop balancing: (a) Capacitor (C_{A1} and C_{A2}) voltage with initial offset (b) capacitor (C_{A1} and C_{A2}) voltage in steady-state.

4.6.3 Closed-loop balancing

Based on the previous simulation result it can be concluded that for the PowerDAC closed-loop capacitor voltage balancing is a requirement. It is also advised to include hardware over-voltage protection in a practical implementation.

The result of the modulation scheme proposed in this chapter is shown in Figure 4.12. Notice that balancing of the capacitor voltages occurs much faster and that the desired nominal value is almost reached. Here, the controller is simply a gain, and therefore a small offset is still present. If desired, this small offset can be removed by including an integral action in the controller. Furthermore, due to the resolution of the microcontroller, limit cycles may be present, where the correction shows a repetitive pattern.

The reason for the not-so-fluent transient is the changing reference and limitation of the possible correction. It should be noted that in steady-state the control action for balancing only occasionally amounts to 1 or 2 microcontroller counts, which means that the deviation of the pulse placement from nominal is minimal.

To conclude, the filtered output voltage of the PowerDAC is shown in Figure

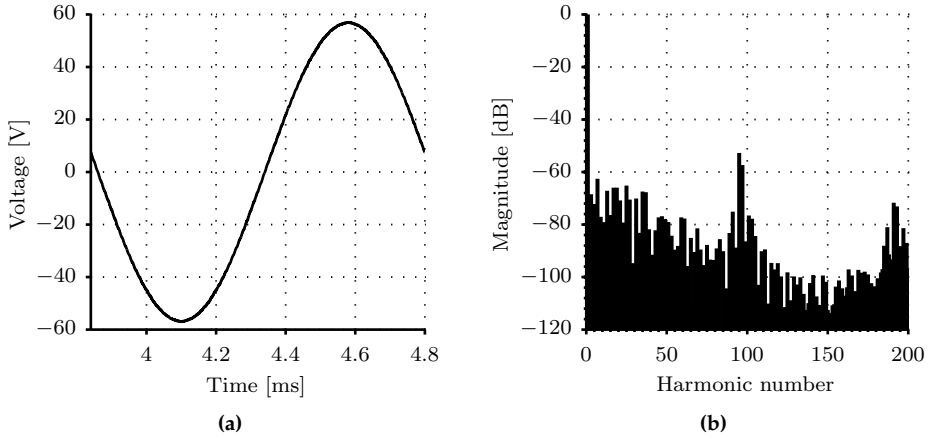


Figure 4.13: Simulation result of capacitor closed-loop balancing: (a) Filtered output voltage and (b) harmonic spectrum of filtered output voltage.

4.13(a) and the harmonic spectrum of this waveform is shown in Figure 4.13(b). The spectrum can be compared with Figure 4.10(d), and the additional harmonics which are visible now are thus mostly caused by sampling and quantization distortion.

4.6.4 Unipolar and bipolar switching

Since the PowerDAC that has been simulated has a full-bridge configuration, two types of switching patterns can be distinguished. Similar to two-level switching, unipolar and bipolar switching can be applied. For multilevel, it means that for unipolar switching a phase-shift of 180° compared to the effective switching frequency needs to be added. The results are shown in Figure 4.14, and it can be seen that with unipolar switching a 9-level output voltage can be created. A disadvantage of the unipolar switching approach is the resulting common-mode voltage. It should be mentioned that closed-loop balancing introduces a common-mode voltage as well, also with bipolar switching. That is because closed-loop balancing changes the pulse pattern and this results in slightly different pulses between the two phases.

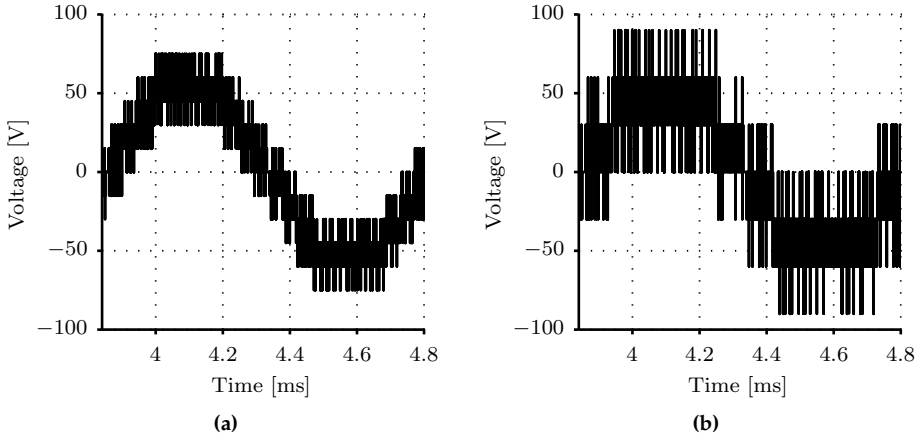
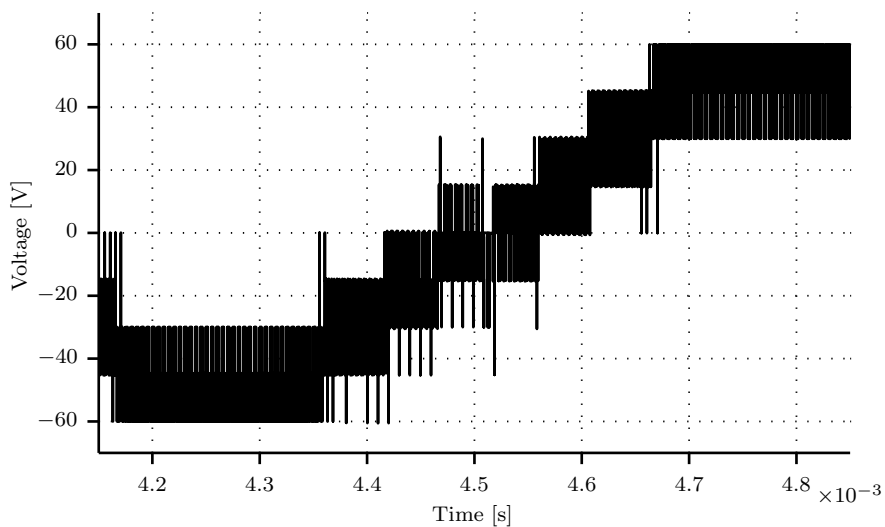


Figure 4.14: Output voltage when using (a) unipolar switching and (b) bipolar switching.

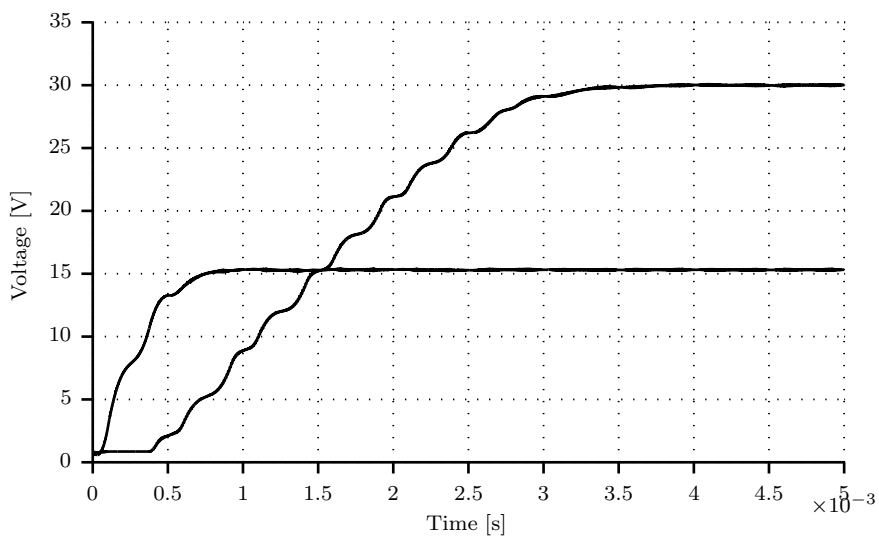
4.6.5 Dead time

Dead time is a well-known distortion effect in power amplifiers. Not surprisingly, similar to conventional two-level approaches, dead time also has effect on the output waveform quality in the PowerDAC topology. For the analysis, it is important that a distinction is made between the main and correction amplifiers. For the main amplifier the distortion mechanism is identical to a conventional switching leg. In other words, during the blanking time, the switch node voltage will clamp, depending on the direction of current, to the positive or negative supply rail. When the main amplifier is a flying-capacitor converter, the dead time will result in a similar error.

For the H-bridge correction amplifiers, however, the mechanism is slightly different. This can be illustrated by means of the following simulation result. In Figure 4.15(a) the output voltage at the switch node is shown when dead time is included. It can be seen that additional spikes occur and depending on whether a positive or negative current is flowing these spikes point upward or downward. The reason is that it does not really matter what reference is applied, for both positive and negative current the path through the diodes leads to charging the capacitor voltage. The capacitor voltage will charge over time and this is shown in Figure 4.15(b) where capacitors are being balanced. It can be seen that in steady-state the capacitor voltage has a small offset. Note that in this figure a different time scale is used, and the wiggling is caused by the fact that a sinu-



(a)



(b)

Figure 4.15: Simulation result showing the effect of dead time: (a) switched output voltage (b) capacitor voltages.

soidal reference is applied. The reason why one capacitor balances first is because priorities have been set as explained in section 4.4.3 of this chapter.

4.7 Summary

This chapter addresses the synthesis of the PowerDAC, a multilevel alternative in the family of series multicell converters. The PowerDAC is constructed as a series connection of a switched main amplifier and a number of switched correction amplifiers. The main amplifier is characterized by an active power supply providing the output power, while correction amplifiers contain only capacitive storage and are used to fine-tune the output voltage.

The configuration is such that each correction cell has half the voltage and twice the switching frequency of the preceding cell. It has been shown that this factor between the voltages of two adjacent cells is the maximum factor providing both uniformity of the voltage levels and sufficient redundancy for balancing the capacitor voltages. A fixed-frequency modulation scheme has been proposed by which any desired output voltage can be created while keeping the capacitor voltages balanced. Symmetry in the modulation scheme results in the property that an unbalance of the capacitor voltages only results in minimal distortion on the output voltage. Furthermore, a closed-loop method has been presented by which the capacitor voltages can be balanced.

The PowerDAC topology can easily be expanded by adding additional cells and the number of levels will grow exponentially. As such, it is possible to generate a high-quality output voltage waveform with only a limited amount of components. The main disadvantage of the topology is that it often requires simultaneous switching to jump between adjacent voltage levels. This disadvantage translates in a higher total switch stress compared to alternative solutions. Also, in practice, the switching devices have a finite switching time, and spikes can be expected. The experimental verification of the results is presented in chapter 7.

Part III

Techne

Chapter 5

Modeling and control of series multicell converters

“There is nothing more practical than a good theory.”

(James. C. Maxwell)

5.1 Introduction

Series multicell converters in which capacitors are used for the creation of voltage levels are subject to two control objectives. First, the tracking of the external variable, the output voltage or current and, second, the regulation of the internal variables, the capacitor voltages. In the previous chapter it was already mentioned that without any additional measures the compensators which are responsible for these objectives may influence each other. To minimize the effects, duty cycles had to be changed and limitations were set. However, the coupling between the two compensators remains an issue that needs to be addressed. Therefore, in this chapter the analysis of closed-loop balancing and its influence on the output is extended and an in-depth analysis is performed.

To be able to do that we need to take a step back, and start with focusing on a basic three-level flying-capacitor topology (full-bridge) as shown in Figure 5.1. The main contribution of this chapter is now to present two solutions for the coupling problem. Moreover, it presents the design and implementation of two different, nonlinear and vector, closed-loop control methods for flying-capacitor power converters. In the first method the coupling between the internal voltage balancing dynamics and the external load dynamics is solved in the pulse-width modu-

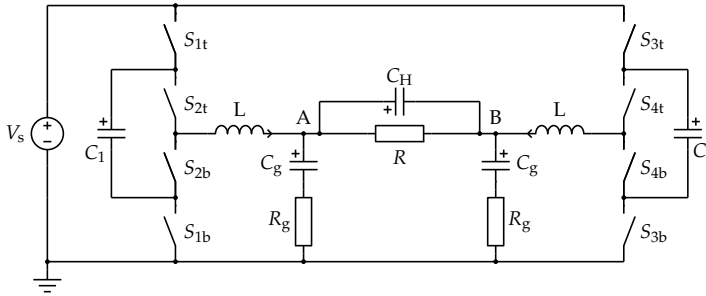


Figure 5.1: Circuit diagram of a full-bridge flying-capacitor converter with two cells per leg.

lator by means of vector modulation. In the second method input-output decoupling is achieved by feedback linearization to resolve the nonlinearity caused by switching the flying-capacitor voltage state.

Closed-loop balancing control in flying-capacitor converters is a requirement. In particular for converters with a high number of voltage levels [143]. Open-loop natural balancing may not be sufficient, as for instance in [34] it has been shown how small perturbations/disturbances in combination with parasitics can lead to steady-state solutions which are undesirable. Also, in some situations it may be necessary to be able to track supply voltage variations, for example during start-up of the converter, and natural balancing time-constants can be too slow. As a result, in a worst case situation it is possible that the voltages seen by the switch devices exceed their maximum.

Closed-loop control methods for flying-capacitor topologies have been proposed in for instance [17, 24, 48, 64, 69]. It has been noticed that, when duty cycle corrections are performed, very often the coupling between the two control tasks is neglected and superposition is used to calculate the duty cycles. In these situations, the adjustments made by the balancing controller will influence the reference controller. The coupling between the two controllers can become a serious issue, especially in applications where high accuracy and bandwidth are required. Decoupling of the two control tasks requires, therefore, special attention.

In [46] input-output decoupling by means of feedback linearization has been presented as a solution for half-bridge flying-capacitor converters, and in previous work [17] various control methods, which include linear control with vector modulation, LQR and finite-set model-predictive control have been implemented on a half-bridge flying-capacitor topology. Here, some of the methods presented earlier are applied to the full-bridge topology and new elements are included. More specifically, there will be a focus on the implementation of tools for nonlinear con-

trol design and the results are compared with vector decoupling. For that reason, this chapter is specifically focusing on the decoupling of the two control objectives, and not the eventual design of the compensator. Additionally, nonlinear tools as applied in [2, 46] are discussed more elaborately.

The two closed-loop control methods which are proposed achieving both control objectives are applied to a full-bridge flying-capacitor amplifier system of which the schematic is shown in Figure 5.1. The proposed methods can be extended in such a way that they can be applied to systems with more voltage levels. It should be noted that resistors R_g have been added on purpose to dampen the resonance in the frequency response of the filter. It is also possible to dampen the resonance actively, however, this is not the focus of this work. Proportional control is proposed for balancing the capacitors as the capacitors behave as a type-1 system, so the integrator in the controller is superfluous. Non-idealities in the control-loop (disturbances) may cause a small steady-state error, however, for most applications this has a negligible impact. For the output voltage control it is shown how an LQR controller can be designed - subject to a feedback linearizing coordinate transformation - containing a cost function that is minimizing the energy in the output filter.

The organization of this chapter is as follows. The modeling of the flying-capacitor topology is discussed in section 5.2. In section 5.3 the input-output decoupling by feedback linearization is explained in detail, and in section 5.4 the second method, decoupling by means of vector PWM, is explained. Section 5.5 shows how an LQR controller can be designed. In section 5.6 simulation results of the proposed control methods are presented.

5.2 Modeling

In this section a model is derived for the topology shown in Figure 5.1. The modeling procedure consists of a number of steps, starting with the derivation of a continuous-time switched-model. This type of model can be put in different forms and also provides the basis for the modeling used in simulation tools such as PLECS [118]. The second step is to remove the nonlinearity which is caused by the PCM-to-PWM conversion and the switching nature of the model, which can be done by using a sampled-data modeling procedure [33] or by considering only the moving average [65, 99]. The latter approach is applied here. It is shown that the resulting model belongs to a particular class of nonlinear systems, a bilinear system. A linear controller can be designed when the bilinear system is linearized. A disadvantage of conventional Jacobian linearization in the symmet-

ric operating point (x_0, u_0) in which the steady-state output voltage is equal to zero is that the dynamics which are responsible for the balancing mechanism in the model are eliminated. Another disadvantage of Jacobian linearization is that the Jacobian model provides an exact representation only in the operating point, and, therefore, the control law based on linear control theory might yield unsatisfactory results in other points. For these reasons the more general approach, feedback linearization as applied in nonlinear control theory [62, 108], is investigated in the following.

5.2.1 Averaging switched model

Consider a smooth input-affine nonlinear MIMO system with m inputs, m outputs and n states of the form

$$\dot{x} = f(x) + \sum_{i=1}^m g_i(x) q_i, \quad (5.1)$$

$$y = h(x), \quad (5.2)$$

in which

$$\begin{aligned} x &= (x_1, \dots, x_n)^T, \\ f(x) &= (f_1(x), \dots, f_n(x))^T, \\ g_i(x) &= (g_{1i}(x), \dots, g_{ni}(x))^T \quad 1 \leq i \leq m, \\ h(x) &= (h^1(x), \dots, h^m(x))^T, \\ y &= (y^1(x), \dots, y^m(x))^T. \end{aligned} \quad (5.3)$$

Smooth means that all entries of $f(x)$, $g_i(x)$ and $h(x)$ are assumed to be C^∞ -functions. In other words, these functions are continuous and the partial derivatives of any order exist. As a consequence, certain nonlinearities that commonly exist in power electronics systems, caused by for instance blanking-time or input saturation, which are often described by discontinuous functions, are not included in the model. Note that inputs are indexed with subscripts, and outputs with superscripts. The input of a switched system is defined as $q(t) = [q_1, \dots, q_m]^T$, of which the elements contain the switching functions defined as

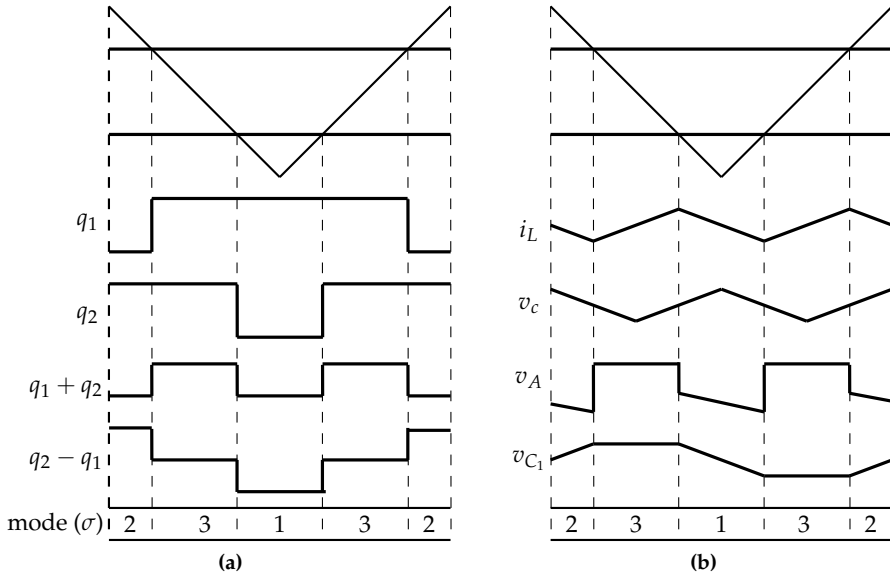


Figure 5.2: (a) Switching sequence of open-loop modulation and (b) approximate waveforms of the state variables.

$$q_i(t) = \begin{cases} 1 & \text{when } S_{it} \text{ is closed at time } t \\ 0 & \text{when } S_{ib} \text{ is closed at time } t \end{cases} \quad (5.4)$$

where subscript t refers to the top switch and b to the bottom switch as illustrated in Figure 5.2. The switching function in (5.4) represents a PWM waveform, which can be applied to one of the switches in the power converter. To be more specific, a switching function q_i is applied to switch S_i . A mode σ of the system is defined as the binary interpretation of the q -vector, and σ is a time-dependent function, defined as the switching law. The switching law defines the mode of the converter at each time instant. In Table 5.1 the different modes are listed for half the system, and in Figure 5.2 the q -functions and mode σ are illustrated.

An averaged model can be derived from the switched model by replacing the switching functions by their moving average [65], according to

$$d_i(t) = \langle q_i \rangle = \frac{1}{T_s} \int_t^{t+T_s} q_i d\tau. \quad (5.5)$$

Table 5.1: Switching modes for half the topology.

mode σ	q_2/q_4	q_1/q_3	v_A	i_{C_1}
0	0	0	0	0
1	0	1	$V_s - v_{C_1}$	$+i_{out}$
2	1	0	v_{C_1}	$-i_{out}$
3	1	1	V_s	0

The differential equations that describe the flying-capacitor circuit shown in Figure 5.1 can be put in bilinear form [2], resulting in a state-space model of the converter topology according to

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \sum_{i=1}^m (\mathbf{B}_i\mathbf{x} + \mathbf{b}_i) \cdot d_i \\ \mathbf{y} &= \mathbf{C}\mathbf{x},\end{aligned}\tag{5.6}$$

in which the state and input vector are defined as

$$\begin{aligned}\mathbf{x} &= [v_{C_{A1}}, i_{L_A}, v_{C_{gA}}, v_{C_{B1}}, i_{L_B}, v_{C_{gB}}, v_{C_H}]^T \\ \mathbf{u} &= [d_1, d_2, d_3, d_4]^T.\end{aligned}$$

The averaged model is not exact for bilinear models due to the multiplication of inputs and states [132], however, it is a sufficiently accurate for the purpose of this chapter. The system matrices can be derived by applying Kirchhoff's laws to the switching circuit, resulting in

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-R_g}{2L} & \frac{-1}{2L} & 0 & \frac{-R_g}{2L} & \frac{-1}{2L} & \frac{-1}{2L} \\ 0 & \frac{1}{2C_g} & \frac{-1}{2C_g R_g} & 0 & \frac{1}{2C_g} & \frac{1}{2C_g R_g} & \frac{1}{2C_g R_g} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-R_g}{2L} & \frac{-1}{2L} & 0 & \frac{-R_g}{2L} & \frac{-1}{2L} & \frac{1}{2L} \\ 0 & \frac{1}{2C_g} & \frac{-1}{2C_g R_g} & 0 & \frac{1}{2C_g} & \frac{-1}{2C_g R_g} & \frac{-1}{2C_g R_g} \\ 0 & \frac{1}{2C_H} & \frac{-1}{2C_H R_g} & 0 & \frac{1}{2C_H} & \frac{-1}{2C_H R_g} & \frac{-(R+2R_g)}{2C_H R_g R} \end{bmatrix}\tag{5.7}$$

$$\mathbf{B}_1 = \mathbf{B}_2 = \begin{bmatrix} 0 & \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{L} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (5.8)$$

$$\mathbf{B}_3 = \mathbf{B}_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (5.9)$$

$$\mathbf{b}_2 = \mathbf{b}_4 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{b}_1 = \begin{bmatrix} 0 \\ \frac{V_s}{L} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{b}_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{V_s}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix}. \quad (5.10)$$

It can be seen that $f(x)$ in (5.1) is equal to $\mathbf{A}x$ in (5.6), in which \mathbf{A} is a constant matrix only depending on system parameters. The input vector functions are given by $g_i(x) = (\mathbf{B}_i x + \mathbf{b}_i)$. As it is desired to regulate the capacitor voltages and to track the output voltage, references need to be defined

$$\mathbf{y}_{\text{ref}} = \begin{bmatrix} v_{CA1}^* \\ v_{CB1}^* \\ v_{DM}^* \\ v_{CM}^* \end{bmatrix}. \quad (5.11)$$

The output functions are defined as

$$e(x) = h(x) - y_{\text{ref}} = \begin{bmatrix} x_1 \\ x_4 \\ x_7 \\ x_3 + x_6 \end{bmatrix} - y_{\text{ref}}. \quad (5.12)$$

Note that h^3 represents the differential mode voltage and h^4 the common-mode voltage. For the latter it should be noted that in practice the voltage at nodes A and B are measured instead of the actual voltages of the capacitor voltages C_g .

5.3 Input-output decoupling by feedback linearization

In this section the first of two methods for decoupling the model presented in the previous section will be explained, and some tools from nonlinear control theory are introduced. In Appendix B a brief summary of the Lie Algebra meaning and notation is given. Also, the definition of relative degree and the decoupling matrix for a nonlinear MIMO system is given as it plays an important role in the following calculations. For the flying-capacitor topology the set of relative degrees is given by

$$r = \left\{ \begin{array}{c} 1 \\ 1 \\ 2 \\ 2 \end{array} \right\}, \quad (5.13)$$

and so it is found that the total relative degree for the system is $r^t = \text{sum}\{r\}^T = 6$.

5.3.1 System transformation

The next step in finding the linearizing control law is the definition of transformed inputs

$$v = [v_1, \dots, v_m]^T. \quad (5.14)$$

The goal is to find a transformation such that the map between each newly defined input v_i and output y^i is linear, and, that each of the m outputs is controlled

by one and only one of the inputs v_i . The latter objective is referred to as the input-output decoupling problem. In other words, with a coordinate transformation our goal is to find a diffeomorphism

$$\begin{bmatrix} \tilde{\xi} \\ \eta \end{bmatrix} = \Phi(x), \quad (5.15)$$

that creates for each of the $1 \leq i \leq m$ transformed inputs v_i a system in Brunovsky normal form, as

$$\begin{aligned} \dot{\tilde{\xi}}_1^i &= \tilde{\xi}_2^i \\ \dot{\tilde{\xi}}_2^i &= \tilde{\xi}_3^i \\ &\vdots \\ \dot{\tilde{\xi}}_{r^i-1}^i &= \tilde{\xi}_{r^i}^i \\ \dot{\tilde{\xi}}_{r^i}^i &= v_i \\ y^i &= \tilde{\xi}_1^i, \end{aligned} \quad (5.16)$$

where r^i is the relative degree of output y^i . In matrix notation (5.16) becomes

$$\begin{aligned} \dot{\tilde{\xi}}^i &= \begin{bmatrix} 0 & 1 & & 0 \\ \vdots & & \ddots & \\ 0 & & & 1 \\ 0 & 0 & \cdots & 0 \end{bmatrix} \tilde{\xi}^i + \begin{bmatrix} 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix} v_i, \\ y^i &= \tilde{\xi}_1^i. \end{aligned} \quad (5.17)$$

In (5.17), $\tilde{\xi}^i$ denotes an r^i -dimensional vector of transformed state variables and v_i denotes the transformed input. The state variables can be combined together in a single vector, according to

$$\tilde{\xi} = \left[\tilde{\xi}_1^1, \dots, \tilde{\xi}_{r^1}^1, \tilde{\xi}_1^2, \dots, \tilde{\xi}_{r^2}^2, \dots, \tilde{\xi}_1^m, \dots, \tilde{\xi}_{r^m}^m \right]^T, \quad (5.18)$$

in which each of the transformed states can be calculated as

$$\tilde{\zeta}_k^i(x) = L_f^{k-1} h^i(x) \text{ for } 1 \leq k \leq r^i, 1 \leq i \leq m. \quad (5.19)$$

Additionally, $n - r^t$ zero-dynamics are introduced in (5.15), as

$$\eta = [p_1, \dots, p_{n-r^t}]^T, \quad (5.20)$$

in which p_j is a function of (η, ξ) . These zero-dynamics describe the internal behavior of the system when the input and initial conditions have been chosen in such a way that the output remains zero. The zero-dynamics are not uniquely defined and can be chosen arbitrarily as long as

$$L_{g_i} \Phi_j(x) = 0 \text{ for } 1 \leq j \leq n - r^t, 1 \leq i \leq m. \quad (5.21)$$

For the system defined in (5.6), the required coordinate transformation in (5.15) is found to be

$$\begin{aligned} \Phi(x) &= \begin{bmatrix} \tilde{\zeta}_1^1 \\ \tilde{\zeta}_1^2 \\ \tilde{\zeta}_1^3 \\ \tilde{\zeta}_2^3 \\ \tilde{\zeta}_1^4 \\ \tilde{\zeta}_2^4 \\ \eta \end{bmatrix} = \begin{bmatrix} h^1(x) \\ h^2(x) \\ h^3(x) \\ L_f h^3(x) \\ h^4(x) \\ L_f h^4(x) \\ x_3 - x_6 - x_7 \end{bmatrix} \\ &= \begin{bmatrix} x_1 - v_{CA1}^* \\ x_4 - v_{CB1}^* \\ x_7 - v_{DM}^* \\ -\frac{Rx_6 - Rx_3 + Rx_7 + 2R_g x_7 - R_g Rx_2 + R_g Rx_5}{2C_H R_g R} \\ x_3 + x_6 - v_{CM}^* \\ \frac{x_2 + x_5}{C_g} \\ x_3 - x_6 - x_7 \end{bmatrix}. \end{aligned} \quad (5.22)$$

As mentioned before the zero-dynamics are not defined uniquely, and, here $\eta = x_3 - x_6 - x_7$ is chosen, as it is related to the circular mesh voltage in the output filter involving the three capacitors.

5.3.2 Input-output decoupling

The relation between the transformed inputs v and actual inputs u of the plant is given by

$$v = \mathbf{G}(x) + \mathbf{F}(x)u. \quad (5.23)$$

Here, $\mathbf{F}(x)$ is the characteristic decoupling matrix of the system

$$\mathbf{F}(x) = \begin{bmatrix} L_{g_1} L_f^{r_1-1} h^1(x) & \cdots & L_{g_m} L_f^{r_1-1} h^1(x) \\ \vdots & \ddots & \vdots \\ L_{g_1} L_f^{r_m-1} h^m(x) & \cdots & L_{g_m} L_f^{r_m-1} h^m(x) \end{bmatrix}, \quad (5.24)$$

as given in the Appendix (see (B.18)), and

$$\mathbf{G}(x) = \begin{bmatrix} L_f^{r_1} h^1(x) \\ L_f^{r_2} h^2(x) \\ L_f^{r_3} h^3(x) \\ L_f^{r_4} h^4(x) \end{bmatrix}. \quad (5.25)$$

For the flying-capacitor topology the decoupling matrix is found to be

$$\mathbf{F}(x) = \begin{bmatrix} \frac{x_2}{C_1} & -\frac{x_2}{C_1} & 0 & 0 \\ 0 & 0 & \frac{x_5}{C_1} & -\frac{x_5}{C_1} \\ \frac{V_s - x_1}{2C_{HL}} & \frac{x_1}{2C_{HL}} & -\frac{V_s - x_4}{2C_{HL}} & -\frac{x_4}{2C_{HL}} \\ \frac{V_s - x_1}{C_g L} & \frac{x_1}{C_g L} & \frac{V_s - x_4}{C_g L} & \frac{x_4}{C_g L} \end{bmatrix}. \quad (5.26)$$

This matrix is characteristic for the system and reveals some of its fundamental properties. For instance, the matrix becomes singular whenever x_2, x_5 or V_s is equal to zero, meaning that the feedback linearization is not valid anymore in these operating points. It should be noted that if the output function $h(x)$ is selected such that if instead of the common-mode and differential mode voltages, the voltages of capacitors C_g are controlled, (5.24) will yield a different result, and the decoupling matrix will become singular for all x .

5.3.3 Linearizing control law

The input-output linearization of a bilinear model as described by (5.6) is now calculated. A linearizing control law can be found according to

$$u = \alpha(x) + \beta(x)v, \quad (5.27)$$

in which

$$\begin{aligned} \alpha(x) &= -F(x)^{-1}G(x) \\ \beta(x) &= -F(x)^{-1}. \end{aligned} \quad (5.28)$$

Here, $F(x)$ is again the decoupling matrix in (5.26) and $G(x)$ is found to be

$$G(x) = \begin{bmatrix} 0 \\ 0 \\ \frac{a_1}{4C_H^2 C_g L R^2 R_g^2} \\ \frac{x_3 + x_6 + R_g x_2 + R_g x_5}{C_g L} \end{bmatrix}, \quad (5.29)$$

where

$$\begin{aligned} a_1 = & 2C_H L R^2 x_6 - 2C_H L R^2 x_3 + 2C_H L R^2 x_7 - C_g L R^2 x_3 + \dots \\ & C_g L R^2 x_7 + C_g L R^2 x_7 + 4C_g L R_g^2 x_7 - 2C_g L R R_g x_3 + \dots \\ & 2C_g L R R_g x_6 + 4C_g L R R_g x_7 - 2C_g L R R_g^2 x_2 - C_g L R^2 R_g x_2 + \dots \\ & 2C_g L R R_g^2 x_5 + C_g L R^2 R_g x_5 - 2C_H C_g R^2 R_g^2 x_7. \end{aligned} \quad (5.30)$$

5.4 Decoupling by vector PWM

In this section a second solution for the input-output decoupling problem is presented. The modulation/decoupling method which is proposed here is quite similar to space-vector modulation/control as applied in three-phase converters. In three-phase systems, the output voltages define an orthogonal three-dimensional

space, which results in a cube that delimits the boundaries of all possible combinations of voltages that could be created. The simplified Clarke transformation is an isometric projection of this cube on the α, β -plane.

Here, a similar approach is used, where input voltage and output current are placed orthogonal in a two-dimensional space. While in three-phase systems the space vectors are mostly assumed to be static, now, the space vectors are dynamic and depend on the system state. Another difference to point out is that so-called zero-vectors (vectors in the origin) do not exist.

Contrary to the full system analysis in the previous section, the vector decoupling problem is solved for each of the switching legs individually. It is most convenient to implement such decoupling as a part of the PWM modulator. Here, a modulator is proposed which achieves the decoupling under the assumption that the state variables do not change significantly within one PWM cycle.

For the vector PWM, first of all, it is required to identify the various switching modes of the converter, as these form the basis for the space vectors. These modes are shown in Table 5.1. The effects of the modes on capacitor balancing and on the output voltage are included. For the two-cell flying-capacitor topology we can find four space vectors, given by

$$\begin{aligned} v_0 &= [-\frac{1}{2}V_s, 0]^T \\ v_1 &= [-v_d, i_{\text{out}}]^T \\ v_2 &= [v_d, -i_{\text{out}}]^T \\ v_3 &= [\frac{1}{2}V_s, 0]^T. \end{aligned} \tag{5.31}$$

Here v_d represents the deviation from $\frac{1}{2}V_s$ in the flying-capacitor voltage, which is a consequence of the fact that the voltage vectors have been centralized around the origin. From (5.31) it can be seen that the vectors are dynamic, as v_d and i_{out} change in time. For the balanced case, that is $v_d = 0$, the vectors can be drawn in a vector diagram as shown in Figure 5.3(a). The x-axis represents the desired output voltage of one switching leg (the voltage at node A or B in Figure 5.1). Similarly, the y-axis represents the desired current to balance the capacitor. As a result, a reference vector is defined as

$$v_{\text{ref}} = [V_{\text{ref}}, I_{\text{ref}}]^T. \tag{5.32}$$


$$I_{\text{ref}} = -\frac{C_1}{T_s} v_d. \quad (5.33)$$
$$T_0 \mathbf{v}_0 + T_1 \mathbf{v}_1 + T_2 \mathbf{v}_2 = T_s \mathbf{v}_{\text{ref}}. \quad (5.34)$$
$$T_0 + T_1 + T_2 = T_s. \quad (5.35)$$

In most cases the capacitor voltage is slightly unbalanced, leading to a skewed

vector diagram, shown in Figure 5.3(b). Now, to determine the sector, the following expression can be used

$$\det \begin{bmatrix} -v_d & V_{\text{ref}} \\ i_{\text{out}} & I_{\text{ref}} \end{bmatrix} < 0. \quad (5.36)$$

If the expression results in 0, the reference vector is in sector 1, otherwise in sector 2. Alternatively, the equations (5.34) and (5.35) for both sectors can be evaluated, after which the result without any negative switching time is selected.

The next step is to calculate the switching times. For instance, for sector 1 it follows from (5.34) and (5.35) that

$$\begin{bmatrix} T_0 \\ T_1 \\ T_2 \end{bmatrix} = \begin{bmatrix} v_0 & v_1 & v_2 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} T_s v_{\text{ref}} \\ T_s \end{bmatrix}. \quad (5.37)$$

If $i_{\text{out}} \neq 0$ and $V_s \neq 0$, the inverse matrix in (5.37) can be determined and the resulting switching times can be derived analytically. Exactly the same calculation can be performed for sector 2. With the knowledge that $D_1 = \frac{T_1}{T_s}$ and $D_2 = \frac{T_2}{T_s}$ in sector 1, and $D_1 = \frac{T_1+T_3}{T_s}$ and $D_2 = \frac{T_2+T_3}{T_s}$ in sector 2 (see Figure 5.2) the duty cycles for both sectors yield

$$\begin{aligned} D_1 &= \frac{2I_{\text{ref}}v_d + V_s I_{\text{ref}} + i_{\text{out}} V_s + 2i_{\text{out}} V_{\text{ref}}}{2i_{\text{out}} V_s} \\ D_2 &= \frac{2I_{\text{ref}}v_d - V_s I_{\text{ref}} + i_{\text{out}} V_s + 2i_{\text{out}} V_{\text{ref}}}{2i_{\text{out}} V_s}. \end{aligned} \quad (5.38)$$

5.5 Control design

In this section two alternative solutions for a compensator are presented, namely, LQR and discrete-time PI control. It has been chosen to present the design of an LQR controller in combination with input-output feedback decoupling. The reason is because it contains an additional step, a coordinate transformation of the **Q**-matrix. The LQR controller is designed only for the output voltage part. As a result, only a subset of transformed states and inputs of the system is required. The system can be split up as such, because the system is decoupled.

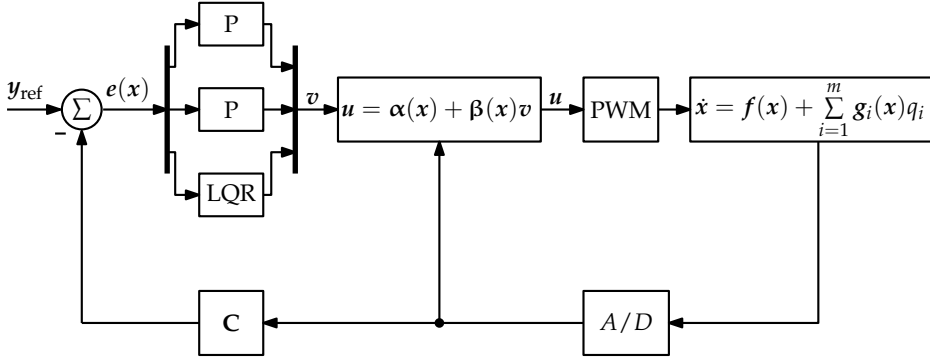


Figure 5.4: Block diagram of controller with input-output decoupling by feedback linearization of flying capacitor voltage and output voltage.

A discrete-time PI controller is presented in combination with vector decoupling. However, it is also possible to exchange the strategies.

5.5.1 Output voltage control by full-state feedback with LQR

A block diagram of the control structure with feedback linearization is shown in Figure 5.4. The control gain matrix can be determined in various ways, for instance by using pole placement [147]. Here, an LQR approach is selected, because it allows calculating an optimal gain when setting priorities to certain states and inputs, achieving a good balance while controlling the output. The LQR control law is given by

$$\hat{v} = -\mathbf{L}\hat{\xi}, \quad (5.39)$$

in which the gain \mathbf{L} is determined by minimizing the cost function

$$J(\hat{\xi}, \hat{v}) = \int_0^\infty (\hat{\xi}^T \mathbf{Q} \hat{\xi} + \hat{v}^T \mathbf{R} \hat{v}) dt, \quad (5.40)$$

with

$$\begin{aligned} \hat{\xi} &= [\tilde{\tau}_1^3, \tilde{\tau}_2^3, \tilde{\tau}_1^4, \tilde{\tau}_2^4, \eta]^T, \\ \hat{v} &= [v_3, v_4]^T. \end{aligned} \quad (5.41)$$

The state vector has been redefined in such a way that it only contains states which are part of the output filter. The next step is to determine the weighting matrices \mathbf{Q} and \mathbf{R} in such a way that the energy in the output filter is minimized. Therefore, the \mathbf{Q} -matrix needs to be transformed as

$$\hat{\xi}^T \mathbf{Q} \hat{\xi} = \frac{1}{2} \hat{x}^T \mathbf{Q}_H \hat{x}, \quad (5.42)$$

where weighting matrix \mathbf{Q}_H is selected in such a way that the right-hand side of (5.42) represents the total energy in the output filter, given by

$$\mathbf{Q}_H = \begin{bmatrix} L & 0 & 0 & 0 & 0 \\ 0 & C_g & 0 & 0 & 0 \\ 0 & 0 & L & 0 & 0 \\ 0 & 0 & 0 & C_g & 0 \\ 0 & 0 & 0 & 0 & C_H \end{bmatrix}. \quad (5.43)$$

Solving (5.42) results in the matrix in (5.44). The \mathbf{R} -matrix penalizes the input and there is no specific guideline in selecting the value, although it represents an energetic term in the cost function (5.40), and a higher value will result in slower transients. Furthermore, since the two inputs have been constructed to regulate the common-mode and differential mode voltage, in the \mathbf{R} -matrix a weighting factor could be selected for both these two terms. In this chapter a value of $3.3750 \cdot 10^{-33}$ is used for both terms.

$$\mathbf{Q} = \begin{bmatrix} \frac{2C_H R^2 + C_g R^2 + 4L}{4R^2} & \frac{C_H L}{R} & 0 & 0 & -\frac{(2L - C_g R_g R)}{4RR_g} \\ \frac{C_H L}{R} & C_H^2 L & 0 & 0 & \frac{C_H L}{2R_g} \\ 0 & \frac{C_g}{4} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{C_g^2 L}{4} & 0 \\ -\frac{(2L - C_g R_g R)}{4RR_g} & \frac{C_H L}{2R_g} & 0 & 0 & \frac{C_g R_g^2 + L}{2R_g^2} \end{bmatrix}. \quad (5.44)$$

When applying the digital LQR solving algorithm from Matlab [88], `dlqr`, the resulting gain matrix is found to be

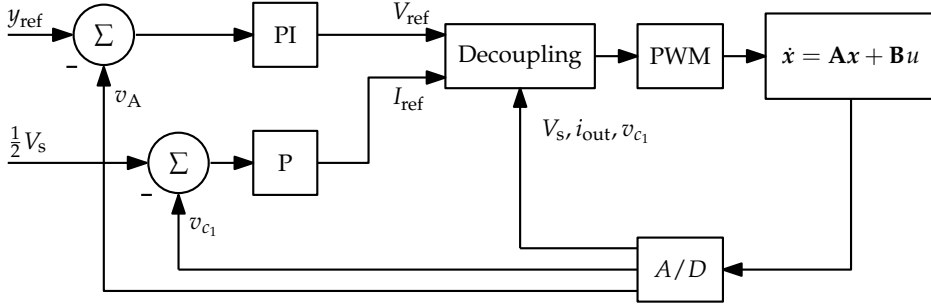


Figure 5.5: Block diagram of controller with decoupling of flying capacitor voltage and output voltage.

$$\mathbf{L} = 10^{10}. \quad (5.45)$$

$$\begin{bmatrix} 1.0825 & 0.0000 & -0.0000 & -0.0000 & -0.0148 \\ -0.0000 & -0.0000 & 1.3052 & 0.0000 & 0.0000 \end{bmatrix}.$$

In Figure 5.4 it can be seen that proportional control is used for the capacitor balancing and that these states have been removed in the design of the output voltage controller.

5.5.2 Linear PI control

As mentioned earlier, the vector decoupling method is presented here combined with a PI controller. With the use of linear control both the capacitor voltage and the output voltage are measured and a PI-controller is used to track the output voltage. The basic structure of such a controller system is shown in Figure 5.5. The compensation may be implemented in the modulator by means of various methods, i.e. by changing the duty cycle or the phase-shift. Alternatively, it is possible to calculate the switching times instead of a duty cycle/phase-shift and implement a space-vector controller. The chosen method is not relevant as long as the balancing control action is decoupled from the output voltage/current control. The compensator for the output voltage is a PI-controller, given by the transfer equation in the z-domain:

$$\text{PI} = K_p + K_i \frac{T_s}{z - 1}. \quad (5.46)$$

In this chapter, $K_p = 0.2$ and $K_i T_s = 0.3$. The gain for the balancing compensator has been selected as $K_{v_{C_1}} = 0.03$.

5.5.3 Prevention of saturation effects

One of the problems that have been encountered during the implementation of the controllers is input saturation. While theoretically the inputs have been decoupled, when one of the inputs is saturated, the decoupling is not valid anymore. In this chapter a solution for the saturation problem in the vector PWM is proposed by setting priorities. That is, the maximum capacitor voltage correction is calculated, in such a way that the capacitor voltage correction will not saturate the output. In other words, V_{ref} is limited between $-\frac{1}{2}V_s$ and $\frac{1}{2}V_s$, and I_{ref} is calculated in such a way that the maximum possible vector is placed exactly on the boundary of one of the sectors. It should be noted that this strategy may result in a change of sector, because it projects the reference vector on the boundary. The maximum value can be calculated by using

$$I_{\text{ref,max}} = \frac{|i_{\text{out}}| \cdot (V_{\text{ref}} \pm \frac{1}{2}V_s)}{(av_d \pm \frac{1}{2}V_s)}, \quad (5.47)$$

in which a $+$ -sign is used when $V_{\text{ref}} < av_d$ and where a represents the sign of the output current.

5.5.4 Output current singularity

Both the feedback linearization as well as the vector pulse width modulator yield a singularity for zero output current. The division by zero cannot be calculated and in practice it also means that certain values in the digital microcontroller can become very high when the output current is very low. As a result, additional code is required to prevent these situations from happening.

It is questionable whether it is required that the control law for balancing the capacitor voltages has linear behavior. Furthermore, a low output current will in any case not be able to quickly unbalance the capacitor. Therefore, the output-current singularity could be solved by a multiplication with $|i_{\text{out}}|$ or i_{out}^2 in the feedback control law.

Table 5.2: Simulation parameters.

Parameter	Description	Value	Unit
V_s	Supply voltage	40	[V]
f_s	Switching/Sample frequency	100	[kHz]
C_1	Flying capacitor capacitance	100	[μ F]
L	Filter inductance	15	[μ H]
C_g	Common-mode filter capacitance	0.47	[μ F]
C_H	Differential mode filter capacitance	1	[μ F]
R_g	Common-mode damping resistance	10	[Ω]
R	Output resistance (Load)	6	[Ω]

5.6 Simulation results

The flying-capacitor topology of Figure 5.1 has been simulated with the parameters shown in Table 5.2. Simulation results are obtained by using Matlab/Simulink [88] including the PLECS blockset [118] and are shown in Figure 5.6. In this simulation every 500 μ s a step of 24 V (± 12 V) is generated, while at the same time the capacitor voltage is being balanced. Such a transient in the reference of both compensators can be seen as a worst-case situation. Especially, because also a change in current sign occurs during the step. The capacitor voltage has an initial offset. In all simulations only feedback control is applied and no feedforward techniques are included, also the control-loop elements are assumed to be ideal. It can be seen that both methods show very similar results given the current conditions (i.e. designed controller gains, modulation index). For the output voltage it takes only 5 switching cycles to reach 90 % of the steady-state end value. The capacitor balancing still has a small effect on the output voltage as can be noted, because the decoupling methods rely on the assumption that the state variables do not change within one switching cycle.

Furthermore, from the simulation results in chapter 4 it has been observed that without any control of the capacitor voltage (open-loop), the time to balance can be excessive. Faster balancing is easily achieved with feedback control. For linear control the time to balance is of course dependent on the gain which is chosen. Here, the gain and also modulation index is chosen such that saturation is prevented. However, if both these values are increased and a step of 56 V is generated with a higher capacitor-balancing gain, saturation effects can clearly be noticed. This is shown in Figure 5.7, where the LQR controller has no pre-

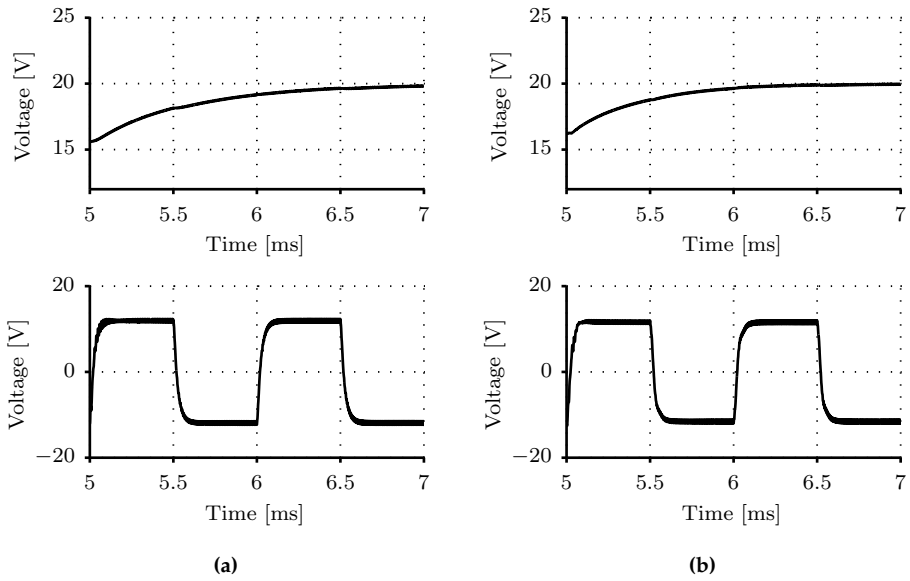


Figure 5.6: Transient response of the flying capacitor voltage v_{C_x} after a step change in the output voltage and initial offset. The top figures show the flying-capacitor voltage and the bottom figures the output voltage. (a) Feedback linearization with LQR (b) Vector decoupling with PI control.

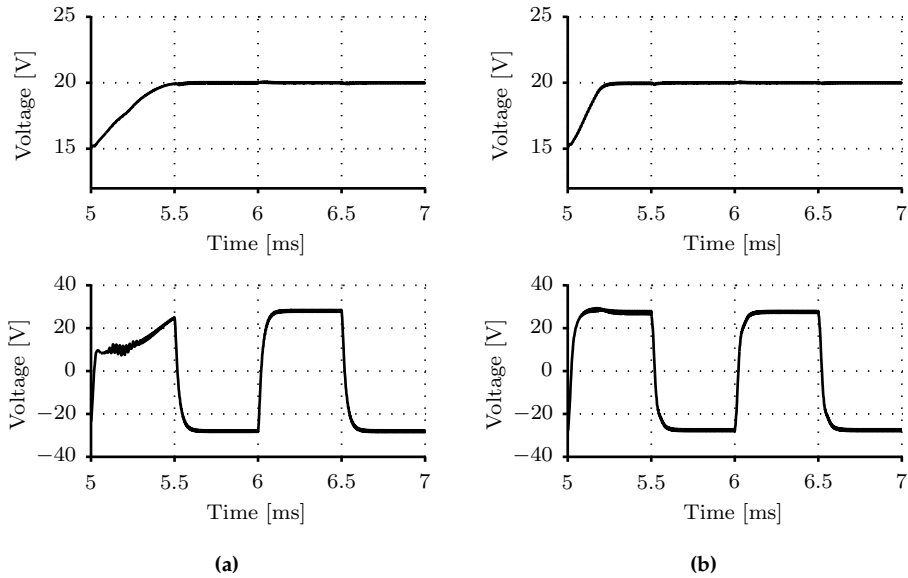


Figure 5.7: The effect of input saturation when both modulation index and control gain are increased. The top figures show the flying-capacitor voltage and the bottom figures the output voltage. (a) Feedback linearization with LQR (b) Vector decoupling with PI control.

vention of saturation, and it can be seen that the transient is heavily distorted. The PI controller, on the other hand, has a limitation on the capacitor balancing compensation, as explained in section 5.5.3.

5.7 Conclusion

This chapter has presented two different control methods for balancing capacitor voltages in flying-capacitor topologies while at the same time controlling the output voltage with feedback control. Specific attention has been given to the decoupling of these two control tasks, the decoupling problem. In the first method the decoupling has been achieved by using feedback linearization. In the second method the decoupling problem has been solved by using a variant of space-vector modulation. For both methods it is possible to design a controller as desired. In this chapter, the vector decoupling method has been demonstrated with PI control and for the nonlinear input-output decoupling an LQR controller

has been designed for tracking the output voltage reference. Simulation results are presented to show how the decoupling methods show quite similar behavior and are both able to decouple the two control actions. The methods are, in principle, extendable to flying-capacitor topologies with more voltage levels. However, when multiple capacitors need to be balanced, prevention of saturation requires setting priorities. It is suggested that the nonlinear approach could be further improved by analyzing the effect of saturated inputs.

Chapter 6

Impact of asymmetries in parallel multicell converters

“I dettagli fanno la perfezione e la perfezione non è un dettaglio.”

(Leonardo da Vinci)

6.1 Introduction

In the previous chapters the focus has been on series multicell converter topologies. However, it was shown in chapter 3 that switching cells can also be connected in parallel, and thus provide an alternative multicell solution. The interleaved buck topology is an example of such a multicell converter. This topology can be created by connecting switching cells in parallel in such a way that the cell inductors are star-connected at the output node. An example is the 5-fold interleaved buck converter shown in Figure 6.1. This type of converter can be controlled by using phase-shifted carrier modulation, also known as interleaved switching. For that reason the topology is generally referred to as interleaved converter. When N represents the number of cells and the N carrier waves are shifted by $\frac{2\pi}{N}$ with respect to each other, then, this type of modulation will result in significant reduction of the current-ripple at the output of the converter.

In the ideal case, the ripple reduction is very advantageous. However, when component variation is taken into consideration, the presumed phase-shift of $\frac{2\pi}{N}$ is no longer optimal, and subharmonic switching-frequency components will appear in the output current, resulting in a higher current and voltage ripple than

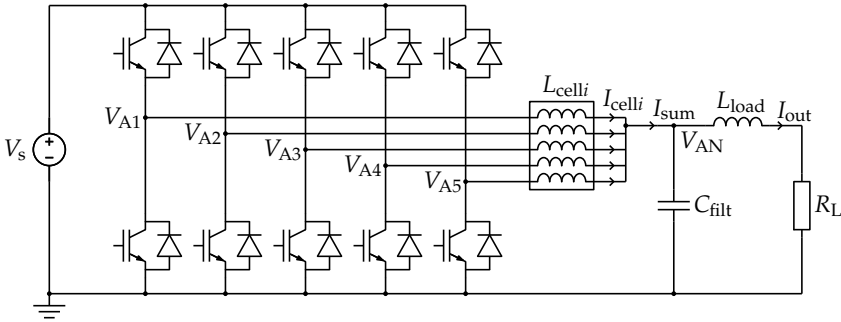


Figure 6.1: 5-fold interleaved buck converter with inductive load.

designed for. The main contribution of this chapter is to present a solution, eliminating this subharmonic, for the case that non-ideal components are used. As in [14, 18], a generalized harmonic elimination method is proposed to suppress subharmonic components, caused by non-idealities, in the output current. The algorithm in [18] comprises a set of equations, which lead to a phase-shift correction in the interleaved converter in such a way that particular harmonics are eliminated. The transcendental equations, which need to be solved, are similar to those in selective harmonic elimination pulse-width modulation (SHEPWM). Although the equations are very cumbersome to solve for the general case, an analytic solution of the transcendental equations is derived for the situation in which three interleaved cells are used. This solution eliminates one subharmonic component, that is, the fundamental switching-frequency component. When more than three cells are interleaved, the optimal phase-shifts are not calculated analytically and numerical methods have to be used. A disadvantage of the method, though, is that inductance values of the cell inductors are required.

Investigations to the effect of tolerances in interleaved converters have already been reported in [45, 56, 136, 146]. For instance, in [45], a method has been proposed where not the phase-shift is adapted, but the sequence of the PWM signals is interchanged. This method is quite useful, in particular for a high number of interleaved cells and also leads to less harmonic distortion in the output current. Another investigation [146] focuses on the effect of delay mismatch between switch device drivers. This kind of delay causes distortion on the output current similar to component variation and, therefore, it can be solved in a similar manner, i.e. by a phase-shift correction. The method proposed in [146] requires, however, the switch-node voltages to be measured. The resulting delay is then determined based on these measurements. More recent studies [56, 136] extend the method to applications with different input or output voltages and duty cycles.

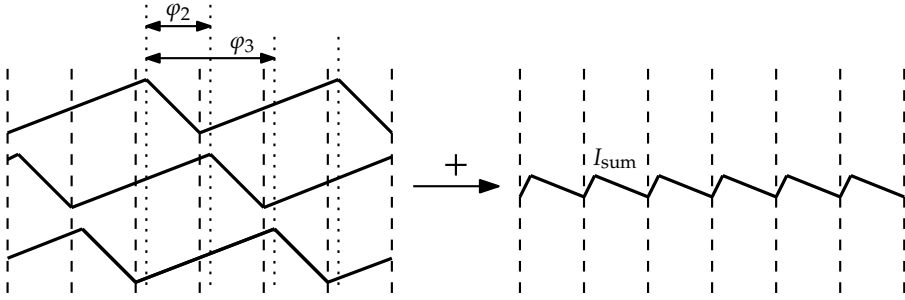


Figure 6.2: Visualization of ripple cancellation: Summation of cell currents results in a sum current with reduced amplitude and increased effective frequency.

In this chapter, besides the theoretical background of the phase-shift correction, in section 6.2.1 the impact of tolerances for different numbers of cells is demonstrated first. Then, an alternative method for implementation, a numerical iterative approach [15] based on Newton's method is presented. This method can be used without having to know the cell inductance values in advance. Neither the cell currents nor switched node voltages have to be measured. Thereby, the method is superior and more useful in practical situations compared to the methods presented earlier in literature. At the end of this chapter simulation results including the weighted harmonic distortion (WHD) are shown for different tolerances of inductances.

6.2 Interleaving

The basic idea of interleaving is depicted in Figure 6.2. By applying a phase-shift φ to the carrier waves also the cell current ripples will have a phase-shift. The total current ripple can be obtained by summing the individual cell current ripples as

$$I_{\text{sum}} = \sum_{i=1}^N I_{\text{celli}}. \quad (6.1)$$

In steady-state operation the capacitor voltage V_{AN} is approximately constant and equal to $d \cdot V_s$, where d is the duty cycle. This is similar to single-cell buck converters. As the voltages at the switch nodes have a square waveform, the cell currents have approximately a triangular-shaped current ripple. These cell-current ripples are phase-shifted with respect to each other, because a phase-shift is applied to

Table 6.1: Simulation parameters.

Parameter	Description	Value	Unit
f_{sw}	Switching frequency	10	[kHz]
d	Duty cycle	0.5	[-]
V_s	DC bus voltage	100	[V]
$L_{cell,nom}$	Nominal cell inductance	7.5	[mH]
C_{filt}	Output filter capacitance	41	[μ F]
R_{load}	Output load resistance	10	[Ω]

the carrier waves of the pulse-width modulator. Consequently, the fundamental harmonic components from the cell currents cancel each other at the output node V_{AN} , leaving only carrier-harmonic multiples of Nf_{sw} . This cancellation results in a sum current which has a reduced current ripple at a higher frequency. The maximum peak-to-peak current ripple will reduce by a factor N and the current ripple frequency will be N times higher than the switching frequency. This phenomenon in interleaved converters is referred to as ripple cancellation.

6.2.1 Effect on higher number of cells

In the previous described principle of ripple-cancellation ideal/equal inductors were assumed. In this section it is shown that the expected consecutive phase-shift of $\varphi = \frac{2\pi}{N}$ is not optimal anymore for unequal filter inductors and the impact for a varying number of cells is demonstrated. Subsequently, a correction for the phase-shifts is suggested. It was already shown in [45] how, when taking component variations into account, an increase in the number of cells at a certain moment does not lead to any further decrease of the output voltage-ripple. This was done by deriving an analytic expression of the voltage ripple for both situations: a converter having equal inductances and a converter with unequal inductances. Then, given a specified voltage ripple, the required capacitor to obtain this ripple was calculated.

This same estimation is used here with the modification that a numerical simulation is performed, instead of an analytic calculation. And, not the required capacitor is calculated, but given a capacitor, the voltage ripple is determined. In the simulation an ideal converter of which the schematic is shown in Figure 6.1 with a varying number of switching legs is simulated. However, a resistive instead of inductive load is used. Relevant simulation parameters are shown in

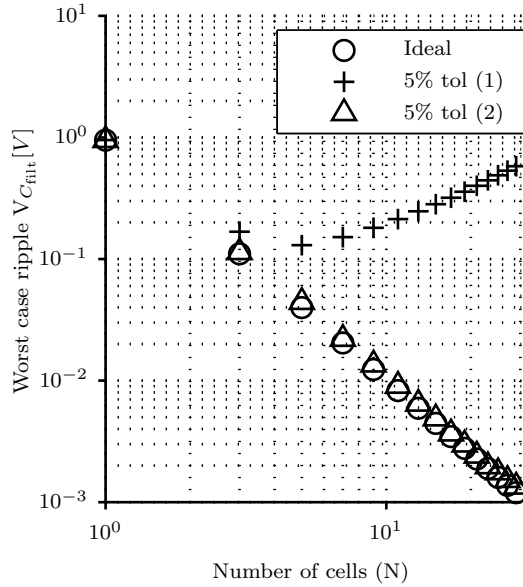


Figure 6.3: Simulation result showing a comparison between i) an ideal interleaved converter ii) an interleaved converter with unequal inductances with conventional phase-shift iii) an interleaved converter with unequal inductances with improved phase-shift.

Table. 6.1. The cell inductor tolerance amounts to 5 %, and inductances are linearly distributed between +5 % and -5 % of the nominal inductance.

The results of the simulations are shown in Figure 6.3. A duty cycle of 0.5 (the worst case situation for cell ripple currents for odd N) was chosen. Only odd values for N have been simulated, as for even values of N , the ripple would completely cancel out. From the figure it can clearly be seen how much influence a small tolerance (indicated as 5% tol (1)) has on the output voltage ripple compared to the ideal situation, especially for a large number of parallel cells. The simulation results are even worse than the analytic calculations of [45], because here, at a certain moment the ripple amplitude increases when extra cells are added. This can be explained, by considering that the result strongly depends on the LC filter dynamics. By adding extra cells the equivalent inductance is decreasing and the cutoff or resonance frequency f_r is increasing as

$$f_r = \frac{1}{2\pi\sqrt{\frac{L_{\text{cell}}}{N}C_{\text{filt}}}}. \quad (6.2)$$

Consequently, due to the low damping of the filter, some switching frequency harmonics which are attenuated for low N can become more and more dominant in the output ripple. With the optimized phase-shift, indicated as 5 % tol (2) and of which the calculation is shown in the following, almost the same result can be achieved as in the fully symmetric case. It must be noted that in the simulation ideal components are used, and the algorithm works best for a duty cycle of 0.5. For other duty cycles, evaluation of the performance can only be done for a single value of N .

6.3 Theory

In this section the theoretical basis for the phase-shift correction is derived. In the following analysis it is assumed that the current ripple can be approximated by a triangular wave shape. In other words, the switched voltages at the nodes of each phase leg are assumed to be constant over one switching period and the output voltage ripple is neglected.

6.3.1 Fourier series of a triangular wave

To be able to give an analytic description of the harmonics in the output current ripple, first of all, the ripple has to be rewritten in terms of its harmonics. This can be done by performing a Fourier series expansion (see Appendix B) of a triangular wave with a duty cycle $d \in [0, 1]$ and zero crossings at normalized time $t = 0$, $t = 0.5$ and $t = 1$, leading to

$$f(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} (a_n \cos(2\pi nt) + b_n \sin(2\pi nt)), \quad (6.3)$$

where

$$\begin{aligned} a_0 &= 0 \\ a_n &= 0 \\ b_n &= -\frac{2(-1)^n}{n^2 d(1-d)\pi^2} \sin[n(1-d)\pi]. \end{aligned} \quad (6.4)$$

In Figure 6.4 up to $n = 20$ harmonics and its sum are shown. The amplitude of the cell current ripple depends on certain electrical parameters and can be estimated

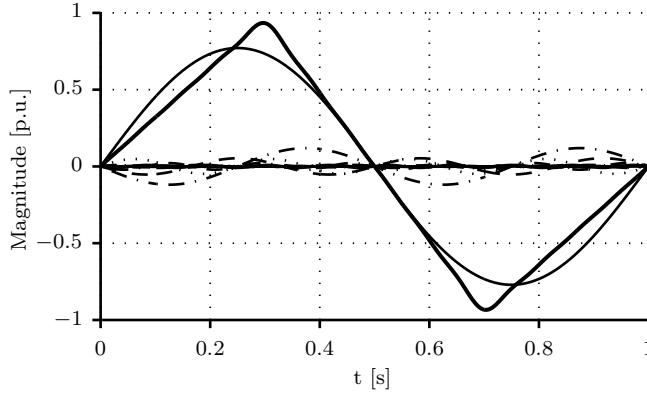


Figure 6.4: Triangular wave and harmonics up to $n = 20$ for $d = 0.6$.

from

$$I_{\text{cell}} = \frac{d(1-d)V_s}{f_{\text{sw}}L}, \quad (6.5)$$

where V_s and L are defined as in Figure 6.1. It follows that the amplitude (denoted by $A_{i,n}$) of the fundamental component ($n = 1$) of the cell current ripple can be calculated from (6.4) and (6.5) with

$$A_{i,1} = \frac{V_s}{f_{\text{sw}}L} \frac{2}{\pi^2} \sin[d\pi]. \quad (6.6)$$

The ripple amplitude is now only dependent on the inductance, because the duty cycle is equal in each of the cells. Unequal duty cycles would imply unequal current sharing and cause circulating currents between cells. Also the other electrical parameters are, for this setup, equal for each of the cells.

6.3.2 Improved phase-shift - Analytic description

The Fourier series of a triangular wave, as shown in Figure 6.4, can be used to calculate improved phase-shifts for an interleaved converter with N cells. The proposed method attempts to eliminate the first $M = \lfloor \frac{N-1}{2} \rfloor$ harmonics from the output current ripple. This is desirable, because lower harmonic components generally have a very large share in the output current's harmonic distortion.

A harmonic component of the sum current ripple can be calculated by summing that particular harmonic of each of the cell currents as

$$I_{\text{sum},n} = \sum_{i=1}^N A_{i,n} \sin(n\omega t + n\varphi_i). \quad (6.7)$$

The values of A_i can be calculated by using the inductance of the cell inductors as described by (6.6) and $\omega = 2\pi f_{\text{sw}}$. The optimal phase-shift values need now to be calculated in such a way that $\sum_{n=1}^M I_{\text{sum},n} = 0$. According to the harmonic addition theorem a sum of sinusoidal functions can always be rewritten to a single sinusoid as

$$\begin{aligned} I_{\text{sum},n} &= A_{c,n} \sin(n\omega t) + A_{s,n} \cos(n\omega t) \\ &= A_{t,n} \sin(n\omega t + \varphi_{t,n}), \end{aligned} \quad (6.8)$$

where A_c denotes the sum of the cosine terms and A_s the sum of the sine terms, as

$$\begin{aligned} A_{c,n} &= \sum_{i=1}^N A_{i,n} \cos(n\varphi_i), \\ A_{s,n} &= \sum_{i=1}^N A_{i,n} \sin(n\varphi_i). \end{aligned} \quad (6.9)$$

The total magnitude and phase-shift can then be calculated with

$$A_{t,n} = \sqrt{A_{c,n}^2 + A_{s,n}^2} \quad (6.10)$$

$$\varphi_{t,n} = \text{atan2}(A_{s,n}, A_{c,n}). \quad (6.11)$$

Here atan2 is defined as the four-quadrant arc tangent. Equation (6.10) needs now to be solved in such a way $A_{t,n} = 0$. This leads to

$$A_{t,n} = \sum_{i,j}^N A_{i,n} A_{j,n} \cos(n(\varphi_i - \varphi_j)) = 0. \quad (6.12)$$

By considering only the fundamental component ($n = 1$) the equation can be solved for $N = 3$ by moving one of the summation terms from (6.7) to the left-hand side. Doing so leads to a slightly different formulation, namely

$$A_N^2 = \sum_{i,j}^{N-1} A_i A_j \cos(\varphi_i - \varphi_j), \quad (6.13)$$

where the subscripts $n = 1$ have been dropped for simplicity. By setting φ_1 to zero the other two angles follow as

$$\begin{aligned} \varphi_2 &= \pi - \arccos\left(\left(A_1^2 + A_2^2 - A_3^2\right) / (2A_1 A_2)\right) \\ \varphi_3 &= \pi + \arccos\left(\left(A_3^2 + A_1^2 - A_2^2\right) / (2A_1 A_3)\right). \end{aligned} \quad (6.14)$$

These equations can be recognized as the law of cosines. It should also be noted that (6.13) is a generalized version of the law of cosines for a convex polygon. Although this analytic approach is applicable for a triangular shaped output current wave ripple, in fact, the mathematical solution is applicable for any shape, as long as the fundamental component can exactly be calculated.

This section presented an analytic solution for $N = 3$. For $N > 3$ the analytic derivation becomes more complex, because there are multiple solutions for the problem. However, this freedom can be used to minimize higher-order harmonics. Additionally, it might be interesting to remark that an analytically equivalent method was also proposed in [80] for cascaded multilevel topologies to eliminate output voltage harmonics caused by unequal dc voltage sources. To understand this relation, refer to Figure 3.11, which demonstrates the equivalence between the two topologies.

6.3.3 Improved phase-shift - Geometric visualization

The improved phase-shift can also be explained by means of a graphical visualization. This gives a better insight in how the method works. Therefore each harmonic is represented as a complex vector

$$I_{\text{cell},n} = A_{i,n} e^{jn\varphi_i}. \quad (6.15)$$

A visualization of $n = 1$ for $N = 3$ is given in Figure 6.5. The magnitude of the vectors can again be calculated by using (6.6).

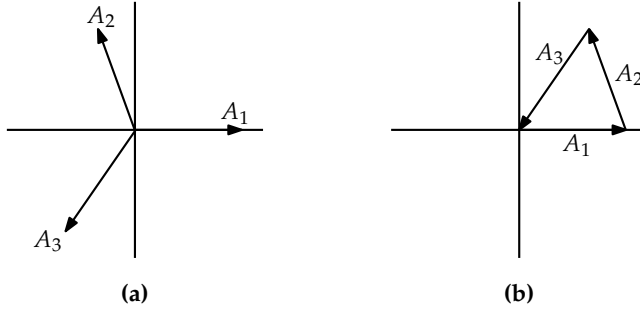


Figure 6.5: Graphical visualization of phase-shift (a) vectors placed with respect to the origin and (b) vectors placed head to tail.

The idea is to combine the vectors in such a way they form a closed chain or polygon, or for $N = 3$, to find a unique triangle. This closed polygon represents the solution for which the sum of that particular cell current harmonic is zero. When the three edge lengths of a triangle are known and the angles unknown, the angles can be solved by using the law of cosines if the three edge lengths comply with the triangle inequality: $\|x + y\| \leq \|x\| + \|y\| \quad \forall x, y \in \{A_1, A_2, A_3\}$.

For other polygons (6.12) is used to derive that the sum of all inner products between all combinations of the complex vectors has to be zero

$$\sum_{i,j}^N \langle I_{\text{cell}i,n}, I_{\text{cell}j,n} \rangle = 0, \quad (6.16)$$

in which the Cauchy-Schwarz inequality has to be maintained such that

$$\langle I_{\text{cell}i,n}, I_{\text{cell}j,n} \rangle \leq A_{i,n} A_{j,n}. \quad (6.17)$$

This inequality ensures that all the cosine-terms are in the domain of $[-1, 1]$.

6.3.4 Iterative phase-shift calibration

In the previous section it was shown that when the cell inductor inductances, $L_{\text{cell}i}$, are not exactly equal to each other, also the cell current ripples will have a different magnitude. As a result, the ripple cancellation is not optimal anymore and the fundamental switching frequency subharmonics return in the output current. A phase-shift correction was, therefore, proposed to suppress this

undesirable effect, and to eliminate particular subharmonics. Unfortunately, the method requires that the cell inductance values are known. Hence, a calibration algorithm is proposed in the following to determine the phase-shift adaptively without having to know the inductances in advance.

In (6.12) it is shown that a particular harmonic n in the output current can be eliminated when the phase-shifts are calculated in such a way that both the real part and imaginary part of that harmonic are equal to zero. In other words,

$$\begin{aligned} A_{c,n} &= \sum_{i=1}^N A_{i,n} \cos(n\varphi_i) = 0, \\ A_{s,n} &= \sum_{i=1}^N A_{i,n} \sin(n\varphi_i) = 0. \end{aligned} \quad (6.18)$$

It was shown that these equations can analytically be solved for a single harmonic when $N = 3$. However, when N is higher and yet more harmonics can be eliminated, the transcendental equations become too cumbersome to solve analytically. A numerical solver is, therefore, required. Furthermore, a numerical solver is also more convenient to implement in practice. As such, Newton's method [66] is used to find the solution. The set of equations (6.18), of all the harmonics to be eliminated, is written in terms of a single $(N - 1)$ -th order vector function which needs to be equal to zero, as

$$F(\Phi) = 0, \quad (6.19)$$

where $\Phi = [\phi_1, \phi_2, \dots, \phi_N]$, a vector containing all the N phase-shifts. From this equation a number of constraints can be derived. First, at least 1 phase-shift needs to be preselected, otherwise an infinite amount of solutions would exist. This can be achieved by setting $\phi_1 = 0$. As a result, there are $N - 1$ phase-shifts to determine and so $N - 1$ equations need to be solved. Since, according to (6.18), per eliminated harmonic two equations are produced, the total harmonics which can be eliminated is equal to $M = \left\lfloor \frac{N-1}{2} \right\rfloor$. As an example, suppose $N = 5$, then 2 harmonics can be eliminated as there are 4 phase-shifts which can be modified. From the resulting equation $F(\Phi)$ the Newton iteration sequence is then given by

$$\Phi_{k+1} = \Phi_k - F'(\Phi_k)^{-1}F(\Phi_k), \quad (6.20)$$

where $F'(\Phi_k)^{-1}$ is the inverse Jacobian matrix. For each iteration k new phase-shifts are calculated and applying these new phase-shifts will eventually lead to a better approximation of (6.19). As it is known that Newton's iteration sequence is not necessarily stable, especially when Φ_0 is too far away from the solution, it is recommended to limit or saturate the iteration step size.

6.3.5 Modified Newton's method for small deviations

The difficulty of (6.20) lies in the calculation of the inverse Jacobian. A new phase-shift vector Φ_k changes the harmonic content of the cell currents. This affects the inverse Jacobian. As a result, it is required to measure the cell currents, to determine the values of $A_{i,n}$, and to recalculate the Jacobian each iteration. In this chapter, a slightly adapted version of Newton's method is proposed, as evaluation of (6.19) reveals that the values of the function $F(\Phi_k)$ are just the real and imaginary parts of the sum current I_{sum} . Therefore, the sum current, instead of all the cell currents, may be measured and its harmonics can be extracted and used in this optimization algorithm¹. Furthermore, parameter changes (i.e. inductance values), due to for instance temperature variations, are often relatively slow. The values of $A_{i,n}$ can be calculated by using

$$A_{i,n} = -\frac{(-1)^n V_s}{n^2 \pi^2 f_{\text{sw}} L_{\text{celli}}} \sin[nd\pi], \quad (6.21)$$

where for L_{celli} the nominal inductance can be taken.

6.4 Simulation results

Although in the previous sections a result has been established which is applicable for any N -cell interleaved converter, detailed simulation results are only shown for the case $N = 5$, as the present experimental setup allows a maximum

¹Evaluation of the inverse Jacobian reveals that the magnitudes $A_{i,n}$ have effect on the magnitudes of the elements of the inverse Jacobian, but not on the sign. Consequently, this algorithm also iterates to the optimal solution and the only difference is that it iterates slightly slower.

Table 6.2: Simulation parameters.

Parameter	Description	Value	Unit
f_{sw}	Switching frequency	9.8	[kHz]
d	Duty cycle	0.1	[-]
V_s	DC bus voltage	10	[V]
$L_{cell,nom}$	Nominal cell inductance	75	[μ H]
R_{cell}	Cell resistance	80	[m Ω]
C_{filt}	Output filter capacitance	37.6	[μ F]
L_{load}	Inductive output load	291	[μ H]
R_L	Output resistance	45	[m Ω]

Table 6.3: Cell inductor and parasitic resistance values.

Parameter	Value	Unit	Parameter	Value	Unit
L_{cell1}	84.6	[μ H]	R_{cell1}	130	[m Ω]
L_{cell2}	74.6	[μ H]	R_{cell2}	80	[m Ω]
L_{cell3}	74.3	[μ H]	R_{cell3}	80	[m Ω]
L_{cell4}	75.2	[μ H]	R_{cell4}	80	[m Ω]
L_{cell5}	75.3	[μ H]	R_{cell5}	80	[m Ω]

of five parallel cells. Also, in this section, an attempt to qualify the algorithm by determining the weighted total harmonic distortion is shown.

6.4.1 Results for five interleaved cells

As mentioned, simulations have been performed for the case $N = 5$, with corresponding simulation parameters listed in Table 6.2. The parameters which are shown are identical to those of the real experimental setup. In Table 6.3 the cell inductor values and their parasitic resistance are shown. It can be noted that the inductance of cell 1 has been chosen deliberately a bit higher. Additionally, in the simulations, the resolution of the DSP used in the setup (which applies also to the phase-shift) has been taken into account.

The simulated cell current ripples are shown in Figure 6.6. It can be seen that one cell current ripple has a lower magnitude because of the higher inductance. The higher cell resistance also leads to a different DC value, which is in this case largely caused by the additional wire. In practice, the difference in resistance will

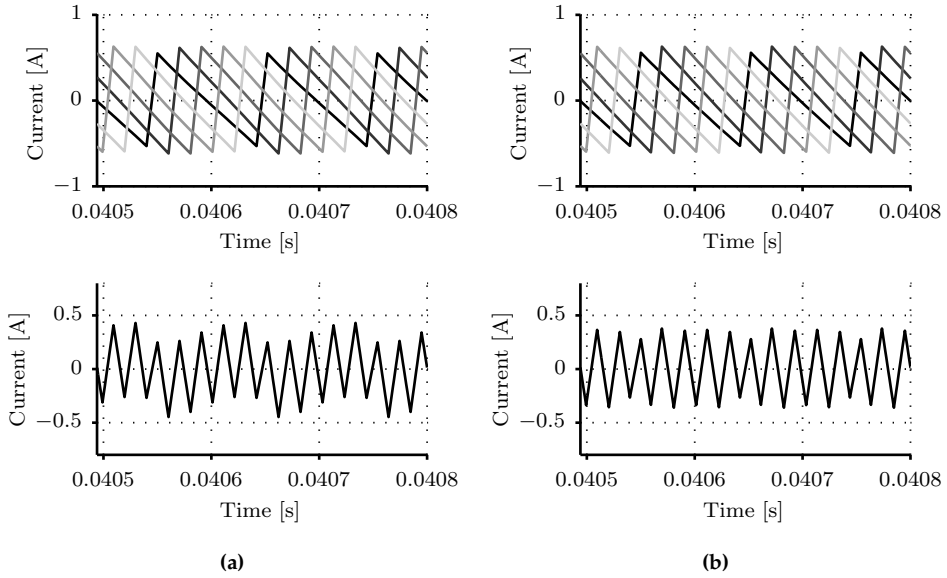


Figure 6.6: Simulation results - Cell currents and sum current (a) without improved phase-shift (b) with improved phase-shift.

generally be lower. For the sake of clarity, this has been corrected for. The sum current is shown in Figure 6.6 as well and it can be seen that the sum current is dominated by the five-times switching frequency multiple. However, it also contains the switching frequency harmonic. Depending on the filter dynamics, or cut off frequency, this fundamental component can be even more visible in the output current.

Next, an iterative simulation has been performed, starting with the nominal phase-shift and 10 iterations. The resulting new phase-shifts are shown in Table 6.4. This phase-shift is given in a similar manner as it would be applied on the digital signal processor in the experimental setup. One PWM cycle on the DSP is 10200 clock-cycles. This means that the nominal phase-shift is 2040, 4080, 6120, 8160 clock cycles, respectively. However, due to implementation restrictions, phase-shifts φ_4 and φ_5 are complemented with respect to the PWM cycle, again resulting in the values 2040 and 4080. Also shown in the last column of the table are the amplitude of the first and second harmonics. These harmonics are calculated by using DFT. As can be seen, there is a rapid decay in the values. The number of iterations to find the improved phase-shift is very modest, after 4 iterations the optimal phase-shift is already found.

Table 6.4: Iteration values (simulation).

Iter. #	ϕ_2	ϕ_3	ϕ_4	ϕ_5	$A_{t,1}$	$A_{t,2}$
1	2040	4080	4080	2040	0.0475	0.0129
2	1951	4091	4059	1947	0.0041	0.0021
3	1946	4076	4055	1948	0.0003	0.0002
4	1946	4075	4057	1948	0.0000	0.0000
10	1946	4075	4057	1948	-	-
Precalculated	1951	4084	4048	1943	0.0025	0.0003

An even better result would be achieved when the applied phase-shift is more accurate, i.e., when more clock cycles per PWM cycle could be used. Ultimately, the phase-shift between the PWM signals should be infinitely accurate to achieve the theoretical minimum value. Therefore, the algorithm performs worse when the number of bits for creating the PWM is less.

Remarkable is the fact that the precalculated phase-shift does not give us the optimal value. The numerical method seems to find a better phase-shift. The explanation is that the precalculation based the first harmonic magnitudes solely on the inductance values. However, also the cell inductor resistance influences this component. It can be concluded that the time-constant of the cell inductor, otherwise stated, also its parasitic resistance, influences the optimal phase-shift.

6.4.2 Harmonic distortion for five interleaved cells

This section will show the weighted harmonic distortion for different tolerances of the filter inductors for both the original and improved case. In Chapter 2 it was shown how for a gradient amplifier the integrated current error is an important criterion for the quality of the produced images, as the current-error time-integral distorts k-space. Due to this integration criterion the harmonics should be weighted by a factor $1/f$. When the filter elements are also included, the filter is two orders higher and a weighting factor of $1/f^3$ is used. This gives a good indication of the consequence of harmonic distortion in most applications as long as the lowest harmonic component is higher than the cutoff frequency of the output filter. The WHD_1 is defined as

$$\text{WHD}_1 = \sqrt{\sum_{n=1}^{30} \left(\frac{I_n}{n} \right)^2}, \quad (6.22)$$

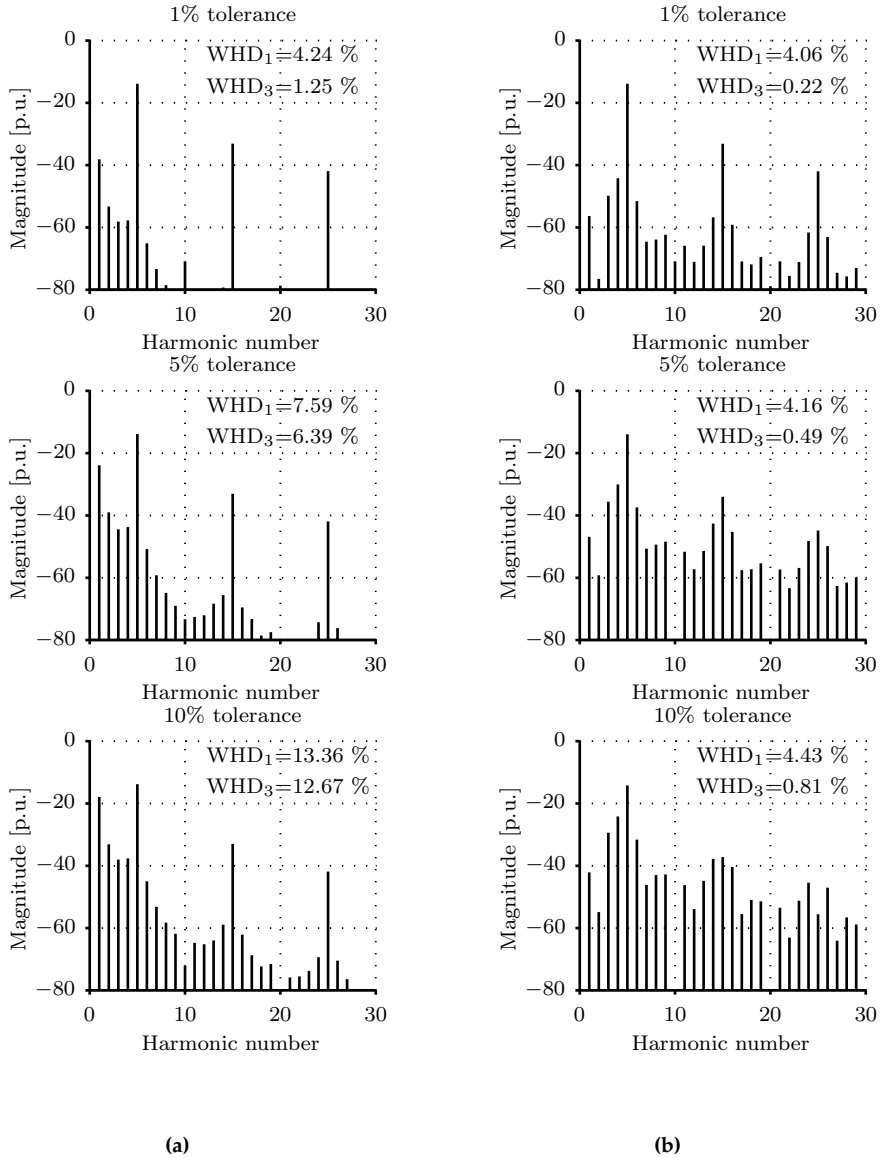


Figure 6.7: Comparison of the harmonic spectrum for different tolerances of the cell inductors: (a) without improved phase-shift (b) with improved phase-shift.

and the WHD_3 as

$$\text{WHD}_3 = \sqrt{\sum_{n=1}^{30} \left(\frac{I_n}{n^3} \right)^2}. \quad (6.23)$$

The WHD_1 and WHD_3 can be calculated for different tolerances (1%, 5% and 10%). It should be mentioned that such tolerances are not unusual for real-life inductors. The results of the analytically determined harmonics for $d = 0.1$ are shown in Figure 6.7. These harmonics are normalized with respect to 1 A cell current ripple for a duty cycle of $d = 0.5$.

It can be seen that the fundamental component is indeed removed and that the magnitude of higher-order harmonics is increased. Despite of this rise in higher-order harmonics the harmonic distortion is still significantly lower, especially the WHD_3 . The improvement is larger when the tolerances of the filter inductors are higher, i.e. when the fundamental component is more dominant.

6.5 Summary

In parallel multicell converters interleaving is a commonly used technique to reduce the output current ripple. Harmonic cancellation is achieved by applying a phase-shift to the carrier waves of the pulse width modulator, resulting in a reduced output current ripple at a higher effective frequency. However, optimal interleaving is only achieved when switching cells are identical. When variations between switching cells are taken into account, subharmonic switching-frequency components appear in the output current, resulting in a higher voltage ripple than designed for.

In this chapter it is shown that for this situation an optimal phase-shift exists. A method is proposed to calculate the phase-shift in such a way that harmonics, such as the switching frequency are removed from the spectrum. Furthermore, an adaptive phase-shift control method is proposed which can solve the optimal phase-shift problem. It is shown that, by this method, the phase-shift values can be determined by only measuring the output current.

Simulation results have been presented in which the result of the adaptive algorithm has been compared to that of using pre-calculated phase-shifts. Also, for various tolerances, the harmonic distortion has been determined. It was shown how low-order harmonics could be eliminated at the cost of more energy in

higher-order harmonics. It can, therefore, be concluded that the proposed phase-shift correction is especially beneficial in applications where lower-order harmonics have a more devastating effect. Experimental results are presented in chapter 7.

Chapter 7

Experimental results

“My favorite programming language is ... solder.”

(Bob Pease)

7.1 Introduction

From theory to practice, it is the purpose of this chapter to give a practical demonstration of a number of elements from this thesis. The chapter can, as such, be divided into three parts. The first part deals with measurement results which are related to the concepts that were developed in chapter 4, the synthesis of the PowerDAC and its associated control/modulation scheme. To be able to do that, a prototype board has been realized of which the power stage has the same configuration as the one that has been used for the simulation results in chapter 4. The most relevant details and design aspects of this prototype board can be found in Appendix C.

The prototype board consists of a full-bridge amplifier, where each phase leg comprises a main amplifier and two correction amplifiers. The main amplifier and first correction amplifier are merged into a flying-capacitor stage for the reasons explained in chapter 4. With such a phase leg a 5-level output voltage can be generated, and, depending on whether bi- or unipolar PWM is applied, across the load, a 5- or 9-level voltage is created. In section 7.2 a measurement result of such a 9-level output voltage is presented together with the resulting output load current. Additionally, PWM waveforms are shown when applying a constant or dynamic reference. It is also shown how the flying capacitors can be balanced, while generating arbitrary waveforms.

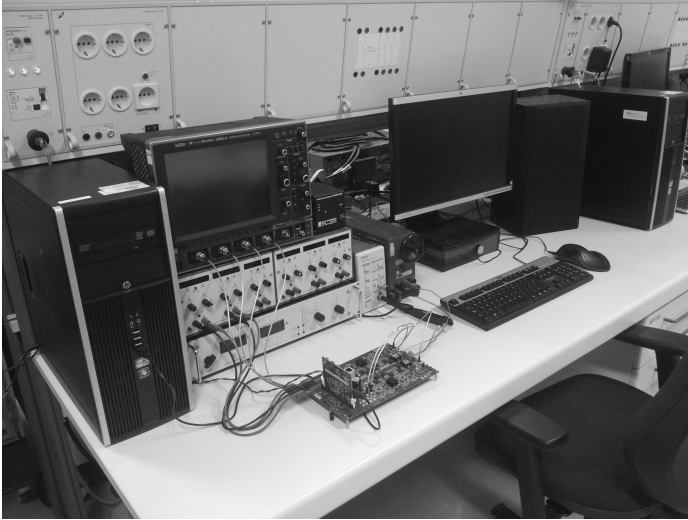


Figure 7.1: Photograph of experimental setup A.

The second part, that is section 7.3, presents the measurement results which are related to the proposed closed-loop control and decoupling methods developed in chapter 5. For these measurements, the same experimental setup is used, since, by enabling the two top or bottom switches in the second correction amplifier, the cell can be bypassed and a full-bridge amplifier configuration results where each phase leg contains only a flying-capacitor stage. Both decoupling methods are tested subject to the most challenging condition: a simultaneous step change in the reference for both controllers while the output current changes its sign.

Lastly, the third part of this chapter addresses the proposed improved phase-shift for parallel multicell converters, as explained in chapter 6. The algorithm has been implemented on a different setup and the relevant details are explained in section 7.4. A practical implementation of the adaptive harmonic elimination method is demonstrated, and the minimization of the harmonic components is confirmed by means of the harmonic spectrum.

7.2 Experimental results of PowerDAC

The experiments for verifying the capabilities of the PowerDAC have been conducted with setup A, of which a photograph is shown in Figure 7.1. In this setup,

besides the PowerDAC prototype board, a Delta EST 150 power supply is used for powering the board. A larger supply (Delta Elektronika SM 120-13) is used as input for the power stage. The measurements are recorded with a LeCroy WaveSurfer 24MXs-A 200MHz oscilloscope, and current is measured with a Tektronix TCPA300 amplifier and current probe. The output voltage and flying capacitor voltages have been measured with a Tektronix P5200 differential probe. All measurement plots have been generated with MATLAB, and raw data is visualized. No post-processing algorithms have applied to the presented images.

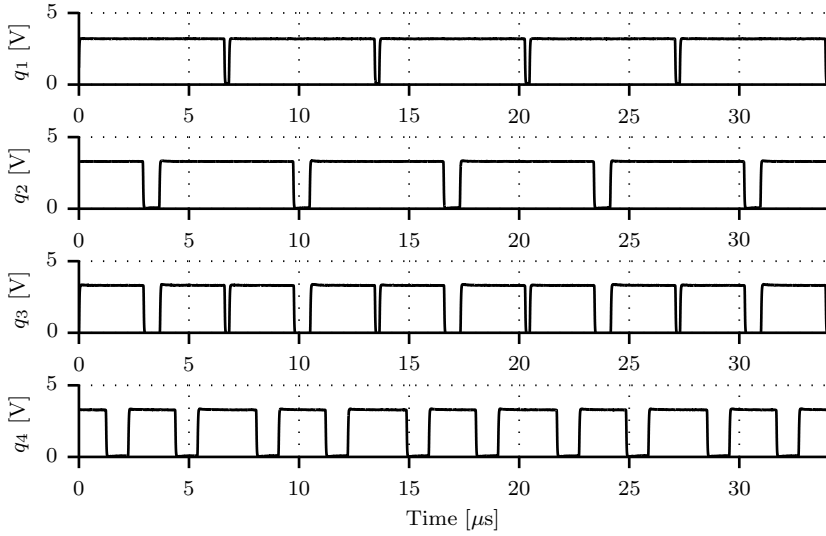
7.2.1 Gate signaling

First, PWM waveforms are shown when a constant duty cycle is applied and a certain correction for both capacitors in one phase leg is desired for balancing. The measured PWM is shown in Figure 7.2(a). The figure displays five switching cycles of the main amplifier. The switching frequency is 146 kHz, and it can be seen that the PWM of the correction amplifier has twice this switching frequency (292 kHz). Notice that, due to a desired correction, the pulses have been adapted. The adaption can be implemented in two ways: by alternating the duty cycle or the phase-shift. Here, on the DSP the duty cycles are alternated, as this method is easier to implement compared to the alternative method. Note that there are quite some moments in which devices need to switch simultaneously.

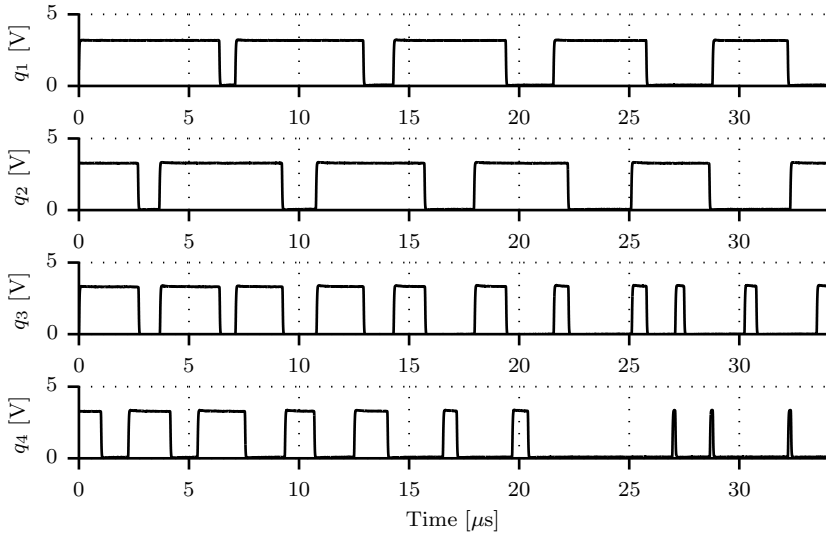
When the reference is dynamic, the PWM waveforms become a bit more complex. In Figure 7.2(b) an example is given of the PWM waveforms when a sinusoidal waveform is created. Also here a correction for balancing is applied.

7.2.2 Output voltage and output current

To show the operation under uni-polar switching, a phase-shift of one-eighth of the switching period is applied in phase leg B. In this mode a 9-level switched output voltage is created. The result is shown in Figure 7.3(a), where the reference is a 1.5 kHz sine wave. The effective switching frequency of this waveform is 8 times the switching frequency of the main amplifier, i.e. 1.168 MHz. As predicted by the simulations, spikes are clearly visible on top of the 9-level waveform. The most important reason for why they are so clearly visible is dead time. The rise time of the switching devices is 12 ns, whereas the blanking time is 100 ns. Notice also that there is some sort of asymmetry in the spikes. This is caused by the current lagging due to the parasitic inductance of the resistor. The output current is shown in Figure 7.3(b).



(a)



(b)

Figure 7.2: Measured gate signals (PWM) (a) the reference is a constant (b) the reference is a sine wave.

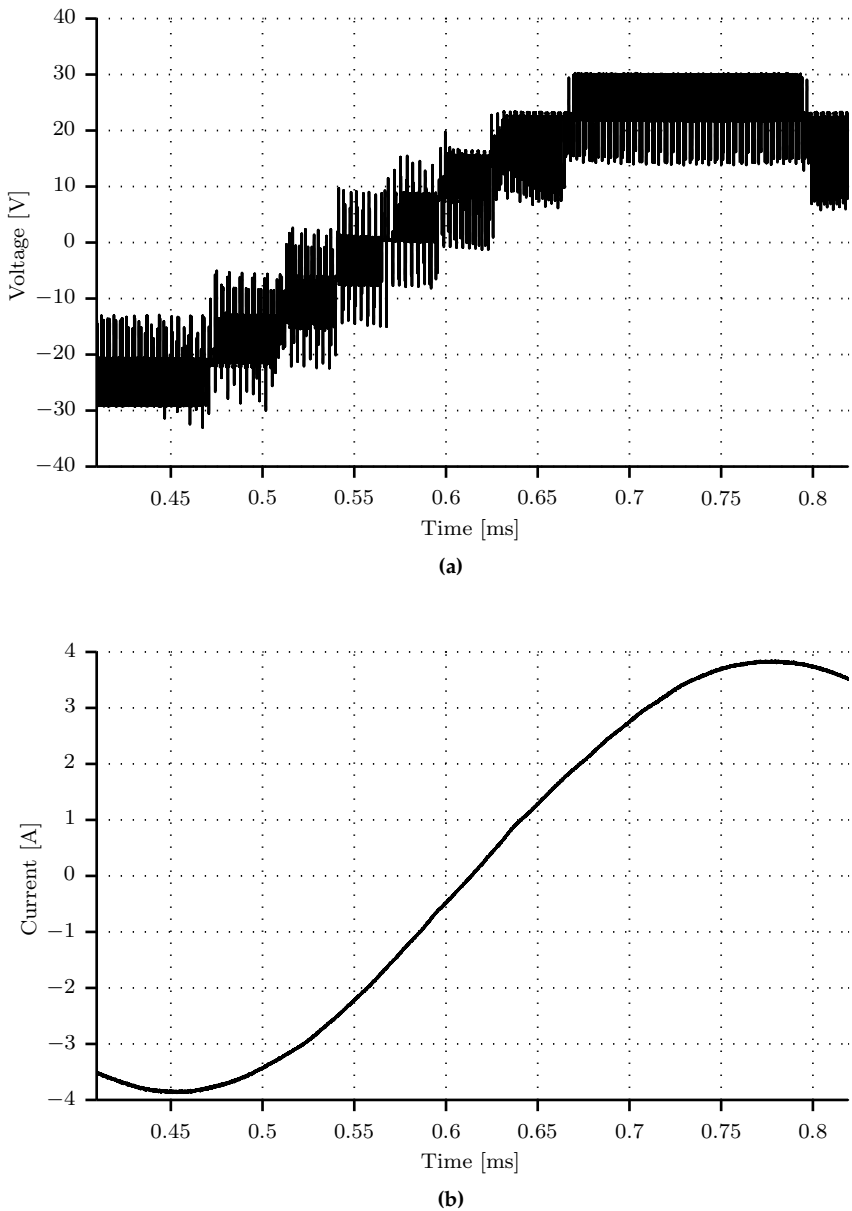


Figure 7.3: Measurement results of (a) switched output voltage and (b) output current.

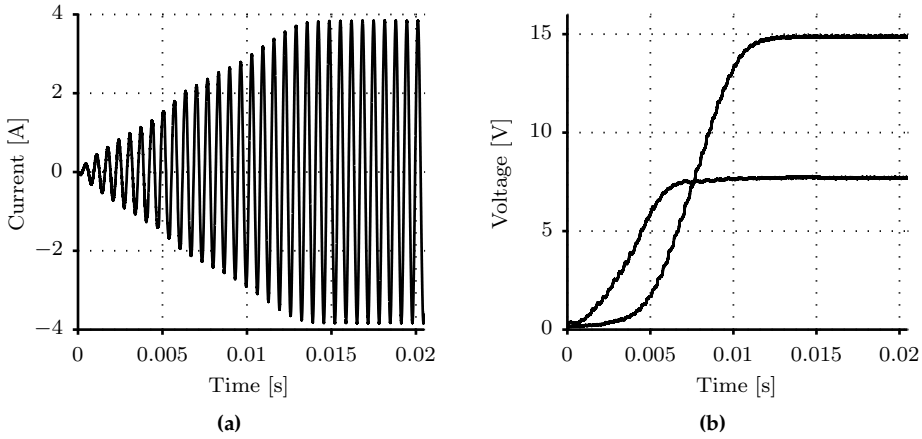


Figure 7.4: Measurement results of (a) output current and (b) capacitor voltages during start-up of the PowerDAC.

7.2.3 Capacitor balancing

Balancing of the capacitor voltages is demonstrated by showing the start-up procedure of the PowerDAC, where the supply voltage ramps up, while at the time already a 1.5 kHz sine wave is created. In Figure 7.4(a) the output current is shown. Since there is no feedforward of the supply voltage, the amplitude of this current is following the supply voltage. In Figure 7.4(b) it can be seen how the capacitors are balanced, and remain balanced. Note that the capacitor voltage of the second correction amplifier is slightly higher than expected. This is, again, caused by dead time, as explained in chapter 4.

7.3 Closed-loop control for flying-capacitor converters

Both decoupling control methods proposed in chapter 5 have been implemented. Again, the setup shown in Figure 7.1 has been used. The control procedure is as follows: On the DSP, at the start of each switching cycle the reference signal is updated and a start-of-conversion signal is sent to the internal 12-bit ADC's of the DSP. All state variables are measured and an interrupt is generated when the conversion is finished. Then, calculations are performed as presented in this thesis to calculate the duty cycles. This sequence is continuously repeated. For

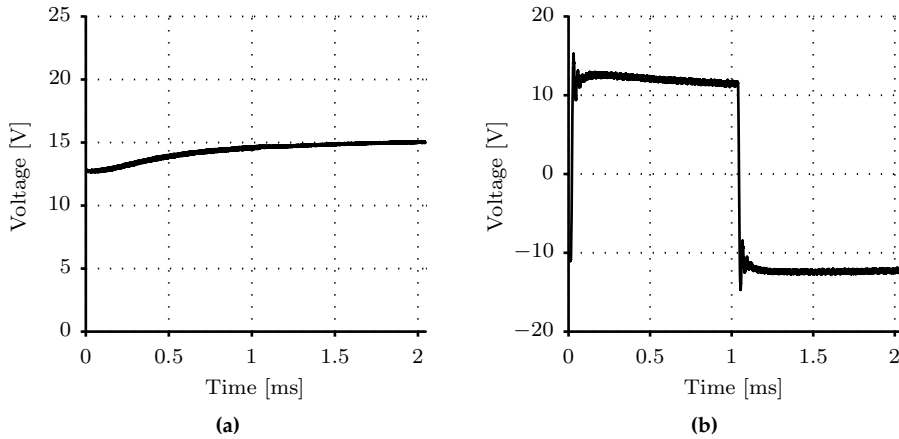


Figure 7.5: Measurement results of the feedback linearization with LQR: Transient response of the output voltage after a step change in the flying-capacitor and initial offset. (a) capacitor voltage (b) output voltage.

achieving high accuracy (32-bit) in the calculations the IQmath library has been used.

For both control algorithms a measurement result is shown in which simultaneously a step is applied in both the output voltage and flying-capacitor voltage reference. Initially, the flying-capacitor voltage has a small offset.

7.3.1 Feedback linearization with LQR

In Figure 7.5 a measurement result has been shown of the implementation of feedback linearization with LQR. The control algorithm is executed at a frequency of 146 kHz. Due to the use of PSCPWM, a three-level output voltage is realized with an effective frequency of twice this frequency (292 kHz). Furthermore, the supply voltage has in this case been set to 30 V and a duty cycle of 0.4 has been used. To remove noise from switching on the measurements a noise filter has been applied to the measured waveforms. The output voltage transient is very fast and it can be seen that the balancing of the flying-capacitor has hardly any influence on this transient. Similar to the simulation results, when the duty cycle or gain are increased and inputs become saturated due to balancing, the transients can become very poor.

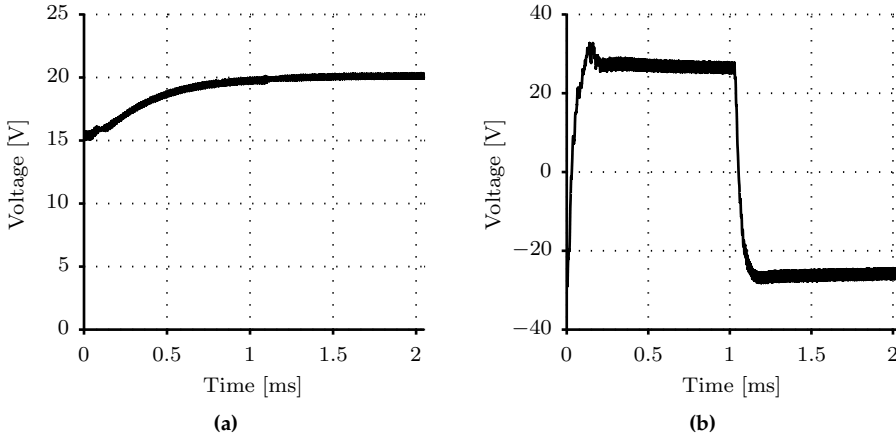


Figure 7.6: Measurement results of vector decoupling with PI control: Transient response of the output voltage after a step change in the flying-capacitor and initial offset. (a) capacitor voltage (b) output voltage.

7.3.2 Vector decoupling with PI control

The calculations of the vector decoupling with PI control took more processing time. As a result, the switching and sample frequency have been reduced to 73 kHz. At the same time the modulation index and supply voltage have been increased to show the input saturation prevention. The measurement results are shown in Figure 7.6 and it can be seen that balancing still has some effect on the transient of the output voltage, although it is much less than without decoupling or saturation prevention.

7.4 Harmonic elimination in parallel converters

The ideas proposed in chapter 6 have been verified on a separate experimental setup. This setup is shown in Figure 7.7 and it is referred to as setup B. The setup makes it possible to verify the proposed ideas for $N = 5$. It consists of (A) an interleaved power amplifier. This amplifier contains two six-packs of IGBTs, which are controlled by 6 individual drivers as indicated by (B). The control board (C) contains a TMS320F28044 digital signal processor (DSP), which is used to create pulse-width modulation. Furthermore, five cell inductors are shown (D) and one additional inductor (E) has been placed to add an extra inductance in one

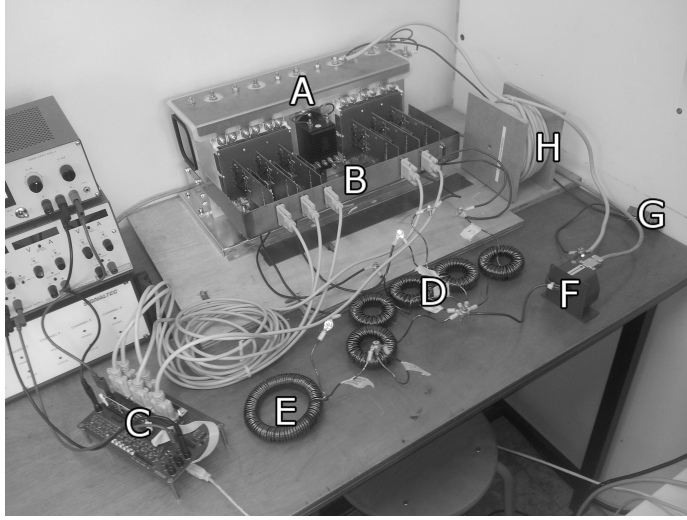


Figure 7.7: Photograph of experimental setup B.

of the cells of approximately 10% of the nominal inductance. The sum current of the three cell currents is measured with an LEM type current sensor (F), behind which the filter capacitor is placed (G) and, lastly, the load inductor is indicated with (H). The current sensor is connected to an oscilloscope, the measured data (current signal) is transferred to an external computer on which the iterative phase-shift algorithm is being executed. This algorithm basically involves a DFT of the measured data and calculation of (6.20), in which

$$F(\Phi_k) = \begin{bmatrix} \text{Im}(I_{\text{sum},1}) \\ \text{Re}(I_{\text{sum},1}) \\ \text{Im}(I_{\text{sum},2}) \\ \text{Re}(I_{\text{sum},2}) \end{bmatrix}, \quad (7.1)$$

where $I_{\text{sum},n}$ denotes the n^{th} harmonic of the sum current. The new phase-shift is then applied in the next iteration. This sequence is repeated until the minimum value is obtained.

7.4.1 Results for five interleaved cells

The results of the measurements for five interleaved cells are shown in Figure 7.8, where they are compared with results obtained during the simulation. First

Table 7.1: Iteration values (measurement).

Iter. #	ϕ_2	ϕ_3	ϕ_4	ϕ_5	h_1	h_2
1	2040	4080	4080	2040	0.0291	0.0092
2	1965	4065	4094	2000	0.0114	0.0023
3	1947	4060	4090	1977	0.0043	0.0002
4	1945	4059	4084	1966	0.0018	0.0002
5	1944	4058	4081	1962	0.0009	0.0001
6	1943	4058	4079	1961	0.0002	0.0002

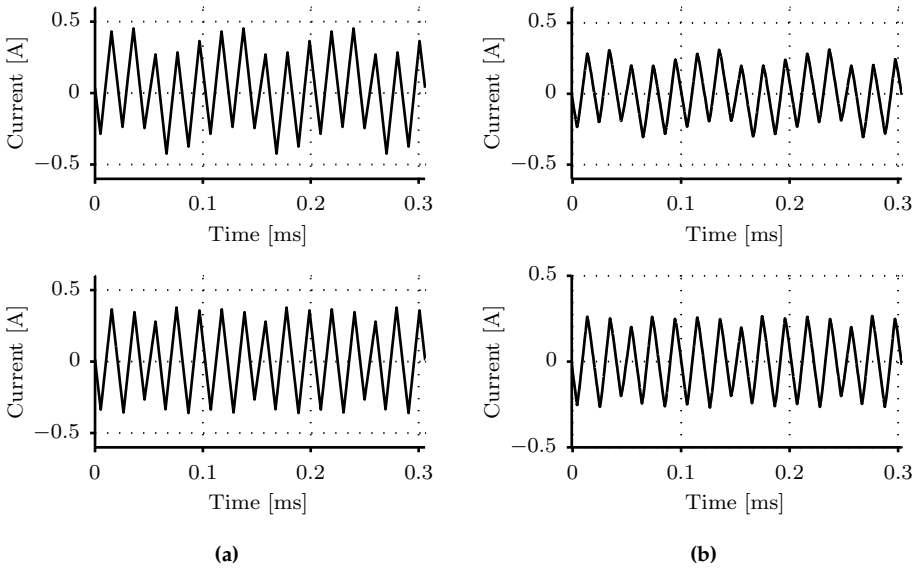


Figure 7.8: Comparison of (a) simulation and (b) measurement results of steady-state behavior: The upper plots show the sum current without correction, the bottom plots the sum current with correction.

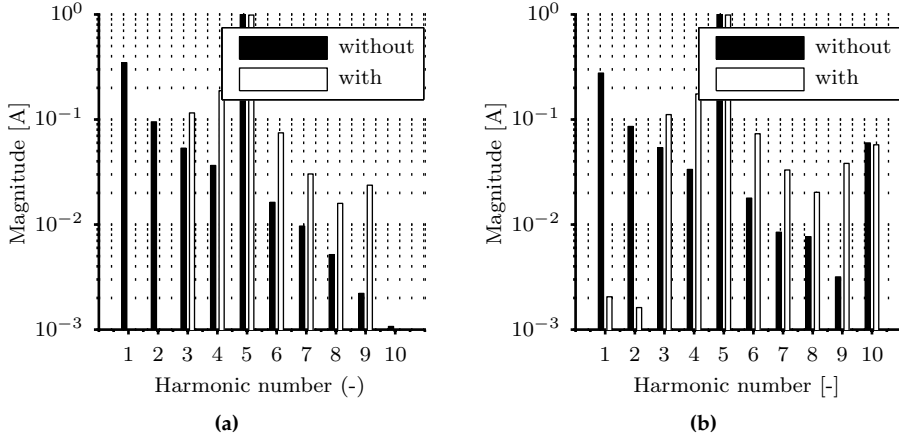
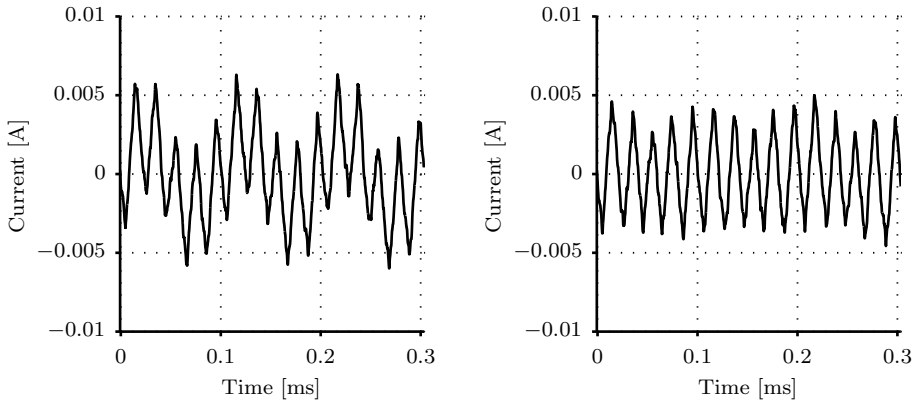


Figure 7.9: Harmonic spectrum of the sum current comparing harmonics with and without the improved phase-shift: (a) Simulation results and (b) measurement results.

of all, the phase-shift values for the iteration process are given in Table 7.1. The parameters which apply to the experimental setup are equal to those that were used for the simulation results presented in chapter 6, and again 10 iterations were performed. In the Table 6 iterations are shown and the 6th iteration shows the best result, after which the algorithm presents an errant behavior. In other words, because of practical limitations the algorithm does not perform as well as in simulation. That is because in the real setup not every cycle is exactly identical, due to measurement noise. It also means that if the phase-shift is fixed, slightly different harmonic components are measured every new switching cycle. Three cycles of the measured sum current, both with and without correction, are shown in Figure 7.8. Note that this is an AC measurement to obtain more bits for the ripple current. Also, a 3-bit noise filter has been applied on the measured current to remove high-frequency oscillations during switching events.

The harmonic spectrum in Figure 7.9 shows that the first two harmonics are significantly reduced. Note that the elimination of the lower-order harmonics comes at the cost of a higher magnitude of higher-order harmonics. Remarkable is the presence of the 10th harmonic as this harmonic was not visible in the simulation results. This is caused by parasitics (such as the switching device output capacitance) that are not included in the model.

During the measurements, a significant delay was noticed, because the switched node voltage was not exactly centrally placed in between the two interrupt pulses. This delay, caused by the driver blanking-time, has been measured and manually



(a) Measured sum current - no phase-shift correction (b) Measured sum current - with phase-shift correction

Figure 7.10: Measurement results of output current (a) without improved phase-shift (b) improved phase-shift.

corrected for ($2\ \mu\text{s}$). Furthermore, during the measurements it was also observed that the output filter capacitor may not be too small, otherwise the capacitor voltage is changing too much in one cycle causing the algorithm to fail. This event has also been verified in the simulations. It is worth recalling that the equations of the algorithm were based on the assumption that the capacitor voltage does not have a ripple.

7.4.2 Output current

Evaluation of the improvement of the sum current due to the phase-shift by a first look at the traces in Figure 7.8 may lead to the conclusion that not much is gained. However, of primary interest is the output current, because this is the current which is passing through the load inductor. This output current is shown in Figure 7.10, and it can be seen directly that here a significant improvement is achieved. Due to the filtering behavior of the capacitor and cell inductors, higher-order switching-frequency harmonics are attenuated more, as is also discussed in section 6.2.1.

7.5 Discussion

In this chapter the experimental results are presented. Measurement results have been shown to demonstrate that the proposed topology and its associated control/modulation scheme provide a feasible solution for power amplification purposes. Specific performance qualifiers such as efficiency or THD have not been determined, because the prototype board has not been optimized for these parameters. Also the proposed closed-loop control methods for flying-capacitor topologies have been implemented on the prototype board and measurement results have been presented.

The proposed ideas related to the improved phase-shift for parallel multicell converters have been tested on a different experimental setup. For the iterative algorithm, the DFT has not yet been implemented on the DSP. For verification and further research, it is therefore recommended to qualify the method when fully implemented on a microcontroller. It should be mentioned that the phase-shift optimization algorithm does not necessarily need to be fast or real time, as the parameters (i.e. inductance values) that would be able to change the phase-shift are expected to change slowly (for instance due to thermal effects).

Part IV

Closing

Chapter 8

Conclusion and discussion

“If you are not part of the solution, you are part of the precipitate.”

(Don Lancaster)

8.1 Conclusions

In this thesis the PowerDAC, a new approach for high-precision power amplification, has been presented and evaluated. The PowerDAC topology may be an attractive and alternative solution for existing power amplifiers. The topology can be seen as a mixture or hybrid between the existing flying-capacitor and series-connected H-bridge topology. The topology might, at first, be most successful in applications where one of these topologies is already employed. For instance, as an alternative to the conventional series-connected H-bridge converter to get rid of isolated voltage supplies. Or as an improvement of the flying-capacitor topology to obtain more voltage levels. While no in-depth analysis has been performed, reliability and ride-through may also be improved, as it is easier to bypass an H-bridge cell than a flying-capacitor cell.

Still, in the current version of the PowerDAC, a number of non-idealities are present, which should be addressed for making the technology successful. First, the requirement of having an output current for balancing the capacitors. This especially plays a major role during start-up, as it might be undesirable to require an output current during start-up. The solution may also solve the problem which occurs at particular duty cycles (i.e. 0.5), where certain correction cells are not switching for a long period. An associated issue are the singular points in the control loop. Second, the asymmetry in the chosen voltage levels leads to a high

number of levels compared to the number of components. However, the requirement to simultaneously switch to jump between adjacent levels has an enormous impact on the performance of the PowerDAC solution.

In general, this research has been a struggle between the ideal and reality. Although we strive to obtain the ideal, in reality we are confronted with practical issues. Especially in multilevel solutions that have been proposed in recent years the ideal seems very promising. The naked reality, however, is that the multilevel concept has already been known for decades, and industry does not seem to hurry implementing this improvement. There is of course the exception of applications in which the two-level approach is simply not an alternative, because of a high voltage and/or high power rating. For multilevel, non-idealities seem to have a huge impact which diminishes the benefits.

In this thesis, on the other hand, two of these non-idealities have been specifically addressed. First, the impact of a capacitor voltage unbalance and the impact of the compensator which is used for balancing these capacitor voltages. Second, the impact of unequal inductors on the output current in interleaved parallel converters. For both issues an effective solution has been proposed. For the coupling effect of a capacitor voltage compensator, two decoupling methods have been proposed. For non-idealities in parallel converters, an improved phase-shift has been proposed. The benefit of both methods has been demonstrated by means of simulation and measurement results.

Additionally, friction between ideal and reality has also been noticed in the theoretical part. In chapter 3 for instance, the duality theorem itself has been part of the discussion. To be able to find the dual transformation of the (non-planar) interleaved converter ($N > 2$), it was necessary to allow the inclusion of transformers. A new type of duality had to be defined and in this situation the duality theorem seems to have lost some of its elegance.

8.2 Original contributions

In this section the main research contributions of this thesis are given.

- **Investigation to the influence of distortions in gradient amplifiers on image quality in MRI.**

Fundamentals of MRI are described from a power-electronics perspective. This brief introduction was required to establish a relation between a current waveform, as generated by a gradient amplifier and the produced image in an MR scanner. Additionally, it is shown how these relations can

form the basis for a simulation tool that can be used for the analysis of gradient amplifier distortions.

- **A proposal for the classification of multilevel converters and the derivation of the interleaved dual.**

A multi-layer classification or taxonomy is proposed for the categorization of power-electronic circuits, in particular multicell topologies. Symmetrical relations have been recognized leading to the dual transformation of interleaved converters.

- **Synthesis of a multilevel converter variant topology.**

An asymmetrical series-connected H-bridge converter topology is proposed in which floating capacitors are used to create the voltage levels. The innovative part of the proposed topology is that it is characterized by the fact that each additional cell has half the voltage and twice the switching frequency of the preceding cell. The topology comes with a modulation scheme that allows fully balanced operation while generating arbitrary waveforms. A proof-of-concept PowerDAC prototype board has been designed and assembled from which we were able to successfully demonstrate the PowerDAC concept.

- **Establishment of two innovative control methods for solving the decoupling problem in series multicell converters.**

For series multicell topologies, two control methods, a vector and nonlinear, are proposed for the decoupling of the capacitor voltage compensator and the output voltage tracking controller. Both methods were successfully implemented both in simulation and on an experimental setup.

- **Development of an improved phase-shift for interleaved parallel converters to counteract distortion caused by unequal output inductors.**

For interleaved parallel converters, a phase-shift correction is proposed to eliminate harmonics in the output current caused by unequal output inductors. Two methods for implementation are presented: A pre-calculated improved phase-shift and an iterative closed-loop optimization. The methods have been successfully verified in simulation and in practice.

Parts of this dissertation has been published elsewhere [14–18,133]. The following scientific papers have been published in conferences and journals:

- M. L. A. Caris, “Output current harmonic elimination of a 3-fold interleaved precision power amplifier,” in Proceedings of the 6th IEEE Young Researchers Symposium in Electrical Power Engineering: challenges in sustainable electrical energy, Apr 2012.

- M. L. A. Caris, H. Huisman, J. M. Schellekens, and J. L. Duarte, "Generalized harmonic elimination method for interleaved power amplifiers," in Proceedings of the 38th Annual Conference on IEEE Industrial Electronics Society (IECON), Oct 2012, pp. 4979–4984.
- J. M. Schellekens, M. L. A. Caris, J. L. Duarte, H. Huisman, M. A. M. Hendrix, and E. Lomonova, "High precision switched mode amplifier with an auxiliary bias circuit," in Proceedings of the 15th European Conference on Power Electronics and Applications (EPE), Sept 2013, pp. 1–10.
- M. L. A. Caris, H. Huisman, and J. L. Duarte, "Harmonic elimination by adaptive phase-shift optimization in interleaved converters," in Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Sept 2013, pp. 763–768.
- M. L. A. Caris, H. Huisman, and J. L. Duarte, "Theoretical analysis of the duality principle applied to interleaved topologies," in Proceedings of the International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), May 2014, pp. 2954–2959.
- M. L. A. Caris, H. Huisman, and J. L. Duarte, "Implementation of various balancing control methods for flying-capacitor power amplifiers," in Proceedings of the International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE), Oct 2015, pp. 115–120.
- M. L. A. Caris, H. Huisman and J. L. Duarte, E. A. Lomonova, "Nonlinear and Vector Closed-loop Control methods for Flying-capacitor Power Converters," International Journal of Electronics, 2016 (accepted).

Patents

- H. Huisman, M.L.A. Caris, "Power converter for powering an MRI gradient coil and method of operating a power converter", WO2013136224 A3, 20 February 2014.
- R.B. Dai, M.L.A. Caris, J.L. Duarte, "Basic Crossover Correction Cells (B3C) for high-precision electric power processing amplifiers", provisional, 3 April 2016.

8.3 Recommendations and future research

While this dissertation has laid the basic groundwork for a new approach in high-precision power amplification, further theoretical and practical improvements

may be addressed. In this section we would like to briefly point out some topics for future research.

First, a basic simulation tool for the analysis of distortions in gradient amplifiers has been established. However, the tool is based on quite some assumptions and other subsystem non-idealities were fully neglected. The analysis could be further improved by including also these neglected aspects. Doing so, a full system analysis can be performed to improve the specifications that are important in the design of such an amplifier.

The analysis of the PowerDAC topology could be further improved if its reliability is investigated. For instance, improved ride-through capabilities can be obtained by adding an additional correction cell, and allowing cells to be bypassed if necessary. Furthermore, it is recommended to investigate the limited balance mode, where also voltage levels are applied which exceed the supply voltage. Using this mode could in some applications lead to a near-doubled peak power from the same circuit. Additionally, it is recommended to investigate the impact of other distortion effects, such as non-ideal switching devices, dead time, external voltage supply distortions more elaborately. Lastly, it would be interesting to realize a setup which includes different switching device technologies (IGBT, MOSFET) in the correction amplifiers.

In the control methods, the nonlinear feedback linearization can be improved if the equations are simplified. For instance, since the output load is linear, it would be convenient if this part of the model is excluded from the feedback linearization. Additionally, to improve the model, and to make it more exact, an observer has to be added for the estimation of the common-mode capacitor voltages. In the practical setup the voltage at the output node is measured, and this measured voltage includes the voltage across the series resistor. It is, therefore, an approximation.

The vector decoupling method could be further improved by analyzing the general case. Based on the results of chapter 4, it is expected that this goal can be accomplished by creating a set of rules that set priorities.

Appendices

Appendix A

Nomenclature

A.1 Symbols

Symbol	Quantity	Unit
B	magnetic field	T
C	capacitance	F
d	duty cycle	—
e	error	—
f	frequency	Hz
G	magnetic field gradient	T m^{-1}
i	current	A
j	imaginary unit ($j^2 = -1$)	—
k	wavenumber	—
K	gain	—
L	angular momentum	$\text{kg m}^2 \text{s}^{-1}$
L	inductance	H
M	net magnetization	T
q	switching function	—
Q	quality factor filter	—
r	spatial position vector	—
r	relative degree	—

Symbol	Quantity	Unit
R	resistance	Ω
s	signal	—
t	time	s
T	time period	s
u	input	—
v	transformed input	—
\boldsymbol{v}	space vector	—
V	voltage	V
x	state	—
y	output	—
γ	gyromagnetic ratio	$\text{rad s}^{-1} \text{T}^{-1}$
ε	electromotive force	V
η	efficiency	—
μ	magnetic moment	N m T^{-1}
$\tilde{\zeta}$	transformed state	—
ρ	proton spin density	moles/m^3
τ	torque	N m
ϕ	PWM phase-shift	rad
ω	angular frequency	rad s^{-1}

A.2 Subscripts

Symbol	Meaning
d	difference
eff	effective
im	imaginary part
L	load
m	main
mc	micro-controller
re	real part
ref	reference
rf	radio-frequency
s	sample
	supply
sw	switching
t	total

A.3 Notation

Acronym	Meaning
t, f	scalar variables are denoted italic
\mathbf{u}, \mathbf{v}	vectors are denoted bold and italic
\mathbf{A}, \mathbf{B}	matrices are denoted bold and upright
i, I, v, V	electric quantities, voltages and currents, when small denote time-dependent functions. Capital size electric quantities denote RMS values
A^T	matrix transpose
A^{-1}	matrix inverse
$\langle x \rangle$	average value
$\langle x, x \rangle$	inner product
x^*	reference value
$\ x\ $	norm or absolute value
\tilde{x}	peak-to-peak ripple

A.4 Acronyms

Acronym	Meaning
AC	Alternating current
ADC	Analog-to-digital converter
APOD	Alternative phase-opposite disposition
CPU	Central processing unit
DAC	Digital-to-analog converter
DC	Direct current
DFT	Discrete Fourier transform
DSP	Digital-signal processor
EMI	Electromagnetic interference
HVDC	High voltage direct current
IC	Integrated circuit
IGBT	Insulated-gate bipolar transistor
LQR	Linear-quadratic regulator
MOSFET	Metal-oxide-semiconductor field-effect transistor
MIMO	Multi-input and multi-output

Acronym	Meaning
MR	Magnetic resonance
MRI	Magnetic resonance imaging
NMR	Nuclear magnetic resonance
PCB	Printed circuit board
PCM	Pulse-code modulation
PD	Phase-disposition
PDM	Pulse-density modulation
PI	Proportional-integral
POD	Phase-opposite disposition
PWM	Pulse-width modulation
QAM	Quadrature-amplitude modulation
RF	Radio frequency
SPI	Serial peripheral interface
SNR	Signal-to-noise ratio
THD	Total harmonic distortion
WHD	Weighted harmonic distortion
ZOH	Zero-order hold

Appendix B

Definitions

B.1 Fourier series and transform

Fourier analysis has been an important tool throughout this thesis when analyzing signals. In this section of the Appendix the key equations and their interrelation are listed together.

B.1.1 Fourier series

Consider a periodic function $f(x)$, satisfying the Dirichlet conditions, within the interval $-L \leq x \leq L$, then $f(x)$ can be written as a Fourier series according to

$$f(x) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} \left(a_n \cos\left(\frac{n\pi}{L}x\right) + b_n \sin\left(\frac{n\pi}{L}x\right) \right), \quad (\text{B.1})$$

where

$$\begin{aligned}
a_n &= \frac{1}{L} \int_{-L}^L f(x) \cos\left(\frac{n\pi}{L}x\right) dx \\
b_n &= \frac{1}{L} \int_{-L}^L f(x) \sin\left(\frac{n\pi}{L}x\right) dx.
\end{aligned} \tag{B.2}$$

A specific harmonic n of the function $f(x)$ is denoted with the addition of a subscript as

$$f_n(x) = a_n \cos\left(\frac{n\pi}{L}x\right) + b_n \sin\left(\frac{n\pi}{L}x\right). \tag{B.3}$$

Often such a specific harmonic component is written as a single sinusoid, that is,

$$f_n(x) = A_n \cos\left(\frac{n\pi}{L}x + \phi_n\right), \tag{B.4}$$

in which

$$\begin{aligned}
A_n &= \sqrt{a_n^2 + b_n^2} \\
\phi_n &= \text{atan2}\{-b_n, a_n\}.
\end{aligned} \tag{B.5}$$

B.1.2 Complex Fourier series expansion

By using the Euler equations the complex version of the Fourier series can be derived, that is by using

$$\begin{aligned}
\cos(x) &= \frac{e^{jx} + e^{-jx}}{2} \\
\sin(x) &= \frac{e^{jx} - e^{-jx}}{2j}.
\end{aligned} \tag{B.6}$$

By substituting (B.6) in (B.1), it is found that

$$f(x) = \sum_{n=-\infty}^{\infty} c_n e^{j\pi n x / L}, \quad (\text{B.7})$$

where

$$c_n = \frac{1}{2L} \int_{-L}^L f(x) e^{-j\pi n x / L} dx. \quad (\text{B.8})$$

The complex coefficients can also be expressed in terms of a_n and b_n , and are given by

$$\begin{aligned} c_n &= \frac{a_0}{2} \quad n = 0 \\ c_n &= \frac{1}{2}(a_n - b_n j) \quad n \in \mathbb{N}_1 \\ c_{-n} &= \frac{1}{2}(a_n + b_n j) \quad n \in \mathbb{N}_1. \end{aligned} \quad (\text{B.9})$$

B.1.3 Fourier transform

Fourier series apply to periodic functions only. For non-periodic functions, it can be shown by approximation [5] that the Fourier transform can be derived. Let us define $k_n = \frac{n\pi}{L}$, and $\Delta k = k_{n+1} - k_n = \frac{\pi}{L}$, then equation B.7 becomes

$$f(x) = \frac{L}{\pi} \sum_{n=-\infty}^{\infty} c_n e^{jk_n x} \Delta k, \quad (\text{B.10})$$

in the limit $L \rightarrow \infty$, the discrete summation becomes a continuous integral with k a continuous variable, and when taking the definition of c_n as in (B.8), the "Fourier integral formula" results as

$$f(x) = \frac{1}{2\pi} \int_{-\infty}^{\infty} \left[\int_{-\infty}^{\infty} f(x) e^{-jkx} dx \right] e^{jkx} dk. \quad (\text{B.11})$$

The Fourier integral formula can be split up into what is defined as the Fourier transform

$$F(k) = \int_{-\infty}^{\infty} f(x) e^{-jkx} dx, \quad (\text{B.12})$$

and the inverse Fourier transform

$$f(x) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(k) e^{jkx} dk. \quad (\text{B.13})$$

Note that the derivation is not mathematically accurate because the Riemann sum approximation does not apply to improper integrals.

B.1.4 Band-limited functions

Consider the inverse Fourier transform of a band-limited function (i.e. a function of which the spectrum is zero outside the band $(-2\pi W, 2\pi W)$),

$$f(x) = \frac{1}{2\pi} \int_{-2\pi W}^{2\pi W} F(k) e^{jkx} dk. \quad (\text{B.14})$$

Then, similar to (B.7), a Fourier series expansion of the spectrum can be defined as

$$F(k) = \sum_{n=-\infty}^{\infty} c_n e^{-jnk/2W}, \quad (\text{B.15})$$

where

$$c_n = \frac{1}{4\pi W} \int_{-2\pi W}^{2\pi W} F(k) e^{jkn/2W} dk = \frac{1}{2W} f\left(\frac{n}{2W}\right). \quad (\text{B.16})$$

This result shows how the spectrum of a band-limited function is determined by $f(\frac{n}{2W})$, i.e. by samples of the original signal.

B.2 Lie Algebra

In this section very briefly the most important aspects of Lie Algebra are revisited. Here, definitions are given of the Lie derivative and the Lie bracket. More detailed and elaborated information can be found in [62, 108].

B.2.1 Lie derivative

Given a smooth function $h(x)$ along a smooth vectorfield $\mathbf{f}(x)$

$$\mathbf{f}(x) = \begin{pmatrix} f_1(x) \\ \vdots \\ f_n(x) \end{pmatrix},$$

the Lie derivative of h with respect to \mathbf{f} is defined as the inner product between $\frac{\delta h}{\delta x}$ and \mathbf{f} , and is denoted as

$$L_{\mathbf{f}}h(x) = \langle \frac{\partial h}{\partial x}, \mathbf{f} \rangle = \frac{\partial h}{\partial x_1} f_1 + \cdots + \frac{\partial h}{\partial x_n} f_n.$$

The Lie derivative operator can be used twice to different vector fields \mathbf{f} and \mathbf{g}

$$L_{\mathbf{g}}L_{\mathbf{f}}h(x) = \langle \frac{\partial(L_{\mathbf{g}}h)}{\partial x}, \mathbf{f} \rangle.$$

The Lie derivative of a higher order is calculated as recursively repeated Lie derivatives

$$L_{\mathbf{f}}^k h(x) = \langle \frac{\partial(L_{\mathbf{f}}^{k-1}h)}{\partial x}, \mathbf{f} \rangle,$$

and with $L_{\mathbf{f}}^0 h(x) = h(x)$.

B.3 Nonlinear control concepts

B.3.1 Relative degree

A MIMO system has a set of relative degrees $\{r^1, \dots, r^m\}$ in a point x_0 if all entries in the set

$$\left\{ \begin{array}{ccc} L_{g_1} L_f^{r^1-k} h^1(x) & \cdots & L_{g_m} L_f^{r^1-k} h^1(x) \\ \vdots & \ddots & \vdots \\ L_{g_1} L_f^{r^m-k} h^m(x) & \cdots & L_{g_m} L_f^{r^m-k} h^m(x) \end{array} \right\} \quad (\text{B.17})$$

are equal to zero for all $k > 1$, and if the characteristic decoupling matrix

$$\mathbf{F}(x) = \begin{bmatrix} L_{g_1} L_f^{r^1-1} h^1(x) & \cdots & L_{g_m} L_f^{r^1-1} h^1(x) \\ \vdots & \ddots & \vdots \\ L_{g_1} L_f^{r^m-1} h^m(x) & \cdots & L_{g_m} L_f^{r^m-1} h^m(x) \end{bmatrix} \quad (\text{B.18})$$

is nonsingular at the point x_0 . The relative degree r^i is, therefore, the smallest number that satisfies the previous conditions for all the m inputs. The total relative degree of the system $r^t = \text{sum}\{r^1, \dots, r^m\}$.

Appendix C

Design aspects of prototype board

C.1 Hardware aspects

For a part of the measurements presented in Chapter 7, the prototype board shown in Figure C.1 is used. The board is referred to as experimental setup A, and in this Appendix the most important design and component selection aspects are described in detail. The main purpose of this prototype is the realization of a proof-of-concept, in which the PowerDAC topology is used as end-stage. However, for demonstration purposes, the board can also be used as full-digital audio amplifier, where audio data (reference data) is read from an SD-card, and converted into an output voltage. As such, it is possible to connect a loudspeaker and listen to music.

A block diagram of the board is shown in Figure C.2. For this prototype, the priority has been to obtain robustness and flexibility. This choice translates in, for instance, the use of overrated components and additional hardware protection circuitry. It should be stressed that, as a consequence of this choice, the prototype board cannot be compared with state-of-the-art high-fidelity audio amplifiers in

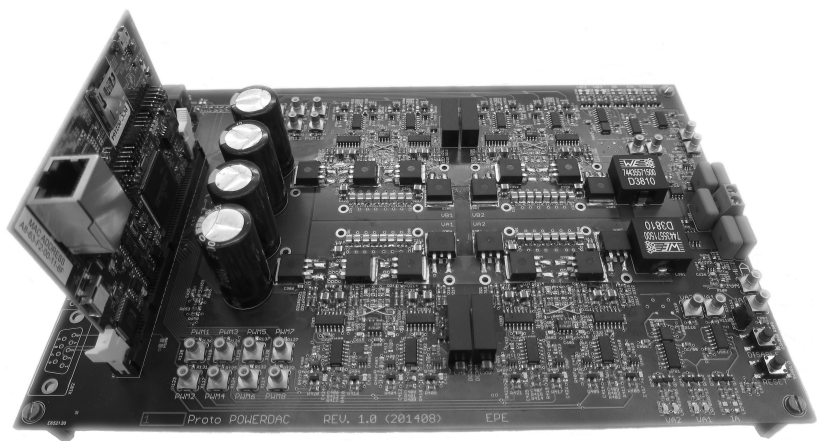


Figure C.1: Photograph of the PowerDAC prototype board.

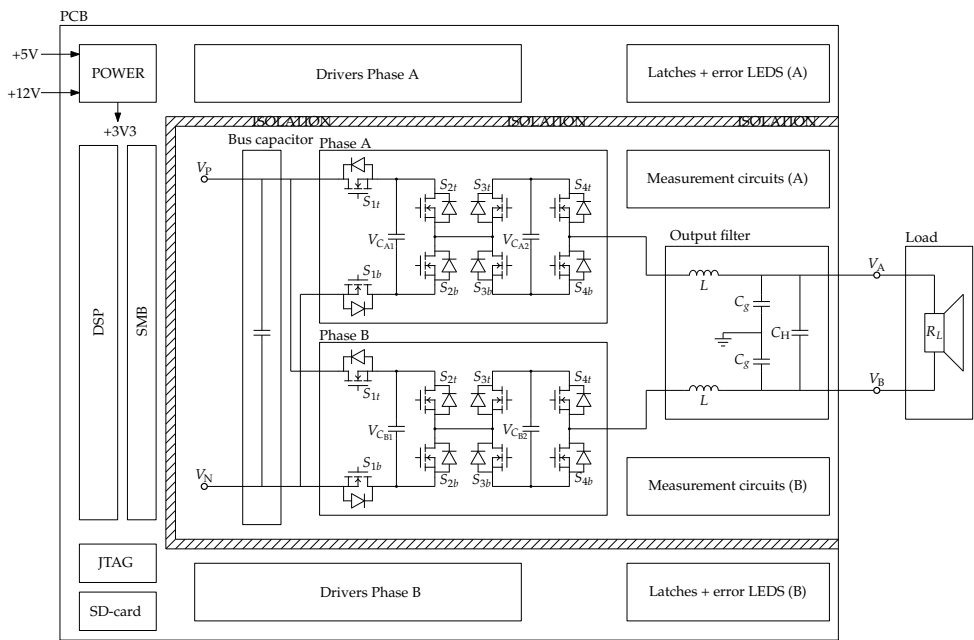


Figure C.2: Block diagram of the PowerDAC prototype.

terms of performance qualifiers, such as THD, SNR or efficiency.

Additionally, all the PWM signals (inputs) and measured signals (outputs) are connected to SMB connectors, which allows the visualization of the most important signals, and, allows for the connection of an external control system. However, this prototype is intended to make use of a so-called DSP ControlCARD (TMDSCNCDH52C1) from Texas Instrument, which can be inserted into a DIMM 100 pin socket. On this prototype board, the ControlCARD contains a TMS320F28M35 DSP. The use of such a relatively cheap microcontroller solution on this prototype demonstrates that the implemented algorithms can be used in industrial applications or products.

The main board is a 4-layer PCB that includes a ground and power plane on the two internal layers, signal traces are placed on the top and bottom layers. Additionally, measurement circuits are present for signal conditioning, and protection circuitry with LED indication is added for the prevention of over-voltages. In the remaining sections of this Appendix some more details are given about the main elements: 1) ControlCARD and DSP 2) the Power stage 3) the driver circuitry 4) floating capacitor voltage measurement circuit.

C.1.1 DSP and controlCARD

The prototype board contains a TMS320F28M35 DSP, which is a multicore microcontroller system-on-a-chip from the Concerto-family of Texas Instruments. It consists of three sub-systems, a communications subsystem, a real-time control subsystem and an analog subsystem. The communication subsystem is based on a 32-bit ARM cortex-M3 CPU and it has access to multiple communication peripherals, such as Ethernet, CAN, SPI and USB. These peripherals can all be controlled/handled by this processing unit. On the prototype board this part of the DSP is mainly used for loading the reference from the SD-card (with SPI), and to communicate with the input power supply through Ethernet and to communicate with an external PC through a UART.

The second subsystem is the control subsystem, which is based on the 32-bit C28x floating-point CPU. It also has access to some of the communication peripherals, however, its main task is to generate the PWM signals based on its inputs (Reference and measured signals). Also, capacitor voltage and output voltage control algorithms are implemented on this part of the DSP. Inter-processor communication in combination with a buffer on the shared RAM is used for transferring the reference between the two cores.

Table C.1: Output power specifications for different load DC resistance values (with 60 V supply voltage)

Resistor value	Peak current	Rated power
4 Ω	15 A	450 W
6 Ω	10 A	300 W
8 Ω	7.5 A	225 W

The third subsystem is the analog subsystem, which consists of 20x 12-bit ADCs. Measurement results can be read out by both cores. Furthermore, the two processing units have access to the shared RAM. Communication with the ADCs takes place through the analog common interface bus. More elaborated information can be found in the product brochure of the DSP or in the datasheet.

C.1.2 Power stage and output filter

The power stage has a full-bridge configuration, which means that there are two phase legs. Each phase leg is constructed from a main amplifier stage and two correction amplifier stages. As explained in Chapter 4, the main amplifier stage and the first correction amplifier stage can be merged together to result in a flying-capacitor stage.

The nominal input voltage is defined as 60 V and, therefore, the switching devices of the first flying-capacitor stage will see a nominal voltage of 30 V. The second stage MOSFETs will see a voltage of 15 V. For all the switching devices in the power stage, 60 V power MOSFETs of Infineon (N-channel OptiMOS) are chosen. The IPB057N06N comes in a D2PAK package (TO-263), which is advantageous, because this package is standard, and makes it possible to replace the MOSFET with another type (also from other suppliers). At the same time this package has a lower parasitic inductance than for instance the classic TO-220, leading to better performance.

Table C.1 displays the peak RMS output power for various DC resistance values of a loudspeaker, which is calculated, assuming sinusoidal current and voltage waveforms, by using

$$P_{\text{peak}} = \frac{(V_s)^2}{2R_L}. \quad (\text{C.1})$$

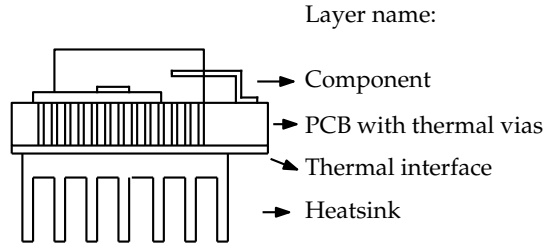


Figure C.3: Construction of a D2PAK MOSFET with heatsink on the backside of a PCB.

Based on [52, 61], and using $\frac{1}{2}V_s = 30\text{ V}$, $f_{sw} = 100\text{ kHz}$, $I_{RMS} = 7.5\text{ A}$, it is estimated that the worst-case losses amount to approximately 6 W . Since the junction-to-ambient thermal resistance amounts to 50 K W^{-1} , a heatsink is required. As classical D2PAK heatsink solutions can take up quite some space, increasing parasitic inductances in the switching legs, it has been chosen to apply the thermal design as depicted in Figure C.3. In this solution, in the pad, on which the component is placed, a large number of VIA holes is drilled. These thermal vias provide a low-resistive thermal pad to the other side of the PCB. On the other side of the PCB it is then possible to place a heatsink. On this protoboard one heatsink is used per 4 switching devices, which means voltage isolation is required because the pads are not all connected to the same voltage potential.

The last element of the power stage are the floating capacitors. Of all capacitor types (i.e. ceramic, film, tantalum, electrolytic), the film capacitor (MKP/MKS) seems to be most suitable, as these capacitors are more often chosen in flying capacitor topologies [30, 148]. An important reason is their capability to handle the switched currents and their relatively low parasitic series resistance (ESR). One disadvantage of film capacitors, though, is their bad volume/capacitance ratio compared to the other capacitor types. As a result, it has been chosen to use ceramic capacitors. This also allows that the placement of the switching devices is better. Each floating capacitor consists of $10 \times 10\text{ }\mu\text{F X7R}$ capacitors from AVX (12105C106KAT2A).

Input and output filter

On this prototype board two filters are placed. At the input side of the power stage $4 \times 1000\text{ }\mu\text{F}$ radial electrolytic capacitors are placed to ensure a stable DC input voltage. Another filter is placed at the output as depicted in Figure. C.2, and component values have been calculated by using [121]. When $L = 15\text{ }\mu\text{H}$, $C_H = 0.47\text{ }\mu\text{F}$ and $C_g = 47\text{ nF}$, it can be found that $\omega_0 \approx 40\text{ kHz}$ and $Q \approx 0.8$.

In series with C_g a resistor of $10\ \Omega$ has been placed to damp the common-mode resonance.

C.1.3 Gate drivers

For controlling the power MOSFETs, a driver circuit is required. Since most of the switching devices are floating in the PowerDAC topology, it is necessary to use isolated gate drivers. Furthermore, it is convenient to use the same driver circuit for all the switching devices, to ensure similar behavior. It means that the two switching devices which are connected to the common ground are also controlled by an isolated driver circuit. Four types of isolated driver technologies have been found [67]:

- Direct with transformer
- Optocoupler isolation IC
- Capacitive isolation IC
- iCoupler isolation IC

From a simple comparison it has been concluded that the ADuM3223 (with iCoupler technology) has the best performance characteristics and is, therefore, the best candidate for the isolated gate driver. Compared to the opto-coupler and capacitive solution the iCoupler technology has less propagation delay and also a better part-to-part delay matching. The coupled transformer has not the optimal switching performance and cannot be used with all duty cycles, due to saturation of the transformer [67].

The ADuM3223 contains two isolated PWM channels, including the driver circuit for both channels. Furthermore, there is no level shifter in the driver circuit for driving the high-side MOSFET (This causes a worse channel-to-channel matching). A disadvantage of the solution is the necessity of an isolated dc-dc converter for supplying the secondary side of the drivers. Also for the selection of an isolated dc-dc supply a simple comparison has been made, and the RP-1212S has been chosen, because it has a relatively low capacitive coupling. A lower capacitive coupling will result in less noise (due to common-mode currents and conducted EMI) on the primary side due to the high switching-frequency component on the secondary ground [36].

One isolated supply for each switching leg can be saved when a bootstrap circuit is used. Such a bootstrap circuit is also suitable for a flying-capacitor stage. In Figure C.4 a schematic diagram is shown of the entire driver circuit. A resistor

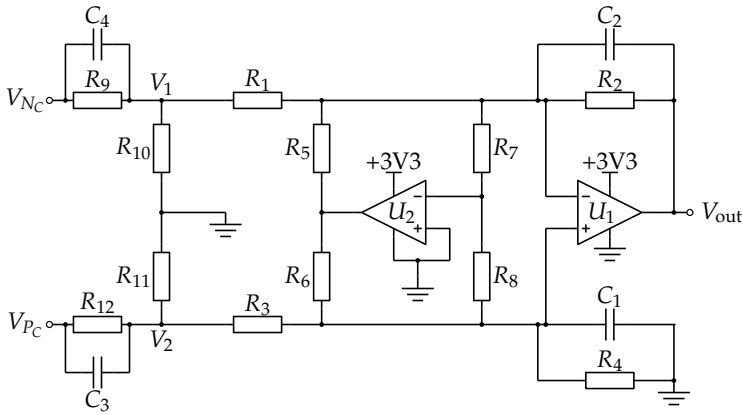


Figure C.5: Circuit diagram of floating-capacitor voltage measurement.

Table C.2: Voltage measurement circuit parameters

Parameter	Description	Value	Unit
$R_1 \dots R_4$	Differential amp resistors	10	[k Ω]
$R_5 \dots R_8$	Common-mode correction resistors	10	[k Ω]
R_9, R_{12}	Voltage divider resistors 1	100	[k Ω]
R_{10}, R_{11}	Voltage divider resistors 2	33	[k Ω]
C_1, C_2	Filter capacitors	10	[pF]
C_3, C_4	Filter capacitors	1	[pF]

for a direct connection to the ADC. The input voltage of the ADC on the DSP is limited to 3 V, and these voltage divider resistors are calculated such that an absolute maximum voltage of 40 V results in a 3 V output voltage. Since the voltages are measured, a comparator will generate an error signal when the maximum voltage is exceeded. Additionally, on the TI controlCARD, protection diodes are placed in front of the ADC, providing an additional security measure. In the following the three sub-parts are described briefly in more detail.

Differential amplifier

First, only the differential amplifier is considered. The output voltage can be calculated with the resistor values by using

$$V_{\text{out}} = \frac{(R_2 + R_1) \cdot R_4}{(R_3 + R_4) \cdot R_1} V_2 - \frac{R_2}{R_1} V_1. \quad (\text{C.2})$$

When the amplifier is designed symmetrical and $R_1 = R_3$ and $R_2 = R_4$, the expression simplifies to

$$V_{\text{out}} = \frac{R_2}{R_1} (V_2 - V_1). \quad (\text{C.3})$$

This equation directly shows a simple proportional relation between the differential input voltage and the output voltage.

Voltage divider

The next step is to take also the voltage divider into consideration. The voltage division can be calculated by using

$$V_{\text{out}} = \frac{R_2 R_{10}}{R_1 R_{10} + R_9 (R_1 + R_{10})} (V_{\text{PC}} - V_{\text{NC}}), \quad (\text{C.4})$$

in which it assumed that the circuit is fully symmetrical ($R_9 = R_{12}$, and $R_{10} = R_{11}$). The resistor values which are applied on the prototype board are shown in Table C.2, and when applying these values in (C.4), the equation becomes

$$V_{\text{out}} = 0.07127 \cdot (V_{\text{PC}} - V_{\text{NC}}). \quad (\text{C.5})$$

The inverse of the conversion factor is 14.0303, which can be used as a constant in DSP to retrieve the actual voltage.

Common-mode suppression

The resistors $R_5 \dots R_8$ and opamp U_2 are used to suppress the common-mode voltage seen by U_1 . The non-inverting input of opamp U_2 is connected to ground and the output of the output is now controlled such that the inverting input also tends to go to 0 V. This circuit is, therefore, correcting for the common-mode voltage seen by inputs of the other opamp U_1 . In terms of component variations, it is important that R_5, R_6 and R_7, R_8 are approximately equal.

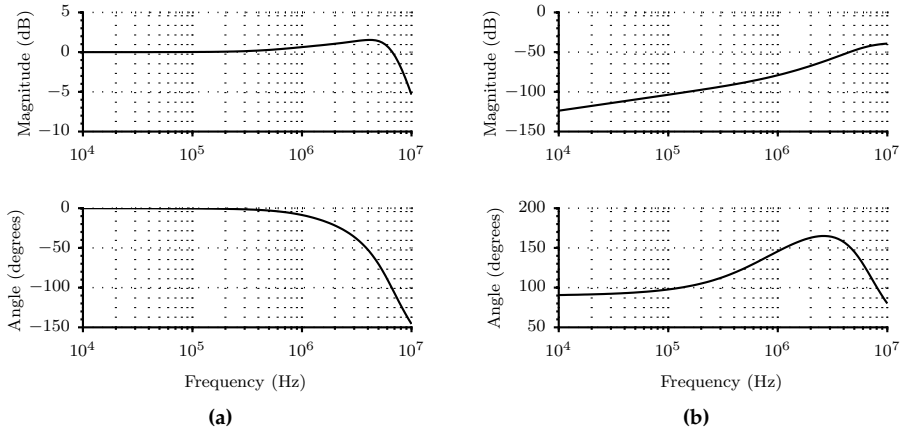


Figure C.6: Frequency response of transfer function (a) differential mode (b) common-mode.

Simulation result

The circuit has been simulated in LTspice to demonstrate its performance. In this simulation a realistic voltage waveform has been applied to the input of the circuit, including a 30 V, 100 kHz common-mode signal. Furthermore, parasitic capacitances (approx. 200 fF) have been added parallel to the input resistances. A frequency response analysis has been performed and the Bode plots, both for common-mode and differential mode, are shown in Figure C.6. The differential mode shows almost no gain/attenuation and phase-shift up to 1 MHz. Common-mode rejection is 100 dB at 100 kHz. Both frequency responses have been corrected for nominal gain.

C.2 Software aspects

In this section, very briefly, two main aspects of the software implementation are explained. In the first subsection some details are provided regarding the implementation of open-loop sound play and in the second subsection the implementation of closed-loop methods is explained in more detail. All software on the DSP has been written in the C programming language. Code composer studio is the integrated development environment which is used to compile the C-code and to program the processor. The tool also includes a debug environment and

provides a communication interface for real-time observing the internal registers and variables.

C.2.1 Open-loop sound play

The PowerDAC prototype is designed in such a way that any digital reference can be played. There are two possibilities for loading a digital reference: Either the reference is directly generated or available on the DSP, and, for instance, periodic signals (such as a sine) wave are put in a lookup table. The second option is to load a reference from an external storage (SD-card). The latter method can be used for larger reference files, such as an entire audio file. Both methods have the advantage that there is only one clock involved for the waveform generation.

In principle we would like to generate an audio data stream. However, since the DSP is a dual core, during the implementation one faces a number of challenges, because the ARM-core communicates with the SD-card, while the C2000-core generates the PWM. Therefore, a circular buffer is implemented on the shared RAM to transfer data from one core to the other. This buffer contains two large blocks of 256x16 bit reference values. A read-pointer tracks the index, and when all reference values in one block have been used, an interrupt is generated to retrieve a new block of data from the SD-card. The buffer is sufficiently large for playing a 16-bit 48 kHz audio file.

C.2.2 Closed-loop algorithm implementation

For the closed-loop implementation, besides the reference loading sequence described in the previous subsection, a control algorithm needs to be executed. This is done as follows: At the start of one PWM cycle, when the PWM period counter is zero, a start-of-conversion signal is sent to the ADC module. When all the relevant measurements have been obtained, an interrupt is generated by the ADC. In this interrupt the calculations are performed which are necessary to calculate the duty cycles for the next cycle. These mathematical calculations are performed with the use of the `IQmath` library to obtain more accuracy. This library emulates floating-point calculations, while in the background 32-bit fixed-point calculations are performed. The described sequence is repeated as long as the DSP is operational.

Bibliography

- [1] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters - State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics*, no. 8, pp. 2581–2596, Aug 2010.
- [2] S. Bacha, I. Munteanu, and A. I. Bratcu, *Power Electronic Converters Modeling and Control*. Springer-Verlag London, 2014.
- [3] Z. Bai and Z. Zhang, "Conformation of Multilevel Current Source Converter Topologies Using the Duality Principle," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2260 –2267, Sept 2008.
- [4] R. H. Baker, "High-voltage converter circuit," US Patent 4 203 151, 1980.
- [5] R. J. Beerends, H. G. ter Morsche, J. C. van den Berg, and E. M. van de Vrie, *Fourier and Laplace Transforms*. Cambridge University Press, 2003.
- [6] P. M. Bhagwat and V. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-19, no. 6, pp. 1057–1069, 1983.
- [7] A. Bhat and F. Tan, "A unified approach to characterization of PWM and quasi-PWM switching converters: topological constraints, classification,

- and synthesis," *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 719–726, Oct 1991.
- [8] T. H. Blakesley, "A new electrical theorem," *Proc. Phys. Soc. London*, vol. 13, pp. 65–67, 1894.
- [9] A. Bloch, "On methods for the construction of networks dual to nonplanar networks," *Proc. Phys. Soc.*, vol. 58, pp. 677–694, 1946.
- [10] N. Bohr, "Über die Serienspektren der Elemente," *Zeitschrift für Physik*, vol. 2, pp. 423–478, 1920.
- [11] B. Bose, "Recent advances in power electronics," *IEEE Transactions on Power Electronics*, vol. 7, no. 1, pp. 2–16, Jan 1992.
- [12] T. Bruckner and S. Bemet, "Loss balancing in three-level voltage source inverters applying active NPC switches," in *Proceedings of the 32nd Annual Power Electronics Specialists Conference (PESC)*, vol. 2, 2001, pp. 1135–1140.
- [13] S. Busquets-Monge, J. Bordonau, and J. Rocabert, "A Virtual-Vector Pulsewidth Modulation for the Four-Level Diode-Clamped DC-AC Converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1964–1972, Jul 2008.
- [14] M. L. A. Caris, "Output current harmonic elimination of a 3-fold interleaved precision power amplifier," in *Proceedings of the 6th IEEE Young Researchers Symposium in Electrical Power Engineering : challenges in sustainable electrical energy*, Apr 2012.
- [15] M. L. A. Caris, H. Huisman, and J. L. Duarte, "Harmonic elimination by adaptive phase-shift optimization in interleaved converters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2013, pp. 763–768.
- [16] M. L. A. Caris, H. Huisman, and J. L. Duarte, "Theoretical analysis of the duality principle applied to interleaved topologies," in *Proceedings of the International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 2954–2959.
- [17] M. L. A. Caris, H. Huisman, and J. L. Duarte, "Implementation of various balancing control methods for flying-capacitor power amplifiers," in *Proceedings of the International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE)*, Oct 2015, pp. 115–120.
- [18] M. L. A. Caris, H. Huisman, J. M. Schellekens, and J. L. Duarte, "Generalized harmonic elimination method for interleaved power amplifiers," in

- Proceedings of the 38th Annual Conference on IEEE Industrial Electronics Society (IECON)*, Oct 2012, pp. 4979–4984.
- [19] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, “A new multilevel PWM method - a theoretical analysis,” *IEEE Transactions on Power Electronics*, vol. 7, no. 3, pp. 497–505, Jul 1992.
- [20] T. Chaudhuri, “Cross Connected Multilevel Voltage Source Inverter Topologies for Medium Voltage Applications,” Ph.D. dissertation, Ecole polytechnique fédérale de Lausanne, 2008.
- [21] J. N. Chiasson, B. Ozpineci, and L. M. Tolbert, “A Five-Level Three-Phase Hybrid Cascade Multilevel Inverter Using a Single DC Source for a PM Synchronous Motor Drive,” in *Proceedings of the 2nd Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2007, pp. 1504–1507.
- [22] N. S. Choi, J. G. Cho, and G. H. Cho, “A general circuit topology of multilevel inverter,” in *Proceedings of the 22nd Annual IEEE Power Electronics Specialists Conference (PESC)*, Jun 1991, pp. 96–103.
- [23] L. Corradini, D. Maksimovic, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. Wiley-IEEE Press, 2015.
- [24] L. Costa, S. Mussa, and I. Barbi, “Capacitor voltage balancing control of multilevel DC-DC converter,” in *Proceedings of the Brazilian Power Electronics Conference (COBEP)*, Oct 2013, pp. 332–338.
- [25] B. Cougo, “Design and Optimization of InterCell Transformers for Parallel MultiCell Converters,” Ph.D. dissertation, Institut National Polytechnique de Toulouse (INP Toulouse), 2010.
- [26] S. Cuk, “General Topological Properties of Switching Structures,” *IEEE Power Electronics Specialists Conference*, vol. 1, pp. 109–130, 1979.
- [27] A. Damiano, M. Fracchia, M. Marchesoni, and I. Marongiu, “A new approach in multilevel power conversion,” *EPE 1997 Conference Record*, vol. 4, pp. 4216–4221, 1997.
- [28] F. Defay, A. M. Llor, and M. Fadel, “Direct Control Strategy for a Four-Level Three-Phase Flying-Capacitor Inverter,” *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2240–2248, Jul 2010.
- [29] C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*. McGraw-Hill, 1969.

- [30] F. Dijkhuizen and J. Duarte, "Proper choice of flying capacitors based on distinct power dissipation models," in *Proceedings of the 33rd IAS Annual Meeting Industry Applications Conference*, vol. 2, Oct 1998, pp. 1174–1180.
- [31] F. Dijkhuizen, "A converter arrangement for power compenstation and a method for contcontrol a power converter," WO Patent 2014/194 968A1, 2014.
- [32] Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "A cascade multilevel inverter using a single DC source," in *Proceedings of the 21th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar 2006, pp. 5 pp.–.
- [33] J. Duarte, "Small-signal modelling and analysis of switching converters using MATLAB," *International Journal of Electronics*, vol. 85, pp. 231–269, 1998.
- [34] J. Duarte, L. Offringa, and W. v. Groningen, "Stability analysis of multilevel converters with nested cells," *EPE Journal*, vol. 9(3-4), pp. 26–32, 2000.
- [35] D. Dujic, C. Zhao, A. Mester, J. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power Electronic Traction Transformer-Low Voltage Prototype," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5522–5534, Dec 2013.
- [36] R. W. Erickson, "EMI and Layout Fundamentals for Switched-Mode Circuits," university of Colorado, Supplementary notes on ECEN 5797 Power Electronics.
- [37] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," in *Proceedings of the 11th Annual Applied Power Electronics Conference and Exposition (APEC)*, vol. 1, Mar 1996, pp. 207–213.
- [38] E. Espinosa, J. Espinoza, F. Villarroel, J. Munoz, P. Melin, and R. Ramirez, "A novel modulation technique for asymmetric multi-cell inverters of 27-level without regeneration," in *Proceedings of the 38th Annual Conference on IEEE Industrial Electronics Society (IECON)*, Oct 2012, pp. 123–128.
- [39] S. S. Fazel, "Investigation and Comparison of Multi-Level Converters for Medium Voltage Applications," Ph.D. dissertation, Technische Universität Berlin, 2007.
- [40] N. Flourentzou, V. Agelidis, and G. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592–602, Mar 2009.

- [41] H. Foch and T. Meynard, "Electronic device for converting electrical energy," EP Patent 0 555 432, 1995.
- [42] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, Jun 2008.
- [43] S. Freeland, "Techniques for the practical application of duality to power circuits," *IEEE Transactions on Power Electronics*, vol. 7, no. 2, pp. 374–384, Apr 1992.
- [44] R. Frodeman, J. Klein, and C. Mitcham, *Oxford Handbook of Interdisciplinarity*. Oxford University Press, 2010.
- [45] O. Garcia, A. De Castro, P. Zumelis, and J. Cobos, "Digital-Control-Based Solution to the Effect of Nonidealities of the Inductors in Multiphase Converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2155–2163, 2007.
- [46] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: active control and observation of flying-capacitor voltages," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 998–1008, Oct 2002.
- [47] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): properties and design," in *Proceedings of the 32nd Annual Power Electronics Specialists Conference (PESC)*, vol. 3, 2001, pp. 1583–1588.
- [48] A. Ghias, J. Pou, M. Ciobotaru, and V. Agelidis, "Voltage-Balancing Method Using Phase-Shifted PWM for the Flying Capacitor Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4521–4531, Sept 2014.
- [49] R. Giri, R. Ayyanar, and E. Ledezma, "Input-series and output-series connected modular DC-DC converters with active input voltage and output voltage sharing," in *Proceedings of the 19th Annual Applied Power Electronics Conference and Exposition (APEC)*, vol. 3, 2004, pp. 1751–1756.
- [50] B. Girod, *Signal and Systems*. John Wiley & Sons, 2001.
- [51] G. Gong, D. Hassler, and J. Kolar, "A Comparative Study of Multicell Amplifiers for AC-Power-Source Applications," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 149–164, 2011.
- [52] D. D. Graovac, M. Purschel, and A. Kiep, "MOSFET Power Losses Calculation Using the Datasheet Parameters," Jul 2006.

- [53] E. M. Haacke, R. W. Brown, M. R. Thompson, and R. Venkatesan, *Magnetic Resonance Imaging: Physical Principles and Sequence Design*. John Wiley & Sons, 1999.
- [54] C. Haederli, "Convertisseurs multiniveaux a bus continu avec point milieu. Nouvelles topologies et strategies de controles," Ph.D. dissertation, Institut National Polytechnique de Toulouse, 2008.
- [55] L. G. Hanson, "Is Quantum Mechanics necessary for understanding Magnetic Resonance," *Concepts in Magnetic Resonance Part A.*, vol. 32A, pp. 329–340, 2008.
- [56] A. D. Ho, M. Schuck, and R. C. N. Pilawa-Podgurski, "Asymmetric interleaving in low-voltage CMOS power management with multiple supply rails," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 365–372.
- [57] P. Horowitz and W. Hill, *The Art of Electronics*. Cambridge University Press, 1989.
- [58] S. H. Hosseini and R. M. Mathur, "A binary multi-level voltage-source inverter for static VAR generation," in *Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering*, vol. 2, May 1997, pp. 427–430.
- [59] J. Huang and K. Corzine, "Extended operation of flying capacitor multi-level inverters," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 140–147, Jan 2006.
- [60] H. Huisman, "Lecture notes in Special topics in Power Electronics," May 2012.
- [61] Infineon, "IPB057N06N Datasheet," Dec 2012, rev.2.2.
- [62] A. Isidori, *Nonlinear Control Systems*. Springer-Verlag Berlin, 1995.
- [63] A. J. Jerri, "The Shannon sampling theorem - Its various extensions and applications: A tutorial review," *Proceedings of the IEEE*, vol. 65, no. 11, pp. 1565–1596, Nov 1977.
- [64] D. W. Kang, W. K. Lee, and D. S. Hyun, "Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter," *IEE Proceedings - Electric Power Applications*, vol. 151, no. 2, pp. 239–248, Mar 2004.
- [65] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*. Pearson, 1991.

- [66] C. T. Kelley, *Solving Nonlinear Equations with Newton's Method*, N. J. Higham, Ed. Siam, 2003.
- [67] B. Kennedy, "Implementing an Isolated Half-Bridge Gate Driver," *Analog Dialogue*, vol. 46, pp. 1–3, May 2012.
- [68] W. Kester, *The Data Conversion Handbook*. Analog Devices, 2005.
- [69] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 769–778, Feb 2012.
- [70] F. Khoucha, A. Ales, A. Khoudiri, K. Marouani, M. E. H. Benbouzid, and A. Kheloui, "A 7-level single DC source cascaded H-bridge multilevel inverters control using hybrid modulation," in *Proceedings of the International Conference on Electrical Machines (ICEM)*, Sept 2010, pp. 1–5.
- [71] J. Kolar, H. Ertl, and F. Zach, "Quasi-dual modulation of three-phase PWM converters," *IEEE Transactions on Industry Applications*, vol. 29, no. 2, pp. 313–319, Mar/Apr 1993.
- [72] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.
- [73] J. Kroot, "Analysis of Eddy Currents in a Gradient Coil," Ph.D. dissertation, Technical University Eindhoven, 2005.
- [74] R. Lai, J. Sabate, S. Chi, and W. Skeffington, "High performance gradient driver for magnetic resonance imaging system," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2011, pp. 3511–3515.
- [75] E. Landsman, "A unifying derivation of switching DC-DC converter topologies," *IEEE Power Electronics Specialists Conference*, pp. 239–243, 1979.
- [76] A. Lega, S. Munk-Nielsen, F. Blaabjerg, and D. Casadei, "Multilevel converters for UPS applications: comparison and implementation," in *Proceedings of the 12th European Conference on Power Electronics and Applications (EPE)*, Sept 2007, pp. 1–9.
- [77] E. Lemmen, J. van Duivenbode, J. L. Duarte, and E. A. Lomonova, "Flexible Multilevel Converters Using Four-Switch Extended Commutation Cells," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 3, pp. 794–804, Sept 2015.

- [78] A. Leredde, "Étude, Commande et Mise en Oeuvre de Nouvelles Structures Multiniveaux," Ph.D. dissertation, Institut National Polytechnique de Toulouse (INP Toulouse), 2011.
- [79] B. R. Lin and J. Y. Chen, "Interleaved resonant converter with the balanced flying capacitors," *IET Power Electronics*, vol. 8, no. 3, pp. 447–457, 2015.
- [80] M. Liserre, V. Monopoli, A. Dell'Aquila, A. Pigazo, and V. Moreno, "Multi-level Phase-Shifting Carrier PWM Technique in case of Non-Equal DC-Link Voltages," in *Proceedings of the 32nd Annual Conference on IEEE Industrial Electronics (IECON)*, Nov 2006, pp. 1639–1642.
- [81] S. Lloyd, "Least squares quantization in PCM," *IEEE Transactions on Information Theory*, vol. 28, no. 2, pp. 129–137, Mar 1982.
- [82] P. Lorrain, D. R. Corson, and F. Lorrain, *Electromagnetic Fields and Waves*. W. H. Freeman and Company, 1988.
- [83] M. D. Manjrekar and T. A. Lipo, "A generalized structure of multilevel power converter," in *Proceedings of the International Conference on Power Electronic Drives and Energy Systems for Industrial Growth*, vol. 1, Dec 1998, pp. 62–67.
- [84] M. Manjrekar, P. Steimer, and T. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 834–841, May/Jun 2000.
- [85] S. Mariethoz, "Systematic Design of High-Performance Hybrid Cascaded Multilevel Inverters With Active Voltage Balance and Minimum Switching Losses," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3100–3113, Jul 2013.
- [86] S. Mariethoz and A. Rufer, "Design and control of asymmetrical multi-level inverters," in *Proceedings of the 28th Annual Conference on IEEE Industrial Electronics Society (IECON)*, vol. 1, Nov 2002, pp. 840–845.
- [87] R. Marks, *Introduction to Shannon Sampling and Interpolation Theory*. Springer-Verlag New York, 1991.
- [88] MATLAB, 8.1.0.604 (R2013a). Natick, Massachusetts: The MathWorks Inc., 2013.
- [89] J. Max, "Quantizing for minimum distortion," *IRE Transactions on Information Theory*, vol. 6, no. 1, pp. 7–12, Mar 1960.

- [90] B. P. McGrath and D. G. Holmes, "Natural Current Balancing of Multicell Current Source Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1239–1246, May 2008.
- [91] B. P. McGrath and D. G. Holmes, "Enhanced Voltage Balancing of a Flying Capacitor Multilevel Converter Using Phase Disposition (PD) Modulation," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1933–1942, Jul 2011.
- [92] B. P. McGrath, D. G. Holmes, M. Manjrekar, and T. A. Lipo, "An improved modulation strategy for a hybrid multilevel inverter," in *Proceedings of the Industry Applications Conference*, vol. 4, Oct 2000, pp. 2086–2093.
- [93] C. W. T. McLyman, *Transformer and inductor design handbook*, 3rd ed. Marcel Dekker, 2004.
- [94] W. McMurray, "Fast response stepped-wave switching power converter circuit," US Patent 3 581 212, 1971.
- [95] D. W. McRobbie, E. A. Moore, M. J. Graves, and M. R. Prince, *MRI from Picture to Proton*. Cambridge University Press, 2006.
- [96] T. Meynard, B. C. Laplace, F. Forest, and E. Labouré, "Parallel multicell converters for high current: Design of intercell transformers," in *Proceedings of the IEEE International Conference on Industrial Technology (ICIT)*, Mar 2010, pp. 1359–1364.
- [97] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Proceedings of the 23rd Annual Power Electronics Specialists Conference (PESC)*, Jun 1992, pp. 397–403.
- [98] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 955–964, Oct 2002.
- [99] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," *International Journal of Electronics*, vol. 42, 6, pp. 521–550, 1977.
- [100] R. Middlebrook, *Advances in Switched-Mode Power Conversion*. TESLAcO, California Institute of Technology, 1983.
- [101] C. Mitcham, *Thinking through technology - the path between engineering and philosophy*. The University of Chicago Press, 1994.

- [102] Z. Mohzani, B. P. McGrath, and D. G. Holmes, "A generalised natural balance model and balance booster filter design for three level neutral point clamped converters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 211–218.
- [103] O. Mueller and J. Park, "Quasi-linear IGBT inverter topologies," in *Proceedings of the 9th Annual Applied Power Electronics Conference and Exposition (APEC)*, vol. 1, Feb 1994, pp. 253–259.
- [104] R. Munnig Schmidt, G. Schitter, A. Rankers, and J. Van Eijk, *The Design of High Performance Mechatronics 2nd Revised Edition*. IOS Press, 2014.
- [105] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.
- [106] C. Ng and L. Ran, *Offshore Wind Farms: Technologies, Design and Operation*. Woodhead Publishing Ltd, 2016.
- [107] D. Nielsen, A. Knott, and M. Andersen, "Multilevel inverter based class D audio amplifier for capacitive transducers," in *Proceedings of the 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, Aug 2014, pp. 1–7.
- [108] H. Nijmeijer and A. van der Schaft, *Nonlinear Dynamical Control Systems*. Springer-Verlag New York, 1990.
- [109] P. Palanivel and S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," *IET Power Electronics*, vol. 4, no. 8, pp. 951–958, Sept 2011.
- [110] R. Parry, "Episteme and Techne," in *The Stanford Encyclopedia of Philosophy*, fall 2014 ed., E. N. Zalta, Ed., 2014.
- [111] G. Peeren, "Stream Function Approach for Determining Optimal Surface Currents," Ph.D. dissertation, Technische Universiteit Eindhoven, 2003.
- [112] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611–618, Mar/Apr 2001.
- [113] F. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Proceedings of the International Power Electronics Conference (IPEC)*, Jun 2010, pp. 492–501.

- [114] M. A. Perez and S. Kouro, "Asymmetric cascaded converter for solar PV applications," in *Proceedings of the 23rd International Symposium on Industrial Electronics (ISIE)*, Jun 2014, pp. 2484–2489.
- [115] Philips, *Basic Principles of MR Imaging*. Philips.
- [116] Philips, "Picture of Philips Achieva 1.5T SE," <http://www.medical.philips.com/main/products/mri/systems/achieveaSE>, Jan 2016, accessed: 2016-01-14.
- [117] V. F. Pires and J. F. Silva, "Hybrid cascade multilevel inverter using a single DC source for open-end winding induction motors," in *Proceedings of the IEEE International Conference on Industrial Technology (ICIT)*, Mar 2012, pp. 966–970.
- [118] PLECS, *version 3.6.2*. Zurich, Switzerland: Plexim GmbH, 2014.
- [119] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 190–196, Feb 2005.
- [120] Prodrive Technologies, "Picture of NG1800 MR gradient amplifier," <https://prodrive-technologies.com/products/ng1800-mri-gradient-amplifier/>, Jun 2016, accessed: 2016-06-06.
- [121] Y. B. Quek, "Class-D LC Filter Design," Jan 2008.
- [122] C. Rech and J. R. Pinheiro, "Hybrid Multilevel Converters: Unified Analysis and Design Considerations," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 1092–1104, Apr 2007.
- [123] J. D. Reiss, "Understanding Sigma-Delta modulation: The solved and unsolved issues," *J. Audio Eng. Soc.*, vol. 56, pp. 49–64, 2008.
- [124] J. P. Ridgway, "Cardiovascular magnetic resonance physics for clinicians, Part 1," *Journal of Cardiovascular Magnetic Resonance*, pp. 12–71, 2010.
- [125] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219–2230, Jul 2010.
- [126] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug 2002.
- [127] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A Five-Level Inverter Topology with Single-DC Supply

- by Cascading a Flying Capacitor Inverter and an H-Bridge," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3505–3512, Aug 2012.
- [128] J. A. Ross, "High Power Synthetic Waveform Generator," US Patent 3 100 851, 1963.
- [129] J. A. Sabaté, R. R. Wang, F. Tao, and S. Chi, "Magnetic Resonance Imaging Power: High-Performance MVA Gradient Drivers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 280–292, Mar 2016.
- [130] A. K. Sadigh, V. Dargahi, M. Abarzadeh, and S. Dargahi, "Reduced DC voltage source flying capacitor multicell multilevel inverter: analysis and implementation," *IET Power Electronics*, vol. 7, no. 2, pp. 439–450, Feb 2014.
- [131] K. Sano and H. Fujita, "Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters," *IEEE Transactions on Industry Applications*, vol. 44, no. 6, pp. 1768–1776, Nov 2008.
- [132] J. M. Schellekens, "A class of robust switched-mode power amplifiers with highly linear transfer characteristics - On the elimination of zero-crossing distortion in switching converters," Ph.D. dissertation, Eindhoven University of Technology, 2014.
- [133] J. M. Schellekens, M. L. A. Caris, J. L. Duarte, H. Huisman, M. A. M. Hendrix, and E. Lomonova, "High precision switched mode amplifier with an auxiliary bias circuit," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–10.
- [134] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Elimination of zero-crossing distortion for high-precision amplifiers," in *Proceedings of the 37th Annual Conference on IEEE Industrial Electronics Society (IECON)*, Nov 2011, pp. 3370–3375.
- [135] F. Schmitt, "The Gradient System. Understanding Gradients from an EM perspective," *Proc. Intl. Soc. Mag. Reson. Med.*, vol. 21, pp. 1–13, 2013.
- [136] M. Schuck and R. C. N. Pilawa-Podgurski, "Ripple Minimization Through Harmonic Elimination in Asymmetric Interleaved Multiphase DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7202–7214, Dec 2015.
- [137] M. Schweizer and J. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, Feb 2013.

- [138] D. Shmilovitz, "Application of duality for derivation of current converter topologies," *HAIT Journal of Science and Engineering B*, vol. 2, pp. 529–557, 2005.
- [139] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, "Voltage Balancing Approaches for Diode-Clamped Multilevel Converters Using Auxiliary Capacitor-Based Circuits," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2111–2124, May 2013.
- [140] A. Shukla, A. Ghosh, and A. Joshi, "Natural Balancing of Flying Capacitor Voltages in Multicell Inverter Under PD Carrier-Based PWM," *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1682–1693, Jun 2011.
- [141] R. Stala, "The Switch-Mode Flying-Capacitor DC-DC Converters With Improved Natural Balancing," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1369–1382, Apr 2010.
- [142] Stephen James Watkins, "Optimal Control of Multilevel Flying-Capacitor Converters," Ph.D. dissertation, The University of Leeds, 2005.
- [143] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Self-precharge for single-leg odd-level multilevel converter," in *Proceedings of the 5th IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Apr 2010, pp. 1–6.
- [144] L. M. Tolbert, F. Z. Peng, F. H. Khan, and S. Li, "Switching cells and their implications for power electronic circuits," in *Proceedings of the 6th International Power Electronics and Motion Control Conference (IPEMC)*, May 2009, pp. 773–779.
- [145] R. Turner, "Gradient Coil Design: A Review of Methods," *Magnetic Resonance Imaging*, vol. 11, pp. 903–920, 1993.
- [146] S. Utz, M. Stadler, and J. Pforr, "Active phase-shift control of multi-phase converters to minimize input current sub-harmonics," in *Proceedings of the 13th European Conference on Power Electronics and Applications (EPE)*, 2009, pp. 1–10.
- [147] R. Vaccaro, *Digital Control - A state-space approach*. McGraw-Hill, 1995.
- [148] J. van Emden, J. van Duivenbode, and J. Duarte, "Flying capacitor resonant pole inverter topology with reduced switch voltage stress," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–10.

- [149] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural Balance of Multicell Converters: The General Case," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1658–1666, Nov 2006.
- [150] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural Balance of Multicell Converters: The Two-Cell Case," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1649–1657, Nov 2006.
- [151] P. J. Wolfs, G. F. Ledwich, and K. C. Kwong, "The application of the duality principle to nonplanar circuits," *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 104–111, Apr 1993.
- [152] G. B. Yundt, "Series parallel connected composite amplifiers," Master's thesis, Massachusetts Institute of Technology. Dept. of Electrical Engineering and Computer Science., 1983.
- [153] G. B. Yundt, "Series- or Parallel-Connected Composite Amplifiers," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 1, pp. 48–54, Jan 1986.
- [154] L. Zhang and S. J. Watkins, "Capacitor voltage balancing in multilevel flying capacitor inverters by rule-based switching pattern selection," *IET Electric Power Applications*, vol. 1, no. 3, pp. 339–347, May 2007.
- [155] Y. Zhang, G. P. Adam, T. C. Lim, S. J. Finney, and B. W. Williams, "Hybrid Multilevel Converter: Capacitor Voltage Balancing Limits and its Extension," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 4, pp. 2063–2073, Nov 2013.
- [156] G. S. Zinoviev and N. N. Lopatkin, "Evolution of multilevel voltage source inverters," in *Proceedings of the 9th International Conference on Actual Problems of Electronic Instrument Engineering (APEIE)*, vol. 01, Sept 2008, pp. 125–136.

Dankwoord

Met het schrijven van het dankwoord komt een einde aan dit promotieonderzoek. Ik had dit werk zeer zeker nooit voor elkaar gekregen zonder de hulp en steun van anderen en dit is de plaats om hen daarvoor te bedanken.

Het begin van het promotietraject werd al gemaakt in 2010, in Wenen, waar ik samen met Ruud een stage deed bij AIT. Vanuit de vakgroep EPE kwam Korneel ons opzoeken, en bij het diner viel voor het eerst het woord promotieonderzoek. In eerste instantie wilde ik graag het bedrijfsleven in, maar twee weken kerstvakantie gaf mij de tijd om van mening te veranderen. Na deze vakantie had ik een gesprek met Elena, die mij in een twee uur durend gesprek definitief wist te overtuigen. Ik ben blij dat ik destijds die keuze heb gemaakt en het is daarom dat ik graag, op de eerste plaats, Elena wil bedanken voor de kans die ze mij gegeven heeft.

Na de buitenlandse stage begon de promotie niet meteen, omdat ik nog een afstudeeropdracht had te vervullen. Henk en Jorge werden wel al mijn begeleiders, omdat zij ook de toekomstige copromotoren zouden worden. Ik kan mij het eerste gesprek met Henk nog goed herinneren waarbij het van meet af aan ging over serie/parallel en interleaven. De toon was gezet, ook omdat we allebei muzikanten zijn. Van de vele discussies en meetings heb ik veel geleerd en zij hebben allebei een belangrijke stempel gedrukt op de totstandkoming van dit proefschrift. Bovendien vind ik het uitzonderlijk en geweldig dat zij in hun

vakantie, in respectievelijk Noorwegen en Brazilië, tijd vrij hebben gemaakt om het laatste nakijkwerk te verrichten en om het proefschrift verder te perfectioneren. Jorge en Henk, heel, heel erg bedankt!

Furthermore, I would like to thank the committee members prof. M.A.E. Andersen, P. Mattavelli, and E. Cantatore for reading the dissertation. I also would like to thank them for traveling to the Eindhoven University of Technology and for their participation in the committee. In het bijzonder wil ik het commissielid Jan Schellekens bedanken voor de voorgestelde correcties, alsmede voor het feit dat hij mij tijdens mijn afstudeeronderzoek en promotieonderzoek veelvuldig heeft ondersteund.

Het PowerDAC project werd mogelijk gemaakt dankzij financiering uit het THOR-project. Ik wil graag de projectleider van dit project, Mark van Helvoort, bedanken voor de samenwerking.

Verder wil ik ook graag alle collega's van de EPE vakgroep bedanken, in het bijzonder Nancy voor alle administratieve afhandelingen, de technische staf voor de assistentie in het lab, het zaalvoetbalteam "spielen und erleben" en Dave met wie ik veelvuldig ben gaan zwemmen voor de ontspanning in de pauze. Daarnaast wil ik de **TheBruceDickinson** productions bedanken voor het grafische ontwerp van dit proefschrift, alsook voor de gezellige avonden tijdens hun ALV. Tot slot wil ik de collega's met wie ik op een kamer heb gezeten, Bas, Nico, Gabriel, Erik, Sjef, Georgios, Baris, Mert, Ya en Jing bedanken voor de discussies, koffiepauzes en de speciaalbier avonden.

Naast werk heb je soms goede ideeën tijdens vrije tijdsbesteding, en om die reden zijn ook alle vrienden zonder dat ze het wisten belangrijk geweest. In het bijzonder wil ik Tom Schreurs bedanken, die tijdens het afronden van zijn eigen promotiewerk tijd heeft vrij gemaakt om hoofdstuk 2 na te lezen. Tevens wil ik Ruben Hekkens bedanken voor het ontwerpen van de omslag. Dit jaar heeft de organisatie van het LKZH door jonk geweld en de harmonie ook voor afleiding gezorgd. Op het moment van schrijven moet het LKZH nog gaan gebeuren, maar ik hoop dat we er met zijn allen een geweldig feest van gaan maken.

Tot slot wil ik mijn oma's en de hele familie bedanken, simpelweg omdat het de meest geweldige familie van het land is. Maar het aller- allerbelangrijkste voor mij zijn pap, mam, Rik en Yvon. Bedankt voor jullie liefde en support. Jullie hebben me altijd ondersteund en staan altijd voor me klaar.

About the author

Mark Caris was born in Heythuysen, the Netherlands, on the 24th of June in 1987. After finishing the Atheneum on SG Sint Ursula Horn in 2005, he started his bachelor and master studies in electrical engineering at Eindhoven University of Technology, the Netherlands.

During his master education he did an internship at the Austrian Institute of Technology (AIT) in Vienna, where he made a comparison between multilevel and full-bridge converters with respect to Eddy current losses in permanent magnets of synchronous machines. In 2011 he graduated on the investigation of imperfections in interleaved precision amplifiers, which resulted in a patent application.

In January 2012 he started this PhD research at the Eindhoven University of Technology in the group of Electromechanics and Power Electronics of which the results are presented in this dissertation. His research focused on advanced multi-level structures, modulation and control in the field of power electronics.

