A106nW 10 b 80 kS/s SAR ADC with duty-cycled reference generation in 65 nm CMOS

A 106 nW 10 b 80 kS/s SAR ADC With Duty-Cycled Reference Generation in 65 nm CMOS

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***Abstract*— This paper presents a 10 b 80 kS/s SAR ADC with low-power duty-cycled reference generation. It generates a stable reference voltage on chip for the SAR ADC and imparts very good immunity against power supply interference to the ADC. A 0.62 V-VDD 25 nW CMOS reference voltage generator (RVG) is presented, which has only ±1.5% variation over process corners. A duty-cycling technique is applied to enable 10% duty-cycling of the RVG, resulting in negligible power consumption of the RVG compared to that of the ADC. Furthermore, a bi-directional dynamic preamplifier is adopted in the SAR ADC, which consumes about half the power compared with a regular dynamic structure and maintains noise and gain performance. Compared with prior-art low-power ADCs, this work is the first to integrate the reference generation and include it in the power consumption while maintaining a competitive 2.4 fJ/conversion-step FoM. The chip is fabricated in 65 nm CMOS technology.**

***Index Terms*— CMOS, duty-cycle, dynamic comparator, reference voltage generator, SAR ADC.**

I. Introduction

AUTONOMOUS wireless sensor networks have been a prevailing research topic during the past few years. A wide range of promising applications could be realized based on these networks in areas like health care, security, logistics and so on. In these sensor networks, low-power, low-speed, moderate-resolution ADCs are usually needed to digitize the sensed signals. State-of-the-art SAR ADCs can accomplish this goal with very good power-efficiency (<10 fJ/conversion-step) [1]–[5]. At the same time, the reference voltage is very important for precise digitization of sensor information, but this aspect is usually ignored in low-power ADC publications where the VDD is typically used as reference. However, as the VDD is usually provided by a battery or energy harvesting, this results in an unstable reference. In addition, the ADC faces a lot of crosstalk noise from other circuit blocks through this shared VDD. Another solution for creating a reference voltage is to integrate a reference voltage generator (RVG) on chip. It can provide a stable, well-defined reference voltage with good PSRR. However, most existing low-power RVGs consume a power in the order of 32–200 nW [6]–[9], which is beyond the power needed for a power-efficient low-speed SAR ADC. Thus, this work introduces a duty-cycled RVG integrated with a low-power SAR ADC to obtain an overall solution that is power-efficient and accurate, independent of the external supply [10].

In terms of RVGs, bandgap reference (BGR) circuits are favorable for reference generation thanks to their high accuracy over process corners as the output reference voltage is determined by the bandgap voltage of silicon. For the conventional BGR [11], the output voltage is about 1.2 V and the power supply needs to be higher than 1.4 V, which makes this BGR impossible for low-VDD (< 1 V) applications. Several BGRs [6]–[8] are developed to operate at sub-1 V VDD, and their power consumption could be as low as 32 nW. As an alternative to BGRs, CMOS RVGs can more easily achieve sub-1 V VDD and low power operation. However, the output reference voltage of many CMOS RVGs [9], [12] highly depends on the absolute value of the MOSFET threshold voltage, which is sensitive to process variations. Though [13] claims that a DTMOST-based RVG could reduce this dependency by a factor of two, this advantage may become smaller with technology scaling as the back-gate tends to have less impact on the MOSFETs depletion region.

This paper presents a low-power low-VDD CMOS RVG based on the threshold voltage difference between normal- and high-V_t transistors, which is easier to control [14] compared with the absolute threshold voltage, thus leading to a more accurate reference over process corners.

The power consumption of an ADC scales down with its sampling frequency, but the power consumption of an RVG is static, which may be comparable or higher than that of a low-speed ADC. In order to reduce the RVG power consumption, a duty-cycling technique using a 3-stage S&H is applied, which overcomes the slow start-up of the RVG and achieves 10% duty-cycling.

For low-speed SAR ADCs, the power consumption of the DAC and the comparator dominates the total power consumption. The SAR ADC in this work adopts very small unit capacitors (250 aF) to save DAC power. Further, a bi-directional dynamic comparator makes use of both charging and discharging phases to perform amplification so that about half of the preamplifier power is saved.

This paper is organized as follows. Section II explains the architecture of the SAR ADC with duty-cycled reference

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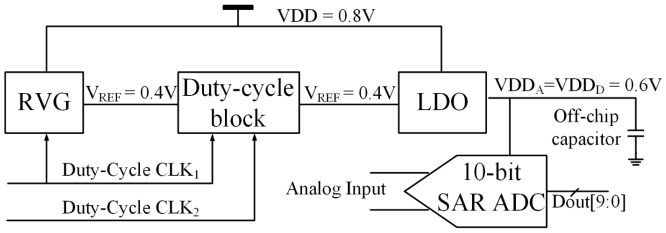

Fig. 1. Architecture of the SAR ADC with reference generation.

generation. Section III describes the details of the CMOS RVG. In Section IV, the duty-cycling technique is introduced. Section V shows the design of the LDO regulator driving the SAR ADC. The 10 b SAR ADC is depicted in Section VI, including the bi-directional comparator. Measurement results of both the stand-alone RVG and the SAR ADC with duty-cycled RVG are shown in Section VII, and Section VIII concludes this paper.

II. SAR ADC Architecture With Duty-Cycled Reference Generation

In order to meet the ADC requirements in wireless sensor networks, a moderate resolution (10 b), low-speed (80 kHz) SAR ADC is developed that operates at a minimum VDD of 0.6 V to save power. For an SAR ADC with reference generation, besides the RVG, an LDO is also needed to drive the SAR ADC. Due to the inevitable LDO dropout, which is in practice at least 200 mV, the power supply of the system is set to 0.8 V for the sake of low-power operation, requiring the RVG to operate at this low power supply while producing a controlled 0.6 V output voltage. For the consideration of power consumption, it is reasonable that the power consumption of the supporting blocks (RVG and LDO) is smaller than that of the main function (ADC). Thus, low-power low-VDD RVG and LDO blocks are required in this integrated system.

The SAR ADC with reference generation is shown in Fig. 1. It comprises an RVG, a 3-stage S&H for duty-cycling, an LDO and a SAR ADC. The system operates at one single external 0.8 V VDD. The RVG generates a 0.4 V reference voltage and is duty-cycled by CLK_1 to save power. With a 3-stage S&H block, a continuously stable reference voltage is provided to the LDO. The LDO then multiplies the reference voltage to 0.6 V and powers the SAR ADC. An off-chip capacitor is used to stabilize the LDO. The LDO is always-on to provide a stable supply and reference to the ADC during both tracking and conversion phases of the ADC.

III. Low-Power Low-VDD CMOS RVG

A. Process Characteristics of MOSFETs' Threshold Voltage

A perfect RVG needs to provide a reference voltage independent of process, power supply and temperature, of which process-independence is the most challenging as process variations are usually inevitable and there is not much to do about it from the aspect of circuit design. Hence, it is advantageous if an RVG can be based on a voltage unit from a well-defined physical mechanism, for example, a BGR based on

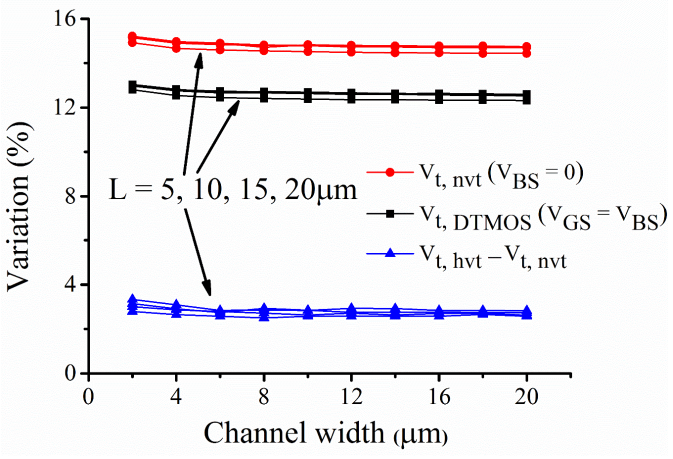

Fig. 2. Simulated variation of $V_{t,nvt}$, $V_{t,DTMOS}$ and ($V_{t,hvt}$– $V_{t,nvt}$) in 3 process corners.

the bandgap voltage of silicon. For CMOS design, an obvious voltage unit is the threshold voltage, which can be expressed as follows for a normal-V_t NMOS:

$$V_{t,nvt} = V_{FB} - \frac{Q_{SS}}{C_{OX}} + 2|\Phi_P| + \frac{|Q_d|}{C_{OX}} \quad (1)$$

where $V_{t,nvt}$ is the threshold voltage of a normal-V_t NMOS, V_{FB} is the flat-band voltage, Q_{SS} is the surface charge per unit area, C_{OX} is the gate-oxide capacitance, $2|\Phi_P|$ is the voltage required for strong conversion, and Q_d is the charge per unit area in the inversion layer [14]. In (1), every term is process-dependent, leading to a process-sensitive threshold voltage. As shown in Fig. 2, at three corners (typical, slow, fast), the simulated process variation divided by the average value is calculated to evaluate the effect of process variations for various transistor sizes. The $V_{t,nvt}$ varies about 15% in this particular 65 nm CMOS technology. For most CMOS RVG publications based on the absolute threshold voltage, measurements of multiple samples reveal smaller variation as those samples usually come from the same die and have the same process corner. However, for a robust design, an RVG should provide a stable reference voltage over different process corners. In [13], the authors claim that DTMOS (a MOS with the back-gate connected to the gate) could improve the threshold voltage stability over process corners by a factor of 2, but in the simulations based on the utilized 65 nm technology, the improvement is only about 20% (Fig. 2, $V_{t,DTMOS}$). In many modern CMOS technologies, the foundry provides transistors with a higher threshold voltage by applying an extra ion implantation step, while the oxide thickness remains the same. The threshold voltage shift due to this ion implantation can be expressed as

$$\Delta V_t = V_{t,hvt} - V_{t,nvt} = 2|\Delta\Phi_P| + \frac{\Delta|Q_d|}{C_{OX}} \quad (2)$$

where $V_{t,hvt}$ is the threshold voltage of the high-V_t NMOS. For a given implantation energy and a large t_{ox}, when t_{ox} decreases, there will be more ions implanted into the substrate, leading to a larger ΔV_t. However, when t_{ox} becomes sufficiently small and all the ions have penetrated into the substrate,

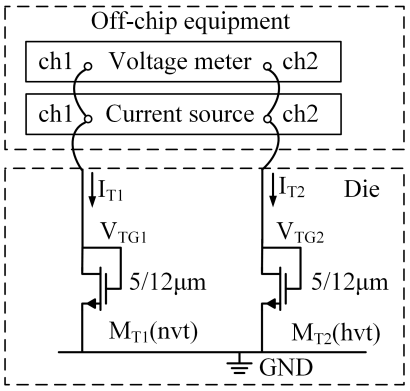

Fig. 3. Measurement setup for the test pair, creating a temperature-insensitive reference voltage ΔV_{TG}.

a further decreasing t_{ox} will result in a smaller ΔV_t. Thus, in the vicinity of a certain $t_{ox}$with certain implantation energy, the threshold voltage shift ΔV_t should be independent of t_{ox} [14], and thus becomes less sensitive to process variations. This is confirmed in the simulations based on the utilized 65 nm technology (Fig. 2, $V_{t,hvt}- V_{t,nvt}$). The ΔV_t varies only by 3%, which is a 5x process stability improvement compared to $V_{t,nvt}$. The above improvements are seen independent of sizing (W, L). To summarize, ΔV_t is a more suitable voltage unit for CMOS RVGs as it is much more stable over process corners compared to $V_{t,nvt}$ or $V_{t,DTMOS}$.

B. Temperature Characteristics of ΔV_t

In [15], the temperature dependency of ΔV_t is derived by calculating $\partial \Delta V_t/\partial T$. For a shallower implanted depth than the depletion edge, ΔV_t is CTAT (Complementary To Absolute Temperature). This CTAT effect was confirmed by measurements. The measurement setup is shown in Fig. 3. $M_{T1,T2}$ are normal-V_t and high-V_t transistors respectively, fabricated in 65 nm technology. They are diode-connected and biased in the subthreshold region. Large transistor sizes (W/L = 5 μm/12 μm) are chosen for both transistors as this is advantageous for matching and avoids short-channel and narrow-channel effects which will introduce a more complex temperature dependency.

When $V_{TG1,TG2} >> V_T$ (V_T is the thermal voltage), the current flowing in $M_{T1,T2}$ could simply be expressed as

$$I_d = \mu_n C_{OX} \frac{W}{L}(\eta - 1)V_T^2 \exp\left(\frac{V_{GS} - V_t}{\eta V_T}\right) \quad (3)$$

where μ_n is the carrier mobility, C_{OX} is the gate–oxide capacitance, W and L are the width and length of the transistor respectively, η is the subthreshold slope factor, V_T is the thermal voltage, V_{GS} is the gate–source voltage, and V_t is the threshold voltage [16]. Hence, the gate voltage difference of M_{T1} and M_{T2} could be expressed as

$$\Delta V_{TG} = V_{TG2} - V_{TG1} = \left(V_{t,hvt} - V_{t,nvt}\right) + \ln\left(\frac{I_{T2}}{I_{T1}} \cdot \frac{\mu_{n1}}{\mu_{n2}} \cdot \frac{C_{OX1}}{C_{OX2}} \cdot \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}\right) \cdot \eta V_T \quad (4)$$

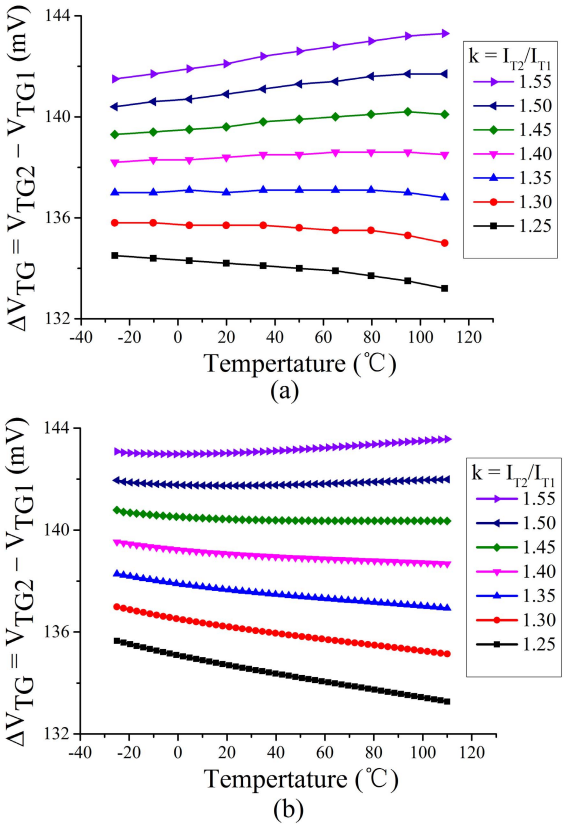

Fig. 4. (a) Measured and (b) simulated ΔV_{TG} of the test pair with different current ratios.

where the first term is CTAT and the second term is PTAT. By properly setting the current ratio k (I_{T2}/I_{T1}) of $M_{T1,T2}$, the TCs (Temperature Coefficient) of these two terms can cancel out each other, which makes ΔV_{TG} insensitive to temperature. In Fig. 3, two branches of current (I_{T1} = 8nA, $I_{T2} = k \cdot I_{T1}$) are pushed into the drains of $M_{T1,T2}$ and the gate voltages $V_{TG1,TG2}$ are measured with a different current ratio k from −25 °C to 110 °C [Fig. 4 (a)]. The measured results fit well with the simulations in Cadence [Fig. 4 (b)]. Corresponding to (4), with an increasing current ratio, the TC of ΔV_{TG} varies from negative to positive. By optimizing this ratio (e.g., 1.4 in this case), a temperature-insensitive ΔV_{TG}can be achieved.

C. CMOS RVG

Now that a temperature- and process-insensitive ΔV_G can be achieved according to the previous discussion, the next step is to generate a reference voltage relative to ground. The RVG core is shown in Fig. 5 (right-hand side). $M_{1,2}$ are normal-V_t and high-V_t transistors, respectively. They are diode-connected and operate in sub-threshold as the test pair. Since the size (11.2 μm/12 μm) of $M_{1,2}$ is different from the test pair, the optimized k (1.5) for a temperature-insensitive ΔV_G ($V_{G2}- V_{G1}$) is also slightly different. A negative feedback loop using an OPAMP forces V_P to equal V_{G2}, so that the voltage drop over resistor R_1 equals ΔV_G. By copying current I_1, a temperature-insensitive V_{REF}, which only depends on temperature-insensitive current and resistor ratios as well

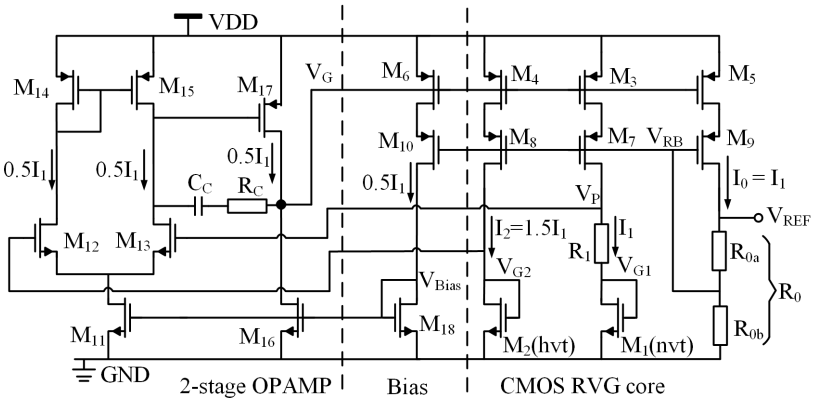

Fig. 5. CMOS RVG without duty-cycling.

as the temperature-insensitive ΔV_G is achieved as follows:

$$V_{REF} = I_0 \cdot R_0 = \frac{I_0}{I_1} \cdot \frac{R_0}{R_1} \cdot \Delta V_G \tag{5}$$

where R_0 equals the sum of R_{0a} and R_{0b}. Since V_{REF} is temperature-insensitive while V_P is CTAT as V_P tracks the CTAT threshold voltage, the accuracy of a single-transistor current copy will be dramatically affected by the drain-source voltage, introducing a complex TC to V_{REF}. Hence, as shown in Fig. 5, a cascode structure is chosen here to achieve an accurately copied current. The transistors comprising the cascode structure operate in the sub-threshold region and the drain-source voltage is designed to be larger than 100 mV to diminish channel length modulation effects. V_G is generated by the feedback loop and V_{RB} is a fraction of V_{REF} so the cascode structure does not consume too much voltage headroom, making it compatible with low-VDD operation.

The OPAMP composing the negative feedback is shown in Fig. 5 (left-hand side). It consists of two stages whose gain is large enough to guarantee V_P is close enough to V_{G2}. RC-miller compensation is adopted to make sure the stability of the negative feedback loop. The bias for the OPAMP is generated by a copy of current I_1, which is approximately expressed as $\Delta V_G/R_1$.

D. Minimum VDD

From Fig. 5, it is easy to observe that the minimum operational VDD for the RVG core is

$$VDD_{min,core} = V_{G2} + V_{DS4} + V_{DS8} \tag{6}$$

where V_{G2} is the gate voltage of M_2 and $V_{DS4,8}$ are the drain–source voltage drop of $M_{4,8}$ respectively. Similarly, the minimum operational VDD for the OPAMP is

$$VDD_{min,OPAMP} = V_{SG14} + V_{DS12} + V_{DS11} \tag{7}$$

where V_{SG14} is the source–gate voltage of M_{14}, and $V_{DS11,12}$ are the drain–source voltage drop of $M_{11,12}$ respectively. The minimum power supply of the RVG is determined by the smaller of (6) and (7). Due to the subthreshold operation of $M_{2,14}$, voltages V_{G2} and V_{SG14} are smaller than the absolute threshold voltage value of $M_{2,14}$. $V_{DS4,8,11,12}$ need to be at least about 100 mV. The simulated minimum VDD is about 720 mV among 5 process corners from −25 °C to 110 °C, which means this RVG is suitable for sensor networks and other sub-1 V systems.

E. Power Consumption

From Fig. 5, it is found that the power consumption of this RVG is proportional to I_1. In order to suppress the power consumption, a large R_1 is required at the expense of chip area. On the other hand, current I_1 must force $M_{1,2}$ to operate in the subthreshold region and be large enough to make (3) valid. As a tradeoff between chip area, temperature performance and power consumption, R_1 is set to 17 MΩ and R_0 is set to 48.5 MΩ, leading to I_1 of 8.25 nA. The simulated power consumption of the RVG at 0.8 V VDD is about 40 nW. Since ΔV_G changes little with process, power supply and temperature, the current consumption of the RVG is also stable over PVT corners.

F. Process Stability

The complete RVG is also simulated at different corners (Fig. 6). The simulated V_{REF} varies about only ±1.5% (3% variation range) over five corners, well corresponding to the threshold voltage simulations in Section III-A. This implies that the presented threshold voltage difference-based RVG reveals much better process stability than absolute threshold voltage-based RVGs.

IV. Duty-Cycling Technique

A. Duty-Cycling and Start-up of the RVG

As discussed in Section II, the RVG will be duty-cycled in order to save power, which means the RVG should be switched on and off while VDD remains on. Switch transistors are inserted in each branch between PMOS and NMOS as shown in Fig. 7. While not shown in the figure, the current paths in the OPAMP are disabled in a similar way. To boost duty-cycling speed, voltages V_G and V_{Bias} should be restored quickly. To do so, two switched capacitors $C_{S1,S2}$ are placed at these nodes to save and restore their levels when the RVG is duty-cycled.

Besides this duty-cycling technique, the RVG also needs a start-up circuit to guarantee correct start-up of the circuit

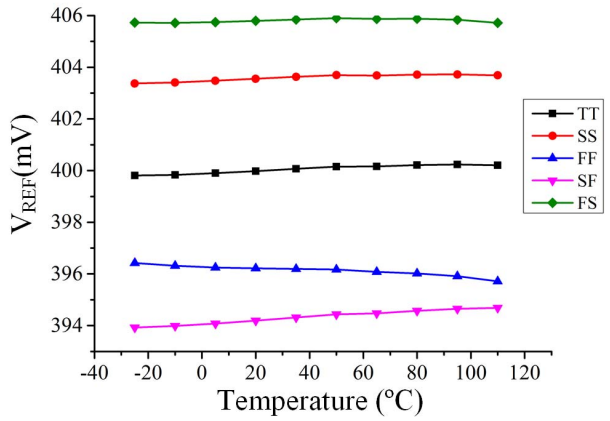

Fig. 6. Simulated V_{REF} in 5 process corners.

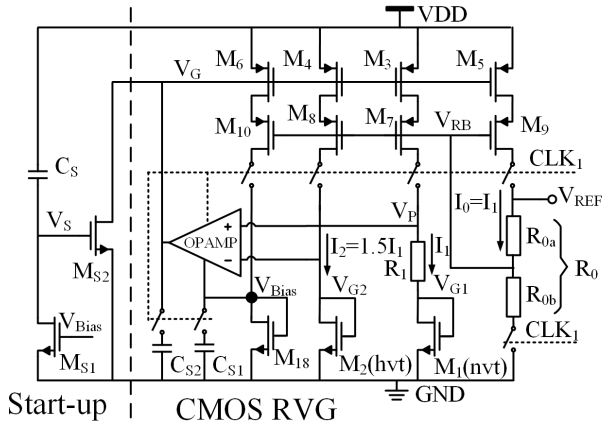

Fig. 7. RVG with start-up circuit and duty-cycling switches.

when VDD is switched on for the very first time. The start-up circuit is shown in Fig. 7. Assuming the duty-cycling switches are on, the moment VDD is switched on, V_S will jump to a high voltage level due to C_S being discharged prior to this moment, and thus open transistor M_{S2}. V_G is then discharged and $M_{3\sim6}$ are switched on gradually, enabling current flow and functionality of the circuit. As soon as V_{Bias} rises sufficiently, M_{S1} will pull V_S to ground to switch off M_{S2} and disable the start-up circuit. The RVG core takes over and will settle to the proper operation state. The start-up time is approximately 1.5 ms. In case the duty-cycling switches are not on (or already duty-cycled) during the moment VDD is switched on, correct start-up is still ensured, but the initial start-up will take longer due to the duty-cycled operation.

B. One-Stage Sample-and-Hold

As discussed in Section II, even though the RVG is duty-cycled, a continuously stable reference voltage is required for the LDO as it is switched on all of the time. A one-stage S&H could be adopted to sample and hold the reference voltage of the RVG as shown in Fig. 8. The RVG and the switched capacitor network (S_A, C_A) are controlled by the same clock CLK_1 and voltage V_A is provided to the LDO. This scheme suffers from two problems. The moment CLK_1 switches the RVG and S_A on, V_A would experience a large start-up ripple

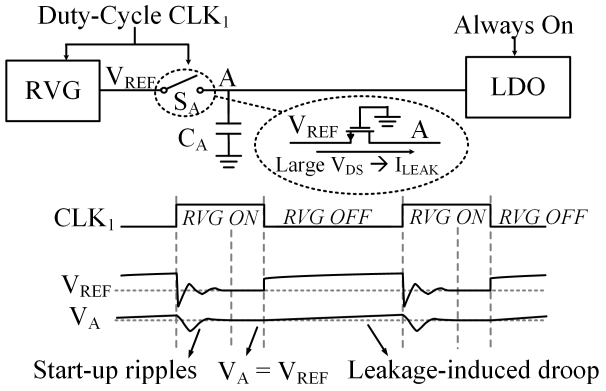

Fig. 8. Architecture and waveforms of a one-stage S&H.

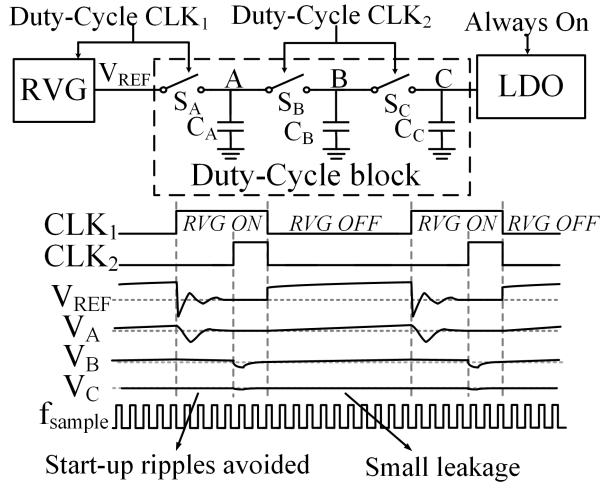

Fig. 9. Architecture and waveforms of a three-stage S&H.

of V_{REF}, the output of the RVG. When RVG and S_A are switched off and C_A begins to hold the sampled voltage, due to the voltage drop over NMOS switch S_A, there will be leakage through S_A causing droop of V_A. As a result, voltage V_A is neither stable nor accurate for most of the time, which will cause performance loss of the SAR ADC compared to operation with a non-duty-cycled RVG.

C. Three-Stage Dual-Clock Sample-and-Hold

To solve the above problems, a three-stage dual-clock S&H is presented as shown in Fig. 9. Compared with Fig. 8, two more switched capacitors controlled by CLK_2 are inserted between node A and the LDO. CLK_1 and CLK_2 have the same frequency but different pulse widths. CLK_1 switches the RVG and S_A on simultaneously as before, thus V_A will be stable after some start-up time. At that time, CLK_2 switches S_B and S_C on, so that voltage V_B and V_C are refreshed from the stable V_A. In this way, V_C is isolated from the start-up behavior of the RVG. Subsequently, CLK_1 and CLK_2 switch the RVG and $S_{A,B,C}$ off simultaneously and the hold phase starts. As before, the leakage through S_A causes an unstable V_A. However, the voltage drop over S_B is smaller than that of S_A leading to smaller leakage from node B

because the leakage of a MOS switch is proportional to the voltage drop between drain and source. Furthermore, the voltage drop over S_C is again smaller than that of S_B so that the leakage from node C becomes very small. As a result, a very stable V_C is achieved during the entire clock period, and the simulated maximum ripple is merely 0.1 mV. Considering the target application is a 10 b SAR ADC with an LSB step of approximately 1 mV, this ripple of 0.1 mV is acceptable. The above discussion indicates that a too high or too low V_{REF} will either make the leakage in the S&H switches too high, or will increase the RC time, which would slow down the settling time and thus degrade the duty-cycling speed. As a result, a V_{REF} of 400 mV is chosen here.

The performance requirements for node A, B and C are different as it is more important to start-up fast at node A and B than to leak slightly, while small leakage is more important to enable longer hold time and better stability at node C. However, a small C_B will lead to a large leakage at node B and increase the leakage on C_C subsequently. Consequently, the value of $C_{A,B,C}$ is set to 12.5 pF, 25 pF and 50 pF respectively. S_A is set to about 5 times the size of $S_{B,C}$ and $S_{B,C}$ have the same size.

In this work, the duty-cycle clocks CLK_1 and CLK_2 are generated externally from an FPGA. The frequency is 20 Hz and the pulse widths are 5 ms and 2.5 ms respectively. This frequency is determined by the maximum hold time the duty-cycling could achieve plus the start-up time and refresh time needed. Because of the low frequency of operation and the insensitivity to the exact timing, they could be generated on chip with little power consumption. According to simulations, this logic would consume only 2 nW and occupy only 50 μm x 12 μm.

V. Low Dropout Regulator

Since the V_{REF} generated by the RVG is small ($\sim$ 0.4 V) without driving capability, an LDO regulator is required to multiply the V_{REF} to 0.6 V and drive the SAR ADC. For an N-bit SAR ADC, it usually takes N comparison and DAC switching cycles for each conversion, which puts forward strict requirements for the LDOs as they have to respond fast enough to settle the DAC outputs at more than N times the sampling frequency. As a result, the power consumption of the LDOs (or buffers) is usually several times or even more than 10 times higher than that of ADCs [17], [18].

In this work, we adopt an off-chip capacitor (10 μF) to ease the strict response and power consumption requirements for the LDO. The SAR ADC in this work is primarily using dynamic circuits, which have little static power but require large current peaks once in a while. Since the feedback loop of the LDO is too slow to respond to this load change, the off-chip capacitor will provide those current peaks with slight voltage drop. As a result, the LDO only needs to provide a nearly constant current equal to the average current consumption of the SAR ADC.

As shown in Fig. 10, the reference voltage V_C of the LDO is taken from C_C (Fig. 9). A 2-stage OPAMP is utilized to achieve high loop gain. Since the impedance at the output of the LDO is very high, the resulting main pole locates at a very low frequency so no extra compensation is needed here to guarantee the loop stability. As discussed previously, the LDO is always-on, which requires an always-on bias voltage for $M_{19,25}$. Looking back at Fig. 7, V_{Bias} is duty-cycled and C_{S1} stores the voltage of V_{Bias} to make the rebuilding faster. Similar to the duty-cycling block, another S&H (C_{SB}) controlled by CLK_2 is inserted to generate continuous biasing voltage for $M_{19,25}$. The current consumption of the LDO is $1.35I_1$.

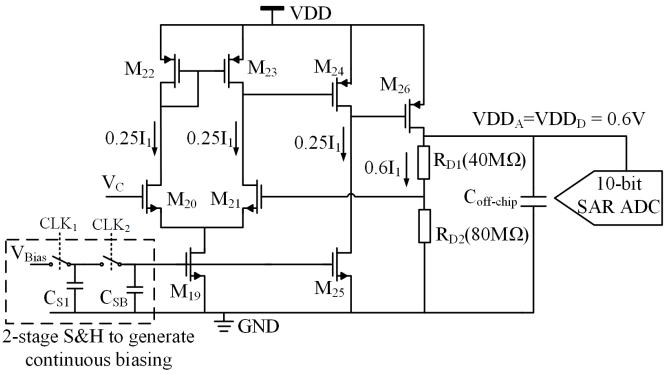

Fig. 10. LDO with continuous biasing generation.

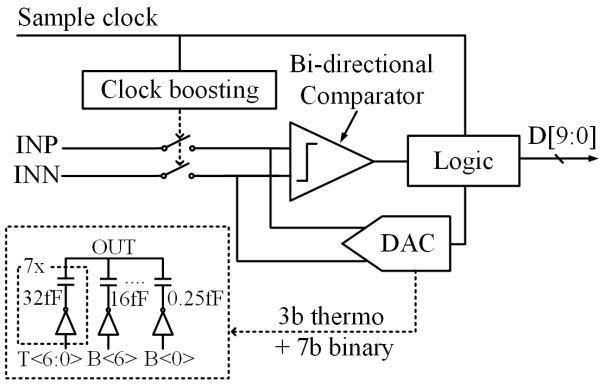

Fig. 11. Architecture of the 10 b SAR ADC.

VI. SAR ADC With Low-Power Bi-Directional Dynamic Comparator

The 10 b asynchronous SAR ADC is shown in Fig. 11. The clock for the logic is generated internally as in [4] hence only the sample clock is required externally. The DAC is segmented into three thermal encoded MSBs and Seven binary encoded LSBs, reducing power consumption and avoiding large MSB errors. Lateral metal-metal capacitors [20] are adopted to implement the DAC and the total capacitance is 256 fF for high power-efficiency. The power-efficiency of the SAR ADC is further improved by a low-power bi-directional dynamic comparator.

A. Typical Dynamic Comparator With Integration-Based Preamplifier

The schematic and operation of a typical dynamic comparator [19] are shown in Fig. 12. It comprises an integration-based preamplifier and a latch. During the reset phase, the

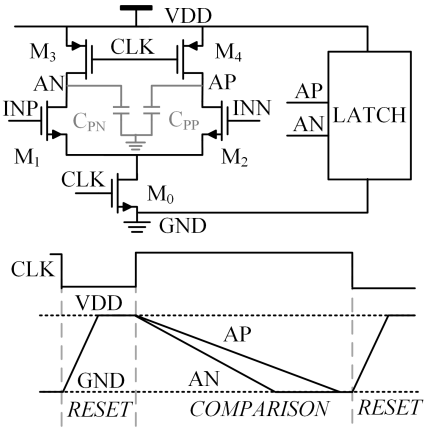

Fig. 12. Prior-art dynamic comparator [19] and waveforms of key nodes.

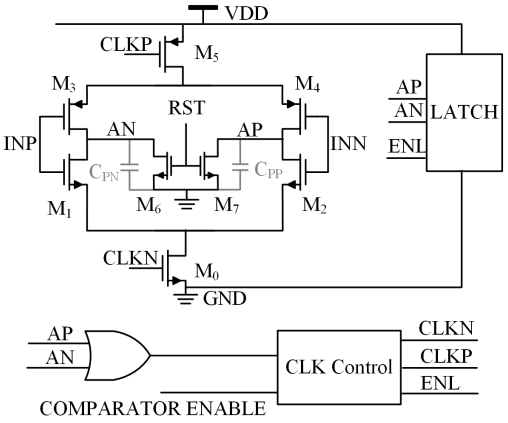

Fig. 13. Bi-directional dynamic comparator.

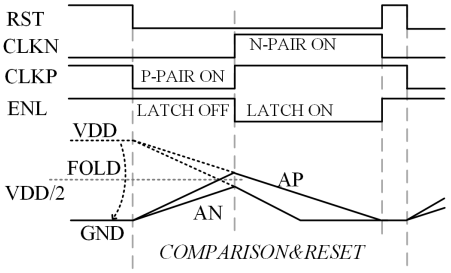

Fig. 14. Key nodes waveforms of the bi-directional dynamic comparator.

parasitic capacitors $C_{PP,\ PN}$ are charged to VDD by $M_{4,3}$. The comparison starts when CLK goes high. $C_{PP,\ PN}$ are discharged through input pair $M_{2,1}$ and $V_{AP,AN}$ will drop according to the input voltages $V_{INP,\ INN}$. In time, the common mode of $V_{AP,AN}$ is gradually decreasing while the differential input signal is gradually amplified. When the common mode of $V_{AP,AN}$ reaches the threshold of the latch, the latch will take over and output the comparison result. Next, CLK will go low and the pre-amplifier and latch are reset to their initial conditions. Thanks to the amplification of the preamplifier, the noise and power efficiency of the overall comparator are dominated by the preamplifier. The equivalent input noise of this preamplifier equals [19]

$$\sigma_v \approx k \cdot T \cdot \sqrt{\frac{8}{q}} \cdot \frac{1}{\sqrt{\left|C_{PP} \cdot (V_{thlatch} - V_{DD})\right|}} \sim \frac{1}{\sqrt{Q_C}} \quad (8)$$

where $V_{thlatch}$ is the threshold voltage of the latch and Q_C represents the absolute value of average transferred charge on parasitic capacitor $C_{PP,PN}$ before the latch takes over. The preamplifier energy dissipation of one comparison equals

$$E_C = 2 \cdot C_{PP} \cdot V_{DD}^2. \quad (9)$$

From (8) and (9), the tradeoff between noise and energy consumption can be observed. For fixed V_{DD} and $V_{thlatch}$, the equivalent input noise of the preamplifier is proportional to $(C_{PP})^{-0.5}$, while the energy consumption is proportional to C_{PP}. If one wishes to reduce the noise by a factor of 2, the consumed energy has to be quadrupled.

B. Bi-Directional Dynamic Comparator

When reflecting on the operation of the dynamic comparator (Fig. 12), one can note that the discharging slope of $C_{PP,PN}$ is used to perform dynamic amplification. On the other hand, the charging slope of $C_{PP,PN}$ is not used for amplification, but only to reset the comparator. The bi-directional preamplifier takes advantage of both slopes to perform amplification and can thus improve the power-efficiency by a factor of two.

As shown in Figs. 13 and 14, a PMOS input stage $M_{3,4}$ is inserted in parallel with NMOS pair $M_{1,2}$. Before the comparison starts, $V_{AP,AN}$ are pushed to ground by $M_{6,7}$. Then, the PMOS input pair $M_{3,4}$ is enabled first by switching on tail transistor M_5. $C_{PP,\ PN}$ are charged and $V_{AP,AN}$ increase according to the input signal. An OR gate is utilized to detect when V_{AP} or V_{AN} reaches half VDD. At that point, the PMOS pair $M_{3,4}$ is disabled by switching off M_5 while M_0 is switched on to enable NMOS pair $M_{1,2}$ together with the latch. From this moment onwards, this bi-directional comparator operates as the typical structure and achieves the same gain (see Fig. 14). A further advantage of this comparator is that $V_{AP,AN}$ return inherently to their initial condition (GND) at the end of the comparison, which avoids a reset cycle. An RST signal is still present to avoid floating $V_{AP,AN}$ between cycles. For this bi-directional preamplifier, the sum of absolute value of average transferred charge on $C_{PP,PN}$ during charging and discharging is

$$\begin{aligned} Q_{CB} &= \left|C_{PP} \cdot \left(\frac{V_{DD}}{2} - 0\right)\right| + \left|C_{PP} \cdot \left(V_{thlatch} - \frac{V_{DD}}{2}\right)\right| \\ &= C_{PP} \cdot (V_{DD} - V_{thlatch}) = Q_C \end{aligned} \quad (10)$$

which means that with the same $C_{PP,PN}$, the bi-directional preamplifier has the same noise performance as the typical structure. However, as $C_{PP,PN}$ are only charged to one-half VDD rather than VDD, the energy consumption of the bi-directional preamplifier is

$$E_B = 2 \cdot C_{PP} \cdot \frac{V_{DD}}{2} \cdot V_{DD} = C_{PP} \cdot V_{DD}^2 \quad (11)$$

which is only half of (9). Note that the threshold of the OR gate does not have to be very precise as it only changes the noise

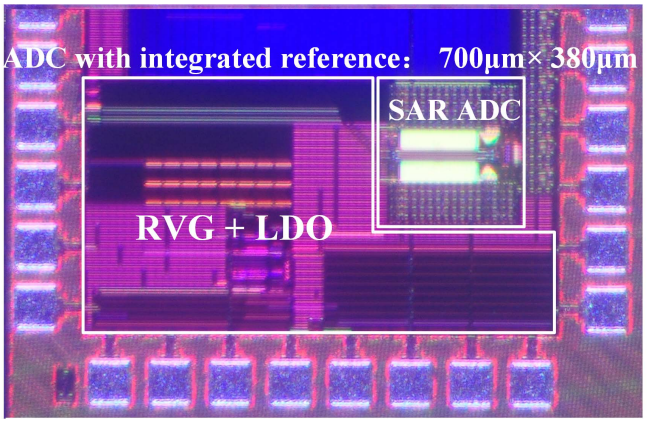

Fig. 15. Die photograph in 65 nm CMOS technology.

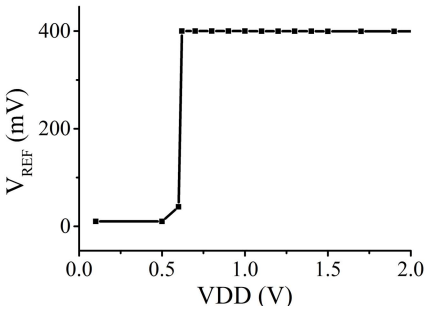

Fig. 16. Measured output reference voltage of the RVG versus power supply.

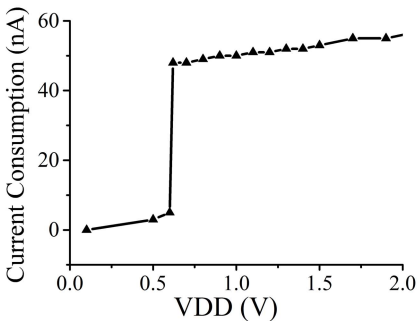

Fig. 17. Measured current consumption of the RVG versus power supply.

performance and consumption slightly. For the whole dynamic comparator, the power consumption ratio of preamplifier and latch is about 3:1, which suggests this bi-directional comparator saves about 37.5% of the power of the typical comparator. In practice, the additional logic causes 4.5% overhead, which is mostly due to short-circuit current in the OR gate, thus saving 33% overall.

VII. Measurement Results

The SAR ADC with duty-cycled reference generation was implemented in a 65 nm CMOS technology and occupies 0.266 mm^2 due to the large resistors used in the RVG and LDO (Fig. 15). First, a stand-alone RVG is measured without duty-cycling. Then, the measurements of the SAR ADC with duty-cycled reference generation are shown.

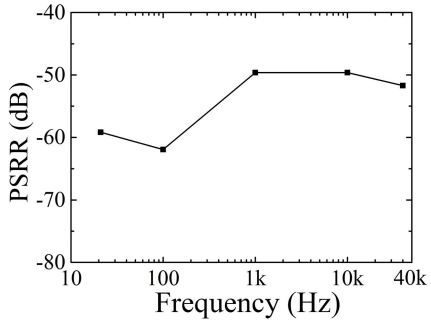

Fig. 18. Measured PSRR of the RVG.

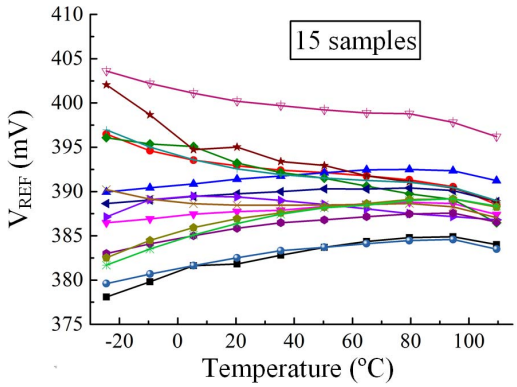

Fig. 19. Measured temperature dependency of 15 samples.

A. Stand-Alone RVG

A total of 15 RVG samples was measured. They all begin to operate from a minimum VDD between 0.60 ~ 0.62 V. A sample with 0.62 V minimum VDD is selected for the measurements shown here. Figs. 16 and 17 display the V_{REF} and current consumption as function of VDD. From 0.62 V to 2.0 V, the line sensitivity is 0.07%/V. At 0.8 V VDD, the measured power consumption is only 38 nW. At the minimum supply of 0.62 V, the measured power consumption is 25 nW. The PSRR is measured by measuring the transfer from a tone at VDD to the output of the RVG. The measured PSRR of the RVG is better than −49 dB up to near Nyquist frequency as shown in Fig. 18. The temperature dependency of the 15 samples is shown in Fig. 19. From −25 °C to 110 °C, the TCs vary from 44 to 248 ppm/°C with an average TC of 108 ppm/°C. At 25 °C, the average output reference voltage is 389.9 mV with a 4.0 mV standard deviation. According to Monte-Carlo simulations, the dominant reason for part-to-part variation is mismatch in the OPAMP and the current mirror $M_{3-5,7-9}$. Table I compares this RVG with other low power CMOS and BJT RVGs. After applying duty-cycling, this RVG consumes lower power. Besides, the sample-to-sample variation is comparable to BJT RVGs and substantially better than V_t-based CMOS RVGs. Further, the PSRR at 100 Hz is equal or better than other listed work.

B. SAR ADC With Duty-Cycled Reference Generation

The power breakdown and ENOB of the reference-included ADC (operating at 80 kS/s) with different duty-cycling rates are shown in Figs. 20 and 21. At 10% duty-cycle of the RVG, the power consumption of the RVG is 3.7 nW from

TABLE I
RVG PERFORMANCE SUMMARY AND COMPARISON

		[6]	[7]	[8]	[9]	[12]	This work
Type		BJT	BJT	BJT	V_t	V_t	ΔV_t
VDD_{min}		0.75	0.7	0.5	0.9	0.45	0.62
Area (mm^2)		0.070	0.025	0.026	0.045	0.043	0.077
TC (ppm/°C) [T range (°C)]		40 [-20:85]	114 [-40:120]	75 [0:100]	10 [0:80]	165 [0:125]	108 [-25:110]
Power(nW)	w/o DC	170	52.5	32	36	2.6	25
	with DC	-	-	-	-	-	2.5
Sample-to-sample V_{REF} variation: σ/μ (%)		1.0	1.05	0.67	3.1	3.9	1.0
Line sensitivity (%/V)		0.005	-	-	0.27	0.44	0.07
PSRR @100Hz (dB)		-	-62	-	-47	-45	-62

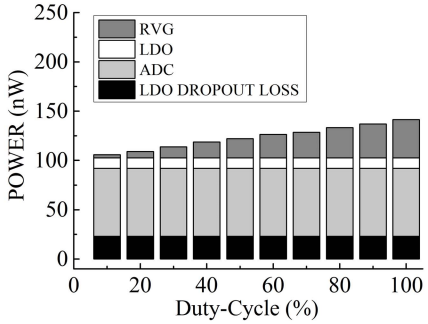

Fig. 20. Measured power breakdown of the reference-included 10 b ADC at 80 kS/s versus different duty-cycling rates.

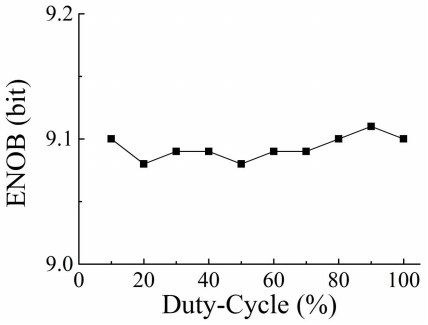

Fig. 21. Measured near-Nyquist ENOB of the reference-included 10 b ADC at 80 kS/s versus different duty-cycling rates.

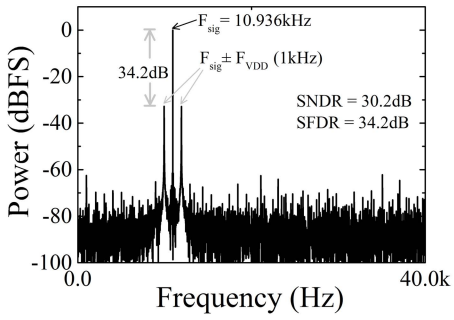

Fig. 22. Measured spectrum of the ADC powered by external power supply (0.6 V) imposed with 1 kHz 150 mVPP interference.

0.8 V supply, which is far less than that of the ADC core. Meanwhile, the ENOB (measured near Nyquist at 80 kS/s) remains 9.1 bit regardless of the duty-cycling, resulting in a

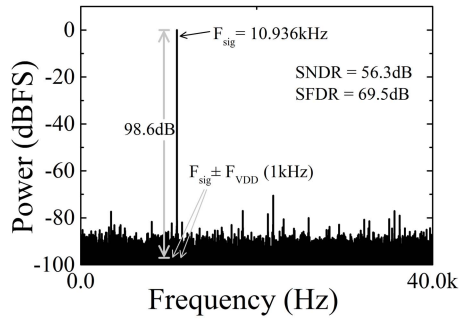

Fig. 23. Measured spectrum of the ADC powered by a 10% duty-cycled RVG and LDO with 1 kHz 150 mVPP interference imposed on the external power supply (0.8 V).

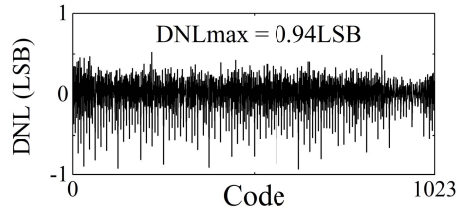

Fig. 24. Measured DNL of the ADC with 10% duty-cycled RVG.

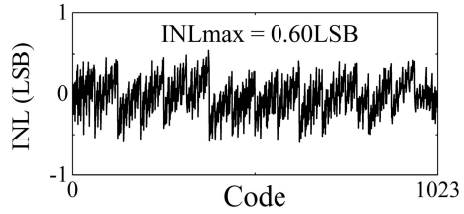

Fig. 25. Measured INL of the ADC with 10% duty-cycled RVG.

FoM of 2.4 fJ/conversion-step. Note that since the LDO is always-on, the power consumption and the inevitable dropout loss due to the voltage drop between power supply and output of the LDO takes about 1/3 of the total power consumption. In order to demonstrate the PSRR of the whole system, the ADC is measured with an intentional interference imposed on the external power supply while all decoupling capacitors are removed. First, the ADC without RVG/LDO powered by external power supply (0.6 V) imposed with 1 kHz 150 mV_{PP} interference is measured, where the input signal is modulated by the interference and two large spurs at $F_{sig} \pm F_{VDD}$ are observed (Fig. 22). Along with other noise from the external power supply, the ADC achieves a poor SNDR (30.2 dB) and SFDR (34.2 dB). Fig. 23 displays the spectrum of the ADC powered by a 10% duty-cycled RVG and LDO with the same interference imposed on the external power supply (0.8 V), which reveals 64.4 dB suppression on the intermodulation spurs at $F_{sig} \pm F_{VDD}$ and better noise suppression. The achieved SNDR and SFDR are the same as the case with an ideal clean supply powering the ADC directly. With 10% duty-cycling, other performances of the SAR ADC are also measured. The maximum DNL is 0.94 LSB (Fig. 24) and the maximum INL is 0.60 LSB (Fig. 25). At near Nyquist input, the SNDR

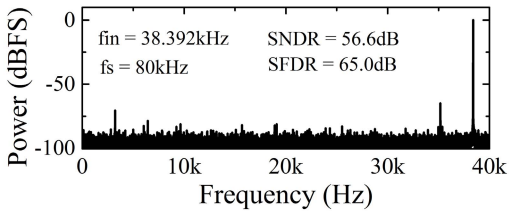

Fig. 26. Measured spectrum of the ADC with 10% duty-cycled RVG.

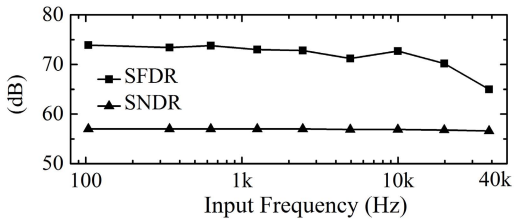

Fig. 27. Measured SFDR and SNDR of the ADC with 10% duty-cycled RVG versus input frequency.

TABLE II
SAR ADC PERFORMANCE SUMMARY AND COMPARISON

	[1]	[2]	[3]	[4]	[5]	This work
Technology (nm)	90	40	90	65	65	65
Resolution (bit)	10	10	10	10	10	10
Supply voltage (V)	0.4	0.45	0.4	0.6	0.6	0.8
Sample rate (S/s)	250k	200k	500k	40k	100k	80k
Area (mm²)	0.04	0.065	0.042	0.076	0.053	0.26
INL (LSB)	0.67	0.45	0.62	0.48	0.87	0.60
DNL (LSB)	0.43	0.44	0.34	0.32	0.96	0.94
Power (μW)	0.2	0.084	0.5	0.072	0.088	0.106
Including reference	No	No	No	No	No	Yes
ENOB (bit)	8.6	8.95	8.72	9.4	9.2	9.1
FoM (fJ/conv.-step)	2.02	0.85	2.47	2.7	1.5	2.4

is 56.6 dB and the SFDR is 65.0 dB (Fig. 26). The SFDR and SNDR versus input frequency are shown in Fig. 27. While the SFDR slowly degrades due to the T&H, the SNDR is maintained at a constant level. Compared with other low-power SAR ADCs (Table II), this work is the only one to integrate the reference generator and LDO with an ADC. Meanwhile, it has a comparable ENOB and FoM.

VIII. CONCLUSION

In this work, a 10 b SAR ADC with duty-cycled reference generation is implemented, which has an accurate reference voltage over PVT corners and good immunity against power supply interference at the expense of little power consumption. The low-VDD low-power CMOS RVG is based on the threshold voltage difference of normal- and high-V_t transistors, which has at least 4x better process stability than the absolute threshold voltage of a single transistor and DTMOS, resulting in a more robust CMOS RVG. Thanks to the sub-threshold operation, this CMOS RVG operates at a minimum power supply of 0.62 V at room temperature and consumes 25 nW, which is suitable for low-VDD low-power systems. Besides, this CMOS RVG also reveals good temperature and power supply independence. The power consumption of the RVG is further reduced with a 3-stage dual-clock S&H duty-cycling block. Dual-clock control protects the output from the start-up behavior of the RVG and the multi-stage structure diminishes the leakage, enabling 10% duty-cycling of the RVG. A low-power bi-directional dynamic comparator is adopted in the SAR ADC, which makes use of both charging and discharging to perform the pre-amplification, resulting in high power-efficiency. Compared to a typical comparator [19], this bi-directional comparator reduces the power by 33% including the power of extra logic circuits while maintaining the same noise performance. With the above techniques, the reference-included SAR ADC achieves a FoM of 2.4 fJ/conversion-step.

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