Integrated millimeter-wave broadband phased array receiver frontend in silicon technology

Integrated Millimeter-Wave Broadband Phased Array Receiver Frontend in Silicon Technology

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op donderdag 9 juni 2016 om 16.00 uur

door

Qian Ma

geboren te Xinjiang, China

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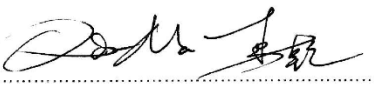

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List of Abbreviations

BW	Bandwidth
(Bi)CMOS	(Bipolar) Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CB	Common Base
CC	Common Collector
CE	Common Emitter
CF-LNA	Current Feedback Low Noise Amplifier
CPW	Co-Planar Waveguide
DSB	Double-Side-Band
DTI	Deep Trench Isolation
DV	Delay Variation
DUT	Device Under Test
EM	Electromagnetic
FE	Front-End
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GSG	Ground-Signal-Ground
GSSG	Ground-Signal-Signal-Ground
HBT	Heterojunction bipolar transistor
IC	Integrated Circuits
ICP1dB	Input 1dB Compression Point
IF	Intermediate Frequency
IIP3	Third Order Input Intercept Point
LC	Inductor and Capacitor
LMDS	Local Multipoint Distribution Service
LNA	Low-Noise-Amplifier
LO	Local Oscillator
LP	Low Power
LPF	Low Pass Filter
LSB	Least Significant Bit
LV	Low Voltage
HP	High Power
HV	High Voltage
HG	High Gain

MEMS	Micro-Electro-Mechanical Systems
MIM	Metal-Insulator-Metal
Mm-Wave	Millimeter-Wave
NDV	Normalized Delay Variation
NF	Noise Figure
NFmin	Minimum Noise Figure
P2P	Point-to-Point
PA	Power Amplifier
PS	Phase Shifter
RC	Resistor and Capacitor
RF	Radio Frequency
RMS	Root Mean Square
RX	Receiver
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SOI	Silicon-On-Insulator
SOL	Short, Open, and Load
SPI	Serial Peripheral Interface
SSB	Single-Side-Band
TL	Transmission Line
TTD	True Time Delay
TX	Transmitter
UWB	Ultra-Wide-Band
VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer
VSAT	Very-Small-Aperture Terminal

1. Introduction

1.1. Background and Motivation

The investigation of high-speed radio-frequency (RF) transceivers becomes popular nowadays due to the increasing need for high-speed wireless data transfer. These transceivers support multi-Gbps data rate which enables high-speed communication and high-resolution radar applications. Based on the Shannon–Hartley's information theorem [1], one effective way to improve data rate (or throughput) is to increase the signal bandwidth. Inherently, millimeter wave (mm-wave) frequencies offer larger available signal bandwidth and are therefore attractive for high-speed transceivers. However, the high path loss of mm-wave frequencies requires a transmitter (Tx) with high output power and a receiver (Rx) with high sensitivity; both are challenging in mm-wave frequency circuit design. One effective way to compensate high path loss and improve the signal to noise ratio (SNR) is to employ phased array techniques.

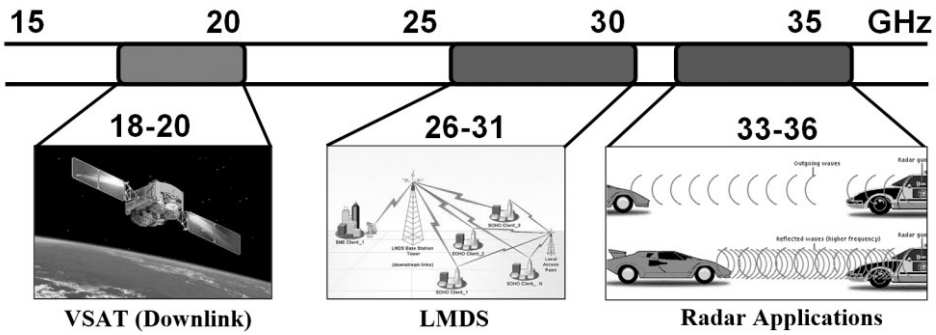


Figure 1-1. Spectrum of main Ka-band applications

The Ka-band usually refers to the frequency range from 26GHz to 40GHz. As shown in Figure 1-1, typical Ka-band applications are downlink of VSAT[1] (Very-Small-Aperture-Terminal), LMDS (Local Multipoint Distribution Service), and radar applications, i.e. military radar and traffic radar for speed detection. Moreover, the P2P (Point-to-Point communication) applications with distributed bands from 9GHz up to 40GHz partly locate at the Ka-band as well, e.g. the wireless backhaul of base stations in cellular communication. Driven by the high-performance requirements, the market for these applications is still dominated by III-V compound technologies such as GaAs (Gallium arsenide), etc. Compared to the silicon-based technologies, these compound solutions have lower integration level thus have a higher cost. Meanwhile, the continuous downscaling of silicon-based technologies, i.e. CMOS (Complementary Metal–Oxide–Semiconductor) and BiCMOS (with also bipolar junction transistors), has enabled to realize mm-wave integrated circuits (IC) in silicon using devices with f_T > 200GHz, and minimum noise figures (NF_{min}) of less than 1.5dB [2]. Therefore, an interesting research topic is how to realize these Ka-band RF ICs with competitive performance using the silicon-based technology, which will reduce the cost and increase integrated functionality.

To further improve the integration capability and reduce the cost, a generic RF transceiver can be used to cover multi-bands from one application or cover multi-applications. For instance, a single wideband receiver can be used to receive the different P2P bands at Ka-band instead of using multiple narrow-band receivers. The reception of different bands can be realized by changing the local oscillator (LO) frequency.

The target of this work is to explore and investigate the possibility of realizing a wideband phased array receiver at Ka-band using silicon-based technologies with competitive performance.

1.2. Problem Statement

Compared to III-V devices, silicon-based technologies have higher intrinsic NF_{min}, higher substrate loss and larger parasitic capacitance to the substrate. As a result, the problem statement of this thesis is:

[1] The uplink of Ka-band VSAT is at 29-31GHz but the downlink locates at 18-22GHz.

How to design wideband phased array receiver at Ka-band in silicon with competitive RF performance.

Specifically, the whole problem statement can be divided into two parts:

1. How to design wideband LNAs in silicon with low noise figure at Ka-band.
2. How to design wideband true-time-delay (TTD) phase shifters with low in-band delay error.

1.3. Aim of the Thesis

The thesis aims to carry on research in high performance mm-wave wideband phased array receiver. More specifically, this thesis will aim at design methodologies and techniques that can help reduce the NF of the LNAs and improve the delay flatness of the TTD phase shifters in silicon, and more specifically: BiCMOS.

1.4. Scope of the Thesis

This thesis will mainly focus on the front-end of a phased array receiver, which consists primarily of an LNA and a TTD phase shifter. Different versions of LNAs and phase shifters will be investigated and compared. Additionally, two different LNA/TTD frontends will be discussed, i.e. a low power version and a high power version, which could suit for applications with different power and linearity requirements. In the end of the thesis, a multi-channel phased array receiver will be discussed to provide a system level picture of this work.

1.5. Proposed Approach

To overcome the two main challenges discussed in Section 1.2, several approaches are proposed:

A. From the circuit level:

- Different LNA topologies will be compared and analyzed, from which the most proper topology of the given technology and frequency is selected. To optimize noise performance, different noise matching techniques will be investigated during the LNA design. Finally, alternative LNAs will be designed with different trade-offs between NF, gain, linearity, and power consumption.

- Explore delay variation (delay error) reduction techniques and prove the concept by silicon.

- Different delay cells will be investigated. For each delay cell, the correlation between delay variation and cut-off frequencies will be analyzed for different types of delay cells.

- Investigate both active and passive TTD phase shifter architectures to make comparison and suit for applications with different power and linearity requirements.

- The electromagnetic (EM) software will be extensively used to characterize passive components at mm-wave frequencies.

B. From the system level:

The characteristic and challenges of broadband phased array system will be investigated, including biasing, isolation between different channels, power dissipation, and signal combining, etc.

1.6. Outline of the Thesis

The thesis is organized as follows. Chapter 2 presents the broadband phased array concept, analysis of different TTD circuit cells, and the characteristic of the technology that will be used in this work. Chapter 3 discusses three alternative Ka-band LNAs and the noise matching techniques involved in the first stage LNA design. In Chapter 4, a delay variation cancellation technique is proposed and explained. With the delay variation reduction technique, an active TTD phase shifter will be presented, which achieves 6.6% normalized delay variation at 20-40 GHz. A high power 25-35 GHz TTD receiver frontend will be discussed afterward by integrating the active TTD phase shifter with one of the proposed

Ka-band LNAs. In order to suit for low power applications, Chapter 5 presents a passive TTD phase shifter, which employs the proposed broadband matching technique and achieves only 3.9% normalized delay variation at 10-50 GHz. By integrating the passive TTD phase shifter and the proposed low power Ka-band LNA, a 25-35 GHz TTD frontend with 22.4mW power consumption will be presented as well. In Chapter 6, a 2-by-2 TTD phased array receiver will be presented. The receiver includes low-power LNA, passive TTD phase shifter, RF variable gain amplifier (VGA), power combiner and down-conversion mixer. Chapter 7 concludes this thesis and gives directions for future work.

2. Broadband Phased Array System

2.1. Phased Array Systems

A Phased array is an array of antenna elements acting as a single antenna, which can adjust its effective radiation pattern to be reinforced in the desired direction and suppressed in the undesired direction. Figure 2-1 shows the system diagram of a typical one-dimensional 4-element all-RF phased array receiver frontend. Each individual receiver element consists of an LNA, an RF phase shifter, and an RF VGA, and can therefore independently change its relative amplitude and phase response from the other receiver elements. By applying proper gain and phase settings of each receive element, a receiver beam pattern can be generated with the main beam in the direction of the desired signal and a null in the direction of the interference [3]. This behavior is called spatial selectivity and is realized when all the four signal is combined, which in Figure 2-1 is achieved by the RF combiner.

Especially in mm-wave frequencies, the high path loss usually results in a stringent link budget and limits the communication distance. Fortunately, the phased array technique helps to improve the effective single-to-noise ratio (SNR) at the receiver side. This is achieved at the signal combiner, where the signal is added coherently while the noise is added incoherently [4]. As a result, SNR of the signal can be improved by $10\log(N)$ (dB).

The phased array technique is also useful in transmitter designs where the PA needs to deliver a large output power. Comparing an N-element phased array transmitter to a single antenna transmitter, if each transmitter element has the same radiation power, the saturation power (P_{sat}) of the PA in each transmitter element is reduced by 10log(N), making the PA design less challenging. The total transmitted power will be summed in the air at the desired direction, which improves the power efficiency by avoiding a lossy power combiner on-chip.

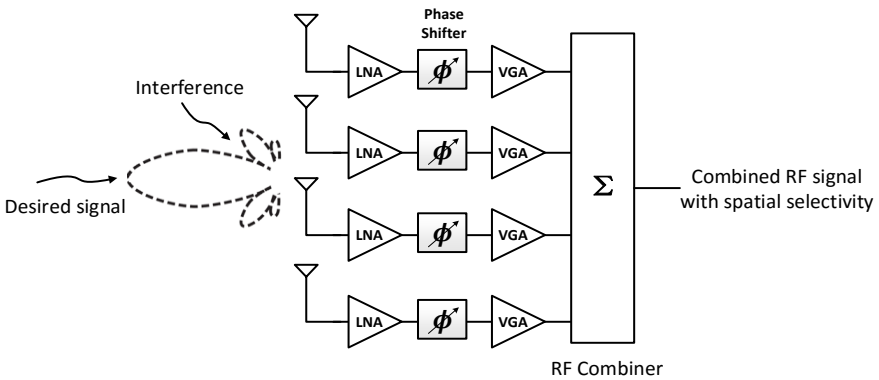


Figure 2-1. A typical all-RF one-dimensional 4-element phased array receiver frontend

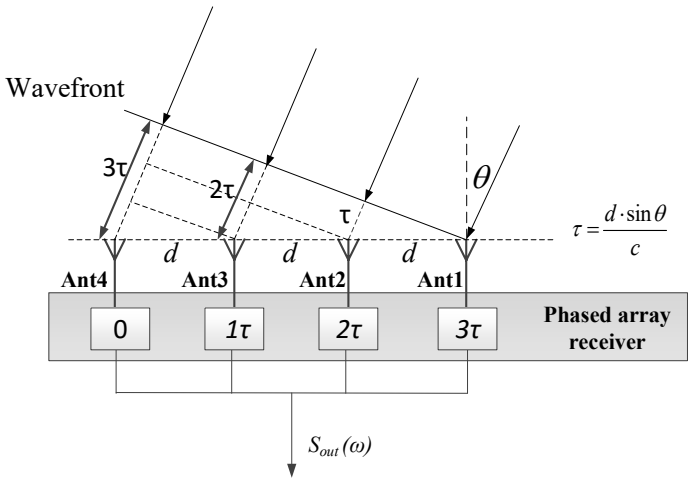


Figure 2-2. Basic concept of a one-dimensional 4-element phased array receiver

Figure 2-2 shows the basic concept of a one-dimension 4-element phased array receiver, where d is the distance between two antenna elements, θ is the angle of the incoming signal, and τ is the time delay between the received signal at two adjacent antennas. With an equal distance d between antennas, τ can be expressed as:

$$\tau = \frac{d \cdot \sin\theta}{c} \tag{2.1}$$

where c is the speed of light in the air. Since in practice d is fixed once the antenna array is fabricated, τ is constant over the frequency. As a result, to coherently add the signal at S_{out} node, each phased array receiver element has to provide a so-called true-time-delay (TTD) to compensate for the frequency independent time delay τ. Equation (2.1) can also be written in the form of a frequency dependent phase shift:

$$\phi = \omega_{sig}\tau = \frac{2\pi d \cdot \sin\theta}{\lambda_{sig}} \tag{2.2}$$

where ω_{sig} and λ_{sig} are the angular frequency and the wavelength of the incoming signal, respectively. Note that ω_{sig} does not necessarily equal to the frequency at which the antenna is designed and fabricated. To distinguish the two, the antenna operating frequency is denoted as ω_{Ant}. To prevent multiple main beams [5], the spacing d is usually chosen close to half of the antenna wavelength, i.e. $d = \pi c/\omega_{Ant}$. As a result, (2.1) and (2.2) can be reformed as:

$$\tau = \frac{\pi \cdot \sin\theta}{\omega_{Ant}} \tag{2.3}$$

$$\phi = \pi \sin\theta \frac{\omega_{sig}}{\omega_{Ant}} \tag{2.4}$$

As ω_{Ant} is fixed once the antenna array is design and fabricated, the phase shift ϕ in (2.4) is a linear function of the signal frequency ω_{sig}. In a narrow band system, however, it can be assumed that $\omega_{sig} \approx \omega_{Ant}$, with which (2.4) reduces into the well-known equation:

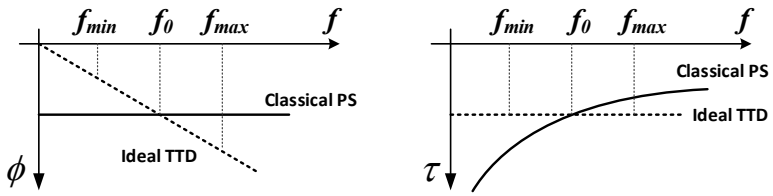
$$\phi = \pi \sin\theta \tag{2.5}$$

Regarding phased array receiver architectures, there are several ways to compensate the delay between adjacent antenna elements: RF phase shifting [6], IF phase shifting [7], local oscillator (LO) phase shifting [8], and digital phase shifting [9]. Among all of these solutions, RF phase shifting architecture repeats only the RF components, i.e. LNA, phase shifter, RF VGA, in each channel and is therefore the most compact architecture. The drawback of RF phase shifting is the increased NF and nonlinearity introduced by the RF phase shifter. LO phase shifting avoids degrading the RF performance by realizing the required delay in the LO paths before feeding to the mixer of each channel. However, it requires multiple mixers and an LO distribution network. Especially in mm-wave frequencies, long distance LO routing may introduce undesired coupling between different blocks and degrade the phase noise of the LO signal. When the delay is implemented at a lower frequency, such as in IF and digital phase shifting architecture, more design flexibility can be gained, e.g. applying signal processing and different calibration algorithm. However, compared to RF and LO phase shifting, even more blocks has to be integrated before signal combining, adding significant power dissipation. Another important advantage of RF phase shifting is the suppressing of strong interference by combing multi-channel signal in very early stage. Therefore, RF phase shifting greatly relaxes the linearity requirement of the following receiver blocks. On the contrary, digital beamforming requires high dynamic ADCs due to the existence of strong inference, which is extremely power hungry.

2.2. Broadband Beamforming

As the signal bandwidth increases, the assumption $\omega_{sig} \approx \omega_{Ant}$ does not hold anymore and a TTD phase shifter is required. Figure 2-3 shows the comparison of the phase response (Figure 2-3a) and delay responses (Figure 2-3b) between the ideal TTD phase shifter (dash) and the classical phase shifter (solid). The ideal TTD circuit exhibits a linear phase response and a constant delay response over the frequency, which is in equivalent with (2.3) and (2.4). The classical phase shifter, which provides constant phase shift over the frequency, can only approximate the required delay near the center frequency f_0. Assume the received signal has a bandwidth from f_{min} to $f_{max,}$ the realized delay using a classical phase shifter significantly varies over the frequency *(*see Figure 2-3b*)*. As a result, the beam angle of the receiver changes as a function of signal frequency (see Figure 2-4), which is also called as beam squint phenomena [10]. For simplicity, it is assumed

that the beam angle for the central frequency f_0 (denoted as θ_{f0}) is aligned with the direction of the desired signal. The amount of beam angle offset is defined as $\theta_{offset} = | \theta_{fmin} - \theta_{fmax} |$ in degree (see Figure 2-4).



(a) (b)

Figure 2-3. Comparison of (a) phase response and (b) delay response between classical phase shifter and ideal delay circuit

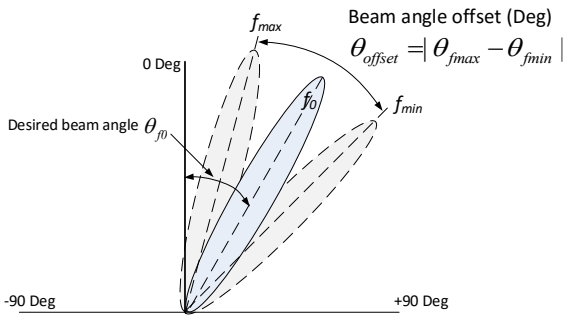


Figure 2-4. Beam squint phenomena due to large delay variation of the phase shifter

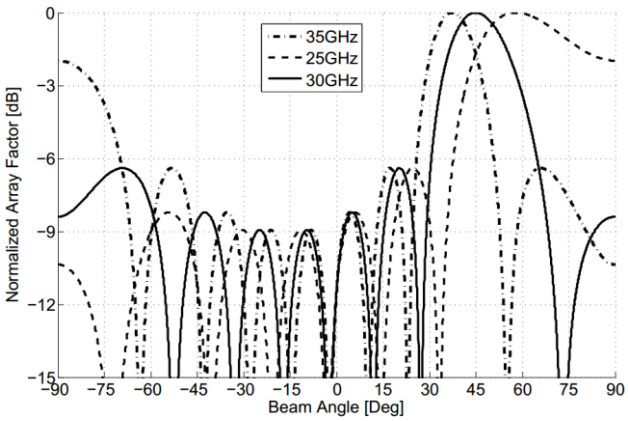


Figure 2-5. Simulated beam pattern for a one-dimension 8-element phased array which uses classical phase shifters (with a 30GHz antenna and 45-degree beam angle)

To demonstrate the negative impacts of the beam squint on broadband beamforming, Figure 2-5 plot the beam pattern of a one-dimension 8-element phased array using classical phase shifters. It is assumed that the antenna array is designed at 30 GHz, i.e. f_0 = 30 GHz and d = 5 mm, with the desired beam angle θ_{f0} = +45 degree at 30 GHz. It can be seen that as the signal frequency changes from 25 GHz to 35 GHz, the beam angle varies from 37 to 59 degrees ($\theta_{offset} = 22°$). Consequently, if there is a strong inference from +55 degree direction, it will be picked by the receiver with the maximum array gain.

Moreover, even without an interference issue, the SNR of the desired signal is reduced due to the misalignment of the beam angle. For instance, both the 25 GHz the 35 GHz signal coming from +45 degree direction are attenuated by 1.7 dB. As the array size increases, the signal attenuation level mentioned above can increase dramatically, e.g. 12.2 dB attenuation for a one-dimension 16-element phased array receiver.

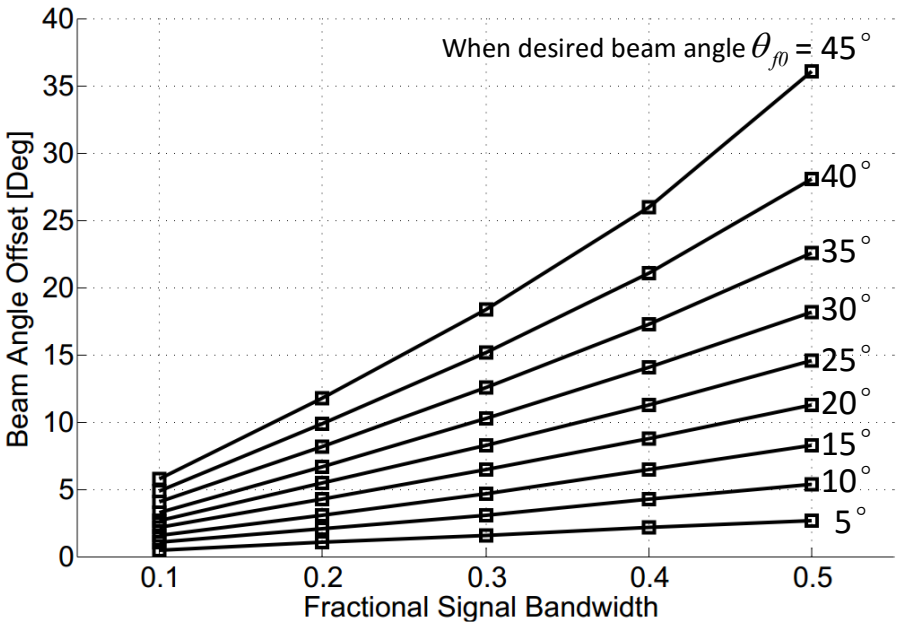


Figure 2-6. Resulted beam angle offset as a function of fractional signal bandwidth and desired beam angle at central frequency f_0

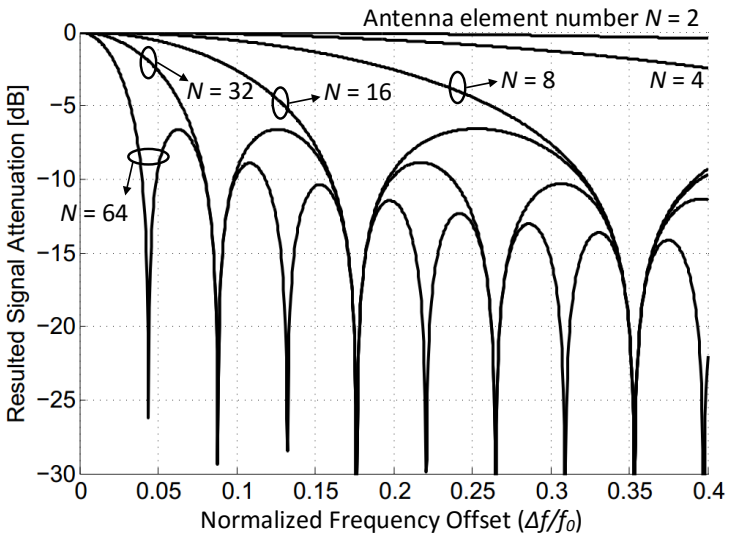


Figure 2-7. Resulted signal attenuation from beam squint as a function of frequency offset and array size N, assuming $\theta_{f0} = 45°$

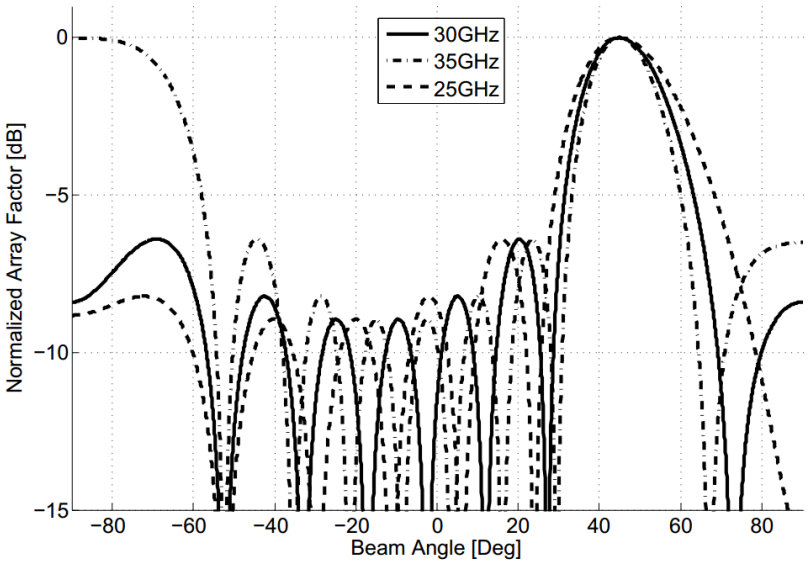


Figure 2-8. Simulated beam pattern for a one-dimension 8-element phased array which uses TTD phase shifters (with a 30GHz antenna and 45-degree beam angle)

Consider a general phased array using classical phase shifters, the beam angle offset and the resulted signal attenuation due to the frequency change depend on the signal bandwidth, array size, and the desired beam angle, i.e. θ_{f0}. Figure 2-6 plots the beam angle offset as a function of fractional signal bandwidth and θ_{f0}, where the fractional signal bandwidth is defined as $|f_{max} - f_{min}| / f_0$ (see Figure 2-4). The antenna array is assumed to be one-dimensional and has a uniform antenna spacing equals to a half wavelength. It can be seen that beam squint becomes more severe when the signal bandwidth becomes larger or a large beam angle has to be achieved. Note that the result shown in Figure 2-6 is independent of the array size. In another word, a 2-element and a 16-element phased arrays result in the same beam angle offset.

To evaluate the impact of the beam squint on the degradation of signal SNR, Figure 2-7 plots the resulted signal attenuation as a function of normalized frequency offset and array size N (assuming $\theta_{f0} = 45°$). The normalized frequency offset is defined as $|\Delta f / f_0|$, where Δf represents the difference between signal frequency and the central frequency f_0. Due to symmetry, the signal attenuation at $\pm\Delta f$ is identical. As shown in Figure 2-7, with the same frequency offset, a larger N results in a larger signal attenuation. This is as expected because a larger array size leads to a narrower beam, making the signal attenuation more sensitive to the frequency offset. Additionally, as N and frequency offset increases, one or multiple nulls are generated at certain frequencies, indicating that the signal at these frequencies will be completely blocked due to the beam squint.

All of these beam squint issues in broadband beamforming can be eliminated by using TTD phase shifters. As shown in Figure 2-8, the main beam direction of a TTD phased array receiver keeps constant as the desired angle of +45 degree for different signal frequencies. As a result, there will be no signal attenuation or beam angle offset for any array size and signal bandwidth. Depending on the system speciation, i.e. array size, signal bandwidth, and maximal allowable signal attenuation, one can determine whether a TTD phase shifter or a classical phase shifter should be used.

This work targets to design a phased array receiver frontend covering 25-35 GHz frequency band, which results in more than 33% fractional bandwidth. As shown in Figure 2-6 and Figure 2-7, performing such broadband beamforming using classical phase shifters will result in severe beam squint, e.g. 22° beam offset and >10 dB signal attenuation (assume $N = 8$ and $\theta_{f0} = 45°$). The beam squint issue can be mitigated by adaptively changing the phase setting according to the

incoming signal frequency. However, it will introduce additional feedback loops and extra power for digital signal processing. Therefore, in the work, the proposed broadband phased array receiver frontend employs TTD phase shifters rather than classical phase shifters.

2.3. Basic Delay Circuits and Delay Variation

2.3.1. Different types of delay cells

There are several approaches towards the silicon integrated implementation of delay cells. These time delay circuits can be mainly categorized into 2 groups: LC-based and RC-based. Two typical examples of the LC-based delay cell are the LC π-network [11] (C-L-C configuration) and the transmission line (TL) [12-14]. Actually, a TL can be viewed as a distributed structure composed by many small LC π-networks. The RC-based delay cells can be implemented either by RC low pass filters (LPF) or G_m-RC circuits [15-17]. Depending on amplitude responses versus frequency, the G_m-RC circuits can either be low-pass [17] or all-pass [15, 16].

At lower frequencies, e.g. below 10 GHz, where the dimension of the inductors are oversized, TTD circuits are usually implemented by RC or G_m-RC filters [15, 16]. Compared to the LC-based delay cells, these RC-delay cells are compact in area and have less design complexity by avoiding the inductive components in the design. However, one of the dominant drawbacks is the undesired trade-off between insertion loss, power dissipation, and linearity. RC-delay cells are very lossy, resulting in a high NF when used in a receiver. Adding G_m-cells for gain compensation will increase the power dissipation and limits the linearity of the overall TTD circuit. This issue is mitigated when realizing a TTD at high frequencies, e.g. beyond 20 GHz, where the transmission line and LC-network can be integrated with a reasonable footprint. Theoretically, the TL-based or LC-based delay cells have no power dissipation, unlimited linearity performance, and no additional loss except metal loss. However, the TTD performance of these circuits can be severely impacted by undesired parasitic and magnetic coupling, which are well-known issues at mm-wave frequencies.

2.3.2. Definition of normalized delay variation

Compared to an ideal TTD response, the realized delay from a practical delay circuit suffers from a certain fluctuation over the frequency. For simplicity, this undesired fluctuation is denoted as delay variation (DV) in this thesis. As the impact of the DV scales with the operating frequency, the normalized delay variation (NDV) is important too. For a delay circuit which offers a fixed delay, NDV_{fix} is defined as:

$$NDV_{fix} = [\max(\tau(\omega)) - \min(\tau(\omega))]/\tau_0 \times 100\% \tag{2.6}$$

where $\tau(\omega)$ is the delay response of the delay cell versus frequency and τ_0 is its nominal delay at low frequency (close to DC). For a complete TTD phase shifter with a variable time delay, NDV_{PS} is defined as the worst case delay variation for all delay settings in percentage of the total variable delay:

$$NDV_{PS} = max[\max(\tau_{1..i}) - \min(\tau_{1..i})]/\tau_{tot} \times 100\% \tag{2.7}$$

where $\tau_{1...i}$ is the delay response of phase shifter for each delay setting and τ_{tot} is the total variable delay.

2.3.3. Delay variation versus cut-off frequency

There are various sources of the delay variation. Besides those related to practical issues, e.g. parasitics and impedance mismatch, a delay cell inherently presents DV when operating close to its cut-off frequency (ω_C). In this section, the relation between DV and ω_C of the delay cells will be investigated. Since the distributed transmission line theoretically has an infinite cut-off frequency and no DV, the analysis will be focused on two types of lumped delay cells, i.e. the LC and G_m-RC delay cells.

Figure 2-9 shows the simplified LC delay cell and G_m-RC delay cell. For simplification of analysis, it is assumed that the LC network is matched both at the source and the load to $R_0 = \sqrt{L_A/2C_A}$. The absolute phase delay for the two delay cells can be written as:

$$\tau_{LC}(\omega) = -\frac{1}{\omega} tan^{-1} \frac{\omega}{\omega_{LC}} \frac{2-(\omega/\omega_{LC})^2}{1-2(\omega/\omega_{LC})^2} \tag{2.8}$$

$$\tau_{RC}(\omega) = -\frac{1}{\omega} tan^{-1} \frac{\omega}{\omega_{RC}} \tag{2.9}$$

where $\omega_{LC} = 2\pi f_{LC} = \sqrt{2/(L_A C_A)}$ and $\omega_{RC} = 2\pi f_{RC} = 1/R_B C_B$ are the cut-off frequencies of the two delay cells, respectively. The reason that τ_{LC} and τ_{RC} are negative values is because the delay cells perform a negative phase shift to the passing signal, i.e. making it slower than the original signal. It can be noted that when the operating frequency is far below the cut-off frequencies, i.e. $\omega \ll 2\pi f_{LC}$ and $\omega \ll 2\pi f_{RC}$, (2.8) and (2.9) will be reduced into $\tau_{LC}(\omega) \approx \tau_{LC}(0) = -\sqrt{2L_A C_A}$ and $\tau_{LC}(\omega) \approx \tau_{RC}(0) = -R_B C_B$, with which the delay cells provide a constant TTD over the frequency.

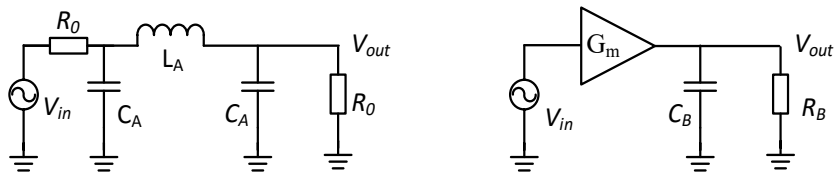


Figure 2-9. Simplified LC π-network (left) and Gm-RC cell (right)

However, when the operation frequency approaches the cut-off frequency, delay variation will be present. Figure 2-10 shows the simulated delay response of single stage LC and Gm-RC delay cell from 0.1 GHz to 60 GHz. It can be seen that with larger delay realized per cell, f_{LC} and f_{RC} drop and result in a larger delay variation at high frequencies. Figure 2-11 shows the quantitative relation between the realized delay per cell, resulted cut-off frequencies, and the resulted NDV. The NDV is calculated using definition in (2.6) assuming the operation frequency is from DC to 60 GHz. The realized delay per cell is expressed in phase shift at 30 GHz. It can be noted that by realizing the same amount of delay, f_{RC} is only half of f_{LC}, making RC delay cell more vulnerable to the delay variation at high frequencies. For instance, if both delay cells provide 20 degree phase shift at 30 GHz, i.e. about 1.85 ps delay, f_{RC} is 85.9 GHz while f_{LC} is 171.9 GHz (Figure 2-10), As a result, according to Figure 2-11, the NDV from Gm-RC delay cell is 12.7% compared to only 2.3% for LC delay cell. One of the reason is that Gm-RC delay cell has less poles than the LC delay cell hence the phase of the former decreases slower than the latter as the frequency increases. As a result, to provide the same amount of phase shift (or delay), the Gm-RC delay cell must have lower frequency pole than LC delay cell, resulting in lower cut-off frequency. Since less delay per delay cell helps to minimize the DV, TTD circuits usually employ a multistage architecture. By cascading *N*-stage uniform delay cells, each delay cell only provides 1/*N* of the total delay, which increases the cut-off frequency of each delay cell by a factor of *N* hence enables a low NDV up to a higher frequency. The NDV of the overall TTD circuit, by definition, is as good as the

NDV of individual delay cell. However, as in practice more delay stages result in larger area for LC delay cells, or higher power consumption for Gm-RC delay cells, trade-offs must be made carefully.

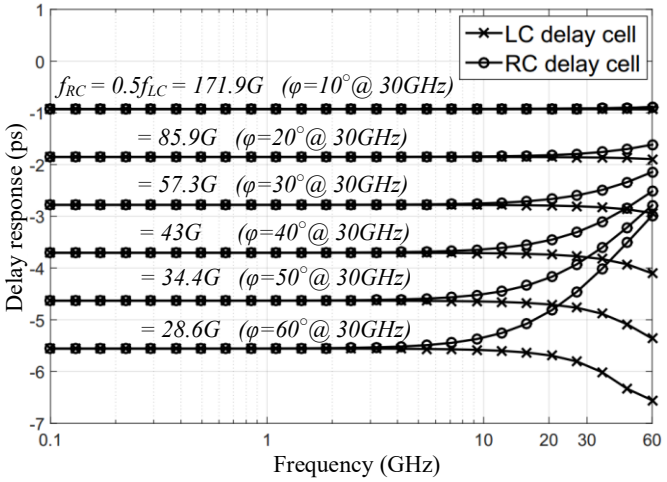


Figure 2-10. Simulated delay response of single stage LC and Gm-RC delay cell from 0.1 GHz to 60 GHz with different cut-off frequencies f_{LC} and f_{RC}

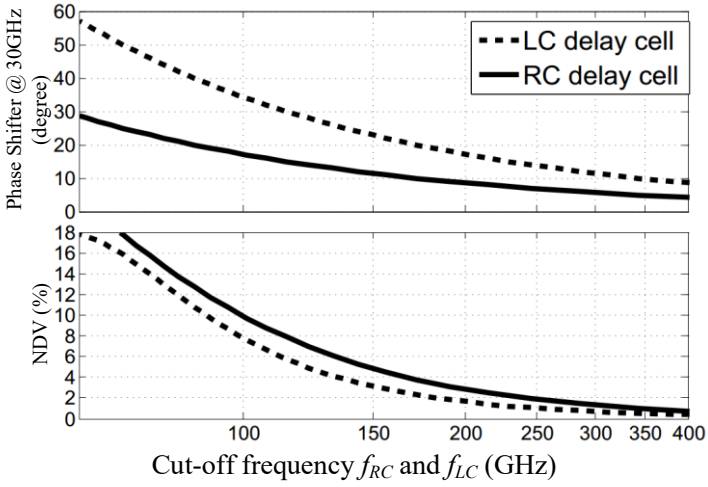


Figure 2-11. Simulated relation between the realized delay per delay cell, expressed in phase shift at 30 GHz (Top) and the resulted in-band NDV up to 60 GHz (Bottom), both plotted as a function of f_{LC} and f_{RC}.

2.4. Technology and Passive Components

2.4.1. Technology Comparison

The recent development of SiGe BiCMOS technologies enables designing high-performance mm-wave circuits and sub-systems. Compared to standard CMOS technologies, the SiGe HBT devices achieves larger small signal gain with the same power consumption. Additionally, SiGe HBT devices present lower *1/f* noise corner frequency and provide better frequency responses than standard CMOS devices at the same technology node.

Compared to III-V semiconductor-based technologies, e.g. GaAs and InP, SiGe BiCMOS technologies has a higher level of system integration and lower cost. In addition, as SiGe BiCMOS technologies maintain compatibility of standard CMOS manufacturing, the biasing and digital circuits which need to be implemented by CMOS transistors can be fully integrated.

2.4.2. SiGe Technology

The Ka-band receiver front-end ICs will be realized using a 0.25 μm SiGe:C BiCMOS technology with a peak f_T/f_{max} of 216/177 GHz [2]. The current gain of the low voltage NPN (LV-NPN) device is close to 2000 which almost eliminates the base current shot noise and makes the device rather similar to a GaAs FET in terms of noise performance. The NF_{min} of the LV-NPN device is approximately 0.35 dB at 2 GHz and 1.4 dB at 30 GHz for a minimum emitter width of 0.3 μm. A high voltage NPN device (HV-NPN) with reasonable f_T is also available in this technology, offering a collector-emitter breakdown voltage for the open base (BV_{ceo}) of 2.5 V.

The back-end in this technology has 2 thick top metal layers suitable for the realization of high-performance inductors with large current handling. The process also offers high-quality, high-density (5 fF/μm^2) Ta_2O_5 MIM capacitors with low parasitics (less than 0.5% capacitance to substrate). Furthermore, a high-ohmic substrate (200 Ω·cm) which reduces the effect of parasitic capacitances can be combined with deep trench isolation (DTI) to further increase the substrate resistance.

2.4.3. Quality factor of passive components

The quality factor (Q-factor) of passive components e.g. inductors and capacitors, has a significant impact on the RF circuit performance. The Q-factor degradation of the passive components basically originates from two part: the metal resistive loss and the coupling to the lossy substrate. The metal loss can be significantly reduced by using a thick and wider metal at low frequency. At high frequencies, however, the improvement is limited due to the skin effect. The coupling to the lossy substrate consists of both capacitive coupling and magnetic coupling. This can be improved by inserting an isolation layer between the passive circuits and the lossy substrate. For instance, in CMOS technologies where the substrate is relatively low-ohmic, a patterned metal shielding is usually used underneath the inductors to improve Q-factor. The shielding, however, increases the parasitic capacitance and limits the self-resonant frequency of the inductors.

The available high-ohmic substrate and DTI in the used technology significantly reduces both coupling mechanisms to the substrate, which enables high Q-factor passive circuits design without using a metal shielding. For instance, a single metal layer 200 pH spiral inductor with single-ended excitation achieves a Q-factor of 29 at 30 GHz with the self-resonant frequency above 90 GHz. A 500 fF MIM capacitor achieves a Q-factor of 135 at 30 GHz. By stacking the 2 thick top metals, the 50 Ω transmission line exhibits an insertion loss of 0.48 dB/mm at 30 GHz. If the 2 top metals are used to realize the primary and secondary windings of a vertical transformer, a coupling factor of 0.75 can be achieved at 30 GHz.

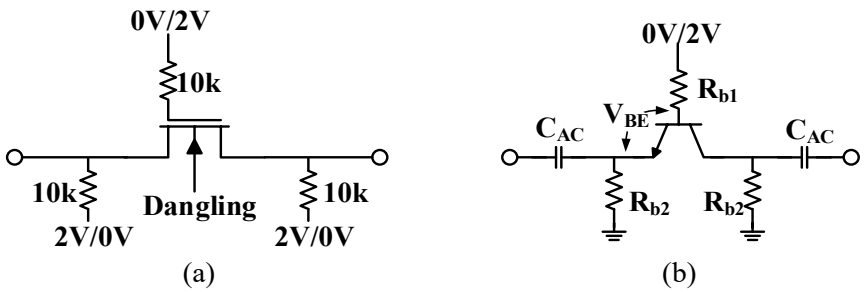


Figure 2-12. Schematic of RF switches using (a) 0.25 μm nMOS device and (b) 0.3 μm LV-NPN (same for HV-NPN)

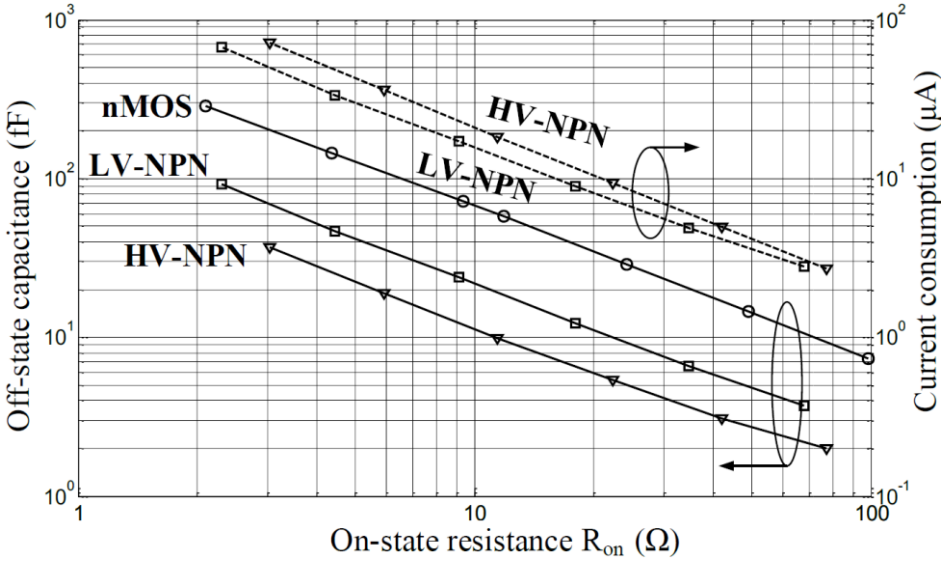


Figure 2-13. Simulated on-state resistance, off-state capacitance, and current consumption for nMOS switch, LV-NPN switch, and HV-NPN switch. The V_{BE} of both LV- and HV-NPN switches in on-state is fixed to 800 mV.

2.4.4. RF switches

To obtain low insertion loss in on-state and high isolation in off-state, the RF switch needs a low on-resistance (R_{on}) and low off-state capacitance (C_{off}). Unfortunately, for the same device with the same bias condition, the product of the two parameters, i.e. $R_{on} \times C_{off}$ is more or less constant during device scaling. Therefore, trade-offs must be made.

Within the technology, the RF switches can be realized in 3 ways, based on a 0.25 μm nMOS device, a 0.3 μm LV-NPN device or a 0.3 μm HV-NPN device. Figure 2-12 shows the schematic of nMOS and NPN device based series-switches. The maximal supply voltage is assumed to be 2 V. The nMOS switch is configured as V_G = 2 V, V_D/V_S = 0 V at ON state and V_G = 0 V, V_D/V_S = 2 V at OFF state. The bulk node of the nMOS device is dangling, i.e. connected to the very high impedance node, in order to isolate the parasitic capacitance from the global substrate and improve the isolation of the switch at OFF state. To eliminate power dissipation, the NPN-based switch is used between 2 AC-coupling capacitors, i.e. C_{AC}. As a result, no collector current is consumed, making the proposed NPN

switches similar to nMOS passive switches. There is, however, a small DC current flowing from the base terminal to both emitter and collector terminals when the switch is on. The amount of the base current depends on the base-emitter voltage (V_{BE}) of the device in on-state, which is set by the biasing resistor R_{b1} and R_{b2}. Figure 2-13 shows the simulated R_{on}-C_{off} characteristic for the switch based on nMOS device, LV-NPN device, and HV-NPN device. In the simulations, the maximal supply voltage is assumed to be 2 V and the on-state V_{BE} for both LV- and HV-NPN switches are fixed to 800 mV during the scaling of the NPN devices. With the biasing condition shown in Figure 2-12, the HV-NPN device as RF switch presents the lowest product of $R_{on}C_{off}$. Therefore, all the switches used in the discussed phase shifter and receiver front-end designs are based on the HV-NPN switch shown in Figure 2-12b. Depending on the requirements in the designs, R_{on} and C_{off} of the switches are adjusted by scaling the device and changing the on-state V_{BE}. The current consumption per switch ranges from 3 to 50 μA.

3. Ka-Band Low Noise Amplifier

Typical applications in Ka-band (26.5 GHz to 40 GHz) such as LMDS and broadcast VSAT require highly sensitive receivers to improve the communication distance and reliability. The NF of the receiver limits the receiver sensitivity thus must be minimized. The low noise amplifier is the first circuit component in the receiver chain. According to the Friis' formula, the NF of the LNA, if ignoring filters, dominates the overall receiver NF. Although LNA designs in III-V compound technologies such as pHEMT GaAs can offer a low NF, the relatively higher cost and lower integration capability has advocated for (fully) integrated solutions in silicon-based technologies.

The recent breakthroughs in BiCMOS/CMOS technologies with cut-off frequencies (f_T) better than 200 GHz have enabled the realization of silicon-based LNAs at Ka-band frequencies using devices with a minimum noise figure (NF_{min}) below 1.5 dB. In this chapter, 3 alternative 0.25 μm SiGe:C BiCMOS Ka-band LNAs are presented which are capable of achieving less than 3 dB NF in the 30 GHz range. These LNAs have different trade-offs between gain, bandwidth, power dissipation and linearity, in order to fit different application needs.

3.1. Input stage of the LNA

According to the Friis' formula, the first stage of the LNA is the most critical stage in determining the overall NF of the LNA. With given technology and operating frequency, the noise performance can be optimized by choosing the most suitable topology; choosing an optimum noise current density and proper noise matching; and careful circuit implantation at layout level. These three aspects will be discussed in the following sub-sections.

3.1.1. Topology Comparison

Figure 3-1 shows 5 topology candidates that are commonly used as input stages in LNAs and we need to explore their capability at mm-wave frequencies.

A. Common-base (CB)

One of the superior features of the CB structure (Figure 3-1a) is that it minimizes the impact of the Miller capacitor, improving thereby the reverse isolation and stability. In addition, the CB topology is widely used in ultra-wide-band (UWB) LNA designs for its wideband input match. However, the input impedance of a CB LNA is approximately $1/g_m$, with $g_m \approx 40 I_c$ for a bipolar design. Having the input impedance matched to 50 Ohms means that the collector current is approximately $I_c \approx 0.5$ mA. First of all, such a small current consumption can hardly fit the input 1dB compression point (input P_{1dB}) requirement of this work. Secondly, according to the optimal noise current density (section 3.1.2) the corresponding optimum emitter length is smaller than 1 μm, which can hardly be fabricated in practice. Even if the fabrication issue can be disregard, an LNA with such a small transistor size will be very sensitive to process variations.

B. Common emitter (CE) structure with degeneration

The CE topology is one of the most popular architecture choices in LNA designs (Figure 3-1b). With the inductive emitter degeneration to provide the desired real part of the input impedance, the input of the LNA can be easily matched to 50 Ohm. Due to the negative feedback, the NF and linearity performance are also improved slightly compared to CE only without degeneration. The downside of this architecture is that when the frequency increases, the CE LNA is vulnerable to the Miller effect and hence has a degraded reverse isolation and stability performance.

C. Voltage-voltage feedback structure

The usage of an integrated transformer provides extra freedom. As shown in Figure 3-1c, by properly utilizing the mutual coupling between the degeneration inductor L_{deg} and load inductor L_O, the impact of miller capacitance C_{bc} can be removed [18]. This neutralization behavior improves gain and reverses isolation.

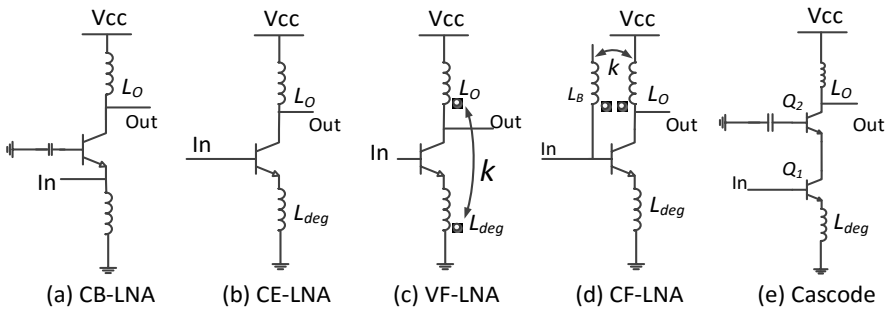


Figure 3-1. Schematic of different LNA topologies (bias circuitry not shown).

To achieve this, the transformer need to satisfy the relation $N/k = -C_{be}/C_{bc}$ with the assumption that k is close to 1, where $N = \sqrt{L_O/L_{deg}}$ is the turn ratio of the transformer and k as the coupling coefficient between L_O and L_{deg} [18]. This requirement is more reasonable when the circuit was built in CMOS, where a typical ratio of C_{gs}/C_{gd} is 3 [18, 19], leading to a realistic solution of N = 2.4, k = 0.8 [18]. For the low-noise bipolar device used in this work, however, a typical ratio of C_{be}/C_{bc} is about 12. Since the turn ratio of a transformer is limited for practical consideration, a weak coupling is needed, e.g. k = 0.25, N = 3. With such a low coupling factor, the assumptions for neutralization will not hold any more and the benefits that can be gained from the feedback will be marginal [19]. In fact, since the device has an f_T of over 7 times of operating frequency, the negative impact due to the Miller capacitor is rather limited, meaning that a good reverse isolation can be achieved even without neutralization techniques.

D. Current feedback structure

Figure 3-1d shows the current feedback LNA (CF-LNA). The feedback is applied via a transformer, consisting of weakly coupled inductors L_B and L_O, with a coupling coefficient k. During the operation, the secondary inductance L_O senses the current in the collector branch and feeds back a small current to the base node via the primary inductance L_B. With an optimum combination of k, L_O, and L_B, the LNA can be unilateral, improving gain and isolation [20]. However, it can be shown that this topology at 30GHz has an instability risk for a large coupling coefficient k, i.e. $k > 0.5$. For this reason, the value of k must be controlled within a certain desired range, which requires intensive EM-simulations and increases the design complexity. The advantage of this feedback, however, is limited to

some extent due to the inherent good reverse isolation of the device, as has been mentioned above.

E. Cascode structure

The cascode structure offers conditions for the achievement of high gain, good isolation, input matching and low noise simultaneously (Figure 3-1e). The achieved available gain (G_a) and reverse isolation help to minimize the impact of following stages on the overall NF and S_{11} of the LNA, which is attractive in a multi-stage LNA design. A potential drawback of the cascode architecture, on top of the need for a higher supply voltage, is that the noise mismatch between Q_1 and Q_2 can degrade the total NF of the LNA. Hence, a noise matching network may be necessary between the CB (Q_2) and CE (Q_1) transistors.

Based on the discussion above, a cascode structure as the first stage has been chosen, because it incorporates the advantages of both CB and CE topologies and is easier to realize compared to solutions using transformer elements.

3.1.2. Noise matching

A. Optimum Noise Current Density

With a cascade input stage, the noise contribution from the input CE transistor is dominating, therefore, must be minimized. Figure 3-2 shows the NF_{min}, unit current-gain frequency (f_T), and maximum oscillation frequency (f_{MAX}) of the low noise NPN device (with CE configuration) as a function of the collector current density (J_C). It shows that the lowest NF_{min} at 30GHz is achieved with J_C = 2mA/μm². However, at a higher current density, e.g. J_c = 4mA/μm², a higher power gain can be obtained, due to higher f_T and f_{MAX}. In practice, this is also beneficial for minimizing overall LNA NF as it reduces the noise contribution from the cascode CB transistor as well as the following stages of the LNA. Fortunately, the NF_{min} responses shown in Figure 3-2 is almost flat with J_C from 1mA/μm² to 4mA/μm². As a result, a compromise is achieved by choosing the optimum noise current density J_{optN} = 3.8mA/μm², which results in an NF_{min} of 1.45 dB at 30GHz and f_T better than 200 GHz.

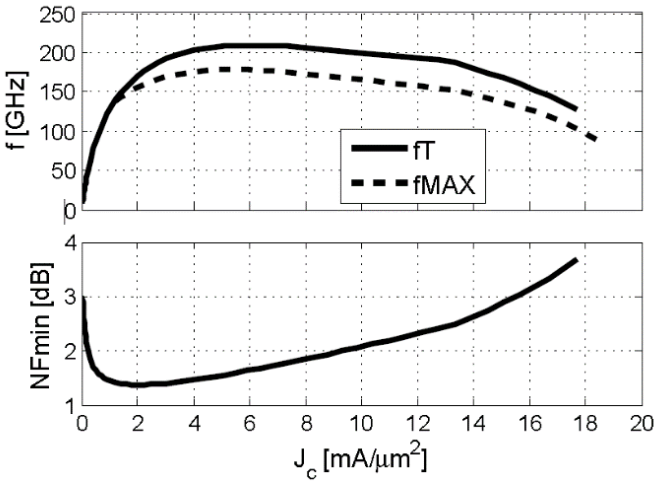


Figure 3-2. Simulated NF_{min}, f_T, and f_{MAX} of the low noise NPN device (with CE configuration) as a function of the collector current density J_C.

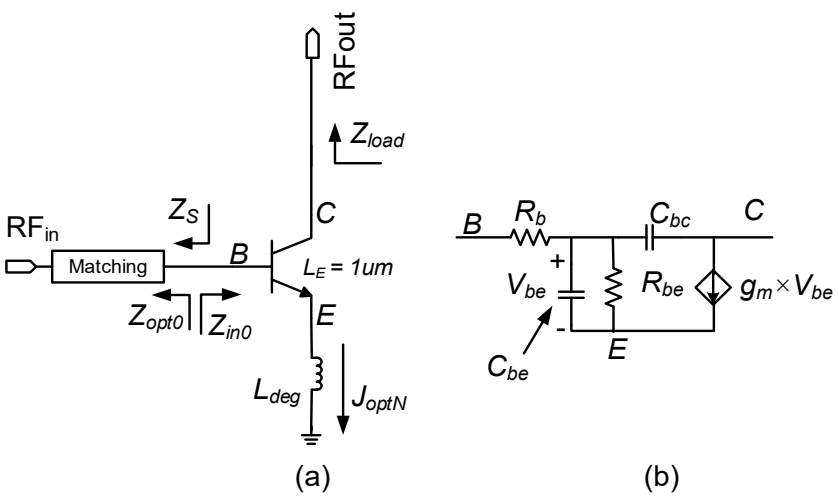


Figure 3-3. (a) Schematic of a unit-size degenerated CE-LNA and (b) the transistor model used for calculation.

B. Simultaneously noise and power matching

A good noise match is crucial in the LNA design as it minimizes the degradation of the actual NF from NF_{min}. Meanwhile, the gain match or conjugate match at

the input should also be fulfilled to maximize both G_T and G_a, which improve the signal gain and minimize the noise contribution from the later stages. However, a trade-off exists between NF and the input return loss as the optimal noise source impedance Z_{opt} is usually different from the source impedance Z_S which has a conjugate match with the input impedance of the LNA (Z_{in}). Hence, the desired target is to make Z_{in} close to Z^*_{opt}, in which case the noise and gain match can be simultaneously achieved. Mathematically, this is equivalent to minimize the expression [21]:

$$\left|\Gamma_{in-opt}\right| = \left|\frac{Z_{in} - Z^*_{opt}}{Z_{in} + Z^*_{opt}}\right| \tag{3.1}$$

In this work, two main parameters are optimized for minimizing (3.1), which are the degeneration inductance L_{deg} and the emitter length L_e, assuming minimum emitter width is used. To derive the optimum relation between L_e and L_{deg}, both Z_{in} and Z_{opt} in (3.1) have to be derived as a function of L_e and L_{deg}.

As shown in Figure 3-3a, where a unit-size (L_e = 1 μm) inductively degenerated common-emitter (CE) transistor is biased at the optimal noise current density J_{optN} = 3.8 mA/μm². Both the optimal noise source impedance and the input impedance of the transistor can be derived, denoted as Z_{opt0} and Z_{in0}, from its Y- or Z-parameters [22] . Assuming ideal linear scaling of emitter length L_e, Z_{in} can be written as:

$$Z_{in} = \frac{1}{L_e} Z_{in0} = \frac{1\,\mu m}{L_e}\left(z_{11} - \frac{z_{12}z_{21}}{z_{22}+Z_{load}}\right) \tag{3.2}$$

with

$$z_{ij|i,j=1,2} = z_{ij0|i,j=1,2} + sL_{deg} \tag{3.3}$$

where $z_{ij0|i,j=1,2}$ are the Z-parameters of the unit-size transistor for which the small-signal equivalent circuit is shown in Figure 3-3b, and Z_{load} is the output termination of the transistor, which can be approximated as $1/g_m$ for cascade structure. When $L_{deg}C_{bc}\omega^2$ is much smaller than 1 and g_m/sC_{bc} much larger than 1, Z_{opt} becomes to:

$$Z_{opt} = \frac{1\,\mu m}{L_e} Z_{opt0} - sL_{deg} \tag{3.4}$$

As a result, with each given transistor emitter length L_e, an optimum L_{deg}, which leads to a simultaneous noise and gain matching, can be found by solving:

$$\frac{\partial \left| \Gamma_{in-opt} \right|}{\partial L_{\deg}} = 0 \tag{3.5}$$

Based on the knowledge above, we start now to design the CE transistor from a minimum size (W_e = 0.3 μm, L_e = 1 μm), and assume that the device is optimal biased according to J_{optN}. The Z-parameters for the device can be extracted using the small-signal model in Figure 3-3b and lead to Z_{opt0} is *1040+j660* at 30 GHz [22]. The optimum relation between L_{deg} and L_e can now be derived by substituting (3.1)-(3.4) in (3.5), and is plotted in Figure 3-4. Since each combination of L_e and L_{deg} in the figure minimizes (3.1), an extra design freedom can be obtained by optimizing the value of L_e. On one hand, the CE transistor needs to be scaled and biased at a reasonably large collector current for input P1dB and IIP3 requirements. On the other hand, as shown in the right axis of Figure 3-4, the real part of the input impedance ($Re(Z_{in})$) is plotted as a function of different combinations of L_e and L_{deg} values, based on (3.2) and (3.4). For instance, the combination L_{deg} = 50 pH and L_e = 20 μm leads to $Re(Z_{in})$ close to 50 Ω. This will ease the design of input matching network because only a small series inductance is required to transform Z_{in} to 50 Ω. In practice, L_{deg} with such a small value needs to be implemented with a customized transmission line and characterized in the EM simulator, e.g. Agilent Momentum.

Figure 3-5 shows the simulated impedance transformation in the Smith chart, providing a more intuitive way to demonstrate how simultaneous noise and gain matching is achieved with the derived L_{deg} and L_e values. Starting point are Z_{opt0} and Z_{in0}, marked with the black crosses, which are the optimal noise source impedance and the input impedance of the unit-size CE transistor, respectively. By scaling L_e up 20 times, both impedances decrease by 20 times, shown as triangles in the figure. The added 50 pH degeneration inductor L_{deg} increases the real part of the Z_{in} and decreases the imaginary part of the Z_{opt}. Since (3.1) is minimized, Z_{opt} and Z_{in} become almost conjugate to each other and are located on the 50 Ohm constant real impedance circle, shown by the squares in Figure 3-5. Finally, with a series inductor at the input, both the noise and gain matching can be achieved for 50 Ohms source impedance.

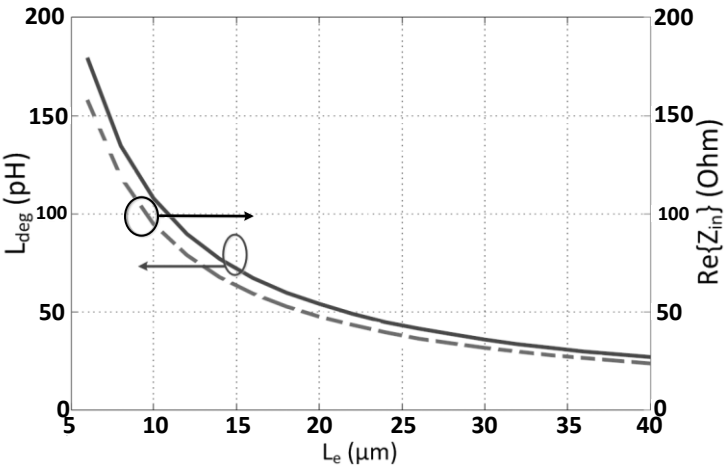


Figure 3-4. Different combinations of L_{deg} and L_e that minimize $\Gamma_{in\text{-}opt}$ and the corresponding real part of the input impedance of the LNA.

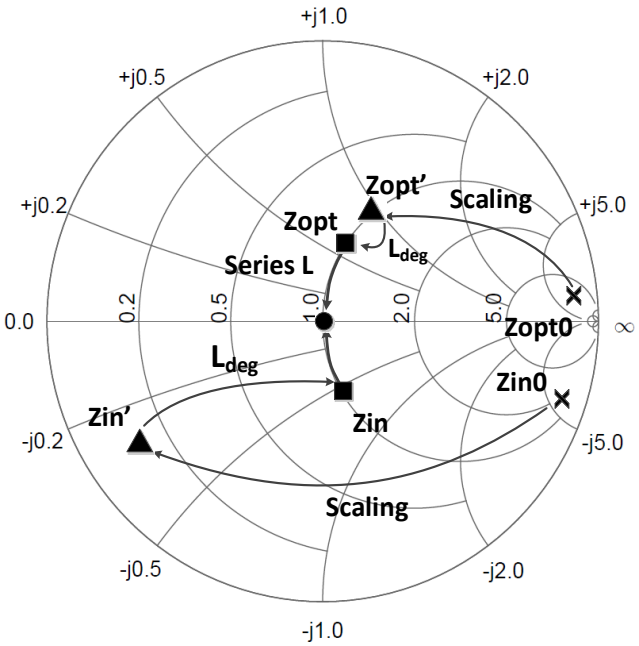


Figure 3-5.Transformation of Z_{opt} and Z_{in} in the Smith chart by scaling the device and adding a degenerated inductance.

C. Noise matching between CE and CB transistors

Although the CE-transistor has provided a certain available power gain, the noise from the CB-transistor in the cascode stage will degrade the overall NF. Therefore, a proper noise matching is needed between the CE and CB transistors. Denote the output impedance of the CE-transistor (Q_1) as Z_{out1} and the optimal noise source impedance of CB transistor (Q_2) is Z_{opt2}. A noise matching network, located between the output of the CE-transistor and the input of the CB-transistor, is supposed to transform Z_{out1} to Z_{opt2} and makes the NF of transistor Q_2 equal to the $NF_{min\text{-}Q2}$. As a result, the noise contribution of the CB-transistor to the overall NF is minimized.

As shown in Figure 3-6, Z_{out1} is plotted as a black square. By increasing the length of Q_2, the corresponding Z_{opt2}, plotted as black crosses in the Smith chart, moves to the lower impedance side. For the simplicity of the matching network, Q_2 is chosen to have a length of 40 μm, at which Z_{opt2} shares the same real part as Z_{out1}. This means that the transformation from Z_{out1} to Z_{opt2} can easily be done with only a series inductor of, in this case, 70 pH. Compared to the traditional cascode topology, the proposed structure with noise matching between CB and CE transistors improves the overall NF by 0.15 dB at 30 GHz.

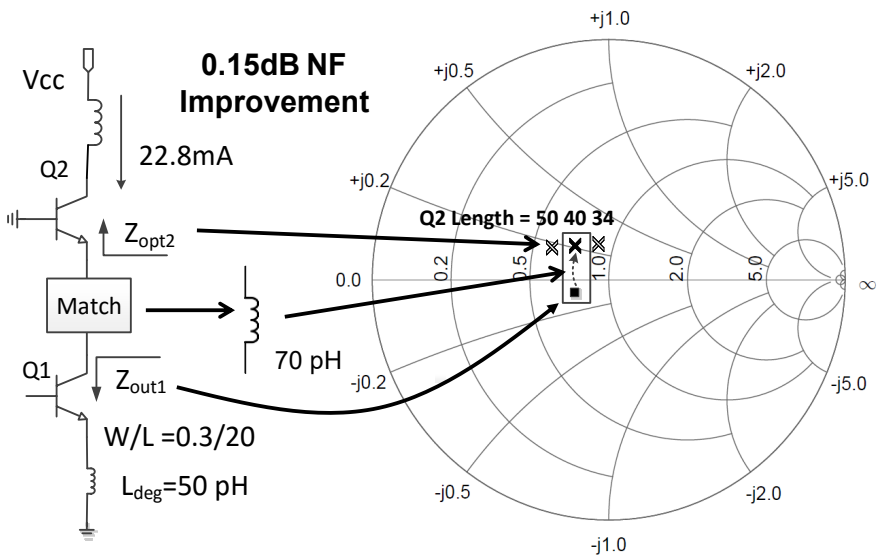


Figure 3-6. The design of noise matching network between CE and CB transistors.

3.1.3. Design of passive components and floorplan

To reach low noise figures, passive components with high Q values are required. The MIM capacitors provided by the technology offer a high-density capacitance with a Q around 50 at 30 GHz, which hardly degrades the NF performance of the LNA. The two remaining critical passive components are the integrated inductors and the interconnect. To reduce the loss mechanism of the inductors due to the substrate coupling, both metal shield and deep-trench-isolation (DTI) layer are added underneath the inductors. The presence of the grounded metal shield, however, introduces parallel parasitic capacitance and reduces the self-resonance frequency of the inductors. Since these effects depend on the physical layout and can hardly estimate precisely in the schematic, EM simulator (Agilent Momentum) is used to characterize the inductors and long interconnections.

In addition to the passive circuits, a proper grounding strategy in the floorplan and layout is required in order not to degrade the noise figure. Especially, single ended circuits at mm-wave frequencies are sensitive to the parasitic inductance from the grounding lines. In the proposed cascode LNA design, the parasitic inductance will degrade the gain, input matching and stability performance when presented at the emitter of the CE-transistor and the base from the CB-transistor. To obtain a well-defined small signal ground, a global ground plane is created around (with Metal-6) and beneath (with Metal-1) the complete circuit. The low impedance of the metal significantly reduce the impact of grounding inductance.

Finally, cross-talk due to undesired coupling might also negatively impact the performance. One effective way to reduce cross-talk is to increase the physical distance between the sensitive circuits, e.g. inductors from different stages. In the end, EM-simulators is used again to validate the overall post-layout performance of the circuit, which incorporate both the grounding and cross-talk effects.

3.2. Design I: A 2.1dB NF Single-Ended Ka-band LNA

3.2.1. Circuit Design

Figure 3-7 shows the schematic of the proposed single-ended Ka-band LNA. The first cascode stage is implemented by following the design procedure in Section 3.1. For measurement purpose, a second CE stage is added to provide the 50 Ω output matching. Meanwhile, the second stage offers additional power gain.

To ease the input matching, L_{deg} = 50 pH and L_e = 20 μm (for Q_1) are chosen to obtain $Re(Z_{in})$ close to 50 Ω. To reduce the base resistance, Q_1 is implemented with multiple finger configuration, i.e. 8 fingers with 2.5 μm per finger. Inductors L_{in}, L_{mid} in combination with L_t form the input matching network, which tunes out the parasitic capacitance at the input node and transforms the 50 Ω source impedance to the desired Z_{opt}. The size of Q_2 is selected to achieve the best noise matching between Q_1 and Q_2. The complete 1st stage has a G_a better than 10 dB, resulting a reasonable noise suppression of the 2nd stage. For instance, with NF_{stage1} = 2 dB and NF_{stage2} = 4dB, the NF of the complete LNA will be less than 2.4 dB. The inter-stage matching is realized by L_{O1}, C_{11}, and L_{11}, providing a reasonable noise and gain matching between the two stages. The second CE stage has a larger transistor size to deliver more output power and to improve output linearity. Inductor L_{deg2} represents the parasitic inductance between Q_3 emitter and the real RF ground. At the output of LNA, the filter network L_{21}, C_{21} and C_{22} enhances the bandwidth, meanwhile providing a 50 Ω output matching.

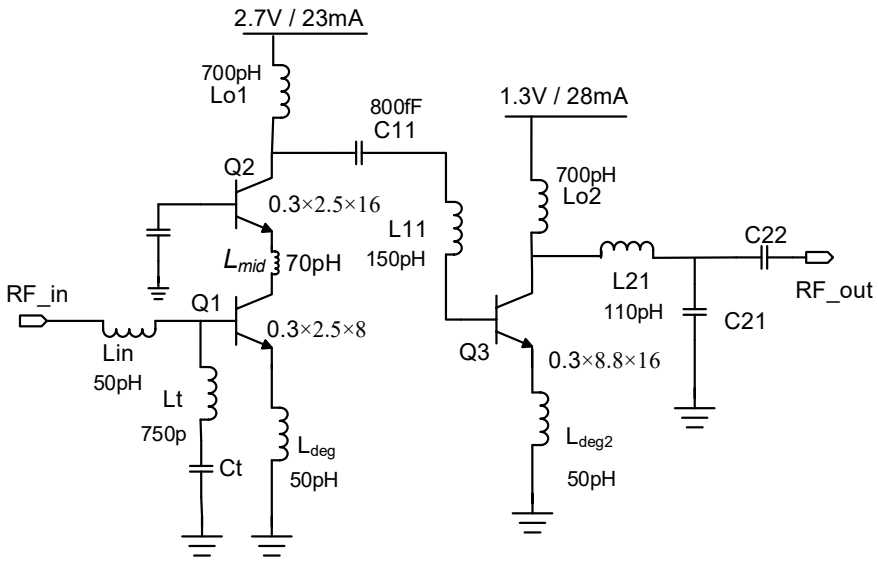


Figure 3-7. Proposed 2-stage LNA design, bias circuitry not shown.

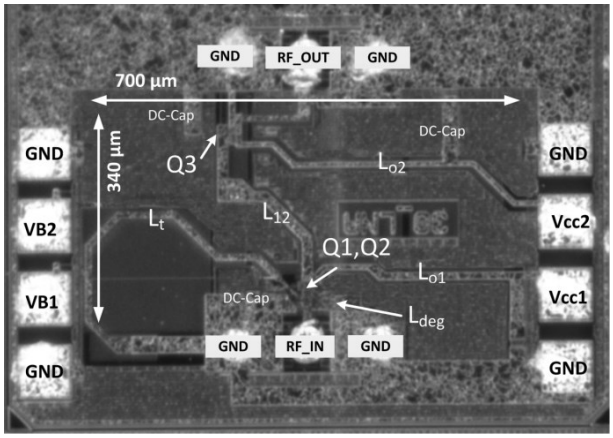


Figure 3-8. Die photo of the proposed Ka-band LNA.

Figure 3-8 shows the die photograph of the LNA. Instead of using spiral inductors, all the inductors are realized by metal lines in order to achieve higher quality factor (Q-factor). Note that the inductance L_{mid} is not obviously visible in the die photo because it is small (70 pH) and implemented by the parasitic inductance between Q_1 and Q_2, i.e. via inductance and interconnection wire inductance. To verify the layout performance, EM software Agilent Momentum has been used to simulate all the inductors, interconnects and bond pads. The total chip area including bond pads is 1.0×0.7mm^2. The input stage is biased at 23mA from a 2.7V voltage supply. The output stage consumes 28mA from a 1.3V supply and the total power consumption is 98mW.

3.2.2. Noise Parameter Measurement

Measurements have been performed on-wafer using a dedicated RF/mm-wave probe station. The characterization of the LNA has been done at room temperature.

In order to characterize the noise performance of the proposed LNA, the noise parameters are extracted using the Y-factor method in combination with a source tuner. The four noise parameters are F_{min}, Γ_{opt} and R_n, where F_{min} is the minimum noise figure of the two port network, R_n is the equivalent noise resistance

and Γ_{opt} is the optimal source reflection coefficient. By changing the source impedance connected to the LNA, the NF of the LNA varies as given by the well-known equation:

$$F = F_{min} + 4\frac{R_n}{Z_0}\frac{|\Gamma_S - \Gamma_{opt}|^2}{(1-|\Gamma_S|^2)|1+\Gamma_{opt}|^2} \tag{3.6}$$

where Z_0 is the characteristic impedance of the system, Γ_s is the actual source reflection coefficient connected to the LNA. Since the noise parameters cannot be directly measured, a set of noise figure measurements with different Γ_s have to be performed. Knowing that Γ_{opt} is a complex quantity, in principle only four measurements are enough to obtain the three noise parameters. However, to get a more reliable result, more measurements have been done. The basic noise figure measurement set-up is shown in Figure 3-9.

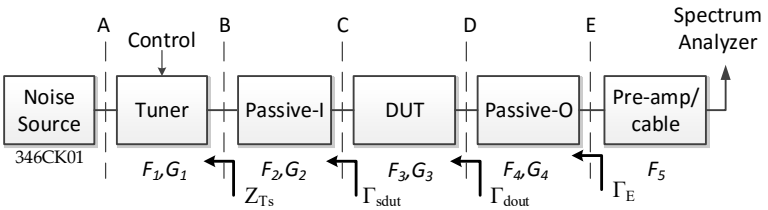


Figure 3-9. The basic scheme of Ka-band noise figure measurement setup.

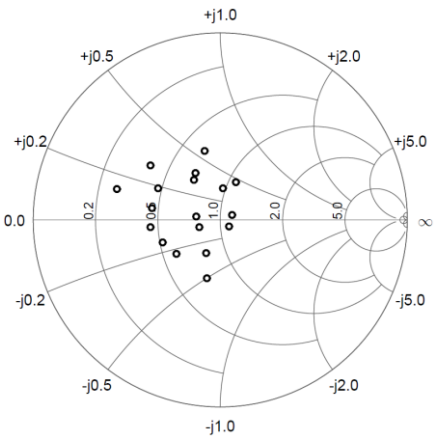


Figure 3-10. Measured source impedance Γ_{sdut} for 18 different tuner positions, plotted in the Smith chart.

At the input, a 346CK01 noise source from Agilent covers the whole Ka-band and has an excess noise ratio of 12.8 dB at 30 GHz. A MPT6080 impedance tuner from Focus is inserted in order to provide controllable source impedance for the DUT. The Block labeled Passive-I includes passives such as connecters, de-coupling capacitor, cable and input probe located between the tuner and the LNA (referred as DUT). At the output of the DUT, the block labeled Passive-O consists of the output probe and cable between the DUT and the input of the pre-amplifier. The pre-amplifier levels up the noise power at node E and make it significantly larger than the internal noise level of the spectrum analyzer.

As indicated in Figure 3-9, the input referred noise factor and available gain of each block are denoted as Fi and G_i (i = 1,2..,5). According to the Friis' formula, the total noise factor F_{tot} is given by:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \frac{F_5 - 1}{G_1 G_2 G_3 G_4} \tag{3.7}$$

To characterize F_i and G_i of each block, separate calibration and measurement have been performed over the frequency band 25-33 GHz. To begin with, the S-parameters of the DUT are measured by using the calibrated vector network analyzer (VNA), denoted as S_{dut}. The calibration is made on-wafer with a standard GSG calibration substrate, bringing the reference planes to C and D as shown in Figure 3-9. Without changing the configuration of the probe station, the noise source is calibrated with the spectrum analyzer to the reference plane E. Thus, the noise of the output path is removed, i.e. F_5=1. Note that this calibration only holds when Γ_E is close to 0. In this measurement, due to the losses in network D-E and small Γ_{dout} achieved by the DUT, Γ_E is smaller than 0.1 over the band of interest. Given 10 dB G_a from the DUT, the error due to $\Gamma_E \neq 0$ is negligible to the overall NF. With the calibrated noise source, 18 NF measurements have been performed with different tuner positions. The noise source is used in hot/cold mode and the total noise factor $F_{toti\text{-}mea}$ (i=1,2,…18) can be directly read from the spectrum analyzer with a known ENR table. Since the characterization of passives networks B-C cannot be done directly, two one-port calibrations are done, i.e. a coplanar short-open load (SOL) on-wafer calibration in reference plane C and mechanical standard SOL calibration in reference plane B. The S-parameters of the network B-C can then be calculated based on the data of two calibrations. The calibration of network D-E can be done in the same way. Finally, the S-parameters of 18 tuner positions can be obtained by measure the tuner separately

(see Figure 3-10). A good repeatability of the mapping between the tuner positions and achieved impedance is obtained by the tuner calibration.

With the data above, the noise parameters of DUT, F_{min}, Γ_{opt} and R_n can be solved by equation (3.6) and (3.7). Since the equations are not linear, for each frequency the optimal noise parameters are solved recursively based on the least square approach. The residue square error *(ER_{tot})* is expressed as:

$$\mathrm{ER}_{tot} = \sum_{i=1}^{18} \left(\frac{F_{toti-fit} - F_{toti-mea}}{F_{toti-mea}}\right)^2 \tag{3.8}$$

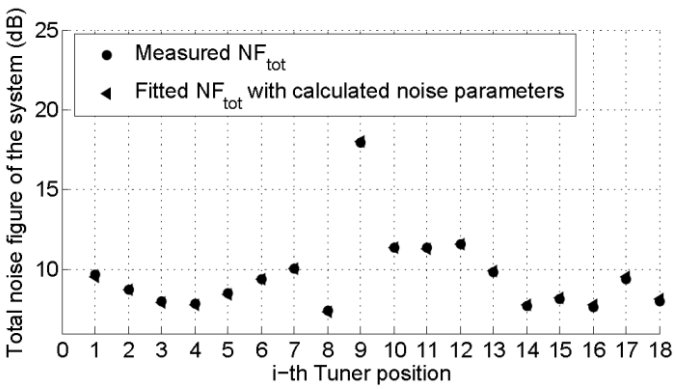


Figure 3-11. Comparison between the measured and fitted NF_{total} of the system at 30GHz.

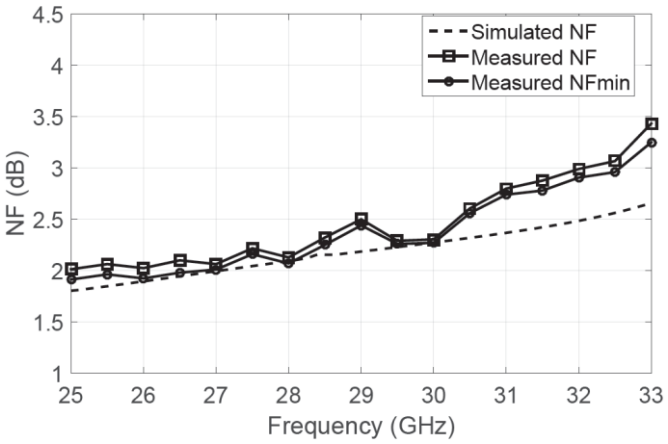


Figure 3-12. Measured NF and NF_{min} of the proposed LNA, compared with the simulated NF.

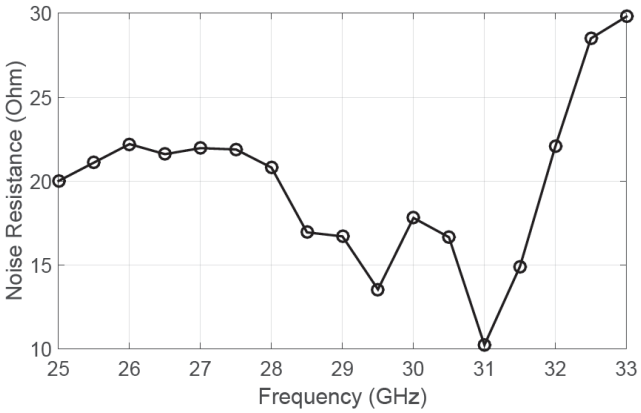


Figure 3-13. Measured noise resistance of the proposed LNA.

where $F_{toti-mea}$ and $F_{toti-fit}$ are respectively the measured and fitted total noise factor of the system for the *i*-th tuner position. By minimizing (3.8), the noise parameters of the DUT can be determined. Figure 3-11 shows the comparison between $\mathrm{NF}_{\mathrm{toti-mea}}$ and $\mathrm{NF}_{\mathrm{toti-fit}}$ at 30 GHz. A good fit indicates that the calculated noise parameters are reliable. It can be seen that the 9th tuner position results in a larger NF, this is because the 9-th tuner position results in a large output impedance, i.e. $353 + 240j$ at the DUT input, which is very far away from 50 Ω. As a result, the DUT have a much higher noise contribution. Figure 3-12 to Figure 3-13 show the noise parameters of the proposed LNA from 25 GHz to 33 GHz. A minimum 2dB NF is achieved around 25-28 GHz, and the NF at 30 GHz is 2.3 dB. Over the band of interest, NF_{min} and NF have a good fit, meaning that the proposed LNA achieves a good noise matching. The measured NFs fit well with the simulated NF up to 30 GHz. Above 30 GHz, the LNA presents a higher NF than expected. This could be explained by the fact that the measured gain of the LNA starts to drop quickly after 30 GHz (see Figure 3-14), e.g. at 33 GHz the measured gain drops to 5dB while the simulated gain is around 11dB.

3.2.3. S-parameters, linearity, and large-signal measurements

The measured input return loss and transducer gain (G_T) are shown in Figure 3-14. The LNA has a measured peak G_T of 12.8 dB at 27.6 GHz and 11.4 dB at 30 GHz. The 3dB-power bandwidth is from 25-31 GHz, covering the complete LMDS bandwidth. The input return loss is better than 10 dB in a bandwidth around the frequency of interest. The LNA is unconditionally stable from 18-40 GHz with a K-factor larger than 5.

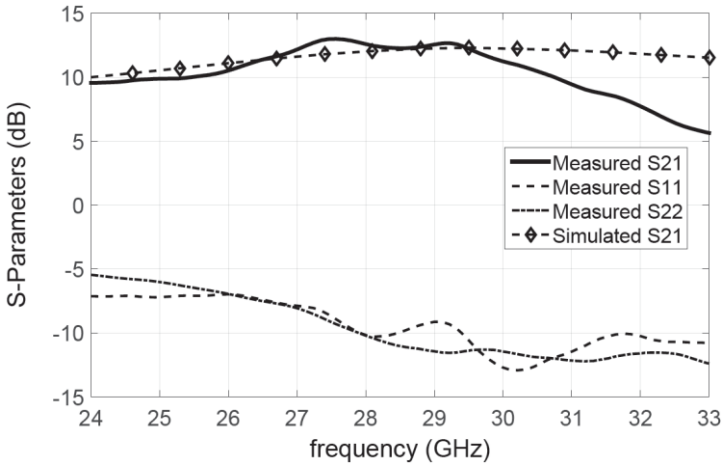


Figure 3-14. Measured S-parameters of proposed LNA.

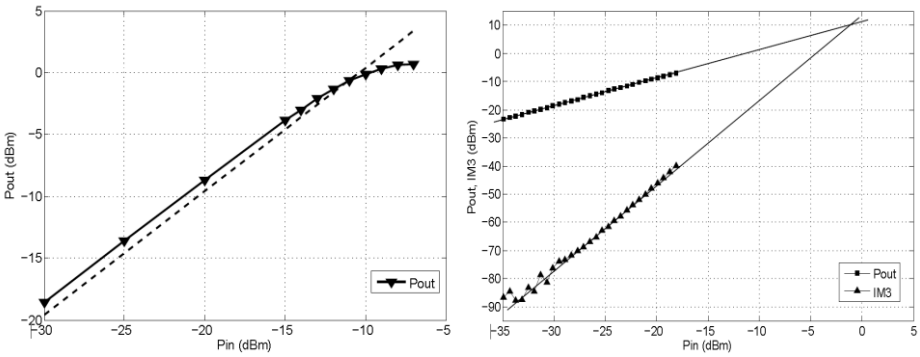


Figure 3-15. Measured Input 1dB compression point (left) and IIP3 (right) of the LNA

Figure 3-15 shows the large-signal behavior of the proposed LNA. The measured input 1-dB compression point (input P_{1dB}) is -11 dBm at 30 GHz. A two-tone measurement, with tones at 30 GHz and 30.1 GHz, reveals that the input 3rd-rder intercept point (IIP3) is -1.4 dBm and the OIP3 is +10 dBm, indicating a signal gain of 11.4 dB, in line with the s-parameter measurement results.

3.3. Design II: A 26dB Gain 2.2dB NF LNA with 10GHz Bandwidth

Although the single-ended LNA in design-I achieves a low NF, its relatively low gain could be an issue when integrated into a complete system. Suppose the

LNA is integrated with a passive RF phase shifter which presents 10 dB insertion loss, the LNA should provide at least 20 dB gain in order to obtain a reasonable frontend gain, e.g. 10 dB. Additionally, the LNA proposed in this section will provide a single-to-differential (S2D) conversion. The single-ended input enables it to interface with a single-ended antenna and eases the NF measurement, i.e. most of noise sources are single-ended. The differential output enables to design the following receiver blocks such as phase shifter, mixer in the differential form. Compared with single-ended circuits, the differential circuits provide well-defined virtual signal ground, which helps avoid grounding issues such as grounding inductance and undesired signal coupling through the ground plane.

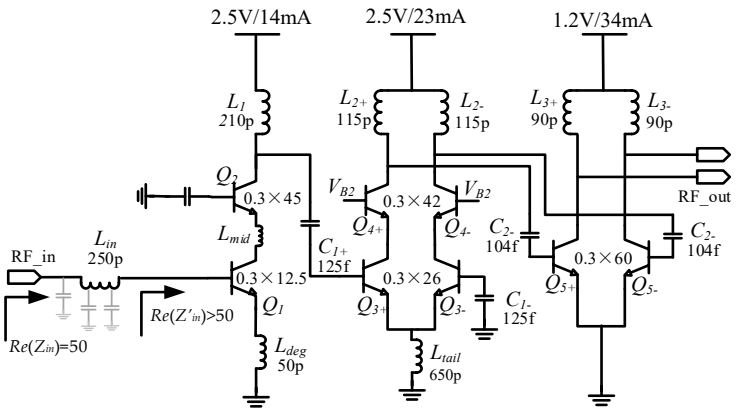


Figure 3-16. Schematic of the 3-stage high gain LNA (biasing circuitry not shown).

3.3.1. Circuit Design

Figure 3-16 shows the schematic of the proposed 3-stage high gain LNA (HG-LNA). The first stage of the LNA follows the procedure described in Section 3.1 to achieve low noise and good input impedance matching. Different from the LNA in design-I, the input parallel inductance L_t (see Figure 3-7) is removed to minimize the loss of the input matching network. The function of L_t in design-I is to tune out the parasitic capacitance from the bondpad and series inductance L_{in} (see Figure 3-16), which, if not turned out, will make $Re(Z_{in}) < Re(Z'_{in})$. Fortunately, with this known effect, a smaller emitter size of Q_1, i.e. $L_e = 12.5$ μm, can be chosen to achieve $Re(Z'_{in}) > 50\ \Omega$. As a result, the overall $Re(Z_{in}) = 50\ \Omega$ can be obtained at the input node of the LNA using a single series inductor L_{in}. For optimum noise performance, device Q_1 is biased at $I_{C1} = 14$ mA ($J_{optN} = 3.8$ mA/μm^2),

with which Q_1 exhibits 1.4 dB NF_{min} at 30 GHz. The size of Q_2 is chosen to optimize the noise matching between Q_1 and Q_2. Similar to design-I, L_{mid} is implemented as parasitic inductance, i.e. via inductance and interconnection wire inductance between Q_1 and Q_2.

The second stage serves as a gain stage and performs the S2D conversion. Instead of an active current source, L_{tail} is used as an RF choke to minimize the voltage drop. Ideally, L_{tail} is preferred to be as large as possible. However, in practice large L_{tail} results in large chip area and low self-resonance frequency. Therefore, L_{tail} is chosen moderately to be 650 pH, i.e. $122\ j\Omega$ at 30 GHz. Compared to the impedance seen from the emitter of Q_{3-}, i.e. $1/g_{m3-} < 5\ \Omega$, L_{tail} is large enough to minimize the leakage current through L_{tail}. The load inductors $L_{2\pm}$ and $L_{3\pm}$ are implemented as a single inductor with a center tap, connected to the supply voltage. The second stage is biased at I_{C2} = 23 mA to make sure it does not limit the overall ICP_{1dB}.

The last common emitter stage is mainly optimized for linearity performance and facilitates the output matching to ease measurements. Suppose the complete LNA is targeted to achieve 25 dB gain and an ICP of -15 dBm, the last stage has to be designed to handle +10 dBm output power. To increase the power efficiency, the knee voltage of Q_5 is minimized by choosing a large emitter size. As a result, with 1.2V supply voltage and 34 mA DC biasing current, the last stage achieves an output P_{1dB} above + 10dBm. The gain bandwidth of the LNA is controlled by two high-pass networks, i.e. L_1-C_1, L_2-C_2 and the output inductance L_3. By introducing three zero's below 30 GHz, the gain of the LNA is flattened over 10 GHz BW.

3.3.2. Measurement results

Figure 3-17 shows the die photo of the HG-LNA, which has a core area of 0.165 mm^2 (0.35 mm×0.47 mm). The small signal performance of the high power S2D LNA is measured by performing a 3-port S-parameters measurement (ports configuration shown in Figure 3-17), from which the S2D 2-port S-parameters are derived. For NF and linearity measurements, an external hybrid is used to convert the output into single ended.

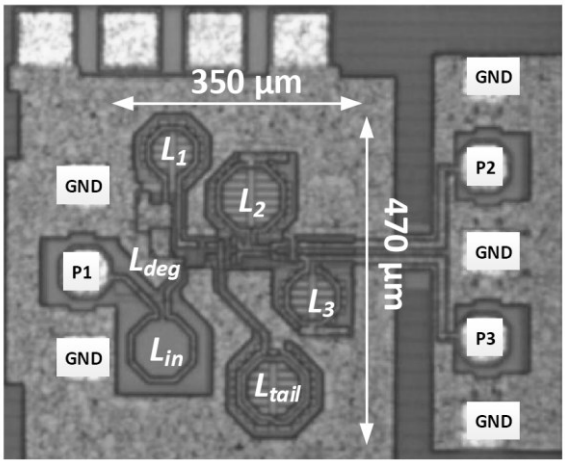


Figure 3-17. Die photo of the HG-LNA

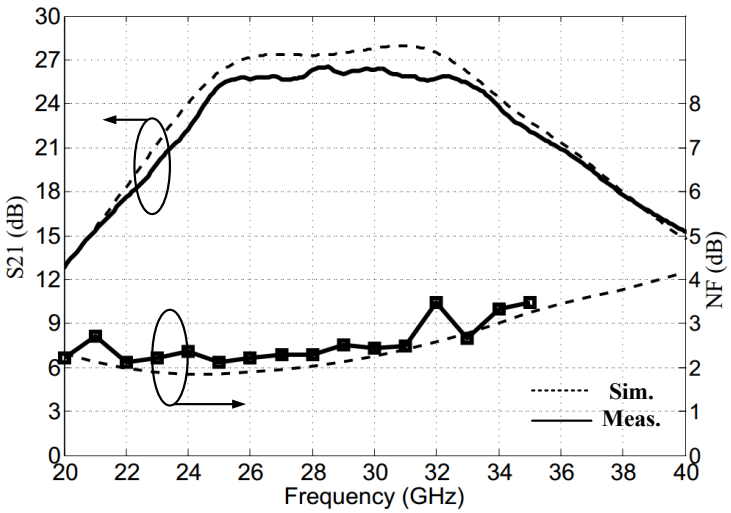


Figure 3-18. Measured gain and NF performance of the HG-LNA.

As shown in Figure 3-18, the measured LNA exhibits 26.4 dB flat gain around 30GHz with the -3dB gain bandwidth of 9.7 GHz from 24.3 to 34 GHz. The measured minimal in-band NF is 2.1 dB at 25 GHz and 2.5 dB at center frequency 29 GHz. Figure 3-19 shows the measured amplitude and phase imbalance at the differential output. The two differential outputs (P2 and P3 in Figure 3-17) have

a relative amplitude variation of less than 1dB and phase imbalance of less than 6 degrees (referred to ideal 180-degree phase difference).

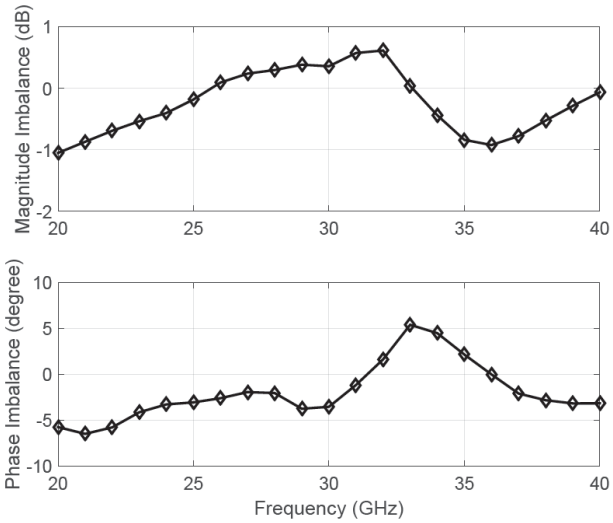


Figure 3-19. Measured magnitude and phase imbalance of the differential output.

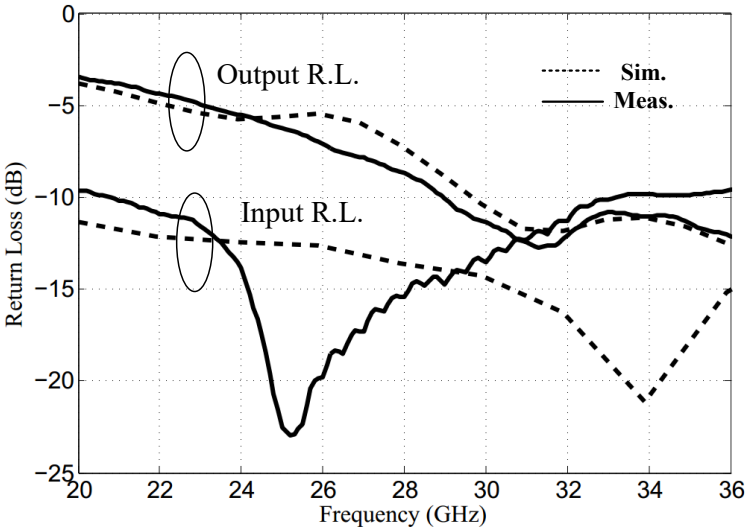


Figure 3-20. The measured return loss of the HG-LNA.

A broadband input matching is achieved with the in-band input reflection coefficient below -10 dB (Figure 3-20). Compared with the simulation, the measured input impedance resonates at a lower frequency, i.e. 25 GHz instead of 34 GHz. The frequency shift can be caused by the underestimation of the parasitic capacitance at the input, e.g. from the bond pad. In addition, since DTI is not included in the EM software when characterizing the input inductor L_{in}, the actual value of L_{in} can be larger than expected, resulting in a lower resonance frequency for S_{11}. The measured input P_{1dB} (output P_{1dB}) and IIP3 (OIP3) of the LNA at 30 GHz are -14.9 dBm (+10.5 dBm) and -5 dBm (+21.4 dBm) respectively at 134 mW power dissipation (see Figure 3-21). The two tone frequency offset for IIP3 measurement is 80 MHz.

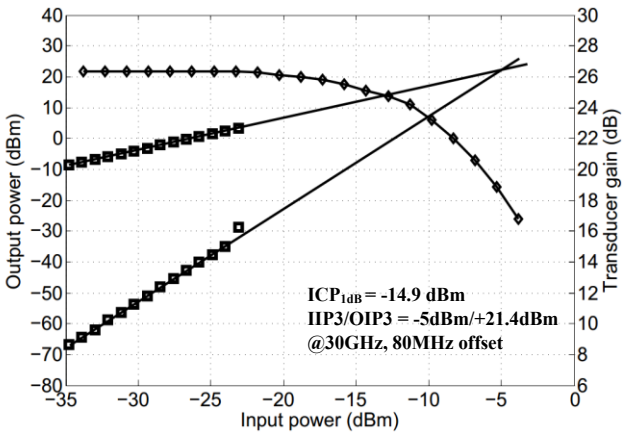


Figure 3-21. Measured IIP3/OIP3 and input P_{1dB} of HG-LNA at 30GHz.

3.4. Design III: A 20mW 2.6dB NF LNA with 10GHz Bandwidth

For some low power applications, a standalone LNA consuming more than 100 mW power could burden the power budget. Additionally, as a packaged silicon chip has a maximal power (heat) handling capacity, the LNAs proposed in design-I and II will limit the maximal number of array elements that can be integrated on one chip. Therefore, a relatively low-power LNA is proposed in this section, which makes a trade-off between power consumption and linearity,

while maintaining the other required specifications, such as NF, gain, and bandwidth.

3.4.1. Circuit Design

Figure 3-22 shows the schematic of the proposed low-power LNA (LP-LNA). The first two stages are inductively-degenerated cascode amplifiers, which are optimized for low noise, large bandwidth, and enough gain. The third stage of the LP-LNA is configured as common-collector (CC) stage, which offers almost constant output impedance over frequencies, i.e. $Z_{out} \approx 1/g_{m5}$. This is important when integrated together with a true-time-delay phase shifter, which needs to see a broadband source impedance (Z_{out} of the LNA) to minimize its delay error. We will elaborate on this point in Chapter 5. Instead of having S2D conversion in an earlier stage, the LP-LNA performs the S2D conversion at the output using a 1:1 transformer, resulting in a single-ended CC stage. This helps to reduce the current consumption of the LNA, because with the same voltage swing delivered to the same loading, the single-ended CC stage consumes only half of the DC current than using a differential CC stage. To further reduce current consumption, one can increase the load impedance seen by the CC stage. This can be achieved by using a high turn ratio transformer or an additional LC matching network. However, these solutions introduce extra loss. Besides, the LC matching network operates in a narrow band. Therefore, this does not fit in the wideband LNA design.

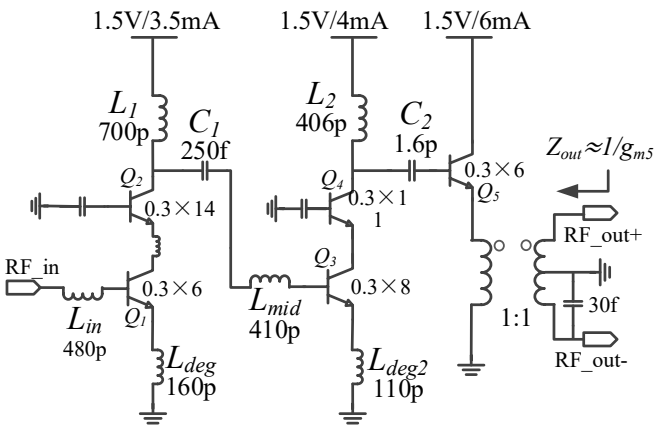


Figure 3-22. Schematic of the 3-stage LP-LNA (biasing circuitry not shown).

To reduce power consumption meanwhile keeping the first stage operate with a reasonable current density for f_t and noise performance, Q_1 is scaled down to 0.3×6 μm². The biasing current for Q_1 is chosen to be 3.5mA. Although the resulted emitter current density J_E =1.94 mA/μm² for Q_1 deviates from the optimum noise current density, i.e. J_{optN} = 3.8 mA/μm² (see Figure 3-2 and Section 3.1.2A), the NF_{min} of Q_1 only receives 0.15 dB penalty. In return, it halves the power consumption of the first stage. The down-scaling of the first stage also leads to larger values of L_{in} and L_{deg} compared to HG-LNA. To improve the Q-factor, both L_{in} and L_{deg} are realized by stacking the top two thick metals. At 30 GHz, L_2 and C_2 resonate with the parasitic capacitance at the collector of Q_4, making Q_4 directly loaded with the input impedance of the CC stage, i.e. approximately 150 Ω. The first two stages offer 20 dB gain at 30 GHz, meaning that Q_4 has to deliver 0 dBm output power to maintain an overall ICP of -20 dBm. With 0 dBm power delivered to the 150 Ω load, the second stage needs to source RF current with the magnitude of 3.7 mA. As a result, the second stage is biased at 4 mA to prevent Q_3 and Q_4 entering class-AB operation. Assume the transformer is ideal, the load impedance of the output CC stage is 100 Ω, which is 2/3 of the load impedance of the second stage. As a result, by duplicating the RF voltage from the output of the second stage, the CC stage has to handle 1.5 times of the RF current in the second stage, i.e. 1.5×3.7 mA = 5.6 mA. The last stage is therefore biased at 6 mA for fully class-A operation. Similar to the HG-LNA, the gain bandwidth of the LP-LNA is controlled by the inter-stage matching networks, i.e. L_1-L_{mid}-C_1 and L_2-C_2. Compared to only using a simple L_1-C_1 matching network, matching with L_1-L_{mid}-C_1 has more freedom for bandwidth control and results in more broadband impedance transformation. Due to the imbalanced parasitic capacitance to the substrate, the S2D transformer suffers from a certain common mode signal at the differential output. This is compensated by the additional 30 fF capacitance added between the negative output path and the ground path (Figure 3-22).

3.4.2. Ka-Band Low Noise Amplifier Measurement Results

Figure 3-23 shows the die photo of the LP-LNA, which has a core area of 0.2 mm² (0.49 mm×0.41 mm). The LP-LNA is measured using the same setup as in HG-LNA measurement. As shown in Figure 3-24, the LNA exhibits a peak gain of 25.3 dB at 31.5 GHz with the -3dB gain bandwidth of 10 GHz from 25 to 35 GHz. The measured minimal in-band NF is 2.45 dB at 25 GHz and 2.7 dB at center frequency 30.5 GHz.

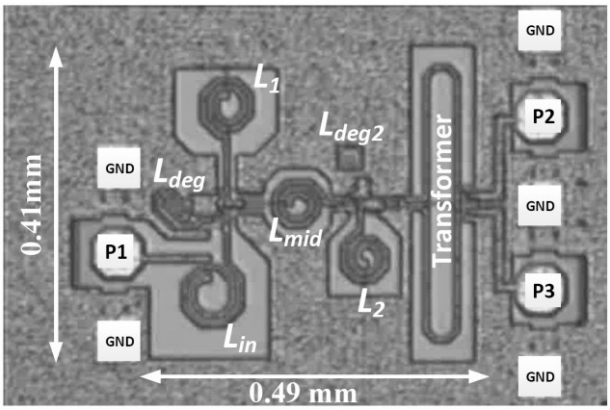


Figure 3-23. Die photo of the LP-LNA.

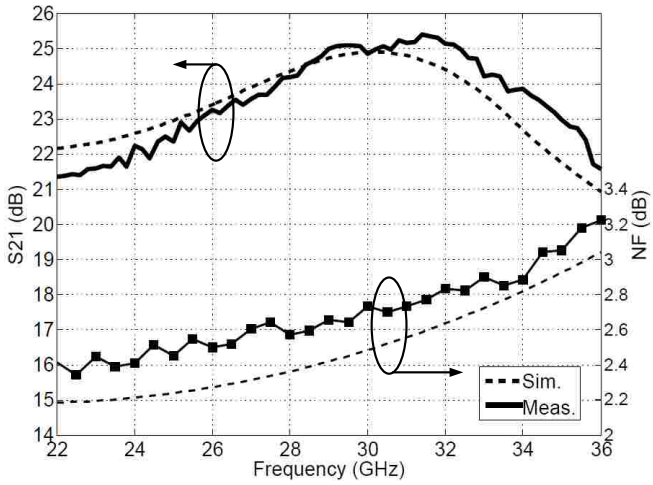


Figure 3-24. Measured S-parameters and NF of the LP-LNA

The slightly increased NF compared to the HG-LNA in design-II is mainly due to the extra loss of the input matching network. As shown in Figure 3-4, with small device size, the input impedance of the LNA is far from 50 Ω. As a result, a large impedance transformation ratio is required for the input matching network, which introduces more loss and increases the NF.

Figure 3-25 shows the measured amplitude and phase imbalance of the differential output of the LP-LNA. The relative amplitude variation is less than 0.6 dB and the phase imbalance (referred to ideal 180-degree difference) is less than 7 degree.

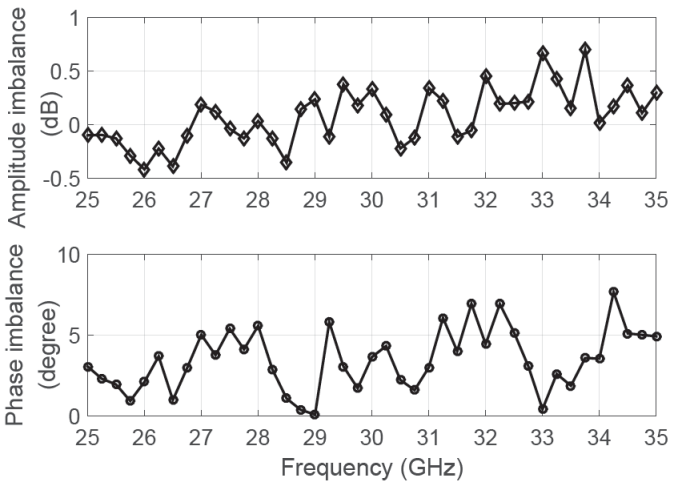


Figure 3-25. Measured amplitude and phase imbalance at the LP-LNA differential output.

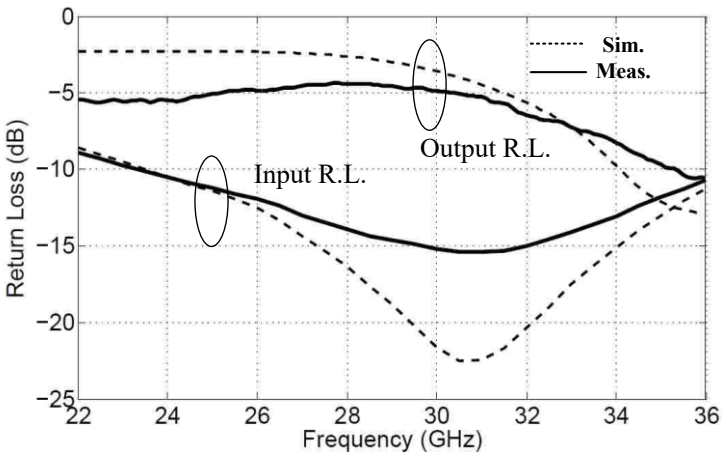


Figure 3-26. The measured return loss of the LP-LNA.

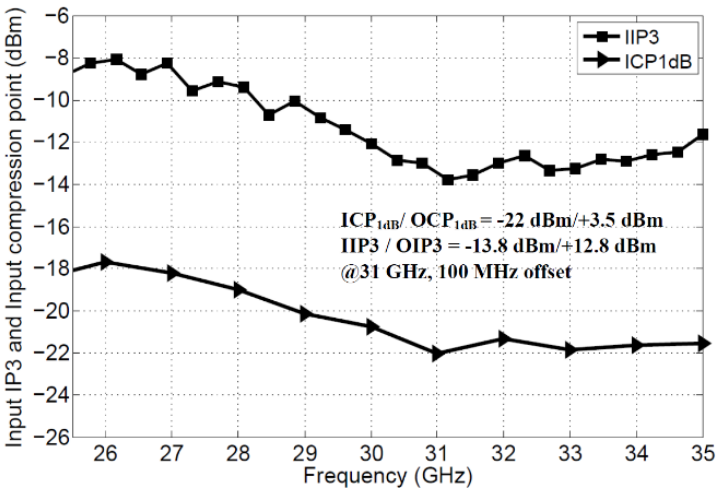


Figure 3-27. Measured IIP3 and input P_{1dB} of the LP-LNA.

As shown in Figure 3-26, a broadband input matching is achieved with the in-band input reflection coefficient below -10 dB. The complete LNA consumes 20.3 mW (13.5 mA, 1.5 V). Figure 3-27 shows the measured linearity and large signal performance of the LP-LNA over the entire gain bandwidth. The worst-case measured input P_{1dB} (output P_{1dB}) and IIP3 (OIP3) of the LNA at 31 GHz are -22 dBm (+2.1 dBm) and -13.8 dBm (+11.3 dBm) respectively. The two tone frequency offset for IIP3 measurement is 100 MHz.

3.5. Conclusion and discussion

Three alternative Ka-band LNAs have been realized using a 0.25 μm SiGe:C BiCMOS process. Table 3-1 shows the benchmarking which compares the proposed 3 LNAs to other published Ka-band LNAs. It is seen that the proposed LNAs have the best reported NF for silicon-based technologies.

Regarding the power dissipation, the proposed LNAs in Design-I and II have a relatively large power consumption compared to the other designs, because these 2 LNAs are supposed to be used in applications where high input P1dB is required, e.g. with strong interferences that may desensitize the LNA. With a certain gain requirement, a high output P1dB must be achieved. The LNA in [23] achieves better ICP1dB with lower power dissipation but with lower gain (i.e. lower OCP1dB) and higher NF. It is interesting to observe the trade-off between

output P1dB and power consumption by comparing design-II and III. It is seen that the power consumption of the LNA in design-II is 6.6 times (about 8.2 dB) of that in design-III, while its output P1dB (+10.5 dBm) is 8.3 dB higher than the counterpart in design-III (+2.3 dBm), i.e. almost dB-to-dB trade-off. However, this is not valid when comparing design-I and II, where the output P1dB of design-I is about 10 dB lower than in design-II but still has a comparable power consumption. It reveals that the devices in design-I (especially in the output stage), are not operating as efficient as in design-II and III.

Table 3-1. Performance summary and the benchmarking with other Ka-band LNAs.

	Tech-nology	Freq. (GHz)	BW (GHz)	Peak Gain (dB)	Minimum In-band NF (dB)	Average In-band NF (dB)	ICP_{1dB} (dBm)	IIP3 (dBm)	Power (mW)
Design-I	**0.25µm SiGe**	**25 - 31**	**6**	**12.8**	**2.05**	**2.2**	**-11**	**-1.3**	**98**
Design-II	**0.25µm SiGe**	**24.3 - 34**	**9.7**	**26.4**	**2.1**	**2.4**	**-14.9**	**-5**	**134**
Design-III	**0.25µm SiGe**	**25 - 35**	**10**	**25.3**	**2.45**	**2.7**	**-22**	**-13.8**	**20.3**
[21]	0.12µm SiGe	30 - 37	7	23.5	2.6	2.8	-28	-19.5	11
[23]	90nm SOI	26 - 42	16	12	3.6	3.8	-7	N/A	41
[24]	65nm CMOS	21 - 26	5	15.2	2.7	3.1	N/A	-5.4	7
[25]	0.25µm SiGe	25 – 31	6	10.4	6.4	6.6	N/A	N/A	7.9
[26]	0.18µm SiGe	23 – 32	9	12	4.5	5.1	N/A	-5.5	13
[27]	0.15µm InGaAs	23 - 30	7	14.5	1.75	1.8	N/A	N/A	37.5

4. Active True-Time-Delay Phase Shifter and Receiver Frontend

4.1. Introduction

As discussed in Section 2.2, a true-time-delay (TTD) phase shifter is required in order to perform broadband beamforming. Various TTD techniques have been explored in the literature. Photonic TTD modules [28] and MEMS-based TTD phase shifters [29] exhibit low delay variation (DV) over a large BW, low insertion loss, and large total variable delay. However, these solutions are not suitable for integrated and low-cost systems. Within the integrated TTD solutions, switched transmission line (TL) [12-14] and switched LC-network [11] are most commonly used techniques as they have low power dissipation and high linearity. However, more than 10% normalized delay variation (NDV) over the BW can be observed in these implementations. Besides, to achieve large total variable delay, these techniques usually occupy a large chip area. There are also active TTD solutions proposed based on RC or g_m-RC filters [15, 16] which achieve large variable delay within a small die area. Especially in [8], the resulted NDV is less than 4%. However, these techniques are only explored at frequencies below 10 GHz.

In this Chapter, a delay variation cancellation technique will be introduced, with which the proposed active TTD phase shifter achieves a flat delay response over 20-40 GHz with only 6.6% NDV. To improve gain and suppress the overall NF, a TTD frontend is also implemented by integrating a high gain LNA in front of the TTD phase shifter.

4.2. Delay Variation Cancellation Theory

Section 2.3.3 shows that the two types of the lumped delay cells, i.e. LC delay cell and G_m-RC delay cell, can both be considered as low-pass filters (LPF), which have limited cut-off frequency. As a result, the phase response of these lumped delay cells can approximate the TTD up to a limited frequency, beyond which delay variations (DV) will be present.

Fortunately, as shown in Figure 2-10, the delay patterns of the two types of delay cells are opposite to each other. The delay of the G_m-RC delay cell compresses as the frequency increases, while the delay of the matched LC π-network offers an expansion behavior. As a result, by cascading the two types of mechanism in a proper way, the expansion and compression behavior can cancel each other and a flat delay response will be achieved over a large frequency band. This mechanism is called the DV-cancelling technique in the following discussion.

To demonstrate the impact of the DV cancellation, 3 different cases are evaluated. As shown in Figure 4-1, these are respectively a single stage LC π-network (a), a single stage Gm-RC delay cell (b), and a combined structure by cascading the LC and G_m-RC cells (c). Figure 4-2 shows their simulated delay responses. It can be seen that although the original LC and G_m-RC delay cells present 13.8% and 21.8% NDV, the cascaded structure internally cancels the individual NDV and the overall NDV can be as low as 1.57% up to 60 GHz.

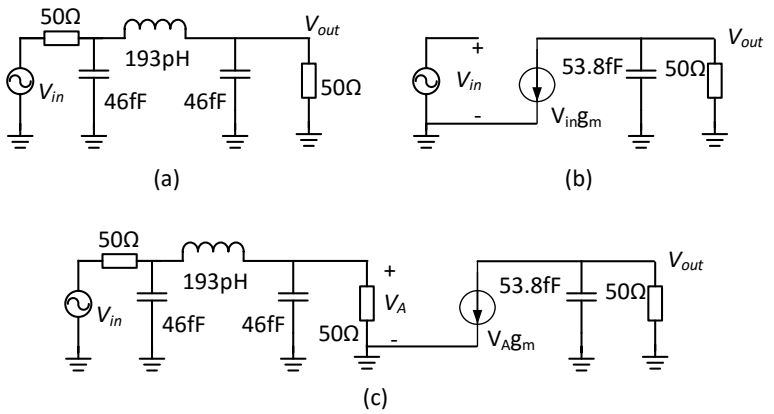


Figure 4-1. Simplified schematic of (a) single stage LC π-network (b) single stage G_m-RC cell and (c) cascaded LC and G_m-RC delay cells.

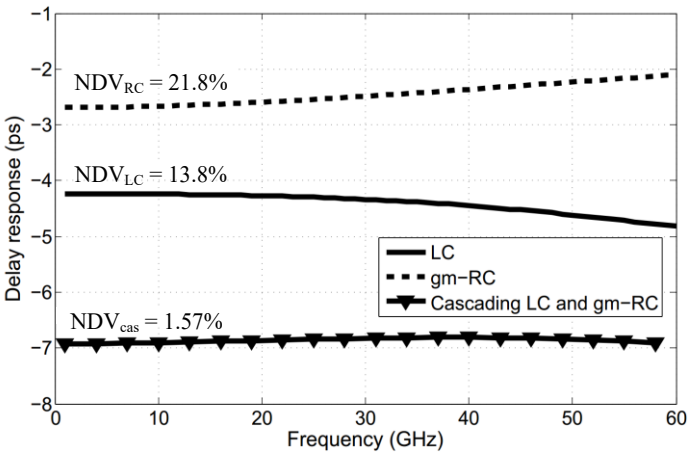


Figure 4-2. Delay variation canceling: simulated delay response of the single stage LC delay cell, single stage g_m-RC delay cell, and the cascaded delay cells (with parameters in Figure 4-1)

4.3. 20-40GHz Active True-Time-Delay Phase Shifter

4.3.1. Architecture

The proposed TTD phase shifter is targeted to achieve a total variable delay of 12 ps, i.e. the relative delay between two receiver channels will then range from -12 ps to 12 ps. This enables a 2-element beam former with 5 mm antenna spacing (30 GHz) to perform -45 to 45-degree beam scanning, enough for most K_a-band applications. To reduce the NDV, the DV canceling technique is employed.

Figure 4-3 shows the block diagram of the proposed fully differential TTD phase shifter (figure shows single-ended implementation for simplicity). To perform a delay variation cancellation, the required delay is generated by cascading varactor-loaded LC-networks with G_m-RC delay cells. The N-stage G_m-RC cells, each with a fixed delay τ_D and unit-gain, perform the coarse delay tuning. Switches k_1, k_2… k_N are acting as path selectors to control the coarse delay with a time step τ_D. G_m-RC cells that are bypassed by the switches are turned off to reduce power consumption. Since the first G_m-RC cell has to be activated all the time, the N-stage G_m-RC cells generate a variable delay $(N\text{-}1)\tau_D$. The LC-delay cell, composed by the M-stage cascaded LC π-networks, performs a continuous fine tuning with a total variable delay of τ_f ($\tau_f \geq \tau_D$). As a result, the total continuously

variable delay is $\tau_f + (N-1)\tau_D$. As the Gm-RC cells are inductorless, the maximal variable delay of the proposed structure can be extended by cascading more Gm-RC cells in a compact way. Signals from different channels are summed in current domain at node RF_{out}.

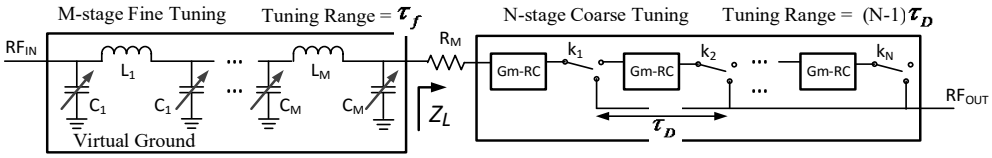


Figure 4-3. Block diagram of the proposed differential TTD phase shifter (plotted in single-ended form for simplicity)

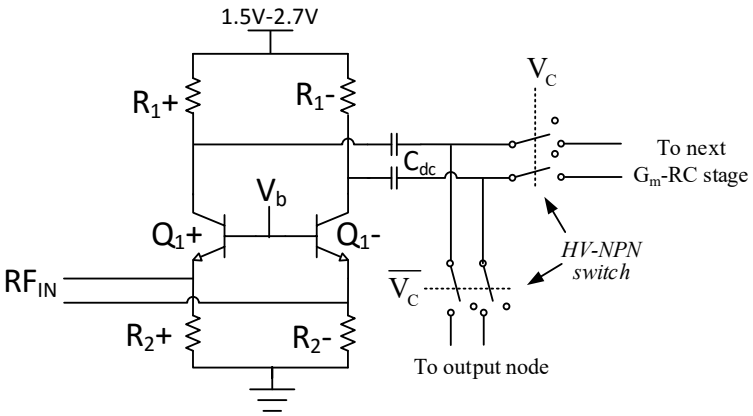


Figure 4-4. Schematic of Gm-Cells (bias not shown)

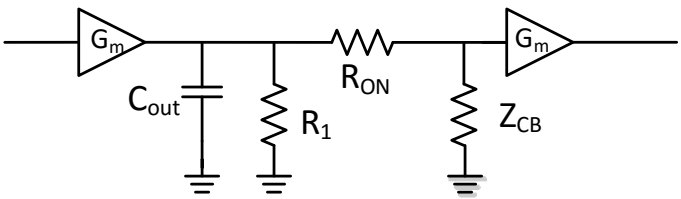


Figure 4-5. Composition of *R'C'* at the output of Gm-cell

With a fixed total variable delay, increasing the number of stages cascaded in the LC and Gm-RC cells, i.e. *M* and *N*, will reduce the implemented delay per stage.

For the fine tuning part, it can help to reduce the gain variation and input impedance variation over the delay tuning. For the coarse tuning part, as shown in Figure 2-11, reducing implemented delay per stage can reduce NDV of G_m-RC cells. However, larger N and M will result in larger chip area and power consumption. A trade-off has been achieved by choosing M = 3 and N = 3, which yields τ_D= 4 ps. As a result, with $\tau_f \geq 4$ ps, the phase shifter can perform 12 ps continuous variable delay.

4.3.2. Gm-RC Cells Design

The G_m-cell is implemented by a common-base (CB) differential amplifier (Figure 4-4). RF chokes are realized by resistors R_1 and R_2 instead of inductors to keep the structure compact. Each path-selecting switch $k_{1,2,...N}$ in Figure 4-3 is implemented as HV-NPN device with control voltage V_C (Figure 4-4). Capacitance C_{dc} acts as a DC blocking capacitor. To generate 4 ps delay per stage, the equivalent parallel resistance R' and capacitance C' at the output node of G_m-cell should satisfy $R'C'$=4ps. As shown in Figure 4-5, this $R'C'$ is mainly composed out of the output capacitance of G_m cell (C_{out}), the load resistor (R_1), series resistance of switches (R_{ON}) and the input impedance of next G_m-RC stage (Z_{CB}). As the load of the G_m cell is approximately equal to $1/G_m$, the gain of each G_m-RC stage is close to unity. In reality, however, all kinds of lossy mechanism results in 2-3 dB insertion loss per G_m-RC stage, resulting in large amplitude variation over the coarse delay tuning. To mitigate this issue, the switches $k_{1,2,...N}$ in Figure 4-3 are sized differently, keeping the overall insertion loss constant over the coarse delay settings.

Due to the CB structure, the input impedance of G_m-RC cells are low, i.e. < 10 Ω. As a result, the G_m cells, which should operate in Class-A mode, have to be biased with a large DC current in order to maintain a high input P_{1dB}. To make a flexible trade-off between power dissipation and linearity performance, the G_m-RC cell is designed to be able to operate at a wide range of supply voltages, i.e. from 1.5 V to 2.7 V. As a result, the overall TTD phase shifter can adjust its power consumption depending on the linearity requirement of the application. When operating at lower supply voltage, it is important to avoid Q_1 entering saturation region. This is achieved by proportionally downscaling the biasing current of the device, which reduces the voltage drop across R_1 and R_2. As the biasing current changes, the G_m value of the device changes as well, which have an impact on the gain and totally delay response. Fortunately, due to the proposed DV

cancellation mechanism, the degradation of the overall TTD performance is marginal. Each differential G_m-RC stage in high power mode (2.7V) draws 27 mA, and in low power mode (1.5 V) consumes 11 mA. Depending on the delay settings, the biasing of the un-used G_m-RC cells can be turned off, i.e. by turning off V_b in Figure 4-4, in order to save the power dissipation. The simulated worst-case delay variations of the complete G_m-RC cells are 1.3 ps and 1.5 ps respectively in high and low power modes over 20-40 GHz frequency band.

4.3.3. Design of LC delay cell

Figure 4-6 shows the implemented 3-stage LC fine tuning delay cells. As the G_m-RC stage has a low input impedance ($1/G_m$), the LC cells are preferred to have a low characteristic impedance (Z_0) as well in order to ease the inter-stage impedance matching. This results in a small inductance L_1 and a large varactor C_{var}, i.e. $Z_0 \approx \sqrt{L_1/2C_{var}}$. However, a too large varactor can give two issues. First, it introduces large parasitic capacitances, which degrades the delay tuning ability. Moreover, as the insertion loss of the varactor varies as its capacitance changes, a larger varactor results in larger amplitude variation during fine delay tuning. As a result, a trade-off has been made to have the single-ended $Z_0 \approx 24\ \Omega$. To achieve $\tau_f \geq 4$ ps, L_1 is designed to be 120 pH, and the single-ended capacitance C_{var} varies from 130 fF to 190 fF. This results in a continuous variable delay of 4.3 ps, covering the 4 ps coarse delay tuning step. As the 4.3 ps variable delay is distributed into 3 stage, the characteristic impedance of the LC cells is only slightly affected during the capacitance tuning, i.e. from 23 Ω to 25 Ω. This reduces the variation of the input impedance matching as well as the amplitude variation over the fine delay tuning.

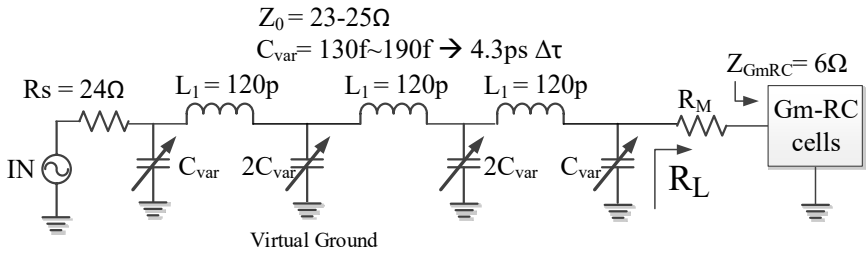


Figure 4-6. Design of LC fine tuning stages

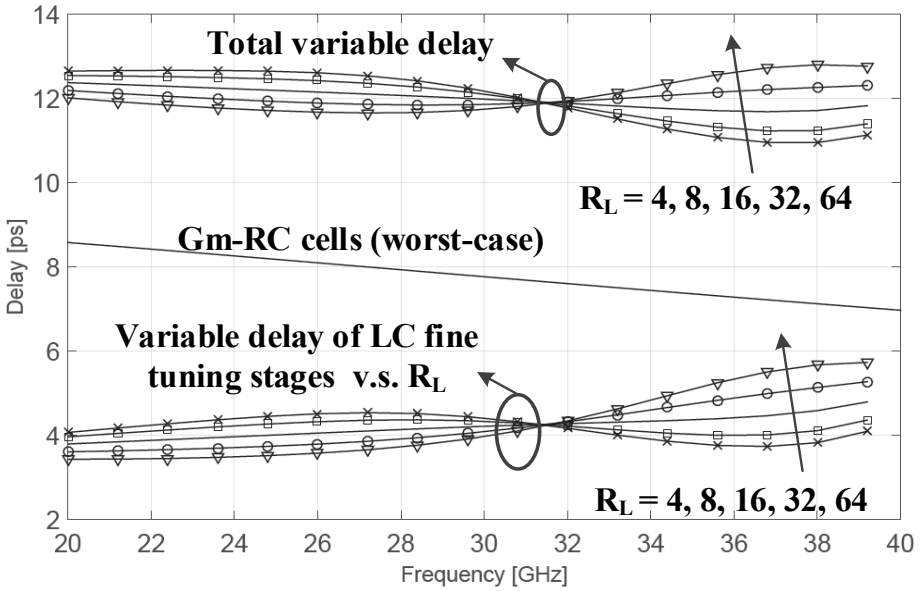


Figure 4-7. Optimization of R_L value to perform DV cancellation, the R_L impedances are based on single-ended values.

As the delay pattern of the LC π-network also depends on its load impedance, R_L, shown in Figure 4-6, has to be optimized in order to get the best DV canceling performance. As shown in the lower part of Figure 4-7, with different R_L values (based on single-ended values), the variable delay response of the LC fine tuning stages part varies. With the known delay response of the Gm-RC cells (the worst DV case), the overall variable delay response of the active TTD phase shifter can be estimated (see the upper part of Figure 4-7). It can be seen that the best DV cancellation can be achieved with a single-ended R_L value around 16 Ω.

With CB configuration, the single-ended input impedance of a Gm-RC stage (Z_{GmRC}) is about $1/G_m \approx 25mV/(I_C/2) = 50mV/I_C$, where I_C is the biasing current of a differential Gm-RC cell. Depending on different supply voltages, I_C ranges from 11 mA to 27 mA, resulting in Z_{GmRC} ranges from 1.9 Ω to 4.5 Ω. In reality, due to the impact of R_I and metal resistance, Z_{GmRC} is slightly larger, i.e. 4.5-7 Ω. As a result, to achieve the optimum R_L =16 Ω, a 10 Ω series resistor R_M is added in series with the Gm-RC cells.

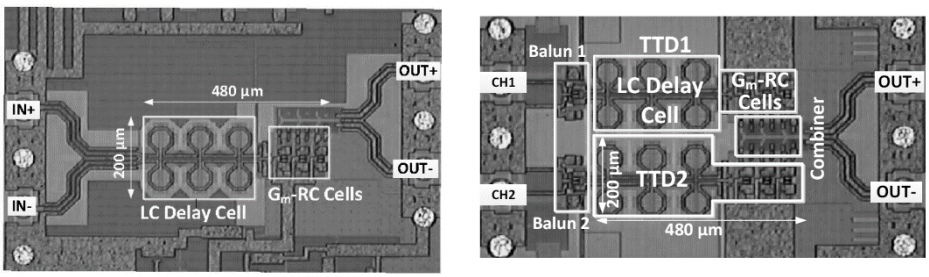


Figure 4-8. Die photos of (a) single channel active TTD phase shifter, and (b) two-channel active TTD beamformer

4.3.4. Measurement Results

Figure 4-8 shows the die photos of the implemented single channel active TTD phase shifter and two-channel active TTD beamformer. Both are fully differential circuits. The two channel version includes a passive combiner at the output, as the output signal of the Gm-RC stage is already converted in the current domain. To simplify the measurement, the two channel version also includes an active balun at the input of each channel in order to perform the S2D conversion. The power dissipation (P_{diss}) of the phase shifter depends on the value of the realized delay. Denote P_D as the power consumed by each Gm-RC cell, then the maximum P_{diss} of the 2-channel beamformer is $4P_D$, i.e. with one channel activating three Gm-RC cells and the other channel turning on one Gm-RC cell. This leads to an effective average P_{diss} per channel of $2P_D$, which in high power mode equals to 146 mW, i.e. 2×27 mA×2.7 V, and in low power mode is 33 mW, i.e. 2×11mA×1.5 V.

S-parameters measurement of the single-channel phase shifter has been performed with different supply voltages. With the supply voltage varying from 1.5 V to 2.7 V, the realized phase shifter presents similar performance regarding S_{11}, delay and gain variation. Taking V_{CC} = 2.7 V as an example, Figure 4-9 shows the measured relative delay response for different delay settings. To evaluate the flatness of the achieved delay response, Figure 4-10 shows the fitted Gaussian distribution function of the worst-case normalized delay variation (NDV_{PS}) over 13 circuit samples. The results show an average NDV of 0.77 ps ($\sigma < 60\,fs$) within a 20 GHz frequency band, and of only 0.36 ps ($\sigma < 35\,fs$) within a 10 GHz frequency band. As shown in Figure 4-11, the core of the phase shifter presents an available gain G_a of -10.5±0.9 dB dB at 30 GHz and almost constant input

impedance, i.e. $|S_{11}| < -15$dB for all delay settings. The large signal performance of the phase shifter, as expected, changes as a function of supply voltage, i.e. power dissipation. As shown in Figure 4-12, the measured worst-case input P_{1dB} and IIP3 at 30GHz are +9.7 dBm and +18 dBm in high power mode and are +3.6 dBm and +13 dBm in low power mode.

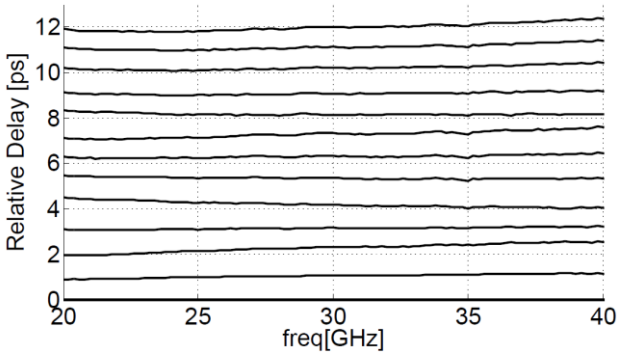


Figure 4-9.Relative delay response for different delay settings (V_{CC} = 2.7 V).

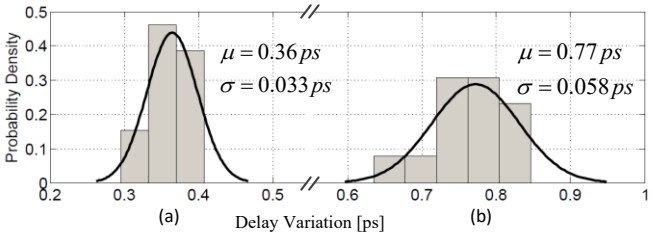


Figure 4-10. Fitted Gaussian distribution of worst-case delay variation over 13 samples within (a) 25-35GHz (b) 20-40GHz (V_{CC} = 2.7 V).

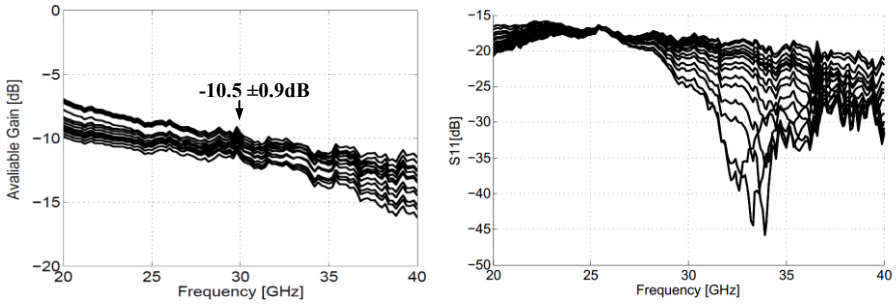


Figure 4-11. Measured available gain (left) and input return loss (right) of the active TTD phase shifter over different delay settings (V_{CC} = 2.7 V).

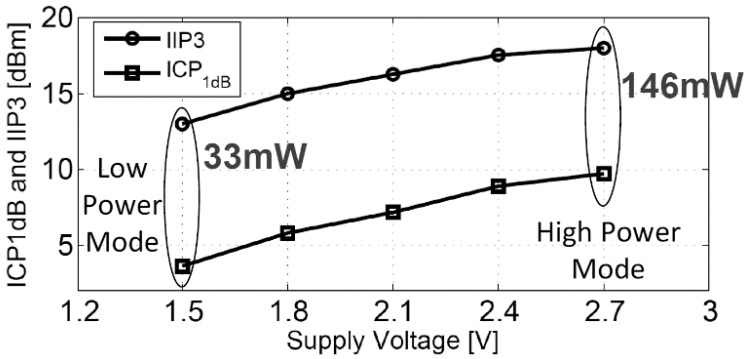


Figure 4-12. Measured worst-case input P_{1dB} and IIP3 at 30GHz versus different power supply.

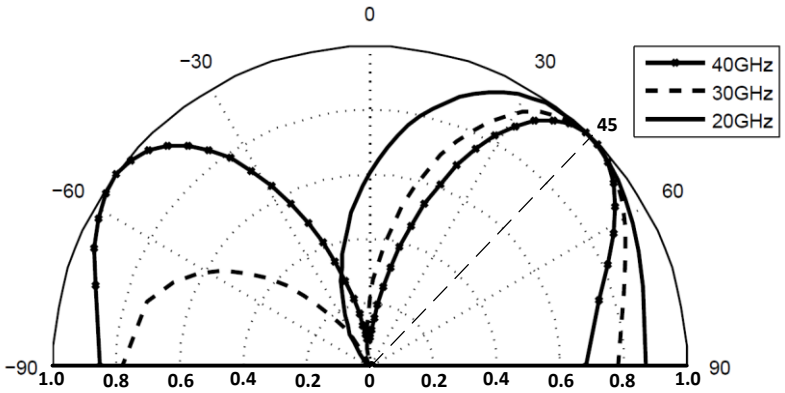


Figure 4-13. Normalized beam pattern of 2-channel beamformer

The two-channel TTD beamformer (Figure 4-8b) consists of two identical TTD phase shifters as in the single-channel version. On-chip active baluns are used to perform single-to-differential conversion from the two single-ended channel inputs. At the output, signals from two channels are summed in current domain via a microstrip-line based passive combiner which also acts as a part of output matching network. To evaluate the beam pattern of the 2-channel beamformer, taking into account of the coupling between channels, a full 3 ports S-parameters measurement is performed for different delay settings, i.e. single-ended port 1 and 2 for two channel input and differential port 3 at the output. Figure 4-13. shows the normalized array pattern for the 2-channel beamformer for maximal delay setting (in high power mode), which is synthesized from the measured 3-

port S-parameters. It is seen that signals with 20GHz frequency difference simultaneously reach their optimum at a signal angle of 45° without obvious beam-squinting.

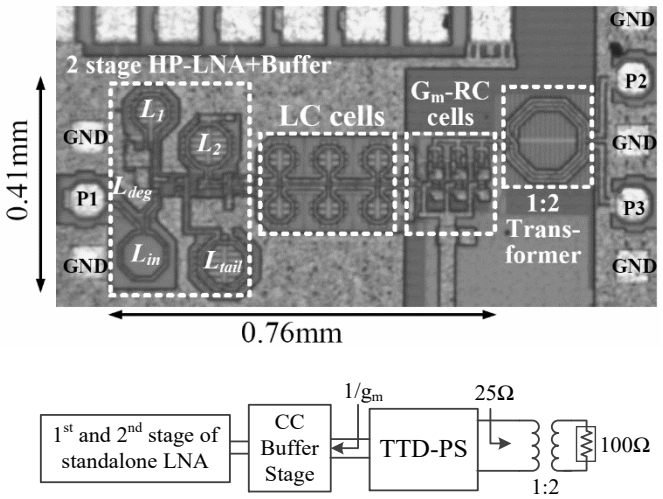


Figure 4-14 Die photo and architecture of the high power TTD receiver front-end (HG-LNA/active TTD).

4.4. 25-35GHz High Power Phased Array Receiver Frontend

4.4.1. Architecture

Figure 4-14 shows the die photo and the architecture of the high power TTD receiver front-end, which consists of the proposed HG-LNA (Design-II in Section 3.3) and active TTD phase shifter. The complete front-end has a core area of a core area of 0.31 mm² (0.76 mm×0.41 mm). To reduce the DV of the TTD phase shifter, both the input and the output of the active TTD phase shifter need to be terminated with frequency independent impedances, e.g. broadband real impedances. At the input of the TTD, this is achieved by replacing the last CE stage of the HG-LNA by a common-collector (CC) buffer stage. Although this modification slightly reduces the gain of the LNA, it provides almost a constant source impedance over the frequency for the TTD-PS, i.e. $Z_s \approx 1/g_{mCC}$, where g_{mCC} is the

transconductance of the CC buffer stage. At the output of TTD, the output matching network is implemented using a broadband 1:2 transformer.

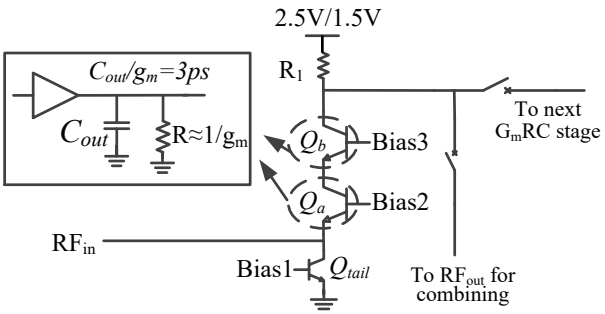


Figure 4-15. Improved implementation of the G_m-RC cells in front-end design for larger realized delay per stage (plotted in single-ended form for simplicity).

To realize a 30 GHz 2×2 beamformer with a beam steering from -45 to 45 degree, the active TTD phase shifter needs to provide 18 ps total variable delay, which is 50% more compared to the 12 ps standalone version TTD phase shifter presented in Section 4.3. The total variable delay can be increased by either adding extra G_m-RC cells, or realizing more delay per G_m-RC cell, i.e. a trade-off between power dissipation and NDV. To relax the trade-off, an improved implementation of G_m-RC delay cell is proposed (Figure 4-15), where each G_m-RC stage realizes 50% more delay, i.e. 6ps, meanwhile keeping a low NDV. As shown in Figure 4-15, instead of using only one CB transistor per G_m-RC stage, two CB transistors are stacked, i.e. Q_a and Q_b. Together with the parasitic capacitance $\underline{C_{out}}$ at the collector node, each device now acts as a sub- G_m-RC cell. As a result, the implemented delay per sub- G_m-RC cell is only 3 ps, while the whole G_m-RC stage still achieves 6 ps delay. Compared to the standalone version TTD phase shifter where each G_m-RC cell implement 4 ps delay, the improved design results in even better NDV. Transistor Q_{tail} acts as a current source, which can be switched off to reduce power dissipation when the corresponding delay cell is not activated.

As indicated in Section 4.3.2, the active TTD phase shifter can operate from 1.5 V to 2.5 V supply voltage to meet different linearity requirement. Additionally, for lower input power level, the first 2 stages of HG-LNA can also operate with lower supply voltage, i.e. 1.8 V, without too much NF degradation. As a result, the complete front-end can operate in a dual power mode. Depending on the coarse delay settings, the power dissipation of the complete front-end is 201-336 mW in high power mode and 94-127 mW in low-power mode.

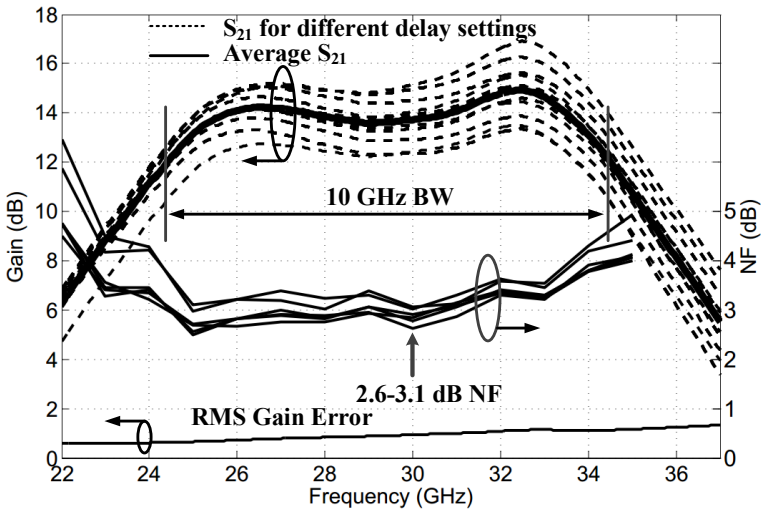


Figure 4-16. Measured S-parameters and NF of the high power receiver front-end (HG-LNA/active TTD) in high power mode for different delay settings.

4.4.2. Measurement Results

The measured gain and NF performance of the front-end (HG-LNA/active TTD) in high power mode are shown in Figure 4-16. With different delay settings, the front-end presents 13.8±1.3 dB gain at 30GHz and an -3 dB BW of 10 GHz for the average gain, i.e. from 24.4 GHz to 34.4 GHz. Within the bandwidth, the RMS gain error is 0.6-1.1 dB. In low power mode, the gain drops to 12.3±2 dB at 30 GHz and the average gain BW reduces to 7.6 GHz. The measured NF of the front-end at 30 GHz is 2.6-3.1 dB in high power mode and 3.4-4dB in low power mode.

Due to good reverse isolation, i.e. S_{12}, the input return loss of the front-end is dominated by the S_{11} of the HG-LNA and is better than -10 dB for all the delay settings. Figure 4-17 shows the relative delay response for different delay settings from 22 GHz to 37 GHz (high power mode). The TTD front-end offers 17.8 ps continuous variable delay with an in-band NDV_{PS} of 3.5%, i.e. 0.62 ps worst case delay variation. The large signal and linearity performance of the front-end are measured when the front-end reaches its peak gain, i.e. 17.2 dB at 32.5GHz with the lowest delay setting. The measured input P_{1dB} and IIP3 are respectively -15.8 dBm and -9 dBm in high power mode, and -18 dBm and -12dBm in low power mode. The two tone frequency offset for IIP3 measurement is 80 MHz.

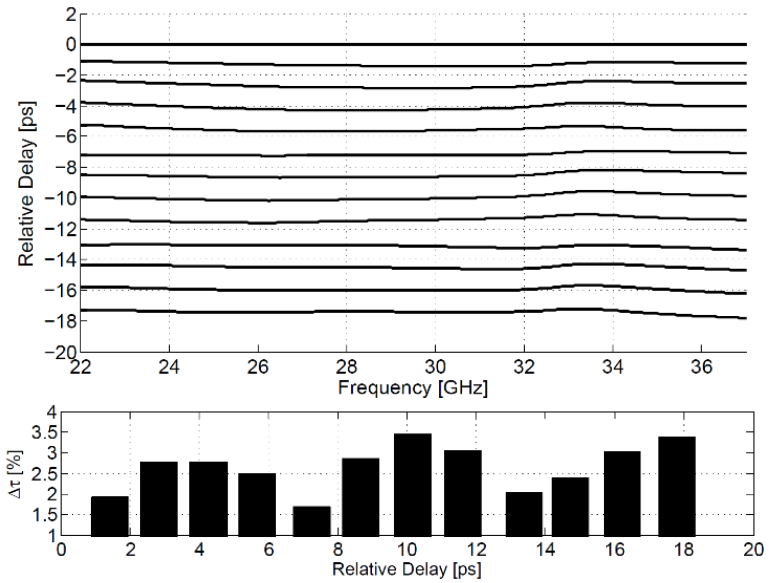


Figure 4-17. Measured relative delay response and NDV_{PS} of high power TTD receiver front-end (HG-LNA/active TTD).

4.5. Conclusion and Discussion

4.5.1. Conclusion

A compact Ka-band active TTD phase shifter and a wideband TTD receiver frontend have been realized using a 0.25 μm SiGe:C BiCMOS process. With the proposed delay-variation cancellation technique, the TTD phase shifter achieves

a flat delay response from 20 GHz to 40 GHz with only 6.6% normalized delay variation. A constant input impedance, i.e. $|S_{11}| < -15$dB, is maintained for all delay settings within 20-40 GHz frequency band. The TTD receiver frontend presents 10 GHz gain BW and 15 GHz flat delay BW with only 3.5% normalized delay variation.

Table 4-1. Benchmarking of the proposed standalone active and passive TTD phase shifter with other fully integrated TTD phase shifter.

	Tech-nology	Freq. (GHz)	Amp. Error (dB)	Max. Delay (ps)	NDV* (%)	Pwr (mW)	ICP_{1dB}** (dBm)	Resolu-tion (ps)	Size*** (mm^2)
Active TTD (2.7V)	**0.25µm SiGe**	**20-40**	**±0.9**	**12**	**6.4**	**146**	**+9.7**	**Cont.**	**0.1**
Active TTD (1.5V)	**0.25µm SiGe**	**20-40**	**±1.4**	**12.5**	**6.6**	**33**	**+3.6**	**Cont.**	**0.1**
[12]	0.18µm SiGe	1-15	±1	64	~16	87.5	N/A	4	0.82
[13]	0.13µm SiGe	31-41	N/A	54	N/A	104	N/A	18	1.44
[14]	0.13µm CMOS	15-40	±2	42	>20	8.6-24.6	+8	3	0.99
[11]	0.13µm CMOS	1-15	±3	225	~14	78	N/A	15	1.5
[15]	0.14µm CMOS	1-2.5	±0.4	550	3.6	90	N/A	Cont.	0.07
[16]	0.8µm SiGe	3-10	±0.7	25	40	38.8	-1	Cont.	0.23
[30]	0.13µm SiGe	55-65	N/A	16	N/A	0	N/A	1.2	0.35

* NDV: The worst case delay variation in percentage of total variable delay, values with '~' are estimated from the given delay response

** For TTD phase shifter only

*** Estimated core size of TTD circuits only

Table 4-1 shows the benchmarking of the proposed standalone TTD phase shifter (both active and passive TTD phase shifter) with other works in the literature. It can be seen that the proposed standalone active TTD phase shifter has an improved performance regarding flat delay bandwidth, delay variation, gain variation, delay resolution, and chip area. The only exception is the work in [15], which implements the complete TTD circuit using G_m-RC all-pass filters, and present only 3.5% NDV over 1-2.5 GHz BW. Meanwhile, due to the inductorless

architecture, the chip area is greatly reduced. However, as [15] operates at a much lower frequency, all the parasitic effects in the proposed designs are significantly mitigated, making it easier to maintain the constant delay and amplitude response. As the frequency goes up, the performance of the G_m-cell will degrade, therefore the architecture in [15] will hardly be used at mm-wave frequencies.

Table 4-2 shows the benchmarking of the proposed high power (HP-) frontends with other works in the literature. It can be seen that the proposed two TTD frontend has the best reported overall NF, linearity and TTD performance, i.e. the smallest delay variation over the largest BW.

Table 4-2. Benchmarking of the proposed wideband TTD frontend with other fully integrated TTD frontend.

	[12]	[13]	[11]	**HP-FE**	
				2.5V	**1.5V**
Min. NF (dB)	N.A.	4.0*	2.9*	**2.6**	**3.4**
Avg. Gain (dB)	~10	~12	9	**13.8**	**12.3**
Gain Err. (dB)	±1	±1.5	±3	**±1.3**	**±2**
Gain BW (GHz)	12	10	N/A	**10.1**	**7.6**
Delay BW** (GHz)	1-15	30-40	1-15	**22-37**	**22-37**
Total Delay (ps)	64	54	225	**17.8**	**18.3**
NDV_{PS}	~12%	N.A.	~14%	**3.5%**	**3%**
Input P_{1dB} (dBm)	-23	N.A.	N.A.	**-15.8**	**-18**
P_{DC}/channel (mW)	87.5	104	138	**268.5**	**110.5**
Resolution (ps)	4	18	15	**Cont.**	**Cont.**
Size*** (mm^2)	> 1.5	> 1.4	> 1.2	0.31	

* NF for LNA only

** Within which the delay variation is evaluated

*** Estimated core size of one front-end channel

Mark with "~" is estimated from the measurement results

4.5.2. Limitation and Discussion

Regarding the DV canceling, theoretically, the LC delay cells can only be optimized to cancel the DV for a specific setting of the G_m-RC stage. In other coarse settings, the DV canceling is less effective. This is also the reason that the final measurement results still present 6.6% NDV at 20-40 GHz frequency band. One

can also foresee that with more G_m-RC stages and more coarse settings, the overall NDV will be further degraded.

In addition, although the total variable delay can be extended by adding the compact Gm-RC cells, the power dissipation will be significantly increased. Except for the direct increase of power consumption by including more active stages, the added G_m-RC cells will result in more insertion loss of the overall phase shifter. It will call for a larger gain from the LNA to keep a reasonable frontend gain. Consequently, with a fixed overall input P_{1dB}, both the LNA and the G_m-RC cells must increase their power consumption to handle the larger output power at the output of the LNA.

5. Passive True-Time-Delay Phase Shifter and Receiver Frontend

5.1. Introduction

In the previous chapter, an active true-time-delay (TTD) phase shifter has been realized, which combines G_m-RC and LC delay cells and achieves flat delay from 20 to 40GHz. However, to maintain a high input compression point (ICP), the frontend with active TTD solution tends to have a large power dissipation, which is not preferable in many low power applications. To relax the trade-off between power dissipation and ICP, a passive TTD phase shifter solution is investigated and implemented in this chapter.

As the passive TTD phase shifter only contains passive components and switches, the G_m-RC based DV canceling technique cannot be applied anymore. As a result, an alternative DV reduction technique – a broadband matching technique is proposed, which can be applied to a fully passive TTD architecture. With the proposed broadband matching architecture, the presented standalone passive TTD phase shifter achieves a flat delay response over 10-50GHz with only 3.9% normalized delay variation (NDV_{PS}). The corresponding low power TTD frontend is also implemented by integrating the previously discussed low-power LNA (Design-III in Section 3.4).

5.2. Broadband Matching Architecture

According to the delay response of two types of delay cells shown in Figure 2-10 and Figure 2-11, by realizing the same amount of delay per delay cell, the matched LC π-network exhibits much lower NDV than the G_m-RC delay cell. Therefore, if the LC delay cells can be used in broadband matched condition, they can replace the G_m-RC stages in active TTD phase shifter for realizing coarse delay tuning and achieve low DV without power dissipation.

Figure 5-1 demonstrates the delay performance of a matched LC delay cell. As shown in Figure 5-1b-c, when achieving 2.77 ps, i.e. 30 degrees at 30 GHz, the matched LC cell only presents about 5% NDV up to 60 GHz. Therefore, maintaining broadband matched condition of an LC delay cell can be a solution to design a low DV passive TTD phase shifter. For instance, a simplified passive TTD phase shifter architecture can be implemented as shown in Figure 5-2, where all the delay cells are realized with LC π-network with a characteristic impedance of Z_0. The delay is discretely tuned by path selectors $k_{1,2,\ldots m}$. To minimize DV, each enabled LC cell has to see a broadband impedance that equals to Z_0 at both source and load. However, due to all kinds of parasitic effects at a mm-wave frequency, there are several challenges to maintain the broadband matching condition of LC delay cells.

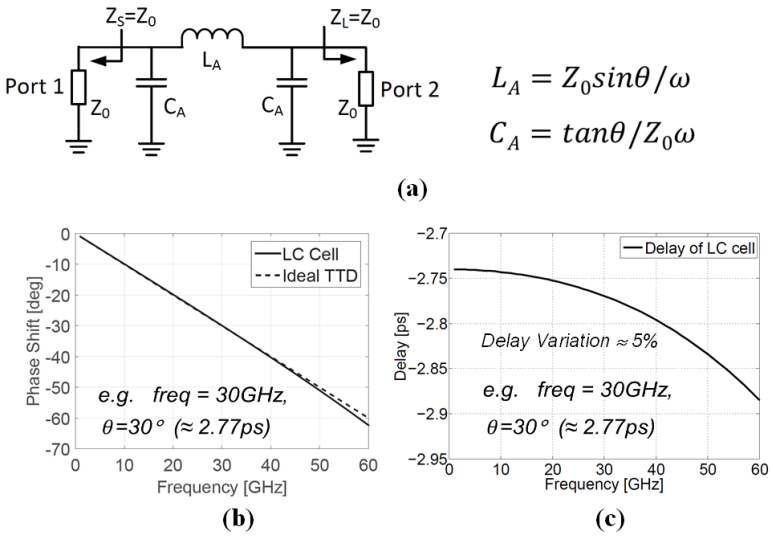


Figure 5-1. Phase response and NDV of a broadband matched LC delay cell when achieving 2.77 ps delay.

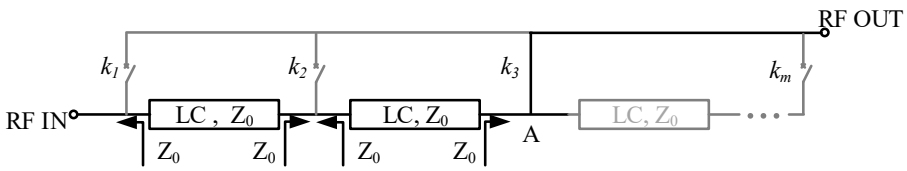


Figure 5-2. Simplified architecture of a passive TTD phase shifter.

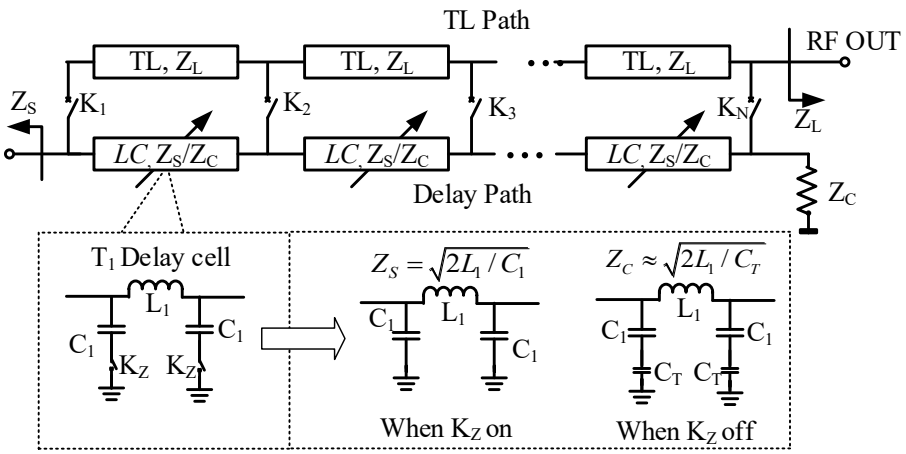


Figure 5-3. Proposed broadband matching based passive TTD architecture.

First of all, when the switches $k_{1,2,..m}$ are turned off, a certain parasitic capacitance is present and loads the LC cells. Secondly, if not designed carefully, the disabled LC cell can present parasitics at node *A* as well. Both the parasitic loading mentioned above result in frequency-dependent mismatching, leading to an increased DV.

To solve these two issues, a broadband matching TTD architecture is proposed. As shown in Figure 5-3, the *N*-stage discrete tuning delay network consists of two paths and switches $k_{1,2,...N}$ as path selectors. The lower delay path consists of LC delay cells, offering a much larger delay than the sections in the upper TL path, which are coplanar waveguide (CPW) TLs and serve as interconnects between two discrete delay cells. As a result, a variable delay can be achieved by activating different switches $k_{1,2,...N}$. Assume that the TTD phase shifter is terminated by the broadband impedances Z_S and Z_L, (usually both are 50Ω). The TLs

in TL path will then have the characteristic impedance equal to Z_L. The LC cells in the delay path are implemented by LC π-networks with switches K_Z added in both ground branches. By switching K_Z on and off, the characteristic impedance of the LC cell can be varied between Z_S and Z_C (illustrated in the lower part of Figure 5-3), where C_T represents the parasitic capacitance of K_Z when it is off. Here it is assumed that $C_T \ll C_1$. To minimize undesired reflections, path T_1 is terminated with a resistance equal to Z_C.

Figure 5-4 shows how broadband matching is achieved within the proposed architecture. Assume that the m-th path selector k_m is activated, then all the LC cells before k_m are switched to the Z_S mode (with K_Z in Figure 5-3 on) and those after k_m are switched to the Z_C mode (with K_Z in Figure 5-3 off). Due to the matched termination at the end of the LC path, Z_{LC2} is always equal to Z_C, independent of the delay settings. The source and load impedance seen by the m-th LC delay cell can be derived as $Z_{Sm}=Z_S$ and $Z_{Lm}=Z_C//(R_{on}+Z_L)$, where R_{on} is the on-resistance of m-th switch K_m. As $Z_C>Z_S$, parameters L_1, C_1 and C_T can be designed such that:

$$Z_{Sm} = Z_S = Z_C // \left(R_{on} + Z_L\right) = Z_{Lm} \tag{5.1}$$

With (5.1) satisfied, the LC delay cell is well matched to both source and load. Note that this condition applies to all the other delay settings. Additionally, since the characteristic impedance of a TL is frequency independent, the matching condition in (5.1) is valid for a wide frequency range. As a result, with the proposed architecture a flat delay response can be achieved over tens of GHz frequency band.

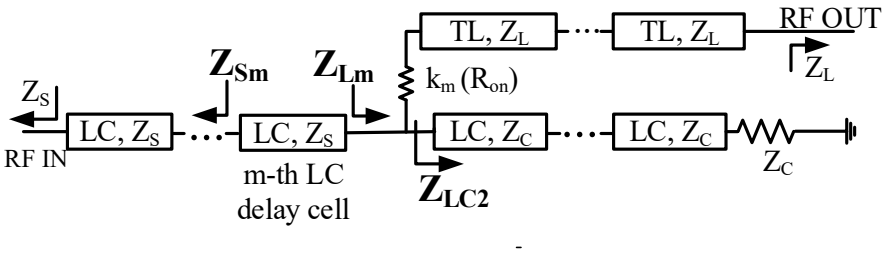


Figure 5-4. Broadband matching mechanism of the proposed TTD architecture.

5.3. 10-50GHz Passive True-Time-Delay Phase Shifter

5.3.1. Architecture

The proposed TTD phase shifter is targeted to achieve 32ps continuous variable delay, which enables a 4-element beam former with 5 mm antenna spacing to perform a beam-squint free beam-steering from -40 to 40 degree in the 10-50 GHz range. Figure 5-5 shows the block diagram of the fully differential TTD phase shifter (plotted in single-ended only for simplicity). Coarse tuning and fine tuning are combined to relax the trade-offs between the large total variable delay and high tuning resolution. The coarse tuning part is based on the proposed broadband matching architecture. With 7 LC delay cells cascaded, the coarse tuning part provides 3 bits or 7 steps discrete delay tuning, with the tuning range and tuning step of 28 ps and 4 ps, respectively. To cover the 4 ps step of the discrete tuning, the fine tuning stages, based on variable-C LC π-networks, offer in total 4.4 ps continuous variable delay. All the switches in the design are implemented using HV-NPN devices (see Figure 2-12). The base current of each switch, depending on the switch locations, is only a few μA.

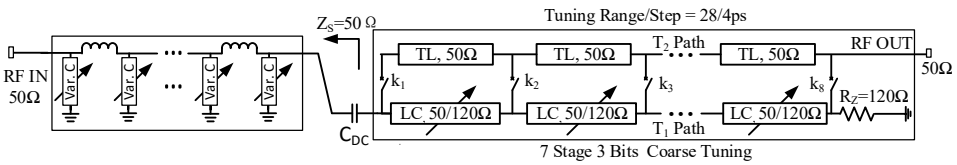


Figure 5-5. Block diagram of proposed differential TTD phase shifter (plotted in single-ended form for simplicity)

5.3.2. Design of the Coarse Tuning Part

To meet the broadband condition in (5.1), Z_L, R_{on}, Z_S and Z_C values have to be determined. According to the proposed architecture shown in Figure 5-3, Z_L should be equal to the load termination of the TTD phase shifter. To facilitate the output matching, Z_L is chosen to be 50 Ω. Switches $k_{1,2,...8}$ are implemented with small transistors in order to minimize the parasitic when they are off. Smaller transistors as switches, however, results in a large on-resistances, i.e. R_{on} is 35 Ω at 30 GHz. As indicated in Figure 5-5, for a good S_{11} performance, the value of Z_S

should be equal to the nominal characteristic impedance of the fine tuning stage, which finally should be equal to the source termination of the complete TTD phase shifter. As a result, Z_S is chosen to be 50 Ω to ease the input matching. With the known Z_S, R_{on} and Z_L, Z_C can be calculated based on (5.1), being 120 Ω.

With the broadband matching condition satisfied, the parameters of LC cell and switch K_Z can be derived, i.e. L_1, C_1, and C_T (see Figure 5-3). When the LC cell is in Z_S mode, the delay difference between one LC delay cell and CPW TL cell is 4 ps. As the dimension of the CPW TL in the layout results in 0.5 ps delay, each LC delay cell has to offer 4.5 ps delay. Based on the value of Z_C, Z_S and required delay time, parameters L_1, C_1, and C_T, in LC delay cell can be calculated, i.e. 200 pH, 48 fF, and 8.3 fF, respectively. Note that these parameters in each stage may shift within a certain range during the layout phase due to the parasitic of switches $k_{1,2,...8}$ and metal resistance along the LC delay path.

5.3.3. Design of the Fine Tuning Part

In order to reduce the characteristic impedance changes of the LC π-network, the 4.4 ps variable delay is distributed over two LC stages, where each LC stage varies the capacitance in a smaller range. However, the required variable delay per stage still calls for a large size varactor, which would introduce large parasitic capacitance and reduce the tuning ability of each LC stage. Therefore, instead of using varactor-only tuning, a hybrid tuning is employed, i.e. 3 bits digitally controlled binary capacitor bank in parallel with an analog controlled varactor (see Figure 5-6a). As a result, only a small varactor is required. With a control voltage V_C from 0 V to 2.8 V, the varactor varies its capacitance from 14 to 27 fF (see Figure 5-6b), covering the 12 fF LSB of the capacitor bank.

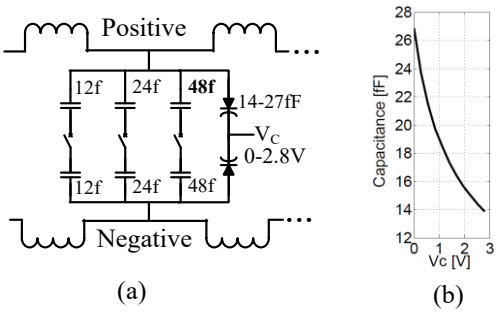


Figure 5-6. Implementations of (a) differential hybrid capacitance tuning and (b) varactor characteristic

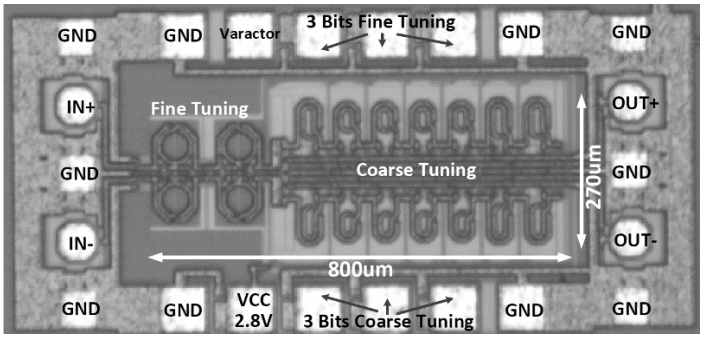


Figure 5-7. Die photo of the proposed passive TTD phase shifter.

5.3.4. Measurement Results

Figure 5-7 shows the die photo of the proposed fully differential passive TTD phase shifter. The size of the core phase shifter is less than 0.22 mm^2. The delay of the TTD phase shifter is controlled by 6 bits digital signal, i.e. 3 bits coarse tuning plus 3 bits fine tuning, and one analog signal, with a control voltage from 0 V to 2.8 V. To evaluate the small signal performance of the differential TTD phase shifter, a 4 ports S-parameters measurement has been performed, from which the 2 ports differential S-parameters are derived.

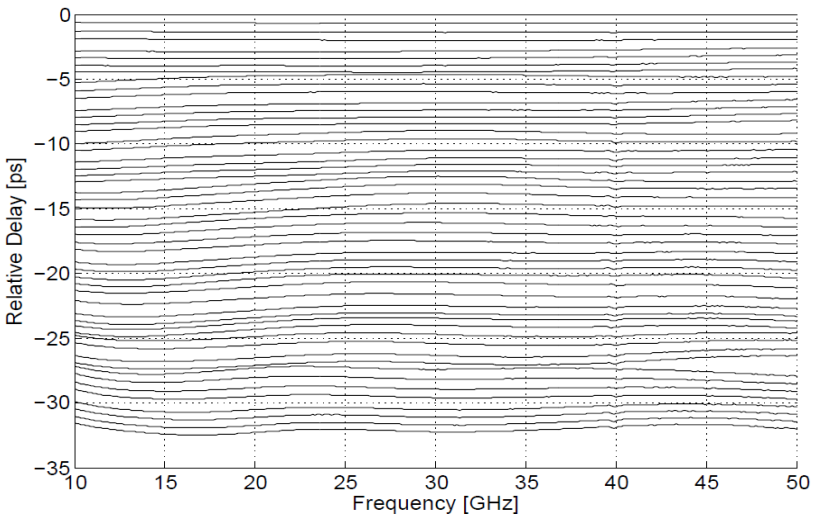


Figure 5-8. Measured relative delay response for different settings.

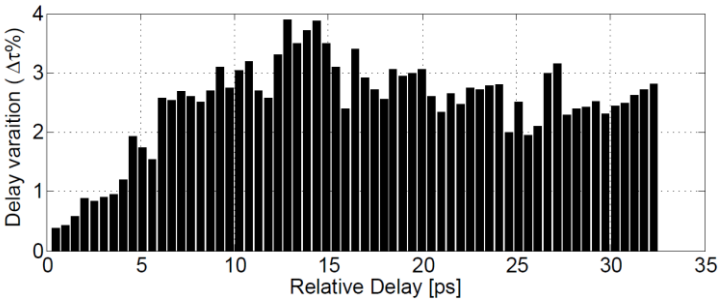


Figure 5-9. Measured normalized delay variation of each delay setting for 10-50GHz.

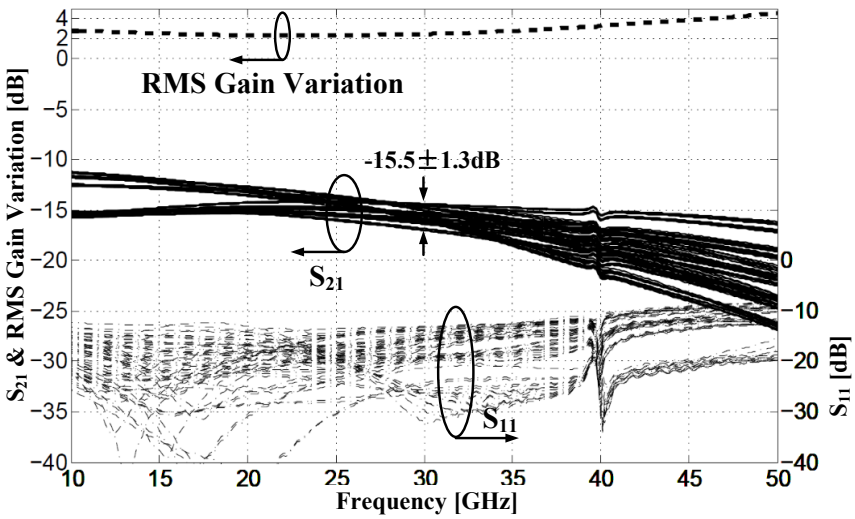


Figure 5-10. Measured S_{21}, S_{11} and RMS gain variation of the TTD phase shifter.

Figure 5-8 shows the relative delay response for different delay settings from 10 GHz to 50 GHz. The total achieved variable delay is 32.8 ps, close to the design target of 32 ps. To evaluate the flatness of the achieved delay response, Figure 5-9 shows the in-band NDV of each delay setting. The worst-case NDV_{PS} (defined in equation (2.7)) is 3.9%. The degraded delay flatness below 10 GHz is mainly caused by the series DC decoupling capacitance, e.g. C_{DC} in Figure 5-5. The flatness can be improved by using a larger capacitance, but that results in a larger area.

Figure 5-10 shows the measured S_{21}, S_{11}, and the RMS gain variation. The insertion loss of the proposed TTD phase shifter is 15.5±1.3 dB at center frequency 30

GHz, with the RMS gain variation less than 3dB from 10 GHz to 37 GHz. The measured input reflection coefficient is well below -10dB up to 40GHz, and degraded to -8 dB at 50 GHz. The measured worst-case input P_{1dB} and IIP3 at 30GHz are +15.5 dBm and +24.7 dBm. Suppose the proposed TTD phase shifter is used in a receiver with an input P_{1dB} specification of -20 dBm, a high gain LNA, e.g. S21 > 30 dB, can be integrated in front the phase shifter to suppress the overall NF of the frontend (LNA+TTD) and result in a reasonable frontend gain, i.e. 15 dB.

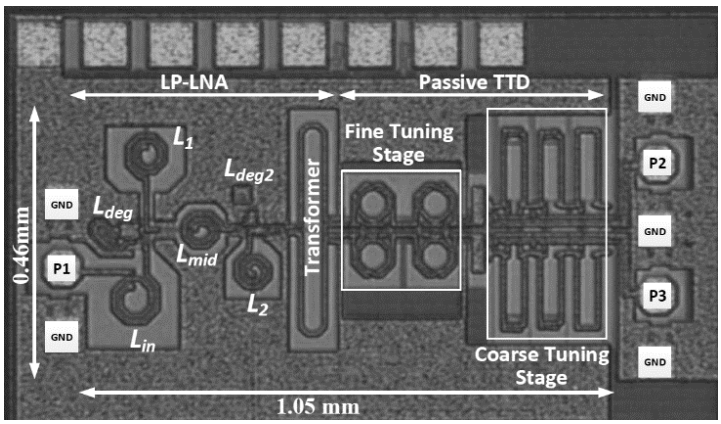


Figure 5-11. Die photo of the low power TTD receiver front-end (LP-LNA/passive TTD).

5.4. 25-35GHz Low Power Phased Array Receiver Frontend

5.4.1. Circuit Design

To realize a low power receiver, the passive TTD phase shifter is integrated with the LP-LNA (Design-III in Section 3.4). Figure 5-11 shows the die photo of the low power TTD receiver front-end. The complete front-end has a core area of 0.48 mm² (1.05 mm×0.46 mm). Since the proposed LP-LNA has included the CC stage (see Figure 3-22), no additional buffer stage is needed when connecting the LNA and the passive phase shifter.

The presented standalone passive phase shifter, with a total variable delay of 32.8 ps, enables a 30 GHz 2×2 beamformer to perform a full range beam-scanning from -90 degree to 90 degrees. However, in practice a scanning range from -60

degree to 60 degrees would be enough for most of the Ka-band applications. As a result, the total variable delay of the low power front-end has been reduced to 20.5 ps, which also reduces the loss and die area of the passive phase shifter. The revised passive phase shifter has the same architecture as in the standalone version but only has 3 discrete tuning stages, with each stage providing 5 ps fixed delay. For fine tuning stages, 5.5 ps continuous variable delay is required to cover the discrete delay step and fulfill 20.5 ps of the overall variable delay. The tuning range of the fine tuning stages, compared with that in the standalone phase shifter, is increased by 25 %. To include some extra margin, all the inductors, capacitors, and varactors in fine tuning stages are up-scaled by 30%, resulting in 5.7 ps variable delay. As the ratio between inductance and capacitance is not changed during scaling, the characteristic impedance maintains the same.

The delay of the TTD phase shifter is controlled by 5 bits digital signal, i.e. 2 bits for 3 stages coarse tuning plus 3 bits fine tuning, and one analog signal. To be compatible with the 1.5 V voltage supply of LP-LNA, the supply voltage for both digital and analog control for the phase shifter is changed to 1.5 V as well. As in standalone phase shifter design, the supply voltage is 2.8 V, the impact of changing supply voltage needs to be compensated. For all the NPN switches, the biasing resistors are adjusted to keep the same on-state V_{BE} as in standalone phase shifter design. For the varactors, the size is further increased to compensate the reduced tuning range. The simulated insertion loss of the revised passive phase shifter ranges from 7 dB to 10 dB with different delay settings.

5.4.2. Measurement Results

The complete low power front-end (LP-LNA/passive TTD) consumes in total 22.4 mW (14 mA, 1.6 V, including the leakage current for switches and logic circuits). Figure 5-12 shows the measured gain and NF performance. With different delay settings, the front-end presents 14.8±3 dB gain at 30 GHz and an -3 dB BW of 11.5 GHz for the average gain, i.e. from 24 GHz to 35.5 GHz. Within the bandwidth, the RMS gain error is 2.3-3.2 dB.

The measured amplitude variation is much larger than in simulation. As the measured gain of the LP-LNA matches well with the simulation, we believe that the gain variation discrepancy is mainly coming from the TTD circuit, caused by the inaccurate RC extraction of the BJT switches, i.e. the loss of transistor interconnects are underestimated. This is confirmed by re-characterizing the transistor interconnects using an EM simulator. As a result, each BJT switch including

interconnects causes 0.2-0.6 dB more insertion loss than expected at on state. By taking into account of this extra switch losses, the simulated gain variation is 5.7 dB at 30 GHz, which agrees well with the measurement result.

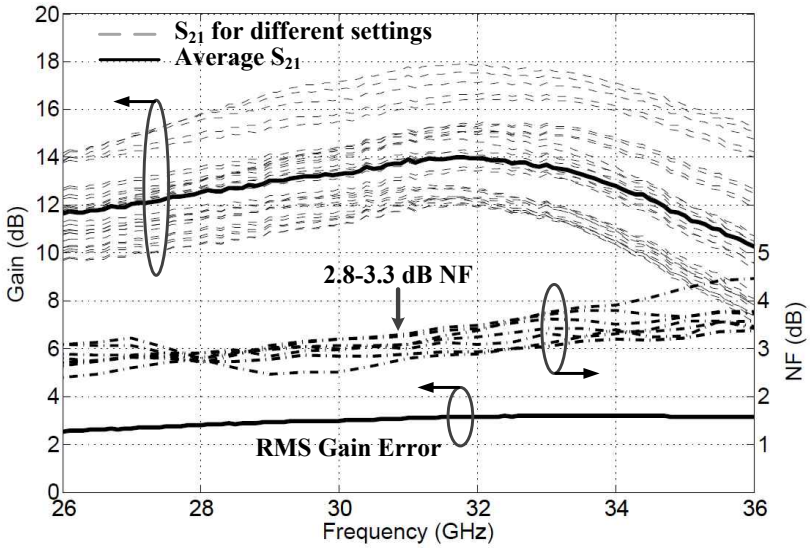


Figure 5-12. Measured S-parameters and NF of the low power receiver front-end (LP-LNA/passive TTD) for different delay settings.

The measured NF of the low power front-end at 30 GHz is 2.5-3.2 dB. The input return loss of the front-end is almost identical to the S_{11} of the LP-LNA (see Figure 3-14) and is better than -10 dB for all the delay settings within the gain bandwidth.

Figure 5-13 shows the relative delay response for different delay settings from 26 GHz to 40 GHz. The TTD front-end offers 22 ps continuous variable delay with an in-band NDV_{PS} of 5.4%, i.e. 1.2 ps worst case delay variation. Compared with the standalone passive TTD circuit, the degraded NDV_{PS} is mainly due to the impedance mismatch between the LNA and TTD, especially at frequencies below 30 GHz. Although the output CC stage of the LNA provides a broadband impedance, the transformer in parallel contributes a significant reactance at lower frequencies. With such a frequency dependent source termination, the TTD fine tuning stage results in an increased delay variation. From 30 GHz and above, however, the transformer operates close to its self-resonance frequency. As a result, the TTD circuit again sees a broadband source impedance and the

delay variation reduces. As shown in Figure 5-13, if the TTD performance is evaluated from 30-40 GHz only, the measured NDV_{PS} is reduced to 3.7 %, which is comparable with the NDV of the standalone passive TTD circuit (see Figure 5-9).

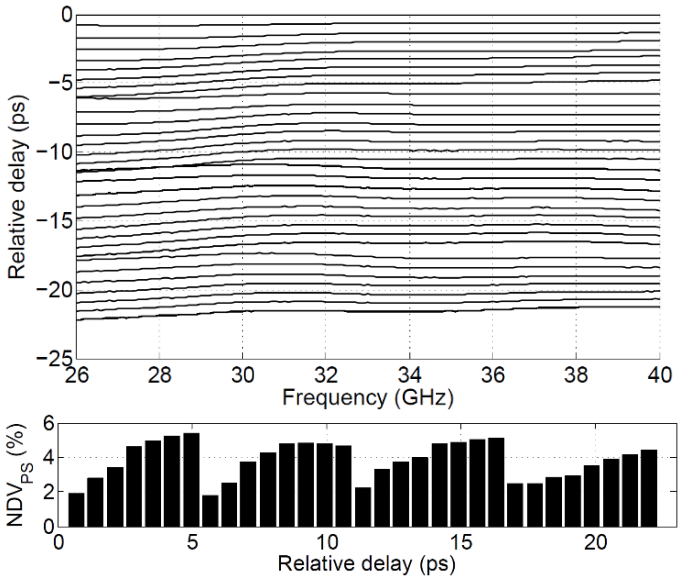


Figure 5-13. Measured relative delay response and NDV_{PS} of low power receiver frontend (LP-LNA/passive TTD).

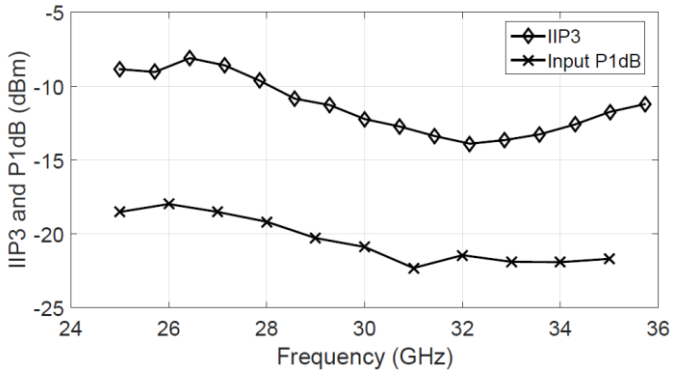


Figure 5-14. Measured input P1dB and IIP3 of and NDV_{PS} of low power receiver frontend (LP-LNA/passive TTD).

As shown in Figure 5-14, the worst-case measured input P_{1dB} and IIP3 of the low-power frontend are -22.2 dBm and -14 dBm at 31 GHz, which is almost the same

as the standalone LP-LNA (see Figure 3-24). This is because the passive TTD phase shifter is highly linear (>20dBm IIP3) therefore the frontend linearity is limited by the LP-LNA.

Table 5-1. Benchmarking of the proposed standalone active and passive TTD phase shifter with other fully integrated TTD phase shifter.

	Tech-nology	Freq. (GHz)	Amp. Error (dB)	Max. Delay (ps)	NDV* (%)	Pwr (mW)	ICP_{1dB}** (dBm)	Reso-lution (ps)	Size*** (mm^2)
Passive TTD	**0.25µm SiGe**	**10-50**	**±1.3**	**32.8**	**3.9**	**< 1**	**+15.5**	**Cont.**	**0.22**
Active TTD (2.7V)	**0.25µm SiGe**	**20-40**	**±0.9**	**12**	**6.4**	**146**	**+9.7**	**Cont.**	**0.1**
Active TTD (1.5V)	**0.25µm SiGe**	**20-40**	**±1.4**	**12.5**	**6.6**	**33**	**+3.6**	**Cont.**	**0.1**
[12]	0.18µm SiGe	1-15	±1	64	~16	87.5	N/A	4	0.82
[30]	0.13µm SiGe	55-65	N/A	16	N/A	0	N/A	1.2	0.35
[13]	0.13µm SiGe	31-41	N/A	54	N/A	104	N/A	18	1.44
[14]	0.13µm CMOS	15-40	±2	42	>20	8.6-24.6	+8	3	0.99
[11]	0.13µm CMOS	1-15	±3	225	~14	78	N/A	15	1.5
[15]	0.14µm CMOS	1-2.5	±0.4	550	3.6	90	N/A	Cont.	0.07
[16]	0.8µm SiGe	3-10	±0.7	25	40	38.8	-1	Cont.	0.23

* NDV: The worst case delay variation in percentage of total variable delay, values with '~' are estimated from the given delay response
** For TTD phase shifter only
*** Estimated core size of TTD circuits only

5.5. Conclusion and Discussion

5.5.1. Conclusion and Benchmarking

A passive broadband TTD phase shifter and a wideband TTD receiver frontend have been realized using a 0.25 µm SiGe:C BiCMOS process. With the proposed broadband matching technique, the standalone passive TTD phase shifter achieves a flat delay response from 10 GHz to 50 GHz with only 3.9% NDV. A

constant input impedance, i.e. $|S_{11}| < -10$dB, is maintained for all delay settings within 10-40 GHz frequency band. The TTD receiver frontend presents 11.5 GHz gain BW and 14 GHz flat delay BW with only 5.4 % normalized delay variation.

Table 5-1 shows the benchmarking of the proposed standalone TTD phase shifter (both active and passive TTD phase shifter) with other work in the literature. It can be seen that both of the proposed standalone TTD phase shifters have an improved performance regarding flat delay bandwidth, delay variation, delay resolution, and the chip area. The only exception is the work in [15], which implements the complete TTD circuit using G_m-RC all-pass filters, and present only 3.5% NDV over 1-2.5 GHz BW. Meanwhile, due to the inductorless architecture, the chip area is greatly reduced. However, as [15] operates at a much lower frequency, all the parasitics issued in the proposed designs are significantly mitigated, making it easier to maintain the constant delay and amplitude response. As the frequency goes up, the performance of the G_m-cell will degrade, making the architecture in [15] difficult to apply in mm-wave frequencies.

Table 5-2. Benchmarking of the proposed wideband TTD frontend with other fully integrated TTD frontend.

	[12]	[13]	[11]	HP-FE		**LP-FE**
				2.5V	1.5V	
Min. NF (dB)	N.A.	4.0*	2.9*	2.6	3.4	**2.5**
Avg. Gain (dB)	~10	~12	9	13.8	12.3	**14.8**
Gain Err. (dB)	±1	±1.5	±3	±1.3	±2	**±3**
Gain BW (GHz)	12	10	N/A	10.1	7.6	**11.5**
Delay BW** (GHz)	1-15	30-40	1-15	22-37	22-37	**26-40**
Total Delay (ps)	64	54	225	17.8	18.3	**22**
NDV_{PS}	~12%	N.A.	~14%	3.5%	3%	**5.5%**
Input P_{1dB} (dBm)	-23	N.A.	N.A.	-15.8	-18	**-22**
P_{DC}/channel (mW)	87.5	104	138	268.5	110.5	**22.4**
Resolution (ps)	4	18	15	Cont.	Cont.	**Cont.**
Size*** (mm^2)	> 1.5	> 1.4	> 1.2	0.31		**0.48**

* NF for LNA only

** Within which the delay variation is evaluated

*** Estimated core size of one front-end channel

Mark with "~" is estimated from the measurement results

Table 5-2 shows the benchmarking of both the proposed high power (HP-) and low power (LP-) frontends with other work in the literature. It can be seen that the two proposed TTD frontends have the best reported overall NF, linearity and TTD performance, i.e. the smallest delay variation over the largest BW. Besides, the low power front-end has the lowest power dissipation meanwhile maintaining an acceptable ICP.

5.5.2. Discussion

Compared to the low power front-end, the high power front-end occupies less chip area and has a better linearity performance. Especially for a system where a larger total variable delay is needed, the high power front-end can cascade more G_m-RC cells, which is much more compact than adding more LC delay cells in the low power front-end. Besides, due to the high output impedance and high reverse isolation of the active phase shifter, the high power front-end enables multiple channels to combine at the output in the current domain without using a bulky power combiner, e.g. Wilkinson combiner. However, as the G_m-RC cells are loaded with very small impedance, i.e. $1/G_m < 5\ \Omega$, they are poor in power efficiency and need a large DC current to maintain the required ICP. As a result, the high-power front-end including active TTD circuits consumes a significantly higher power than the low-power front-end.

The low power front-end, eliminating the active G_m-cells in TTD circuits, is preferred in the low power system. It also enables more phased array elements to be integrated on one chip without burdening the power budget. Additionally, as the operating frequency continuously increase, the footprint of the passive scales down and the performance of the G_m-cell degrades. As a result, the proposed passive architecture may find more potential at higher frequencies.

6. Ka-band 2x2 True-Time-Delay Phased Array Receiver

6.1. Introduction

In order to apply the proposed low power TTD frontend (Chapter 5) in a phased array receiver, a 2-by-2 TTD phased array receiver will be presented in this chapter. It can be seen from Figure 5-12 that the low power TTD frontend (LNA+TTD) presents more than 5 dB gain variation over different delay settings. Such a large amplitude variation will change the array pattern and negatively impact the beamforming directivity. As a result, each receiver channel needs an RF variable-gain amplifier (VGA) to compensate for the gain variation. To ease the LO distribution and cancel out the interference from the undesired direction, the 4 RF channels are combined before the signal down conversion, which will be achieved by a high linear mixer.

The complete phased array receiver design aims to maintain the RF performance of the standalone low power TTD frontend in Chapter 5, e.g. NF, TTD, ICP_{1dB} performance. In addition, system level issues such as biasing, ground plane distribution, isolation between various channels, power dissipation, and signal combining will be investigated.

6.2. Architecture

Figure 6-1 shows the proposed Ka-band 2×2 TTD phased array receiver, which includes four RF frontends, a 4:1 power combiner and a down-conversion mixer

followed by a buffer. The RF frontend consists of the low-power frontend discussed in Section 5.4 as well as a 3-bits RF VGA. Each RF frontend is able to provide 20.5 ps variable delay and 6 dB variable gain. The RF frontend covers 25-35 GHz frequency band. With such a phased array receiver system, a beam-squint free beam-steering with +/-60 degrees can be achieved by a 2-by-2 antenna array with 5 mm spacing, which is enough for most Ka-band applications.

The four RF channels are combined using a 2-stage Wilkinson power combiner, which provides a good isolation between different channels. The complete receiver employs a super-heterodyne architecture, with IF_1 centered at 11 GHz and IF_2 centered at 1.75 GHz (L-band). The L-band is commonly used in VSAT and P2P systems as the connection between the outdoor unit and the indoor unit. This work mainly focuses on the circuits from RF to IF_1 (Figure 6-1). The first down-conversion is achieved by Mixer1, driven by an external LO_1 from 14-23 GHz. The buffer followed is used for measurement purposes. The selected IF_1 = 11 GHz results in an RF image frequency ranging from 3-12 GHz. First, the image frequency is far from the 25-35 GHz RF band thus will be significantly attenuated by the frontend. Additionally, as the image does not overlap the L-band, a simple filter will be sufficient.

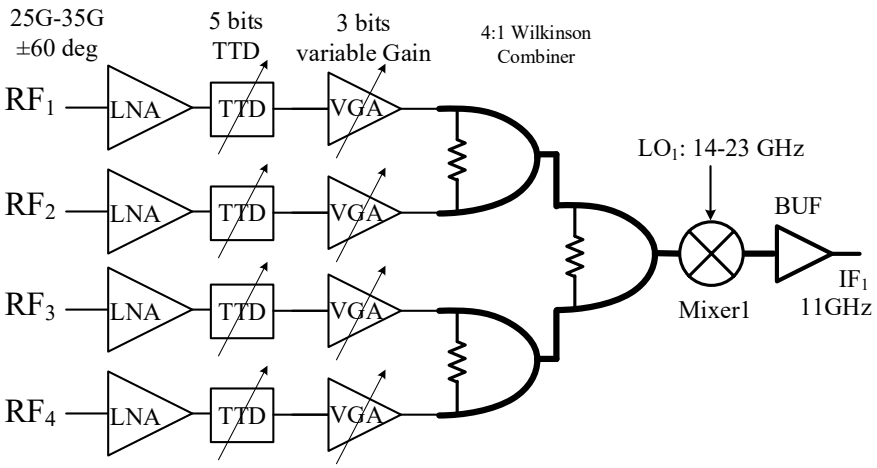


Figure 6-1. Architecture of the designed 2x2 TTD phased array receiver.

6.3. Design of VGA

6.3.1. Topology selection

The RF VGA is used after the TTD phase shifter. To avoid degrading the TTD performance of the whole frontend, the VGA has to satisfy 2 conditions. First of all, the input impedance of the VGA must be a frequency independent impedance, e.g. a broadband resistive value. Otherwise, the TTD phase shifter with a frequency-dependent loading will result in an increased delay variation. Secondly, the insertion phase of the VGA has to be kept constant over the gain settings. This is to ensure that the gain settings can be performed without disturbing the delay settings.

Figure 6-2 shows two VGA architectures that fulfill the design considerations mentioned above. In Figure 6-2a, the amplitude variation is achieved by changing the attenuation level in front of a fixed-gain amplifier. To achieve a broadband input impedance of the VGA, the attenuator is implemented with components with resistive impedance only, e.g. resistors and switches (when in ON-state). Moreover, due to the limited isolation from the attenuator, any non-resistive impedance at node *B* can be present at node A as well. As a result, the amplifier is also designed with a broadband input impedance. In the meanwhile, the attenuator has to maintain a constant insertion phase for different attenuation settings.

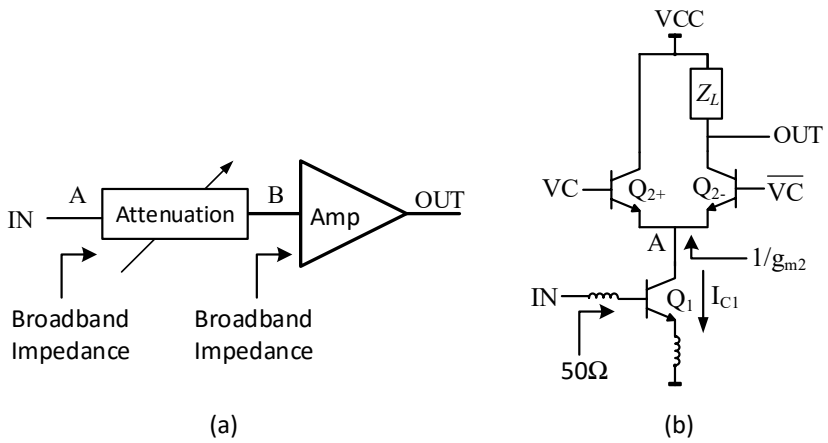


Figure 6-2. Two possible VGA implementations: (a) attenuation based VGA (b) current splitting based VGA.

Figure 6-2b shows an alternative VGA with constant insertion phase over gain settings, where the amplitude variation is realized by splitting the output signal current [31]. By switching on and off the control voltage *VC*, the RF current generated by Q_1 is either steered to the output or to the AC ground, resulting in a 1-bit VGA. As Q_{2+} and Q_{2-} have the same size, the current steering operation has little impact on the impedance at node *A*, i.e. $1/g_{m2}$, because the current flowing through Q_1 does not change. As a result, both the input impedance and the insertion phase of the VGA maintain the same value as the gain is varied. The tuning resolution can be increased by having multiple of these structures in parallel, where each stage is scaled differently to provide a linear variable gain [6].

The two topologies, however, exhibit a different characteristic in noise and linearity performance. With an attenuator added at the input, the topology in Figure 6-2a presents a higher NF, mainly because the attenuator in practice has a minimal insertion loss even with the lowest attenuation setting. However, at low gain setting, the topology in Figure 6-2a has a much better input linearity than in Figure 6-2b, where the signal is attenuated at the output rather than at the input. In this work, it is important to keep power dissipation low meanwhile maintaining an acceptable input P_{1dB}. Therefore, the topology in Figure 6-2a is chosen.

6.3.2. Circuit Design

Figure 6-3 shows the proposed differential RF VGA. The attenuator is realized with a tunable resistor network and the amplifier is implemented with a single-stage CE amplifier. The input matching of the CE stage is implemented by a series capacitor C_{in} and a parallel inductor L_{in}, resulting in a broadband input impedance, i.e. Z_{amp} = 100 Ω. Compared to classical series-L input matching, the employed input matching network exhibits a high-pass characteristic, which helps to flatten the gain response of the VGA. In addition, C_{in} serves as a DC decoupling capacitor, which enables independent biasing of the tunable resistor network and the CE stage. The output matching network consists of L_{OUT} and C_{OUT}, with which the CE stage presents an output impedance of 200 Ω at 30 GHz. The CE amplifier provides a fixed transducer gain of 11.1 dB at 30 GHz and consumes 7 mA from a 1.5 V supply voltage.

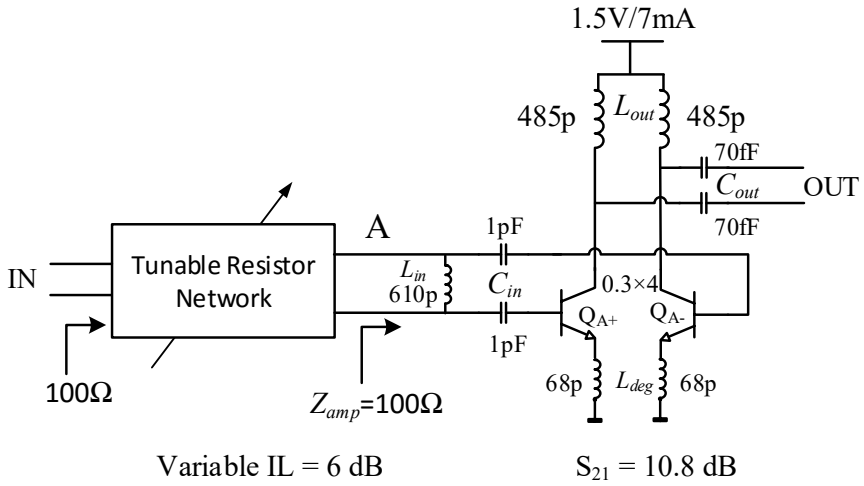


Figure 6-3. Schematic of the attenuation-based VGA.

Figure 6-4a shows the simplified model of the tunable resistor network, where the insertion loss is discretely controlled by the switches K_1 and K_2. As mentioned above, the attenuator is loaded with a broadband impedance Z_{amp} = 100 Ω. With K_1 on and K_2 off, ideally, the resistor network has no insertion loss. When K_1 is off and K_2 is on, the network presents IL = 6 dB. In both cases, the attenuator presents the same input impedance, i.e. Z_{in} = 100 Ω. In practice, K_1 and K_2 are implemented as HV-NPN devices (Figure 2-12). In order to improve tuning resolution, the tunable resistor network is finally realized as shown in Figure 6-4b. The HV-NPN devices are used as variable resistors R_{VC1} and R_{VC2}, with the on-resistance controlled by the variable voltage VC_1 and VC_2, respectively. The on-resistance and parasitic capacitance of the HV-NPN devices result in approximately 0.7 dB extra loss around 30 GHz. To realize fine enough gain step, i.e. less than 1dB/step, VC_1 and VC_2 are controlled by 3-bits digital signal, resulting in 7 steps variable IL from 0.7 dB to 6.7 dB, i.e. about 0.86 dB per step. In order to keep Z_{in} = 100 Ω for all attenuation settings, R_{VC1} and R_{VC2} have to be selected so that the overall series resistance R_S and parallel R_P (see Figure 6-4b) satisfy $2R_S + R_P // 100 = 100$ Ω. The base voltages VC_1 and VC_2 that are controlled by the 3-bits digital signal $A_{0,1,2}$ are generated as shown in Figure 6-5. As the switches are only used at DC, nMOS switches are used to reduce the current consumption.

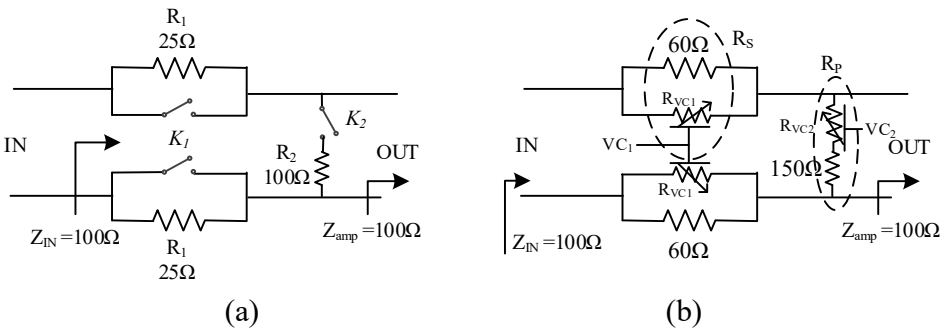


Figure 6-4. Implementation of the tunable resistor network: (a) simplified ideal model (b) practical implementation.

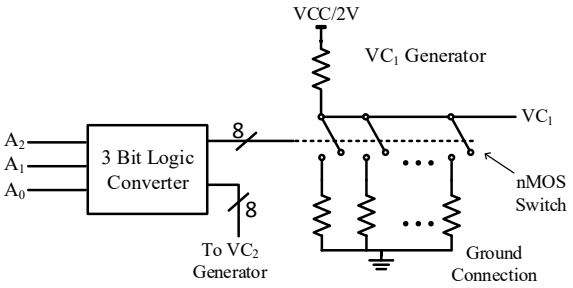


Figure 6-5. Control circuits that generate *VC1* and *VC2*.

6.3.3. Simulation Results

As the VGA is not fabricated standalone, simulation results are shown in this section instead of measurement results. Note that all the simulation results are based on post-layout simulation, i.e. the active cells are RC-extracted and the complete metal layers in the layout are characterized in EM software.

Figure 6-6 shows the simulated NF and gain of CE-stage, i.e. from node A to the output (see Figure 6-3). The simulation is performed with a 100 Ω input port and a 200 Ω output port. The CE stage has a transducer gain of 9.4-11.5 dB and an NF of 3-4 dB within 25-35 GHz frequency band. The input and output return loss are both better than -10dB over 25-35 GHz.

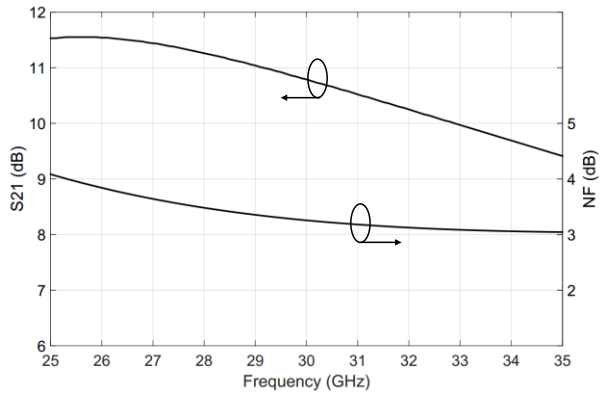


Figure 6-6. Simulated gain and NF performance of CE-stage (PortZ_{IN} = 100 Ω, PortZ_{OUT} = 200 Ω).

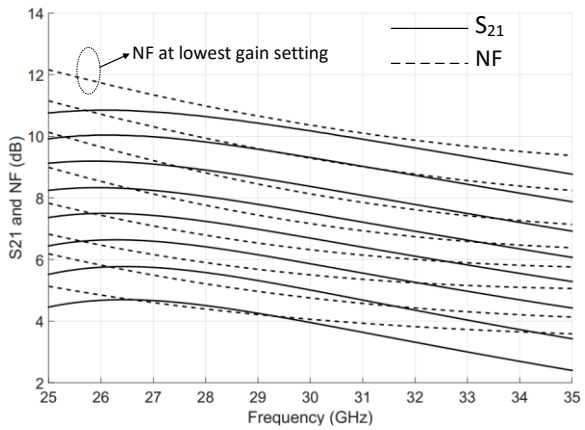


Figure 6-7. Simulated S_{21} of the complete VGA with 3-bit gain settings (PortZ_{IN} = 100 Ω, PortZ_{OUT} = 200 Ω).

Figure 6-7 show the simulated NF and gain of the complete VGA with 3-bit gain settings. The transducer gain of the VGA can be varied by 6.2 dB from 4 dB to 10.2 dB at 30 GHz, with 7 uniform gain steps. The input and output impedance of the VGA maintained almost constant with different gain settings, i.e. S_{11} < -15 dB and S_{22} < -10 dB at 25-35 GHz. At the highest gain setting, the simulated NF of the VGA is 4 dB at 30 GHz. Meanwhile, the simulated input P_{1dB} and IIP3 at

30 GHz are -4 dBm and +7.5 dBm, respectively. At the lowest gain setting, as expected, the VGA exhibits more or less 6.2 dB more NF than at high gain setting, i.e. 10.2 dB at 30 GHz. In trade off, the input P_{1dB} and IIP3 are improved to +2.2 dBm and +13.7 dBm respectively at 30 GHz. The two tone frequency offset for IIP3 simulation is 100 MHz. As indicated in Section 5.4.2, the low-power LNA/TTD frontend has an output P_{1dB} and OIP3 of -5.2 dBm and +4 dBm at its highest gain of 17.8 dB at 30 GHz (with 100Ω load). In this case the VGA will operate in low gain setting (input P_{1dB} = + 2.2 dBm, IIP3 = +13.7 dBm). As a result, the input P_{1dB} and IIP3 of the whole RF chain are limited by the LNA/TTD frontend, which eventually is limited by the low power LNA.

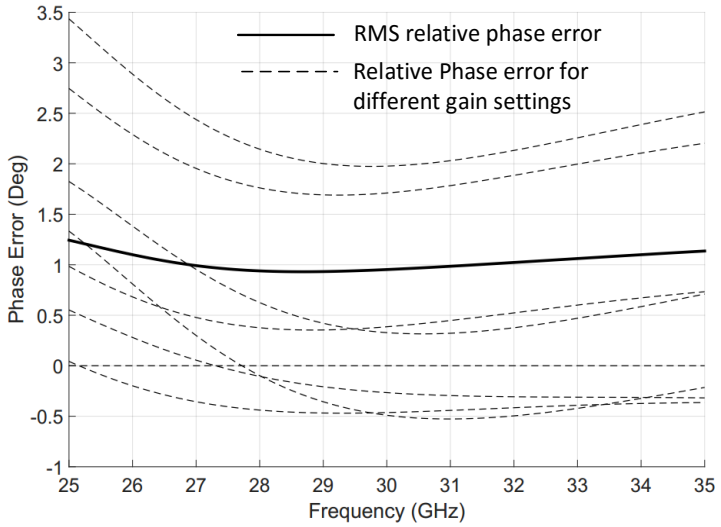


Figure 6-8. The simulated relative phase error of the VGA for different gain settings.

As mentioned above, the VGA should have a constant insertion phase during the gain settings. Figure 6-8 shows the relative insertion phase error over different gain settings. It can be seen that the RMS phase error of the VGA is less than 1.5 degree over 25-35 GHz.

6.4. Design of Mixer and Buffer

6.4.1. Circuit Design

Figure 6-9 shows the schematic of the differential mixer and voltage buffer. The mixer employs a double-balanced structure to reduce LO and RF leakage into IF output. To boost the linearity and input P_{1dB} of the mixer, the G_m stage is removed, leaving only switching pairs to mix the signal. Additionally, a series resistor R_1 is added at the input to further improve the mixer linearity. The device sizes of the switching pair, i.e. Q_1-Q_2, are chosen to make a trade-off between NF and linearity. For a fixed LO power, a smaller switching device results in a larger LO swing, reducing the equilibrium time and NF. However, for better linearity and large signal performance, a larger device is preferred as it can handle a larger biasing current and exhibit a lower knee voltage. Due to the low impedance of the CB configuration, the input impedance of the mixer, even taking into account of R_1, is only 18 Ω. The input impedance matching will be discussed in the next section. To improve the linearity of the mixer, the voltage headroom must be maximized. At the input, it is achieved by using a center-tapped inductor, i.e. L_1, to flow the tail current instead of using an active current source. Additionally, the switching pairs Q_1-Q_2 are implemented as HV-NPN devices, making it possible to bias the mixer with a 2 V voltage supply. The output LC tank, i.e L_2 and C_2, has a resonant frequency at 11 GHz. The mixer in active mode consumes 46 mW power, i.e 23 mA×2 V. Note that the global voltage supply of the 2-by-2 phased array receiver will be 2V. As the RF frontend operates at 1.5V, extra RC networks will be added between the RF frontends supply and the global voltage supply. This helps to reduce the undesired signal coupling between different receiver circuits through the power supplies.

The voltage buffer uses the super-emitter follower structure, which employs a negative feedback structure to increase the input impedance, reduce the output impedance and minimize the voltage error between the input and the output. The linearity of the voltage buffer is limited by the output voltage headroom at node X, which is finally determined by the knee voltage of Q_3 and Q_4 and the supply voltage. Larger Q_3-Q_4 size help reduces knee voltage and improve the linearity, but also results in larger parasitic capacitance that limits the loop gain and bandwidth. With a moderate trade-off, Q_3-Q_4 are designed with 0.3 um x 4 um dimension, which results in 0.3 V knee voltage at 8.5 mA collector current. Given the supply voltage of 2 V, the maximal available voltage headroom of the

buffer is 1.4 V_{pp} (peak-to-peak voltage), resulting in approximately +4 dBm output P_{1dB} with a 100 Ω differential load. To stabilize the voltage gain of the mixer, a parallel load resistor R_G is added at the input of the buffer. R_G also reduces the quality factor of the LC tank, increasing the BW of the IF signal. The complete mixer and buffer consume 40 mA from a 2 V power supply.

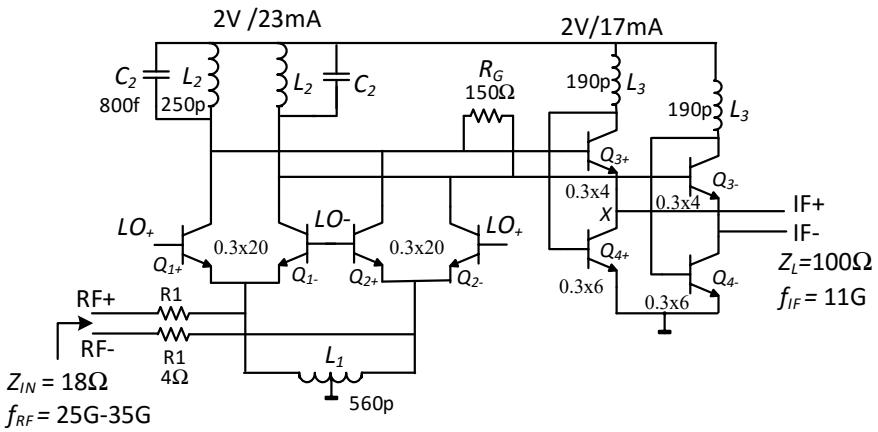


Figure 6-9. Schematic of the differential mixer and voltage buffer

6.4.2. Simulation Results

Figure 6-10 shows the simulated conversion gain and single-side-band (SSB) NF of the proposed mixer (including buffer). To cover 25-35 GHz RF frequencies at the input, simulations are performed in 3 cases: a) f_{RF} = 23-27 GHz, f_{LO} = 14 GHz b) f_{RF} = 28-32 GHz, f_{LO} = 19 GHz, and c) f_{RF} = 33-37 GHz, f_{LO} = 24 GHz. For example, in case (b) the incoming RF signal has a center frequency of 30 GHz and a signal BW up to 4 GHz. The LO frequency is set to 19 GHz to generate an IF signal centered at 11 GHz. In all cases, the mixer exhibits approximately -2 dB power conversion gain, 5.2 dB voltage conversion gain, and a single side band NF (NF_{SSB}) of 13 dB NF at the center frequency (f_{IF} = 11 GHz). The difference between the power conversion gain and the voltage conversion gain is more or less fixed to 7.4 dB, which can be explained by the ratio between the input impedance and the load impedance, i.e. $10\times\log10(Z_L/Z_{IN}) = 10\times\log10(100/18) = 7.2$dB. The conversion gain BW of the mixer is larger than 4 GHz.

Within the whole 25-35 input frequency band, the simulated input P_{1dB} of the mixer is higher than +4.2 dBm and the simulated IIP3 is better than +13.5 dBm.

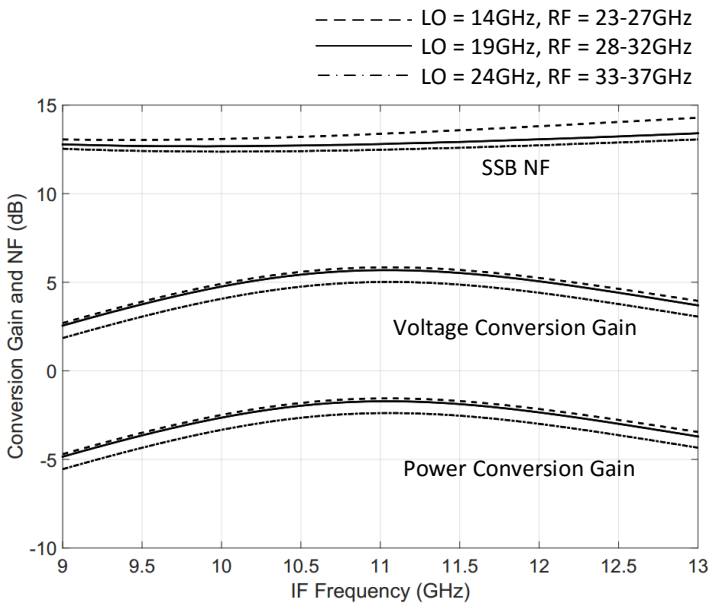


Figure 6-10. Simulated voltage and power conversion gain and NF of the mixer (including buffer) with 3 LO/RF frequency settings.

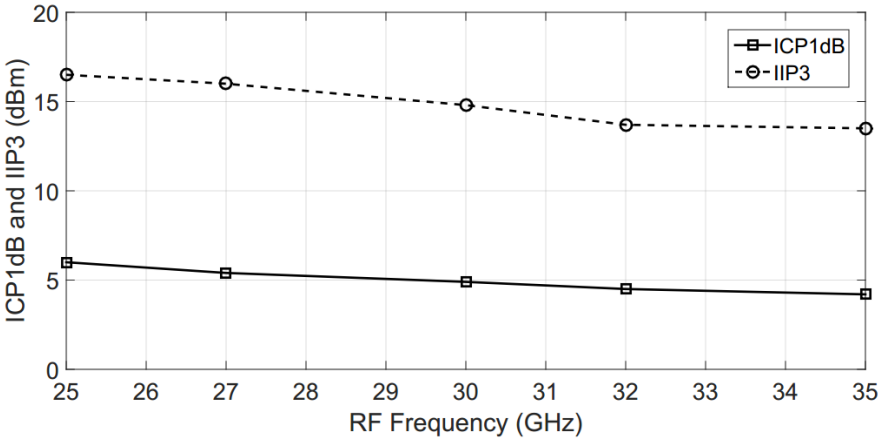


Figure 6-11. Simulated input P_{1dB} and IIP3 of the mixer (including buffer) versus input RF frequency, the LO frequency is adjusted to make f_{IF} = 11GHz.

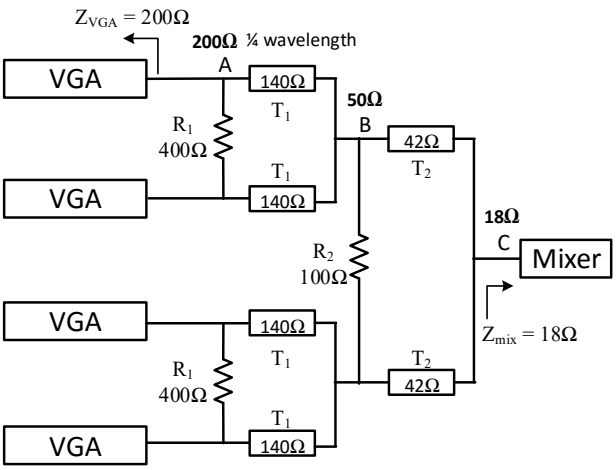


Figure 6-12. Design of 2-stage Wilkinson power combiner

6.5. Design of Power Combiner

To combine the 4 RF channels before the mixer, a power combiner is required. A Wilkinson power combiner is used for its high isolation between different channels, which is crucial to minimize the degradation of TTD performance due to the undesired coupling from the other channel.

6.5.1. Impedance transformation

The output impedance of the VGA is approximately 200 Ω while the input impedance of the mixer is only 18 Ω. If not matched properly, given a large physical distance between these blocks in the layout, a large power reflection can occur. Fortunately, this issue can be significantly mitigated by a 2-stage Wilkinson combiner. As shown in Figure 6-12, the impedance level at node A, B, and C are set to 200 Ω, 50 Ω, and 18 Ω to perform the broadband impedance matching. The characteristic impedance of T_1, accordingly, equals to $\sqrt{2 \times 200 \times 50} \approx 140$ Ω. Similarly, T_2 should has a characteristic impedance of $\sqrt{2 \times 50 \times 18} \approx 42$ Ω. The whole Wilkinson combiner is fully differential. The differential transmission line T_1 and T_2 are realized in top metal layer, i.e. M6, using coplanar waveguide (*GSSG* configuration). The complete Wilkinson combiner occupies 1.8×0.5 mm^2 chip area.

6.5.2. Simulation Results

The 2-stage Wilkinson combiner is fully characterized in EM software Agilent Momentum. The generated 5-port S-parameters dataset is simulated in the test-bench shown in Figure 6-13a. As shown in Figure 6-13b, within the 25-35 GHz frequency band, the insertion loss responses for 4 channels are almost identical and equal to 2.5-3 dB. Both the input and output return loss are well below -10dB. The insertion loss responses for 4 channels are almost identical. Note that due to the power splitting nature, the simulated transducer gain for an individual channel, e.g. S_{51}, is 6 dB worse than the real insertion loss [32]. The combiner also achieves good isolation within 25-35 GHz between any of two channels, i.e. S_{ij} < -25 dB, where i,j = 1,2,3,4.

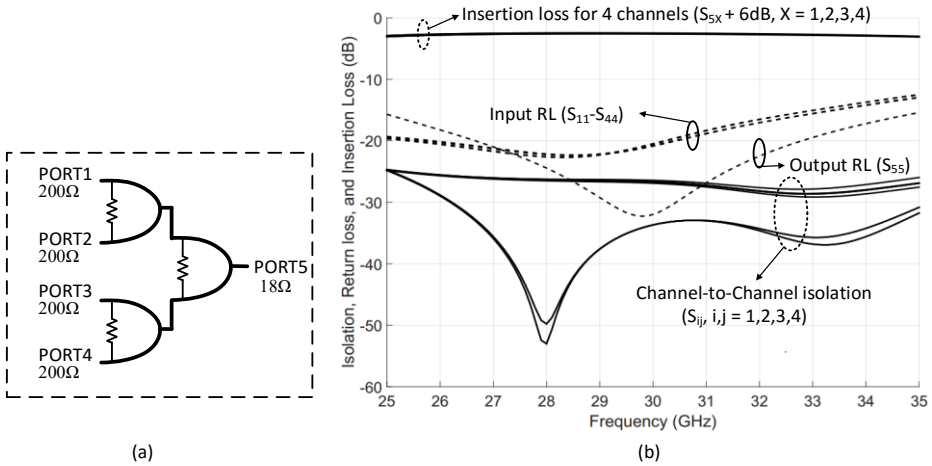


Figure 6-13. (a) Simulation setup (b) Simulated return loss, insertion loss and channel-to-channel isolation for the designed 4:1 Wilkinson combiner.

6.6. Measurement Results

Figure 6-14 shows the die photo of the fabricated 2×2 phased array receiver, with a total chip area of 2.6 mm × 2.6 mm. An on-chip SPI is used to control all the delay and gain settings of the receiver, i.e. in total 32 bits. The core of the RF frontend operates at 1.5 V supply, and extra *RC* network is added at the V_{CC} of each RF circuit block to minimize the undesired coupling between different RF circuits through V_{CC}. This increases the external applied V_{CC} of the RF frontends to 1.8 V. In practice, a 2V global voltage supply will be used for the receiver, which will directly supply the mixer/buffer and generate the 1.8V V_{CC} for the RF

frontends using a regulator. As a result, the effective total power dissipation of the 2×2 phased array receiver is 244 mW (2 V × 122 mA, i.e. 82 mA from the 4 RF frontends and 40 mA from the mixer/buffer). During the measurement, the available power of the LO signal up to the LO pad is +5.2 dBm. The NF measurement of the receiver could not be performed at the time the thesis was written, due to the lack of the 11 GHz pre-amplifier, which is necessary to perform NF measurement calibration. Moreover, by measuring one receiver channel at a time, the Wilkinson combiner will introduce an extra 6 dB signal attenuation, which will significantly increase the receiver NF. The simulation results indicate that the double side band NF (NF_{DSB}) of the complete 2-by-2 receiver ranges from 3.2-4 dB over 25-34 GHz.

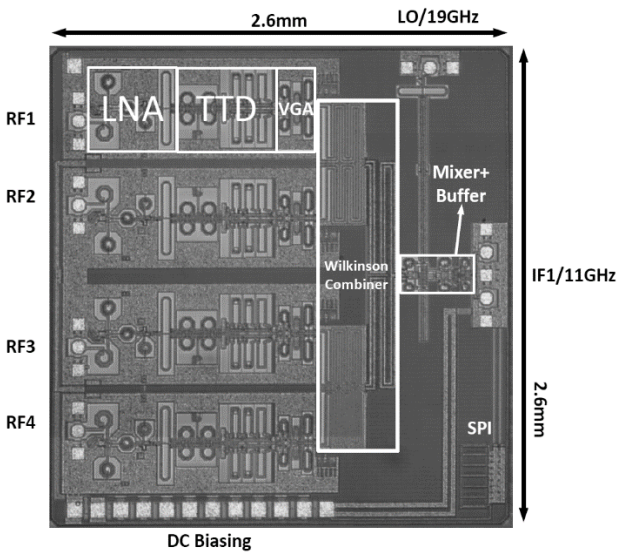


Figure 6-14. Die photo of the designed 2×2 TTD phased array receiver.

6.6.1. Conversion gain and input return loss

The conversion gain of the phased array receiver is measured using network analyzer PNA-X using offset frequency function. Due to the limitation of the probe-on measurement, only one receiver channel is measured at each time. The measurement is performed at the highest gain setting of the VGA and the lowest insertion delay of the TTD phase shifter (control code '00000'). Figure 6-15 shows the measured single channel RF-IF_1 conversion gain of the receiver over different IF_1 and LO settings. Each solid curve in the figure is measured by applying a

fixed LO frequency while sweeping the RF frequencies. From left to right, the LO frequencies are set to 14-24 GHz with 1 GHz step per curve. As shown in the figure, each solid curve more or less peaks at IF_1 = 11 GHz and has an average -3dB BW of 3 GHz. By connecting all the points where IF_1 = 11 GHz, the dashed curve shows the fixed-IF_1 conversion gain of the single channel receiver.

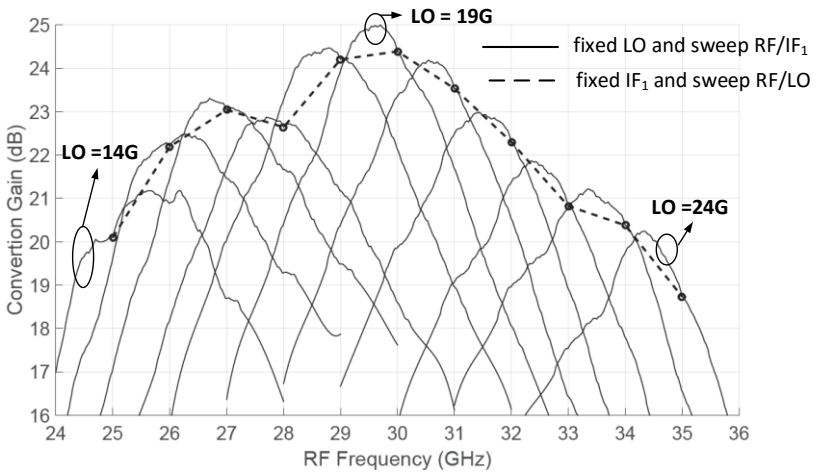


Figure 6-15. Measured conversion gain as a function of input RF frequency: Solid: with fixed LO and sweep RF and IF1; Dash: with fixed IF1 and sweep RF and LO.

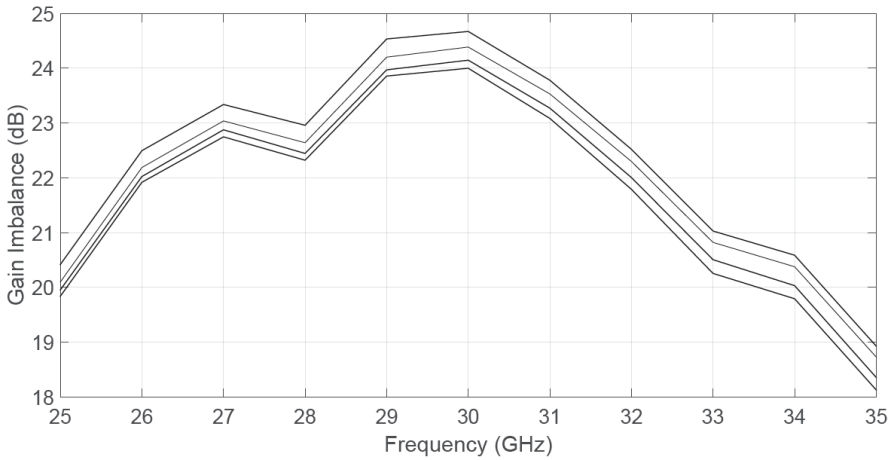


Figure 6-16. Measured fixed-IF Conversion gain for 4 channels.

Figure 6-16 plots such fixed-IF_1 conversion gain from 4 different channels. It can be seen that the phased array receiver provides more than 18 dB conversion gain to applications that locate at 25-35 GHz frequency range, and the gain variation between different channels is less than 0.6 dB. Note that the gain shown in Figure 6-15 and Figure 6-16 is based on single channel measurement. If the 4 channels are summed constructively, the array gain of the complete phased array receiver will be 6 dB more, i.e. > 30 dB at 30 GHz.

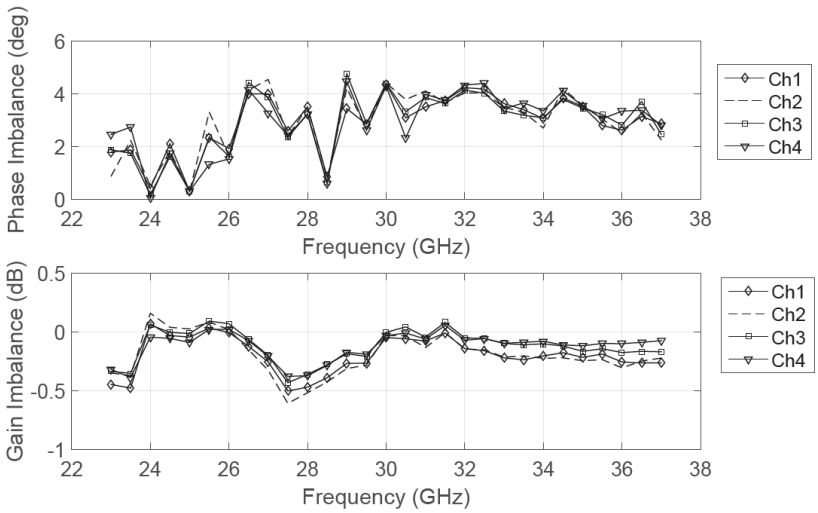


Figure 6-17. Measured phase and gain imbalance between two differential output.

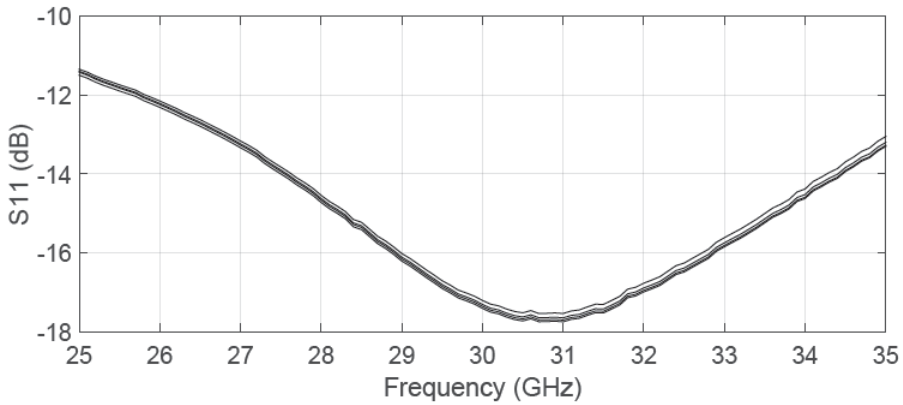


Figure 6-18. Measured S_{11} performance over 4 different channels.

Figure 6-17 shows the phase and gain imbalance at the differential IF_1 output. Over the 4 channels, the differential amplitude and phase imbalance are within 0.6 dB and 5 degrees, respectively. Figure 6-18 shows the measured input return loss at 4 different RF channel inputs, which is better than 10 dB at 25-35 GHz frequency band. In fact, due to the large isolation of the LNA, the input return loss of the whole receiver is almost solely determined by the LNA. As a result, the S_{11} results shown in Figure 6-18 are almost unchanged over the different delay, gain, and LO settings.

6.6.2. TTD performance

The on-chip SPI is found not working properly during the measurement. As a result, the digital control signal for delay and gain settings could not be sent into the circuit. Fortunately, for delay settings, the specific control bit from '0' to '1' could manually be flipped by applying laser cut at the specific inverter, i.e. destroy the NMOS device of the inverter to make the output flip up to '1'. The laser cut operation, however, could not be undone and sometimes it fails because the laser could also destroy the surrounding circuits. As a result, with limited circuit samples, we could only measure 11 delay settings out of in total 5-bits 31-steps delay settings. Figure 6-19 shows the relative delay responses of a single channel receiver at 23-37 GHz. The measured total variable delay is 20.5 ps. The corresponding control code for each delay setting is shown at the right side of the figure.

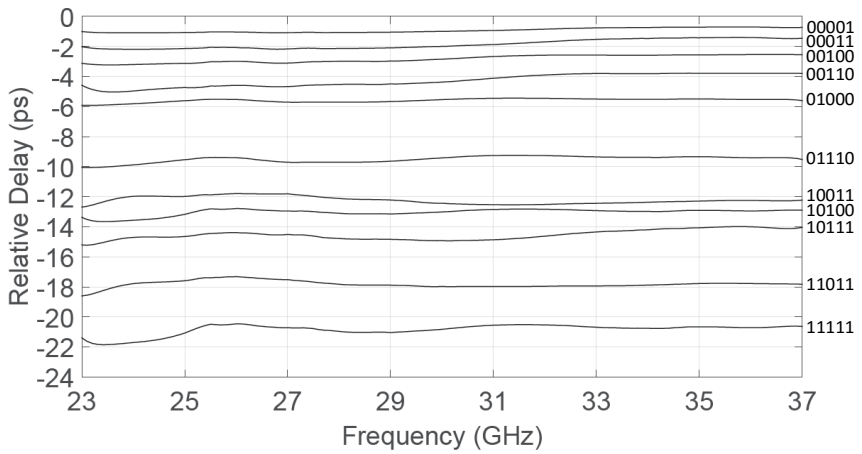


Figure 6-19. Measured relative delay of single channel receiver.

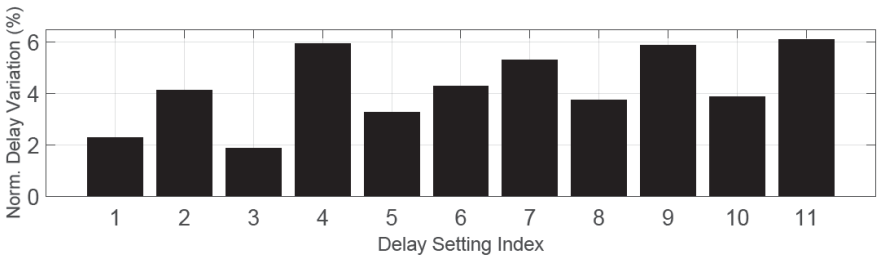


Figure 6-20. Measured normalized delay variation of single channel receiver.

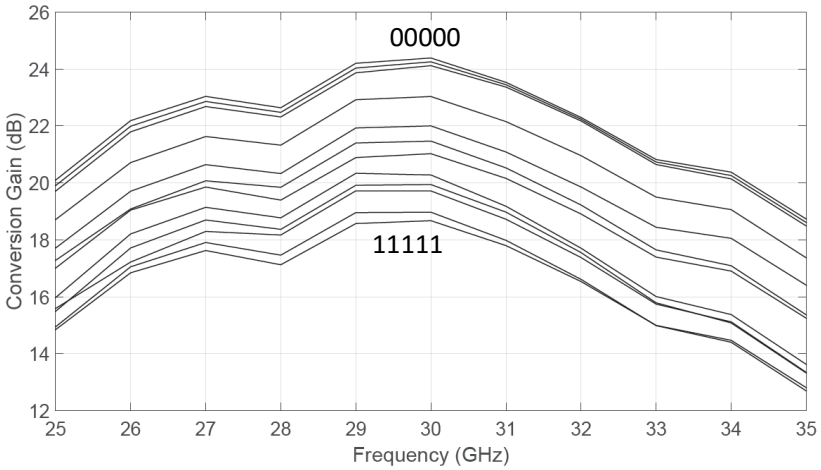


Figure 6-21. Measured conversion gain over different delay setting.

To evaluate the flatness of the achieved delay response, Figure 6-20 shows the normalized delay variation (NDV_{PS}) for each delay settings, where n is the delay setting index. The measured worst-case NDV_{PS} of the proposed TTD phased array receiver is 1.23 ps, i.e. 6% of the total achieved variable delay. The amplitude variation due to different delay settings ranges from 4.5-6 dB within 25-35 GHz (see Figure 6-21). The Larger delay setting results in lower conversion gain as the signal has to travel through more lossy delay circuits, e.g. inductance, capacitance, and switches.

6.6.3. Gain Settings

The VGA settings, however, could not be easily set by laser cut. The logic control circuits for gain settings are buried under the 2 top metal layers thus invisible from the microscope. Moreover, the logics were put very compactly in the layout,

making it difficult to locate the desired laser cutting point. Therefore, an alternative method is used, but with which only the highest and lowest gain settings can be measured. The default VGA setting is the highest gain setting, where the control voltage VC_1 = 2 V and VC_2 = 0 V in Figure 6-4. To achieve the lowest gain, VC_2 is set to 2 V by laser-cutting the ground connection of the VC_2 generation circuit (see Figure 6-5), and the VC_1 is set to 0 V by simply breaking the feeding line of VC_1 toward R_{VC1}.

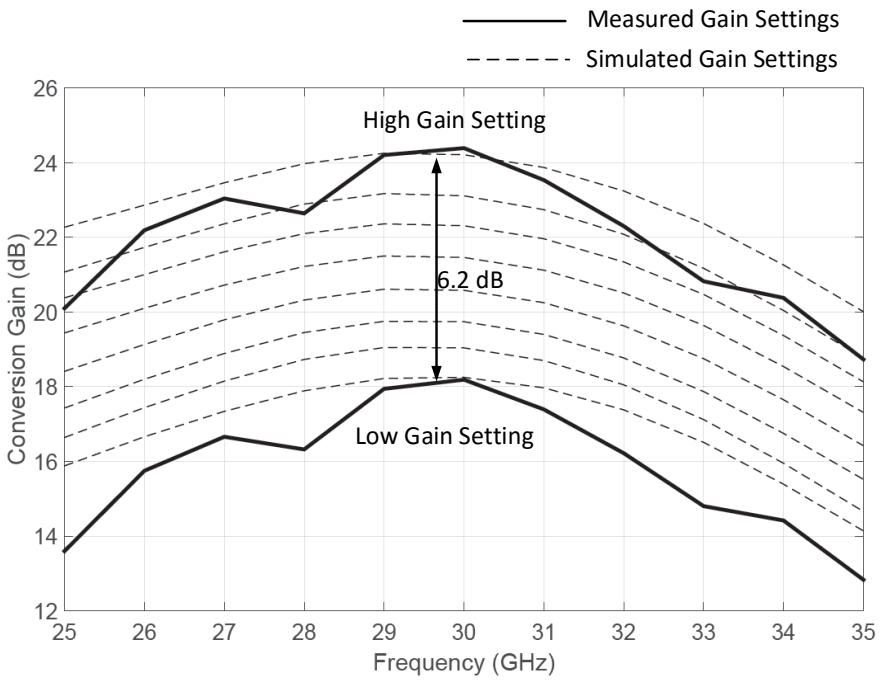


Figure 6-22. Measured and expected conversion gain over different gain setting.

The measured and simulated conversion gain over different gain settings are shown in Figure 6-22 (two solid curves are measured data, and the dash curves are simulated gain responses). It can be seen that the measured two gain settings (highest and lowest setting) agree well with the simulation. The measured variable gain range of the VGA is 6.2 dB. As a result, by properly choosing VGA settings for different TTD settings, the amplitude variation of the receiver should be reduced within 1 dB.

6.6.4. Isolation and spurs

The isolation between differential channels are measured by S-parameters S_{ij}, where i,j are corresponding to the channel number from 1 to 4 (see Figure 6-14). As shown in Figure 6-23, the measured isolation between the non-adjacent channels is more than 38 dB from 20-40 GHz. The isolation between the adjacent channels, however, is limited by the direct coupling through the two RF probes thus could not be measured accurately. This can be verified by measuring only the coupling between two floating probes with the same physical distance as two adjacent channels. For instance, the solid line shown in Figure 6-23 is the measured S_{23} but with both the probes floated in the air. It is shown that the coupling of probes is as large as -25 dB near 30 GHz, which dominates the isolation between adjacent channels.

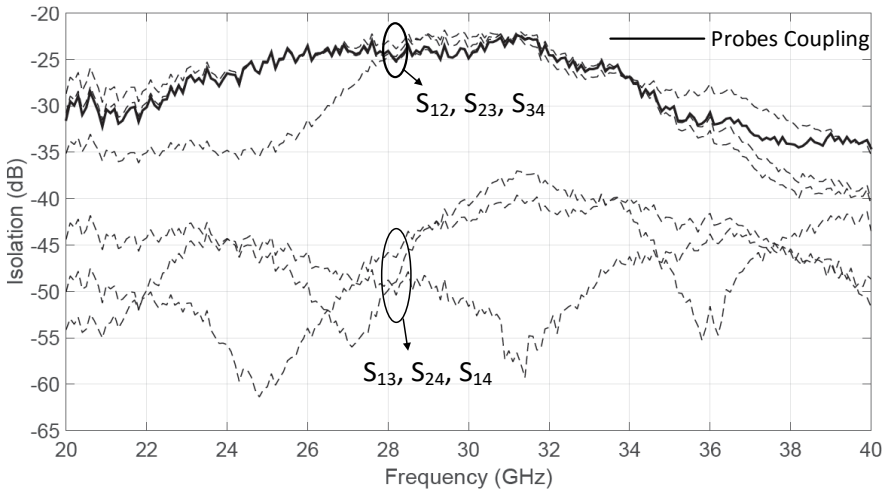


Figure 6-23. Measured channel to channel isolations of the 2-by-2 phased array receiver

6.6.5. Compression point and linearity performance

Figure 6-24 shows the measured input P_{1dB} and IIP3 of the single channel receiver over the frequency (with the highest gain setting and the lowest insertion delay setting). Within the 25-35 GHz frequency band, the measured worst-case input P_{1dB} and IIP3 of the single channel receiver are -24 dBm and -16 dBm, respectively.

The two tone frequency offset for IIP3 measurement is 100 MHz. As the measurement is performed on one channel at a time, the receiver P_{1dB} and linearity are limited by the RF frontend.

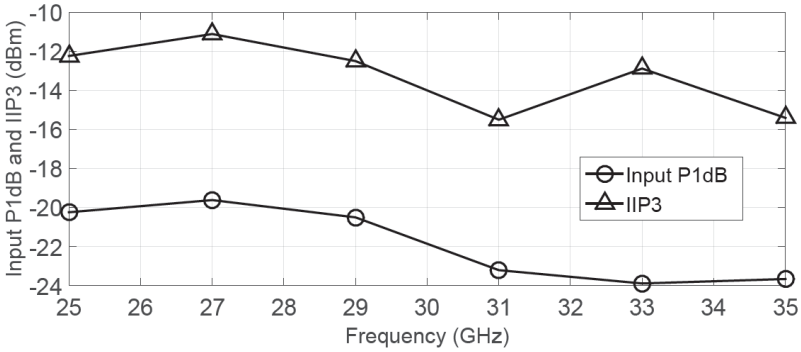


Figure 6-24. Measured input P_{1dB} and IIP3 of the single channel receiver.

6.6.6. Spur and reverse isolation

During the single channel measurement, the largest spur at the output port locates at the LO frequency. With -30 dBm RF input power, the spur is -25 dBc compared to the desired IF_1 signal. For instance, with f_{RF} = 30 GHz and f_{LO} = 19 GHz, before de-embedding out the 6dB extra loss of Wilkinson combiner, the IF_1 signal (11GHz) at the output port is around -10.5 dBm and the LO spur is around -35.5 dBm. Compared with the input LO level, i.e. +5.2dBm, the double-balanced mixer has an LO feedthrough rejection of more than 40dB. The IF_1-RF isolation is more than 60 dB.

6.7. Conclusion and Benchmarking

6.7.1. Conclusion

A 2-by-2 TTD phased array receiver has been realized using 0.25 μm SiGe:C BiCMOS process. The receiver presents 24dB peak conversion gain per channel and 30dB peak array gain. From 25 GHz to 35 GHz, each receiver channel provides more than 18dB conversion gain, and can perform 5 bits 20.5ps variable delay and 3 bits 6 dB variable gain. With such a phased array receiver system, a beam-squint free beam-steering with +/-60 degrees can be achieved by a 2-by-2 antenna array with 5 mm spacing, which is enough for most Ka-band applications. The

measured worst-case delay variation of the receiver is 6% over 23-37 GHz. The 4.5-6 dB amplitude variation due to different delay settings can be compensated by the VGA. A constant input impedance, i.e. |S11|< -11 dB, is maintained for all delay settings within 25-35 GHz frequency, and the in-band worst case input P_{1dB} and IIP3 of the single channel receiver are -24dBm and -16dBm. The total phased array receiver consumes 244 mW DC power and has a die area of 2.6x2.6 mm^2.

6.7.2. Benchmarking

Table 6-1 shows the benchmark with other fully integrated TTD phased array receiver and TTD frontends. The proposed work has an improved performance regarding conversion gain, in-band NDV_{PS} (delay variation in the percentage of total variable delay), delay resolution and low power dissipation.

Table 6-1. The benchmarking with other TTD phased array receiver above 10 GHz

	[12]	[13]	[11]	This work
Average channel gain (dB)	~10	~12	9	21
-3dB Gain BW (GHz)	1-13	30-40	N.A	25.5-32.5
Delay BW[1] (GHz)	1-15	30-40	1-15	23-37
Total delay (ps)	64	54	225	20.5
NDV_{PS}(%)	~12	N.A.	~14	6
Input P_{1dB} (dBm)	-23	N.A.	N.A.	-24
P_{DC} per RF channel (mW)	87.5	104	138	37
Resolution (ps)	4	18	15	0.66
Area per channel[2] (mm^2)	>1.5	>1.4	>1.2	0.48

[1] Within which the delay variation is evaluated

[2] Estimated core size of one channel RF frontend

Mark with "~" is estimated from the measurement results

7. Conclusions and Future Work

7.1. Conclusions

The recent development of BiCMOS technology enables designing high performance phased array receiver building blocks, e.g. LNA and phase shifters.

Wideband phased array receivers not only meet the need for high-speed data transfer but facilitate a generic solution for multi-applications operating in different frequencies. However, in order to avoid beam-squint effect, TTD phase shifters are required, providing flat delay response over the operating frequencies.

In this work, Chapter 1 briefly discussed the broadband phased array system concept. Two types of delay circuit cells were analyzed, including the correlation between their cut-off frequency and delay variation. Some key features of the used BiCMOS technology were covered, including an active device, passives, and RF switches.

In chapter 3, three alternative Ka-band LNAs has been realized using 0.25 μm SiGe:C BiCMOS process. By using simultaneously noise and power matching as well as the noise matching between CB and CE transistors, the proposed LNAs achieve 2-2.5 dB NF at 30 GHz. Moreover, the high gain and low power LNAs achieve more than 25 dB gain at 30 GHz while maintaining a -3dB gain bandwidth around 10 GHz.

In chapter 4, a delay variation cancellation technique has been proposed, which cancels the delay error by combining two types of delay cell, which have opposite delay pattern over the operating frequencies. Based on the delay variation

cancellation technique, a compact Ka-band active TTD phase shifter and a wideband TTD receiver frontend have been realized using 0.25 μm SiGe:C BiCMOS process. The TTD phase shifter achieves a flat delay response from 20 GHz to 40 GHz with only 6.6% normalized delay variation. A constant input impedance, i.e. $|S_{11}| < -15$dB, is maintained for all delay settings within 20-40 GHz frequency band. The TTD receiver frontend presents 10 GHz gain BW and 15 GHz flat delay BW with only 3.5% normalized delay variation.

In chapter 5, an alternative delay variation reduction technique – broadband matching technique has been proposed. Based on the broadband architecture, a passive broadband TTD phase shifter and a wideband TTD receiver frontend have been realized using 0.25 μm SiGe:C BiCMOS process. The passive TTD phase shifter achieves a flat delay response from 10 GHz to 50 GHz with only 3.9% NDV. A constant input impedance, i.e. $|S_{11}| < -10$dB, is maintained for all delay settings within 10-40 GHz frequency band. The TTD receiver frontend presents 11.5 GHz gain BW and 14 GHz flat delay BW with only 5.4 % normalized delay variation. Compared to other existing TTD work above 10 GHz, both of the proposed standalone TTD phase shifters has an improved performance regarding flat delay bandwidth, delay variation, delay resolution, and the chip area.

In chapter 6, a 2-by-2 TTD phased array receiver has been realized using 0.25 μm SiGe:C BiCMOS process. The receiver presents 24dB peak conversion gain per channel and 30dB peak array gain. Over 25-34 GHz, each receiver channel provides more than 20dB conversion gain, and can perform 5 bits 20.5ps variable delay and 3 bits 6 dB variable gain. Within the bandwidth, the measured worst-case delay variation of the receiver is 6%. A constant input impedance, i.e. $|S11| <$ -11 dB, is maintained for all delay settings, and the in-band worst case input P_{1dB} and IIP3 of the single channel receiver are -24dBm and -16dBm.

7.2. Future Work

This thesis presents building blocks for wideband TTD phased array receiver. As future work, several remaining tasks and interesting issues can be studied further:

- To demonstrate the wideband beamforming capability, the presented 2-by-2 TTD phase shifter needs to be packaged and connected with an antenna array.

The expected measurement results should indicate that the optimum beam angle does not change with the signal frequency of 25-35 GHz.

- For research purposes, the biasing voltages and currents in this work are controlled externally. In reality, however, dedicated biasing circuits need to be included, which should be independent of the power supply, temperature and process variation.

- As discussed in Chapter 4 and 5, the TTD phase shifter could achieve less than 5% normalized delay variation over 10-50 GHz. However, to achieve 32.8ps total variable delay, the phase shifter presents more than 15 dB insertion loss. As the insertion loss will be scaled up with the total variable delay, for a system with large array size, a lot of gain stage and power consumption is needed to compensate for the TTD insertion loss. One interesting solution for this scaling issue is to make the current 2-by-2 phased array frontend scalable as a module and realize the delay between different modules off-chip. However, there are some challenges that need to be solved, e.g. the off-chip delay also needs to be variable and synchronized with the on-chip delay settings.

- The TTD phase shifter can also be applied in phased array systems where a large simultaneous signal bandwidth is required, e.g. pulse and imaging system. These systems require a constant group delay over a large frequency span, which can be fulfilled by the TTD phase shifters.

Abstract

Integrated Millimeter-Wave Broadband Phased Array Receiver Frontend in Silicon Technology

The investigation of high-speed radio-frequency (RF) transceivers becomes popular nowadays due to the increasing need for high-speed wireless data transfer. Millimeter-waves frequency offers larger available signal bandwidth and is therefore attractive for high-speed transceivers. However, the high path loss of the mm-wave frequency requires a transmitter with high output power and a receiver with high sensitivity, both are challenging in mm-wave frequency circuit design. One effective way to compensate high path loss and improve the signal to noise ratio is to employ phased array techniques.

This thesis aims to carry on research in high performance wideband phased array receiver at Ka-band. Compared to narrow-band receivers, wideband phased array receivers allow covering of multiple bands without tuning, e.g. point-to-point (P2P) communication with various bands between 7GHz and 40GHz. As classical phase shifters can only be used to approximate the required delay in a narrow bandwidth, true-time-delay (TTD) phase shifters with low delay error are required to avoid beam-squint phenomenon. Moreover, to reduce the cost and increase integrated functionality, silicon-based technology i.e. 0.25 μm SiGe: C BiCMOS, has been used in this thesis. Compared to III-V devices, silicon-based technologies have higher intrinsic noise, higher substrate loss and larger parasitic capacitance to the substrate. As a result, the main research challenge of this thesis is how to design a wideband phased array receiver at Ka-band in silicon with competitive RF performance. More specifically, the target is to design wideband low noise amplifiers (LNA) in silicon with a low noise figure (NF) at Ka-band and wideband TTD phase shifters with low in-band delay error.

From the circuit level, this thesis compares and analyze different mm-wave LNA topologies. To optimize noise performance, different noise matching techniques are investigated during the LNA design. Based on these investigations, three alternative Ka-band LNAs has been realized. By using simultaneously noise and

power matching as well as the noise matching between cascode transistors, the proposed LNAs achieves 2-2.5dB NF at 30GHz. Moreover, the high gain and low power LNAs achieve more than 25dB gain at 30GHz meanwhile maintain a -3dB gain bandwidth around 10GHz.

For the TTD phase shifters, the thesis investigates different delay cells and for each delay cell, the correlation between delay variation and cut-off frequencies is derived. To reduce the in-band delay error of TTD phase shifters, the thesis explores two different delay error reduction techniques. The first technique is delay variation cancellation technique, which cancels the delay error by combining two types of the delay cell. Based on this technique, an active TTD phase shifter is realized, which achieve a flat delay response from 20GHz to 40GHz with only 6.6% normalized delay variation (NDV). The second technique is broadband matching technique. Based on this technique, a passive broadband TTD phase shifter is realized, which achieves a flat delay response from 10GHz to 50GHz with only 3.9% NDV.

Moreover, the thesis integrates two alternative TTD frontends (LNA+TTD). The high power frontend presents 10GHz gain bandwidth and 15GHz flat delay bandwidth with 3.5% NDV. The low-power frontend, consuming only 21mW power, presents 11.5GHz gain bandwidth and 14 GHz flat delay bandwidth with 5.4% NDV. Compared with other existing TTD receiver frontends, the proposed two TTD frontends have the best reported overall NF, linearity and TTD performance, i.e. the smallest delay variation over the largest BW.

From the system level, the thesis realizes and characterizes a complete 2-by-2 phased array receiver, The system-level characteristic and challenges are investigated, including biasing, isolation between various channels, power dissipation, and signal combining, etc.

Acknowledgements

When I started to write this thesis, I could not believe that my four years Ph.D. study was going to end so soon. In my last few months in Eindhoven, I started to miss this Ph.D. journey and all the people that helped me and encouraged me during this period.

First of all, I would like to express my special thanks to my first promoter Prof. Domine Leenaerts. Thank you for providing me such an interesting project. In fact, I did not have much experience in RFIC design when I started the project. Therefore, I was not so confident and even a bit worried that I would make lots of mistakes, which would make you upset. However, you were always patient with my 'entry level' questions. You guided me and gave me time to find the answers. I learned so much from you during our regular meetings, and you always encouraged me even when I told you that I may fail the first tape-out. I could never complete my Ph.D. dissertation without your continuous help and great support.

I am also truly grateful for my second promoter Prof. Peter Baltus. Actually, you already started to help me since my master study in 2008. You are so kind and helpful that even I have bothered you for more than seven years, you never rejected any of my requests. Your humor always made our technical discussions very enjoyable, and every time I got stuck in the project and felt depressed, you could always inspire me with so many possibilities.

My thanks also go to the associate professor Reza Mahmoudi, my daily supervisor in the first two years. You were always there to help us and you even helped me to present my first conference paper when I could not make it. Thank you for your time and effort. It was such a pity that we could not work together till the end, and I wish all the best to you.

Moreover, I would also thank the other members of the doctorate committee: Prof. F.E. van Vliet, Prof. G.M. Rebeiz, Prof. A.H.M. van Roermund, Prof. A.B. Smolders, and Prof. L.C.N. de Vreede for attending my Ph.D. defense.

I would like to express my gratitude also to the people in Catena, Sweden. During the exchange in Catena for the PAR4CR project, I enjoyed working there very much. I would like to especially thank Mats Carlsson. You provided me with a very interesting project, and we had a lot of great discussions. I really learned a lot from you and that project.

Also, special thanks go to the members in the MsM group. I would like to thank Margot for helping me to setup all the meetings and taking care of all the travelings. I would like to thank Jan for arranging PAR4CR exchange. I would like to thank Rainier for helping me solving all the nasty issues during the measurement. Especially, I would like to thank my 'roommates' Lu Chuang, Jaap Essing and Pooyan Sakian. Having you in the same office made my Ph.D. so enjoyable. I also want to thank Hao Gao for so much help not only in projects but also in living in Eindhoven. Additionally, I want to thank Pieter Harper, Eugenio Cantatore, Hans Hegt, Yu Pei, Zhe Chen, Xiangrong Zhang, Jun Wang, Song Ma, Shuang Song, and all the other MsM group members for all the valuable discussions and support during my Ph.D.. There were also many valuable technical discussions outside the group, from whom I learned a lot. For this, I would like to thank Ying Chen and Zizheng Cao.

Last but the most, I want to thank my family. I would like to thank my parents, who are always supportive through my life. And most importantly, I want to say thank you to my dear wife, Hong, for sharing our lives together. You always stand by me, which keeps me optimistic even when I had tough times. Only with your continuous and precious support, encouragement, patience and love that we could have a wonderful time together all those years and also make this dissertation possible.

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