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Codesign of Electrically Short Antenna–Electronics Interfaces in the Receiving Mode

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Abstract—The aim of this brief is to point out the importance of codesigning electrically short antenna-electronics interfaces as a way to improve the system performance. This can be achieved if both the antenna and electronic circuit designer have a common optimization target. In this brief, the codesign principles are presented for antenna systems in the receiving mode, which includes reception of wireless information and wireless power. A general interface analysis is carried out, suggesting that the choice of interface impedance plays a crucial role in the optimization procedure and depends on the preferred signal quantity of the electronic circuit. This allows to effectively improve design criteria such as noise figure, power efficiency and sensitivity without increasing the power consumption. Finally, two examples are treated to demonstrate the antenna-electronics codesign for the reception of wireless information (low-noise amplifier) and wireless power (radio-frequency energy harvesting).

Index Terms—Antenna, codesign, electronics, interface, low-noise amplifiers (LNA), radio-frequency (RF) energy harvesting.

I. INTRODUCTION

DURING the design process of a wireless system, the antenna and electronic circuit designers sometimes are operating independently from each other and considered to belong to separate disciplines. Both designers agree upon a common characteristic impedance (Z_0) of the antenna-electronics interface and subsequently optimize their part of the system. The electronic circuit often requires an impedance transformation network while the antenna usually is directly matched to the characteristic impedance of a transmission line to avoid propagation effects in the interface. Traditionally, this characteristic impedance is commonly assumed to be 50 Ω, without any further discussion. Although this standardization may be convenient from a measurement point of view, it is a rather uncomfortable assumption to make as it clearly cannot be the optimum impedance for all design challenges when for example considering noise performance, efficiency or antenna size.

By codesigning the antenna-electronics interface, both disciplines share a common optimization target and can agree on an alternative interface impedance to optimize the overall system
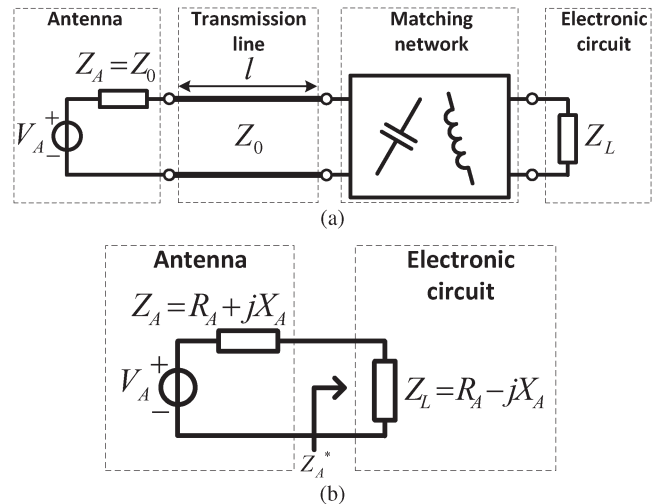
Fig. 1. (a) Conventional and (b) codesigned electrically short antenna-electronics interface in the receiving mode.

performance for a specific application. The choice of interface impedance plays a crucial role in the optimization of antenna systems in the receiving mode, which is the topic addressed in this brief.

II. CODESIGN PRINCIPLE

Codesigning the antenna-electronics interface involves optimizing the system performance by determining the optimum input impedance of the electronic circuit for a particular application and subsequently design the antenna accordingly. Let's first consider the need of the transmission line in the conventional interface, as shown in Fig. 1(a). If the length between the antenna and the electronic circuit is electrically short $(l < \lambda/10)$, then the propagation effects in the interface can be neglected as the voltage and current can be considered constant along the line [1]. This, for example, may be the case for integrated circuits (ICs) with on-chip antennas [2] and ICs that are directly integrated into an off-chip antenna, as demonstrated in [3] and [4].

The interconnection between the antenna and electronics then can be modeled as a simple wire or lumped elements instead of distributed elements. In this case there is no fundamental reason to use transmission lines and hence no need to impedance match to Z_0. This opens up the possibility to directly match the antenna to the electronic circuitry as illustrated in Fig. 1(b). The use of the matching network and transmission line is thus avoided, thereby eliminating the loss and noise that would otherwise be introduced by these networks. Although
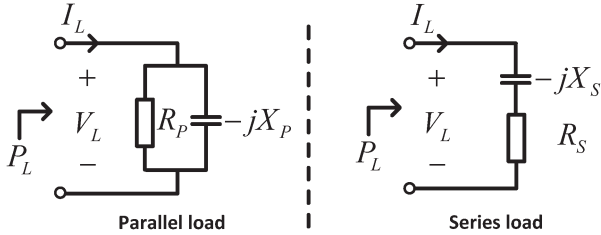
Fig. 2. Antenna load impedance equivalent model.

this non-50 Ω interface makes the verification process more complex as it may require an anechoic chamber [4] or nonlinear source-pull measurement [5], it also allows to increase the voltage or current at the antenna load (i.e., the electronic circuit equivalent input impedance) for the same available power at the antenna.

Before elaborating further on this topic, first a distinction has to be made between wireless power reception and wireless information reception.

A. Wireless Power Reception

The design goal for wireless power reception is obviously to transfer maximum power from the antenna to the electronics. When dc electric power is required, a rectifier can be directly conjugate matched to the antenna. In practice however, the rectifier is implemented using (Schottky) diodes or MOS transistors, which inherently are *voltage controlled* devices and require a minimum voltage to conduct current. This sets the second design condition that a sufficiently large voltage needs to be generated in order to *activate* the rectifier while simultaneously achieving maximum power transfer. This becomes the main design concern for applications with limited available power at the antenna, which is the case for highly sensitive RF energy harvesters and wireless implantable medical devices.

B. Wireless Information Reception

The reception of wireless information is fundamentally different from wireless power reception in the sense that information processing in principle does not require maximum power transfer. From the electronic circuit's point of view, the information in the field strength can be represented by either voltage or current and the designer has to choose which signal quantity represents the information in the most accurate way and which quantity is more favorable to measure with the electronics. The interface then has to be optimized to maximize this preferred signal quantity.

III. VOLTAGE, CURRENT AND INTERFACE IMPEDANCE

Optimizing the interface for maximum voltage or current is a matter of first optimizing the antenna load impedance. In many cases, the load for a given frequency range can be modeled as either a series or parallel combination of resistance and reactance (see Fig. 2). Depending on preference and application, one might be more convenient to use than the other, but both provide the same characteristics. In this brief, an antenna load impedance with capacitive reactance is assumed, which holds for the majority of ICs.

Without making any assumptions about the source, the power in the load can be expressed as

$$P_L = \left(1 - |\Gamma|^2\right) P_{\text{av}} \tag{1}$$

where $\Gamma = (Z_L - Z_A^*)/(Z_L + Z_A)$ is the power wave reflection coefficient [1], Z_A is the antenna impedance, Z_L is the antenna load impedance and P_{av} denotes the power available to the antenna. The current magnitude through the load then is equal

$$|I_L| = \sqrt{\frac{2\left(1 - |\Gamma|^2\right) P_{\text{av}}}{R_S}} \tag{2}$$

while the voltage magnitude across the load is

$$|V_L| = \sqrt{2\left(1 - |\Gamma|^2\right) P_{\text{av}} R_P}. \tag{3}$$

In both cases, a conjugate matched interface ($Z_A = Z_L^*$) produces the maximum voltage and current at a given antenna load, which is the first condition to optimize the desired signal quantity. Although this condition relates the *relative* impedance between the antenna and electronic circuit, the key point is that an additional increase in voltage or current can be achieved by correctly choosing at *which* impedance level conjugate matching occurs.

When assuming an ideal conjugate matched interface, the voltage across the parallel load terminals is given by

$$|V_L| = \sqrt{2P_{\text{av}} R_P}. \tag{4}$$

The voltage across the load of the equivalent series impedance is calculated using the resistance parallel-to-series conversion equation

$$R_P = (1 + Q^2) R_S \tag{5}$$

where $Q = (X_S/R_S) = (R_P/X_P)$. Note that this impedance conversion is only valid around the resonance frequency. The voltage in terms of the series load is then expressed as

$$|V_L| = \sqrt{2P_{\text{av}} R_S} \sqrt{1 + Q^2}. \tag{6}$$

Equation (6) indicates that the output voltage can be 'boosted' by increasing the Q-factor of the interface. It should be noted that this also requires a larger parallel load resistance R_P due to the equivalence of (4) and (6). Hence, when the available power and antenna load are fixed, one cannot increase the load voltage to higher levels by means of antenna design. *The designer therefore needs to design the electronic circuit for the largest R_P possible and subsequently codesign the antenna impedance for conjugate matching.* This conclusion is a key point that needs to be considered during the design procedure.

The load current can similarly be found by writing

$$|I_L| = \sqrt{\frac{2P_{\text{av}}}{R_S}} \tag{7}$$

and thus can only be maximized by minimizing R_S. This is equivalent to the following expression in terms of the parallel load

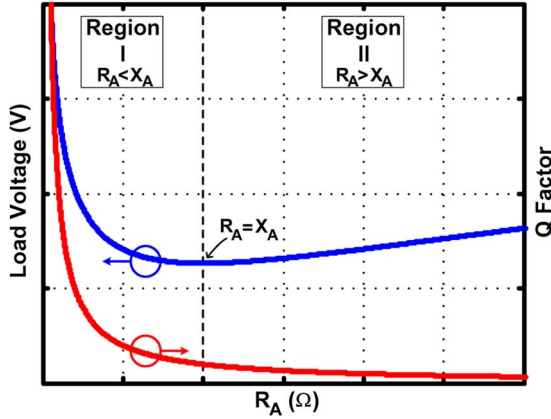$$|I_L| = \sqrt{\frac{2P_{\text{av}}}{R_P}} \sqrt{1 + Q^2}. \tag{8}$$

Fig. 3. Antenna load voltage versus antenna resistance for non-zero antenna reactance.

Fig. 4. Interface model of an inductively degenerated CMOS LNA directly connected to an inductive antenna including relevant noise sources.

Thus, the maximum voltage and current at the interface is set only by the antenna load impedance and the available power. The series and parallel load representations are tools to help the designer to analyze and find the required impedance.

The antenna impedance $(Z_A = R_A + jX_A)$ is found by determining the required ratio of the real and imaginary part of the load impedance. When considering voltage to be the signal quantity to maximize and assuming a conjugate matched interface $(X_A = X_S$ and $R_A = R_S)$, (6) can be rewritten as

$$|V_L| = \sqrt{2P_{av}\left(\frac{R_A^2 + X_A^2}{R_A}\right)}. \tag{9}$$

Equation (9) is plotted in Fig. 3 together with the Q-factor and shows the antenna load voltage versus antenna resistance for a given P_{av} and non-zero X_A. Note that the voltage can be maximized by either decreasing or increasing R_A and is at its minimum when $R_A = X_A$. Two different regions thus can be identified, being Region I for $R_A < X_A$ and Region II for $R_A > X_A$.

When assuming $R_A \ll X_A$ in Region I, (9) simplifies to

$$V_L|_{R_A \ll X_A} \approx \sqrt{2P_{av}}\frac{X_A}{\sqrt{R_A}}. \tag{10}$$

In this region, the output voltage is passively boosted by the presence of the antenna reactance, which forms an LC resonator with the load. Significant improvement for large values of Q can be achieved at the expense of bandwidth. This property is exploited in [4], where the input voltage at the RF energy harvester is effectively increased using a high-Q loop antenna $(Z_A = 4.4 + j328\ \Omega)$. The voltage boost improves the rectifier sensitivity, meaning that a wireless sensor node with an RF energy harvester can be operated at a larger distance from the RF energy source.

When assuming $R_A \gg X_A$ in Region II, (9) simplifies to

$$V_L|_{R_A \gg X_A} \approx \sqrt{2P_{av}R_A}. \tag{11}$$

In this region, the antenna impedance can be considered to be purely real. The load voltage is simply determined by the resistive voltage division between the antenna and its load. However, since the equivalent Thévenin antenna voltage itself depends on the antenna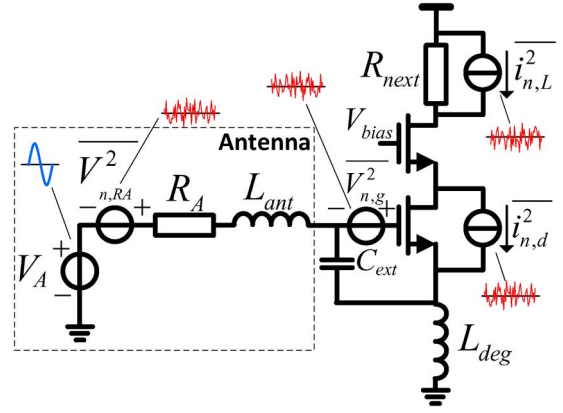 resistance by $V_A = \sqrt{8P_{av}R_A}$ [6], the load volt-age increases, although at a slower rate compared to Region I. On the other hand, Region II has a fundamentally wideband characteristic, which can be exploited in the design of wideband low-noise amplifiers (LNAs), where relatively large antenna resistances of 150 Ω [7] have been reported in the literature.

IV. CODESIGN EXAMPLES

Here, two examples are treated to demonstrate the antenna-electronics codesign for the reception of wireless information (LNA) and wireless power (RF energy harvesting).

A. Low Noise Amplifier

The codesign of any antenna-electronics interface starts by optimizing the antenna load impedance, which in this example is a 900 MHz narrowband LNA. The well-known inductively degenerated CMOS cascode LNA topology [8] is used as it provides an easy way of adjusting the LNA input impedance. The LNA is directly connected to an inductive antenna as depicted in Fig. 4. The information is sensed with a CMOS gate, meaning that voltage is the preferred signal quantity to maximize.

Along with the desired signal V_A, the antenna picks up noise from all points within its directivity radiation pattern and thus depends on how the antenna is directed toward its environment. However, at RFs it is usually assumed that the random noise of an antenna will be as low or lower than the thermal noise corresponding to room temperature [9]. The antenna noise can thus be modeled as $\overline{V_{n,A}^2} = 4kTR_A\Delta f$, where $k = 1.38 \cdot 10^{-23}$ J/K is Boltzmann's constant, $T = 300$ K, and Δf denotes the unit bandwidth. Other relevant sources of noise are the channel noise of the transistor $\overline{i_{n,d}^2} = 4kT\gamma g_m\Delta f$, the gate resistance $\overline{v_{n,g}^2} = 4kT\gamma R_g\Delta f$ and the LNA load noise $\overline{i_{n,L}^2} = 4kT\Delta f/R_{next}$. Here, g_m denotes the transconductance of the MOS transistor, R_g the transistor gate resistance and R_{next} is the loading resistance of the next stage. The coefficient γ is often between 2/3 and 2, depending on the transistor size and the technology.

The performance of the LNA is evaluated using the Noise Factor (F), which is a measure of how much noise is relatively added by the LNA compared to the noise generated by the source. It is worth to emphasize that the noise factor therefore is defined for a specific antenna resistance and thus can be

improved by codesign. A larger antenna resistance for example generates more noise, but also equally scales the desired antenna voltage as $V_A = \sqrt{8 P_{\mathrm{av}} R_A}$. The input signal-to-noise ratio (SNR) therefore does not change. However, the noise of the LNA now appears relatively smaller compared to the antenna noise, resulting in a lower noise factor and therefore better SNR at the output.

For this particular LNA implementation, the interface impedance is defined as $Z_{\mathrm{interface}} = R_A + j\omega(L_{\mathrm{ant}} + L_{\mathrm{deg}}) = R_A + jX_A$ as the total inductance in the interface is the sum of the antenna and the degeneration inductor. As the narrowband LNA operates in Region I, the antenna load voltage is thus approximated by (10) for large values of Q. When assuming the interface to be at the resonance frequency with conjugate matching, the minimum noise factor for low and medium frequencies is approximated as

$$F_{\min} \approx 1 + \delta \frac{R_g}{R_A} + \underbrace{\frac{R_A}{X_A^2}}_{co-design} \underbrace{\left(\frac{\gamma}{g_m} + \frac{4}{g_m^2 R_{\mathrm{next}}} \right)}_{LNA}. \quad (12)$$

Notice that the 'LNA' term in (12) only depends on the LNA circuit parameters and can be minimized by increasing the MOS transistor's bias current and gate area. The 'codesign' term allows to reduce the noise factor without additional power consumption by using a high-Q impedance interface. The input-referred noise of R_g is suppressed by the interface gain due to the presence of the external capacitor C_{ext}. This is indicated by δ, which scales with $1/Q^2$ when $C_{\mathrm{ext}} \gg C_{gs}$.

The LNA is designed in AMS 0.18 μm technology and its design parameters are kept constant during the following circuit simulations ($g_m = 366$ μS, $C_{gs} = 4$ fF, $R_g = 18$ Ω, $R_{\mathrm{next}} = 10$ kΩ, $\gamma = 1.1$). The LNA input impedance is varied by tuning L_{deg} and C_{ext} while the antenna is subsequently conjugate matched to the LNA input for each case. The inductive antenna is modeled as an inductor L_{ant} in series with a power port with resistance R_A. The difference in noise factor is thus only determined by the difference in interface impedance. As a proof of concept, the antenna and matching components are considered lossless.

Fig. 5 shows that the minimum simulated noise factor in dB (i.e., the noise figure, NF) matches well with the theoretical values obtained from (12) for all interface impedances. Note that the $10 + j300$ Ω and $30 + j500$ Ω interface have approximately the same $NF_{\min}$, but the $30 + j500$ Ω interface has a larger NF bandwidth because this interface has an approximately two-times lower Q-factor.

For minimum NF, R_A should be as low and X_A as high as possible. In practice however, this will cause the antenna radiation efficiency to drop considerably when the antenna conduction loss resistance becomes comparable to R_A [6]. In this case, a minimum R_A should be selected during the optimization. The LNA input however, *can* be designed for maximum parallel resistance (i.e., purely capacitive input impedance) and therefore would increase the load voltage by 6 dB when keeping R_A fixed at the minimum value [7]. It is important to point out that a conjugate matched interface in theory would increase the voltage even further, but in this case would require a purely inductive antenna with infinitely small antenna radiation resistance and conduction loss resistance, which of course is not realizable.
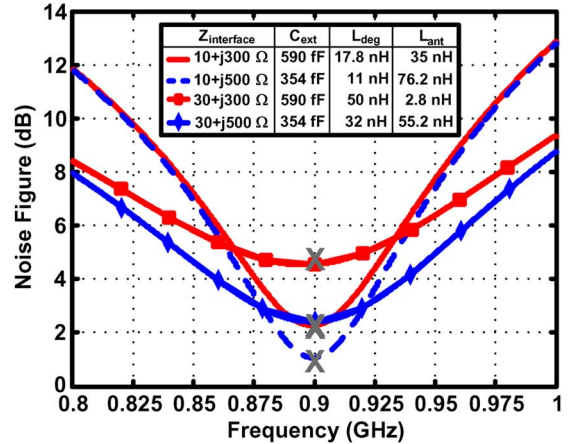

Fig. 5. Simulated noise figure for narrowband LNA for various interface impedances. The calculated $NF_{\min}$ using (12) is marked by 'X'.
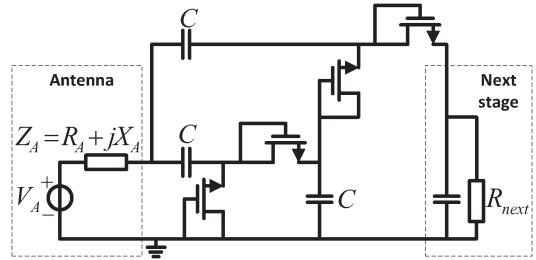

Fig. 6. Two-stage diode-connected NMOS rectifier connected to an inductive antenna.

B. RF Energy Harvesting

The codesign of an antenna and a rectifier is slightly more complex compared to the LNA example in the sense that the rectifier is highly nonlinear. An RF energy harvester therefore is usually optimized for a given input power in a narrow frequency band as the interface is hard to conjugate match over a broad input power range.

Recalling from Section II, it is critical to generate a sufficiently large voltage to overcome the threshold voltage of the transistors while simultaneously achieving maximum power transfer. Although there are many rectifier implementations to choose from that all have their own advantages and disadvantages, it is essential for the codesign to choose a rectifier topology that provides a high parallel input resistance R_P. In this example, a conventional two-stage diode-connected NMOS rectifier is used as depicted in Fig. 6. The effective input resistance R_P of this rectifier implementation depends on the input voltage, but can also be increased by increasing the transistor threshold voltage V_{TH}, as was proven in [10]. A larger V_{TH} increases the voltage boost but also increases the minimum voltage to activate the rectifier, meaning that there is a tradeoff to be made for the value of V_{TH}. This can for example be done by adjusting the body voltage or using different V_{TH} transistors.

Two rectifiers are implemented with identical transistor size (W/L = 1000), coupling capacitors (C = 0.8 pF) and resistive load ($R_{\mathrm{next}} = 300$ kΩ). The only difference is that one rectifier is implemented with standard threshold voltage transistors ($V_{\mathrm{TH,standard}} = 560$ mV) while the other rectifier uses low threshold transistors ($V_{\mathrm{TH,low}} = 440$ mV). The simulated input
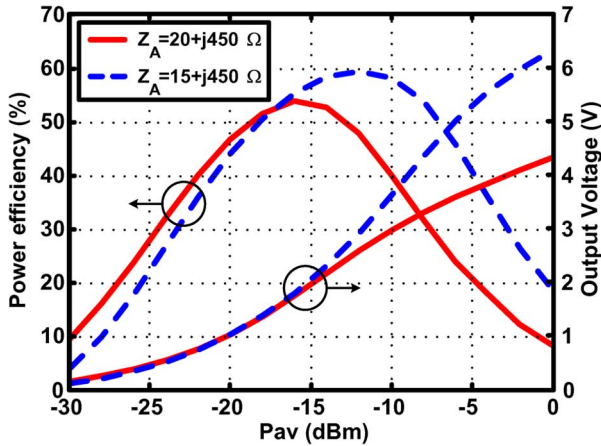
Fig. 7. Simulated power efficiency and DC output voltage versus available power for two different rectifier input impedances with $R_{\text{next}} = 300$ kΩ.

series resistance of the two rectifiers at -15 dBm input power at 900 MHz is 20 Ω and 15 Ω for the $V_{\text{TH,low}}$ and $V_{\text{TH,standard}}$ implementation, respectively. The simulated input series reactance is 450 Ω for both implementations. The antenna is subsequently conjugate matched to the rectifier input impedance for both cases.

The simulated power efficiency ($\eta = P_{\text{out}}/P_{\text{av}}$) and steady state DC output voltage is shown in Fig. 7. For input power levels lower than -20 dBm, both interfaces do not generate sufficient input voltage to overcome the threshold voltage of the transistors. However, since the 20 Ω rectifier implementation uses lower threshold voltage transistors than the 15 Ω implementation, it shows slightly better efficiency at low (< -17 dBm) input levels. For input power levels higher than -17 dBm, the 15 Ω rectifier benefits more from the interface voltage boost and thus has a larger transistor overdrive voltage compared to the 20 Ω interface, resulting in a significant efficiency improvement. When looking at the simulated steady state DC output voltage, it is evident that the 15 Ω interface generates a significantly larger output voltage compared to the 20 Ω interface. This can be used to for example increase the maximum energy storage capability ($E_{\text{store}} = (1/2)C_{\text{store}}V_{\text{out}}^2$) when charging a (super)capacitor for autonomous wireless sensor nodes.

V. CONCLUSION

In this brief, the codesign principles are presented for electrically short antenna-electronics interfaces for antennas in the receiving mode. It was argued that power transfer is not the only design objective in these interfaces, but that the interface needs to be optimized for either voltage or current, depending on which is more favorable to measure with the electronics.

The first condition is to conjugate match the antenna-electronics interface as this maximizes both the voltage and current at the load. The second condition is to determine at which impedance level conjugate matching should occur in order to further increase the load voltage or current. This was demonstrated with a codesign example for the reception of wireless information by means of an antenna and an LNA, and for the reception of wireless power by means of an antenna and a rectifier.

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