A Light-load-Efficient 11/1 Switched-Capacitor DC-DC Converter with 94.7% Efficiency while Delivering 100mW at 3.3V

20.1 A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter with 94.7% Efficiency While Delivering 100mW at 3.3V

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Getting from the mains to a few volts to power electronic circuits requires a very large voltage conversion ratio since the rectified US and EU mains have DC levels of 169V and 325V, respectively. Primary converters, such as flyback converters, use the winding ratio of the isolation transformer to achieve large step-down ratios and generate bus voltages of about 12V. The higher the bus voltage, the higher the efficiency of the primary converter can be and the lower the bus impedance loss. This motivates the investigation of highly efficient DC-DC converters with high voltage conversion ratios (VCRs) to use as secondary converters in AC-DC applications.

Inductive buck converters typically perform high-ratio voltage step-down. Recently, however, their switched-capacitor (SC) counterparts have been evolving in this direction [1,2]. Despite widespread usage of inductive converters for this application, SC converters have a key advantage of 50% duty cycle operation as their VCR is mainly set by the SC topology. In contrast, inductive buck converters depend on very low duty cycles for high step-down ratios. This is an issue as higher switching frequencies are desirable to allow for smaller inductors. SC topologies generally require a larger number of external components than inductive converters, but still compare favorably in terms of area due to efficient component utilization [1,3]. Among SC DC-DC converters, a 3-phase approach [3] requires fewer flying capacitors for a given VCR than regular 2-phase SC converters [4]. This comes at the cost of reduced efficiency due to less optimal component utilization as each phase only lasts 33% of the period, compared 50% in 2-phase operation, leading to larger switches. This paper demonstrates a 2-phase 11/1 SC converter, with the minimum required number of 5 flying capacitors [4], that provides an output voltage, V_o, of 3.3V from an input in the range of 37.4V to 39V. A hysteretic controller ensures stable operation from 0mW up to 140mW under full load step transients and line regulation in the complete input voltage range. For an output power $P_o > 20\%$ of $P_{o,max}$, the system attains an efficiency above 91%, with a peak of 95.5% for a 70mW load from a 37.42V input. In addition of having fewer capacitors than [1], the VCR is higher than [1] and [2]. Next to the 11/1 SC topology, a Multiple-Input Multiple-Output (MIMO) auxiliary rail generator is proposed as a uniform technique to efficiently generate a number of auxiliary supply rails, necessary to reliably generate power switch driving signals.

The targeted combination of high efficiency, high VCR, and high input voltage in a small volume SC converter motivates integration of the power switches, control logic and auxiliary circuits, while keeping the flying capacitors external. This enables larger capacitance with lower parasitics compared to integrated capacitors. Figure 20.1.1 shows the 11/1 SC topology consisting of only 5 flying capacitors and 16 switches. Switch blocking voltages range from $1V_o$ to $6V_o$ and switch source potentials may be different during each phase, making the design of correct and reliable switch drivers complex. However, converter topologies with high regularity and less complex drivers, such as the ladder converter from Fig. 20.1.2, require many more capacitors for the same VCR. The converter IC is implemented in a 0.14µm SOI CMOS technology using 3.3V devices as well as 20V lateral DMOS devices with a 3.3V gate oxide. Because the $q_g R_{on}$ of a cascade of two 3.3V devices is lower than that of a DMOS, S15 consists of two 3.3V devices which achieve the required blocking voltage of $2V_o$. Although S2 and S3 only need to block $2V_o$, they are implemented with a DMOS for reliability, as drain and source terminals experience large potential variations during phase transitions. When the source potential of a switch corresponds to a flying capacitor terminal, it changes with phase and its corresponding driver must also be able to adapt accordingly. For S7-12-14, the required drive swing remains limited to $2V_o$, but S2 requires a 3-state drive signal with a swing of $3V_o$ peak-to-peak, leading to a more complex driver needing multiple auxiliary supply rails.

The capacitor bias voltages V_{Cfly} and charge multipliers q_{ci} are given in Fig. 20.1.1. Even though capacitors C1 and C5, both having higher bias voltages, transfer less charge per cycle than C2-C4, identical 10uF/25V/0603 ceramic capacitors have been chosen for all 5 flying capacitors. Selecting a larger than necessary capacitance, compensates for the capacitance reduction that is typical with ceramic capacitors under DC bias.

Translating control signals from the 0-V_o range into functional power switch drive signals, confirms the need for many auxiliary supply rails: 2-$7V_o$ and $10V_o$, as illustrated in Fig. 20.1.1. A unified approach is preferred over individual auxiliary rail converters, as in [3] and [5], since the required number of auxiliary rails is much higher in this converter. Moreover, stacking control voltage domains in series leads to a substantial charge recycling benefit. Figure 20.1.2 shows the MIMO auxiliary rail generator, generating all integer multiples of V_o. The 11/1 ladder converter, consisting of 2 fragments in opposite phase to reduce noise on the intermediate rails, is fully integrated in an area of 0.77mm^2. This backbone of auxiliary supply rails allows control signals to be transferred to any level with capacitive level shifters, providing a uniform technique to construct drive signals, regardless of complexity.

The hysteretic control, also shown in Fig. 20.1.2, offers excellent load transient response and fast pulse frequency modulation (PFM), as the switching frequency can instantly jump to any value between 0-100kHz, with a 5µs comparator sampling period resolution. Consequently, V_o overshoot does not occur with a load step from high to low, as demonstrated by Fig. 20.1.3. Alternatively, a full load step from low to high without V_o droop is observed. A 200kHz comparator clock signal as well as the fixed 1MHz clock signal for the auxiliary rail generator are both provided externally. To improve light-load efficiency, PFM is also applied in the ladder converter by gating the 1MHz ladder clock with a 4.2µs window, synchronized to the PFM main converter.

Figure 20.1.4 demonstrates the PFM response to line variations while P_o = 100mW. Both a line variation from an example primary AC-DC converter, as well as a 1.6V line step with a dc-level of 38.2V are illustrated. In the AC-DC case, the DC-DC converter operates at 94.3% efficiency.

The excellent efficiency of the converter with large VCR is experimentally verified in Fig. 20.1.5. The 11/1 SC DC-DC is stable at 0mA and delivers up to 140mW to a 3.3V output, with less than 5% noise, from an input within the 37.4V to 39V range. Due to extensive PFM, both in the main converter as well as in the auxiliary rail generator, quiescent current remains below 20uA in all conditions. Consequently, converter efficiency reaches 60% at a light load current of 363µA (1.2mW) and surpasses 80% at 4mW. For the largest part of the load range ($> 20\%$ $P_{o,max}$), efficiencies above 91% are obtained, with a peak of 95.5%. Voltages have been measured without Kelvin contacts.

The presented results are enabled by the proposed 50%-duty-cycle SC topology, which uses only 5 external 0603 ceramic flying capacitors, and by the fully integrated MIMO auxiliary rail generator concept. The hysteretic control allows full load-step transient response without any undershoot or overshoot, with a single 22µF/0603 output buffer. In addition, good line regulation with a realistic input from an example AC-DC conversion stage is shown. Figure 20.1.6 compares this work to state-of-the-art converters with similar V_i, V_o and P_o specifications. This work achieves higher efficiency than existing solutions, over a broader load range (2.8%-100%) and in a smaller and lighter form factor. Figure 20.1.7 shows the chip micrograph measuring 4.53mm^2.

References:

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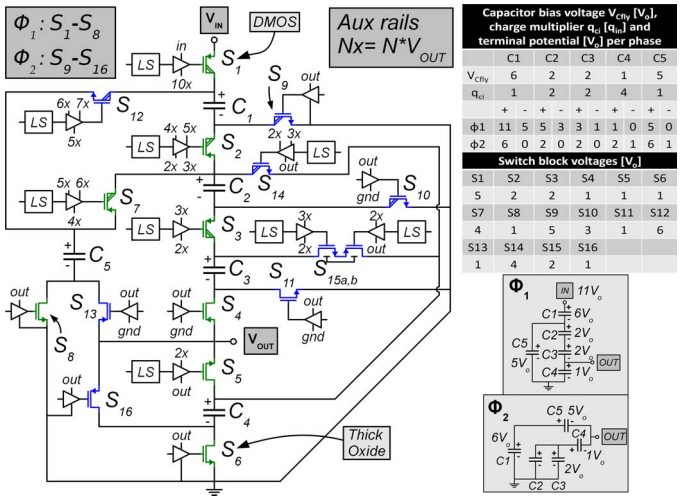


Figure 20.1.1: Transistor-level converter implementation, showing auxiliary supply rails per driver. Specifics on the capacitors and switches are given, as well as a topology illustration per phase.

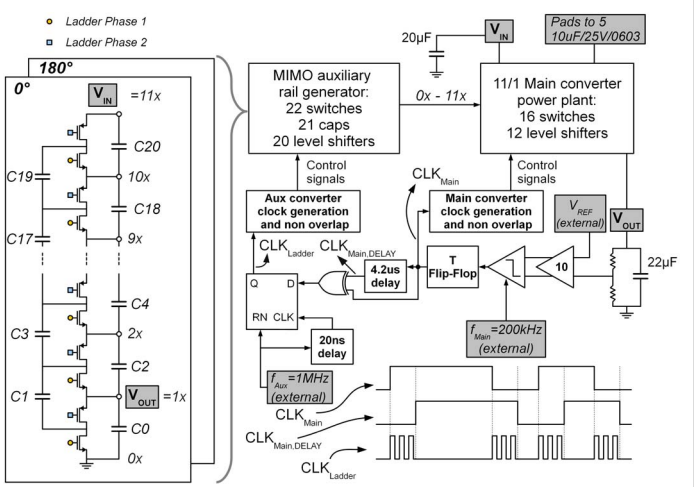


Figure 20.1.2: Block level system view, with details of the MIMO ladder auxiliary-rail-generator topology and its PFM synchronization to the main converter.

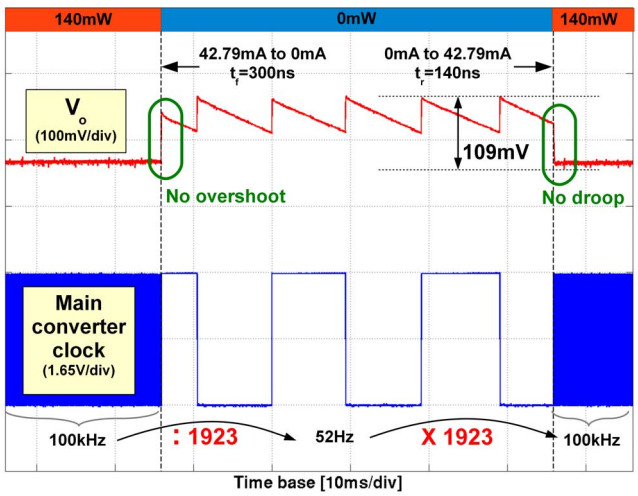


Figure 20.1.3: Load transient response of full load steps, while Vi=37.42V. The switching frequency changes instantly, allowing neither overshoot or undershoot to occur.

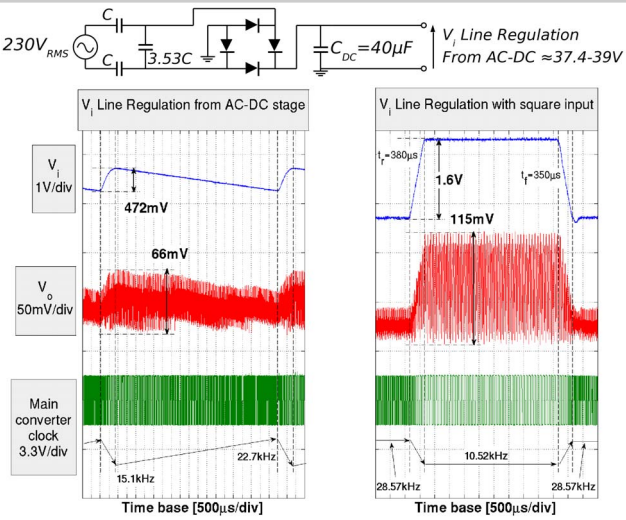


Figure 20.1.4: Line regulation response, while supplied by an example primary AC-DC converter as well as a 1.6V step-wise line variation.

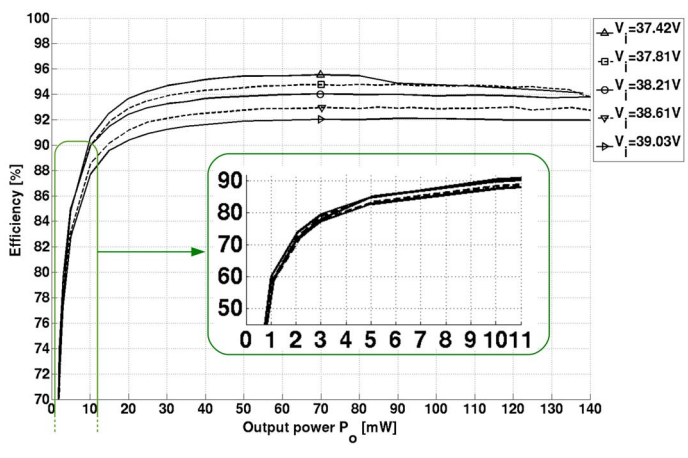
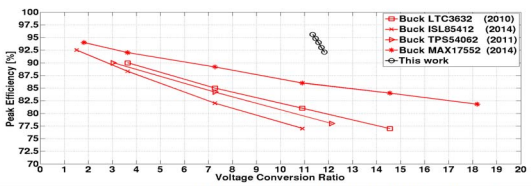


Figure 20.1.5: Efficiency versus load power for multiple input voltages, each corresponding to a theoretical maximum efficiency setting of 97% for Vi=37.42V down to 93% for an input voltage of 39.03V.



Comparison	TPS54062 ('11)	LTC3632 ('10)	ISL85412 ('14)	MAX17552 ('14)	This work
V_i [V]	40	36	36	36	37.42
V_o [V]	3.3	3.3	3.3	3.3	3.3
$I_{o,peak}$ [mA]	46	20	150	100	42.4
C_i [µF]	2.2	4.7	20	1	20
C_o [µF]	22	100	22	10	22
$I_{quiescent}$ [µA]	89	125	50	18.5	20
$Efficiency_{peak}$[%]	78.4	81	77 (PWM)	86 (PWM)	95.5
Power range @ Efficiency >80% [%$P_{o,max}$]	/	35 to 100	/	45 to 100	2.8 to 100
Efficiency at 20% of $P_{o,max}$ [%]	55	78	64/47 (PFM/PWM)	70/77 (PFM/PWM)	91
Energy Transfer	Inductive	Inductive	Inductive	Inductive	Capacitive 5 x 0603
Energy Transfer Component* Area [mm^2]	46.2	36	23	25	5 x 1.28 = 6.4
Energy Transfer Component* Volume [mm^3]	106.4	126	66.8	75	5 x 1.024 = 5.12
Energy Transfer Component* Mass [mg]	4000	480	244	244	5 x 9.1 = 45.5

* Spec sheet recommended

Figure 20.1.6: Performance summary and comparison.

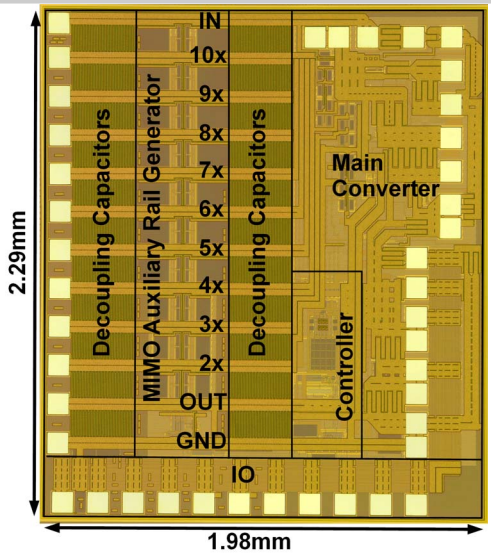


Figure 20.1.7: Chip micrograph with a total area of 4.53mm^2.

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