Analytical drain current model of both p- and n-channel OTFTs for circuit simulation

Fabrizio Torricelli*, Matteo Ghittorelli*, Matteo Rapisarda†, Luigi Mariucci†, Stephanie Jacob‡, Romain Coppard‡, Eugenio Cantatore§, Zsolt Miklos Kovács-Vajna*, and Luigi Colalongo*
*Department of Information Engineering, University of Brescia, 25123 Brescia, Italy. E-mail: fabrizio.torricelli@unibs.it
†CNR-IMM, via del fosso del Cavaliere 100, Roma, Italy
‡CEA-LITEN, 17 rue des martyrs, 38054 Grenoble Cedex 9, France
§Eindhoven University of Technology, Department of Electrical Engineering, Eindhoven, The Netherlands

***Abstract*—Organic thin-film transistors (OTFTs) are an emerging technology for large scale circuit integration, owing the availability of both p- and n- channel devices. For the technology development and the design of circuits and digital systems, the accurate physical modeling is mandatory. In this work we propose an unified analytical model for both p- and n- type OTFTs. The model is physically based and accounts for a double exponential density of states (DOS). It is simple, symmetric and accurately describes the below-threshold, linear, and saturation regimes via a unique formulation. The model is eventually validated with the measurements of complementary OTFTs fabricated in a fully-printed technology.**

I. Introduction

In the last years, organic electronics have seen an impressive performance improvement thanks to new materials [1], fabrication processes [2], and devices [3]. Organic electronics have found application in sensors [4], [5], and circuits [6], [7], [8]: for instance, active matrix organic light emitting displays (AMOLEDs) [9], [10] are already available in the electronic market. State-of-art organic technologies provide both p- and n-type thin-film transistors printed on large-area flexible substrates, like plastic foils, at near to room temperature [11], [12], [13], [14]. Complementary organic thin-film transistors (OTFTs) are the key asset to develop reliable, low-power, fully-organic integrated circuits and systems. To further improve the performances and to integrate high-functionality circuits in the OTFT technologies, accurate and physically-based analytical models are compulsory. The charge transport is the most important physical effect taking place in organic transistors and it is strictly related to the disorder microstructure of the semiconducting layer [15], [16], [17]. The structural and energetic disorder of the organic semiconductor (OSC) are reflected in its density of states (DOS) [18], [19]. According to many experimental observation, the DOS shape can be approximated by an exponential [20], [21], [22], [23] or a double exponential function [24], [25], [26], [27], [28]. In particular, the former has been mainly observed in p-type OTFTs while the latter has been observed in both p-type and n-type OTFTs. Therefore, the proper description of a complementary OTFTs technology requires a double exponential DOS:

$$g(E) = \frac{N_d}{k_B T_d} \exp\left(\frac{E - E_0}{k_B T_d}\right) + \frac{N_t}{k_B T_t} \exp\left(\frac{E - E_0}{k_B T_t}\right) \quad (1)$$

where N_d, N_t and T_d, T_t are the total density and the characteristic temperature of the deep and tail states, respectively. E_0 is a reference energy, and it is the highest/lowest occupied/unoccupied molecular orbital (HOMO/LUMO) in case of the hole and electron DOS, respectively.

In this work an analytical drain-current model for both p-type and n-type OTFTs that accounts or both deep and tail states is proposed. The model is validated with numerical calculations and measurements of high-mobility p- and n-type OTFTs fabricated in a fully-printed technology.

The work is organized as follows. In Section II the transistors fabrication is reported. In Section III the drain-current model is presented. In Section a surface potential analytical model is proposed, and in Section V the drain current model is exploited to describe both p- and n-type OTFTs printed on plastic foil. In section VI conclusions are drawn.

II. Transistors Fabrication

The organic transistors are fabricated on 11cm x 11cm flexible PEN foil using a bottom-contact tog-gate structure for both p- and n-type OTFTs (Fig. 1). At first, 30 nm of gold are deposited by sputtering and then patterned by photolithography forming the source and drain electrodes [29]. Then, a self-assembled monolayer is used to optimize the electron injection in n-type semiconductor. The n-type (Polyera ActiveInk®) and p-type (Merck Lisicon S1200®) OSCs are printed with a thickness of about 100 nm. The gate insulator is fluoropolymer dielectric (Merck Lisicon D139®) screen-printed on top of both semiconductors and then annealed, leaving open areas for via holes, with a final thickness of 750 nm. Finally, a silver-ink conductor is screen-printed on the top of the dielectric and annealed at 100°C, forming in the same step the gate electrodes for devices and the second level for interconnection. Transistors are measured in air at room temperature.

III. Drain-Current OTFT Model

For the sake of simplicity, the drain current model is presented for n-type OTFTs, and same considerations hold for p-type OTFTs. The integral expression of the drift-diffusion current reads [23]:

$$I_{DS} = \frac{W}{L} \int_{V_S}^{V_D} \int_{V_{ch}}^{\varphi_s} \frac{\sigma(\varphi, V_{ch})}{F_x(\varphi, V_{ch})} d\varphi dV_{ch} \quad (2)$$

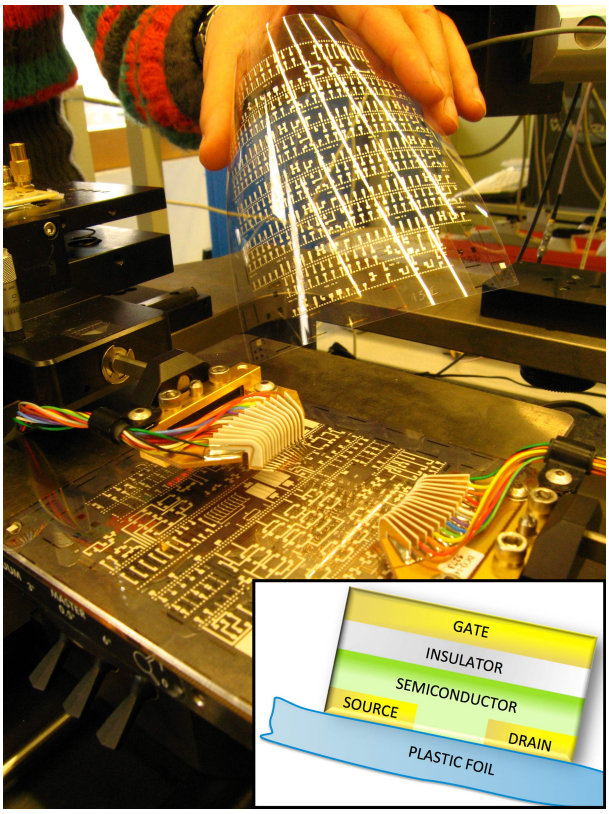

Fig. 1. Main Panel: picture of a 11 cm x 11 cm plastic foil with printed single devices and complementary digital and analog circuits. Inset: cross-section of the OTFT staggered structure.

where W is the channel width, L is the channel length, V_S and V_D are the source and the drain voltages, respectively, V_{ch} is the channel potential (i.e. the pseudo Fermi energy), φ is the electrostatic potential and φ_s is the surface potential at the insulator-semiconductor interface. σ is the Variable Range Hopping conductivity, that in case of a double exponential DOS reads [16]: $\sigma = \omega_0 \exp\left[\Delta E_F/(k_B T)\right]$, where $\omega_0 = \sigma_0[\pi N_t T_t^3/(8\alpha^3 B_c T^3)]^{T_t/T}$ is a function of the organic semiconductor parameters ($B_c = 2.8$, $\alpha^{-1} = 2.2\text{Å}$), $\Delta E_F = q(\varphi - V_{ch}) + \Delta E_{Fi}$, and $\Delta E_{Fi} = E_{gap}/2 - E_0$.

The electric field in the x-direction $F_x(\varphi, V_{ch})$ is calculated with the Poisson equation $\nabla^2\varphi = -(\partial F_x/\partial x + \partial F_y/\partial y)$ and assuming the gradual channel approximation (i.e. $F_x \gg F_y$) results:

$$F_x(\varphi, V_{ch}) = \sqrt{\frac{2q}{\epsilon_s}\int_{V_{ch}}^{\varphi} n(\varphi', V_{ch})d\varphi'} \quad (3)$$

$$\simeq \sqrt{\frac{2q}{\epsilon_s}\left[k_d e^{\frac{q(\varphi - V_{ch})}{k_B T_d}} + k_t e^{\frac{q(\varphi - V_{ch})}{k_B T_t}}\right]} \quad (4)$$

where $\epsilon_s = \epsilon_0 k_s$, ϵ_0 is the vacuum permittivity, k_s is the semiconductor relative permittivity, and $n = \int g(E) f(E; E_F) dE$ is the charge concentration given by the Fermi-Dirac integral solved for the DOS distribution of Eq. 1. k_d and k_t are calculated as $k_o = (N_o \vartheta_o k_B T_o/q)\exp\left[\Delta E_{Fi}/(k_B T_o)\right]$, $o \in \{d, t\}$, and $\vartheta_o = \pi(T/T_o)/\sin(\pi T/T_o)$ because in our case $T_o > T$ [30]. It is worth noting that k_d and k_t depends only on the DOS parameters for a given temperature T.

Since the electric field (Eq. 4) is given by the sum of two exponential functions, Eq. 2 cannot be solved analytically. To this aim, the electric field can be re-written as a single exponential function by means of an effective temperature approach [31], Eq. 4 reduces to $F_x(\varphi, V_{ch}) = F_0 \exp\left[q(\varphi - V_{ch})/(2k_B T_E)\right]$, where $F_0 = \sqrt{2q\left(k_d + k_t\right)/\epsilon_s}$, and the effective temperature results:

$$T_E(\varphi, V_{ch}) = \frac{q(\varphi - V_{ch})}{2k_B \log\left[\frac{F_x(\varphi, V_{ch})}{F_0}\right]} \quad (5)$$

Eq. 5 accounts for both deep and tail states: at small charge carrier concentrations the effective temperature is near T_d, whereas the Fermi level resides at high energy (large carrier concentrations), the effective temperature is closed to T_t.

Replacing Eq. 5 in Eq. 2 and integrating with respect to $d\varphi$, the drain current reads:

$$I_{DS} \simeq \frac{W}{L}\beta_0 \int_{V_S}^{V_D} \exp\left[\frac{q(\varphi_s - V_{ch})}{k_B}\left(\frac{1}{T} - \frac{1}{2T_E}\right)\right] dV_{ch} \quad (6)$$

where

$$\beta_0 = \frac{\omega_0}{F_0}\frac{k_B}{q}\frac{2T_E T}{2T_E - T}\exp\left[\frac{\Delta E_{Fi}}{k_B}\left(\frac{1}{T} - \frac{1}{2T_E}\right)\right]$$

To work out an analytical formulation of the drain current (Eq. 6), an expression of the surface potential φ_s is required. By applying the Gauss' law to the insulator-semiconductor interface, one obtains:

$$F_x(\varphi_s, V_{ch}) = \frac{C_i}{\epsilon_s}(V_{GF} - \varphi_s) \quad (7)$$

where C_i is the gate insulator capacitance per unit area, $V_{GF} = V_G - V_{FB}$, and V_G and V_{FB} are the gate and the flatband voltages, respectively. Replacing Eq. 5 in Eq. 7 the band bending $(\varphi_s - V_{ch})$ is calculated as a function of the gate voltage:

$$\varphi_s - V_{ch} = 2k_B T_E \log\left[\frac{C_i}{\epsilon_s F_0}(V_{GF} - \varphi_s)\right] - \Delta E_{Fi} \quad (8)$$

After substituting Eq. 8 in Eq. 6 and changing the integration variable from dV_{ch} to $d\varphi_s$ [23], the drain current turns out to be:

$$I_{DS} = \frac{W}{L}\left[K_S(V_{GF} - \varphi_{sS})^{\gamma_S} - K_D(V_{GF} - \varphi_{sD})^{\gamma_D}\right] \quad (9)$$

where φ_{sS} and φ_{sD} are the surface potential calculated at the source and the drain contact, respectively, and:

$$K_X = \frac{\omega_0}{F_0}\frac{k_B T}{q(\gamma_x - 1)}\left(\frac{C_i}{\epsilon_s F_0}\right)^{\gamma_x - 1}$$

$$\gamma_X = \frac{2T_E(\varphi_{sX}, V_X)}{T}$$

where $X \in \{S; D\}$. The model Eq. 9 accurately reproduces the transition from deep to tail energy states. The transition regime is implicitly accounted for by the normalized effective temperature (viz. γ_X) that, in turn, is a function of the physical

and geometrical parameters, of the pseudo-Fermi potential V_X, and of the surface potential φ_{sX} at the source and drain. φ_{sX} is calculated by equating Eq. 4 and Eq. 7:

$$\frac{C_i}{\sqrt{2q\epsilon_s}}\left(V_{GF}-\varphi_s\right)=\sqrt{k_d e^{\frac{q(\varphi_s-V_{ch})}{k_B T_d}}+k_t e^{\frac{q(\varphi_s-V_{ch})}{k_B T_t}}} \quad (10)$$

It is worthwhile to note that Eq. 10 can only be solved by numerical iteration.

IV. Surface Potential Analytical Approximation

In this section, we propose an accurate approximation of the surface potential in case of a double exponential DOS. It is based on the extension of the surface potential exact solution given in the case of single exponential DOS case. Indeed, in the latter case, Eq. 10 results $C_i/\sqrt{2q\epsilon_s}\left(V_{GF}-\varphi_s\right)=\sqrt{k_o \exp\left[q(\varphi_s-V_{ch})/(k_B T_o)\right]}$, and the surface potential exact solution reads [32]:

$$\varphi_s = V_{GF}-V_{To}W_0\left[\frac{V_{Ti}}{V_{To}}\exp\left(\frac{V_{GF}-V_{ch}}{V_{To}}\right)\right] \quad (11)$$

where W_0 is the principal branch of the Lambert W_0 Function, $V_{To}=(2k_BT_o)/q$, T_o is the characteristic temperature of the single exponential DOS, $V_{Ti}=Q_i/C_i$, $Q_i=\sqrt{2q\epsilon_s k_o}$ is the charge per unit area at equilibrium, and n_i is the carrier concentration at equilibrium. Unfortunately the Lambert function is not included in CAD simulators and an analytical approximation of Eq. 11 is, in such cases, mandatory.

At this aim, when the transistor is in the linear region, i.e. $V_{GF} > V_{ch}$, the argument of W_0 grows very quickly thanks to its exponential dependence on $V_{GF}-V_{ch}$. A good approximation of W_0 in the linear region is its second order expansion [33] $W_0[x]=\log(x)-\log[\log(x)]$ and the surface potential reads:

$$\varphi_s = V_{ch}+V_{To}\log\left[\frac{V_{To}}{V_{Ti}}\log\left(\frac{V_{Ti}}{V_{To}}\right)+\frac{V_{GF}-V_{ch}}{V_{Ti}}\right] \quad (12)$$

On the other hand, when the transistor is in the subthreshold region, i.e. $V_{GF} < V_{ch}$, the argument of W_0 rapidly goes to zero and the surface potential turns out to be exactly the gate overdrive voltage:

$$\varphi_s = V_{GF} \quad (13)$$

The above two equations are a very accurate approximation in the linear (Eq. 12) and subthreshold (Eq. 13) region, separately. In order to unify the two equations in a single continuous function, one can combine the two behaviors with the following function (Eq. 30 in [34]):

$$\log(1+e^x)\simeq\begin{cases} x & \text{if } x >> 0 \\ e^x & \text{if } x \le 0 \\ 0 & \text{if } x << 0 \end{cases}$$

and hence:

$$\varphi_s = V_{ch}+V_{To}\log\left[\frac{V_{To}}{V_{Ti}}\log\left(1+\frac{V_{Ti}}{V_{To}}e^{\frac{V_{GF}-V_{ch}}{V_{To}}}\right)\right] \quad (14)$$

As shown in Fig. 2, Eq. 14 is a continuous and accurate approximation of the exact numerical solution of Eq. 10 valid in case of a single exponential DOS for all the OTFT operating regions. It is worth noting that when $V_{GF}-V_{ch}>0$ Eq. 14 reduces to Eq. 12, whereas at $V_{GF}-V_{ch}<0$ Eq. 14 reduces to Eq. 13. As shown in the inset of Fig. 2 the maximum error between the solution of Eq. 10 and Eq. 14 is lower than 1.5%.

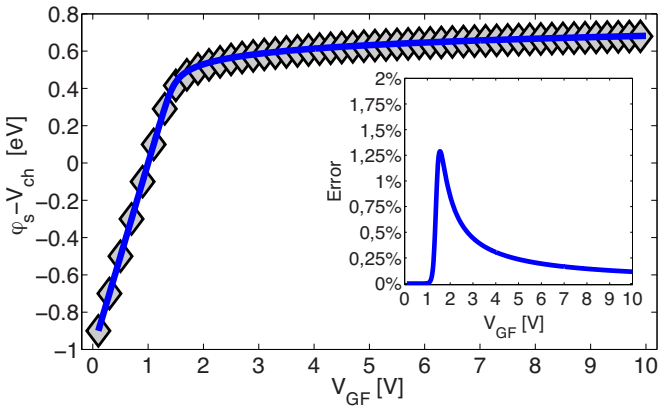

Fig. 2. Main Panel: Surface potential as a function of V_{GF} at $V_{ch}=1$ V calculated by means of the Lambert function (Black Diamond) vs. the proposed approximation Eq. 14 (Blue line). Inset: Percentage error $100\times$ (Eq. 14 - Eq. 11) / Eq. 11. The physical parameters are listed in Table I (P-Type, Tail States).

In order to generalize Eq. 11 to the case of a double exponential DOS, we show in Fig. 3 the surface potential (back diamonds) as a function of the gate voltages. At low gate voltages V_{GF} the surface potential is shaped by the deep states (green dashed line), at large V_{GF} it is defined by the tail states only (red dashed line), while both deep and tail states have to be taken into account in the transition region from the weak accumulation to the strong accumulation.

Basing on the aforementioned analysis, we introduce a modified expression of Eq. 11 defined by three parameters: an effective deep states thermal voltage (V_{Td}), an effective tail states thermal voltage (V_{Tt}) and an effective intrinsic carrier concentration (Q_{ie}):

$$\varphi_s = V_{GF}-V_{Td}W_0\left[\frac{V_{Te}}{V_{Tt}}\exp\left(\frac{V_{GF}-V_{ch}}{V_{Tt}}\right)\right] \quad (15)$$

where $V_{Te}=Q_{ie}/C_i$. The effective parameters V_{Td}, V_{Tt}, Q_{ie}, can be extracted once only on a single transfer characteristic. In Fig. 3 (blue line) the proposed approximation (Eq. 15) is compared with the exact numerical solution of Eq. 10 as a function of the gate voltage V_{GF}. As shown in the inset Fig. 3 of the maximum error is lower than 3%.

Following the same approach discussed above in case of the single exponential DOS, Eq. 15 can be accurately approximated by means of logarithmic and exponential functions only:

$$\begin{aligned}\varphi_s = V_{ch}+\left(V_{GF}-V_{ch}\right)\left(1-\frac{V_{Td}}{V_{Tt}}\right)\\ +V_{Td}\log\left[\frac{V_{Tt}}{V_{Te}}\log\left(1+\frac{V_{Te}}{V_{Tt}}e^{\frac{V_{GF}-V_{ch}}{V_{Tt}}}\right)\right]\end{aligned} \quad (16)$$

Eq. 16 is a continuous analytical equation of the surface potential as a function of the physical and geometrical parameters,

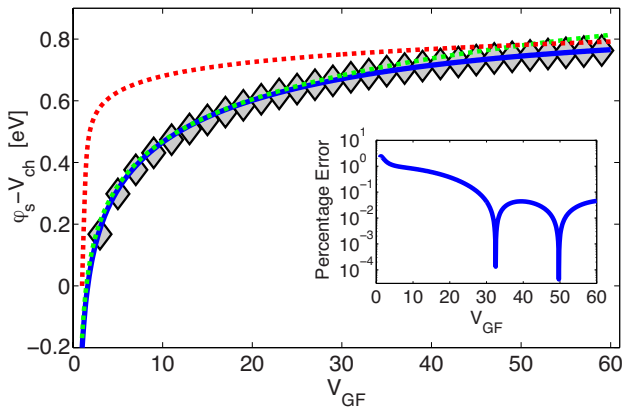

Fig. 3. Main Panel: Surface potential as a function of V_{GF} at $V_{ch} = 1$ V numerically calculated with Eq. 10 (Black Diamond) vs. the proposed approximation Eq. 15 (Blue line). For low gate voltages the surface potential is shaped by the deep states (green dashed line), while for the high gate voltages it is defined by the tail states (red dashed line). Inset: Percentage error. The physical parameters are listed in Table I (P-Type).

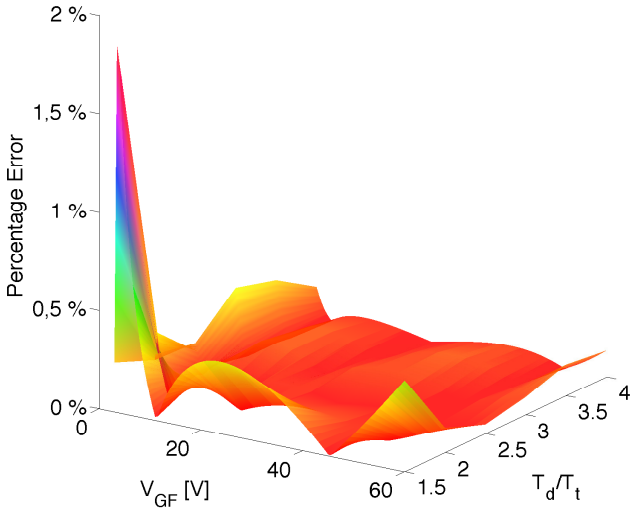

Fig. 4. Main Panel: Percentage error between the numerical solution of the surface potential (Eq. 10) and the double exponential DOS surface potential approximation (Eq. 16) as a function of V_{GF} and T_d/T_t at $V_{ch} = 1$ V. The physical parameters are listed in Table I - (P-Type).

and of the gate and channel potential, in the case of a double exponential DOS. The surface potential parameters (i.e. V_{Td}, V_{Tt}, and V_{Te}) can be calculated by minimizing the difference between the analytical expression Eq. 16 and the numerical solution of Eq. 10. In order to further validate the surface potential model (viz. Eq. 16), we made extensive numerical simulation varying the ratio T_d/T_t, thus explores the whole range of the DOS measured in OTFTs [24], [25], [26], [27], [28]. In Fig. 4 the aforementioned analysis is shown. For the whole range of DOS parameters and gate voltages the error is lower than 2 %. In particular, when the characteristics

TABLE I

GEOMETRICAL AND PHYSICAL PARAMETERS OF THE TRANSISTORS. W IS THE CHANNEL WIDTH, L IS THE CHANNEL LENGHT, k_s IS THE PERMITTIVITY OF THE ORGANIC SEMICONDUCTOR, C_i IS THE GATE-INSULATOR CAPACITANCE PER UNIT AREA, μ_{FE} IS THE LINEAR FIELD-EFFECT MOBILITY, T IS THE TEMPERATURE, σ_0 IS THE CONDUCTIVITY PREFACTOR, N_t IS THE TOTAL NUMBER OF TAIL-STATES, N_d IS THE TOTAL NUMBER OF DEEP-STATES, T_t IS THE TAIL-STATE CHARACTERISTIC TEMPERATURE, T_d IS THE DEEP-STATE CHARACTERISTIC TEMPERATURE, AND V_{FB} IS THE FLATBAND VOLTAGE

	P-TYPE	N-TYPE
W $[\mu m]$	4000	2250
L $[\mu m]$	200	200
k_s	3	3
C_i $[nF/cm^2]$	2.2	2.2
μ_{FE} $[cm^2/Vs]$	1	1
T $[K]$	295	295
σ_0 $[S/cm]$	8.6×10^5	2.2×10^6
N_t $[cm^{-3}]$	1×10^{19}	1.2×10^{19}
N_d $[cm^{-3}]$	3.3×10^{18}	8.7×10^{18}
T_t $[K]$	330	370
T_d $[K]$	940	630
V_{FB} $[V]$	9.3	-10.2

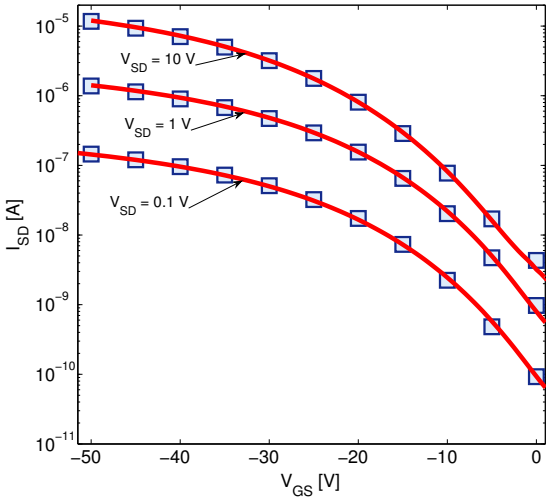

Fig. 5. Transfer characteristics of P-type OTFT at various drain-source voltages. Blue lines with symbols are the measurements and red lines are the model. The geometrical and physical parameters are listed in Table I.

temperature ratio $T_d/T_t > 2$ the percentage error is less then 0.5 % for the whole range of gate voltages, while when $T_d/T_t \leq 2$ the percentage error is of less than 1 % only in the accumulation regime. The first is the typical case of the p-type OTFTs, while the latter is the typical case of the n-type OTFTs.

V. RESULTS AND DISCUSSION

The measured transfer and output characteristics of both p-type and n-type OTFTs are compared with the drain-current model (Eq. 9) in Figs. 5, 6, and 7, respectively. The surface potential is analytically calculated with Eq. 16.

There is good agreement between the measurements and the model in the whole range of biasing conditions. The model

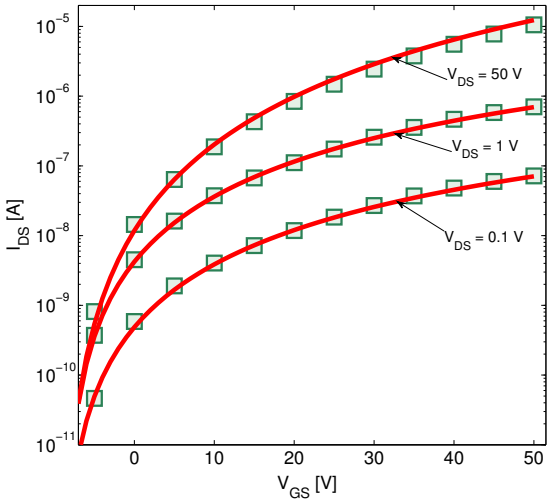

Fig. 6. Transfer characteristics of N-type OTFT at various drain-source voltages. Green lines with symbols are the measurements and red lines are the model. The geometrical and physical parameters are listed in Table I.

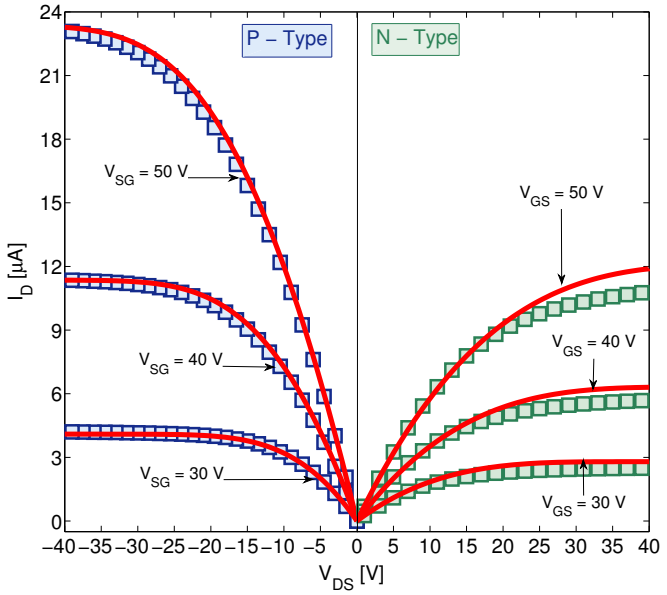

Fig. 7. Output characteristics of P-type (left panel) and N-type (right panel) OTFTs at various gate voltages. Symbols are the measurements and red lines are the model. Geometrical and physical parameters are listed in Table I.

is continuous and accounts for strong accumulation, weak accumulation and sub-threshold regions of operation.

More in detail, in case of p-type OTFTs the model accurately predicts both the transfer and output measurements; while in case of n-type OTFTs the model slightly overestimates the current at large drain voltage. This is evident from the output characteristics shown in Fig. 7 and, according to several studies [35], [36], [37], [38], we verified that it is due to the parasitic contact resistance at the source injecting contact. This is further confirmed by the normalized transfer characteristics shown in Fig. 8. Scaling the transistors channel

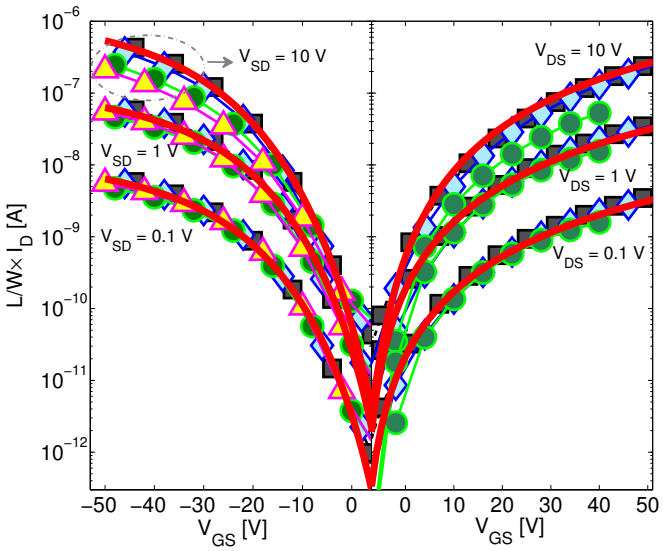

Fig. 8. Left Panel: Measured (black □ $L = 100\mu m$, blue ◊ $L = 50\mu m$, green ◯ $L = 20\mu m$, pink and yellow △ $L = 10\mu m$) and modeled (red lines) L/W normalized transfer characteristics of P-Type transistor. Measured (black □ $L = 100\mu m$, blue ◊ $L = 50\mu m$, green ◯ $L = 20\mu m$) and modeled (red lines) L/W normalized transfer characteristics of N-Type transistor. Geometrical and physical parameters are listed in Table I

length the model overestimates the current only at large drain voltages. The contact resistance is larger in n-type OTFTs and it is commonly related to the energy misalignment between the LUMO and the electrode work function. Indeed, in p-type OTFTs (Fig. 8 left panel) with $L = 100\mu m$ and $L = 50\mu m$ the model perfectly agrees with the measurements whereas at large drain voltages ($V_{SD} = 10V$) and $L \leq 20\mu m$ the contact resistance cannot be neglected. The same considerations hold in case of n-type OTFTs (Fig. 8 right panel) when $V_{DS} \geq 10V$ and $L \leq 50\mu m$. The proposed model does not take into account the contact resistance, which can be easily included following the approaches [35], [39] or with the compact model proposed in [40]. The model parameters, listed in Tab. I, are obtained from a single transfer characteristic measured at the minimum drain voltage ($\|V_{DS}\| = 0.1V$) and from long-channel OTFTs ($L = 100\mu m$). In such conditions the contact resistance is negligible [35], [36], [41] and the model returns the physical parameters of the organic semiconductor.

Comparing the extracted parameters of p- and n-type OTFTs listed in Tab. I, one can see that the transistors show the same field-effect mobility and similar values of flat-band voltage V_{FB}, total density of tail states N_t and tail-states characteristic disorder T_t. On the other hand, the total density of deep states N_d in n-type OTFTs is the double of that in p-type OTFTs. This explains why the maximum drain current is the half (Fig. 7). Such information is useful to further improve the OTFTs performance, providing an optimized technology for complementary logic circuit integration.

VI. Conclusion

In this work an analytical model for both p- and n- type OTFTs is proposed. It provides a unified physical scenario for both holes and electron transport. The model has been validated with respect to both numerical simulations and measurements of OTFTs fabricated on a flexible substrate showing very good agreement. Thanks to its analytical formulation, the model can be easily used for CAD applications, and for the development of high functionality or low power analog and digital circuits.

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