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MIXED SIGNAL LETTER

Classification for synthesis of high spectral purity current-steering mixing-DAC architectures

Elbert Bechthum[1] · Georgi Radulov[1] · Joost Briaire[2] · Govert Geelen[2] · Arthur van Roermund[1]

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Abstract This paper proposes a classification of Mixing-DAC architectures, focusing on spectral purity. Based on literature research, analysis and simulations, the proposed classification shows the impact of architectural choices on the output spectral purity. To concretize the classification and validate the analysis, a number of specific Mixing-DAC architectures are synthesized, discussed and simulated. Given the proposed classification, a set of optimal architectural choices lead to a strong architecture candidate for achieving high spectral purity at high signal frequencies, i.e. SFDR $>$ 80 dBc at $f_{OUT} = 4$ GHz for current and future multicarrier GSM applications. The main characteristics of this architecture are: Cartesian signaling, local Gilbert-cell mixing and a fully differential implementation.

Keywords Mixing-DAC · Digital to analog converter · Mixer · High linearity · Classification

1 Introduction

A popular transmitter architecture is the zero/low-IF transmitter. Thanks to the continuous reduction of CMOS transistor size, integration density increases and errors due to parasitic capacitances and couplings become smaller, which result in a higher linearity. This enables the integration of the mixing and DAC function at high speed and high linearity at low cost. As a single unit, this Mixing-DAC features much more architectural choices, compared to just combining a separate DAC and mixer. Potential advantages of new Mixing-DAC architectures include: lower power consumption, higher linearity and lower noise power [1]. A transmitter signal chain with a Mixing-DAC is shown in Fig. 1.

An overview of the linearity of relevant Mixing-DACs is given in Fig. 2. This figure clearly shows that high-linearity applications, e.g. multicarrier GSM, are not covered by current Mixing-DACs. For the exemplary application of multicarrier GSM, the target Spurious Free Dynamic Range (SFDR) is typically >80 dBc, and the noise power (P_N) is in the order of -160 dBm/Hz. The target output frequency range is between 0.8 and 4 GHz to account for current and future GSM bands. A linearity bandwidth of 300 MHz enables dynamic band selection.

For high linearity applications, a new architecture should be synthesized. However, the design space of Mixing-DACs is highly complex. Numerous interdependent architectural choices exist. Recently an overview of architectural choices for DACs is published [11], which briefly discusses Mixing-DACs. This paper zooms into Mixing-DACs and proposes a Mixing-DAC classification to clarify the impact of high level choices on the spectral purity. Using the classification, a candidate Mixing-DAC architecture is proposed, which is expected to provide sufficient intrinsic performance for multicarrier GSM.

Classifications for various performance figures exist, e.g. power efficiency, output power, output frequency, or signal bandwidth. However, this paper exclusively targets high spectral purity. In this article, a Mixing-DAC is defined as a single integrated design which implements the DAC and mixer functions. The classification focuses are differentiating between the various architectures. Hence, other subjects, e.g. DATA drivers or RF packaging, are not discussed.

✉ Elbert Bechthum
e.bechthum@tue.nl

[1] Department of Electrical Engineering, Eindhoven University of Technology, Eindhoven, The Netherlands

[2] Aquantia, Eindhoven, The Netherlands

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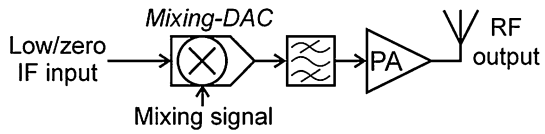

Fig. 1 Transmitter signal chain with Mixing-DAC (I/Q channels not shown)

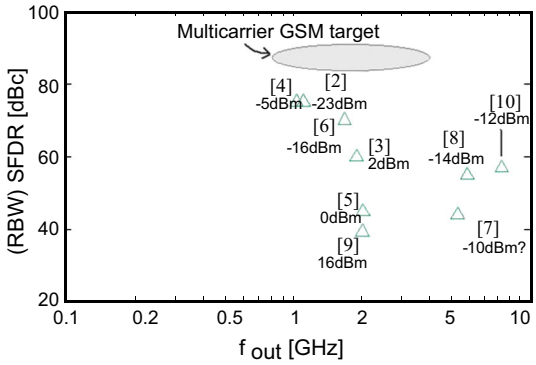

Fig. 2 Overview of the linearity of state-of-the-art Mixing-DAC publications

The limitations in spectral purity of Mixing-DACs are discussed in Sect. 2. A classification of Mixing-DAC architectures is proposed in Sect. 3. Three levels of abstraction are discussed: system level aspects in Sect. 4, signal level aspects in Sect. 5 and implementation level aspects in Sect. 6. Section 7 gives architecture examples and summarizes the proposed architecture for a high spectral-purity. This proposed optimal architecture is shown in Fig. 5(b), the main characteristics are: Cartesian signaling, local gilbert-cell mixing and a fully differential implementation.

2 The mixing-DAC

An example of a Mixing-DAC output spectrum is shown in Fig. 4. The energy in the output spectrum is concentrated at:

$$f_{OUT} = M \cdot F_{LO} + K \cdot F_S + N_1 \cdot f_{IN1} + N_2 \cdot f_{IN2}, \quad (1)$$

where f_{OUT}, F_{LO}, f_{IN1}, f_{IN2} and F_S correspond to the output, LO, and input signal frequencies, and the DATA sample rate; and $N_1, N_2 \in Z$. For high spectral purity, the energy at $M = 1$, $K = 0$, and $N_1 = 1$ or $N_2 = 1$ is desired, the other components should be minimized. The power for different values for M and K depends on a number of variables, such as the shape of the mixing waveform (e.g. sine or square, see Sect. 5.1.1) and the shape of the Mixing-DAC impulse response. The power at $|N_1| > 1$ or $|N_2| > 1$ is due to the non-linear distortion in the Mixing-DAC.

A bandpass filter (dashed line in Fig. 4) can filter out undesired output signals far from the desired output signal frequency. However, Intermodulation Distortion (IMD), which is close to the desired signal, cannot be filtered out and hence is the most critical non-linear distortion.

3 Classification boundary conditions

For high spectral purity at high output frequency, the Current Steering (CS) principle is almost exclusively used, because of its excellent high-frequency and high-linearity characteristics. Therefore, only the class of CS Mixing-DACs is considered. The output noise power is mainly caused by the thermal noise of the current sources, hence it is not differentiating between architectures and is not discussed into detail. Simulations of exemplary circuits are done using an implementation in 1.2 V/3.3 V 65 nm CMOS. In simulations, the Mixing-DAC circuits which are shown in the figures (Figs. 5, 7) are modeled at transistor level. To focus on the differences between various output-stage architectures, the common signals (e.g. the LO and DATA signal, and the biasing signals) are assumed to be ideal, with a transition time of 50 ps.

An overview of the proposed classification is shown in Fig. 3. The three levels of abstraction in the classification are discussed separately in the next three sections.

4 System level classification

Two system level classes are: data representation and Smart methods.

4.1 Data representation

Most traditional transmitters use the Cartesian data representation and processing, i.e. I/Q signaling. Another option for the signal representation is polar signaling [12]. In polar signaling, a signal is defined by its phase and amplitude(i.e. envelope).

An advantage of polar Mixing-DACs is the high efficiency at low output signal power. A disadvantage is that it is only suitable for narrowband signals, e.g. single carrier GSM [13], since the required bandwidth of the envelope and phase signals is much larger than the bandwidth of the original I/Q signal to satisfy EVM [13] and harmonic distortion requirements [14]. Hence, for the same signal bandwidth, Cartesian Mixing-DACs have a higher linearity than Polar Mixing-DACs. A disadvantage of I/Q Mixing-DACs is that the I and Q paths need to be matched in order to achieve good image rejection. This problem has been extensively investigated for traditional I/Q transmitters,

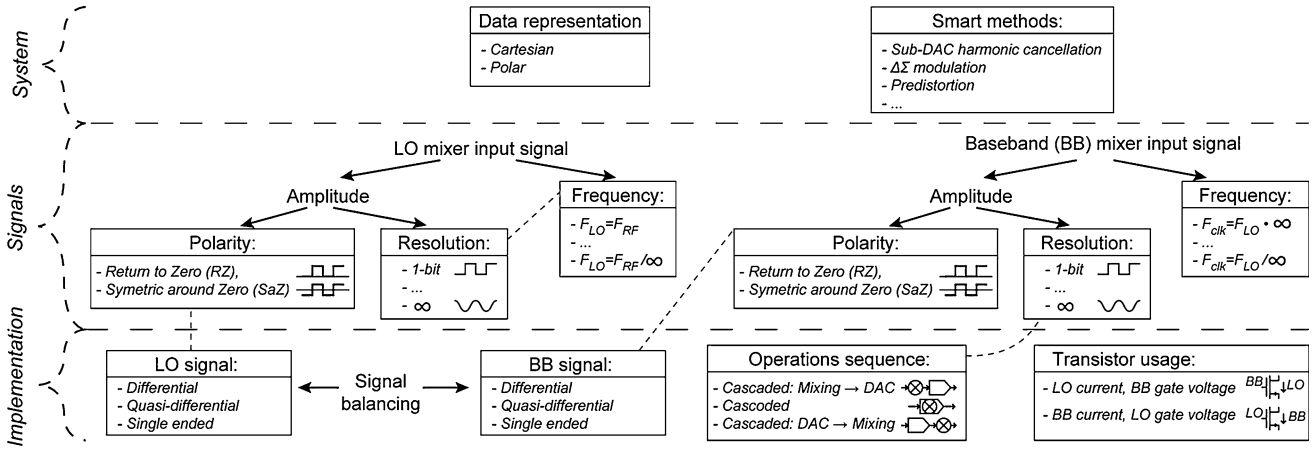

Fig. 3 Overview of the proposed classification of Mixing-DA C architectures

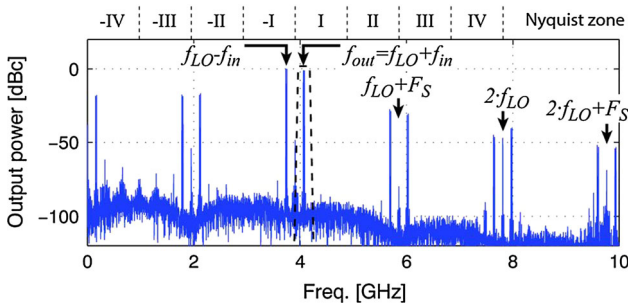

Fig. 4 Exemplary Mixing-DAC output spectrum, transistor level simulated, $F_S = 2$ GSps, $F_{LO} = 4$ GHz

and is usually solved using digital predistortion [15]. Alternatively, a sharp output filter can be used to select one of the two output images, which is shown as a dashed line in Fig. 4. Interesting I/Q combining techniques exist for Mixing-DACs [16].

I/Q signaling is more suitable for the transmission of multicarrier GSM, since the multicarrier GSM signal has a large bandwidth and requires a transmitter with high linearity.

4.2 Smart methods

Smart methods can be used to improve the intrinsic performance of a Mixing-DAC architecture. Examples of smart methods are: amplitude calibration [17–19], timing error calibration [20, 21], Sub-DAC harmonic cancellation [22], ΣΔmodulation [2] or predistortion. Although these smart methods can improve specific non-idealities, the correction mechanisms can introduce or deteriorate other non-idealities, e.g. noise or power consumption.

Since smart methods can be applied with almost equal effect on every architecture, they are not differentiating between architectures and hence they are not discussed into detail.

5 Signal level classification

Two signals are considered in the signal level of the classification: the high frequency LO mixer input signal and the low frequency baseband (BB) mixer input signal.

5.1 LO mixer input signal

The characteristics of the LO mixing signal can be divided in two subsets: amplitude and frequency characteristics.

5.1.1 Amplitude–resolution

The amplitude behavior of the LO mixer input determines the repetition of the BB input spectrum in the RF output spectrum, i.e. $M > 1$ in (1). When the resolution is 1-bit, the LO mixer input is a square-wave. A square wave with 50 % duty cycle results in repetition of the BB input spectrum on each odd multiple of the fundamental LO frequency [9], i.e. $M \in \{1, 3, 5,\ldots\}$. When the resolution of the LO input is infinite, the mixing signal can be a sine-wave, ideally resulting in just one repetition of the BB input spectrum in the RF output spectrum [7], i.e. $M \in \{1\}$.

In the target frequency range, an NMOS transistor is a fast and accurate current switch, but not a linear amplifier. Hence, square-wave mixing is a very attractive way of mixing when implemented in CMOS. The repetitions of the BB signal at higher frequencies can be easily filtered out, which is illustrated by the dashed filter characteristic in Fig. 4.

5.1.2 Amplitude–polarity

Timing errors in the BB signal cause non-linearity. Return to zero (RZ) signaling can be used to mask these timing errors, by switching the BB signal during the 'Zero' phase of the LO signal [2]. The effect of data timing errors can also be alleviated by other techniques [20]. Downside of

RZ mixing is that half of the signal power is lost. Moreover, RZ mixing usually results in a large common mode signal at the output, which makes interfacing with other RF components troublesome. RZ mixing is inherent to single-ended mixing [2, 5, 23], see Sect. 6.1.

Mixing with a Symmetric around Zero (SaZ) shaped LO mixing signal [9] uses the full output power of the Mixing-DAC, which results in a higher output power compared to RZ mixing and can result in a true differential output signal.

In the case that BB timing errors are alleviated by other techniques, the polarity of the mixing signal has no major impact on the spectral purity of the Mixing-DAC and SaZ signaling can be used. Otherwise, RZ signaling should be used to mask the BB timing errors.

5.1.3 Frequency

Usually, the first Nyquist band (with respect to the LO frequency) is used as the primary output signal, i.e. M = 1 in (1) and Nyquist band I in Fig. 4. Also higher Nyquist bands can be used as the primary output signal, i.e. M > 1 in (1). Using M > 1 does not result in better linearity while the signal power and Signal to Noise Ratio (SNR) is worse [10, 24]. Therefore, for high spectral purity, the output signal in the first Nyquist band should be used as the primary output of the Mixing-DAC.

5.2 BB mixer input signal

The characteristics of the BB mixer input can be divided in two subsets: amplitude and frequency characteristics.

5.2.1 Amplitude–resolution

The trade-off between high and low amplitude resolution of the BB mixer input signal is discussed in [25]. When the mixing operation is applied to the combined DAC output ('global mixing'), the BB mixer input resolution is almost infinite. When the mixing operation is applied inside DAC 1-bit unit cells ('local mixing'), the BB mixer input resolution is 1 bit. Examples of global- and local mixing are shown in Fig. 5(a, b) respectively.

For global mixing, a very linear mixer is required since the current through the mixer in Fig. 5(a) is data dependent. However, a current commuting NMOS transistor is not linear [25]. For local mixing, the (small) mismatch of the LO signal and the mismatch of the mix transistors (M_4–M_7 in Fig. 5(a)) cause timing errors which can significantly degrade the linearity. Due to the specific characteristics of the timing errors in the proposed implementation of local mixing of Fig. 5(b), the performance of that implementation is not limited by timing errors [25, 26]. When comparing the two architectures in Fig. 5, simulations of a limited model show that the expected linearity of local mixing is much better than global mixing, i.e. IMD3 = −88 dBc versus IMD3 = −75 dBc. Therefore, local mixing is the best option for high spectral purity.

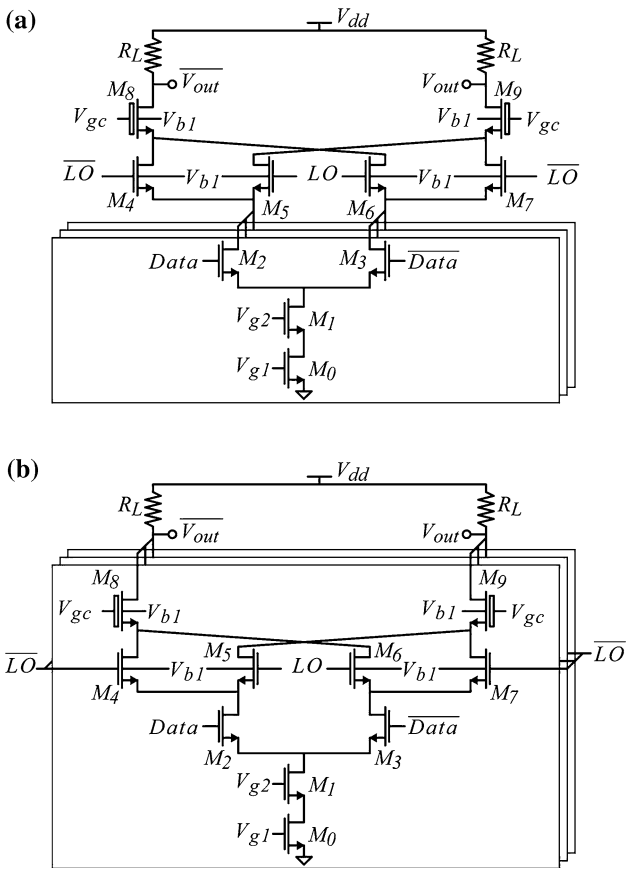

Fig. 5 Synthesized and proposed current steering Mixing-DAC with simultaneous mixing: global mixing (**a**) and local mixing (**b**)

5.2.2 Amplitude–polarity

As discussed in Sect. 5.1.2, there is an advandvantage in using RZ signaling for the LO signal [10]. For the BB signal however, there is no advantage in using RZ signaling instead of SaZ signaling. RZ is only used when the architecture does not allow SaZ signaling because the chosen architecture is completely single ended [23].

5.2.3 Frequency

The sample rate of the BB mixer input influences the spectral content related to the term $K \cdot F_S$ in (1), which can be filtered. However, the ratio between the sample rate of the BB signal and the LO carrier signal should be an integer value to align the LO and BB transitions.

It is known that the distortion level of a DAC depends on the sample rate [27]. However, the choice of sample rate

is usually dictated by the requirements of the application, e.g. quantization noise or width of the Nyquist band.

6 Implementation level classification

At the implementation level, four different aspects are distinguished: Balancing of the signals, sequence of the DAC and mix operation, locality of mixing, and the usage of the mixing transistor.

6.1 Signal balancing

Fully differential signaling minimizes the sensitivity to undesired disturbances, as opposed to single ended signaling. Fully differential signaling also enables the unit cell current source of the CS Mixing-DAC to be always on and thus providing a stable reference. Single ended structures switch the reference on and off, which requires a small-sized reference source and hence a sub-optimal matching between current sources. Single ended structures have the advantage of lower power consumption at low signal amplitudes. Quasi-differential signaling [16] combine some of the distortion immunity of differential signaling with the high power efficiency of single ended Mixing-DACs.

For high spectral purity, disturbance insensitivity is very important. Hence, fully differential signaling is the most optimal choice for high spectral purity.

6.2 Sequence of operations

The sequence of the two operations in the Mixing-DAC (i.e. mixing and digital to analog conversion) can be chosen freely. The two operations can be done cascaded (mixing before the D/A conversion, or mixing after the D/A conversion), or cascoded (i.e. in the same current path).

The choice for the sequence of D/A conversion and mixing operation, and the choice for BB mixer input resolution (i.e. mixing locality, see Sect. 5.2.1) are interdependent. Figure 6 graphically shows this interdependence. For example: global mixing is not available when the mixing operation is done before the D/A conversion.

Therefore, the linearity of analog mixers is limited and 'D/A->mixing' sequence results in a non-linear conversion [1]. In 'mixing->D/A', mixing is done on 1-bit signals, hence a high linearity can be achieved. However, this requires a DAC core which is capable of producing at least 8 GSps for a 4 GHz RF output, which is a very high speed for the required linearity. Known problems with high linearity DACs at high frequency are the data-dependent output impedance [28], timing errors due to mismatch [27] and inter-symbol-interference.

A circuit which uses mixing before the D/A operation is proposed in Fig. 7. The potentially large mismatch in the

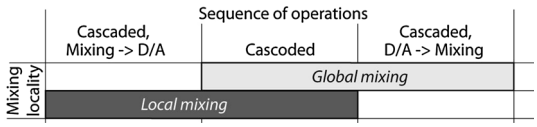

Fig. 6 Interdependent choices for mixing locality and operations sequence

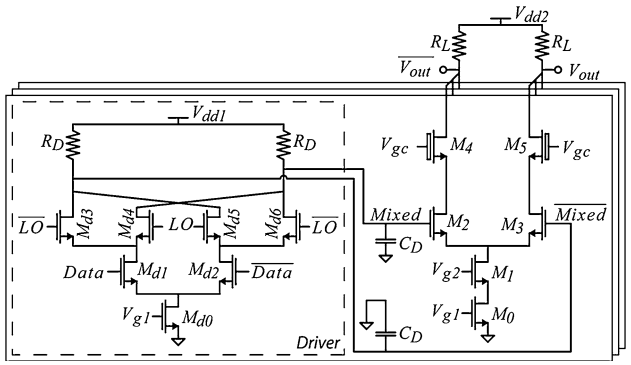

Fig. 7 Synthesized and proposed digital mixing in the driver with fully differential, current steering DAC structure

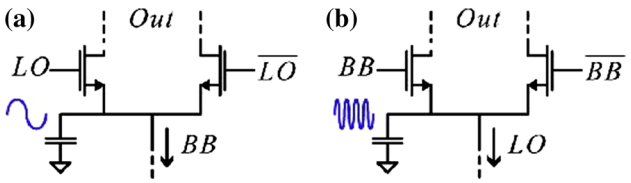

Fig. 8 Difference between options of transistor usage: BB current through transistor (**a**) and LO current through transistor (**b**)

RC time constant of the *Mixed* nodes causes random timing errors, which results in nonlinear distortion. Simple schematic level simulations have shown that the 90 % yield IMD3 value is linearly dependent on the spread in R_DC_D time-constant. A mismatch of 3 % in R_DC_D results in a 90 % yield IMD3 value of −68 dBc, which is much worse than the target −80 dBc. Hence, mismatch in the local driver causes enough timing errors to severely limit the spectral purity, making the 'mixing before D/A' sequence unsuitable for high spectral purity applications.

The previous sections showed that the 'mixing after D/A conversion' and 'D/A conversion after mixing' results in high non-linear distortion. Therefore, it can be concluded that cascoded operations is the most promising choice for high spectral purity.

6.3 Transistor usage

When using a current commutating transistor as a mixer, two different usage scenarios are available with respect to the LO and BB signals, see Fig. 8.

Table 1 Classification of example architectures

Example	System	Signals	Implementation
Proposed [29]	Cart. sign., calibration	Square-w. SaZ mixing, 1st Nyq. band, local mixing, SaZ BB sign.	Fully diff., cascoded operations, LO gate
[5]	Cartesian sign., ΔΣ-modulator, FIR-DAC	SaZ mixing, 1st Nyq. band, global mixing, SaZ BB sign.	
[6]	Cartesian sign.	RZ mixing, 1st Nyq. band, local mixing, SaZ BB sign.	
[10]	Cartesian sign.	Square-w. RZ mixing, 1st–3rd Nyq. band, local mixing, SaZ BB sign.	
[9]	Cartesian sign., ΔΣ-modulator	SaZ mixing, 1st Nyq. band, local mixing, SaZ BB sign.	Fully diff., cascoded operations, BB gate
[3]	Cartesian sign.		
[7, 8]	Cartesian sign ΔΣ-modulator	Square-w. SaZ mixing, 1st Nyq. band, local mixing, SaZ BB sign.	
[2]	Cartesian sign., ΔΣ-modulation	Sine-w. RZ mixing, 1st Nyq. band, local mixing, SaZ BB sign.	Partially single-ended, cascoded, operations, BB gate
[4]	Cartesian sign., ΔΣ-modulator, FIR-DAC		

The main difference between the various operation sequences is the presence/absence of an analog voltage-to-current (V–I) and a current-to-voltage (I–V) conversion. A V–I conversion using a MOST is a very non-linear operation. Only 1-bit signals remain undistorted by definition when passing a non-linear operation while analog signals are distorted.

One option is to supply the gate of the mix transistor with the LO signal and put the BB signal in the current through the mixer, see Fig. 8(a). An example of this mixing configuration is proposed in Fig. 5(b). The other option is to supply the gate of the mix transistor with the BB signal and put the LO signal in the current through the mixer, see Fig. 8(b), imagine Fig. 5(b), but with swapped DATA and LO signals.

Simulations have shown no linearity difference between the two options, but do show an output power difference of 1.5 dB to the disadvantage of the BB-gate option of Fig. 8(b). This figure illustrates the cause of this output power difference, which is the additional parasitic capacitance which experiences the RF frequency. Therefore, the LO gate option can be chosen although there is no advantage in terms of spectral purity.

7 Classification overview

An overview of various Mixing-DAC architectures and their characterization is shown in Table 1. Based on the proposed classification of Mixing-DAC architectures in this paper, a strong candidate Mixing-DAC architecture for high spectral purity is synthesized, which is shown as the proposed architecture in Table 1 and in Fig. 5(b). Implementation and measurements of this architecture are discussed in [29]. Those measurements show that the proposed architecture can indeed achieve a high spectral purity.

8 Conclusion

The proposed systematic analysis and classification of Mixing-DAC architectures reveals the most crucial architectural choices, when high frequency high spectral purity is considered. The sequence of mixing and D/A operation and the resolution of mixing signals are important architectural choices that strongly determine the linearity of a Mixing-DAC architecture.

The future multicarrier GSM application is used as an example to show the effectiveness of the classification. For the required performance, i.e. 80 dBc SFDR and $P_n = -160$ dBm/Hz at 4 GHz, an optimal architecture is synthesized in a 65 nm CMOS technology. The most important characteristics of the synthesized architecture are: current steering, Cartesian signaling, fully differential, local 1-bit mixing.

With the presented analysis of Mixing-DAC architectures, designers and researches now have a clear insight on the impact of architectural choices on the spectral purity of the Mixing-DAC output signal.

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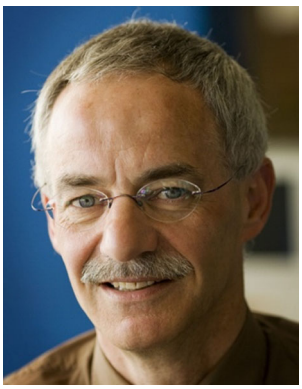
Elbert Bechthum was born in Kapelle, The Netherlands in 1984. He received his B.Sc. and M.Sc. degrees in Electrical Engineering from the Eindhoven University of Technology, The Netherlands in 2006 and 2008 respectively. He worked for one and a half year at SystematIC Design in Delft, The Netherlands before returning to the Eindhoven University of Technology. There he is currently pursuing his Ph.D. degree in the Mixed signal Microelectronics group of the Electrical Engineering faculty on the subject of high performance Mixing-DACs. His research interests include high performance data converters. He is the author of five publications in the scope of his Ph.D. research.

Georgi Radulov was born in Plovdiv, Bulgaria in 1978. He received the M.Sc. engineer (инж.) degree in Electrical Engineering in 2001 from the Technical University of Sofia (TU-Sofia), Bulgaria. In 2004, he received the degree Professional Doctorate in Engineering (PDEng) from Stan Ackermans Institute at Eindhoven University of Technology (TU/e). Georgi Radulov received his Ph.D. degree from TU/e in 2010. Since 2009, he is a part-time Assistant Professor at the Electrical Engineering faculty of TU/e and a part-time director of the micro-electronics consultancy company Welikan B.V. From 2012, he is a full-time assistant-professor at TU/e. In 2008, he was awarded the Outstanding Student Paper of the IEEE conference APCCAS 2008, in Macau. He has co-authored more than 20 publications on DACs, three US patents and one book.

Joost Briaire received the M.Sc. and Ph.D. degrees from Eindhoven University of Technology, The Netherlands in 1996 and 2000, respectively. He joined Philips Research in 2000 and in 2006 he moved to NXP. In 2012 IDT became the employer and since 2015 he is part of Aquantia as a senior principal engineer. The architecture and design of high performance digital-to-analog converters from concept to productionfor both wired and wireless communication applications have been his domain of

expertise, resulting in various papers and patents of which he is either the author or a coauthor.

Govert Geelen was born in Heythuysen, The Netherlands, on November 20, 1957. He received the M.S. degree in Electrical Engineering from the University of Eindhoven, Eindhoven, The Netherlands, in 1983. In 1984 he joined Philips Research Laboratories, Eindhoven, where he was engaged in the design of basic analog building blocks especially opamps and SC-circuits. In 1992 he joined Philips Semiconductors, Eindhoven, where he was involved in the design of PLL and various types of high speed low power CMOS A/D converters. In 2012 he joined IDT, Eindhoven, where he is currently involved in designing high speed D/A converters for mobile communications. Mr. Geelen was a co-recipient of the Lewis Winner Award for outstanding conference Paper of ISSCC 1990 and 1992.



Arthur van Roermund was born in Delft, The Netherlands in 1951. He received the M.Sc. degree in EE in 1975 from Delft University of Technology and the Ph.D. degree in Applied Sciences from K.U. Leuven, Belgium, in 1987. From 1975 to 1992 he was with Philips Research Laboratories in Eindhoven. From 1992 to 1999 he has been a full professor at the EE department of Delft University of Technology, chairman of the Electronics Research Group, member of the management team of DIMES, and chairman of a post-graduate school. From 1992 to 1997 he was also consultant to Philips. October 1999 he joined Eindhoven University of Technology as chairman of the Mixed-signal Microelectronics group. He was director of research of the EE Department (2002–2012), member of the supervisory board of NRC Photonics research centre (2009–2012), chairman of the board of ProRISC, the microelectronics platform in the Netherlands (1999–2012), vice chair of the ICT-research platform for the Netherlands (IPN, 2000–2012), and co-organiser of the yearly workshop on Advanced Analog Circuit Design (AACD, 2001–2012). In 2004 he achieved the 'Simon Stevin Meester' award and 500.000€, for his scientific and technological achievements. In 2007 he was member of an international assessment panel for the Department of Electronics and Information of Politecnico di Milano, Italy; in 2009 for Electronics and Electrical Engineering for the merged Aalto University Finland; and in 2012 for KTH, Stockholm, Sweden. He authored/co-authored about 500 articles and 25 books and is co-editor of another ten books.