High-speed and high-resolution analog-to-digital and digital-to-analog converters

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Lecturer : Prof.Dr Ir R.J. van de PLASSCHE

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Rudy J. van de Plassche.
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The cover illustration shows the subjects of this thesis: Analog-to-digital and digital-to-analog converters.

Contents

List of Figures

List of Symbols

Symbol	Description	Unit
A	Amplitude	1
ΔA	Amplitude deviation	1
A/D	Analog-to-Digital	
$A_{foldback}$	Ratio between amplifier bandwidth and system bandwidth	1
A_j	Amplitude level: index j	1
A_{rms}	Root Mean Square amplitude value	1
$A_{stopband}$	Stopband attenuation	dB
ATE	Automatic Test Equipment	
A_{pp}	Peak-to-peak amplitude	1
A_n	Operational Amplifier: index n	1
$A_{openloop}$	Open-loop amplification	1
B	Full Scale Value	1
B_0	Most Significant Bit Value	1
B_m	m^{th} Bit Value	1
B_{n-1}	Least Significant Bit Value	1
C	Constant	1
C_{bc}	Base-Collector capacitance	F
C_{be}	Base-Emitter capacitance	F
C_{bex}	Extra Base-Emitter capacitance	F
C_d	Diode capacitance	F
C_H	Hold capacitor	F
C_{in}	Input capacitance	F
CML	Current Mode Logic	
$CMOS$	Complementary Metal Oxide Semiconductor	

C_n	Capacitor: index n	F
D/A	Digital-to-Analog	
DC	Direct Current	A
D_n	Diode: index n	
DNL	Differential Non-Linearity	
D_{out}	Digital output data	1
$E(.)$	Statistical expectation	1
ECL	Emitter Coupled Logic	
ERB	Effective Resolution Bandwidth	Hz
E_{glitch}	Glitch error	Vs
E_{LSB}	LSB energy	Vs
E_{noise}	Quantization noise voltage	V
E_{total}	Total noise voltage	V
E_{qns}	Quantization noise voltage	V
$E^2_{qns}(f)$	Quantization noise density	V^2/Hz
f	Frequency	Hz
f_b	-3 dB bandwidth	Hz
f_c	Clock frequency	Hz
f_{comp}	Comparator -3 dB bandwidth	Hz
f_{in}	Input signal frequency	Hz
f_s	Sample frequency	Hz
f_{sig}	Signal bandwidth	Hz
G_A	Amplifier gain	1
g_m	Mutual transconductance	A/V
$H(\omega)$	System transfer function	
$HS3$	High-speed bipolar oxide isolated process	
f_1	Unity gain bandwidth	Hz
I	Current	A
ΔI	Current deviation	A
i	As index	1
IC	Integrated Circuit	
I_{comp}	Compensation current	A
$IEEE$	Institute of Electrical and Electronic Engineers	
INL	Integral Non-Linearity	
I_0	Base-Emitter reverse current	A

I^2S	Inter IC Signal Standard	
I_T	Temperature-dependent current	A/degree C
I_{in}	Input current	A
$J-FET$	Junction Field Effect Transistor	
k	Boltzmann's constant	1.38×10^{-23} J/K
LSB	Least Significant Bit	
m	As index	1
Δ_m	Error of m^{th} bit	
MSB	Most Significant Bit	
N	As variable: Sample rate reduction ratio	1
N_{fold}	Number of folds	1
n	As index: number of bits	1
	As exponent in temp. relation $\approx 1.4-1.8$	
Δn	Error of n^{th} bit	
p	Ratio between emitter areas	1
ppm	Parts per million	10^{-6}
p_{total}	Total noise power	W
q	Electron charge	1.6×10^{-19} C
q_e	Quantization error	1
q_s	Quantization level	1
q_{qns}	Quantization noise power	W
Q_n	Transistor index: n	
RC	First-order time constant	s
R_L	Load resistor	Ohm
R_n	Resistor index: n	Ohm
ROM	Read Only Memory	
R_{ref}	Reference source value	
S/N	Signal-to-noise ratio	dB
$S/N(f)$	Signal-to-noise density ratio	$dB/\sqrt{Hz}$
S/N_{system}	Signal-to-noise ratio of a system	dB
$S/N_{quantizer}$	Signal-to-noise ratio of quantizer	dB
S_n	Switch index: n	
S_t	Step size	1
S_{tout}	Output step size	1
ΔS_{tout}	Output step size deviation	1

T	Absolute temperature	K
ΔT	Absolute temperature variation	K
T_0	Reference temperature	K
T_n	Transistor index: n	
TTL	Transistor Transistor Logic	
t	Time	s
Δt	Time deviation	s
t_{max}	Maximum time deviation	s
t_d	Delay time	s
δt_{td}	Delay time difference	s
t_{dif}	Time difference	s
t_h	Hold time	s
$U(t)$	Unity step function	1
V	Potential	V
ΔV	Potential deviation	V
V_a	Analog voltage	V
V_{be}	Base-emitter voltage	V
V_D	Diode voltage	V
$V_{difference}$	Difference voltage	V
V_{fs}	Full-scale voltage value	V
V_g	Bandgap voltage of silicon	1.208 V
V_{in}	Input voltage	V
V_{lr}	Linear voltage range	V
V_n	Voltage at node index: n	V
V_{out}	Output voltage	V
V_{ref}	Accurate reference voltage	V
V_{rn}	Reference voltage at node index: n	V
β	Transistor current gain	1
ϵ	Amplitude deviation	1
ϵ_m	Error index: m	1
Δ	Matching deviation	1
π	Angular constant	3.14159
$\sigma(P)$	Standard deviation of P	1
τ_d	Delay time	s

ω	Angular frequency	rad/s

TDA1540	Type indication of 14-bit D/A converter [1]
TDA1541	Type indication of dual 16-bit D/A converter [2]
TDA1534	Type indication of 14-bit A/D converter [3]
TDA1535	Type indication of sample-and-hold amplifier [4]
NE5160	Type indication of folding A/D converter [5]

Chapter 1

Introduction

In this introduction an overview of the contents of this book will be given. Analog-to-digital and digital-to-analog converters provide the link between the analog world of transducers and the digital world of signal processing, computing and other digital data collection or data processing systems. Numerous types of converters have been designed which use the best technology available at the time a design is made. The improvements in bipolar and MOS technologies result in high-resolution A/D and D/A converters which can be applied in digital audio systems. Furthermore, the high-speed bipolar technologies show an increase in conversion speed into the Giga Hertz range. Applications in these areas are, for example, in high-definition digital television and digital oscilloscopes. The availability of high-speed memory chips results in so-called "one-shot" memory applications in these oscilloscopes. In this book different techniques to improve the accuracy in high-resolution A/D and D/A converters will be discussed. Also, special techniques to reduce the number of elements in high-speed A/D converters by a repetitive use of comparators will be described.

In chapter two the application of converters in systems will be discussed. If analog-to-digital and digital-to-analog converters are applied in discrete-time systems it is important to perform these operations on frequency-band-limited signals. In most cases filters are needed to limit the input and output spectrum of the analog signals. If no band limitation is performed then aliasing of the analog signals into the signal band of interest can occur. General criteria which determine the overall system performance in the case of ideal converters are introduced and defined.

Performance definitions of converters are defined in chapter three. The performance definitions must be unique for a specific parameter. Good parameter definitions of converters are very important in determining the final performance of a discrete-time system. Furthermore, these definitions can be used to compare different brands of converters. In particular, a good definition of the dynamic parameters of converters is needed. The application of converters in digital audio and digital video systems for example requires these dynamic specifications. Many converters which originally were designed for high-accuracy measurement system applications are not optimized for dynamic operations. In digital audio, for example, many specifications which are important in instrumentation (such as offset, full scale accuracy,temperature drift) are of minor value. The specific dynamic parameters therefore must be defined and related to important design parameters.

After defining the important specifications of converters good measurement set-ups and definitions are needed. In chapter four attention is paid to measuring the dynamic performance of converters. Usually dc parameters can be measured with automatic test equipment and are well defined. Much attention has been paid to obtaining measurements and measurement set-ups which give the required parameter in a fairly simple and with a well-defined test condition. One of the most important parameters to be determined in this way is the dynamic range of a system. This dynamic range is determined by measuring the signal-to-noise ratio of a converter over half the sampling frequency. This signal-to-noise ratio must be close to the theoretical value, which is defined over a bandwidth equal to half the sampling frequency. When large discrepancies are found, then this converter is not designed to operate under dynamic conditions. Sometimes it is possible to overcome some of the problems by adding external circuitry, which for example can be a deglitcher circuit to reduce the glitch of the converter or by adding data latches which perform the switching of the bit weights in a digital-to-analog converter at the same time moment. A high-performance sample-and-hold amplifier in front of a parallel-type A/D converter can improve the dynamic performance of this converter. The sampling of the analog signal in this way is performed by the sample-and-hold amplifier. The following A/D converter must have a good settling performance to the applied input signal step from the sample-and-hold amplifier.

In general it can be said that humans are more inventive in the design of

analog-to-digital converter structures than in the design of digital-to-analog converter structures. The number of systems and circuits which can perform analog-to-digital conversion is much larger than the number of structures and basic solutions to digital-to-analog conversion. In chapter five examples of high-speed analog-to-digital converters are discussed. Up till now the full-flash converter was considered the fastest converter type which can be designed. This, however, is only partly true. Due to the use of a large amount of components, for example in an 8-bit converter 255 comparators are needed to detect every code level. The size of such a converter becomes large with respect to the time a signal needs to travel over the interconnection lines on a chip. In high-speed converters the time difference for signals travelling at the top of the converter structure with respect to signals travelling in the middle of the structure is in the order of pico seconds. Taking into account that the transmission speed over the interconnection lines in an integrated circuit is about two thirds of the speed of light, then 1 psec equals about 200 microns of interconnect. When the size of an analog-to-digital converter chip without sample-and-hold amplifier increases it is practically impossible to match clock- and signal-line delays within the required time accuracy. Therefore, improved converter systems using a continuous input-signal folding architecture are described. In the final system only zero crossings of the analog signal are important for the converter accuracy. To reduce the number of input amplifier-comparator stages in this system interpolation of zero crossings is used. This system results in a compact very high-performance analog-to-digital converter structure. In an MOS technology a switch and a capacitor are the main design elements. The input signal can be stored on multiple capacitors and then a comparison is made to perform the A/D conversion. Even two-step system solutions can be easily implemented in this structure. High-speed converter systems depend on the availability of high-performance sample-and-hold amplifiers. Such systems are difficult to design, while furthermore the maximum sampling frequency and the accuracy of the system are determined by the performance of the sample-and-hold amplifier. In digitally sampled (eg, fulle flash and folding A/D strucutures) systems mostly a much higher sampling clock can be applied without disturbing the analog signal path. In this way additional resolution and accuracy can be obtained by using oversampling.

In high-speed analog-to-digital converters which are based on the full-flash or folding principles the question about the relation between maximum analog input frequency and the bandwidth of the comparator-amplifier stages arises.

In chapter six an analysis which determines the relation between the maximum analog input frequency and the bandwidth of the comparator-amplifier stages is determined. Furthermore it will be shown from this analysis that a limited analog bandwidth of the system results in third-order signal distortion. This distortion can fold back into the baseband of the converter and results in a reduction in the signal-to-noise ratio of the system. The maximum analog input frequency will be defined as that input frequency for which the signal-to-noise ratio is reduced by a value equal to half the least significant bit. The number of effective bits as a function of input frequency will be used as an accurate measure for the performance of high-speed analog-to-digital converters.

In high-accuracy analog-to-digital and digital-to-analog converters the accuracy with which the binary weighting of the bit weights is performed is an important design criterion. Resistor or capacitor matching in integrated circuits limits the resolution of converters based on these elements to about ten to twelve bits. Trimming methods can be used to overcome this problem. These trimming methods, however, are expensive, while in addition changes of the trimmed elements due to time or temperature variations destroy the accurate trimming of the converter. In MOS technologies accuracy is obtained by matching binary weighted capacitor banks. Accuracies of 10- to 12-bits are possible without trimming.
When monotonicity of a converter is the most important design criterion then special system configurations are possible. When the absolute accuracy in the system is required, then special systems are needed.
Systems which convert the digital value in an accurate time need a limited amount of accurate elements. However, speed is limited, while systems with higher sampling rates suffer from extremely high clock frequencies which result in high frequency signal radiation.
In chapter seven generally applicable methods will be introduced. The first method combines accurate passive division with a time interchanging concept to obtain a very high weighting accuracy without using accurate elements. Furthermore, this method is independent of element aging and remains accurate over a large temperature range. Examples of 14- and 16-bit digital-to-analog and analog-to-digital converters will be given which use this special method. The system is not limited to bipolar technologies although at this moment only examples of bipolar implementations exist. In an MOS technology calibration of current sources can be used to obtain a segmented converter structure. Such a structure is less sensitive to elemtent

matching, while the calibration of the individual current sources makes the system independent of element aging and less temperature sensitive. The gate capacitance of an MOS device is used to store the error signal information which is needed to calibrate the bit current sources.

In high-accuracy analog-to-digital converters the analog input signal must be sampled and kept constant during the time the conversion takes place. High- resolution and high-accuracy sample-and-hold amplifiers are a key element for analog-to-digital conversion in, for example, digital audio. A sample-and- hold amplifier, designed in a bipolar technology will be given in chapter eight. This sample-and-hold amplifier uses high-performance operational amplifiers with improved frequency compensation techniques. A specially designed all-NPN class-B output stage with switching capability completes the design.

Low-noise high-stability reference sources are a basic element in converters. In integrated circuits reference sources are designed which are based on the bandgap voltage of silicon. The temperature dependence of the bandgap voltage reference sources is small, but in the case of 16-bit converters this temperature stability is not good enough. Therefore, systems which use a second order temperature compensation will be discussed in chapter nine. The noise analysis of these systems is performed and data will be given on the signal-to-noise ratio and methods to reduce the noise as a function of frequency.

Many circuits given in this book use bipolar technologies. Most of the designs were implemented in a standard 10 micron minimum-size double-metal process. The transition frequency of the transistors in this process is between 350 MHz and 400 MHz. In the high-speed folding and interpolation analog-to-digital converter an oxide-isolated bipolar process with a transition frequency between 7 and 8 GHz is used. The minimum emitter size of the transistors in this technology is 2 x 3 micron. The MOS circuits are implemented in 1 to 2 μ gatelength complementary MOS devices. Mostly such a technology is optimized for digital applications. Therefore the systems must be designed to be rather insensistive to MOS parameter variations and to be incorporated onto a large digital signal processing system. In that case special attention must be paid to the crosstalk problem between the digital system part and the mostly sensitive analag part of the A/D and D/A converter.

In chapter ten examples of noise-shaping techniques to improve the dynamic range of a system are described. Such techniques are very usefull when speed can be exchanged with respect to the wordlength used in the system.
An ultimate of this noise-shaping technique are the well known sigma-delta A/D and D/A converters which basically use a noise shaping filter in co-operation with a one bit D/A or A/D converter stage. Such a converter is extremely linear, which results in a very good differential linearity of such a converter. The most important design criteria and limitations will be given.

Chapter 2

The converter as a black box

2.1 Introduction

A/D and D/A converters are the link between the analog world of transducers and the digital world of signal processing and data handling. In an analog system bandwidth is limited by device and element performance and the parasitics introduced. Thermal noise generated in active and passive components limits the dynamic range of an analog system. The ratio between the maximum allowable analog signal and the noise determines the dynamic range of the system. The signal-to-noise (S/N) ratio is a measure of the maximum dynamic range. By definition the noise is measured over a bandwidth equal to half the sampling frequency of the system.
In a digital system the amplitude is quantized into discrete steps and at the same time the signal is sampled at discrete time intervals. When the sampling time moments at quantization differ from the sample time moments at the time the signal is reconstructed into an analog signal again, a signal distortion is introduced. This phenomenon is very important in time-discrete systems and finds it origin in "time jitter" or time uncertainty of the sampling clock. In particular, input signals at the high-frequency end of the signal band show a great sensitivity to a sampling time uncertainty. Furthermore, the sampling operation of analog signals introduces a repetition of input signal spectra at the sampling frequency and multiples of the sampling frequency. If the input signal bandwidth is larger than half the sampling frequency aliasing of spectra occurs. In that case frequencies around the sampling frequencies and its multiples are folded back into the baseband of the system. Usually this is an unwanted operation. To avoid

aliasing of the signal, the input bandwidth must be limited to not more than half the sampling frequency. (Nyquist criterion see [6]) This filtering must be performed by time-continuous filters.
The quantization of analog signals into a number of amplitude-discrete levels places limitations on the accuracy with which signals can be reproduced. This quantization error is often called "quantization noise" to indicate that the errors have a random amplitude distribution and in this way have a noise-like frequency spectrum. This random character, however, implies that under no circumstances should the analog input signal and the sampling clock have any correlation. If a correlation exists then the quantization errors appear at well-defined points in the frequency spectrum which are generally multiples of the signal frequency. The ratio between the input signal and the sampling frequency should preferably be a prime number to avoid this correlation. The dynamic range of a digital system is determined by the number of quantization levels.
In this chapter the different criteria mentioned will be described in more detail. The converter will be treated as an ideal black box. Specifications for input and output circuitry connected to the ideal converter will be derived under the condition that the overall system performance must be close to the ideal converter performance.

2.2 Basic D/A and A/D converter function

In Fig. 2.1 a block diagram of a D/A converter is shown. Digital signals are applied to the converter as parallel signals. Suppose we have a binary-

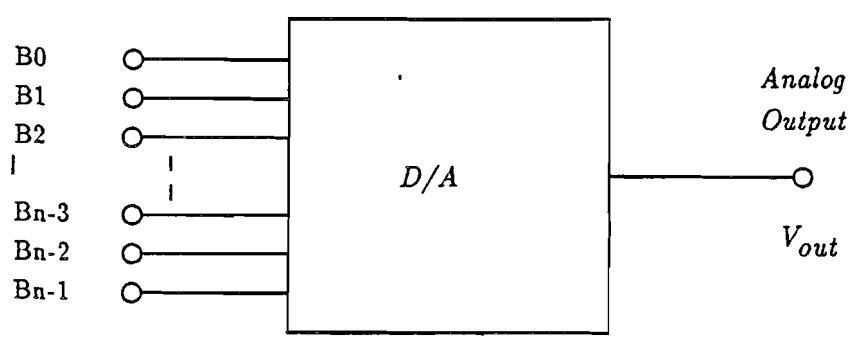

Figure 2.1 : Block diagram of a D/A converter

weighted converter, then the digital input value is converted into an analog

value using the following equation:

$$V_{out} = \sum_{m=0}^{m=n-1} B_m 2^{-m} R_{ref}. \tag{2.1}$$

In this equation V_{out} represents the analog output value and R_{ref} is a reference value.
Note that equation 2.1 represents a n-bit converter.
A reference current source or a reference voltage source is mostly used in practical implementations.
B_0 represents the Most Significant Bit (MSB) of the converter and B_{n-1} is the Least Significant Bit (LSB). The factor 2^{-m} indicates the binary weighting of the bit values as a function of the variable m.
A block diagram of an A/D converter is shown in Fig. 2.2. A sample-

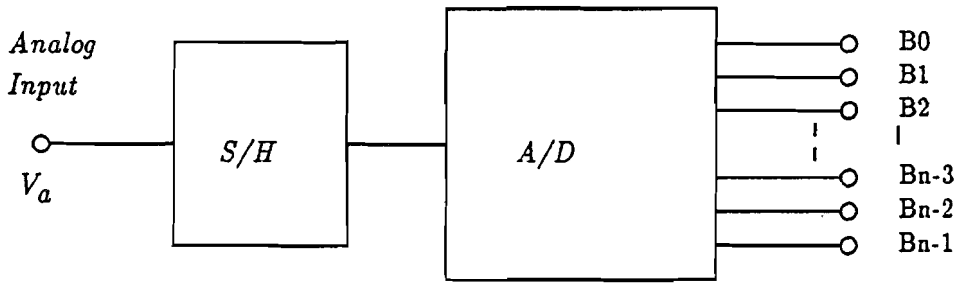

Figure 2.2 : Block diagram of an A/D converter

and-hold amplifier is added to sample the input signal and hold the signal information at the sampled value during the time in which the conversion into a digital number is performed. In an A/D converter the equation 2.1 changes into:

$$\frac{V_a}{R_{ref}} = D_{out} + q_e = \sum_{m=0}^{m=n-1} B_m 2^{-m} + q_e. \tag{2.2}$$

This can be partly rewritten as:

$$D_{out} = \sum_{m=0}^{m=n-1} B_m 2^{-m}. \tag{2.3}$$

In this equation D_{out} represents the digitized value of the analog input signal V_a and q_e represents the quantization error. The quantization error represents the difference between the analog input signal V_a and the quantized digital signal D_{out} when a finite number of quantization levels n is used.

2.3 Classification of signals

2.3.1 Analog signals

Analog signals are time-continuous and amplitude-continuous. Basically, there is no limitation in bandwidth and amplitude. When analog signals are processed by systems, however, frequency limitations are introduced and noise generated by active or passive components is added.
The dynamic range of a system is determined by the signal-to-noise ratio (S/N) of that system. An ideal test signal is supposed to be applied to that system for the determination of the signal-to-noise ratio. Maximum signal is determined by the distortion components generated in the system. A 10 % distortion level is adopted for example in power amplifiers to define the maximum signal level.

2.3.2 Time-discrete signals

Time-discrete signals are generated by sampling an analog signal at discrete time intervals without quantizing the amplitude of this signal. In most systems equal time intervals are used as the sampling clock. The sampling operation, however, introduces replicas of the input frequency spectrum around the sampling frequency and multiples of the sampling frequency. To avoid aliasing of frequency spectra, the input signal bandwidth must be limited to half the sampling frequency as implied by the Nyquist criterion [6]. When an analog signal has to be limited in bandwidth, then a time-continuous filter is needed to avoid a repetition of frequency spectra in this filter. Such filters, however, can introduce phase distortion, which may be audible in high-performance digital audio systems.
One example of a time-discrete system is a sample-and-hold amplifier. In such an amplifier analog signals are sampled and stored on a capacitor during the hold time. Samples are taken at well-defined discrete time intervals without quantizing the signal amplitude.

2.3.3 Amplitude-discrete signals

In a continuous time system the amplitude can be quantized into discrete amplitude levels, resulting in an amplitude-discrete signal. This operation can be performed to maintain well-defined amplitude levels when signals pass through several processing stages. This amplitude quantization introduces quantization errors which limit the accuracy and dynamic range of a system.

To obtain stepped output signals of the quantizer a high gain and a large comparator bandwidth is needed.

2.3.4 Digital signals

Digital signals are obtained if a signal is sampled at discrete time intervals and the amplitude is quantized in discrete amplitude levels. The amplitude quantization introduces quantization errors which limit the accuracy of the system. Sampling at discrete, equal time intervals, requires a limited input signal spectrum to avoid aliasing. Variations in sampling time moments of fast-changing analog signals result in amplitude quantization errors, compared with signals sampled at equal well-defined time intervals. To avoid such errors, the sampling time uncertainty must be small. Especially at the high end of the input frequency spectrum these errors are significant.
Digital values represent well-defined levels. In a binary coded system a "0" or ZERO represents an "off" or "false" state, while a "1" or ONE represents an "on" or "true" state. These well-defined levels are called logic levels which may be TTL, ECL or CMOS levels in a binary-coded system.
A/D and D/A converters perform digitization or reconstruction of analog signals. The performance of such a system can be measured by measuring the signal-to-noise ratio over a well-defined system bandwidth. To simplify comparison of converters a measuring bandwidth equal to half the sampling frequency is used. In the following paragraphs these definitions will be explained in more detail.

2.4 Sampling time uncertainty

Sampling time uncertainty introduces additional errors when analog signals are sampled at equal time intervals and reconstructed at time intervals which show a timing uncertainty or vice versa. To obtain quantitative insight into the problem of sampling time uncertainty, suppose that a sine wave close to half the sampling frequency is applied to an A/D converter. The maximum slope of the input signal occurs at the zero crossing of the signal as shown in Fig. 2.3. If the sampling time moment varies between t and $t + \Delta t$, then an amplitude variation between A_t and $A_t + \Delta A$ is obtained. The peak-to-peak amplitude variation ΔA must be at maximum equal to the quantization step q_s of the converter to avoid a loss in quantization resolution of the converter. As a result, the quantization step q_s is equal to the Least Significant Bit (LSB) value of the converter. Suppose furthermore that the converter has a

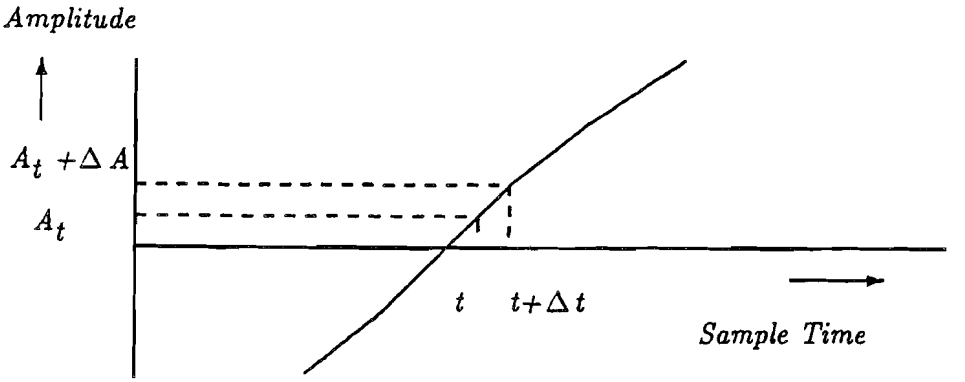

Figure 2.3 : Time-uncertainty calculation model

binary weighting with n bits, then the number of quantization levels is equal to 2^n. The sampling time uncertainty Δt must be so small that the LSB amplitude level is not exceeded for signals with a bandwidth equal to half the sampling frequency .
With a sine wave input of $V_{in} = Asin\omega t$ we obtain for the sampling time uncertainty:

$$\Delta t = \frac{\Delta A}{A\omega \cos \omega t}, \tag{2.4}$$

and with

$$\Delta A = \frac{2A}{2^n}, \tag{2.5}$$

the result becomes:

$$\Delta t = \frac{2^{-n}}{\pi f_{in} \cos 2\pi f_{in} t}. \tag{2.6}$$

Here $2A$ = peak-to-peak amplitude of the signal, $\omega = 2\pi f_{in}$ and f_{in} is the input signal frequency.
Formula 2.6 shows that the sampling time uncertainty depends on the moment the input signal is sampled (t is still in the equation!). The tightest specification for the sampling time uncertainty is obtained when $t = 0$.
Inserting $t = 0$ into formula 2.6 results in:

$$\Delta t_{max} = \frac{2^{-n}}{\pi f_{in}}. \tag{2.7}$$

As an example the sampling time uncertainty is calculated for a 16-bit digital audio system with an input frequency f_{in} of 20 kHz. Inserting these values into equation 2.7 gives a time uncertainty of less than $\frac{1}{4}$ nsec.

2.5 Quantization errors

The quantization process introduces an irreversible error. (see [7,8]). Therefore we want to calculate the relation between the quantization step q_s and the input signal V_{in}. The quantization step is determined by the number of steps a signal is quantized into. This number of quantization steps is expressed in a number of (binary-weighted) bits n. In Fig. 2.4 the quantization

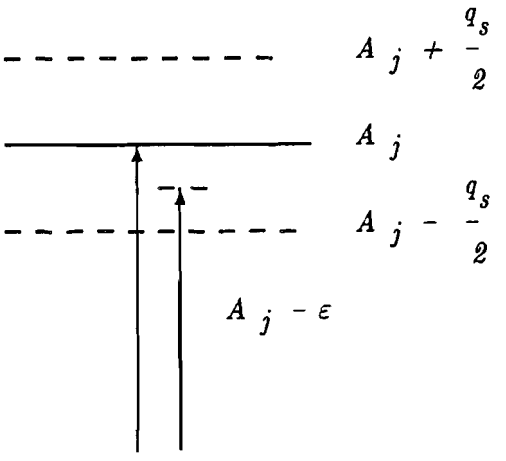

Figure 2.4 : Quantization of a signal at level A_j

of a signal at the amplitude level A_j is shown. A signal $A_j + \varepsilon$ is quantized into level A_j as long as the value of ε is between $-\frac{q_s}{2} < \varepsilon \leq \frac{q_s}{2}$. From this example it can be seen that the quantization error basically never exceeds an amplitude level equal to $\pm\frac{q_s}{2}$. Signals which are larger than $A_j + \frac{q_s}{2}$ are quantized to the next quantizer step A_{j+1}.
The mean-square-error due to quantization can now be calculated. We assume that over a long period of time all levels of uncertainty within the quantizing region $A_j \pm \frac{q_s}{2}$ appear the same number of times. A uniform probability distribution function over the interval $\pm\frac{q_s}{2}$ is defined in this way.

On this assumption the mean-squared value of ε will then be:

$$E(\varepsilon^2) = \frac{1}{q_s} \int_{-\frac{q_s}{2}}^{\frac{q_s}{2}} \varepsilon^2 d\varepsilon. \tag{2.8}$$

The symbol $E(.)$ represents the statistical expectation.
The average error value is zero on the assumptions made.
Solving the integral by using the uniform probability distribution function, the quantization error can be expressed as a quantization error voltage e_{qns}^2.
The rms quantization error voltage $e_{qns}^2 = E(\varepsilon^2)$ can be represented by:

$$e_{qns}^2 = \frac{1}{12} q_s^2. \tag{2.9}$$

The peak-to-peak signal amplitude A_{pp} in the system with n-bits and a full-scale signal amplitude is equal to:

$$A_{pp} = (2^n - S_{tcor}) \times q_s. \tag{2.10}$$

S_{tcor} is a correction factor to obtain an accurate amplitude of the fundamental of the signal frequency f_s. This correction factor can be accurately determined for $n = 1$. At that moment a square wave is generated at the output of the converter. After a series expansion of the square wave, the peak to peak amplitude of the fundamental becomes: $\frac{4}{\pi}$. Using this result to determine the value of S_{tcor} from equation 2.10 the following result is obtained:

$$\frac{4}{\pi} = 2 - S_{tcor} \tag{2.11}$$

Rearranging equation 2.11 results for the correction factor:

$$S_{tcor} = 2 - \frac{4}{\pi} \approx 0.73 \tag{2.12}$$

Although the value of equation 2.12 is exactly valed for a 1-bit quantizer, this value will be inserted into equation 2.10 to give the best approximation for conveters having a low resolution.
Inserting 2.12 into equation 2.10 results in:

$$A_{pp} = (2^n - 2 + \frac{4}{\pi}) \times q_s \tag{2.13}$$

It is easy to calculate the rms signal value A_{rms} of the signal A_{pp}:

$$A_{rms} = \frac{q_s \times (2^n - 2 + \frac{4}{\pi})}{2\sqrt{2}}. \tag{2.14}$$

In this calculation a *sine wave* signal is adopted. The signal-to-noise ratio (S/N) can be calculated using equation 2.14 divided by the square root of equation 2.9, resulting in:

$$S/N = (2^n - 2 + \frac{4}{\pi})\sqrt{1.5}. \tag{2.15}$$

Equation 2.15 can be simplified into:

$$S/N = 2^n\sqrt{1.5} \tag{2.16}$$

when a large number of quantization steps is used. Converting equation 2.16 into decibels results in:

$$S/N = n \times 6.02 + 1.76 \text{ dB}. \tag{2.17}$$

In general equations 2.16 and 2.17 are nearly always used to calculate the dynamic range of a converter. In this book these equations are adopted too. The errors are within the accuracy with which the dynamic range of a system can be measured.
When $n = 4$ the error is 0.4 dB. This error decreases to below 0.01 dB for $n = 10$.
Formula 2.17 shows that the dynamic range of a system increases by 6 dB when an extra bit is added. By definition the dynamic range of a system is equal to the signal-to-noise ratio of that system measured over a bandwidth equal to half the sampling frequency.
The dynamic range of a 16-bit digital audio system can be found by inserting $n = 16$ into formula 2.17. We obtain S/N = 98.1 dB.
Because the quantization error can be modelled by a random process we can compare this error with noise. By this modelling the quantization error is sometimes called quantization noise. It is very useful to express formula 2.9 as a noise density per unit bandwidth:

$$e^2_{qns}(f) = \frac{q_s^2}{12f_{sig}} = \frac{q_s^2}{6f_s}. \tag{2.18}$$

Here f_{sig} is the signal bandwidth and f_s is the sample frequency.
Because the signal-to-noise ratio in a system is calculated over a bandwidth equal to half the sampling frequency the following relation is used: $f_{sig} = \frac{1}{2}f_s$.
The signal-to-noise ratio as density now becomes:

$$S/N(f) = 2^{n-1}\sqrt{3}\sqrt{f_s}. \tag{2.19}$$

The signal-to-noise ratio of a system with a bandwidth of f_{sig} is found by dividing equation 2.19 by $\sqrt{f_{sig}}$.
The result becomes:

$$S/N_{system} = 2^{n-1}\sqrt{3}\sqrt{\frac{f_s}{f_{sig}}}. \tag{2.20}$$

It is very advantageous to use formula 2.20 for dynamic range calculations of systems which do not use Nyquist sampling.

2.6 Oversampling of converters

When in a system the sampling frequency is made much higher than the maximum signal frequency this operation is called "oversampling". The quantization error in this case is randomized over a larger frequency band. As a result the quantization noise density is reduced and the effective resolution of the system increases when the system bandwidth is kept equal to the bandwidth of a Nyquist sampled system using the lower sampling frequency. Using formula 2.20 we have an expression for the signal-to-noise ratio of the oversampled system:

$$S/N_{system} = 2^{n-1}\sqrt{3}\sqrt{\frac{f_s}{f_{sig}}}, \tag{2.21}$$

or in decibels we get

$$S/N = n \times 6.02 - 1.25 + 10\log\frac{f_s}{f_{sig}} \text{ dB}. \tag{2.22}$$

As an example the dynamic range of a four times oversampled system will be calculated. Inserting $\frac{f_s}{f_{sig}} = 8$ into formula 2.22 results in:

$$S/N = (n+1) \times 6.02 + 1.76 \text{ dB}. \tag{2.23}$$

Comparing this result with formula 2.17, it can be seen that the dynamic range increases by 6 dB or 1 bit. In Fig. 2.5 a graphical approach to the oversampling of converters is shown. Note the reduction in quantization noise density of the oversampled system. The total quantization error shown as shaded areas is equal for both systems because the same number of bits is used. In the dashed areas signals appear which are introduced by the

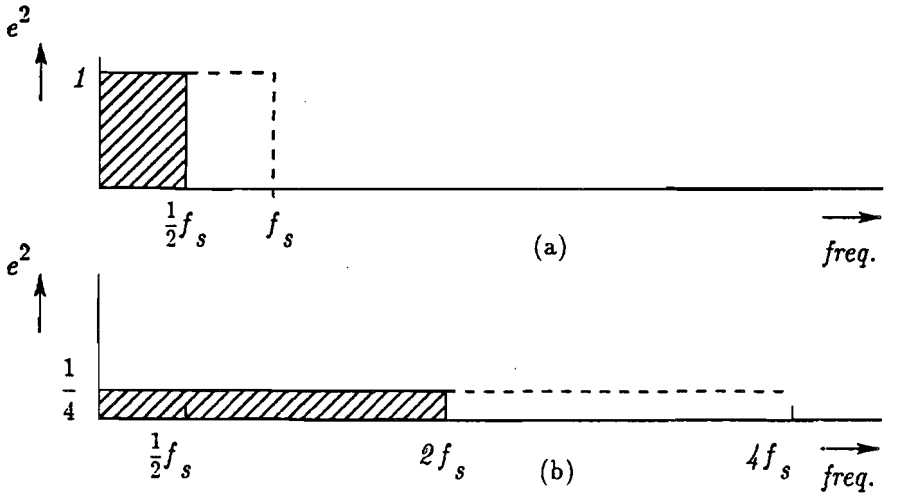

Figure 2.5 : (a) Quantization error of a Nyquist sampled converter system (b) Quantization error of a four times oversampled converter system

sampling process. For simplicity only the frequency range from zero to f_s or $4f_s$ is shown in the figure. The sampling operation introduces replicas of the frequency spectra at multiples of the sampling frequency too. Usually these replicas do not add additonal information to the picture and are therefore omitted. This omission is introduced in the following figures too. When the signal bandwidth is kept at $\frac{1}{2}f_s$ the total quantization error is reduced with a factor four in example b), and the increase in resolution with 1 bit is obtained. Furthermore the distortion in an oversampled system using the same signal bandwidth is reduced. This can be explained by supposing that a signal frequency close to the highest signal frequency is applied to the converter. In a Nyquist sampled system large quantization steps occur. Such large steps result in for example slewing of the output amplifier in a D/A converter system or slewing of the sample-and-hold amplifier in an A/D converter system. This slewing results in a non-linear operation of a part of the circuit which results in distortion. When a large oversampling is used, then the quantization steps are reduced. Mostly slewing of amplifiers can be avoided. As a result a lower distortion in the system is obtained.

2.7 Filtering

As stated before, the signal bandwidth in a sampled system must be limited to maximally half the sampling frequency. In an A/D converter system an analog filter precedes the converter. In a high-resolution system the attenuation of this filter must be large, while the transition band is usually small. Steep filters are needed because of the small transition band. These filters might be of the elliptical type. Such filters have a serious phase distortion. In digital audio systems, for example, this phase distortion can be audible. When constructing L, C type low-pass filters for measuring purpose, care must be taken in choosing the components used. Some type of practical capacitors show a non-linear behaviour resulting in distortion. High performance capacitors are needed in low-distortion systems to avoid this problem. Furthermore the size of the potcores used to construct the inductors must be large to avoid non-linear effects due to magnetic saturation in these cores. An additional problem may exist by mounting the potcores too close to eachother. In that way the magnetic fields generated by the coils are transferred through the filter. This results in a limited stop band attenuation. Using adequate elements low-pass measuring filters can be designed for digital audio systems up to a dynamic range of 20-bits.
To overcome this problem, oversampling of converters is used so a much simpler analog filter can be applied. Such a filter can be designed without too much phase distortion. The final channel filtering is performed by a transversal digital filter which has a linear phase characteristic. (see [48]).
In a D/A converter system low-pass filtering is needed to reject the frequency spectra above the band of interest. The reconstruction filter takes care of this process. Depending on the width of the transition band, a steep analog filter might be required. By using oversampling together with a digital filtering operation a high-performance reconstruction filter can be obtained. In the following paragraphs a more detailed analysis of the filtering operation will be given.

2.7.1 Anti-alias filtering in A/D converter systems

In Fig. 2.6(a) an A/D converter system with only analog filtering is shown. The shaded area (Fig. 2.6(b)) shows the signal response of an ideal filter. The drawn line close to half the sampling frequency shows the transition band of a more practical filter. The dashed area shows the stopband region of the input filter. This region is only drawn up to f_s, but actually starts

from $f = \frac{f_s}{2}$ to $f = \infty$. In systems with a minimum sampling rate compared to the analog bandwidth, a small transition band of the filter is required. Analog filters with such a steep characteristic mostly have a non-linear phase characteristic. Furthermore, the stopband rejection must be related to the number of bits in the system. Aliasing of these stopband signals should result in errors which are below the quantization noise level.

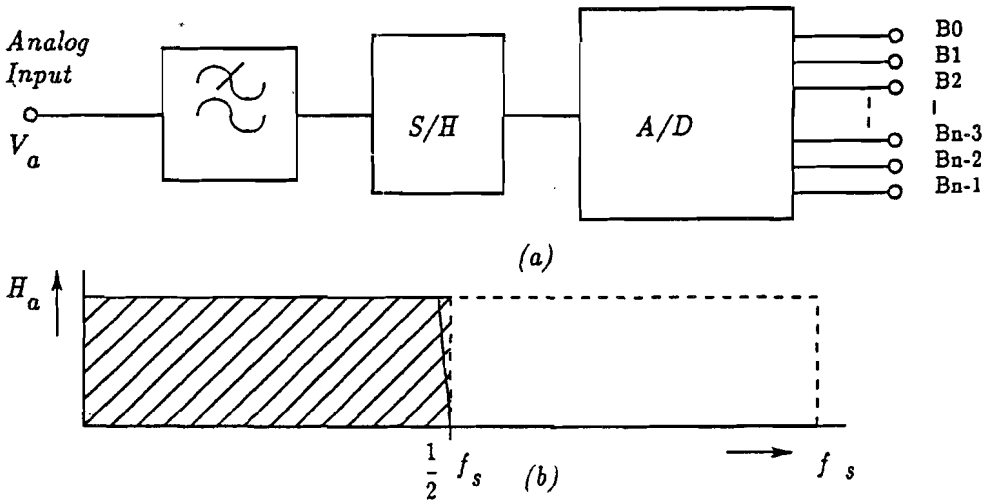

Figure 2.6 : (a) A/D converter system with analog filtering
(b) Analog filter response

A system which uses a combination of an analog prefiltering followed by a digital postfiltering filtering is shown in Fig. 2.7(a). In this system a four times oversampled A/D converter allows the use of a simpler analog nearly linear-phase prefilter to reject the signal band around the high sampling frequency $4f_s$. This simple analog filter is followed by a linear-phase digital filter performing the steep filtering characteristic. In Fig. 2.7(b) the filter characteristic of the analog filter is shown. The digital filter performs the steep filtering at $\frac{f_s}{2}$. Between $3\frac{1}{2}f_s$ and $4f_s$ the passband signal is reproduced again. However, signals, which can be present in the input-signal frequency spectrum are already filtered out by the analog prefilter. The attanuation of the analog input filter must be so large, that signals which are aliased by the sampling operation of sample-and-hold amplifier and appear in the input signal band are below the level of the quantization error. The digital postfilter then performs the required steep filtering around $\frac{f_s}{2}$. The final

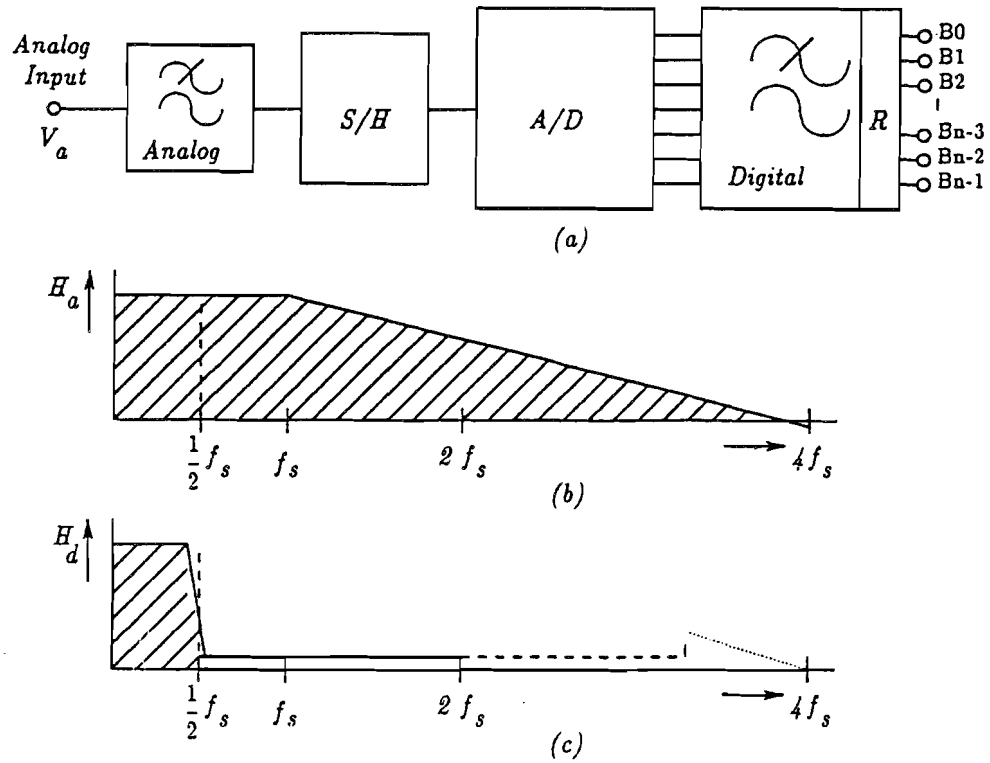

Figure 2.7 : (a) A/D converter system using combined analog and digital filtering
(b) Analog filter response
(c) Total filter response

result of the analog prefiltering and digital postfiltering operation is shown in Fig. 2.7(c). This final characteristic shows the high-frequency tail of the analog filter around $4f_s$. The stopband rejection of the combined analog and digital filter must be made so high that subsampling can be applied without aliasing the stopband signal components into the baseband. In that case digital output words at the lower sampling rate f_s can be supplied to the following digital signal processing circuitry. Remember also that the resolution of an oversampled system can increase. In some cases it can be advantageous to apply oversampling to increase the resolution of a system. (for example distortion products at the high-frequency band edge can be removed by using oversampling). In Fig. 2.7 the subsampling or decimation operation with a factor 4 is shown as the box called R. The final result of this whole operation is an accurate filtering with an almost linear phase characteristic.

Nowadays oversampling ratios of 8 or 16 in digital audio D/A converter systems is not unusual. Dynamic range of these systems increases in this way to above 98 dB, which is more than the input coding used on the disk. It can only be useful when additional digital signal processing is used. An example of such a processing can be tone control. In this application a dynamic range of 18-bits is needed. Furthermore the somewhat large dynamic range can improve the lineraity around zero when small input signals have to be reconstructed. Special noise-shaping techniques can be used to increase the dynamic range of a system. In chapter 10 these systems will be described.

2.7.2 Output filtering in D/A converter systems

In D/A converter systems low-pass filtering is needed to reject the repeated spectra around the sampling frequency and multiples of the sampling frequency. Only the baseband is of interest, while the high-frequency components of the ouput signal of the D/A converter can, for example, overload the power postamplifier which drives the loudspeaker in a digital audio system. This reconstruction filter removes the quantization steps from the signal and transforms it into a smooth amplitude. In Fig. 2.8 an ideal D/A converter

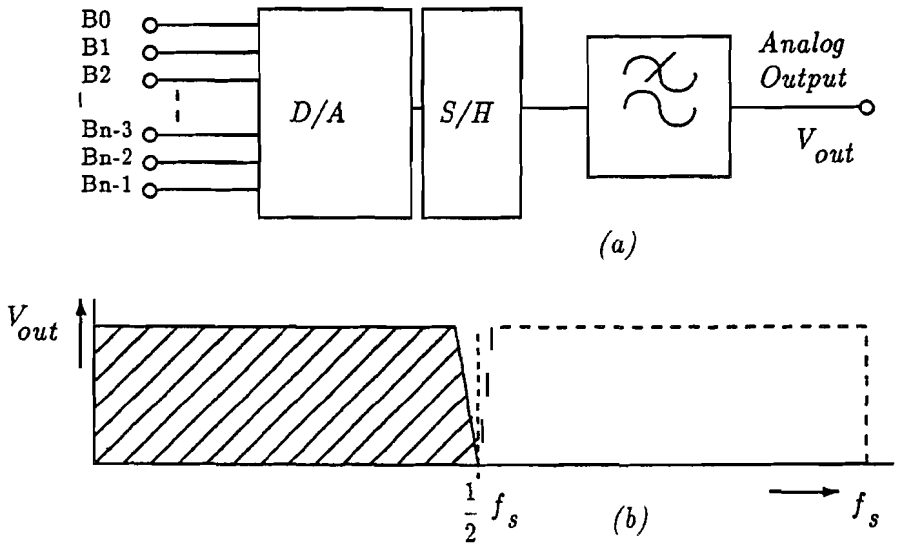

Figure 2.8 : (a) D/A converter system (b) Ideal amplitude characteristic of the total system

system is shown. Basically this system is the inverse function of the A/D

converter system shown in Fig. 2.6.
However, there is one big difference. D/A converters act as a sample-and-hold function during reproduction of the digital signal into an analog value. This zero-order hold operation introduces an extra amplitude distortion. A circuit block called sample-and-hold (S/H) is added in Fig. 2.8 to make this clear, while Fig. 2.9 shows the operation of a zero-order hold. During the hold time t_h of the D/A converter the analog output signal remains constant. The low-pass filter "averages" this signal resulting in the dashed output signal shown in the figure. The transfer function of the zero-order hold can be

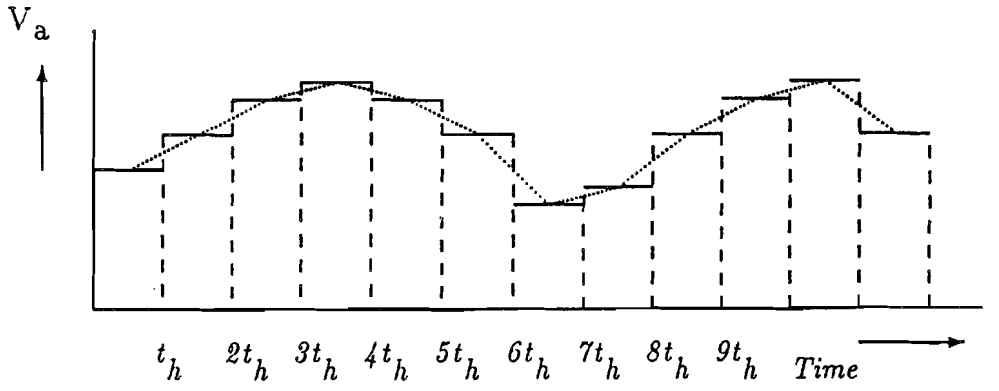

Figure 2.9 : Zero-order hold operation

calculated.
Suppose t_h is the time during which the data is in the hold mode, then the transfer function becomes:

$$H(j\omega) = \frac{1 - e^{-j\omega t_h}}{j\omega}. \tag{2.24}$$

After rearranging we obtain for the amplitude characteristic of the system:

$$\mid H(\omega) \mid = \frac{\sin \omega \frac{t_h}{2}}{\omega \frac{t_h}{2}}. \tag{2.25}$$

This is a well-known amplitude distortion called $\frac{\sin x}{x}$ distortion. In a normal D/A converter the hold time is equal to the sampling time so: $t_h = \frac{1}{f_s}$. Every clock cycle the input data can change and remains constant over that clock

cycle. With $\omega = 2\,\pi f_{in}$ formula 2.25 can be rewritten into:

$$\mid H(2\pi f_{in}) \mid = \frac{\sin \frac{\pi f_{in}}{f_s}}{\pi \frac{f_{in}}{f_s}}. \tag{2.26}$$

In D/A converter system which is sampled at the Nyquist rate, the maximum input frequency is equal to half the sampling frequency. Inserting $f_{in} = \frac{1}{2} f_s$ into equation 2.26 results in an amplitude reduction of $\frac{2}{\pi}$ or 3.92 dB. In some cases it is possible to design the analog low-pass filter in such a way that the $\frac{\sin x}{x}$ amplitude distortion is compensated for by an increase in the amplitude characteristic of this filter at the high frequency band edge.
A second possibility to overcome this problem is obtained by a decrease of the hold time t_h for example by a factor equal to four. In that case the amplitude reduction is only 0.22 dB at the same input frequency f_{in}.
Another possibility to avoid the amplitude reduction is obtained by increasing the sampling frequency of the converter. With the same input frequency f_{in} the ratio $\frac{f_{in}}{f_s}$ decreases, giving the desired result. Such an operation can be performed by oversampling the D/A converter. In Fig. 2.10(a) a D/A converter which combines a digital oversampling annex low-pass filtering function is shown. With the box called R the oversampling is introduced. In this specific example a four times oversampling is used. In reference [9] a detailed description of such a system is given. The digital filtering performs the steep filtering between $\frac{f_s}{2}$ and $3\frac{f_s}{2}$. The analog postfilter takes care of the signal band around $4f_s$. This is shown in Fig. 2.10(c) using the dashed slanting line. The analog filter can be designed having a nearly linear phase characteristic. As a result, the amplitude distortion due to the $\frac{\sin x}{x}$ signal reduction is reduced to 0.22 dB. Although the filter exhibits a small transition band, a nearly linear overall phase characteristic is obtained.

2.8 Minimum required stopband attenuation

Suppose the low-pass filter in the A/D converter system as shown in Fig. 2.6 has a limited stopband rejection. Suppose furthermore that the analog bandwidth of the input amplifier or the comparator in the A/D converter is limited to f_{comp}. Due to the sampling of the input signal all input signal frequencies which are in the aliasing signal bands are folded back into the baseband of the system. The number of aliasing signal bands which are folded back into the baseband are limited by the extra filtering introduced by the input signal amplifier or the bandwidth of the comparator in the

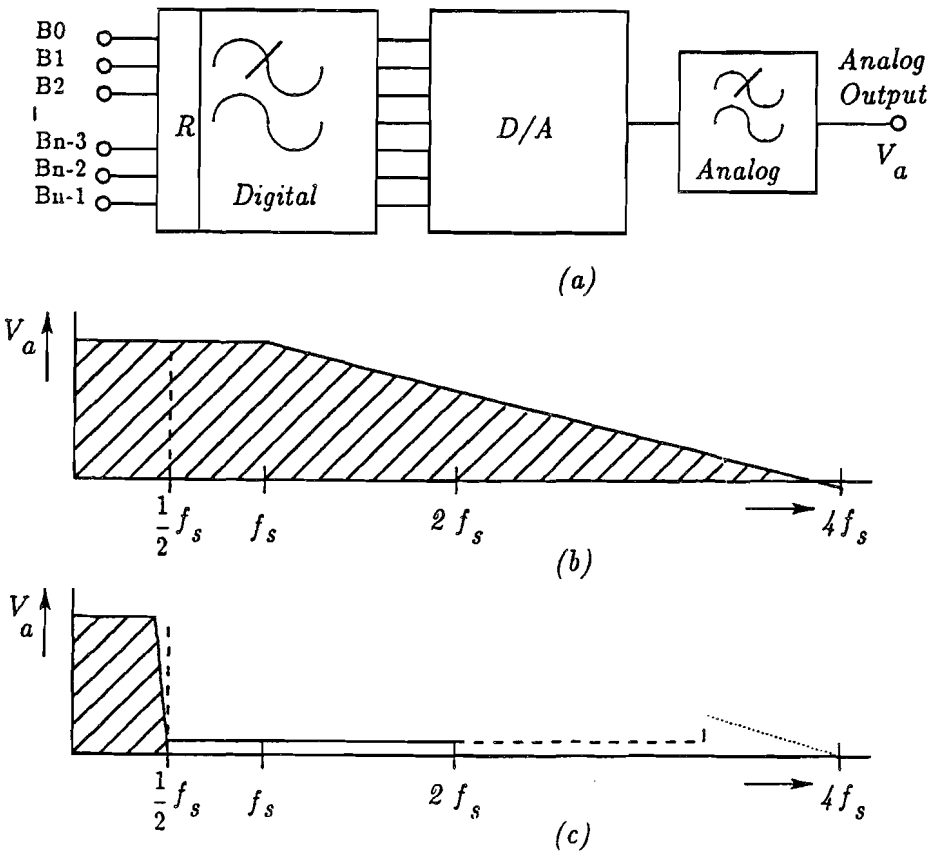

Figure 2.10 : (a) D/A converter system using combined digital-analog low-pass filters
(b) Amplitude characteristic of the analog postfilter (c) Amplitude characteristic of the total system

A/D converter. In Fig. 2.11 the attenuated signal at the output of the amplifier comparator stage is shown as a function of frequency. Note that the bandwidth f_{comp} of the input amplifier or comparator in this case is about $3f_s$. When noise with a frequency spectrum between $f = \frac{f_s}{2}$ and $f \gg 3f_s$ is input into the system, then the number of bands which are folding back noise into the baseband of the system is equal to:

$$N_{fold} = \frac{f_{comp} - \frac{f_s}{2}}{\frac{f_s}{2}}. \tag{2.27}$$

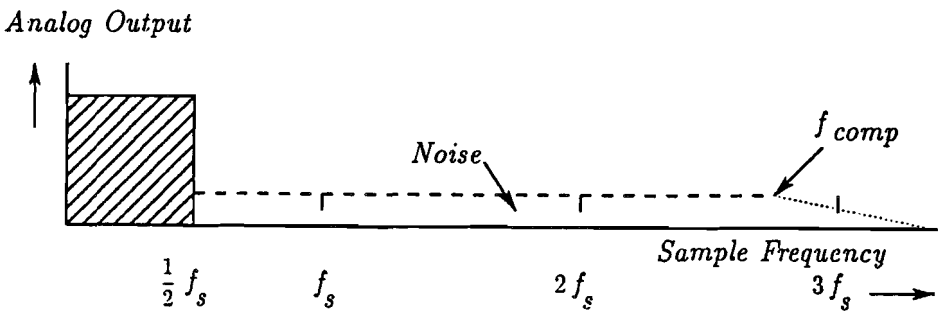

Figure 2.11 : Output signal of the amplifier-comparator stage in an A/D converter system

The fold-back noise adds to the quantization error and thus reduces the signal-to-noise ratio of the system. The quantization "noise" in the baseband now increases by a factor

$$\sqrt{N_{fold}} = \sqrt{2 \times \frac{f_{comp}}{f_s} - 1}. \tag{2.28}$$

If we wish to have a condition in which the total foldback-noise in the baseband is equal to the quantization "noise" in the system when a signal is applied in the baseband, then the stopband rejection of the low-pass filter must be increased by a factor equal to: $\sqrt{N_{fold}}$.
This increase in stopband rejection ($A_{foldback}$) is equal to:

$$A_{foldback} = \sqrt{N_{fold}} = 10 \log N_{fold}\ dB. \tag{2.29}$$

This means that in a system with n bits the minimum stopband rejection of the input filter must be:

$$A_{stopmin} = n \times 6.02 + 1.76 + 10 \log N_{fold}. \tag{2.30}$$

Inserting formula 2.28 into formula 2.30 results in an expression for the minimum required stopband rejection $A_{stopmin}$:

$$A_{stopmin} = n \times 6.02 + 1.76 + 10 \log(2 \times \frac{f_{comp}}{f_s} - 1)\ dB. \tag{2.31}$$

When a low-pass filter with a minimum stopband rejection equal to 2.31 is used, then the dynamic range (S/N ratio) of the system is reduced by 3 dB.

If a smaller reduction is required, then the stopband attenuation must be increased.
Although an A/D converter is mostly preceded by a sample-and-hold amplifier, the transfer function of this sample-and-hold unit does not introduce the well-known $\frac{\sin x}{x}$ amplitude distortion. The reason is that the sample-and-hold amplifier tracks the input signal during sample mode. At the moment the amplifier is switched from the sample to the hold mode, the peak signal value is taken. This means that at the sample moments the exact signal value is sampled and converted into a digital value. No holding or averaging of the signal occurs. The extra hold time is only needed to allow the A/D converter to perform the conversion from an analog time-discrete signal into a digital output signal.
As an example, the minimum stopband rejection of an input filter for an audio A/D converter will be calculated. This calculation involves the worst-case condition of signals outside the signal band. Suppose the bandwidth of the comparator is equal to 8.8 MHz, then with a sampling frequency of 44 kHz we obtain for the minimum stopband rejection using formula 2.31 $A_{stopband} = 98 + 23 = 121$ dB. In practical situations, however, the noise and signals outside the baseband usually do not have the maximum amplitude equal to the signal amplitude. Furthermore, the basic A/D converter itself must have a signal-to-noise ratio measured over the signal band close to the theoretical value of 98.1 dB.

2.9 Conclusion

In this chapter the dynamic range of A/D and D/A converters is defined and requirements for input and output filters are introduced. Different methods of anti-alias or reconstruction filtering are shown. If a linear phase characteristic is required in a system then a combined analog-digital filtering solution gives the best results.
A general relation defining the sampling time uncertainty in relation to the resolution of the converter and the maximum input signal frequency is derived. This relation determines the stability of the sampling clock required over a short period of time.
An analysis of the amplitude distortion in D/A converters is given. Oversampling or reduction of output sample time reduces this distortion to acceptable values.

Chapter 3

Specifications of converters

3.1 Introduction

To obtain insight into the design criteria for converters it is important to arrive at a unanimous definition of specifications. These specifications must include the application of converters in conversion systems (see references [10,11]). Dynamic specifications of converters are needed to obtain insight in the applicability of a certain converter in a digital signal processing system e.g. digital audio or digital video. In a conversion system the complete conversion from analog into digital or digital into analog information is performed. Such systems include input or output amplification and anti-alias filtering.
Unanimous specifications for dc performance are well known in literature. Specifications for converters in signal-processing systems are more difficult to standardize. One of the reasons for this limitation in specification can be that in the early days of conversion the application of converters was in the area of digital voltmeters and control systems. These systems need the high dc performance at low signal speeds.
Digital audio in comparison with voltmeters, for example, applies for high-performance dynamic system specifications. The performance of converters in digital audio systems is at the limit of the possibilities of today's technology. In this chapter the most important specifications will be defined and discussed in more detail.

3.2 Digital data coding

Information in digital form appears at the input of a D/A converter or at the output of an A/D converter. This code can appear in parallel form or serially on a single line.
In the digital world several logic systems are used. Today's CMOS logic is overtaking the widely used Transistor Transistor Logic (TTL) in which a "1", ONE or "true" represents a minimum level of +2.4 V and "0", ZERO or "false" corresponds to a maximum level of +0.4 V. CMOS logic swings are determined by the applied supply voltage, which for todays logic blocks is 5 V. The output swing of CMOS logic then close to 5 V. In high-speed systems Emitter Coupled Logic (ECL) is used with levels of - 0.9 V for a logic "1" and - 1.8 V for a logic "0". The small logic swing of 0.9 V allows high-speed applications. The advantage of ECL circuits is the possibility of a full differential system operation. This differential operation prevents large current spikes from flowing in the supply lines during switching. Thus a low interference between the analog signal path and the digital signal path can be obtained.
In systems with a serial digital data stream a conversion from the serial stream into a parallel word must be performed. A shift register which performs serial to parallel conversion is added for this purpose. Furthermore data latches are added which at the end of the serial-to-parallel conversion get the data word latched on the command of the latch clock. These data latches directly drive the current or voltage switches for example in a D/A converter. Analog data appears at the output of the converter after new data is latched in. The data latches together with the bit switches are optimized to obtain a minimal output glitch during switching of the converter. This is very important in a D/A converter system. Such a system can be operated without a so-called deglitcher when the glitch energy is small compared to the LSB area. In Fig. 3.1 an example of a serial-to-parallel conversion in a D/A converter is shown.

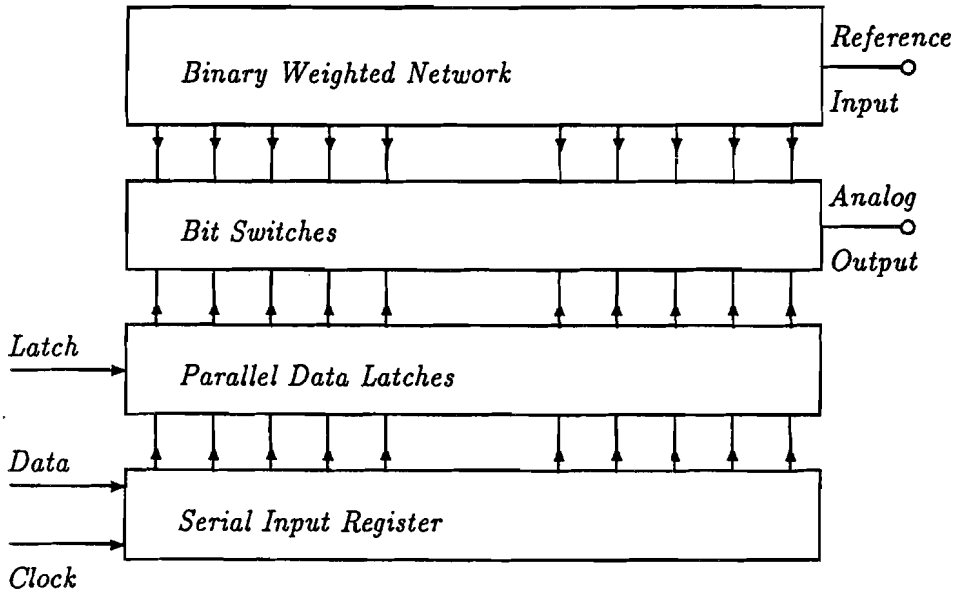

Figure 3.1 : Serial-to-parallel conversion in a D/A converter

The advantage of this circuit configuration is that the data latches together with the bit switches can be optimized for the best switching performance. Usually this means the smallest glitch error. D/A converters with parallel digital inputs often do not have data latches on board. Applying these converters requires an accurate board layout to match the delays between the output signals of the data latches and the switches. Users are not always aware of this problem and therefore end up with a low overall performance of the converter system. Large "glitches" may appear at the output of the converter because of the non-equal switching time of bit switches during code transitions. A "glitch" is a large output signal change (larger than the amplitude of an LSB step) appearing during a code transition of a D/A converter.

3.3 Digital coding schemes

As a digital code the natural binary code (base 2) is used. Without additional measures it is difficult to obtain bipolar signals. Therefore, an offset binary code is introduced. This code is "offset" by turning on the MSB bit for an analog value of zero. Mostly an additional current is added to subtract the MSB bit current from the input or output current value to obtain analog

zero. The principal drawback of the offset binary code is that a major carry transition occurs if a small bipolar signal is generated or converted around zero. Such a transition requires the highest linearity around zero and immediately gives rise to "glitch" problems. These problems are worst for D/A converters. In A/D converters the noise which is part of the offset current is added to the input signal and may result in a reduction of the dynamic range of the system. Furthermore this offset must be stable with temperature and variations in supply voltage should not change the zero setting of the A/D converter.
A Sign-Magnitude code seems to be the most straightforward approach to the glitch and noise problem. The Sign-Magnitude coding introduces an inverter into the system operating on the command of the sign bit of the signal. This inverter, however, introduces an accuracy problem which is even more difficult to solve in high-resolution converters than the dc "offsetting" of the converter in the offset binary mode.
Other codes can also be used. When computational operations are needed the Twos Complement code is very useful. In Fig. 3.2 is a table showing the different codes which can be used in converters. From the table it can be

	Decimal Fraction					
	Positive	Negative	Sign +	Twos	Offset	Ones
Number	Reference	Reference	Magnitude	Complement	Binary	Complement
+7	+7/8	−7/8	0 1 1 1	0 1 1 1	1 1 1 1	0 1 1 1
+6	+6/8	−6/8	0 1 1 0	0 1 1 0	1 1 1 0	0 1 1 0
+5	+5/8	−5/8	0 1 0 1	0 1 0 1	1 1 0 1	0 1 0 1
+4	+4/8	−4/8	0 1 0 0	0 1 0 0	1 1 0 0	0 1 0 0
+3	+3/8	−3/8	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1
+2	+2/8	−2/8	0 0 1 0	0 0 1 0	1 0 1 0	0 0 1 0
+1	+1/8	−1/8	0 0 0 1	0 0 0 1	1 0 0 1	0 0 0 1
0	0+	0−	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
0	0−	0+	1 0 0 0	(0 0 0 0)	(1 0 0 0)	1 1 1 1
−1	−1/8	+1/8	1 0 0 1	1 1 1 1	0 1 1 1	1 1 1 0
−2	−2/8	+2/8	1 0 1 0	1 1 1 0	0 1 1 0	1 1 0 1
−3	−3/8	+3/8	1 0 1 1	1 1 0 1	0 1 0 1	1 1 0 0
−4	−4/8	+4/8	1 1 0 0	1 1 0 0	0 1 0 0	1 0 1 1
−5	−5/8	+5/8	1 1 0 1	1 0 1 1	0 0 1 1	1 0 1 0
−6	−6/8	+6/8	1 1 1 0	1 0 1 0	0 0 1 0	1 0 0 1
−7	−7/8	+7/8	1 1 1 1	1 0 0 1	0 0 0 1	1 0 0 0
−8	−8/8	+8/8		1 0 0 0	0 0 0 0	

Figure 3.2 : Different digital coding schemes

seen that with the Ones Complement and the Sign-Magnitude code two code

possibilities for zero are found. codes. A computation has to be performed to avoid this double zero coding.

3.4 DC specifications

3.4.1 Absolute accuracy

Accuracy of converters should not be confused with linearity and resolution. It includes the errors of quantization, non-linearities, short-term drift, offset and noise.
The *absolute accuracy* of a converter is the actual full-scale output signal (voltage, current or charge) referred to the absolute standard of the National Bureau of Standards. This absolute accuracy is mostly related to the reference source used in the converter. Sometimes this reference source consists of a special temperature-compensated zener diode. In integrated circuits this zener diode is replaced by an integrable source which in modern systems is based on the bandgap voltage of silicon. This reference source should have a low-noise with respect to the resolution of the converter. Temperature coefficients in the ideal case should be so small that the accuracy of the reference over the specified temperature range stays within the resolution of the converter ($\frac{1}{2}$ LSB over the full temperature range).

3.4.2 Relative accuracy

The *relative accuracy* is the deviation of the output signal or output code of a converter from a straight line drawn through zero and full scale.
This error is called: *Integral Non Linearity* (INL) or sometimes *linearity*. Throughout this book the Integral Non Linearity will be used.
In Fig. 3.3 a graphical example is shown of the integral non-linearity definition. In the figure the boundaries for which the non-linearity deviates not more than $\pm \frac{1}{2}$ LSB of a straight line through zero and full scale are shown. The $\pm \frac{1}{2}$ LSB integral non-linearity definition implies a *monotonic* behaviour of this converter.
Monotonicity of a converter means that the output of, for example, a D/A converter never decreases with an increasing digital input code. A minimum increase of *zero* is allowed for a 1 LSB increase in input signal. In Fig. 3.3 the transfer curve of a monotonic converter is shown.
It must be noted at this point that converters can be designed which are *guaranteed monotonic* but do not have the half LSB linearity specification.

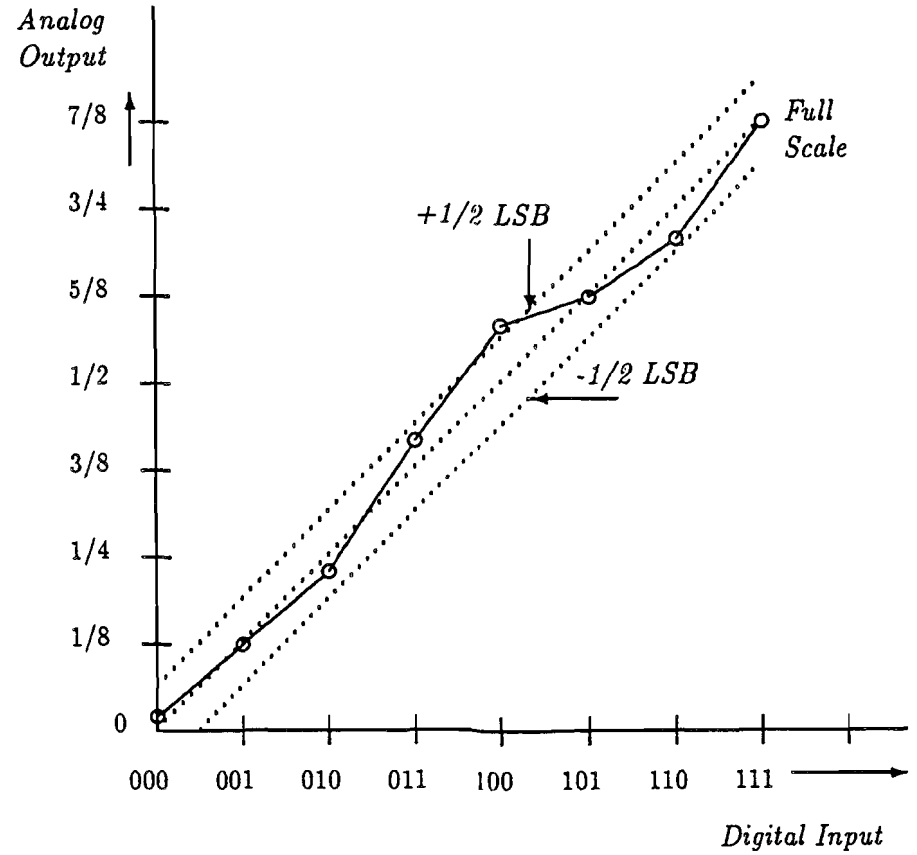

Figure 3.3 : Definition of the Integral Non-Linearity of a converter

These converters are based on non-binary weighting of the bit currents. They can for example use a tapped resistor network.
The specification of *monotonicity* does NOT include that a converter has a $\pm \frac{1}{2}$ LSB integral non-linearity error! Examples of converters which are monotonic by design are presented in references [12,13,14].

3.4.3 Non-linearity calculation

A simple calculation can be performed to show that the non-linearity specification of $\pm \frac{1}{2}$ LSB is necessary to prove *monotonicity* of a binary-weighted converter.
Suppose we have an n-bit binary-weighted converter, then with ϵ_m corre-

sponding to the error of the m^{th} bit, the non-ideal weighting of this bit can be written as:

$$b_m = 2^m + \epsilon_m. \tag{3.1}$$

Note that a unity LSB bit-weight is used in this equation. This does not influence the non-linearity calculations.
The non-linearity will now be calculated as the total deviation from a straight line between zero and full scale. The full-scale value B of an n-bit converter can be expressed as:

$$B = \sum_{m=0}^{m=n-1} (2^m + \epsilon_m). \tag{3.2}$$

With

$$\sum_{m=0}^{m=n-1} 2^m = 2^n - 1, \tag{3.3}$$

this can be simplified into:

$$B = 2^n - 1 + \sum_{m=0}^{m=n-1} \epsilon_m. \tag{3.4}$$

Note that the total number of quantization steps is given by equation 3.2. The "ideal" stepsize S of the converter can be calculated using the full-scale value of the converter and the number of quantization steps, resulting in:

$$S = \frac{B}{2^n - 1} = 1 + \frac{\sum_{m=0}^{m=n-1} \epsilon_m}{2^n - 1}. \tag{3.5}$$

The linearity error Δ_k of the k^{th} bit compared with a value obtained from the ideal straight line through zero and full scale becomes:

$$\Delta_k = 2^k \times (1 + \frac{\sum_{m=o}^{m=n-1} \epsilon_m}{2^n - 1}) - (2^k + \epsilon_k). \tag{3.6}$$

In general errors will have positive and negative signs. Adding all errors together must result in a total error of zero, because the sum of all non ideal bit-weights is used as the full scale value. The following calculation proves this statement. Summing Δ_k results in:

$$\sum_{k=0}^{k=n-1} \Delta_k = \sum_{k=0}^{k=n-1} \frac{2^k}{2^n - 1} \times \sum_{m=0}^{m=n-1} \epsilon_m - \sum_{k=0}^{k=n-1} \epsilon_k. \tag{3.7}$$

Inserting again:

$$\sum_{k=o}^{k=n-1} 2^k = 2^n - 1, \tag{3.8}$$

this equation can be simplified into:

$$\sum_{k=o}^{k=n-1} \Delta_k = \sum_{m=0}^{m=n-1} \epsilon_m - \sum_{k=0}^{k=n-1} \epsilon_k = 0. \tag{3.9}$$

As a result of this calculation the absolute values of the sum of all positive errors Δ_k must be equal to the sum of all negative errors Δ_k. The integral non-linearity of a converter (INL) is now specified as the total error of the positive or negative errors or:

$$INL = \sum_{k=0}^{k=n-1} Positive\Delta_k = -\sum_{k=0}^{k=n-1} Negative\Delta_k \leq \frac{1}{2} LSB. \tag{3.10}$$

To prove *monotonicity* of a binary-weighted converter suppose that as a first step only the MSB bit value is too small. This means that the sum of the remaining bit errors must be equal to the MSB bit error but with the opposite sign. The non-linearity error Δ_{n-1} of the MSB bit can be expressed as:

$$\Delta_{n-1} = 2^{n-1} \times (1 + \frac{\sum_{m=0}^{m=n-1} \epsilon_m}{2^n - 1}) - (2^{n-1} + \epsilon_{n-1}), \tag{3.11}$$

or:

$$\Delta_{n-1} = (\frac{2^{n-1}}{2^n - 1} \times \sum_{m=0}^{m=n-1} \epsilon_m) - \epsilon_{n-1}. \tag{3.12}$$

As defined in equation 3.10 the MSB-bit error given by equation 3.12 is equal to the integral non-linearity (INL) of the converter. Thus:

$$INL = \Delta_{n-1} \tag{3.13}$$

In Fig. 3.4 the minimum condition for *monotonicity* is shown. The dashed slanted lines indicate the $\pm \frac{1}{2}$ LSB boundaries determined by the integral non-linearity specification. As is shown, this converter has a $\pm \frac{1}{2}$ LSB non-linearity specification.
When the MSB-bit is smaller than the sum of the other bits, the converter becomes *non – monotonic* as is indicated by the dashed curve in the figure. The major carry transition from all bits except MSB switched on (011) compared to only MSB switched on (100) is shown. Furthermore, it is supposed

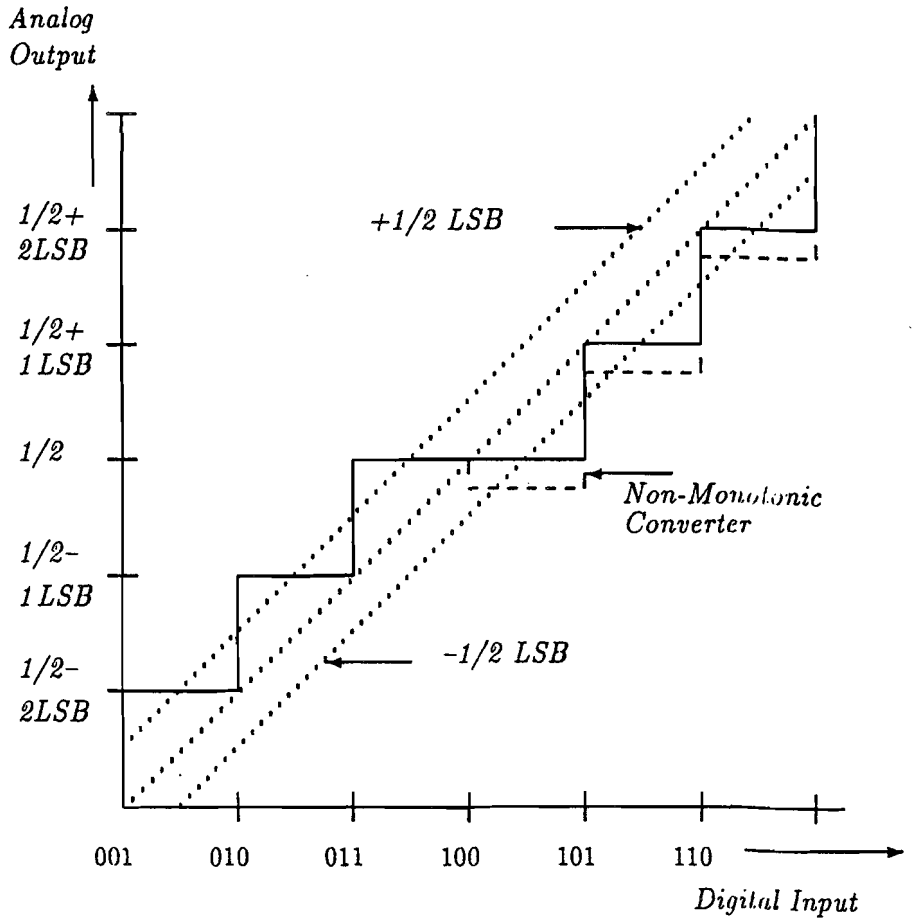

Figure 3.4 : MSB major carry transition

that the MSB bit value is too small compared to the rest of all bits.
The linearity error given by equation 3.10 is a measure for *monotonicity* of the converter. When in a D/A converter the digital input code is increased by a value of 1 LSB then the minimum requirement for *monotonicity* is no increase in analog output value as shown in Fig. 3.4. This means that twice the error given by equation 3.12 must be less or equal to 1 LSB or:

$$\Delta_{n-1} = \frac{2^{n-1}}{2^n - 1} \times \sum_{m=0}^{m=n-1} \epsilon_m - \epsilon_{n-1} \leq \frac{1}{2} LSB, \tag{3.14}$$

or:

$$INL \leq \frac{1}{2} LSB. \tag{3.15}$$

In general it can be said that the errors of the individual bit weights must be added according to the definition given in equation 3.10. To guarantee *monotonicity* of the converter the sum of the errors must never exceed $\frac{1}{2}$ LSB value. An identical calculation can be performed for other bit weights in the converter. In this way the generalized *monotonicity* defintion can be proven.
In Fig. 3.5 the errors of the individual bit-weights of a binary weighted converter are shown. The errors for full-scale and zero are calibrated to be zero. In this way a straight line between zero and full-scale is obtained. Starting from the left side of the figure, the errors start from the MSB-error and go down to the LSB-error. Finally the total of the positive and the negative errors are plotted at the most right side. This converter can be specified as having a $\pm \frac{1}{4}$ LSB integral non-linearity error. In a converter it is always

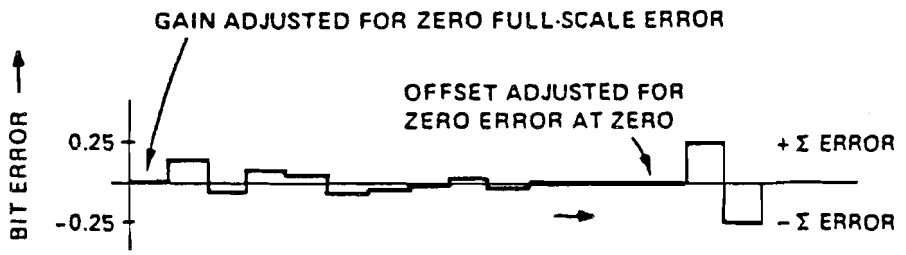

Figure 3.5 : Bit-weight error of a binary weighted converter

possible to generate a code which coincides with this worst case error. Furthermore a converter might be *monotonic* having a linearity error of more than $\frac{1}{2}$ LSB. In that case an increase in analog output larger than 2 LSBs is possible. A "missing" code value is introduced in this converter.
Conclusion: A converter is always *monotonic* when the integral non-linearity specification (INL) is less than or equal to $\pm \frac{1}{2}$ LSB.

However, when a converter is specified to be always *monotonic* then this specification does not automatically imply an integral non-linearity error of less than or equal to $\pm \frac{1}{2}$ LSB.

3.4.4 Differential non-linearity

Differential non-linearity (DNL) error describes the difference between two adjacent analog signal values compared to the step size (LSB weight) of a converter generated by transitions between adjacent pairs of digital code numbers over the full range of the converter.
The differential non-linearity is zero if every transition to its neighbours equals 1 LSB. In a *monotonic binary – weighted* converter an increase of the digital code value by 1 LSB can result in an increase in analog signal between 0 and 2 LSBs. The maximum differential non-linearity in this case is ± 1 LSB.
Writing down the differential non-linearity in a formula gives:

$$DNL = S_{out}(C_{m+1}) - S_{out}(C_m) - 1LSB \tag{3.16}$$

C_{m+1} and C_m are two adjacent digital codes.
S_{out} is the output signal of the converter.
In Fig. 3.6 the transfer curve of a 4-bit A/D converter is shown. The drawn line shows the ideal transfer characteristic, while a dashed line indicates the different non-linearity errors which may occur in practical converters. Integral non-linearity (INL), differential non-linearity (DNL) and full scale range (FSR) are shown partly as a function of the LSB error using dashed lines. Furthermore an example of a missing code is given in the picture. In a visualized way the non-linearity errors are shown to improve understanding.

3.4.5 Offset

Input and output amplifiers and comparators in practical circuits inherently have a built-in offset voltage and offset current. This offset is caused by the finite matching of components in integrated circuits. Such an offset results in a non-zero input- or output voltage, current or digital code.
Offset is very important in dc systems. Temperature dependence of the offset must be small. Trimming or auto zero procedures can remove the offset in a system. Furthermore care must be taken during the layout of the circuit to avoid thermal coupling and thermal gradients over an integrated circuit. If such a coupling exists, then the output code or output signal can change depending on the applied signal.

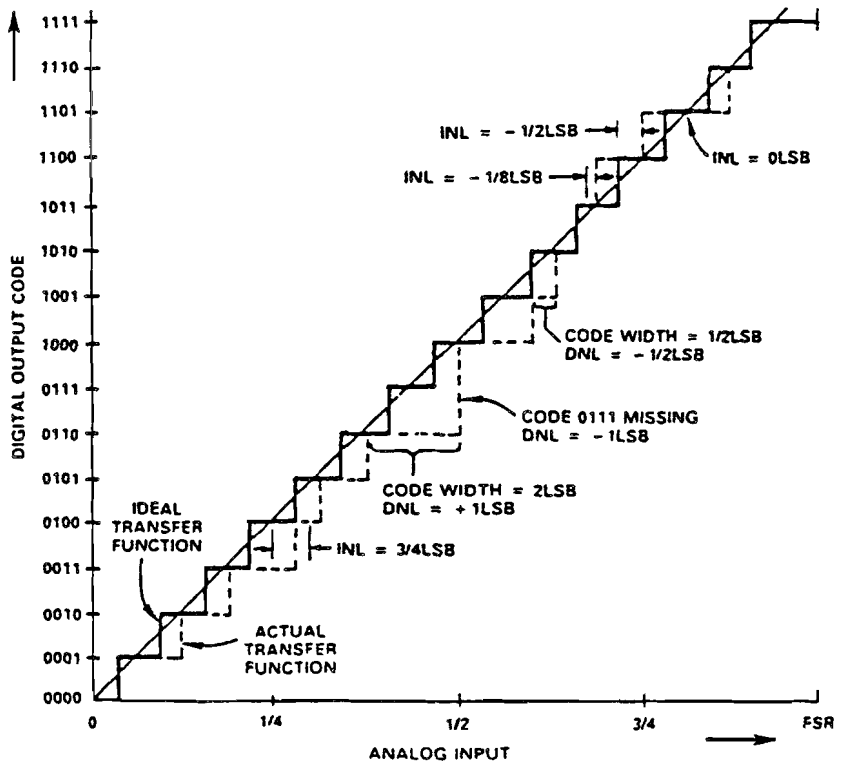

Figure 3.6 : Transfer curve of a 4-bit A/D converter

3.4.6 Temperature dependence

Monotonicity and linearity must be maintained over a large temperature range (-20^0 C to $+85^0$ C) to keep distortion and signal-to-noise ratio within the specified range. Mostly this requires a very good thermal tracking of components. In an n-bit system with a relative accuracy of $\pm \frac{1}{4}$ LSB this linearity may change maximally by $\pm \frac{1}{4}$ LSB over the full temperature range to maintain monotonicity of the system. A $\pm \frac{1}{2}$ LSB linearity over the full temperature range is obtained in this way, while in binary weighted systems this linearity specification automatically includes *monotonicity* of the converter over the full temperature range.

Suppose we have a variation in temperature of ΔT, then the difference in

thermal tracking for components must not exceed a value of

$$\frac{2^{-n}}{4 \times \Delta T} \quad per \quad degree \quad C. \tag{3.17}$$

Because the most significant bits in a converter must have a high accuracy, the thermal tracking of these bits must be very good. The estimate given in 3.17 is only needed for most significant bit matching. In a 16-bit system subjected to a temperature change of 105^0 C this means that the temperature tracking of components should not exceed 0.04 ppm per degree C. In this analysis it is supposed that the linear (first-order) temperature coefficient is much larger than the second-order term. Sometimes the first order temperature coefficient is reduced by a clever design. At that moment the second order coefficient takes over.

3.5 Dynamic specifications

The most important dynamic specification of a converter is the signal-to-noise ratio. This signal-to-noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise and settling time. Over half the sampling frequency this signal-to-noise ratio must be specified and should ideally follow the theoretical formula: $S/N_{max} = 6.02 \times n + 1.76$ dB. Specifications must be given as a function of frequency with various amplitudes and as a function of amplitude with a constant signal frequency. An even more stringent dynamic performance definition is obtained if the total harmonic distortion (THD) of the converter is added to the quantization error. Even in this case the maximum signal-to-noise ratio of a high-performance converter must be close to the aboven given formula. In Fig. 3.7 and Fig. 3.8 examples of these specifications are shown.

3.5.1 Glitches

Glitches are usually important for the performance specification of D/A converters. A glitch is generated when during a major carry code transition the new code signal value appears before or after the signal value of the former code disappears. The largest glitch is mostly generated by a major carry transition around the MSB-bit level. In Fig. 3.9 a styled glitch is shown. Suppose the full-scale (peak-to-peak) amplitude of the converter equals $2A$, then the MSB value is close to A. Furthermore, the difference in

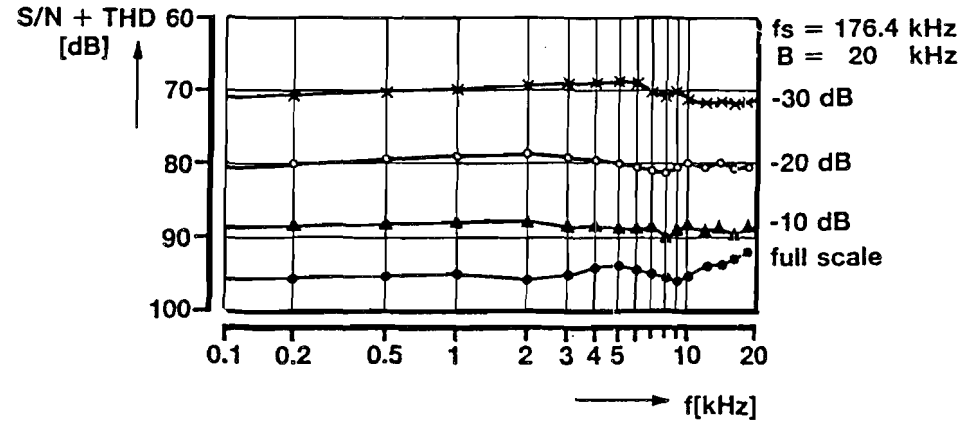

Figure 3.7 : Signal-to-(noise plus distortion) ratio as a function of frequency with various amplitude values

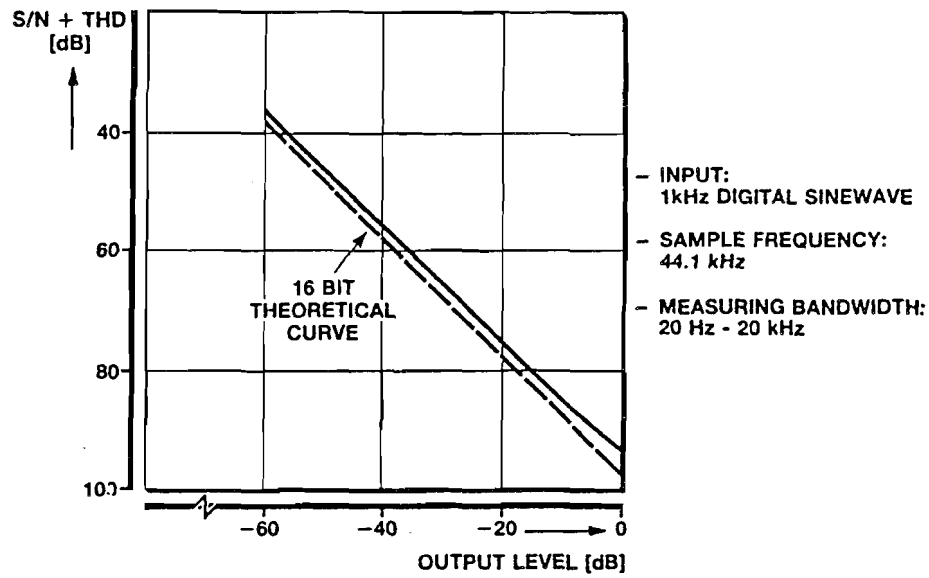

Figure 3.8 : Signal-to-(noise plus distortion) ratio as a function of amplitude

switching time is defined as t_{dif}.
Then the glitch-area error is equal to:

$$E_{glitch} = A \times t_{dif} \quad Vsec \ . \tag{3.18}$$

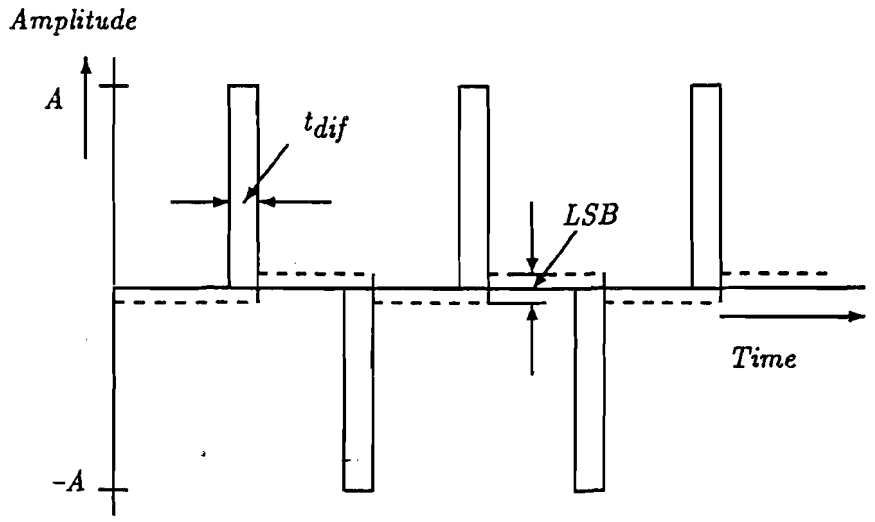

Figure 3.9 : Major carry glitch of a converter

As an example, the glitch error of a 16-bit D/A converter will be calculated compared to the LSB bit value.
Suppose the switching time difference t_{dif} = 1 nsec and the full-scale value of the converter is 1 V, then the glitch error becomes: E_{glitch} = 500 pVsec. The LSB value now equals:

$$E_{LSB} = 2^{-n} \times t_s \quad Vsec. \tag{3.19}$$

With a sample time t_s of 20 μ sec for the converter and n = 16 we obtain: E_{LSB} = 300 pVsec.
The glitch error in this example is about one and a half times larger than the LSB bit value. To qualify this converter as "good", the glitch error must be at least reduced by a factor three. A solution to reduce the glitch error is the addition of a so called "deglitcher" circuit at the output of a D/A converter. However, such a deglitcher circuit uses an analog storage element to maintain the output signal during the code transistion. Such a system is difficult to design, while the performance of such a system is mostly not much better than a well designed D/A converter system. Glitches exhibit in the output signal of a D/A converter as distortion, reduction in signal-to-noise ratio compared to the maximum theoretical value and only a slight improvement in performance when a converter is used in an oversampled mode. An example of a measured MSB-glitch of a 14 bit D/A converter is

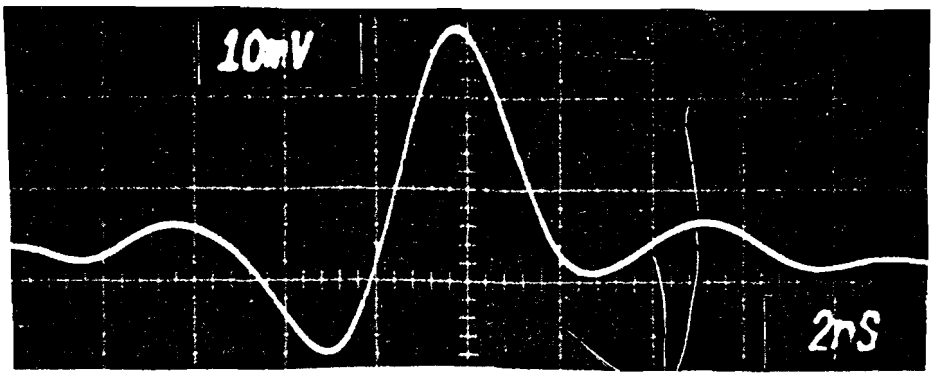

Figure 3.10 : Measured MSB-glitch error

shown in Fig. 3.10. The output signal is measured across a 25 ohm load resistor. The glitch energy becomes even more important in systems which use a large oversampling ratio together with a noise-shaping technique. In such systems an *averaging* of signals occurs. This means that the number of MSB transitions which generate a glitch are increased to more than the minimum number required in generating for example a sine wave. At that moment the amount of glitch energy adds to the output signal. As a result the dynamic range and the distortion of the system do not decrease as much as expected by the theoretical analysis of the system.

3.5.2 Noise

Thermal noise (white noise) of bit-currents, amplifiers, resistors etc. adds to the quantization noise. This thermal noise exhibits itself as a deviation from the theoretical maximum signal-to-noise ratio an ideal converter can have. A simple calculation demonstrates the decrease in signal-to-noise ratio of a system compared to the signal-to-noise ratio of the basic converter in that system. Suppose that the thermal noise in the system is equal to k times the quantization noise of the converter. We then obtain for the signal-to-noise ratio of the system:

$$S/N_{system} = S/N_{quantizer} \times \frac{1}{\sqrt{1+k^2}}. \tag{3.20}$$

In this calculation we suppose that the quantization noise (error) is uncorrelated with the thermal (white) noise. Therefore the thermal noise adds to

the quantization noise in the usual way.
With $k^2 \ll 1$ this can be rewritten as:

$$\frac{1}{\sqrt{1+k^2}} \simeq (1 - \frac{1}{2}k^2). \tag{3.21}$$

Thus:

$$S/N_{system} = S/N_{quantizer}(1 - \frac{1}{2}k^2). \tag{3.22}$$

Inserting for $k = \frac{1}{3}$, then:

$$S/N_{system} = 0.95 \times S/N_{quantizer}. \tag{3.23}$$

This means that in a 16-bit D/A converter system with a theoretical signal-to-noise ratio of 98.1 dB, the thermal signal-to-noise ratio must be at least 108 dB to get an overall signal-to-noise ratio loss in a system of not more than 0.5 dB.
In A/D converters using a successive approximation method for conversion, a much larger comparator bandwidth compared to the signal bandwidth is needed to obtain the same sampling time. It is in this case much more difficult to keep the signal-to-noise ratio in a system low enough. The noise generated in the input circuits causes a "dithering" of the comparator at the transition levels between the successive quantization levels. We also have to add the foldback noise. A rough estimate of the influence of noise on the maximum signal-to-noise ratio of an A/D converter is possible when this converter is operated with an input dc voltage equal to the quantization level. The noise always trips the comparator so a 1 LSB peak-to-peak output code is generated. In Fig. 3.11 the Gaussian distribution curve of noise is shown. Here σ is the rms value of the noise. A code error occurs when the peak-t-peak noise exceeds the 1 LSB threshold. Suppose now that the Gaussian distribution curve lies symmetrically around the $\pm \frac{1}{2}$ LSB decision level. Then $e_{noise} = \frac{1}{2}$ LSB $= \sigma$. Looking at the distribution curve we can say that during 68.2 percent of the time the peak-to-peak quantization error is equal to 1 LSB. During the next 31.5 percent of the time the peak-to-peak error increases to 3 LSBs. The next 0.3 percent of the time the peak-to-peak error increases to 5 LSBs. The input noise trips the different quantization levels with steps equal to 1 LSB.
Subtracting a dc offset from the output code equal to $\frac{1}{2}$ LSB gives an output signal which does not contain dc components. The output noise of the converter can now be estimated with respect to the noise level of a quantization step which is equal to 1 LSB. Adding the quantization noise powers,

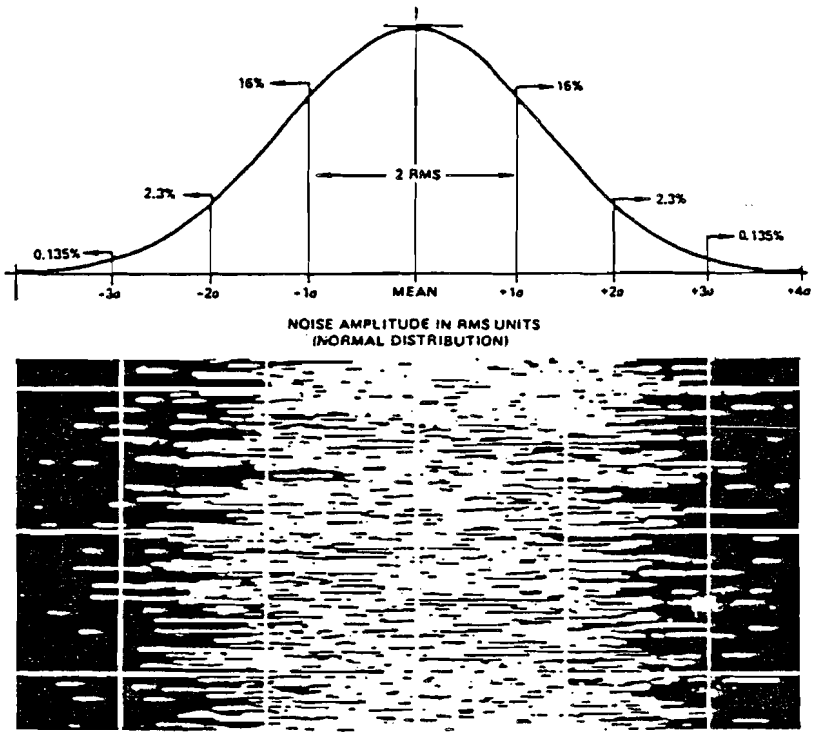

Figure 3.11 : Gaussian distribution curve of noise

we obtain:

$$P_{total} = .682 \times q^2_{qnsLSB} + .315 \times q^2_{qnsLSB+1} + .003 \times q^2_{qnsLSB+2}. \quad (3.24)$$

In this equation q^2_{qnsLSB} represents the quantization noise power of the LSB bit. The quantization error of the LSB + 1 bit is 3 times larger (peak-to-peak) than the quantization error of the LSB bit. Furthermore the quantization error of the LSB + 2 bit is five times larger (peak-to-peak) than the LSB bit. Note again that these errors are peak-to-peak errors. If the next quantization level is tripped by noise, then the peak-to-peak value increases with 2 LSBs.
Inserting these values into formula 3.24 gives:

$$P_{total} = q^2_{qnsLSB} \times 3.59. \quad (3.25)$$

This total power can be converted into a voltage across the same load resistance.

This results in:

$$e_{total} = q_{qnsLSB} \times 1.9. \tag{3.26}$$

The output noise of the system in this way increases by a factor 1.9 or 5.5 dB with respect to the quantization error of the converter. At the moment the dc biasing of the converter is changed so that the decision level is only tripped if the input signal value exceeds $\pm \frac{1}{2}$ LSB, the first term in formula 3.24 disappears. No output code appears in this way because of the hysteresis in the quantizer.
Formula 3.24 now changes into:

$$P_{total} = .315 \times q^2_{qnsLSB+1} + .003 \times q^2_{qnsLSB+2}. \tag{3.27}$$

Inserting values for the two quantization errors as defined above results in:

$$P_{total} = q^2_{qnsLSB} \times 2.91, \tag{3.28}$$

or converted into a voltage this value becomes:

$$e_{total} = q_{qnsLSB} \times 1.7. \tag{3.29}$$

This analysis shows that the output noise changes with changing input dc signal. When in a good converter design the noise generated in the input amplifier and comparator part is reduced, then the changes in output noise with varying input dc signal are much larger. This can be seen if the input noise is reduced from $\sigma = \frac{1}{2}$ LSB to $\frac{1}{4}$ LSB; then the probability for $\sigma = 6$ is so small that the occurrence of quantization errors with a 3 LSB peak-to-peak value is practically zero. At this moment the output noise of the input condition given by equation 3.26 tends to approach the quantization error q_{qnsLSB}, while in the case of the condition given by equation 3.28 the output noise tends to approach zero. In this manner a very good specification of an A/D converter is obtained. In this calculation it is supposed that the noise applied at the input of the A/D converter has a bandwidth which does not exceed half the sampling bandwidth. If the noise bandwidth is much larger than half the sampling frequency then the noise increases by a factor $\sqrt{2 \times \frac{f_b}{f_s}}$. Here f_b is the bandwidth of the input amplifier-comparator stage. The results of formulas 3.26 and 3.28 must be multiplied by this factor.
Designers of high-resolution A/D converters must be aware of this noise phenomenon.

3.5.3 Digital signal feedthrough

Digital signals in most of the converters are TTL-compatible. The disadvantage of the TTL levels in, for example, high-resolution D/A converters is the feedthrough of the TTL logic levels into the analog output current signal. This feedthrough reduces the dynamic range of the converter and introduces harmonic distortion. These distortion phenomena can be explained by supposing that at the output of the D/A converter a sine wave is generated. In a system with offset binary coding the MSB bit changes with the sign of the sine wave. Feedthrough in this case adds to the fundamental frequency, which can result in amplitude changes. The MSB -1 bit, however, changes twice as fast as the output sine wave. Feedthrough in this case adds signals to the output, which results in second harmonic distortion. Identical reasoning can be applied to third- and fourth-order distortion. To avoid this problem a serial coding of the input signal must be used. This serial coding reduces the number of input pins with TTL levels. Furthermore, the frequency spectrum of the input digital signal is far above the working bandwidth of the converter and therefore this spectrum will be removed by the reconstruction low-pass output filter.

3.5.4 Distortion

The signal band of interest is not only present in the frequency spectrum of sampled signals but it is also reproduced around multiples of the sampling frequency f_s, $2f_s$, $3f_s$ etc. If such a signal is applied to a linear amplifier, then due to the finite linearity of such a system intermodulation products are generated. Apart from the harmonic distortion components introduced by the finite linearity of a converter, two dominating intermodulation products for an input signal with a frequency f_{in} can easily be found by mixing the lower band frequency f_s - f_{in} with the upper band frequency $f_s + f_{in}$, resulting in a harmonic distortion $2f_{in}$. When the second harmonic $2(f_s$ - $f_{in})$ of the lower band mixes with the upper band $f_s + f_{in}$ then a non-harmonic product $\mid f_s$ - $3f_{in} \mid$ is obtained. As long as the frequency f_s - $3f_{in} \geq f_b$ only the harmonic distortion $2f_{in}$ is found. Here f_b is the system bandwidth. The minimum sampling frequency at which only harmonic distortion products are found can be calculated. With $f_{in} = f_b$ we obtain $f_s = 4f_b$. In a digital audio system with $f_b = 20$ kHz the lowest sampling frequency to obtain only harmonic products must be at least $f_s = 80$ kHz. However, a lower sampling frequency ($f_s = 44$ kHz) is normally used, so

harmonic and non-harmonic products must be encountered. In Fig. 3.12 a graphical approach to the distortion problem in a D/A converter is shown. From Figure 3.12(b) it can be seen that signals close to half the sampling

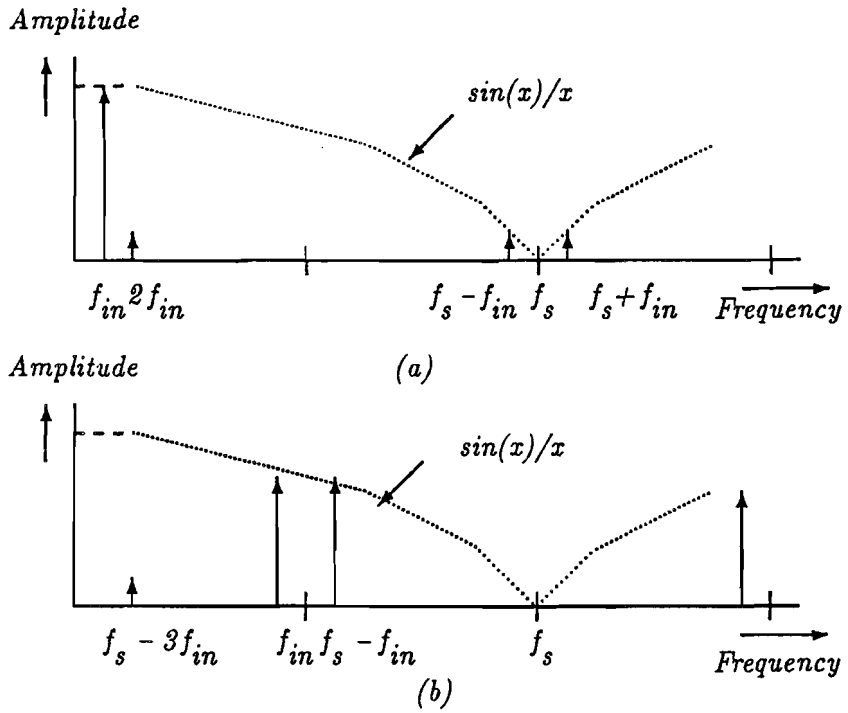

Figure 3.12 : D/A converter distortion model

frequency have a large amplitude "mirrored" signal (f_s - f_{in}). These signals require extreme linearity of the post-amplifier systems to avoid mixing resulting in non-linear distortion products appearing in the baseband. When the "hold" time of the converter is reduced, then the $\frac{\sin x}{x}$ amplitude distortion is reduced. At that moment the amplitude of the high-frequency signal components increases and the linearity requirements of the post amplifier systems must be even more improved. Note that an identical result is obtained for a sample-and-hold amplifier.

3.5.5 Acquisition time

The acquisition time of a system is the time difference between the moment a command is given and the moment the systems responds to this command. At the moment the system responds to the input signal, then the error

between the input signal and the output signal of the system must be within a specified number ususally given in the data sheet. This time is important in for example sample-and-hold amplifiers. In Fig. 3.13 the definition of the acquisition time is shown applied to a sample-and-hold amplifier. The

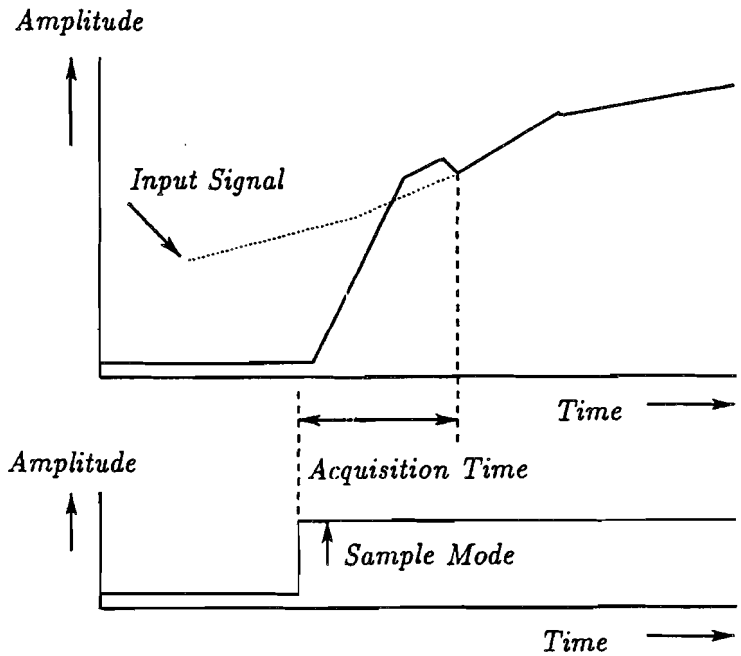

Figure 3.13 : Definition of the acquisition time of a S/H amplifier

acquisition time is defined in this system as the time difference from giving the "track" command until the output signal tracks the input signal. The moment of "tracking" is the time for which the output signal "tracks" the input signal with a well-specified accuracy. The acquisition time is also a measure of the maximum applicable sampling frequency of a sample-and-hold amplifier. After the acquisition time is elapsed the system (sample-and-hold amplifier for example) can be switched into the hold mode.

3.5.6 Aperture time

The aperture time of a sample-and-hold amplifier is specified as the time difference between the "hold" command and the moment the real sample is taken. In a sample-and-hold amplifier and flash-type A/D converters this specification is very important. Differences in aperture time, usually called

aperture time uncertainty, determine one of the major errors in sampled systems (see, for example, chapter 2 "Time jitter").
In sample-and-hold amplifiers the aperture time determines the minimum time required to elapse before the "start conversion" command can be given. Usually an extra time called *hold mode settling time* is needed to be able to specify the exact moment at which the hold output signal is within the specified accuracy. In a flash-type A/D converter the aperture time determines the difference between the sample command and the actual time the analog input signal is sampled and converted into a digital signal. In Fig. 3.14 the definition of the aperture time is shown. A variation of the time differ-

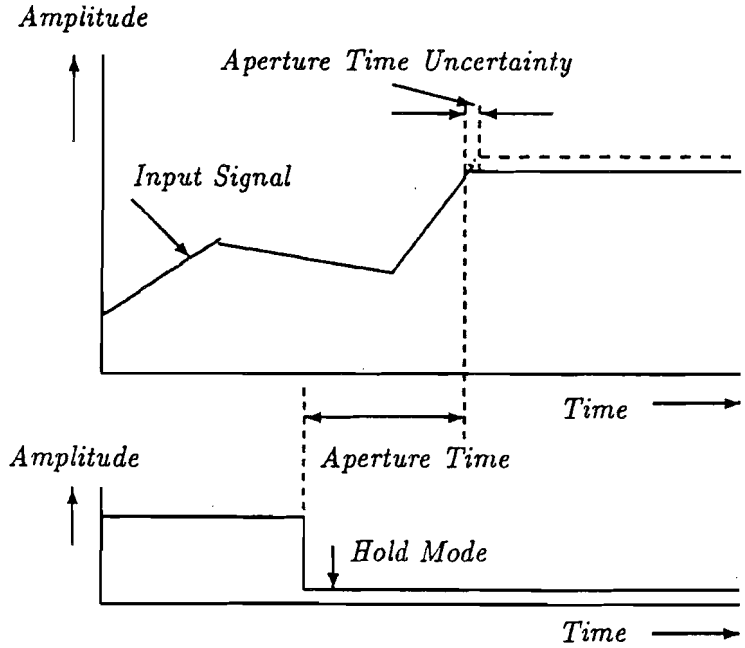

Figure 3.14 : Definition of aperture time

ence between the "hold" command and the "start conversion" command in an A/D conversion system can result in fractional changes of the signal-to-noise ratio. Depending on the type of A/D converter, the start conversion command can be given before the final settling of the hold amplifier. As a result, a fractional change in maximum accuracy of the sample-and-hold amplifier is found. This accuracy variation gives rise to small changes in the maximum the signal-to-noise ratio of a system. An optimum signal-to-noise ratio is mostly obtained when the time difference between the sample com-

mand and the start conversion command is more than the minimum time required according to the specification sheet. The hold mode settling time must be added.

3.5.7 Sample-to-hold step

The sample-to-hold step is a change of the analog output signal in a sample-and-hold amplifier at the moment the circuit changes state from the sample to the hold mode. Due to the charge feedthrough in the switch an extra amount of charge which is not a measure of the analog input signal is added to the hold signal. This *hold* step introduces an error. When the *hold* step is independent of the signal level no non-linear distortion is introduced and the hold step can be seen as an extra dc offset. Sometimes a control signal can be applied to the sample-and-hold amplifier to zero the hold step. Basically, designs can be made which minimize the sample-to-hold step and make this step independent of the input signal level. (see chapter 8 for a detailed description of a sample-and-hold amplifier). In Fig. 3.15 the sample-to-hold step of a sample-and-hold amplifier is shown.

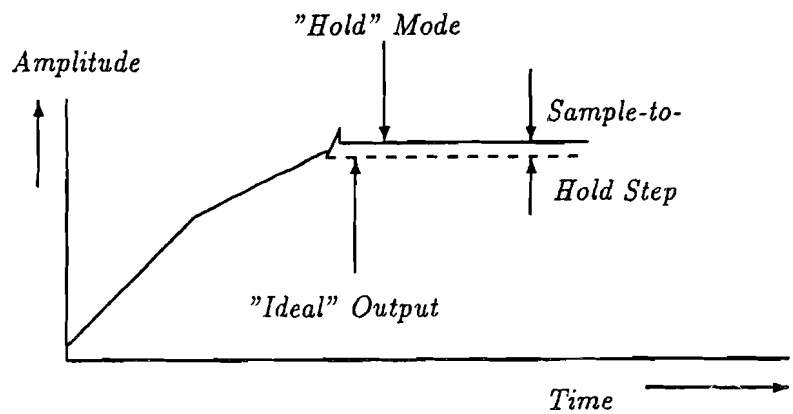

Figure 3.15 : Sample-to-hold step

3.5.8 Analog system bandwidth

In high-speed A/D converter systems the analog bandwidth at full input signal must be defined. In ideal converter systems the maximum analog bandwidth is equal to half the sampling bandwidth. In practice, however, there are various reasons why this theoretical value is not obtained. In

chapter five a number of reasons will be given and explained. Therefore it is necessary to give a good specification for the analog signal bandwidth of a converter.
A very precise specification of this analog bandwidth is found by specifying the maximum analog frequency for which the signal-to-noise ratio of the system decreases by 3 dB or $\frac{1}{2}$ LSB with respect to the theoretical value of the system.
By definition the bandwidth obtained in this way is called *Effective Resolution Bandwidth* (*ERB*).
During the determination of the effective resolution bandwidth of a system a fixed sampling frequency is used. This sampling frequency is usually more than two times the analog effective bandwidth.
In Figure 3.16 the results of a resolution bandwidth measurement are shown. The 3 dB decrease in signal-to-noise ratio of the system is used to define the (full-signal) analog bandwidth of the system. The effective resolution band-

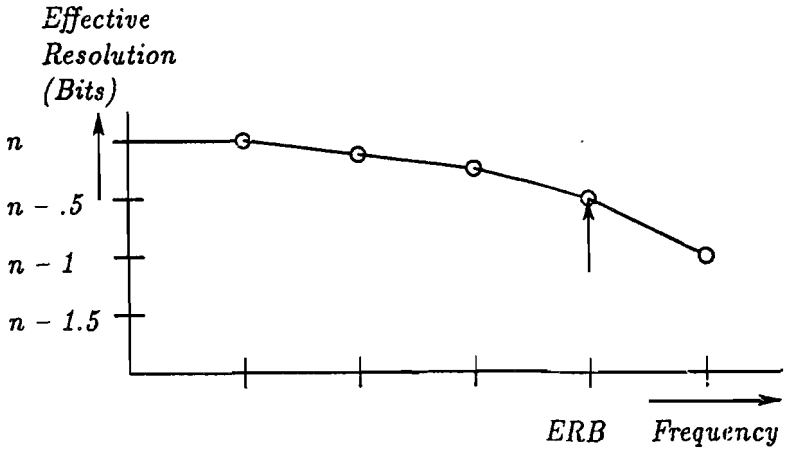

Figure 3.16 : Effective resolution bandwidth of a converter

width must be measured at full scale to include time jitter and linear and non-linear distortion products.

3.6 Conclusion

In this chapter the basic requirements for A/D and D/A converters are defined. These definitions lead to basic circuit design constraints which must be fulfilled to obtain high-performance converters. In a binary-weighted converter the $\pm \frac{1}{2}$ LSB linearity specification is the only necessary specification

to guarantee *monotonicity*.
In high-resolution binary weighted converters the linearity requirement implies a very high accuracy of the most significant bit weights to obtain a monotonic converter. Signal-to-noise and signal-to-(noise plus distortion) specifications give a quick and reliable qualification of a converter. It includes noise, glitch error, sampling time uncertainty and distortion. These dynamic specifications are very important in digital-signal-processing systems such as, for example, digital audio and digital video systems.
The glitch energy is an important measure for the application of a D/A converter in an oversampled and noise-shaped system. Due to the increase in number of *zero crossings* introduced by the noise-shaping operation the distortion might increase or the dynamic range does not decrease according to the theoretically expected values. A low glitch design is needed in this case. In chapter 10 the noise-shaping techniques will be explained.

Chapter 4

Testing of D/A and A/D converters

4.1 Introduction

To verify the different specifications of converters and converter systems it is important to set up test facilities and structures and to agree unanimously on the test procedures. In general, static performance tests can be performed by using digital voltmeters which can be a part of an Automatic Test Equipment (ATE). Dynamic tests, especially in the case of high-dynamic-range tests, require special equipment. Furthermore, these dynamic tests are generally more difficult to standardize and consume more test time. (see [15,16]). Up till now dynamic test results have been listed very briefly in specification sheets. In this chapter we will determine test configurations and test procedures in order toarrive at a unanimous qualification of data converters.

4.2 DC testing of D/A converters

DC specifications are obtained by applying a digital signal source to the input of the D/A converter. This digital source can be a personal computer (PC) or a specially developed device. In Fig. 4.1 a test set-up for DC measurements is shown. At the output an IEEE bus programmable digital voltmeter (part of ATE) is connected. The measured data can be applied to the personal computer to process this data. How the measured data is processed depends on the configuration of the test system. Zero offset, full-scale accuracy and

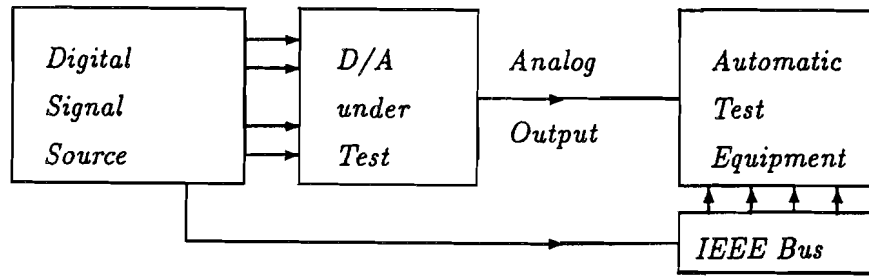

Figure 4.1 : DC measurement test set-up

integral non-linearity can be measured. It is clear that the accuracy of the digital voltmeter must be much higher than the accuracy of the converter under test. In a binary-coded converter the individual bit weights can be measured. Using the equations from 3.6 and 3.10 shown in chapter 3 it is possible to calculate the measured non-linearity of the converter. The non-linearity of a converter is defined as the deviations from a straight line drawn through zero and full scale. In Fig. 4.2 these deviations from a straight line through zero and full scale for the bit weights in a binary-weighted converter are shown. Full scale error and zero error (offset) are trimmed to zero to obtain a straight line between zero and full scale according to the linearity specification. The errors of the individual bit-weights are shown starting with the MSB error at the left side of the figure to the LSB error at the right side of the figure. The total positive and negative error is shown at the most right side of the figure as $\sum error$. This converter has a total non-linearity error of $\pm \frac{1}{4}$ LSB. In a *monotonic by design* type of converter construction

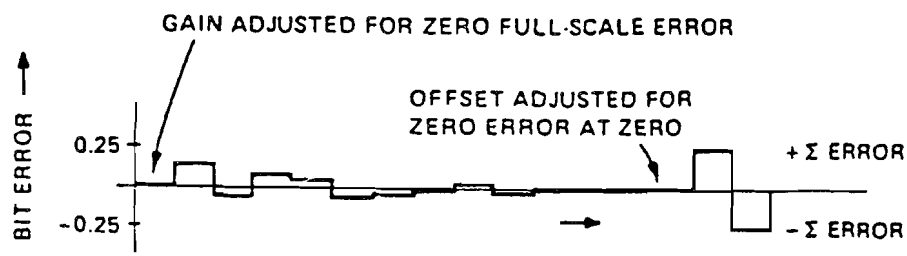

Figure 4.2 : Bit-weight error of a binary-weighted converter

every code must be measured and deviations from the straight line through zero and full scale determined. Testing these *monotonic by design* types is more difficult and requires therefore much more test time. Furthermore,

the converter construction determines how many data points are needed to verify the linearity specification. A resistor string having as many taps as the number of digital codes which can be applied shows a good example of a *monotonic by design* type of D/A converter. From this example it is easily understood that all converter codes must be tested to guarantee a linearity specification. Sometimes it is possible to reduce the amount of test samples to be taken for the linearity specificication when the converter construction is accurately known. Use can then be made of a certain repetitive character which is mostly found in these types of converters. Mostly linearity is determined by the linearity of a number of the most signficant bits. The remaining information interpolates between the values of the most significant bits resulting in the repetitive character. .

4.2.1 Temperature relations

To obtain information about the temperature dependence of DC specifications the offset, full-scale accuracy and integral non-linearity test must be performed at different temperatures. Temperature dependence can then be calculated and specified.

4.2.2 Supply voltage dependence

Information about supply voltage dependence is obtained by performing offset, full-scale and linearity measurements at the minimum, nominal and maximum supply voltage specifications of the converter. Mostly information about the supply voltage sensitivity as a function of frequency is added to these specifications. At frequencies around the digital input frequency the supply rejection ratio must be relatively high to reject noise generated by the digital circuitry which surrounds the converter. When these measurements are performed at different temperatures a full specification is obtained.

4.2.3 Bit weight noise

By applying input codes which switch on the individual bit weights of a binary weighted D/A converter, the noise superimposed on these bit weights can be measured. The value of the total noise of all the bit weights is sometimes specified as the maximum noise of the system. However, it is important to know the bit weight noise values they do not define the dynamic performance (signal-to-noise) of the system. Mostly the noise of the bit weights is well below the total quantization noise value determined by the

signal-to-noise ratio of the system. When in some cases bit weights show a high value, then these bit weights contribute too much to the total system noise.

4.3 Dynamic testing of D/A converters

By using a digital programmable sine wave source at the input of a D/A converter dynamic tests can be performed. A digital sine wave generator applies a practically ideal sine wave to the D/A converter. When an A/D converter with an analog sine wave generator is used at the input of the D/A converter, then the performance of the A/D converter system influences the accuracy of the measurements. In Fig. 4.3 a test set-up is shown. A low-pass

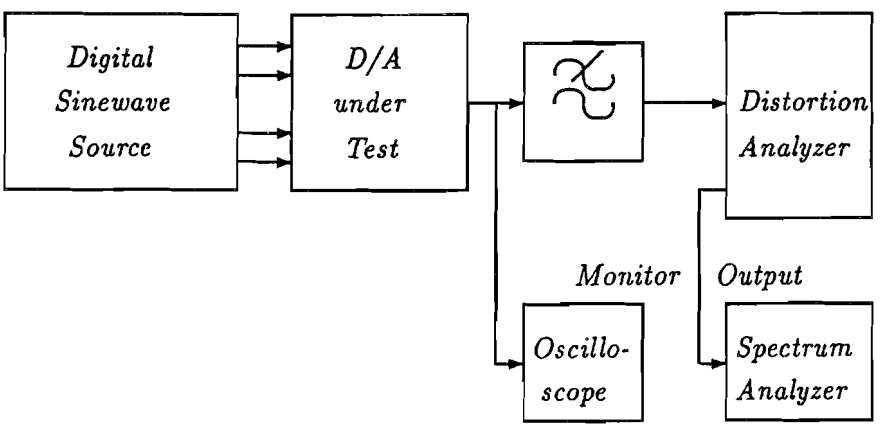

Figure 4.3 : Dynamic test set-up

filter applies the baseband to the analog distortion analyzer. Usually such a distortion analyzer is equiped with a monitor output, which contains all the signal information except the fundamental signal. This monitor output signal can be analyzed using a spectrum analyzer. Information about distortion and spectrum of the error signal is obtained in this way. The test set-up is extended with an oscilloscope to analyze the high-speed analog output of the converter. The glitch error can be measured by adjusting the input signal at a *major carry* transition in a binary-weighted converter. With a distortion analyzer the signal-to-noise ratio is measured over a bandwidth equal to the low-pass filter bandwidth. The monitor output of the distortion analyzer is monitored with a spectrum analyzer to obtain information about the spectrum of the quantization error and distortion of the output signal of

the converter.

4.3.1 Dynamic integral non-linearity test

By measuring the signal-to-noise ratio with a full-scale sine wave at the input and over the full input signal bandwidth information about the dynamic linearity is obtained. In a very well-designed converter the signal-to-noise ratio must be close to the theoretical value given by:

$$S/N = n \times 6.02 + 1.76 \text{ dB}. \tag{4.1}$$

This measurement includes sampling time uncertainty, glitches and integral non-linearity. Additional information about the linearity of the converter is obtained when at a constant frequency the singla-to-noise measurement is performed as a function of the signal amplitude. Usually close to the maximum signal amplitude small deviations from the ideal (theoretical) value are found. When close to maximum signal level large deviations are found, then these deviations may be introduced by a large distortion. Therefore it is important to analyse the quantization error signal as a function of frequency with a spectrum ananlyzer. If no large distortion components are found, then the clock stability must be determined. Using a spectrum ananlyser, the noise level of the clock signal source can be measured. The best information about the noise level of an oscillator is found at $f_m \approx 0$ or $f_m \approx 2f_{osc}$. Determining the signal-to-noise ratio of the clock signal under these conditions must give a high value. Comparing the results obtained with a crystal oscillator must give small deviations in case a high resolution or high-speed system is measured. At this moment no valuable relation exists between the maximum signal-to-noise ratio a converter system can have and the noise performance of the clock signal.

4.3.2 Differential non-linearity

Dynamic differential non-linearity is measured by applying a very low frequency signal of e.g. 0.01 Hz superimposed with a 2- to 3- LSBs-sized signal with a higher frequency eg. 400 Hz. The amplitude of the 0.01 Hz signal is close to the full-scale value of the converter. In this way all the levels in the converter pass by. The variations of the 400 Hz output signal is a measure of the differential non-linearity of the converter. This measurement can be performed in a short time. A maximum variation of 2 LSBs peak-to-peak is allowed for a binary-weighted converter with an integral non-linearity of $\pm \frac{1}{2}$ LSB.

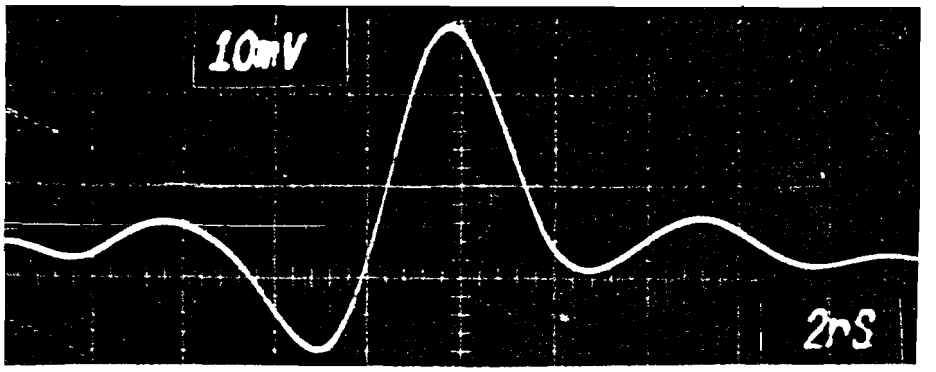

Figure 4.4 : Major carry glitch measurement result

4.3.3 Glitches

Using the oscilloscope the glitch energy can be measured. At the input of a binary weighted converter a code giving a major carry transition must be applied. Usually the largest glitches occur at the major carry transitions. In Fig. 4.4 the result of a major carry glitch measurement is shown. The output glitch of a current type D/A converter is measured across a 25 ohm load resistor. By measuring the total energy and comparing this glitch energy with the LSB energy, it is possible to determine the influence of glitches on the total transfer function of a D/A converter. Especially in oversampled offset-binary-coded D/A converter systems a low glitch energy is very important. In these applications a larger resolution than the basic converter is obtained by using oversampling. When the glitch error cannot be ignored with respect to the LSB size of the emulated higher resolution converter, then this oversampling is mostly paid-off with a larger distortion. In offset-binary-coded converter systems this problem is encountered when small output signals are reproduced around zero. The addition of a deglitcher circuit can improve the performance of the system. However, such a deglitcher circuit is a critical stage in the D/A conversion process too.

4.3.4 Distortion measurement

The distortion of a converter system can be measured by applying an appropriate full scale input test signal. In non-oversampled D/A converters the largest distortion mostly occurs at the high-frequency end of the frequency band. This distortion results from the finite slew rate of output

amplifiers. In these amplifiers, the input signal mixes with the sampling frequency, resulting in non-harmonic distortion products. By analyzing the monitor signal of a distortion analyzer with a spectrum analyzer it is easy to see if this phenomenon occurs. In oversampled converters distortion must be measured at the low-frequency band edge. Non-linear distortion occurs here because of the final accuracy of the converter. This final accuracy results in harmonics of the signal frequency as long as these harmonics are within the passband of the system. The oversampling operation transforms the frequency spectra at a much higher frequency. Therefore it is less probable that non-harmonic mixing products appear in the baseband of the system. Harmonics, of the input signal are rejected by the reconstruction low-pass filter for signals above 10 kHz in an audio converter.

4.3.5 Settling time measurement

A dynamic measurement of the settling time of a converter is possible by measuring the signal-to-noise ratio over a fixed bandwidth and with a fixed measuring frequency. By varying the sampling frequency, the signal-to-noise ratio should increase linearly with the square root of the sampling frequency. At the point when there is no increase in signal-to-noise ratio the settling time of the converter has been reached. To obtain an accurate measurement of this condition a small glitch error is required. Adding a deglitcher, however, can overcome this glitch problem.
Direct measurement of settling time is also possible by applying a special test circuit. In Fig. 4.5 this test set-up is shown. The output signal of the D/A converter is applied to a high-speed Schottky-clamped (D_1, D_2) operational amplifier (OA) which performs a current-to-voltage conversion in this current D/A converter system. Furthermore, a current I_{comp} is subtracted from the output current of the D/A converter. This compensation current determines the current value at which the direct settling time measurement must be performed. Schottky clamping is used to prevent overloading of the oscilloscope. The measurement is performed by switching the D/A digital input value from zero or full scale to the desired current setting. With the oscilloscope the boundary within which the output signal must settle is determined. In this way a direct measurement is obtained. However, the settling time of the operational amplifier and the Schottky-clamped circuit must be much smaller than the values to be measured. Therefore a careful layout and a good choice of devices are needed.

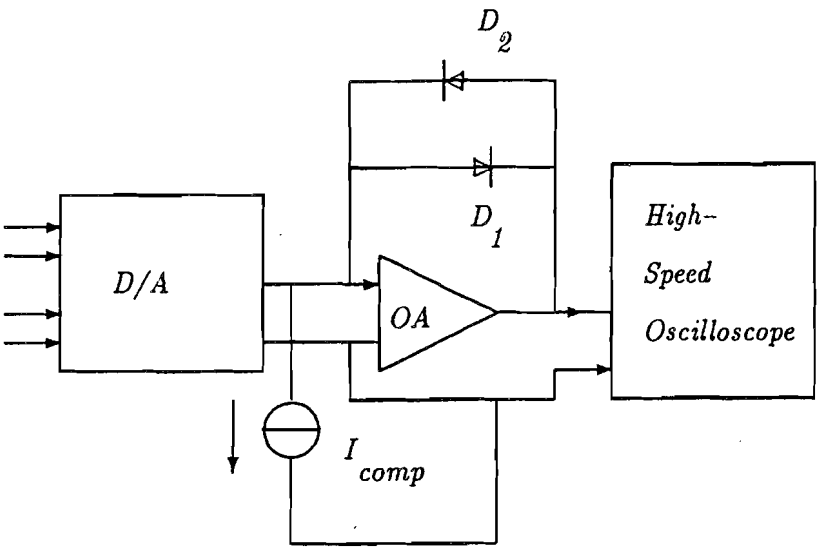

Figure 4.5 : Direct settling time measurement set-up

4.4 DC testing of A/D converters

In Fig. 4.6 a dc test set-up is shown. If dc tests are performed the sample-and-hold function does not need to precede the converter. An accuracy-limiting circuit can be avoided in this way. The set-up consists of a programmable high-accuracy dc voltage source, a logic analyzer and a controller. The output of the A/D converter can be analyzed using a logic analyzer. If a D/A converter with a much higher accuracy than the A/D converter is connected at the output of the A/D then it is advantageous to connect the output data of the A/D to the D/A converter in such a way that an opposite polarity of the output signal compared to the input signal is obtained. By connecting two resistors R_1 and R_2 in a bridge circuit between input and output of the system, the linearity can be measured by monitoring the signal at the connection marked $V_{difference}$ between the resistors R_1 and R_2 with reference to zero (testpoint P). Scale errors can be calibrated by changing the value of one of the two resistors in such a way that only differences appear at the node. By programming the analog input source, offset and full-scale errors can be monitored with a logic analyzer. Differential and integral linearity measurements are performed by slowly varying the analog input signal from zero to full scale. By connecting an X,Y plotter at the same terminals $V_{difference}$ as shown in Fig. 4.6 a hard copy can be made of differential and

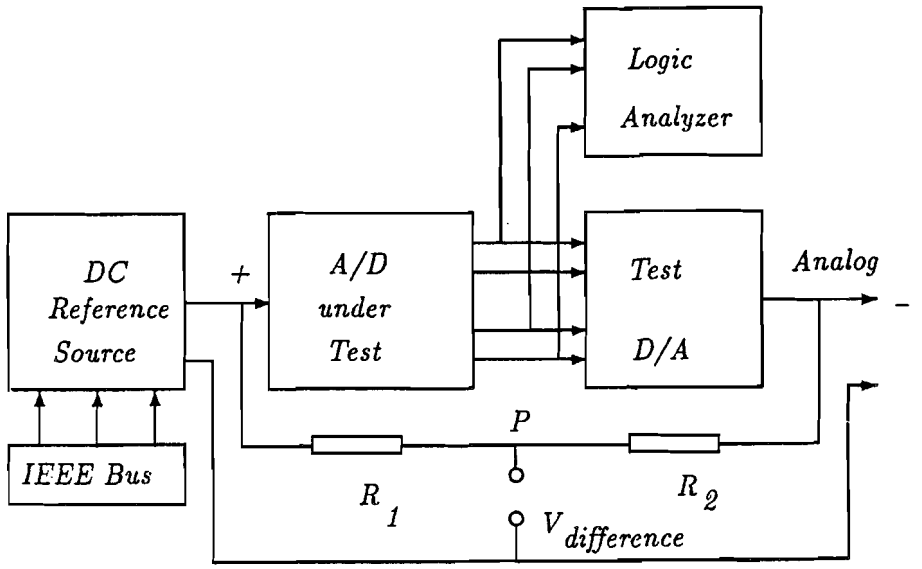

Figure 4.6 : DC test set-up for A/D converters

integral non-linearity of the converter. The difference between every quantization level shows the differential non-linearity. The deviation of $V_{difference}$ from zero gives the integral non-linearity. All steps are verified with this measurement. In Fig. 4.7 a measurement result of such a test is shown. These measurements can be performed over a large temperature range and with varying supply voltages. In this way the temperature variations of linearity and supply voltage dependence on offset, full-scale value and linearity can be determined.

4.5 Dynamic testing of A/D converters

In Fig. 4.8 a test set-up for dynamic performance tests of A/D converters is shown. When dynamic tests are performed a sample-and-hold amplifier must in most cases be added to the input circuitry of the A/D converter to sample the analog input signal. This sample-and-hold amplifier must have a much better performance than the A/D converter to be tested. The sample-and-hold amplifier samples the input signal and keeps this signal constant during the time the A/D conversion takes place. At the input of the test set-up a low-distortion sine wave source is applied. Moreover a low-pass input filter is used to filter out possible high-frequency interference and noise signals which

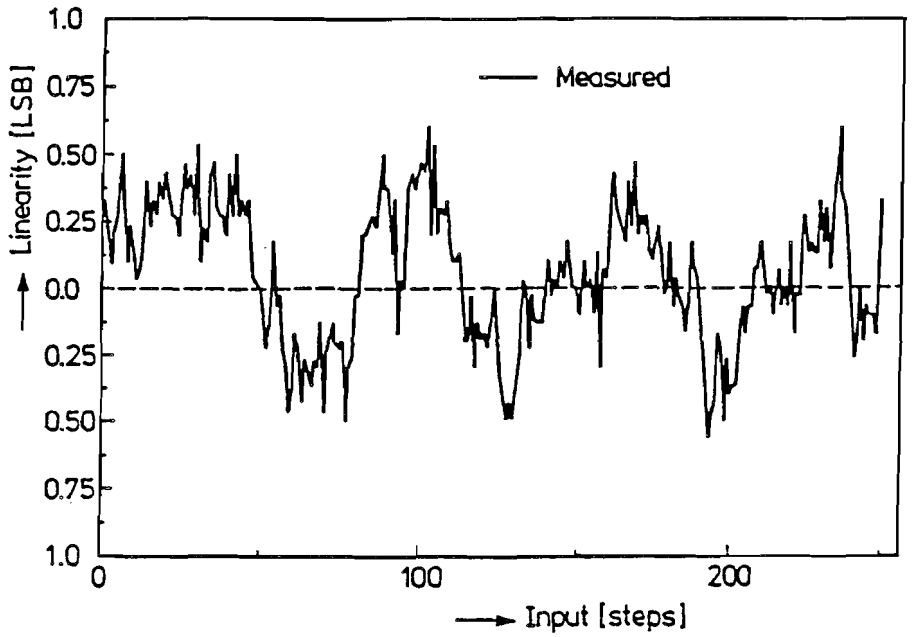

Figure 4.7 : Linearity measurement result

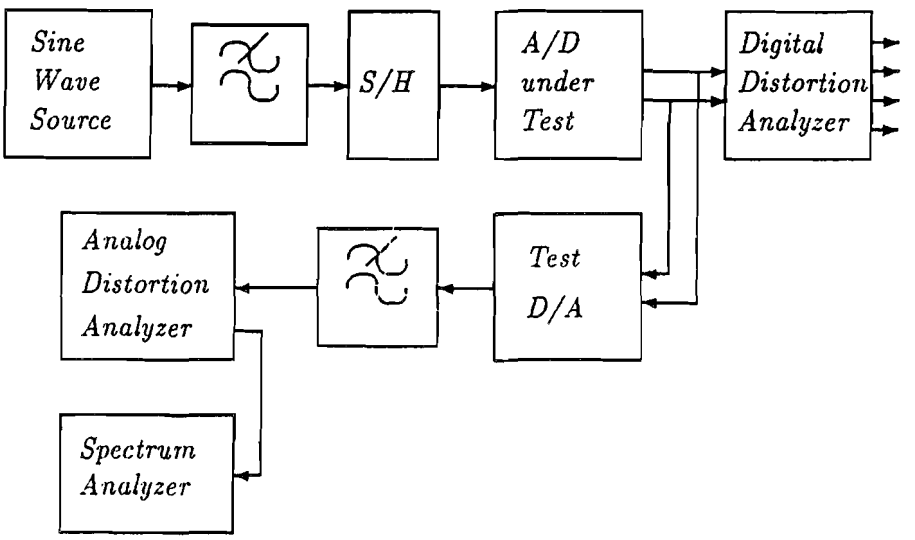

Figure 4.8 : Dynamic test set-up for A/D converters

may be present on the output signal of the sinewave generator. Digital data can be analyzed using a specially built digital distortion analyzer. If such

an instrument is not available, then a high-accuracy D/A converter can be used to convert the digital data into analog signals again. This analog signal is filtered by the reconstruction filter and then analyzed using a distortion analyzer. In most cases distortion analyzers have a monitor output showing the error signal after the fundamental has been removed. This monitor signal can be analyzed with a spectrum analyzer to obtain information about harmonics and glitches. On the other hand, the converted digital signals can be analyzed by using a fast Fourier transform. In such a case enough samples must be taken to obtain accurate information about the signal to be analyzed. Furthermore, the limited number of samples which can be analyzed calls for a completely random choice of input signal frequency with respect to the sampling frequency. To minimize the problems with "leakage" in the Fast Fourier Transform a window function can be applied. It is important to let the ratio between sampling frequency and input frequency be a prime number. In that case the quantization errors are randomized so a correct measurement and interpretation of the results is possible. Signal-to-noise measurements as a function of frequency and amplitude must be performed to characterize the A/D converter.
By measuring at a high sample frequency the signal-to-noise ratio of a system, the *effective resolution bandwidth* can be determined. This bandwidth is the maximum analog input frequency for which the resolution (signal-to-noise ratio) of the system decreased with $\frac{1}{2}$ LSB compared to the low-frequency result. During this measurement it must be noted that the low-frequency signal-to-noise ratio does not deviate more than $\frac{1}{8}$ LSB from the theoretical value.

4.5.1 Conversion speed

The conversion speed of an A/D converter can be measured by varying the conversion time of the converter and keeping the sampling time and input signal conditions constant. Particularly at high input signal frequencies the measurement is sensitive to conversion speed variations because of the small amount of samples per period of input signal. Additional quantization errors introduced by the A/D converter reduce the signal-to-noise ratio, while mixing of the input signal with the sampling frequency can also result in non-harmonic distortion. In Fig. 4.9 the result of such a measurement is shown. When a long conversion time is used the optimum signal-to-noise ratio of such a system is found.

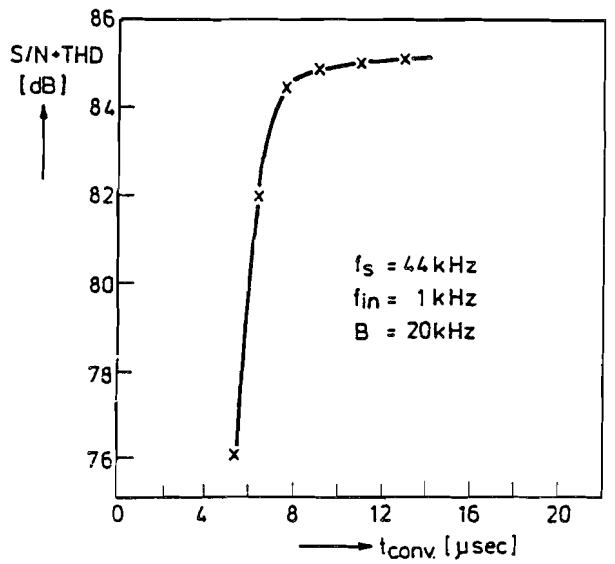

Figure 4.9 : Conversion speed measurement result

A definition of the minimum conversion time of an A/D converter can be specified as: the minimum conversion time for which the signal-to-noise ratio is reduced by 1 dB compared to the optimum long conversion time value.

A 1 dB signal-to-noise reduction is not seen as a disturbing loss. This specification introduces a clear definition of the minimum conversion time of a converter.

4.6 Testing very high-speed A/D converters

Testing very high-speed A/D converters is a different subject. A digital distortion analyzer is difficult to build because of the high sampling rates of these converters. As a result, an A/D -D/A converter loop is the preferred test environment. The test configuration and the test boards which contain the different system elements must be optimized for the best dynamic performance. The influence of small changes in the test board (e.g. wiring) can immediately be analyzed with a spectrum analyzer and an oscilloscope. However, D/A converters which show the required linearity and low glitch error at these speeds are difficult to obtain. Both A/D and D/A converters usually operate at the limit of a technology used to build the devices. Sub-

sampling of output signals of the A/D converter is therefore applied. At the lower subsampling rates D/A converters with a much better linearity and glitch error specification are available. In this manner the question about errors introduced by the D/A converter can be postponed. In Fig. 4.10 a test set-up using a subsampling technique is shown. From figure 4.10 it can

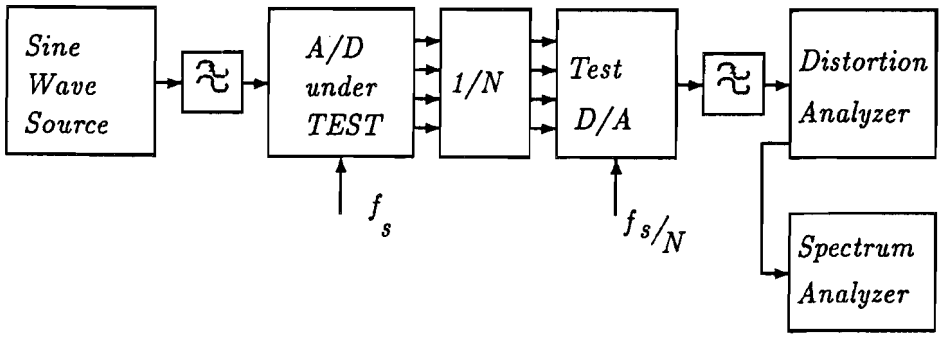

Figure 4.10 : Very high-speed A/D converter test set-up using subsampling

be seen that the output samples of the A/D converter are reduced by a factor N before they are applied to the D/A converter. The maximum amount of reduction in samples N depends on the speed of the D/A converter used in the test,set-up. Moreover, during measurements the subsampling rate N can be optimized to get the best performance of the D/A converter over a large sampling frequency range.
Subsampling of signals is allowed but the signals, quantization errors and distortion are folded back into the baseband. It is already known that a reduction in sampling rate by a factor N increases the quantization noise folded back into the baseband by a factor equal to $\sqrt{N}$. At the same time the measurement bandwidth is reduced by a factor N. As a result of this operation the signal-to-noise ratio of the system does not change. In Fig. 4.11 the subsampling operation is shown. In 4.11 the subsampling operation with a four times subsampling factor is shown. Subsampling with a factor two results in a "mirroring" of frequencies between $3\frac{1}{2}\ f_s$ and $4f_s$ around the subsampling frequency $2f_s$ into the baseband from zero to $\frac{1}{2}\ f_s$. Identical operations are obtained for subsampling with a factor two at f_s and $\frac{1}{2}$ f_s respectively. As a result of this operation the quantization noise density is increased by a factor four as long as no filtering operation is performed before the subsampling takes place. Higher subsampling rates than two can be successfully applied to an A/D - D/A system to obtain accurate informa-

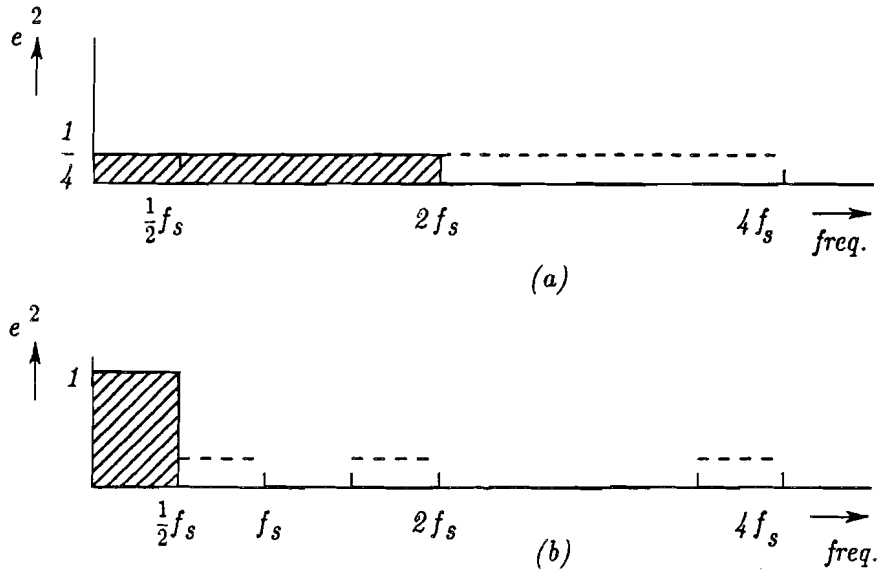

Figure 4.11 : Subsampling in converter systems

tion about distortion and signal-to-noise ratio. The D/A converter in such a system can be repeatedly used over the same sampling frequency by changing the subsampling factor N depending on the sampling frequency range of the A/D converter. The *effective resolution bandwidth* of the system can be determined with this test method.

From the measurements on for example high-speed A/D converters which do not use a sample-and-hold amplifier at the input a dominating third order signal distortion is found. This third order distortion is a measure for the maximum bandwidth of the input circuitry of the converter under test. In chapter 6 a theoretical analysis of this phenomenon will be given. The increase in third order distortion determines the ERB when signal-to-noise plus distortion is measured as a function of frequency. In Fig. 4.12 the result of a distortion measurement as a function of input frequency is shown. This result is measured on an A/D converter which does not need a sample-and-hold amplifier.

With a logic analyzer it is possible to measure a large amount of samples. These samples can be stored in the internal memory of the analyzer and then transferred to a computer system to calculate the spectral response. Care must be taken that there exists no correlation between the input signal frequency and the sampling frequency in the converter. In that way the quantization errors are randomized and a correct result is obtained. Care

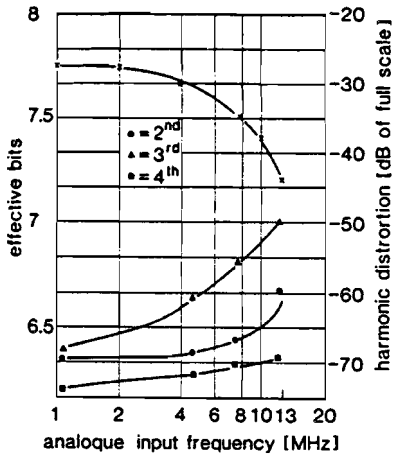

Figure 4.12 : High-speed A/D converter distrotion measurement result

must be taken to avoid "leakage" in the Fast Fourier Transform by using an appropriate window function.

4.7 Beat frequency test configuration

A quick method to obtain information about the high-frequency performance of a converter can be obtained when the input frequency and the sample frequency differ only by a small amount. A low-frequency beat frequency is obtained. In Fig. 4.13 an example of a beat frequency signal is shown. This

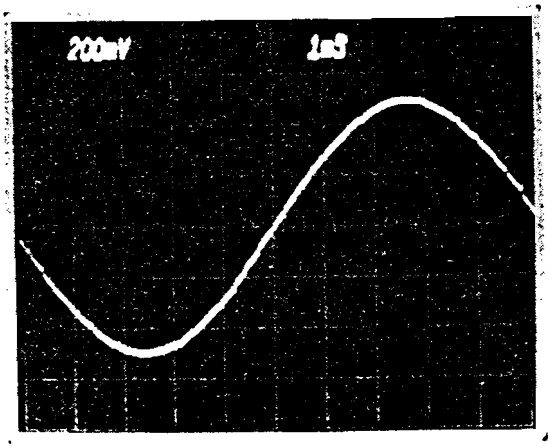

Figure 4.13 : Beat frequency output signal

beat frequency signal can be analyzed. The distortion of the beat frequency can be measured and the result is an indication of the linearity and missing code performance of the system at these frequencies. Note that in this test condition the sample frequency cannot be much higher than the maximum analog input frequency. In this case a D/A converter with good specifications over the total analog input signal bandwidth is required. Glitches must be small compared to the LSB bit value to avoid measurement errors.

4.8 Testing of sample-and-hold amplifiers

In Fig. 4.14 a test set-up for measuring the performance of a sample-and-hold amplifier is shown. A floating digital voltmeter is used to measure the

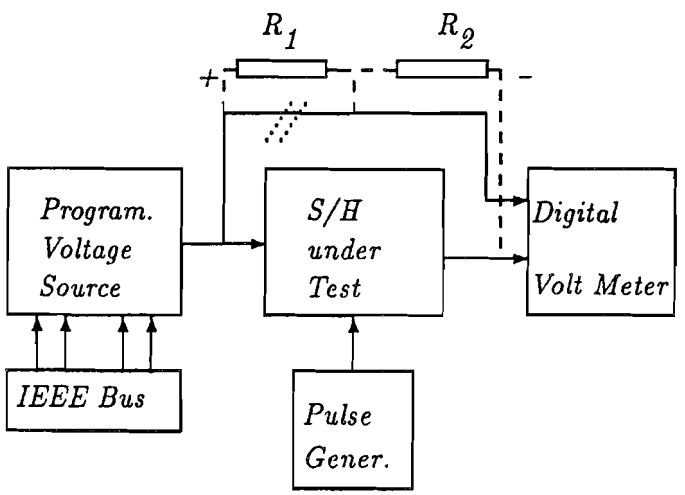

Figure 4.14 : Test set-up for measuring S/H amplifiers

difference between input and output signal of the sample-and-hold amplifier if the circuit performs a non-inverting transfer operation.
When an inverting sample-and-hold amplifier is tested, the configuration shown in dashed lines can be used. In this way a more accurate testing of the linearity is possible by connecting the digital voltmeter at the interconnection of the resistors R_1 and R_2 and the signal reference (not shown in the figure).

4.8.1 Testing DC characteristics

During the *track* mode DC offset and non-linearity can be measured. If an inverting type of sample-and-hold is tested, then the resistor bridge may be used to measure non-linearity. In a non-inverting system a floating measurement instrument must be used to measure the difference between input and output signal as a function of the input signal. Information about non-linearity is obtained in this way. The "track-to-hold step" of a sample-and-hold amplifier is measured by monitoring the difference between the DC input signal during the *track* mode and the signal during the *hold* mode. The temperature dependence of all these parameters is obtained by performing the above-defined measurements at different temperatures.

4.8.2 Dynamic measurements

In Fig. 4.15 a dynamic performance test set-up is shown. The acquisition time of a sample-and-hold amplifier is the time needed to switch from the hold mode into a full-accuracy following (tracking) of the analog input signal. The acquisition time of the system is measured by varying, at a fixed sampling frequency, the track-and-hold time. A small acquisition time is a measure of the performance of a sample-and-hold amplifier. It determines the maximum sample frequency of the sample-and-hold amplifier. The signal-to-noise ratio of a system is measured as a function of the acquisition time. In Fig. 4.16 a test result is shown.

The minimum acquisition time is determined at a point where the signal-to-noise of the system is reduced by 1 dB with respect to a measurement value obtained with a large acquisition time.

The aperture time of a sample-and-hold amplifier is the time difference between the start of the *hold* command and the moment the output signal of the *hold amplifier* is settled within the specified accuracy of the amplifier. The aperture or *track to hold* time is measured by varying the delay time T_d between the hold command, applied to the sample-and-hold amplifier, and the start conversion command, applied to the A/D converter.

During the *track mode* the distortion of the sample-and-hold amplifier is measured. This measurement includes the distortion of the *hold amplifier* too.

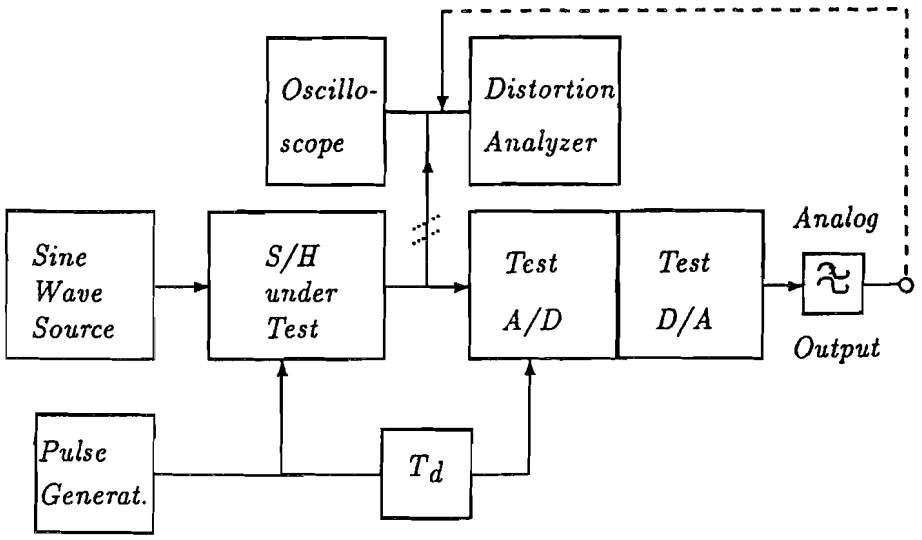

Figure 4.15 : Dynamic test set-up for sample-and-hold amplifiers

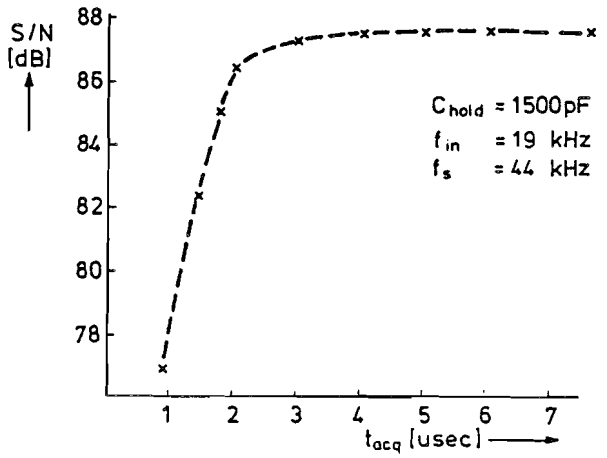

Figure 4.16 : Acquisition time measurement result

A very important parameter is the *aperture uncertainty* time of a sample-and-hold amplifier. This aperture uncertainty determines the timing accuracy with which analog samples are taken. Especially at high analog input frequencies this parameter determines the performance of a system i.e. signal-to-noise ratio. This *aperture uncertainty* of a sample-and-hold amplifier is difficult to measure. With a large acquisition time the signal-to-

noise ratio of the total system is analyzed and results close to the theoretical value must be obtained. If large differences occur, then the clock jitter has to be reduced and the clock generation circuits be improved. Without special measures it is not possible to analyze the sample-and-hold amplifier on itself. Usually a "glitch" is generated when the system switches from *track* to *hold* mode. Therefore it is not possible to analyze the sampled *analog* signal at the output by simply filtering off the harmonics introduced by the sampling process by using a low-pass filter and analyzing the resulting signal with a distortion analyzer and a spectrum analyzer.
The small signal bandwidth of the system must be measured to obtain information about the noise bandwidth. Noise tests are performed by analyzing the output noise of the system during the track mode as a function of the DC input signal. The frequency spectrum of the output noise must be analyzed up to very high frequencies to obtain information about the foldback noise which is finally added to the sampled output signal. The measuring bandwidth is equal to the -3 dB small signal bandwidth of the sample-and-hold amplifier. Slew rate is included in the acquisition time specification and may be specified as an additional parameter.

4.9 Conclusion

In this chapter the measurement set-ups and some measurement results of the most important specifications of converters are shown. Many of the DC parameters are fairly easy to measure in contrast with the more difficult to perform dynamic tests. Some results, however, depend on a conglomerate of parameters and are therefore measured as a total. In high-speed A/D converters subsampling is used to obtain a high measurement accuracy without using D/A converters operating at the speed limit of a technology. A quick test is done by using the beat frequency test between the sampling and input signals. This beat frequency signal can be analyzed using a distortion and a spectrum analyzer to obtain information about the distortion and signal-to-noise ratio at these high frequencies. Aperture-time and acquisition-time definitions for sample-and-hold amplifiers are introduced again together with specific measurement set-ups to perform these tests.

Chapter 5

High-speed A/D converters

5.1 Introduction

The best-known architecture for a high-speed analog-to-digital converter is the flash converter structure. In this structure an array of comparators compares the input voltage with a set of increasing reference voltages. The comparator outputs represent the input signal in a digital thermometer code which can be easily converted into a Gray or binary output code. The flash architecture shows a good speed performance and can easily be implemented in an integrated circuit as a repetition of simple comparator blocks and a ROM decoder structure. However, this architecture requires 2^N-1 comparators to achieve an N-bit resolution. The parallel structure makes it difficult to obtain a high-resolution while maintaining at the same time a large bandwidth, a low power consumption and a small die area. Examples of parallel converters are given in references [17,18,19,20,21,22,23,24,25,26].
An alternative to the full-flash architecture is the multi-step A/D conversion principle. In high-speed converters the two-step architecture is the most popular because of the ease of implementation. However, a two-step architecture must be preceded by a sample-and-hold amplifier which performs the sampling of the analog input signal. In the two-step architecture a coarse and fine quantization takes place. After a coarse quantization is performed, the digital signal is applied to a D/A converter to reconstruct the analog signal. This reconstructed signal is subtracted from the analog input signal which is hold stable by the sample-and-hold amplifier. After subtraction has taken place the error signal can be amplified and is then applied to the fine quantizer which performs the conversion into a digital value. The coarse plus

fine output code with, in many cases an error correction operation results in the final digital output word. A good balance between circuit complexity, power consumption and die size is obtained in this type of converter. The final dynamic performance, however, depends on the quality and dynamic performance of the sample-and-hold amplifier. Such an amplifier is difficult to design.

In MOS circuit solution which are based on a discrete-time operation of the system, the sample-and-hold operation is mostly combined with the operation of the system. A full flash system therefore consists of 2^N -1 small sample-and-hold comparator/amplifier circuits which perform the discrete-time operation on the analog input signal. Offset compensation is obtained at the same time.

A two-step system implementation can be easily obtained by using a set of coarse sampled data comparator/amplifiers stages and a set of fine identical stages. The coarse conversion is performed by comparing the input signal with the coarse tap voltages on the input ladder. After the coarse value is determined, then a block of ine reference voltages is switched on. These reference voltages are in between of the two already determined coarse ladder taps. Again a comparison is performed and the final output code is obtained. In this system the ladder is used for coarse and fine quantization without needing an extra D/A subtractor circuit to drive the fine converter stage. Different system implementations will be described using bipolar, CMOS or biMOS technologies.

To overcome some problems of the sample-and-hold amplifier design alternatives have been worked out which have the advantage of the digital sampling used in the full-flash converter and the die size of the two-step system but do not require a sample-and-hold amplifier. This architecture is called a folding architecture, which is capable of achieving a large analog bandwidth and high resolutions without incurring the power and area penalties associated with the flash architectures. (See references [27,28,29,30,5]).

By using folding techniques an A/D converter can be designed in which each comparator detects the zero crossings of the input signal through a number of quantization levels, thus reducing the number of comparators required for a given resolution. The number of comparators is reduced by the number of times that the input signal is folded by the folding stages. However, each reference level requires a folding stage generating the folding signal. This folding signal is a combination of output signals from folding stages. By combining a number of output signals from folding stages a repetitive folded signal is applied to the decision-making comparators. The folding factor,

which determines the number of signals to be combined reduces at the same time the number of comparators. This reduction in comparators, however, is offset by the number of folding stages which are needed to obtain the resolution of the converter. The number of folding stages can be further reduced by interpolating between outputs of folding stages to generate additional folding signals without the need for more folding stages. The interpolation stage in this way reduces the number of folding stages by the interpolation factor. The folding architecture results in a compact, low-power system with small signal and clock delays over the interconnection lines. Therefore a larger analog input bandwidth can be obtained than would be possible with a standard flash converter.
Up till now no real model has existed which describes the frequency limitations of flash-type converter structures. A high-level model has been developed which describes the non-linear behavior of amplifier stages. This behavior results in a signal-dependent delay giving third-order distortion. Keeping in mind the clock timing accuracies needed in accordance with the converter speed, the third-order distortion term is thought to impose a basic speed limitation on flash converters. This model is used to optimize the analog bandwidth of the converter with respect to the technology used.
Depending on the way the circuits are used a direct implementation form a bipolar technology into an MOS technology is possible if the advantage/ disadvantage of discrete-time MOS solution is not used. In time-continuous MOS designs the same imperfections and limitations as in the bipolar system is found. Auto-zero systems or offset compensation systems might be easier to design in MOS and show a better performance when these systems are not operated at the maximum clock rate of the system but at a much lower sampling rate. An auto zero system therefore must be designed to operate independently of the sampling of the converter.

5.2 Design problems in high-speed converters

There are two main problems that impair the dynamic performance of high-speed A/D converters: *timing* inaccuracies and *distortion*.

5.2.1 Timing errors

In most A/D converters there are three main sources of timing errors:

1) jitter and rise and/or fall time of the sampling clock;

2) skew of the clock and input signal at different places on the chip; and
3) signal-dependent delay.

The sampling clock jitter can originate both inside and outside the A/D converter. The outside sampling clock must be designed to have a very small short-term jitter. Internally, a small rise or fall time of the sampling clock avoids jitter caused by white noise of the clock amplifier circuits. Furthermore, crosstalk from other circuits must be minimized to avoid modulation of the sampling clock. The skew between the clock and the analog signal introduces timing errors into the same signal at different places on the die. The clock signal at the top comparator stage, for example, may be slightly out of phase with the clock signal at the middle comparator. This difference in time causes a quantization error which results in non-linear distortion. As an example, in about 12 ps a signal can travel only 1.8 mm over a die at the speed of light (which is lower on a die because of the high dielectric constant of the oxide layers). Therefore the sampling clock lines and the signal lines in the converter must be laid out very carefully. If the paths of clock and signal lines include different processing circuits then the delays of these processing elements have to match within a fraction of the required timing accuracy.
Finally, many circuits introduce a signal-dependent delay. For example, each amplitude-limiting circuit followed by a bandwidth-limiting circuit introduces a delay which is slope-dependent. These circuits are invariably found in input and comparator stages of high-speed A/D converters. A behaviour model is developed which can be used for optimization of the analog bandwidth of A/D converters.

5.2.2 Distortion

Distortion of the quantized signal can be caused by:

1) large aperture time of the sampling comparators;
2) distortion in the linear part of the input amplifier and comparator input circuits; and
3) changes in the reference voltage values.

A large comparator aperture time may be caused by the architecture of the comparator or by a large rise or fall time of the sampling clock. Such a large aperture time results in high-frequency sampling errors and causes an

averaging effect in the time domain.
Non-linear distortion in the input amplifier and the comparator input circuits introduces harmonics and mixing products of the input signal. These harmonics may give aliasing products in the baseband due to mixing of these components with the sample frequency.
Most high-speed A/D converters require a large number of reference voltages which are normally generated by a resistive divider and a reference source. Errors in these reference voltages introduce a non-linear distortion equivalent to a non-linear distortion in the input amplifier. Comparator offset voltages must be small with respect to the reference voltage steps to obtain a nonlinearity which is only dependent on the accuracy of the resistive divider. An additional problem, especially in converters with a large bandwidth, is the kickback from the comparator stages (clock feedthrough) on the reference voltages. During sampling of the input signal the reference voltage temporarily deviates from the nominal value, resulting in additional quantization errors. Timing and distortion problems are common to all A/D converter architectures with a large analog bandwidth. However, the following sections will show that these problems can be minimized more easily in folding architectures than in full-flash or two-step converters.

5.3 Full-flash converters

In an N-bit flash A/D converter, 2^N -1 reference voltages and comparator stages are used to convert the analog input signal into a thermometer-like digital output code Fig. 5.1. This code is converted into a binary output code using a ROM structure. In today's technologies, 8-bit converters having a reasonable die size and consuming moderate power are available. Increasing the resolution to 10 bits increases the die size and power dissipation roughly four times. In practice, however, there is a limit to the power dissipation which can be handled by packages. Therefore the power per comparator stage must be drastically reduced to keep the overall power dissipation at the same level as the 8-bit unit. As a result, the bandwidth of the comparators has to be reduced, resulting in a much lower effective analog bandwidth for the converter. The bandwidth of a system is mostly related to biasing current, which in turn results in power dissipation. Because of the increase in size, it is more difficult to distribute clock and input signal lines without introducing delay-induced errors exceeding $\pm \frac{1}{2}$ LSB, and to match the properties of all these comparators within the same specification. The input

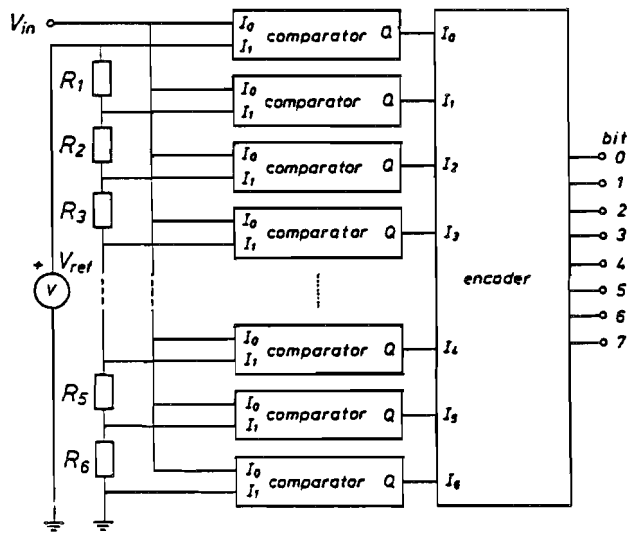

Figure 5.1 : Full-flash A/D converter structure

capacitance of the system increases linearly with the number of comparators, making it impractical to incorporate an input signal buffer on the chip. Even external buffers are difficult to design and need a large power-driving capability at high frequencies. The large number of comparators results in a heavy loading of the clock driving circuits. Small rise and fall times of the clock signals are difficult to obtain and therefore external clock drivers are often required.

In Fig. 5.2 an example of a comparator which can be used in a full-flash converter is shown. The circuit basically consists of a clocked master-slave flip-flop. At the input of the comparator stage an emitter follower is added to increase the input impedance and reduce the loading of the circuit on the reference ladder and the input source. The operation of the circuit is as follows. When the clock signal is high, current flows through the input amplifier of the master flip-flop and during the same time the slave flip-flop is in the latch mode. The input signal is amplified by the input differential amplifier. At the moment the clock changes state, then the input amplifier is disconnected and the difference in signal which is present across the collector resistors of the master flip-flop is amplified by the positively feedbacked master flip-flop. If small signal differences are present, then these differences are amplified until the flip-flop is in a stable condition giving a ONE or ZERO depending on the input signal difference. This signal is amplified by

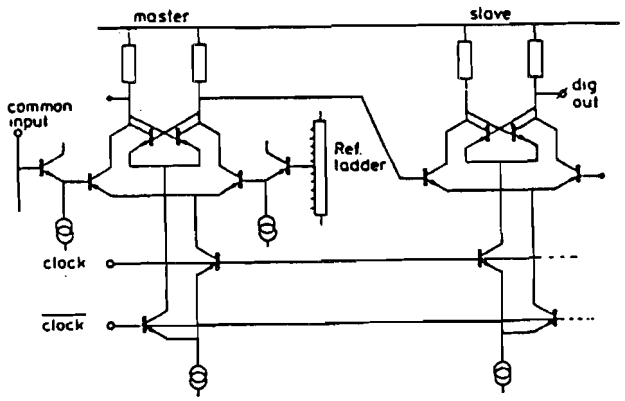

Figure 5.2 : Basic comparator circuit

the input amplifier stage of the slave flip-flop and the decision is transferred to the output. By clocking the flip-flop an analog signal comparison with a large gain and a large bandwidth is obtained. Offset of the input amplifier is an important parameter. In Fig. 5.3 the offset of a differential pair as a function of the collector current is shown. A parameter is the emitter size of the transistors. From the figure it can be seen that with increasing collector current the offset linearly increases. This increase is caused by the emitter resistor difference of the differential pair. An example of a three stage

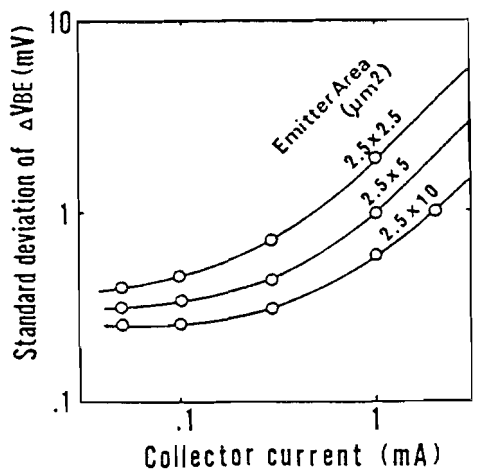

Figure 5.3 : Offset of a differential pair as a function of collector current

comparator cell is shown in Fig. 5.4. In the first stage the input signal is

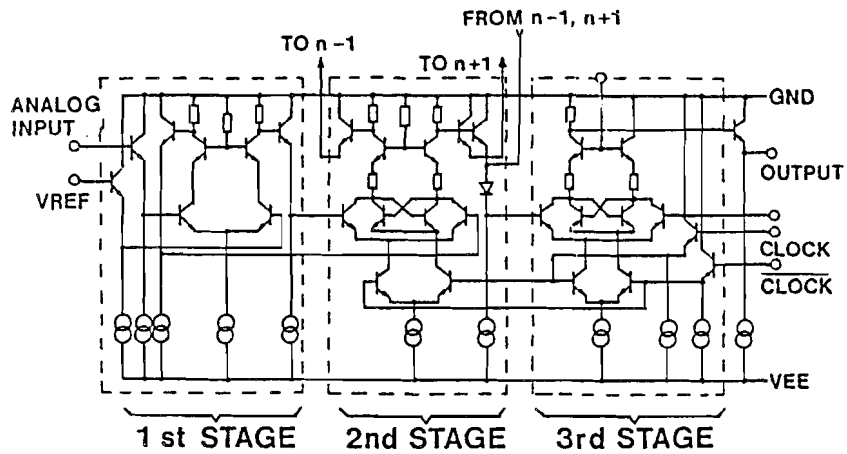

Figure 5.4 : Three stage comparator cell with error correction

continuously amplified. This signal is applied to a clocked comparator consisting of a master-slave flip-flop as shown in Fig. 5.3. Between the master and the slave flip-flop an extra coupling from the above and below neighbour of this comparator is obtained. Therefore the signals "To n-1" and "To n+1" are obtained via emitter followers. These emitter followers together with the output emitter follower of the second stage forms a *wired OR* function. Depending on the signals from the neighbours a correction of the decision signal is possible. In case the above and below neighbour would generate positively a ONE signal and the master comparator would give a ZERO decision, then the wired OR function transfers a ONE signal to the slave flip-flop which is in the third stage. In this way a correction of the decision signal is possible. An improvement in performance is obtained. Furthermore the first encoding from the thermometer into a *one* HIGH level is performed by the wired-OR function too. The ZERO-ONE transition is detected and converted into a HIGH (ONE) signal at the moment this transition occurs. The output of this first encoder is applied to the slave flip-flop which drives the ROM encoder. This ROM encoder performs the final encoding from the thermometer code into the binary output code. In Fig. 5.5 an example of such an encoder is shown. Again this ROM is a wired-OR function. When the signal, for example from the "comparator out n" is a ONE, then all other signals are ZERO. At that moment the bases of the ROM transistors are made high

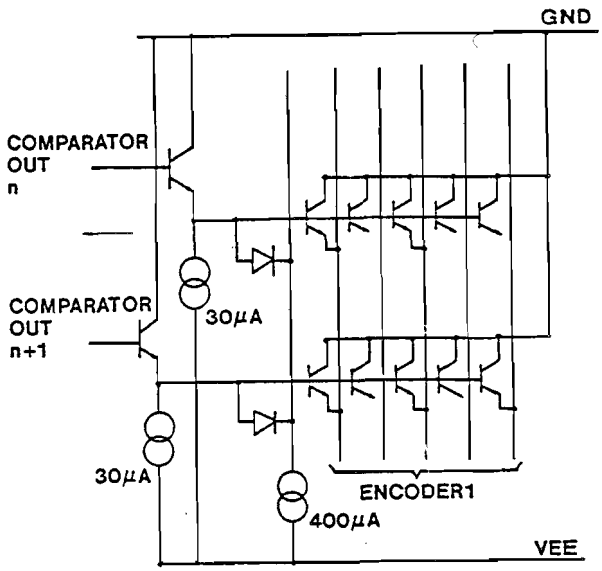

Figure 5.5 : ROM encoder circuit

and a code conversion appears at the output of the encoder. This encoder is very fast and simple to design. In the example shown, the 400 μA current is shared over all the emitter followers which apply the high level to the ROM encoder. In this way a reduction in dissipation is obtained. In Fig. 5.6 a photograph of a 10-bit full-flash converter is shown. The die size is about 10 x 10 mm. In an MOS technology a different comparator architecture is used. In Fig. 5.7 an example of a two stage comparator in MOS is shown. The circuit consists of two capacitive coupled inverter stages, which are bypassed by switches. By closing switch TG_3 the input signal is sampled. During the input sampling the switches TG_2 are closed too. Closing switches TG_2 converts the two CMOS inverters into two diode connected stages which show a low impedance for the signal sampling capacitor C. In this way a sample-and-hold like amplifier construction is obtained. The input signal plus the offset voltage of the comparator stages is stored on the capacitors. After the input signal is stored, all switches are opened and then switch TG_1 is closed to compare the stored signal with the reference voltage which is a part of the ladder tap voltage. The output of the two-stage comparator is applied to a latch circuit which converts the amplified signal into a logic output signal. This logic signal is applied to the thermometer to binary encoder

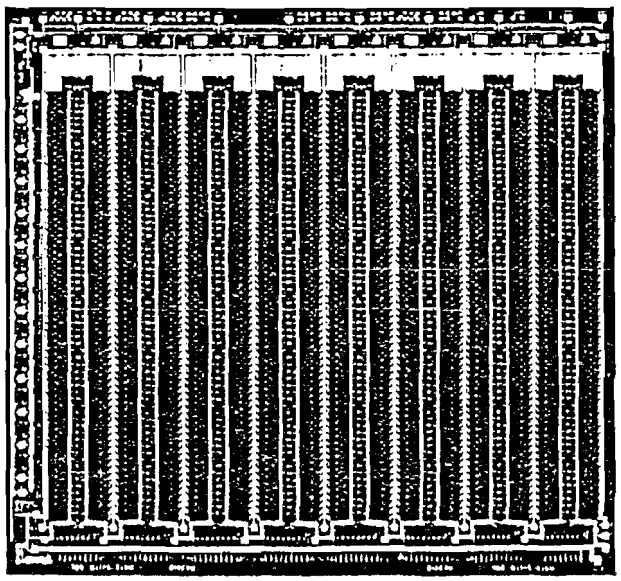

Figure 5.6 : Die photograph of a 10-bit full-flash A/D converter

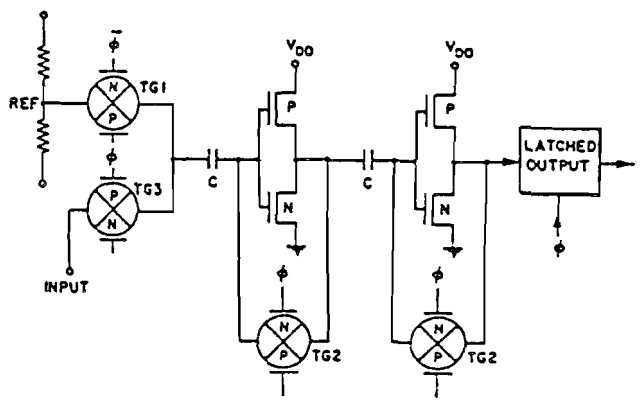

Figure 5.7 : Two-stage MOS comparator circuit

circuit. A problem with this type of comparator is the charge feedthrough of the switches. This charge is stored in the capacitors. Because of this charge there exists no difference between the signal or the channel charge. To overcome a part of the problem, the first switch TG_2 is opened first in time. Afterwards the second switch TG_2 is opened. Channel charge of the first switch, which is closest to the input source is stored as offset on the sec-

ond capacitor and therefore is removed. The comparator described shown in Fig. 5.7 is a sampled comparator type which includes the sample-and-hold amplifier per comparator stage. The maximum sampling frequency of this system is determined by the comparator speed. Because of the single ended construction of the comparator the rejection of the system to noise on the supply voltage is small. This is a second drawback of this system.
A doubling of the sampling speed is obtained by multiplexing the input comparator part. In Fig. 5.8 a simplified circuit diagram is shown.

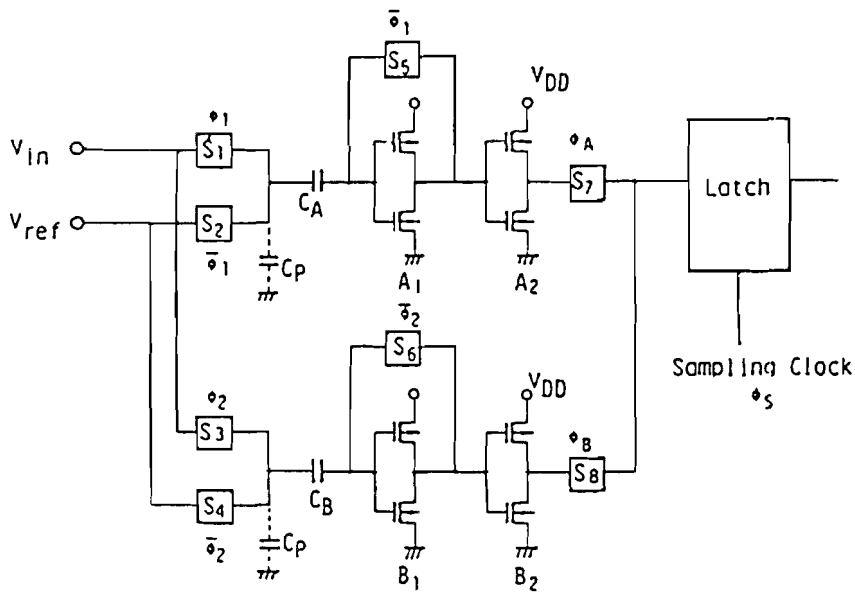

Figure 5.8 : Dual input MOS A/D converter

The circuit consists of two comparator circuits shown in Fig. 5.7 in parallel. The output signal of the comparators is applied to the output latch circuit. The operation of the circuit is as follows. At the moment the input comparator part marked A_1 and A_2 is in the sampling mode by closing switches S_1 and S_5, then the comparator part marked B_1 and B_2 is in the decision phase. Switches S_4 and S_8 are closed and the decision information is applied to the output latch. At the following clock moment the function of comparator A_i and B_i are interchanged and the decision information from A_2 is applied to the latch via switch S_7. A two times faster sampling clock is possible without increasing the circuitry too drastically. The maximum clock frequency in a single MOS A/D converter is determined by the technology. Using the dual input system an increase with a factor two in clock frequency is possible without loosing converter performance.
In Fig. 5.9 an example of a latch circuit in CMOS is shown. The basic latch

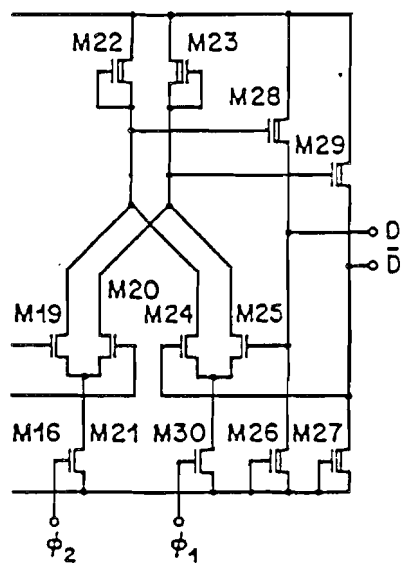

Figure 5.9 : Example of a CMOS latch circuit

is an MOS equivalent of the CML flip-flop shown in Fig. 5.2. Transistors M_{19} to M_{30} perform the latch operation. The clock signals ϕ_1 and ϕ_2 transfer the information from the input to the output of the latch circuit. This circuit configuration can be chosen to minimize the supply voltage noise by clocking and optimize the speed. The high speed is obtained by the reduced

voltage swing of the latch.

5.4 Failure analysis of comparators

When flip-flops are used as comparators then at the beginning of a decision cycle the input signal can be so small that at the end of the decision cycle no digital "1" or "0" value is obtained. Such a condition is called a meta-stable state (MSS). [?] In Fig. 5.10 a generalized curve showing the two logical states V_1 and V_2 and the meta-stable state of a flip-flop are shown. During the design of comparators it is very usefull to obtain a criterion which

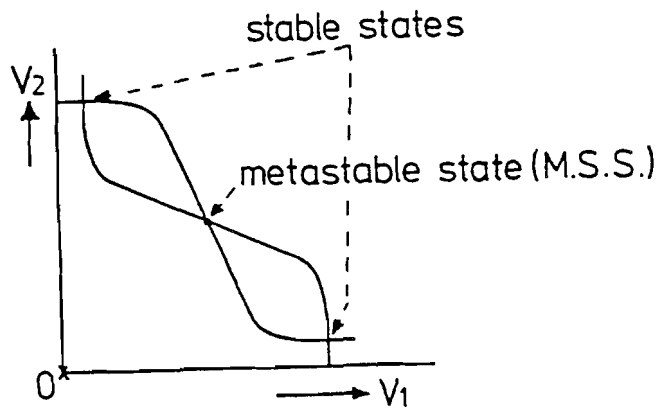

Figure 5.10 : States of a flip-flop used as a comparator

determines the number of times such a state occurs. An analysis will be given which determines the failure rate of a comparator with respect to the sample frequency and the unity gain bandwidth of the amplifiers used in the flip-flop. Noise in the system is supposed to have basically no influence on the number of meta-stable states of the comparators. Using the superposition principle the noise can be referred to the input of the circuit and adds to the input signal. In this way a disturbance of the comparison by noise is obtained but no influence on the number of meta-stable states is found.

5.4.1 First-order model of a flip-flop

In a first approximation a flip-flop can be modeled as two positively feed-backed first order amplifiers. The small signal model is shown in Fig. 5.11 The amplifier stages are modeled as a inveters with a gan $-A$ and a time

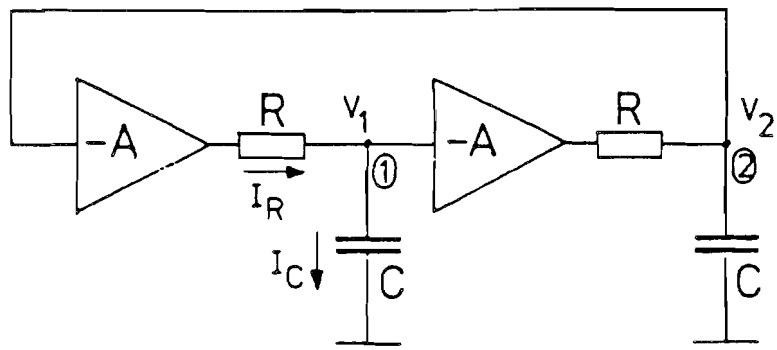

Figure 5.11 : Small signal model of a flip-flop

constant $\tau = RC$. Using feedback theory, the condition for "oscillation" can be used to determine the meta-stable condition. This results in:

$$1 - A^2 = 0 \tag{5.1}$$

In equation 5.1 A is expressed as:

$$A = \frac{A_0}{1 + s\tau} \tag{5.2}$$

Solving equation 5.1 with respect to time the following general relations are found:

$$V_1 = \lambda_1 \exp^{\frac{A_0-1}{\tau}t} + \lambda_2 \exp^{-\frac{A_0+1}{\tau}t} \tag{5.3}$$

and

$$V_2 = -\lambda_2 \exp^{\frac{A_0-1}{\tau}t} + \lambda_2 \exp^{-\frac{A_0+1}{\tau}t} \tag{5.4}$$

V_1 and V_2 are the output voltages of amplifiers 1 and 2 respectivily. In these equations λ_1 and λ_2 are integration constants. These constants can be determined by inserting the intital conditions at $t = 0$ into equation 5.3 and 5.4. These intital conditions are:

$$V_1 = V_{01} = \lambda_1 + \lambda_2 \tag{5.5}$$

and

$$V_2 = V_{02} = -\lambda_1 + \lambda_2 \tag{5.6}$$

Solving λ_1 and λ_2 from equations 5.5 and 5.6 the following result is obtained:

$$\lambda_1 = \frac{V_{01} - V_{02}}{2} \tag{5.7}$$

and

$$\lambda_2 = \frac{-V_{01} + V_{02}}{2} \tag{5.8}$$

Furthermore by analyzing equations 5.3 and 5.4 with increasing time t only the terms with the positive exponent show an increase in signal.
Putting

$$V_{01} - V_{02} = \delta V_0, \tag{5.9}$$

the solutions for the dominating output voltages can be obtained. The result is:

$$V_1 = \delta V_0 \exp^{\frac{A_0-1}{\tau}t} \tag{5.10}$$

and

$$V_2 = -\delta V_0 \exp^{\frac{A_0-1}{\tau}t} \tag{5.11}$$

In general the input signal values δV_0 are uniformly distributed over the decision interval, the same is now found for the output signal values V_1 and V_2 after a time t_d (= decision time) has been elapsed. Note that the differences between the final states of $V - 1$ and V_2 is equal to the logical swing V_l of the system.
This can be related to the probability that a meta-stable state occurs after the sampling time t_d:

$$P(t > t_d) = \exp^{-\frac{A_0-1}{\tau}t_d} \tag{5.12}$$

Equation 5.12 is valed when one sample is taken. If we take $f_s = \frac{1}{t_s}$ samples, then the number of meta-stable states per second becomes:

$$M_n = f_s \exp^{-\frac{A_0-1}{\tau}t_d}. \tag{5.13}$$

Equation 5.13 can be rewritten into general design parameters. Mostly $t_d = \frac{t_s}{2}$ when a symmetrical clocking scheme is used. During half the sampling time the flip-flop is in input position while during the second half sampling time the decision is taken. Furthermore the time constant τ can be expressed into the unity gain bandwidth of the individual amplifiers. This results into:

$$\tau = \frac{1}{2\pi f_{3dB}} \tag{5.14}$$

and with $f_{ugb} = A_0.f_{3dB}$ equation 5.13 can be rewritten into:

$$M_n = f_s \exp^{-(1-\frac{1}{A_0})\frac{f_{ugb}}{f_s}\pi}. \tag{5.15}$$

When a moderate gain is used in the amplifier stages, then equation 5.15 gives a direct relation between the unity gain bandwidth (f_{ugb}) of the amplifiers and the sampling rate which can be applied to the system. At the moment the number of meta-stable states needs to be determined over longer time periods (1 minute, 1 hour, 1 day or even 1 year), then equation 5.15 becomes:

$$M_n = T_p \times f_s \exp^{-(1-\frac{1}{A_0})\frac{f_{ugb}}{f_s}\pi}. \tag{5.16}$$

Here T_p is the time period over which the number of meta-stable states is determined. In Fig. 5.16 the relation between the unity gain bandwidth of a system and the sampling frequency are shown for different time intervals T_p. Figure 5.12 shows a very powerful relation in designing flip-flops with a

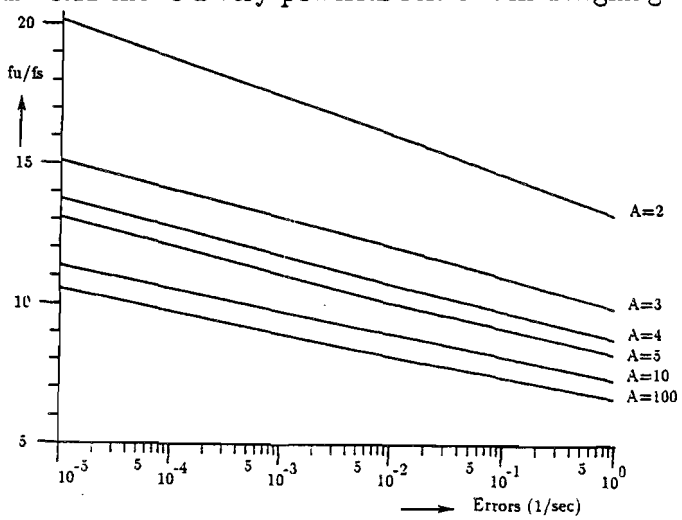

Figure 5.12 : Relation between unity gain bandwidth and sampling frequency to obtain one meat-stable state as a function of period time

high decision accuracy.

5.5 Two-step flash converters

To avoid some of the problems encountered with a full-flash converter the two-step architecture was developed. This two step method uses a coarse and fine quantization to increase the resolution of the converter (see Fig. 5.13). Examples of converters using the two-step architecture are given in references [31,32,33,34,35]. Consider, for example, an 8-bit system that uses a 3-bit coarse quantization. After the coarse quantization has been performed,

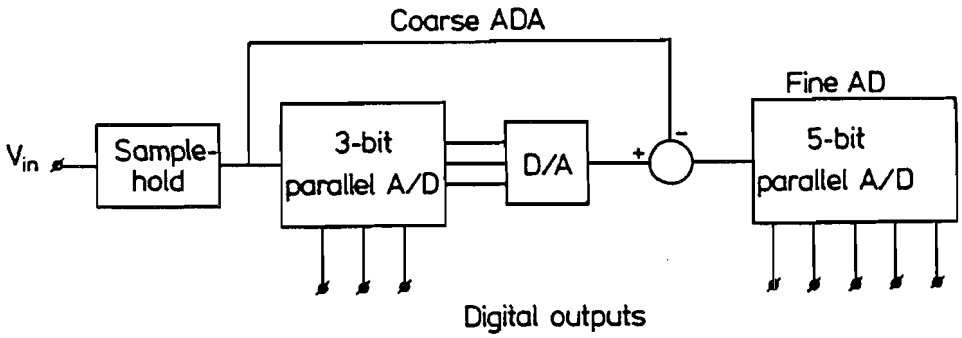

Figure 5.13 : Two-step A/D converter structure

the 3-bit result is converted into an analog value again using a 3-bit D/A converter. This analog value is subtracted from the input signal and the difference is applied to a 5-bit fine converter which generates the fine code. In this system only 40 comparators are needed to achieve 8-bit resolution. The 3-bit D/A converter, however, needs to have an 8-bit accuracy and linearity to obtain the full 8-bit overall linearity. Furthermore, a sample-and-hold amplifier is needed to compensate for the time delay in the coarse quantization/ reconstruction step. In this way the dynamic performance of the A/D converter is mostly determined by the performance of the sample-and-hold amplifier. In some applications a second sample-and-hold amplifier is used to store the analog remainder of the input signal for fine quantization. In the meantime a new input sample is coarse-quantized. This architecture results in a higher throughput rate for the total system. Higher resolutions can easily be obtained without a drastic increase in hardware and power dissipation. The popularity of this converter type depends on the availability of high-performance sample-and-hold amplifiers. Unfortunately, in bipolar technologies it is difficult to design sample-and-hold amplifiers which meet the requirements. In Fig. 5.14 an example of a two-step bipolar converter circuit is shown. The sample-and-hold amplifier is followed by two 6-bit quantizer circuits from which the first quantizer uses a 6-bit D/A converter to reconstruct the analog quantized signal. The 6-bit quantizers are full-flash type A/D converters. At the output of the first A/D converter the thermometer code is used to drive the segmented D/A converter. In this converter equal well matched currents are used to obtain the overall accuracy. The output current of the D/A converter is applied to resistor R_d to reconstruct the quantized analog signal. This signal is subtracted from the

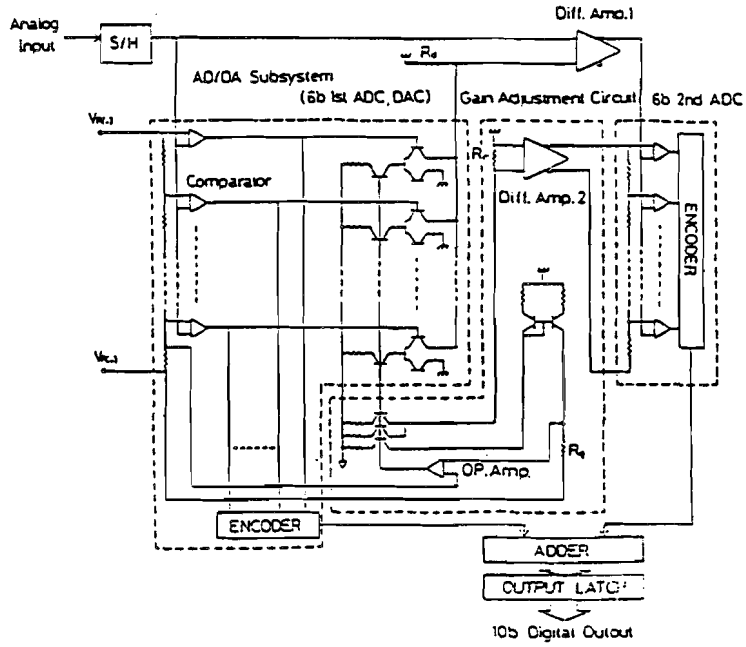

Figure 5.14 : Two-step bipolar A/D converter circuit

input signal and amplified. This amplified signal is applied to the second 6-bit flash converter. The outputs of both 6-bit flash converters are decoded and matching errors between the first and the second step are corrected. At the output a 10-bit binary code is obtained after adding the coarse and fine signals.

The reference voltage for the first flash converter is applied directly across the resistor as V_{R+} and V_{R-}. From V_{R-} with R_g the reference currents for the D/A converter is generated. The operational amplifier controls the bases of the current source transistors in such a way that an identical current as flowing through R_g is generated. An extra D/A current is used to generate across R_r the reference voltage for the second flash converter. Differential amplifier(2) applies this reference voltage across the second string of reference resistors. In this way variations due to process parameters are canceled. The only important factor is matching of the components.

In Fig. 5.15 an MOS implementation of a two-step A/D converter using a cascade of two pipelined sample-and-hold amplifiers is shown. The system is built up using a first 4-bit coarse quantizer with built-in D/A converter

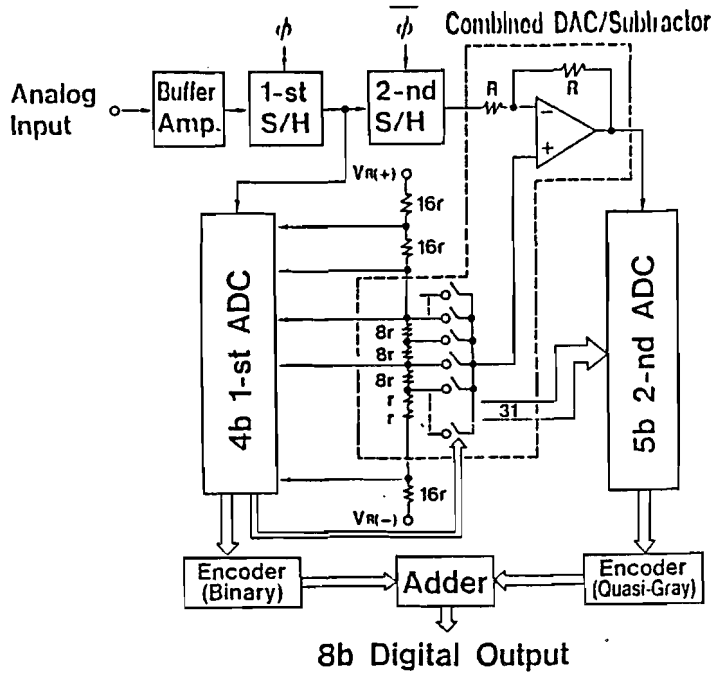

Figure 5.15 : Two-step MOS A/D converter with two pipelined S/H amplifiers

function and a second 5-bit fine quantizer. The first sample-and-hold amplifier samples the analog input signal. This signal is converted into a digital value using the first 4-bit flash A/D converter. The information of the first quantizer is stored and the D/A converter segment is switched on. In the D/A converter a double amount of taps is used because of the factor two gain in the Subtractor circuit. After completion of the coarse quantization the input signal is transferred into the second sample-and-hold amplifier. The D/A output signal is subtracted from the analog input signal and applied to the 5-bit fine quantizer. Finally the digital signals of the coarse and the fine quantizer are added to obtain the final output signal.

In Fig. 5.16 a more detailed circuit implementation of the sample-and-hold amplifiers and the subtractor circuit is shown. The sample-and-hold amplifiers are of the inverting type. The connection of the hold capacitor in parallel with the feedback resistor R_F introduces a frequency limitation which is not allowed. Therefore across the input resistor R_I a compensation capacitor C_C is connected. With equal time constants the transfer function of the sample-and-hold amplifier is only limited by the gain-bandwidth product of the amplifiers.

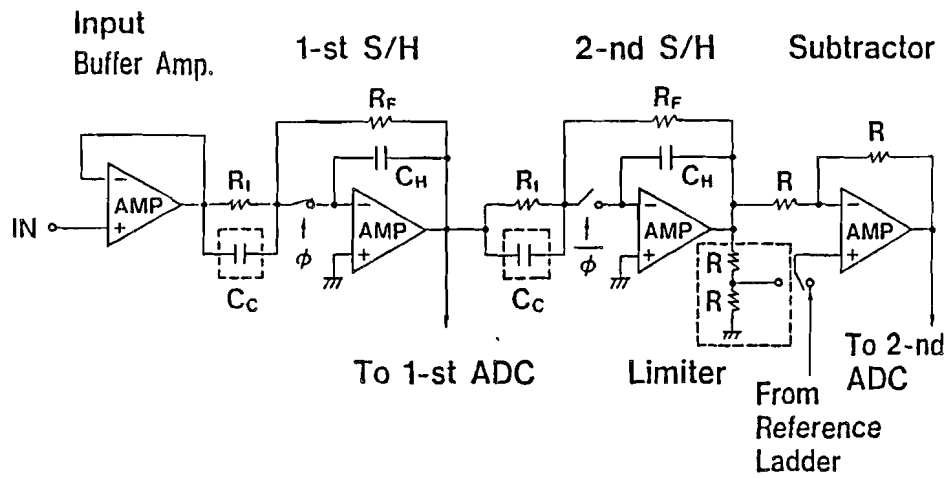

Figure 5.16 : Detailed circuit diagram of the S/H and Subtractor circuit

A second implementation of an MOS two-step A/d converter architecture is shown in Fig. 5.17. Basically it uses two MOS two stage comparator circuits in a coarse and fine quantization mode. The difference in operation of the circuit with respect to the circuit in Fig. 5.8 is the operation of the sampling switches SW_1, SW_2 and SW_3. During the sampling mode all switches except SW_2 are ON. The input signal is sampled on the capacitors C_1. In Fig. 5.17 the top circuit forms the coarse quantizer circuit with the switch driving signals as shown by "Coarse Comparators", while the lower quantizer circuit shows the fine quantizer with at the bottom of the figure he switch driving signals as defined by "Fine Comparators". After the input signal is sampled, the coarse flash quantizer determines the coarse value of the input signal. In the reference resistor string 255 resistors are used. Every 16 taps a coarse level is applied to the coarse quantizer to obtain the coarse reference levels. The coarse digital output signal drives the switches which apply the fine levels to the fine quantizer consisting of 15 sample and hold comparator latches. By switching the V_{refn} levels with the fine information to the 15 fine comparator latches the fine conversion takes place. The total output signal is the sum of the coarse and the fine digital output signals. By using a double fine quantization circuit the coarse quantizer can be used again during the time one of the fine quantizers is determining the fine code. This multiplexing allows a doubling of the conversion speed of the circuit. In Fig. 5.18 the construction of the coarse and fine reference

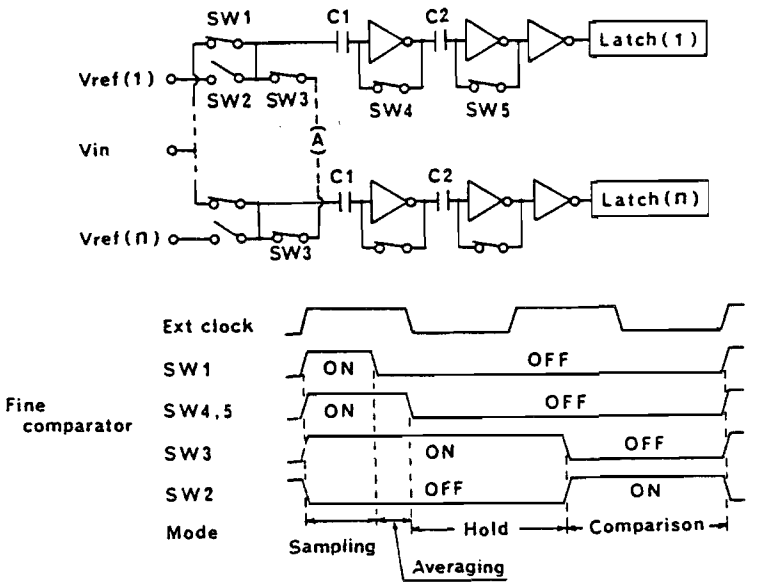

Figure 5.17 : Coarse-fine MOS A/D sampled comparator converter system

circuit is shown. Every 15 taps a coarse tap is used to supply the reference voltage to the coarse quantizer. The fine reference signals applied to the fine bit quantizer are applied by closing one of the 15 row switches by the coarse quantizer circuit. A BiCMOS solution for a two-step A/D converter is shown in Fig. 5.19. The circuit consists of a coarse and fine resistor divider structure. During the coarse conversion the input signal is compared with the coarse reference voltage taps. When a decision is made, the fine voltage divider resistor is connected across two coarse taps which have a voltage level just above and just below the input signal. In the coarse quantizer a resolution of 5-bit is used. In the fine ladder 49 comparators are used to have a correction possibility in case a small error is made during the coarse conversion. The fine ladder is applied via buffer amplifiers across the during the coarse conversion determined ladder taps. MOS switches are used for tap voltage switching while in the comparator stages bipolar transistors can be used because of the low offset voltage. In the output logic circuit the overrange or underrange corrections are made to obtain a 10-bit output code.

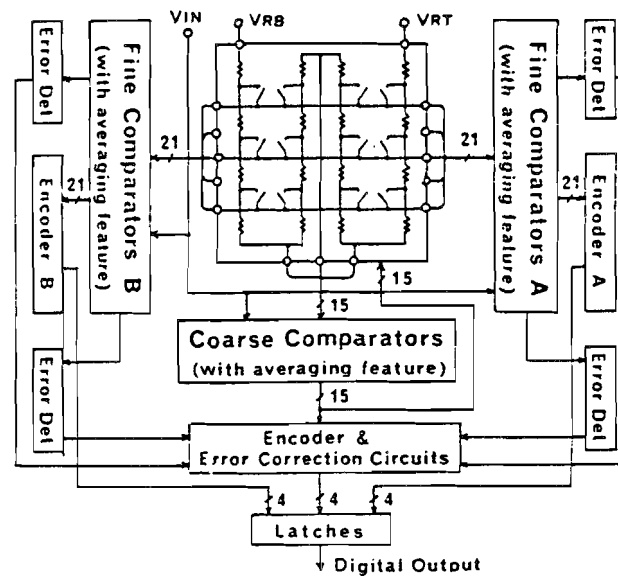

Figure 5.18 : Coarse-fine reference network configuration

5.6 Multi-step A/D converter

In Fig. 5.20 an example of a multi-step A/D converter is shown. The circuit consists of a three comparator quantizer stage with decoder, a successive approximation register which can handle more than one bit at a time and a 10 bit D/A current converter. The output current of the D/A converter can be switched through the three reference resistors R at point V_3 indicated as current I_{01} or through the subtraction resistor R at the node V_1 indicated as current I_{02}. At the start of the conversion the input signal V_{in} is applied at the high input impedance nodes of the comparators. The current I_{02} is made zero and the output current of the D/A converter is switched as I_{01} through the three resistors R generating the three reference voltages. After a decision has been made the D/A output current is switched as I_{02} through the resistor R to subtract a quantized voltage from the input signal V_{in}. The reference voltage level applied to the three comparators is now reduced by decreasing the D/A output current I_{01} so the next quantization step can be performed. This operation is furthermore repeated until the signal at the node V_1 is as close as possible to the input signal V_{in} and all the bit currents of the D/A converter are tried out during the conversion process. The digital

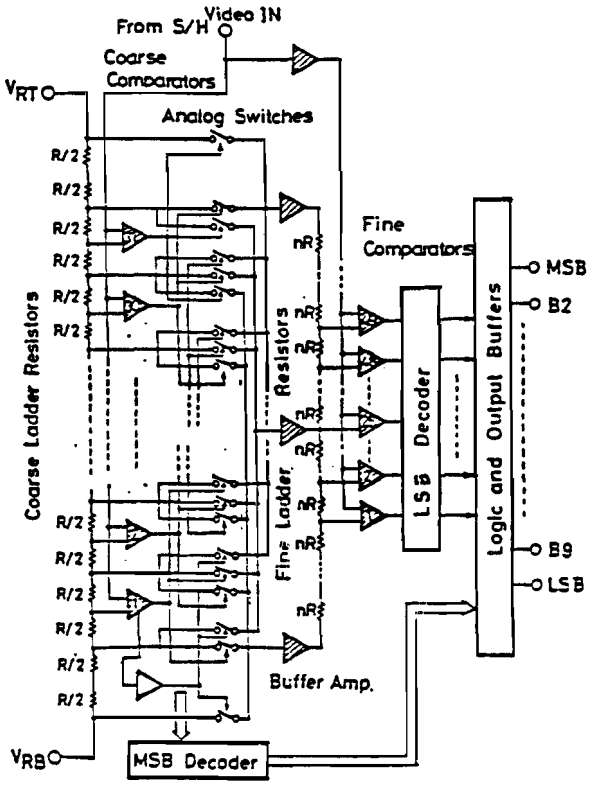

Figure 5.19 : BiCMOS two-step A/D converter

of the successive approximation register is applied to the output buffers to store the output code of the converter.
It is clear that by increasing the number of comparators the number of approximation cycles can be reduced, which results in a smaller conversion time. At the input of the converter, however, a sample-and-hold amplifier is needed to sample the analog input signal and hold this signal during the time the conversion takes place.

5.7 Folding A/D converters

In a folding architecture, analog preprocessing is used to transform the input signal into a repetitive triangular-shaped output signal. (see Fig.5.21) In

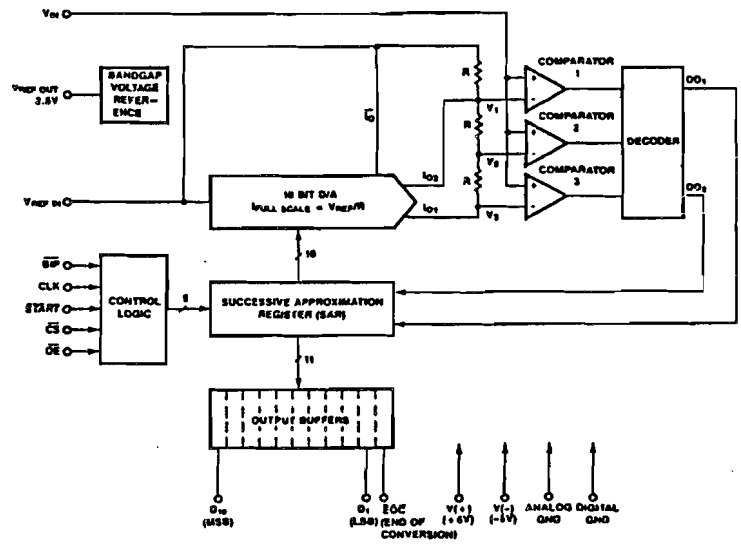

Figure 5.20 : Multi-step A/D converter

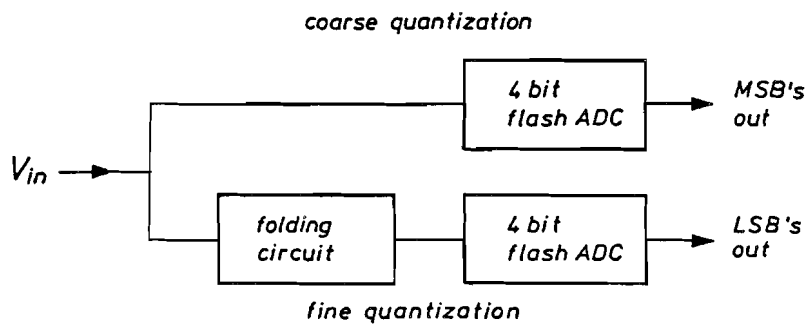

Figure 5.21 : Folding A/D converter architecture

this system the most significant bits are determined by the coarse quantizer, which determines the number of times a signal is folded. The fine bits are determined by the fine quantizer which converts the preprocessed "folded" signal into the fine code. In this way it is possible to obtain an 8-bit resolution with only 30 comparators without the need for a sample-and- hold amplifier. The basic idea behind the "folding" system is to make multiple use of the same components (e.g. comparators). The low component count results in a small die area, while more power can be expended into the system to obtain a larger bandwidth in the comparator and folding stages. One drawback, however, is the higher repetition rate of the folded input signals

which can result in rounding-off of the tips of the folded signal. This rounding problem can result in a loss of resolution at the high-frequency end of the input spectrum when amplitude quantization is used in the conversion process. The moment a sample-and-hold amplifier is added to the system, the rounding problem is eliminated and the only speed limitation is the settling time of the system.

5.8 Current-folding A/D converter system

The basic circuit of a 2-bit quantizer-subtractor circuit using reference currents is shown in Fig. 5.22. The most important parts are the reference

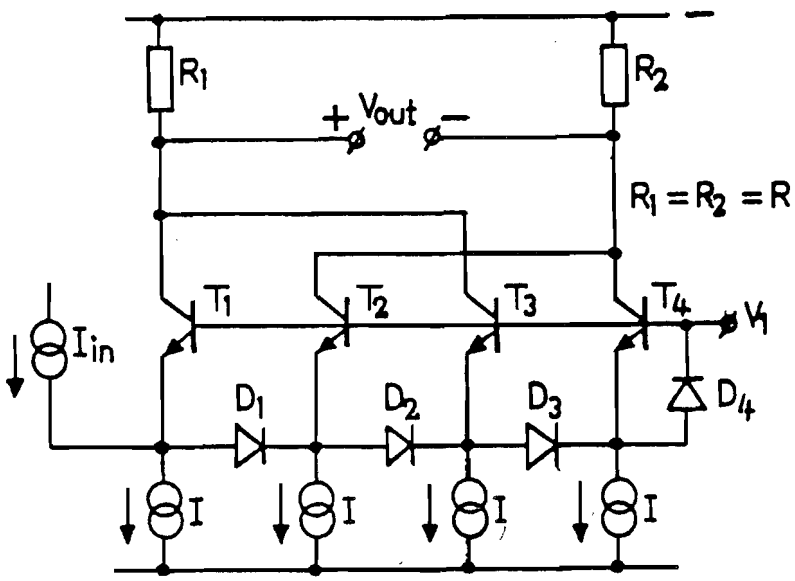

Figure 5.22 : Current-folding 2-bit A/D converter structure

current sources I, the common-base transistor stages T_1, T_2, T_3 and T_4 and the diodes D_1, D_2 and D_3. The input signal current I_{in} is compared with the four reference currents I. The collectors of the odd-numbered transistors of the common-base stages T_1, T_3 are connected and so are the even numbered transistors T_2 and T_4. If the input current I_{in} is equal to zero, then through all common-base transistors currents I will flow. This results in currents $2I$ flowing through each of the resistors R_1 and R_2. With equal-valued resistors, the differential output voltage V_{out} will be zero. If an input signal current I_{in} is applied, e.g. $1\frac{1}{2}I$, then this current is subtracted from

the reference current flowing through T_1. The difference in current, being $\frac{1}{2}I$, will forward-bias the diode D_1 and will be subtracted from the reference current I flowing through T_2. As a result the current through R_1 is reduced to I and the current through R_2 is reduced to $1\frac{1}{2}I$. In Fig. 5.23 the operation of the circuit with a triangular input current changes from 0 to $4I$ as a function of time. To make is easier to understand the circuit operation a triangular-shaped input current is used as shown in the illustrations. The result of the operation is an output signal with a frequency

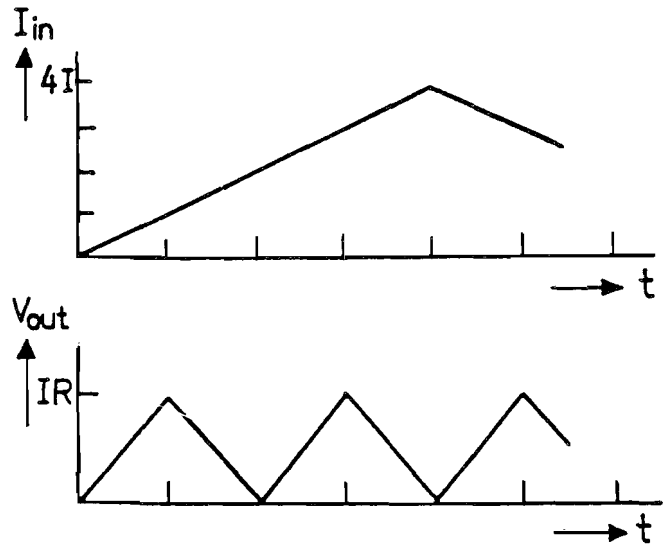

Figure 5.23 : Input and output signal as a function of time

which is a multiple of the input frequency. In this particular case the output frequency is four times higher than the input frequency. Moreover, the output amplitude is reduced from 0 to $4I$ into 0 to I. The output signal of the circuit can be applied to a following quantizer which may consist of a flash A/D converter. The digital output signals of the coarse quantizer are determined by the conduction or non-conduction of the coupling diodes D_1, D_2 or D_3. The voltage excursion at the input of the circuit is equal to the voltage across the number of conducting diodes. In the example given in Fig. 5.22 the maximum voltage excursion will be between zero and $3V_D$ plus the voltage across the overload clamp diode V_{D4}. When for an increasing resolution of this system the number of reference sources is increased, the voltage excursion at the input increases and may exceed the maximum re-

verse bias of the base-emitter voltage of the transistors. This is not allowed because at that moment the transistor will deteriorate. To overcome this problem, more quantizer circuits can be connected in parallel to interpolate additional levels within one diode voltage. The diode switching quantizes the input signal with a very high accuracy. The overall conversion linearity is thus determined by the accuracy of the reference current sources I.

5.8.1 Parallel connection of quantizers

The parallel connection of two coarse quantizers of the type shown in Fig. 5.22 which interpolate within one diode voltage is shown in Fig. 5.24. Diode

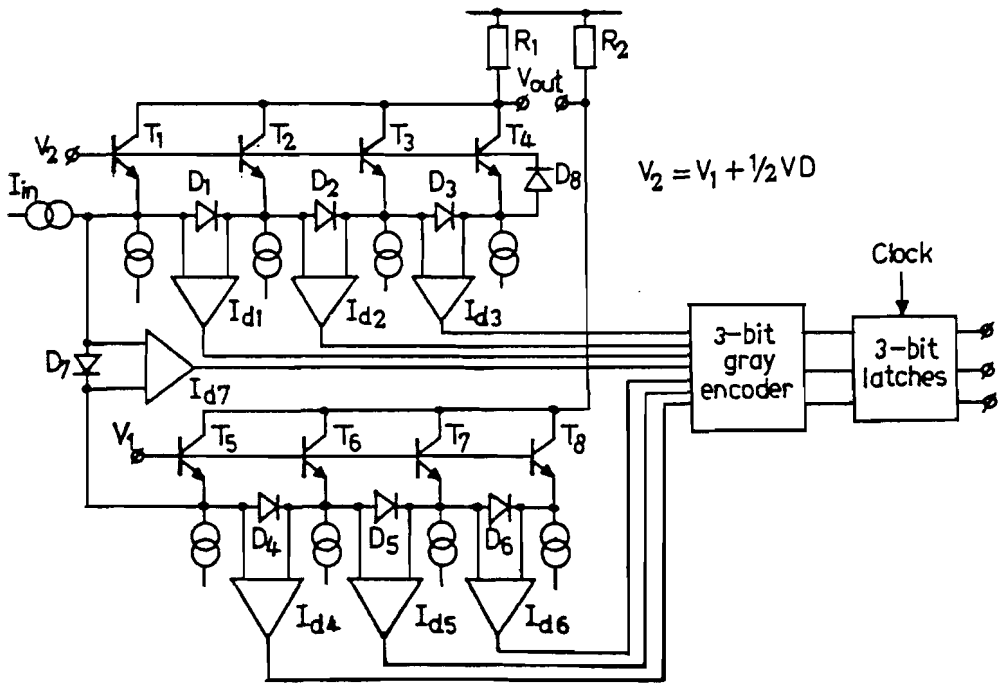

Figure 5.24 : 3-bit coarse quantizer configuration with digital signal encoding

D_7 and the voltage sources V_1 and V_2 are added for this purpose. The voltage difference between V_1 and V_2 is equal to $\frac{1}{2}V_D$. As a result voltage V_1 must be adjusted in such a way that $V_2 = V_1 + \frac{1}{2}V_D$. The parallel connection of the second coarse quantizer also eases the interconnection of the odd or even numbered collectors as shown in Fig. 5.22. As can be seen from figure 5.24, collectors T_1, T_2, T_3 and T_4 are connected to resistor R_1. The same operation

is performed with the collectors of T_5, T_6, T_7 and T_8 which are connected to resistor R_2. The differential output voltage between resistors R_1 and R_2 show again a triangular form. This can be explained by supposing that the input current I_{in} increases from 0 to $8I$. At first the current I flowing through T_1 is subtracted. Then diode D_7 starts conducting and the current through T_5 is subtracted from the input current. The voltage difference between V_1 and V_2 which was equal to half a diode voltage performs the switching in conduction of diodes from one coarse quantizer to the other and vice versa. Diodes D_1, D_4, D_2, D_5, D_3, D_6 and D_8 will become active alternately. In this way the eight quantization levels are tripped by the input signal, and the maximum input voltage span is equal to four diode voltage levels. The digital signals are detected by the level detectors I_{d1} to I_{d7} which are activated by the forward bias voltages of the conducting diodes D_1-D_7. The output signals of the level detectors are fed to an encoder circuit which converts the seven input signals into a 3-bit binary output code. This output code is latched to give a digital output signal.

5.8.2 Fine quantizer circuit

The coupling of the coarse quantizer with a 4-bit fine quantizer is shown in Fig. 5.25. In the fine quantizer system a flash type A/D converter structure

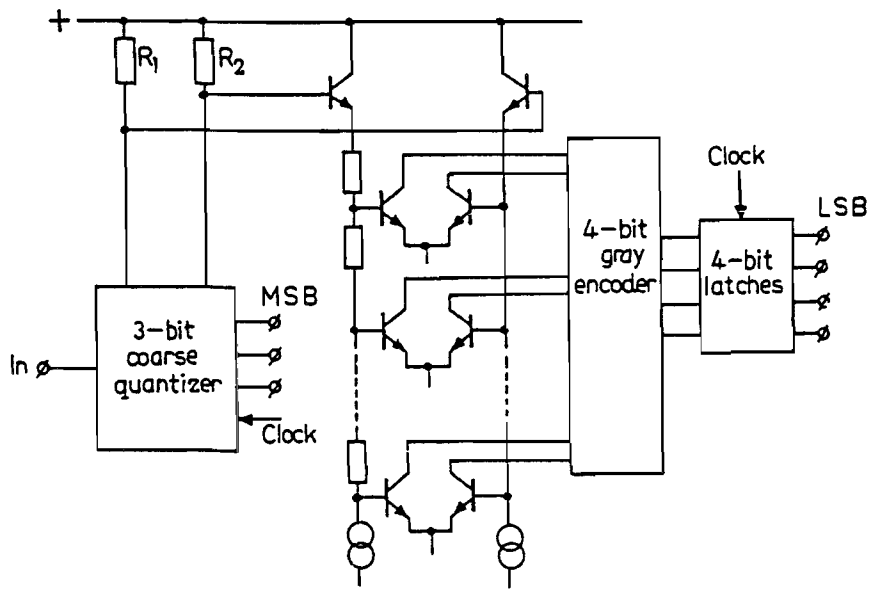

Figure 5.25 : 4-bit fine quantizer system

is used. The fine encoder is driven via emitter followers to avoid loading of the coarse system by the large amount of differential ampliers. The differential amplifier stages are used as comparator stages. The output of these stages is encoded and converted into a 4-bit binary code. This binary code is latched in four latches to give the digital output code of the circuit. The small delay in the coarse quantizer, which is determined solely by the switching on and off of the diodes and the common-base transistors, allows digital sampling of the input signal by latching comparators. Furthermore, this circuit configuration processes the analog input signal independently of the sampling frequency. There is therefore no coupling between the maximum analog input frequency and the maximum sampling frequency which can be used. Usually a much higher sampling frequency can be used without affecting the accuracy of the system. As is known, oversampling increases the resolution of a system without needing additional comparators or other circuitry. Note also that the differential fine comparator stages reject the

common mode signal part which is present on the voltage across R_1 and R_2.

5.8.3 Fine encoder-latch circuit

A detail of the fine encoder-latch circuit is shown in Fig. 5.26. To minimize the amount of comparator latches the encoding of the signal into a binary code is first performed. From Fig. 5.26 it can be seen that the differential

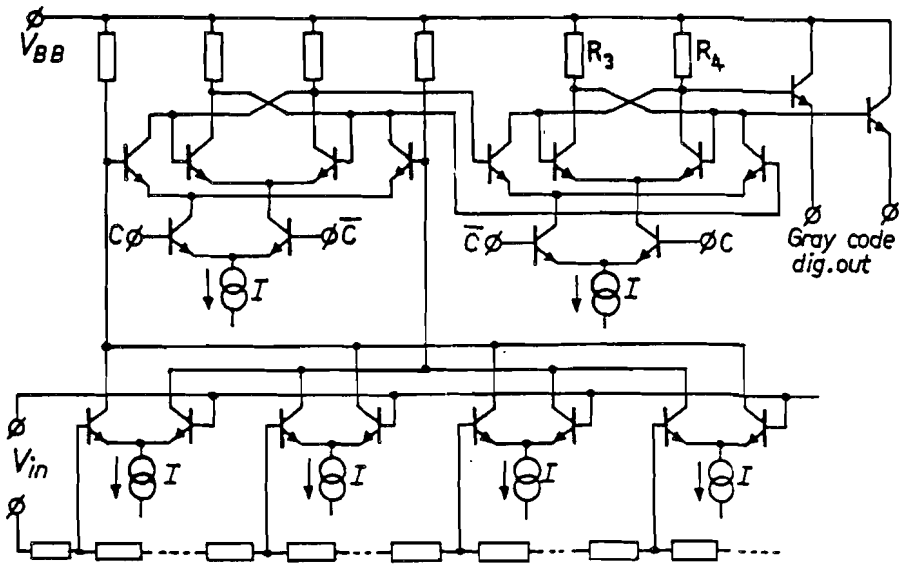

Figure 5.26 : Detail of fine encoder-latch circuit

comparator- amplifier stages are cross-coupled and connected to the input of a master-slave flip-flop, which operates as a sensitive comparator stage. When four stages are cross-coupled, then information about the zero crossing of one differential stage is obtained as long as the other three stages are in the overdrive position. In this way the number of comparator stages can be reduced by a factor four. Note however, that due to the fact that the other three differential stages are overdriven, the bias currents of these amplifiers still flow through the collector resistors. As a result a much better matching of these currents I is needed, while an additional requirement is made for the matching of the collector resistors to obtain an accurate level comparison. In the master flip-flop the decision is made when the clock signal becomes low. At that moment the latch becomes active and is very sensitive to differences

in the input signal. The condition it starts from is a meta-stable condition with nearly equal currents flowing through the collector resistors (suppose a small difference must be detected in this example). After a logical signal is obtained in the master flip-flop, this information is transferred to the slave flip-flop which stores the digital information during the decision phase.

5.8.4 Complete A/D converter

Using the current folding architecture a 7-bit A/D converter IC has been designed. At low frequencies this system performs fairly well. The simplicity of this system results in a small die size of 2.4 x 2.5 mm. A drawback of this system at high frequencies is the rounding of the folding signal. This rounding results in a loss of fine codes. Also the delay between the coarse and the fine quantizer decisions results in code errors at the moment when the most significant bits are changing. These code errors result in glitches which are not allowed. In the next part of this chapter improved systems will be discussed which do not suffer from these drawbacks.

5.9 Double folding system

To avoid missing codes resulting from rounding of folding signals at high frequencies a double folding system has been developed. A block diagram of the double folding system is shown in Fig. 5.27. The system consists, for

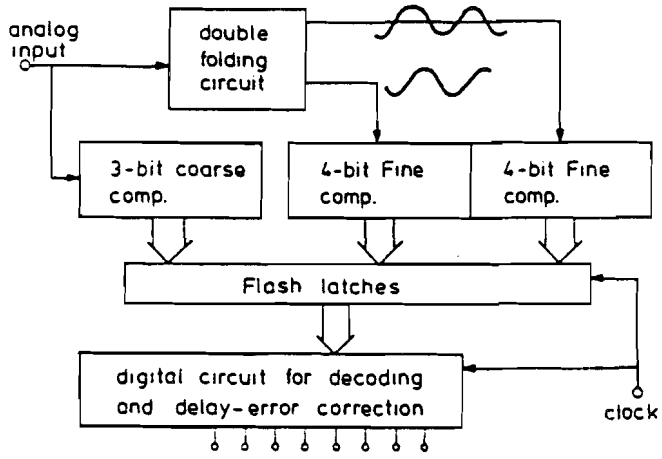

Figure 5.27 : Block diagram of double folding system

example, of a 3-bit coarse quantizer which determines the coarse bit and a folding system which generates two analog output signals with a 90-degree phase shift. The analog output signals from the folding circuit are applied to two 4-bit fine quantizers to determine the fine output code. The basic idea for using two fine quantizers with 90-degree phase shifted input signals is that at the moment the signal applied to, for example, fine quantizer 1 runs out of its linear range, fine quantizer 2 will come into its linear range and vice versa. Furthermore, the connection of the folding signals to two 4-bit fine quantizers increases the resolution to 5 bits. In this way a total resolution of 8 bits for this converter structure is obtained. The folding system reduces the number of input amplifiers which are connected to the input terminal in comparison with a full-flash construction. It is now possible to drive the input stages from an on-chip input amplifier/ buffer amplifier. The output signals of the coarse and fine quantizers are latched and applied to an error correction circuit. In this circuit delays due to the different transit times in the fine and coarse parts of the converter are eliminated. The delay-error correction is based on the idea that the coarse quantizer determines which bit transitions can be erroneous. At that moment a correction is applied which depends on the code of the fine quantizer. The fine quantizer information is accurate to the least significant bit and therefore the exact coarse code transition can be determined. In Fig. 5.28 the output waveforms of the folding circuit are shown. The figure shows that when output 1 is in the linear transfer range, output 2 is in the non-linear range. When these waveforms are compared with the single folding system, the coarse bit should be determined at the tips of the first folding signal. In this double folding system these "tips" coincide exactly with the zero crossing of output signal 2.

5.9.1 Practical double folding circuit

A simplified circuit diagram of the double folding system is shown in Fig. 5.29. The "phase"shift between the two analog output signals of the folding circuit is obtained by connecting one folding processor to a shifted reference voltage with respect to the other folding processor. In practice this shifting is obtained by connecting the input differential amplifiers of the first analog processor to resistor taps which are in between the resistor taps to which the second analog processor is connected. The collectors of the differential amplifiers in the first or the second processor are cross-coupled to obtain a repetitive output signal. This output signal depends only on the switching

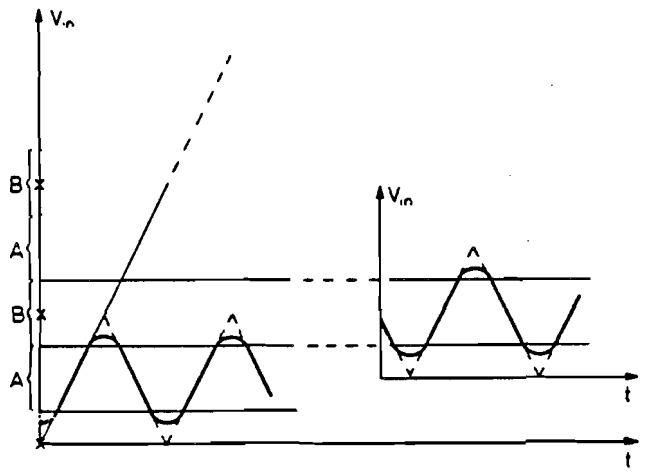

Figure 5.28 : Output waveforms of the double folding circuit

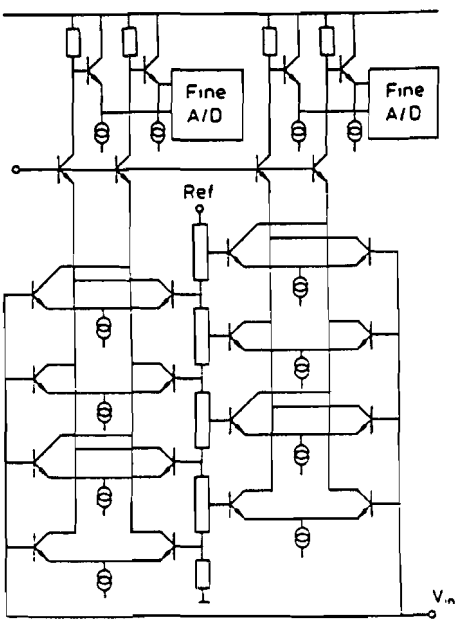

Figure 5.29 : Practical double folding circuit arrangement

of one differential amplifier pair. All other pairs are overdriven so no interaction on the output signal is obtained. One drawback of this connection of differential amplifier pairs is the large bias currents which flow through

the collector resistors. These bias currents can cause extra offsets should the matching of the tail currents of the differential amplifiers or the matching of the resistors not be good enough. Therefore, the number of differential amplifier pairs which can be combined in this way is limited. The two fine quantizer systems are fully differential. To avoid an extreme loading of the double folding system by the two fine quantizer stages emitter followers are added.

5.9.2 Fine quantizer stages

The rounding of the folding signals which are applied to the two fine quantizer systems does not result in an increase in the number of comparators in these systems. In Fig. 5.30 the quantization of the non-linear output signal at one of the outputs of the folding circuit is shown. Suppose an ideal

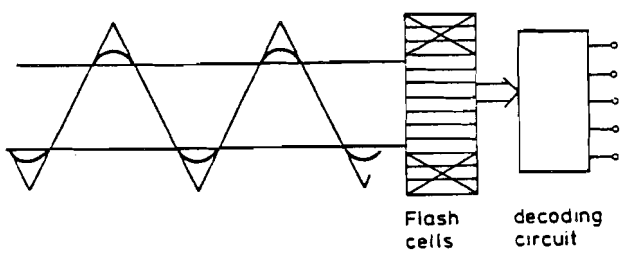

Figure 5.30 : Fine quantization of a non-linear folding signal

triangular signal is generated by an ideal folding circuit. In this case $2n$ fine comparator cells are needed for quantization of the signal. Now apply the non-linear folding signal to the same fine comparator system. Due to the rounding of the signal a reduction in the useful linear range of the system is obtained. In practice this means that the number of effective comparator cells is reduced. At the point when the two non-linear folding signals are each other's complement, for each fine quantizer system the number of effective comparators is reduced by a factor two. This results in n effective comparators cells per branch. The $n/2$ units at the top and bottom shown in the figure can be deleted because they do not add significant information to the system. As a result in the two fine quantizer systems a total of $2n$ comparators are needed to quantize the two folding signals. No difference in the number of comparators between an ideal folding system and the double folding system is found.

5.9.3 Delay-error correction

In Fig. 5.31 the two fine quantizer input signals are shown. In the top part

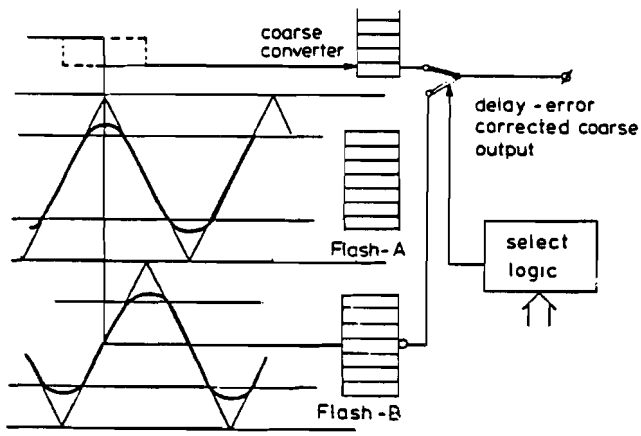

Figure 5.31 : Two fine quantizer input signals

of Fig. 5.31 the switching of the coarse bits is shown. The dashed boxes show the maximum switching time uncertainty which can be corrected by the delay-time correction system. The exact switching of the coarse bits must coincide with the switching of the middle comparator of the second fine comparator array. Differences in switching moments occur because the folding signal and the coarse quantizing signal pass through different amplifier stages. These delays can introduce erroneous output codes which, is not allowed. A system whose basic operation is shown in Fig. 5.31 overcomes this problem. In principle, the two fine quantizers contain all the important information needed for the delay correction. The only additional information which is required is the coarse region in which the fine quantization occurs. This information is determined by the coarse quantizer, but the exact moment of transition of the coarse bit is not transferred to the output as digital data. A logic selection circuit now determines the weak code combinations. Those MSB bits which have to be corrected are in turn determined. A correction is obtained by inserting the zero crossing information of the second fine quantizer as shown in Fig. 5.31 instead of the coarse code information. An exact and corrected output code is now obtained. In the figure the second fine quantizer is denoted as "flash-B". A time correction equal to plus or minus half the coarse region can be obtained.

5.9.4 Complete double folding A/D converter

On a 3x4.2 mm chip area an 8-bit A/D converter has been implemented using a standard bipolar process having double metal interconnections. The performance obtained is shown in Table I. The chip contains an input amplifier

Resolution	8 bits
Maximum analog input freq.	6 MHz
Input voltage range	1 V_{p-p}
Maximum clock frequency	20 MHz
Digital output signals	ECL compatible
Supply voltage	5.2 V
Supply current	100 mA
Chip size	3×4.2 mm^2
Differential phase	0.5 degree
Differential gain	1.5%
(No external sample-and-hold circuit required.)	

Figure 5.32 : Converter data

and digital output buffers.

5.10 Folding and interpolation systems

One drawback of the double folding converter system is the accurate matching between the coarse and fine quantizers which is needed to avoid missing codes. The two fine quantizers also have a matching requirement at high frequencies. This problem is introduced by the rounding of the folding signals at high frequencies. At that moment the rounded signal undergoes an amplitude-limiting action because of the limited practical bandwidth of a system.
The problems caused by the rounding of the triangular waveform at higher frequencies can be avoided by not quantizing these waveforms in amplitude. In that case several folding signals with suitable offsets are required to ensure that there is always at least one folding signal that is close to its zero crossing. Each folding signal has to be generated by its own folding circuit. This results in the same number of folding amplifiers as the number of levels which must be compared. Should an 8-bit circuit be designed, 255 folding

amplifiers are needed. No difference between a full-flash system and this folding system is found concerning input capacitance of the circuit. An important difference of this architecture with respect to the previously given folding systems is that only the zero crossings of the folding signals are used to determine the value of the least significant bits. This has the advantage that the results no longer depend on the shape of the folding signals. There is therefore no need to create an exactly linear triangular folding signal, even at low frequencies. The folding signals actually used in this converter do not resemble triangular signals at all except for a small, almost linear, region around the zero crossings. Also, the use of zero crossings eliminates the need for accurate handling of the input signals through the analog input folding system. Furthermore, the input range of the fine-flash converters does not need to match accurately the range of the folding signals. The folding principle is used in this system to obtain a multiple of zero crossings which can be detected by a single comparator per folding signal. In this way a reduction in hardware is obtained.
As already mentioned, the number of folding amplifiers is equal to the number of reference levels which must be compared with and thus the advantages of the folding architecture seem to be limited. However, this problem can be solved by creating only a small number of folding signals, and deriving the other folding signals by resistive interpolation between the outputs of two adjacent signals. In this case, the 32 folding signals necessary for the five least significant bits are derived from a four times interpolation between eight output signals of the folding encoder. An extension of this interpolation system to 10 or 12 bits by increasing the number of times the input signal is folded, the number of folding circuits, and/or the number of interpolated folding signals versus folding circuits, is relatively straightforward. This makes this architecture very suitable for high-resolution converters that require a large analog bandwidth. In practice, a maximum of eight times interpolation can be used to increase the resolution. The repetition rate with which the comparators need to detect zero crossings increases, but the time accuracy to perform a zero comparison remains the same as in a full-flash converter.

5.10.1 Folding and interpolation system description

In Fig. 5.33 a block diagram of the complete A/D converter system is shown. The input signal is applied to the buffer amplifier which drives the folding stages and includes the level-shift stage. The input signal amplitude in this

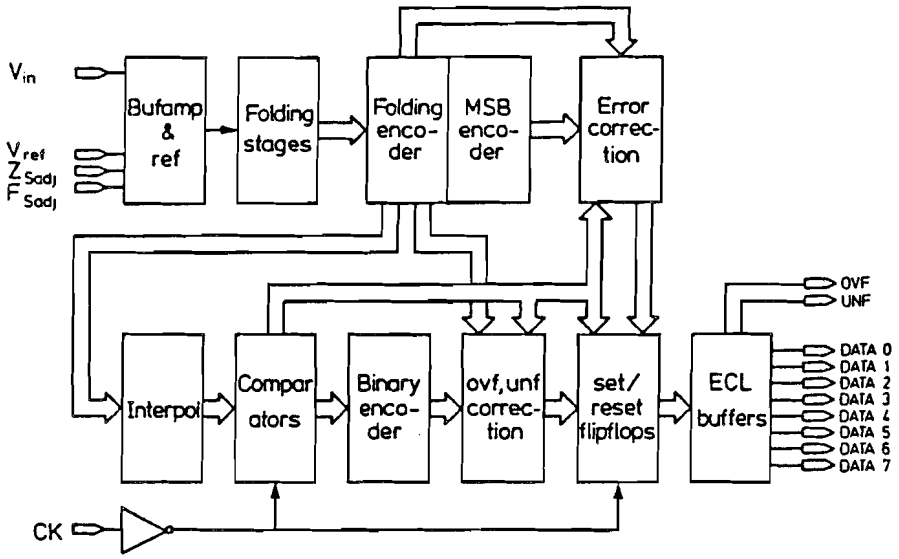

Figure 5.33 : Block diagram of folding and interpolation system

case is from 0 to -1 V. A reference current source generates across a resistive ladder the required reference voltage levels which are applied to the folding circuit block. In the folding block multiple amplifier/comparator stages generate multiple zero crossings which are applied to the folding encoder. This folding encoder is an analog ROM-like structure which combines a number of zero crossings into a repetitive folding signal. At the same time, signals are combined to obtain information about the most significant bits. This operation is performed in the MSB encoder part of the system.
The folding encoder output signals are applied to the interpolation circuit which generates, in this particular application, three additional folding signals for each output of the folding encoder. A four times interpolation is obtained in this way. The output signals of the interpolation circuit are applied to comparator stages which, on the command of the sampling clock, determine the position of their respective input signals with respect to zero. A circular thermometer-like output code is obtained (see Fig. 5.34). This circular output code is converted into a binary form using a binary encoder ROM structure. The outputs of this ROM encoder are the least significant bits of the converter. Information from the circular fine code is used in the error correction block to correct for inconsistencies (e.g. caused by different delays between the coarse and fine zero crossing/encoding/comparison blocks) in the most significant bits before they are applied to the set/reset

THE NUMBERS 0–7

	Thermometer	Circular
0	0 0 0 0 0 0 0	0 0 0 0
1	0 0 0 0 0 0 1	0 0 0 1
2	0 0 0 0 0 1 1	0 0 1 1
3	0 0 0 0 1 1 1	0 1 1 1
4	0 0 0 1 1 1 1	1 1 1 1
5	0 0 1 1 1 1 1	1 1 1 0
6	0 1 1 1 1 1 1	1 1 0 0
7	1 1 1 1 1 1 1	1 0 0 0

Figure 5.34 : Thermometer and circular code representation

flip-flop blocks which drive the ECL output buffers. At the same time, from the folding encoder, overflow and underflow information is used to set the output signals to ZERO when the underflow bit is tripped, or to ONE when the overflow bit is activated. This information overrides the information available in the fine code when overflow or underflow is activated. Using this system avoids large code transitions when the converter is overdriven. An accurate clipping at zero and full scale is also obtained.
The clock driver supplies the sampling clock to the different points in the system and does not increase the timing uncertainty. The gain in the clock driver speeds up the clock and makes the system less dependent on noise.

5.10.2 Folding circuits

In the folding block the input signal is compared with 64 reference voltage levels. This folding system consists of eight blocks, each with eight folding amplifier stages, forming in this way the 64 level comparison circuits. Each amplifier stage is responsible for the generation of one period of a folding signal.
When, for example, 128 reference voltages are used, a folding scheme consisting of eight blocks, each with 16 folding amplifier stages, can be used to increase the resolution of the system to 9 bits. With an eight times interpolation used after the folding encoder, a 10-bit converter is feasible.
In Fig. 5.35 an example of three coupled folding amplifier stages is shown.

The differential pairs Q_1/Q_2, Q_3/Q_4, and Q_5/Q_6 compare the input voltage

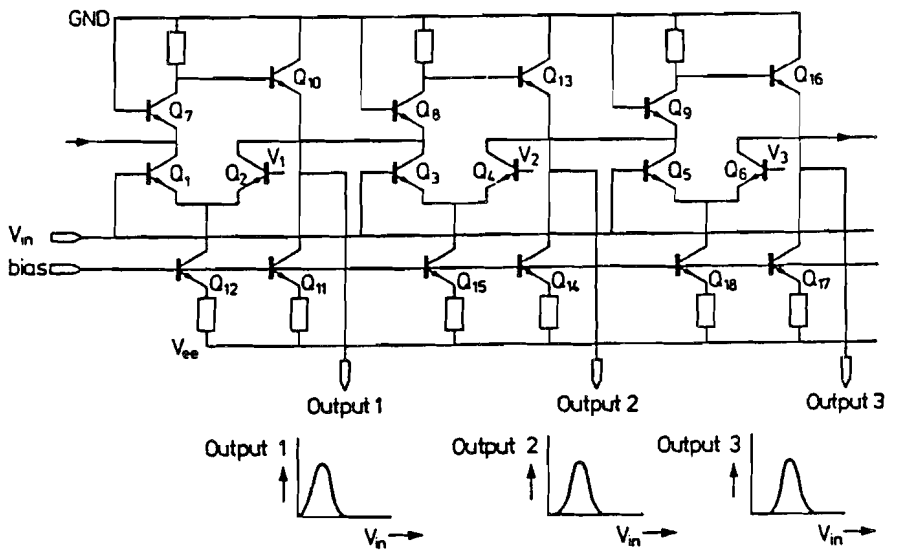

Figure 5.35 : Folding amplifier circuit

with the reference signals V_{r1}, V_{r2}, and V_{r3}. in addition, the collector of Q_2 is cross coupled with the collector of Q_3. The same is true for Q_4 and Q_5. Cascode stages Q_7-Q_9 are added to minimize the parasitic substrate capacitance and to maintain an equal collector-base voltage for all cascode stages in the folding amplifiers. The capacitances in the collectors of Q_7-Q_9 remain more constant and vary identically over the different stages.
The basic function performed by the folding block is the conversion of an increasing (or decreasing) input signal into a number of bell-shaped output signals V_{out1}, V_{out2}, and V_{out3}, which have different V_{in} offsets. Adjacent output signals are complementary near their zero crossings, which results in a full differential operation of the system. This can be explained as follows. Suppose the input signal increases from a level below V_{r1}, with V_{r1} being the smallest and V_{r3} being the largest value of the three reference voltages. The differential tail currents supplied by Q_{12}, Q_{15}, and Q_{18} flow through transistors Q_2, Q_4, and Q_6, respectively. As a result V_{out1} is high and V_{out2} and V_{out3} are low. When the input voltage reaches V_{r1}, the current through Q_2 and therefore through Q_8 decreases, and the current through Q_1 and Q_7 increases, in such a way that V_{out1} and V_{out2} show a differential output voltage change equivalent to the complementary output voltage variation of a differential pair. The same situation is found for V_{out2} and V_{out3} when the

input voltage equals V_{r2}. The bell-shaped output signals which are finally found at the output terminals differ in time by the length of time the input signal needs to change from V_{r1} to V_{r2} to V_{r3}.
The operation of the circuit is valid as long as no interaction exists between the coupled differential pairs due to large differences between the reference voltage sources V_{r1}, V_{r2}, and V_{r3}. It can be shown that differences of 120-150 mV between the reference voltage levels give some interaction but do not influence the operation of the folding stages in a negative way.
Comparison of the input signal level with the reference level is still performed by a single differential pair, giving a possible system implementation with low offset voltages. From the folding amplifier stages 64 output signal lines are supplied to the folding encoder circuit.

5.10.3 Folding encoder circuit

The folding encoder circuit combines the 64 signals from the folding amplifiers into eight complementary output signals. Each folding signal consists of two complementary signals, and one such signal is created by concatenating the outputs of, for example, the odd stages in a row of folding stages. In Fig. 5.35 this would be V_{out1}, V_{out3}, V_{out5}, etc. The complementary signal is created by concatenation of V_{out2}, V_{out4}, V_{out6}, etc. Other folding signals are generated by similar rows of folding stages, but with slightly different V_r to create an offset between the folding signals. This is achieved by interleaving the connections of the V_r on the resistive divider: folding stage 1 for folding signal 1 is connected to tap 1, folding stage 1 for folding signal 2 is connected to tap 2, folding stage 1 for folding signal 3 is connected to tap 3, and so on. In case of eight folding signals, folding stage 2 of folding signal 1 is then connected to tap 9. In order to avoid confusion, folding stages are numbered according to their connections to the reference voltage ladder. Folding stage 1 and folding stage 17 therefore generate subsequent periods of the same folding signal.
The lower part of Fig. 5.36 shows the combinatorial circuit which combines the outputs of the different folding stages into folding signals. The input and output waveforms associated with this circuit are shown in Fig. 5.37. Here the individual outputs of folding amplifiers i, i+16, and i+32 are shown in the top part. The lower part of the figure shows the combined output signal which is a concatenation of the bell-shaped signals.
Returning to the top part of Fig. 5.36 we see that the MSB and MSB-1 signals can also be generated by a proper combination of the folding ampli-

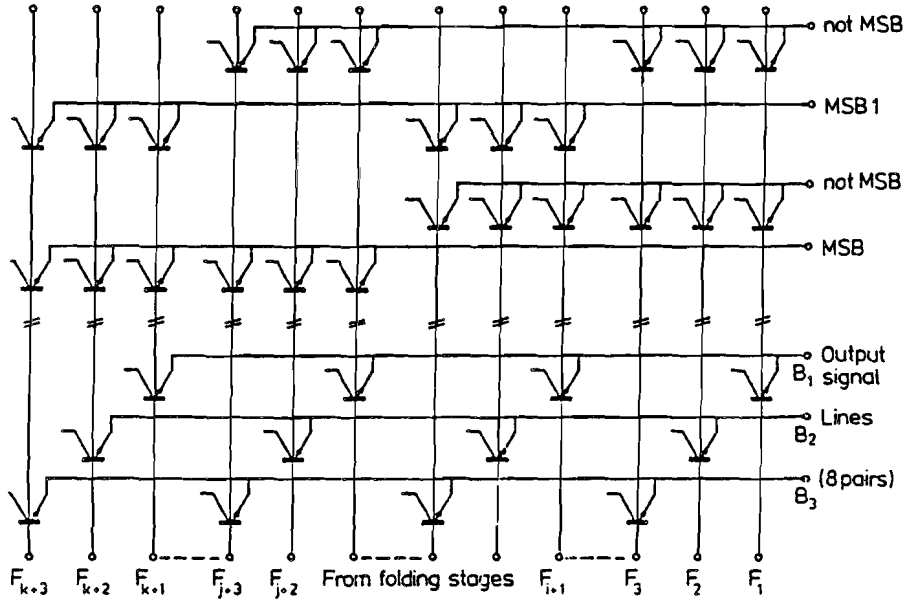

Figure 5.36 : Folding encoder circuit diagram

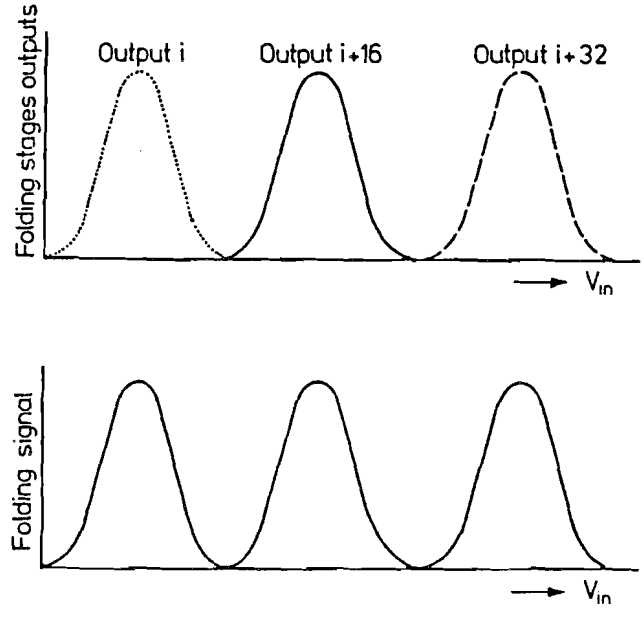

Figure 5.37 : Input and output signals of the folding encoder

fier outputs. Up until half the reference voltage the not-MSB signal is kept high and the MSB signal line is kept low by a combination of the bell-shaped

folding amplifier signals. At half the reference voltage level, a single differential amplifier pair switches and in this way determines the MSB change. No extra offsets or accuracy problems are found relative to the fine conversion signals which are generated in a later stage of the system.
A similar operation can be performed for the MSB-1 signals. Moreover, the MSB-2 signal is equal to the output signal in the lower part of the circuit which combines stages 0, 16, 32, 48.

5.10.4 Interpolation circuit

Up to this point, 64 reference levels have been converted into a repetition of zero crossings that could drive eight differential comparator stages, and thus generate three least significant bits. Together with the three MSBs this corresponds to a 6-bit system. To increase the resolution to 8 bits without adding folding stages, a four times interpolation of zero crossings is introduced at the outputs of the folding encoder. In Fig. 5.38 a simple resistor network which performs the interpolation of zero crossings is shown. For the 32 folding signals created this way, 32 differential comparators are

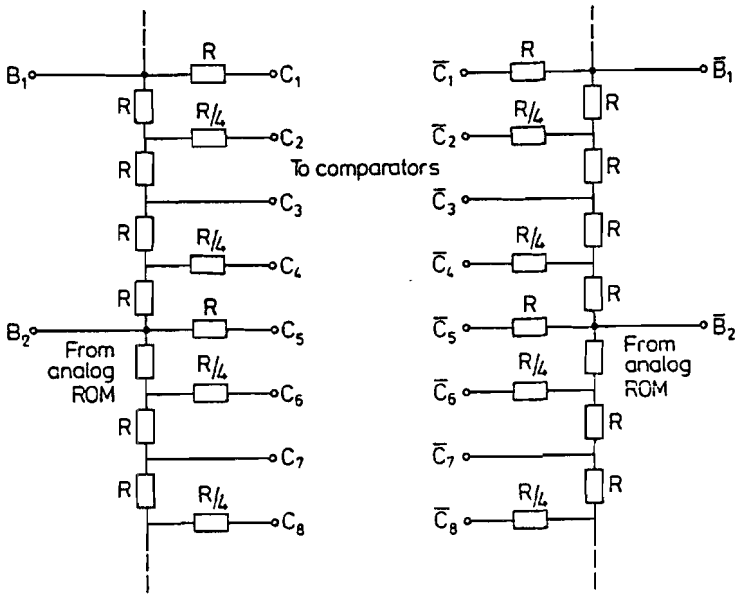

Figure 5.38 : Interpolation circuit diagram

needed to derive the five least significant bits.

Because the interpolation network is driven from voltage-follower stages, the output impedance of the network which drives the comparators varies from zero to R (R is the value of the interpolation resistors). The capacitive load of the comparator input stages on the interpolation network results in a variable signal delay which can easily be more than is allowed in this system (12 psec). Therefore, additional resistors of values R and $\frac{R}{4}$ are added in series with some outputs to adjust the output impedance of the interpolation network equal to R. All comparator stages now have an equal signal delay. A cross-coupling between the beginning and the end of the interpolation network is needed to obtain interpolated signals "around the corner", which is necessary because of the repetitive properties of the folding signal.
In Fig. 5.39 an example of two folding encoder output signals and the interpolated signal are shown. Although the interpolated signal is not exactly

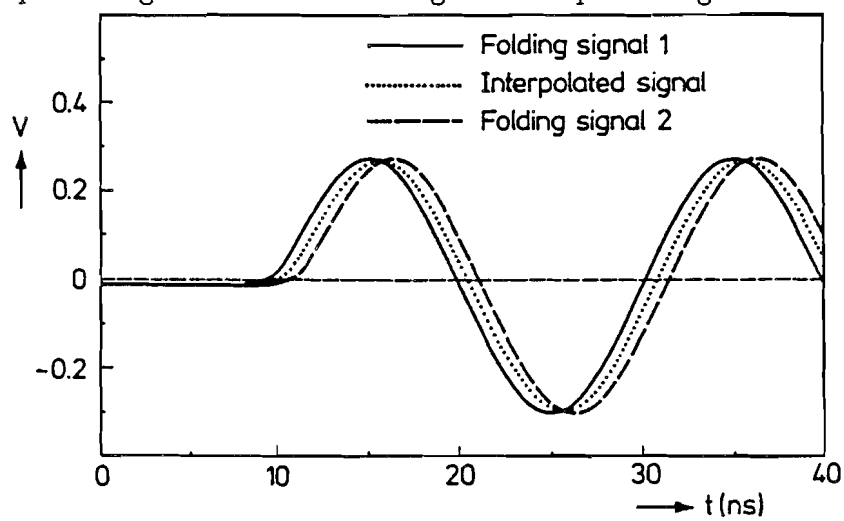

Figure 5.39 : Interpolation circuit output signals

equal to the input signals, the zero crossings which contain the relevant information about the input signal are at the correct positions.

5.10.5 Comparators

Most flash converters use clocked flip-flops for the analog comparators. The basic circuit diagram of such a comparator stage is shown in Fig. 5.40. The operation of this circuit is as follows. When the clock signal is high, then transistors Q_1 and Q_2 are conducting and the input signal is amplified by this amplifier stage with R_1 and R_2 as load resistors. A decision is made when

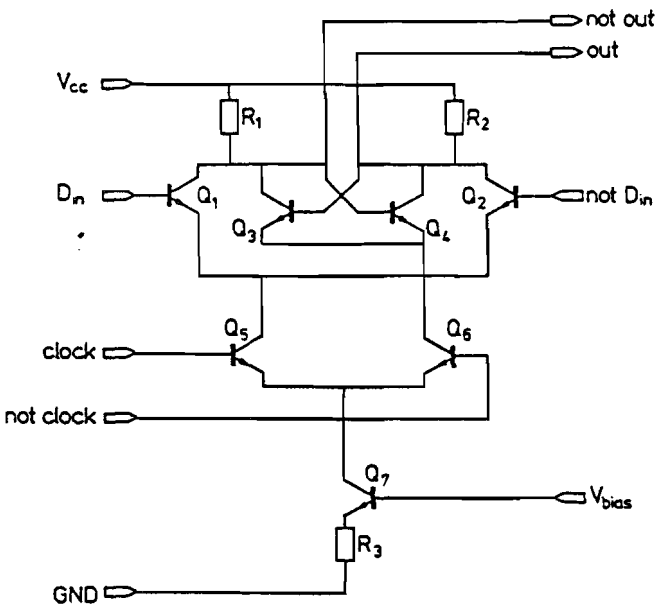

Figure 5.40 : Basic clocked flip-flop comparator circuit

the not-clock signal is made high. This simple circuit shows an extremely good performance. However, every time data has to be entered into the flip-flop, base charge must be applied to Q_1 and Q_2. These transistors were switched off during the decision-making and are switched on again to apply input information to the collectors of Q_1 and Q_2. The base charge results in large charging currents flowing through the interpolation network. These charging currents disrupt the exact zero-crossing information which results in a reduction in effective bits. To overcome this problem a different type of clocking scheme is used. The "high clocking" is shown in Fig. 5.41. In this circuit the input amplifier stage is continuously biased. Kickback effects from the sampling clock are reduced considerably, while the "cascoding" by the clock switches Q_5, Q_6, Q_7, and Q_8 of the input signal and the comparator output signal reduces the Miller effect of the collector-base capacitance of the amplifier transistors Q_1 and Q_2.

5.10.6 Circular-to-binary encoder

Because of the repetitive effect in the fine converter, a circular code, instead of a linear thermometer code, is obtained. In Fig. 5.42 examples of the

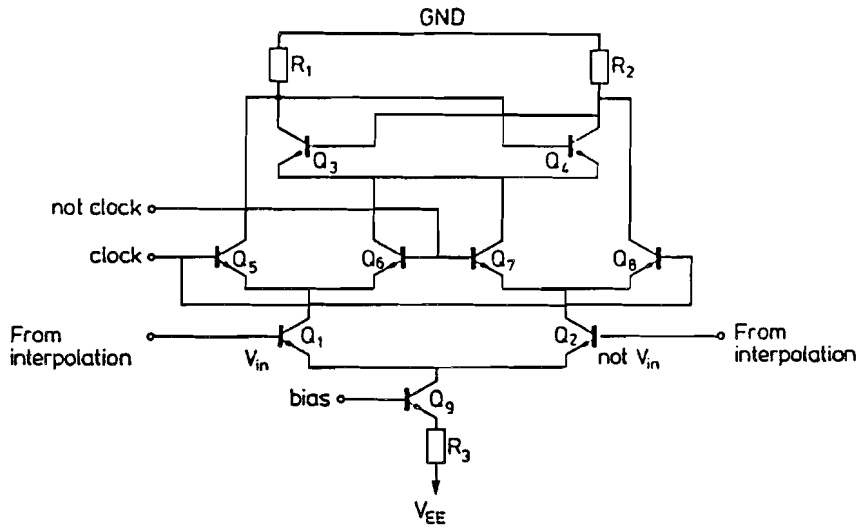

Figure 5.41 : Comparator with "high clocking" operation

thermometer and circular code are shown. When decoding such a code,

CODE REPRESENTATION OF THE NUMBERS 0–7

	Thermometer	Circular
0	0 0 0 0 0 0 0	0 0 0 0
1	0 0 0 0 0 0 1	0 0 0 1
2	0 0 0 0 0 1 1	0 0 1 1
3	0 0 0 0 1 1 1	0 1 1 1
4	0 0 0 1 1 1 1	1 1 1 1
5	0 0 1 1 1 1 1	1 1 1 0
6	0 1 1 1 1 1 1	1 1 0 0
7	1 1 1 1 1 1 1	1 0 0 0

Figure 5.42 : Thermometer and circular code representation

the transition between a group of ONEs and a group of ZEROs must be determined first. In the case of the circular code this function is performed by an EXCLUSIVE-OR function. The output of the EXCLUSIVE-OR function is applied to a ROM structure which converts the transition into a binary

code (Fig. 5.43). The differential output signals of the encoder ROM are

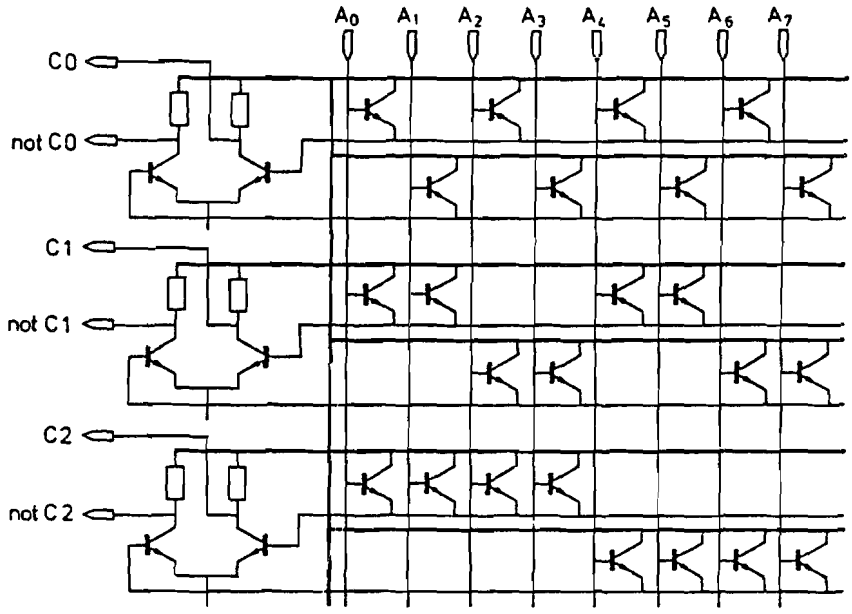

Figure 5.43 : Binary encoder ROM

applied to differential amplifier stages which restore the current mode logic level.

5.10.7 Timing-error correction between MSB, MSB-1, and LSBs

Although care has been taken to ensure equal delays for the MSBs and the LSBs in the converter, noise and decision uncertainties at the zero crossings of the MSB comparators can result in erroneous output codes. To overcome this problem an error correction system is included. This correction is achieved by checking the outputs of a set of folding amplifiers that have the maximum output voltages for input signal values where such errors can occur, i.e., near transitions of the MSBs. If such a folding amplifier output indicates that the signal is in the transition region, then the MSBs are replaced by an appropriate value based on the most significant bit of the LSB bits. Whether one of the MSBs is replaced by the most significant bit of the LSBs or by its complementary value depends on the transition region of the input signal. In Fig. 5.44 these dangerous regions are shown. A timing

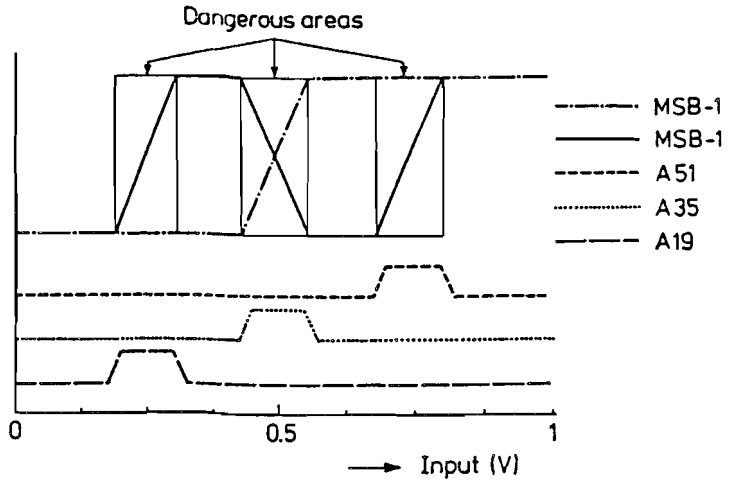

Figure 5.44 : Dangerous regions of MSB and MSB-1 signals

error correction corresponding to $\pm\frac{1}{16}$ of the full scale can be obtained with this method.
A similar problem occurs at the top and the bottom of the input range. Because of the circular properties of the folding signals, the MSB bits saturate at the end of the input range while the LSBs wrap around the corner. This may result in large code errors, which is not allowed. For example, with five LSBs and the three MSBs an input signal decreasing from a value corresponding to the output code "00000010" would go through the following output codes:"00000010," "00000001," "00011111," "00011110," etc. These large signal glitches are not found in the input signal and therefore must be limited to a maximum or minimum code depending on "overflow" or "underflow" indication. A similar correction as described for the MSBs is performed to force the output code to ONEs in the case of overflow and ZEROs in the case of underflow.

5.10.8 A/D converter implementation

The A/D converter was implemented in an advanced oxide isolated bipolar process. (Signetics HS3). Important device parameters are shown in Fig 5.45. In the final system design one of the design goals was a minimum number of external components to operate. The total die size of the A/D converter function needed only 3.2x3.8 mm^2. Although this is a small die compared to a full-flash converter, delays over wires of lengths comparable to

H_{fe}	170
Emitter Size	$2 \times 6\ \mu m^2$
F_t	9 GHz
C_{be}	22 fF
C_{cb}	43 fF
C_{cs}	68 fF

Figure 5.45 : NPN device parameters

the die size are still unacceptable. A 1 psec delay over a wire corresponds to a length of 200 μm, supposing the transmission speed is $\frac{2}{3}$ the speed of light on the oxide/air interface. However, only delay differences in identical operations in the system influence the high-frequency performance. These delay differences can be kept small using proper layout structures. For example, tree-type wire structures as shown in Fig. 5.46 are used to ensure virtually identical path lengths for clock and signal distribution. A die photograph is

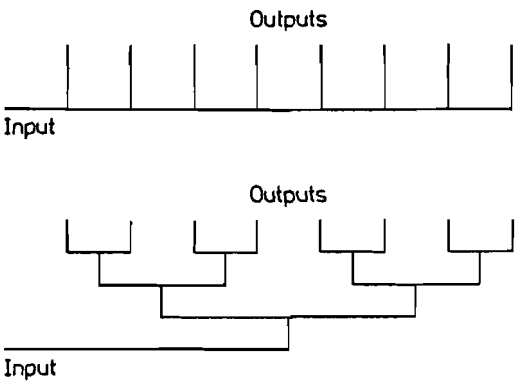

Figure 5.46 : Tree-type wire structures and conventional wire layout

shown in Fig. 5.47

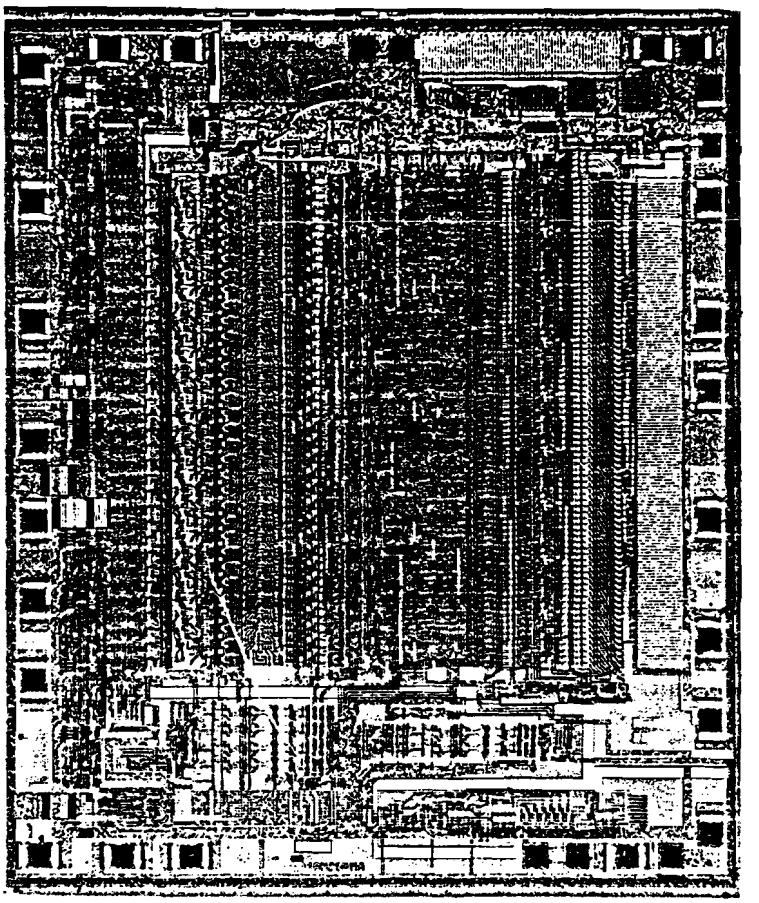

Figure 5.47 : Die photograph

5.10.9 Measurements

To verify the performance of the A/D converter a test set-up using an A/D-D/A loop as shown in Fig. 5.48 was used. In this loop a D/A converter is used to reconstruct the analog value. The performance of this D/A converter must be much better than the performance of the A/D converter to be measured. If DC tests are carried out a 14-bit linear low-speed D/A of the type TDA 1540 can be used. The D/A converter can be hooked up in such a way that the input signal to the A/D converter being tested and the output signal of the D/A converter are in counter phase. Using a half re-

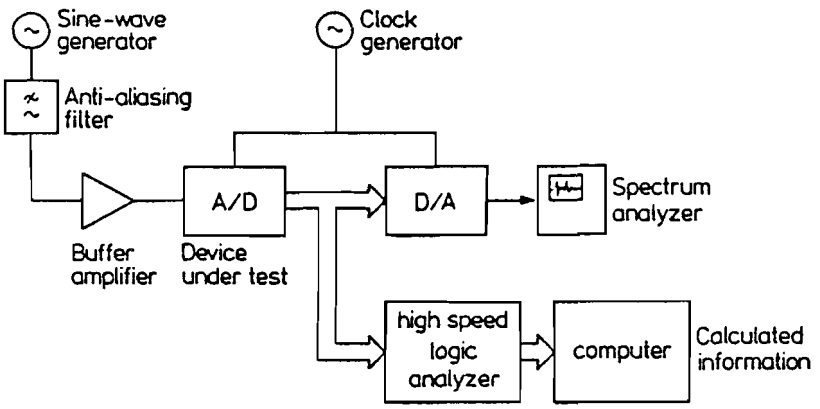

Figure 5.48 : A/D-D/A converter test set-up

sistor bridge between the input and output of this system the non-linearity can be easily measured and recorded using a plotter. No additional accurate elements are needed in this test procedure. The result of the linearity measurement is shown in Fig. 5.49. In dynamic tests a high-performance

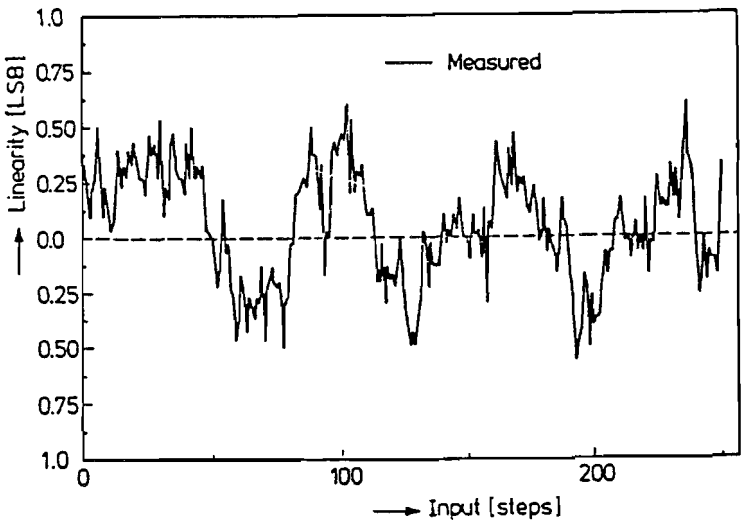

Figure 5.49 : Linearity measurement result

high-speed D/A converter is needed. Because of the availability of a slower

speed D/A converter subsampling is used to allow measurement results up to 60 MHz analog input signals. The measured data are converted to the overall bandwidth of the converter at the used measurement condition. A result of the effective bits as a function of frequency is shown in Fig. 5.50 The figure shows that the converter has an analog bandwidth of 40 MHz. At

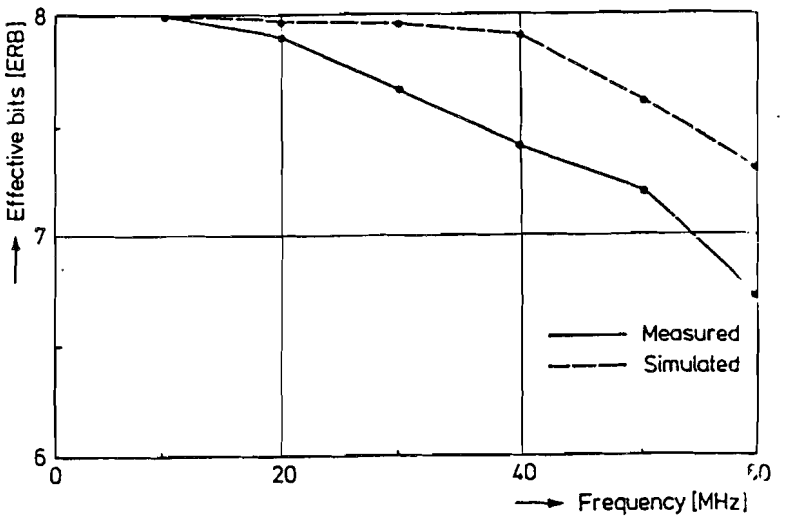

Figure 5.50 : Effective bits as a function of input frequency

this frequency the effective resolution is reduced by 0.5 LSB with respect to the low-frequency resolution. Input signals with a low distortion (below 60 dB) and a sampling clock with an effective jitter below 12 psec are necessary. Verifying the clock jitter is a problem in itself. Further performance data are given in Fig. 5.51. The results of the measurements show that with a folding architecture a high-speed high-performance A/D converter can be designed. This converter needs a moderate die size and consumes less than 1 W of power.

5.10.10 Conclusion

In this chapter high-speed full-flash, two-step and folding A/D converters have been discussed. In time-continuous systems not much difference in problems between a bipolar or an MOS circuit solution is seen. When however time-discrete solutions are used, then only special MOS systems exist because of the special character of this technology.

Resolution	8 bits
Linearity	± 0.5 LSB
Conversion Rate	100 MHz
Effective Resolution Bandwidth	40 MHz
Input Signal Voltage	0 to -1 V
Input Capacitance	2 pF
Power Supply	-5.2 V
Power Dissipation	800 mW
Output Logic Levels	ECL 10K compatible
Outputs	8 data bits, and overflow & underflow
Built-in Clock Driver	
Built-in Input Buffer	
Built-in Voltage Reference	
Die Size	3.2x3.8 mm2
Package	24 pin

Figure 5.51 : A/D converter performance data

A special type of two-step system which uses a continuous coarse-fine operation is discussed. The advantages of folding systems over full-flash types without a sample-and-hold amplifier at the input are clearly shown. With a lower power consumption and a smaller die size the performance of the folding-type converter is better than the best-known full-flash type. Comparator/ amplifier stages can run at higher current levels, increasing the analog bandwidth of the system. This larger bandwidth results in a smaller signal-dependent delay, which results in a lower third-order distortion. Design criteria for full-flash or folding-type converters are identical concerning the signal-dependent delay. In the next chapter a detailed analysis of the signal-dependent delay will be given.

Chapter 6

Signal delay in limiting amplifiers

6.1 Introduction

In most A/D converters the input signal is applied to an amplitude-limiting circuit. This amplitude-limiting circuit can be a differential amplifier stage or the input stage of a comparator. The amplitude of the input signal is usually much larger than the linear range of the input amplifier stages. In this way a limitation of signals for the individual amplifier stages occurs. This amplitude limitation results in variations of the delay times of the zero crossings of the differential stages. This can be explaned in the following way. When a sine wave is applied at the input of the A/D converter then it looks as if this sine wave is cut into pieces with a variable slope. This slope depends on the level at which the input signal is equal to a reference voltage level. The variable slope introduces a variable delay of the zero crossing of the output signal. These delays are accordingly signal-slope-dependent. As a result, a non-linear distortion of the input signal occurs while it travels through the A/D converter system. The moments at which an ideal amplifier would show a zero crossing are shifted in time. These time shifts result in errors in the output code of the A/D converter. This delay variation is caused by the frequency limitation which is always present in practical amplifier stages. This distortion occurs in particular in bipolar amplifier stages which have a limited linear range. MOS amplifier stages have a larger linear range because of the much higher threshold voltage of the individual devices with respect to a bipolar transistor. A simple calculation and design model will

be presented in this chapter. For additional information see [36].
A/D converters which use a sample-and-hold amplifier at the input are less sensitive to this slope-dependent delay phenomenon. In reference [37] the improvements in performance of flash-type A/D converters preceeded by a high-speed sample-and-hold amplifier are shown. The time constant with which the sampling of the analog signals occurs can be made smaller than is the case with the large number of amplifier stages used in parallel or folding types of converters.

6.2 Delay calculation model

A simple model which represents the non-linear behaviour of an amplifier pair with a frequency-limiting circuit is modeled in Fig. 6.1 The model

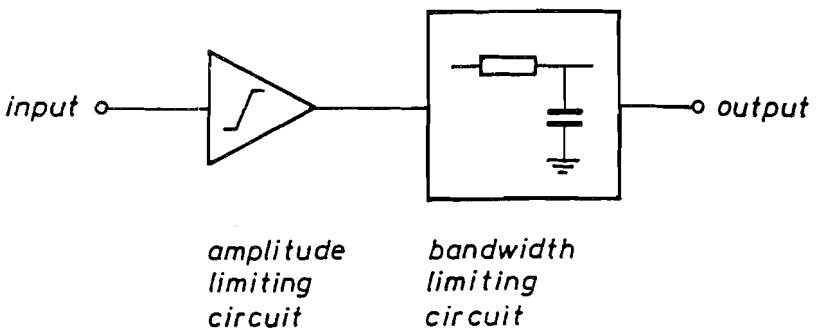

Figure 6.1 : Simple non-linear model of a limiting amplifier stage

consists of an amplitude-limiting stage followed by a bandwidth-limiting circuit. The amplitude-limiting circuit is modeled by a linear transfer curve which saturates on both sides without any smooth transitions. Although practical amplifier stages show a certain smoothing in saturation, this simple model turns out to be good enough for understanding the problem and deriving design requirements for the amplifiers. The bandwidth limitation is modeled by a simple *RC* network. Now assume that the input signal is increasing with a constant slope within the linear region of the amplitude-limiting circuit. Then the first part of the output signal of the *RC* network equals the response of an *RC* network to a ramp function (see Fig. 6.2). After the output signal of the amplitude-limiting circuit reaches its maximum value, the output of the *RC* network equals the response to a step function. During normal operation of an A/D converter, the input signal source, which can be a sine wave, overdrives the differential comparator amplifier stages.

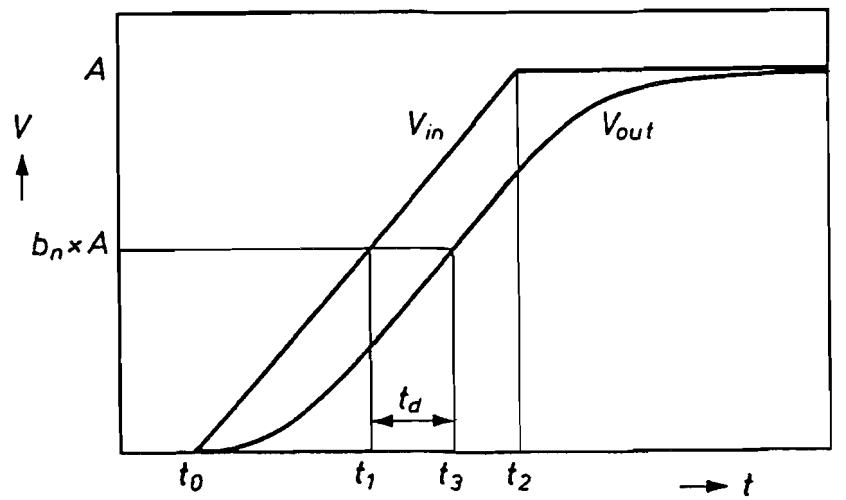

Figure 6.2 : Output signal of an amplitude-limiting circuit with a ramp input signal

When the input signal passes a differential stage at the zero crossing of the signal, a waveform like an input step is applied to the RC network. The delay in this case equals the response of an RC network to a step input signal. This delay, at half the output signal value, equals about 0.7 RC. When the input signal reaches the tips of the sine wave, a signal which can be modeled by a ramp signal is applied to the RC network. In this case the delay will become RC. The result of this operation is that, depending on the slope of the input signal, the output zero crossings will have a variable delay, which changes from $0.7RC$ to RC when the signal changes from maximum to minimum slope. The input slope variations occur because at the high end frequency range a sine wave is always compared with the reference levels. The anti-alias filter which must precede a practical converter to avoid aliasing performs this signal filtering. This variable delay will cause signal distortion, which is not allowed. A more exact analysis of this phenomenon will be presented in the next section.

6.3 Variable delay calculation

In a practical situation a step input response is never obtained. Therefore a ramp with variable slope is used to model the limited input signal. Using Fig. 6.2 the following notations for the variable signal delay are used:

V_{in} input signal
V_{fs} full scale value of the A/D converter
G_A amplifier gain
$V_{lr} = \frac{A}{G_A}$ input amplifier linear range
f_{in} input signal frequency
$f_b = \frac{1}{2 \times \pi RC}$ -3 dB bandwidth of the input amplifier
$\omega = 2 \times \pi \times f_{in}$
S slope of the A/D converter input signal
S_{out} slope of the output signal of the amplitude-limiting circuit
A maximum output voltage
b_n relative output voltage level at which the signal delay is determined
t_0 start time of the ramp signal
t_1 time at which the ramp signal reaches the level $b_n \times A$
t_2 time at which the output signal of the limiting stage reaches the maximum value A
t_3 time at which the output ramp-shaped signal reaches the level $b_n \times A$
$t_d = t_3 - t_1$

Suppose an input signal equal to

$$V_{in} = \frac{V_{fs}}{2} \sin \omega t \tag{6.1}$$

is applied to the input of the A/D converter. Because of the anti-alias filtering which is required at the input of an A/D converter this sine wave is a good model for an input signal at the high end of the input frequency band. The slope of the signal depends on the level at which the reference level crossing occurs. After differentiating the input signal we obtain for the slope of the signal

$$S = \frac{V_{fs}}{2} \times \omega \cos \omega t. \tag{6.2}$$

The input slope is increased by the gain factor G_A of the amplifier/ limiter circuit. As a result, the output slope which is applied to the RC network

becomes

$$S_{out} = G_A \times \frac{V_{fs}}{2} \times \omega \cos \omega t. \tag{6.3}$$

The output slope of the amplitude-limiting circuit can be compared with the slope of the ramp function of Fig. 6.2. This means that:

$$G_A \times \frac{V_{fs}}{2} \times \omega \cos \omega t = \frac{A}{t_2 - t_0} \tag{6.4}$$

The value of $\frac{A}{G_A}$ can be replaced by the linear input voltage range of the amplifier v_{lr}, so then equation 6.4 can be rearranged into:

$$t_2 - t_0 = \frac{2 \times V_{lr}}{V_{fs} \omega \cos \omega t} \tag{6.5}$$

Using Laplace transforms the response of the ramp signal applied to the RC network can be calculated. We obtain using the notations of Fig. 6.2:

$$V_{out}(t) = (\frac{t - t_0}{t_2 - t_0} \times A - \frac{RC}{t_2 - t_0} \times A \times (1 - \exp^{-\frac{t-t_0}{RC}}))U(t - t_0) \tag{6.6}$$

In this equation $U(t - t_0)$ is the unit step response.

$$-(\frac{t - t_2}{t_2 - t_0} \times A - \frac{RC}{t_2 - t_0} \times A \times (1 - \exp^{-\frac{t-t_2}{RC}}))U(t - t_2). \tag{6.7}$$

The time delay t_d between the input and output ramp signal can be expressed in the circuit parameters when the output signal crosses the amplitude level $b_n \times A$.
We obtain after some rearranging and inserting $t = t_3$:

$$b_n \times (t_2 - t_0) = (t_3 - t_0 - RC \times (1 - \exp^{-\frac{t_3-t_0}{RC}}))U(t_3 - t_0) \tag{6.8}$$

$$-(t_3 - t_2 - RC \times (1 - \exp^{-\frac{t_3-t_2}{RC}}))U(t_3 - t_2). \tag{6.9}$$

The time t_3 can be expressed as follows:

$$t_3 = t_0 + b_n \times (t_2 - t_0) + t_d. \tag{6.10}$$

Depending on the value of the time t_3, two cases can be distinguished:
a) $t_3 < t_2$ and
b) $t_3 \geq t_2$.
Inserting the boundary value $t_3 < t_2$ into equation 6.10 results in:

$$t_2 - t_0 > \frac{t_d}{1 - b_n} \tag{6.11}$$

Combining equation 6.5 and equation 6.11 and rearranging results in:

$$\frac{t_d}{RC} < 2(1 - b_n) \times \frac{V_{lr} f_b}{V_{fs} f_{in}} \tag{6.12}$$

Equation 6.12 determines the switching between case a) and b). Suppose $t_3 < t_2$, then only equation 6.8 is valid to express the output voltage. Inserting equation 6.10 into equation 6.8 results in:

$$t_d = RC \times (1 - \exp^{-\frac{b_n \times (t_2 - t_0) + t_d}{RC}}). \tag{6.13}$$

When $\cos\omega t$ equals 0 or 1, then using equation 6.4 a value for $t_2 - t_0$ of ∞ or $\frac{2 \times V_{lr}}{V_{fs} \times \omega}$ is obtained, respectively.
Inserting the value of ∞ for $t_2 - t_0$ into equation 6.13 gives:

$$t_d = RC. \tag{6.14}$$

Now an estimate of the switching point between case a) and case b) can be made. Inserting equation 6.14 into equation 6.12 gives the estimate:

$$\frac{f_{in}}{f_b} < 2(1 - b_n) \times \frac{V_{lr}}{V_{fs}} \tag{6.15}$$

When the slope of the input signal varies, the interesting parameter is the variation of the delay time with respect to the slope of the signal. Define:

$$t_d = RC - \delta t_d. \tag{6.16}$$

Proceed with case a):
Substitution of equation 6.16 into equation 6.13 results in the following relation between the input signal and the delay variation δt_d:

$$\delta t_d = RC \times \exp^{-\frac{2 \times b_n \times V_{lr}}{V_{fs} \times RC \times \omega \cos \omega t} + \frac{\delta t_d}{RC} - 1} \tag{6.17}$$

In Fig. 6.3 the variation of the delay as a function of the input signal slope is shown. In the figure V_{in} represents the input sine wave which is offseted by 0.5 V at which level the maximum slope is found. 0 and 1.0 V are the bottom and top parts of the sine wave respectively. The following values for the different parameters are substituted: RC = 200 psec
b_n = .5
V_{lr} = 160 mV

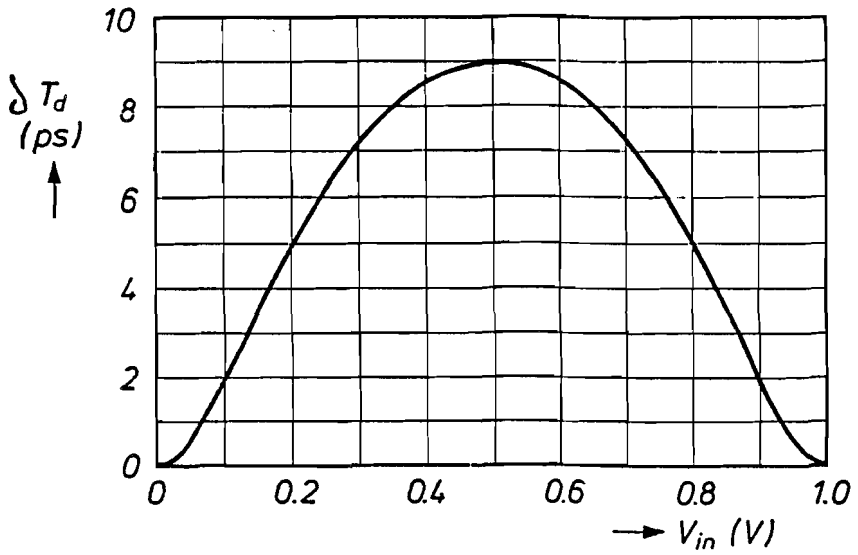

Figure 6.3 : Variation of the delay as a function of the input signal

$V_{fs} = 1$ V
$\omega = 2 \times \pi \times 50MHz.$
Inserting $\cos\omega t = 1$ into equation 6.17 results in a simplified expression for the maximum delay variation:

$$\delta t_d = RC \times \exp^{-2 \times b_n \times \frac{V_{lr} \times f_b}{V_{fs} \times f_{in}} + \frac{\delta t_d}{RC} - 1} \tag{6.18}$$

A further useful simplification is introduced by replacing $\frac{\delta t_d}{RC}$ by the normalized delay variation g.
Then equation 6.18 becomes:

$$g = \exp^{-2 \times b_n \times \frac{V_{lr} \times f_b}{V_{fs} \times f_{in}} + g - 1} \tag{6.19}$$

From equation 6.19 the following can be concluded for a minimum delay-variation:

a) The linear range V_{lr} of the input amplifier must be large.
b) A large amplifier bandwidth f_b is needed.
c) A small full scale range of the converter is needed.

The linear range V_{lr} of an amplifier is determined by the technology used. In a bipolar system without using emitter degeneration elements a linear range of about 120 to 180 mV is obtained. In MOS devices this linear range depends on the threshold voltage of the devices.
The bandwidth of a system is mostly determined by the dc bias condition of the amplifier stage. A large bias current results in a large power dissipation. Due to the complexity of the overall system, bias currents must be kept within certain limits, preventing the power dissipation of the total circuit from growing to excessive values. A small size high-frequency technology is needed to increase the analog bandwidth of the amplifier system. The minimum full-scale range of the converter is determined by the resolution and the matching of the input devices of the input amplifier. In bipolar devices in general a much better matching is obtained than is possible in an MOS technology. On the other hand, the noise generated in the input amplifiers determines the minimum tap spacing in a converter. In practice a minimum full scale value of 1 V can be used for an 8-bit converter in a bipolar technology.

To solve the implicit equation 6.19 a computer program is needed.
However, it is possible to simplify equation 6.19 by putting g $\ll$ 1:

$$g \approx \exp^{-2 \times b_n \times \frac{V_{lr} \times f_b}{V_{fs} \times f_{in}} - 1} \tag{6.20}$$

In Fig. 6.4 the relation between g and the ratio $\frac{f_b}{f_{in}}$ is shown.
Note that this figure is only valid for case a).

Proceeding to case b), the combined equation for the output voltage $V_{out}(t)$ to reach the crossing point $b_n \times A$ is obtained by adding equations 6.8 and 6.9. The result becomes:

$$(1 - b_n) \times (t_2 - t_0) = RC \times (\exp^{-\frac{t_3 - t_2}{RC}} - \exp^{-\frac{t_3 - t_0}{RC}}). \tag{6.21}$$

Inserting equation 6.10 for t_3 we obtain:

$$(1 - b_n) \times (t_2 - t_0) = RC \times (\exp^{\frac{t_2 - t_0}{RC}} - 1) \times \exp^{-\frac{b_n(t_2 - t_0) + t_d}{RC}}. \tag{6.22}$$

Rearranging the terms in equation 6.22 results in:

$$\exp^{-\frac{t_d}{RC}} = (1 - b_n)(\frac{t_2 - t_0}{RC} \times \exp^{b_n \frac{t_2 - t_0}{RC}} \times (\exp^{\frac{t_2 - t_0}{RC}} - 1)^{-1}. \tag{6.23}$$

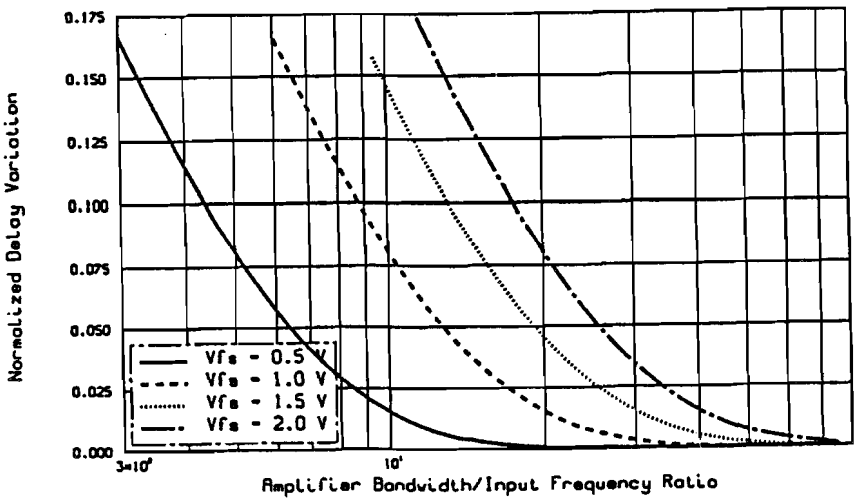

Figure 6.4 : Relation between the delay variation g and the ratio bandwidth/ input frequency

The limit value of $\frac{t_d}{RC}$ when t_2 reaches t_0 equals:

$$\frac{t_d}{RC} = -ln(1 - b_n). \tag{6.24}$$

Inserting a value of 0.5 for b_n gives $t_d = RC\ln(2)$. This value equals the delay of an RC time constant on a unity step response as expected.
A further simplification of formula 6.23 is obtained by inserting equation 6.16 and equation 6.5 for $\cos\omega t = 1$. After rearranging the terms we obtain for a maximum in the normalized delay variation:

$$g = 1 - \ln(\exp^{2\frac{V_{lr} \times f_b}{V_{fs} \times f_{in}}} - 1) + 2b_n \frac{Vlr \times f_b}{V_{fs} \times f_{in}} + \ln(2(1 - b_n)\frac{Vlr \times f_b}{V_{fs} \times f_{in}}). \tag{6.25}$$

In Fig. 6.5 the normalized delay variation ($g = \frac{t_d}{RC}$) for the combination of case a) and b) are shown as a function of the ratio between the amplifier bandwidth and the input frequency. The full-scale value of the converter is inserted as a parameter. The linear range of the input amplifier V_{lr} = 160 mV. This model is verified by extensive simulations at transistor level of chords of input amplifiers performing an A/D input signal operation.

These results can be used in an equation which will determine the third-order distortion in the converter system. This equation will be evaluated in the next section.

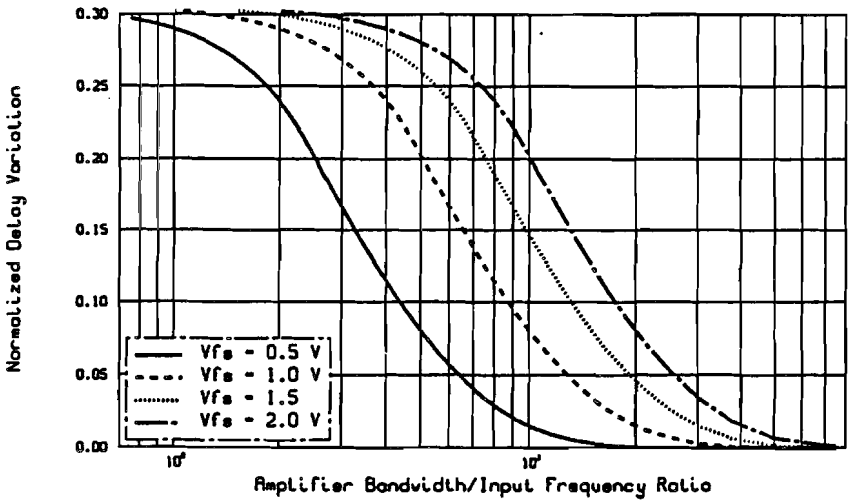

Figure 6.5 : Total normalized delay variation as a function of input amplifier bandwidth/input frequency

6.4 Distortion calculation

Suppose an input signal $V_{in} = \sin(\omega t + \psi)$ is applied at the input of the converter. In this formula ψ is an arbitrary phase shift introduced at the input to compensate for the various delays in the converter system. This phase shift is constant and independent of the slope of the input signal. At the output of the converter a digitized signal is found which follows the following equation:

$$V_{out} = \sin(\omega \times (t + \delta t)). \tag{6.26}$$

From Fig 6.3 it can be seen that a good approximation for the delay difference δt_d as a function of the input frequency is:

$$\delta t \cong -\delta t_d \times \mid \cos \omega t \mid . \tag{6.27}$$

The absolute value for the cosine is inserted because regardless of the signal polarity the delay must have the same sign. Inserting equation 6.27 into equation 6.26 results in:

$$V_{out} = \sin \omega t \cos(\omega \delta t_d \mid \cos \omega t \mid) - \cos \omega t \sin(\omega \delta t_d \mid \cos \omega t \mid). \tag{6.28}$$

Equation 6.28 can be simplified using series expansion and supposing that δt_d is small with respect to t. When only the first-order terms in the series

expansion are used, equation 6.28 becomes:

$$V_{out} = \sin\omega t - \cos\omega t \times \omega\delta t_d \mid \cos\omega t \mid . \tag{6.29}$$

A further simplification is obtained when $\mid \cos\omega t \mid$ is expressed in a Fourier series. We obtain:

$$\mid \cos\omega t \mid \simeq \frac{2}{\pi} + \frac{4}{3\pi}\cos 2\omega t. \tag{6.30}$$

Substitution of the series expansion from equation 6.30 into equation 6.29 results in:

$$V_{out} = \sin\omega t + \frac{2}{\pi}\omega\delta t_d \cos\omega t + \frac{4}{3\pi}\omega\delta t_d \cos\omega t \cos 2\omega t. \tag{6.31}$$

Reworking the product of $\cos\omega t$ and $\cos 2\omega t$ into a sum of cosine terms gives:

$$\frac{2}{3\pi}\omega\delta t_d \cos\omega t + \frac{2}{3\pi}\omega\delta t_d \cos 3\omega t. \tag{6.32}$$

Inserting this simplification into equation 6.31 results in:

$$V_{out} = \sin\omega t + \frac{8}{3\pi}\omega\delta t_d \cos\omega t + \frac{2}{3\pi}\omega\delta t_d \cos 3\omega t. \tag{6.33}$$

From equation 6.33 it is shown that the signal-dependent delay results in a third-order distortion of the input signal after the conversion takes place in an absolutely linear A/D converter.
The small cosine term can be included in the sine wave expression by substituting $\tan\eta = \frac{8}{3\pi}\omega\delta t_d$. This results in a small phase shift of the sine term, we obtain:

$$V_{out} = \sqrt{\tan^2\eta + 1} \times \sin(\omega t + \eta) + \frac{2 \times g \times f_{in}}{3 \times \pi f_s} \cos 3\omega t. \tag{6.34}$$

The third-order term is a direct expression for the distortion in the A/D converter. In Fig. 6.6 the distortion as a function of the ratio $\frac{f_s}{f_{in}}$ for the limited case a) is shown. This curve gives a general insight into the effective bits of a converter as a function of the ratio bandwidth/input frequency. The distortion of the system is shown in Fig. 6.7. Here again, V_{fs} is a parameter to get information about the distortion dependence of the full-scale range of the converter. Care must be taken in using the total distortion equation at the high-frequency end limit. It must be verified that the comparators or amplifiers at those high frequencies settle to the final signal value. Otherwise wrong conclusions are drawn.

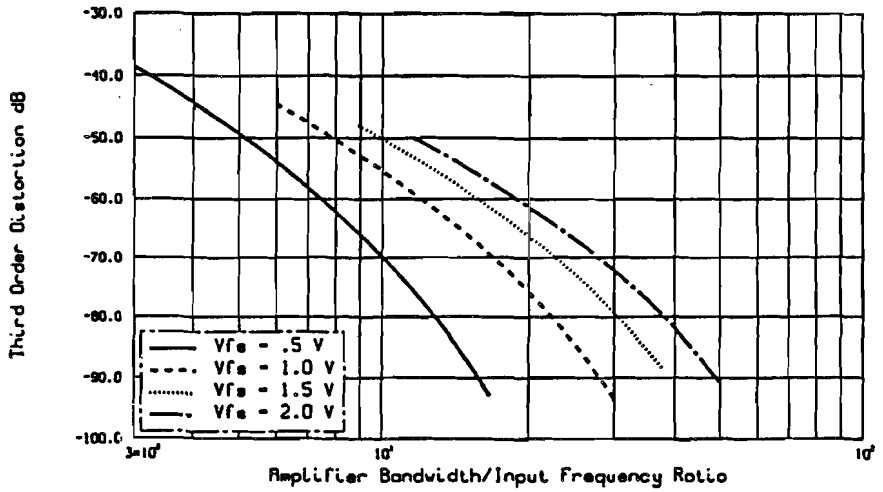

Figure 6.6 : Relation between distortion and bandwidth/input frequency ratio of an A/D converter

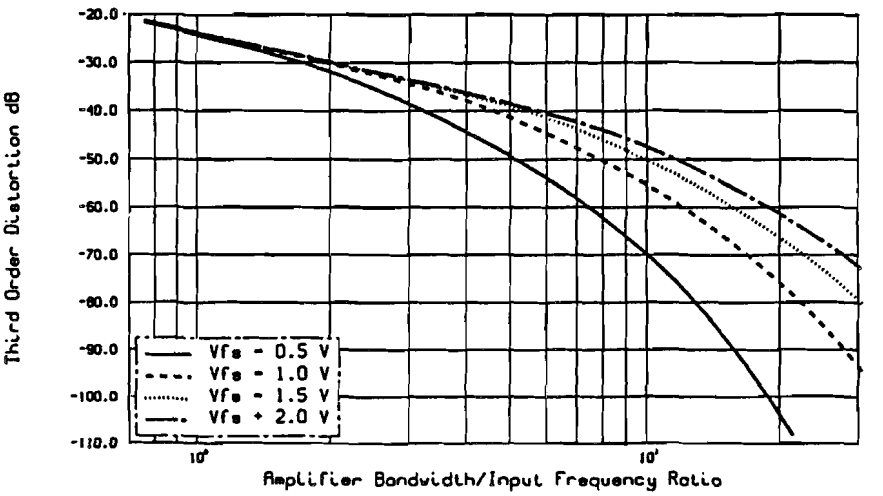

Figure 6.7 : Total distortion versus bandwidth/input frequency ratio of an A/D converter

6.5 Conclusion

In this chapter a generalized relation between amplifier bandwidth and maximum input frequency for an A/D converter is calculated. When no other distortion products due to ladder non-linearity etc. occur, then the given ex-

pressions determine the effective resolution bandwidth of a converter. There is no difference in analysis between a full-flash converter or a folding converter. The relations given are verified using extensive simulations on A/D converter circuits. These simulations are performed at transistor level. Furthermore, measurements on a flash-type A/D converter show the considerable increase in third-order signal distortion at high frequencies.

Chapter 7

High-accuracy A/D and D/A converters

7.1 Introduction

High-resolution monolithic A/D and D/A converters are subject to growing interest due to the rapidly expanding market for digital signal processing systems. An example of such a market is digital audio. The large dynamic range of a digital audio system requires converters with resolutions of 16 to 18 bits. Monolithic converters with such a high linearity are difficult to design and require special circuit configurations. The most simple types of D/A converters are obtained with pulse-width modulation systems. These systems require fast logic systems. In a pulse-width D/A converter structure an output low-pass filter reconstructs the analog signal and removes the modulation signal. Maximum speed of these types of converters is limited to the kHz range. The advantage of these systems is the small amount of accurate components which are needed to construct these converters.
In integrating types of converters an analog signal is reconstructed by integrating a current during a signal dependent time. The output signal of the converter is applied to a sample-and-hold amplifier. The sample-and-hold amplifier reconstructs the stepped quantized waveform. With a low-pass filter the final analog output signal is reproduced again.
With matched components (resistors, capacitors or transistors) it is possible to directly convert a digital number into an analog quantized signal. However, the limited accuracy with which components can be matched maximizes the resolution to about 10 to 12 bits. In that case a converter

still fulfills the linearity specification. Modifying the design can result in *monotonic by design* types of converters which do not have a $\frac{1}{2}$ LSB linearity specification but may have an excellent differential non-linearity specification.
In this chapter finally a special circuit configuration, called "Dynamic Element Matching" will be described. This technique combines an accurate passive current division with a time division method to obtain the very high accuracy needed in monolithic converters without using trimming techniques. This system is furthermore insensitive to element aging and remains accurate over a large temperature range and with varying elements. In references [38,1,2] examples of circuits realized in practice are given.
Furthermore an MOS solution in which currents are calibrated is introduced. This current calibration results in a very high matching accuracy without the need for an extra filtering operation to reduce the interchanging ripple.
At last self calibration schemes are shown, which use an additional cycle to calibrate the complete converter. During calibration, however, it is not possible to effectively use the converter in the system.

7.2 Pulse-width modulation D/A converters

In Fig. 7.1 an example of a pulse-width D/A converter is shown. The system consists of a digital buffer in which the input data is stored. This data is compared with a ramp signal which is generated by a counter operating with a clock frequency f. The digital comparator compares the buffer data with the ramp signal generated by the counter. When the counter signal is smaller than the buffer signal then the output of the comparator is low. At the moment the counter signal is equal or larger than the buffer signal then the comparator output is high. The output signal of the converter is a pulse width modulated signal. This signal is filtered by a low-pass output filter and the analog signal is reconstructed again. A simple calculation gives for the output signal:

$$V_{out} = \frac{T_x}{T} \times V_{ref} \tag{7.1}$$

Here T_x is the time that the comparator output signal is high and T is the repetition time of the ramp signal. V_ref is the reference signal which is modulated by the comparator output signal. Moreover it can be shown

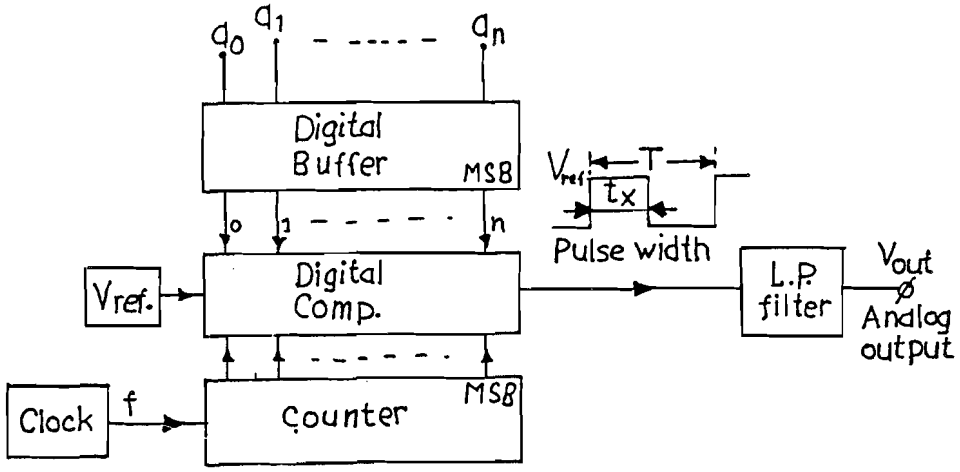

Figure 7.1 : Pulse-width modulation D/A converter

that:

$$T = \frac{2^n}{f_{clock}} \tag{7.2}$$

Here n is the number of bits of the counter.
A disadvantage of this system is the low repetition rate of the pulse-width modulated signal. This results in a large stopband attenuation requirement of the low-pass filter.
A system which overcomes partly this problem is shown in Fig. 7.2. From the figure, which uses exactly the same building blocks, it can be seen that the weighting of the bits of the digital buffer and the bits of the ramp signal generated by the counter are reversed. As a result of this operation the output pulse of the comparator is better randomized during the repetition period T. The requirements of the output filter can be reduced.
The table in shows an example of this randomizing for a 3-bit code 110.

Buffer	Reverse Counter	Normal Counter	Reverse Comparator	Normal Comparator
0 0 0	0 0 0	0 0 0	S	S
1 0 0	0 0 1	1 0 0	L	S
0 1 0	0 1 0	0 1 0	S	S
1 1 0	0 1 1	1 1 0	L	E
- - - -				
0 0 1	1 0 0	0 0 1	S	L

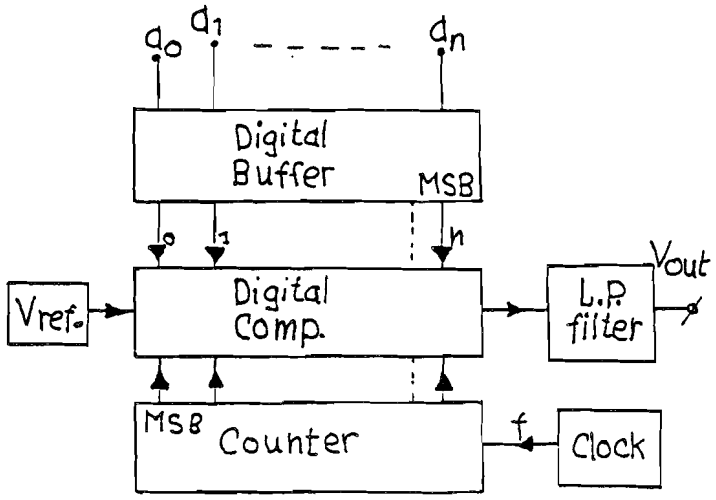

Figure 7.2 : Reverse comparing pulse-width modulating D/A converter

1 0 1	1 0 1	1 0 1	L	L
0 1 1	1 1 0	0 1 1	E	L
1 1 1	1 1 1	1 1 1	L	L

Notation:
S = Smaller
L = Larger
E = Equal.
From the table the randomizing of the comparator output in the case of the reverse bit-weight connected counter can be easily distinguished.

7.3 Integrating D/A converters

In Fig. 7.3 an example of a single slope D/A converter is shown. The system consists of digital input latches which store the input information, a digital comparator and a counter operating from a crystal controlled oscillator. In this part of the circuitry the input data is converted into a time signal which is the output of the digital comparator. The comparator output signal switches the reference current I to the integrator which converts the current signal into an analog output voltage across the capacitor C. At the end of the integration cycle the sample-and-hold using an operational amplifier and

feedback elements R_1, R_2 and C_2, samples the final analog value of the converter and holds the signal during the time the next conversion is performed. A stepped output signal is obtained. This output signal can be applied to a low-pass filter which finally reconstructs the analog output signal. At the

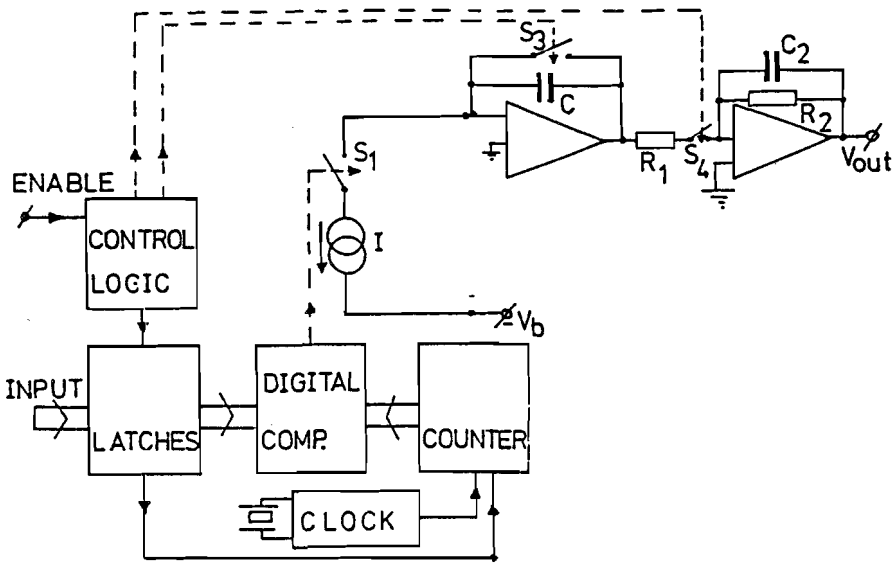

Figure 7.3 : Single-slope integrating D/A converter

start conversion the integrator is reset and the sample-and-hold amplifier remains in the hold mode. When an input data word is loaded into the buffer, the reset switch is opened and the reference current starts charging the capacitor during the time the value in the counter is smaller than the buffer value. At the moment the comparator detects a counter value which equals the buffer value, then the reference current is switched off and the integrator remains at the converted analog value. The sample-and-hold amplifier samples the output signal of the integrator. When the next start conversion comes, the sample-and-hold amplifier is switched in the hold mode storing the analog information during the time the next digital-to-analog conversion is performed. The conversion speed of this systems depends on the number of bits which must be converted and the maximum clock speed which can be applied to the system.

To increase speed the input data word can be split-up into a coarse and fine value. At the same time the reference currents are split-up into two weighted values which correspond with the splitting of the coarse and fine

digital values.
In Fig. 7.4 a simplified form is shown. In this system the number of clock

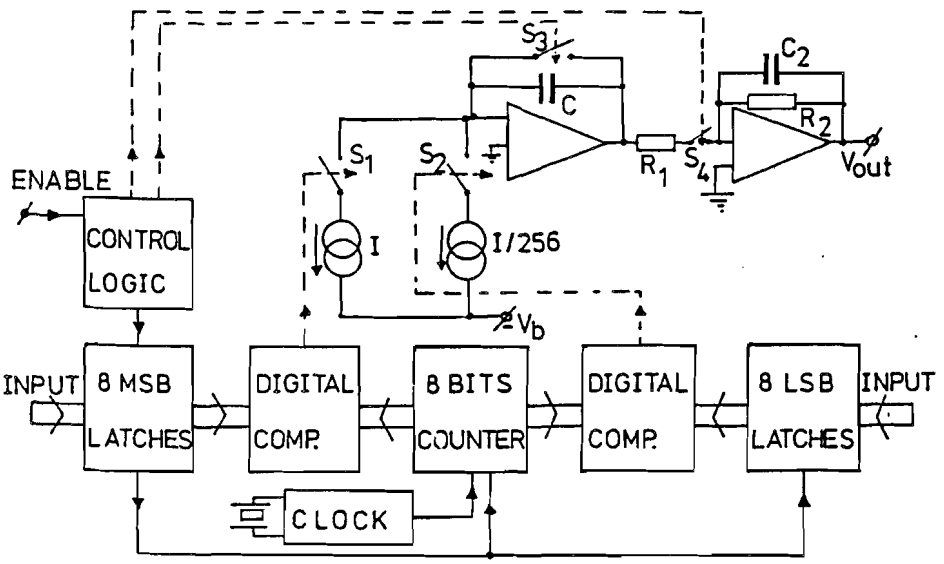

Figure 7.4 : Dual ramp D/A converter system

pulses to obtain a full coarse and fine counter is reduced. In a 16-bit system using an 8-bit coarse and fine split-up a 256 times larger speed can be obtained compared to the circuit of Fig. 7.3. A conversion starts with the reset of the integrator by closing switch S_3. At the same time the coarse and fine digital data is loaded into the input latches. Then switch S_3 is opened and the counter, which is reset to zero, starts counting. As long as the counter data is smaller than the input data, the comparator outputs are closing switches S_1 and S_2 respectively. The reference currents I and $\frac{I}{256}$ are charging the integrator capacitor C. This charging stops at the moment the contents of the counter is larger than the course or the fine input data. Finally the analog data is sampled by the succeeding sample-and-hold amplifier consisting of an operational amplifier with feedback elements R_1, R_2 and C_2. The sample-and-hold circuit is switched into to hold mode during the time a new sample is loaded and converted into an analog value. Then this new value is sampled giving the next output signal. A low-pass filter can be used to reconstruct the analog signal.
A disadvantage of the single integrator systems is that full scale accuracy is dependent on the reference current value I and the integrator capacitor C.

Furthermore the accuracy with which the switches can be operated determines the linearity of the system. Dynamic performance is determined by the performance of the sample-and-hold amplifier.

7.4 Current weighting using ladder networks

7.4.1 R $2R$ ladder network

An R $2R$ ladder network with terminating transistors to generate binary weighted currents is shown in Fig. 7.5. The good matching and excellent thermal tracking of integrated resistors is the main design criterion of this circuit. Some practical information about resistor matching is given in reference [39]. The circuit consists of equal resistors with a value R. The $2R$

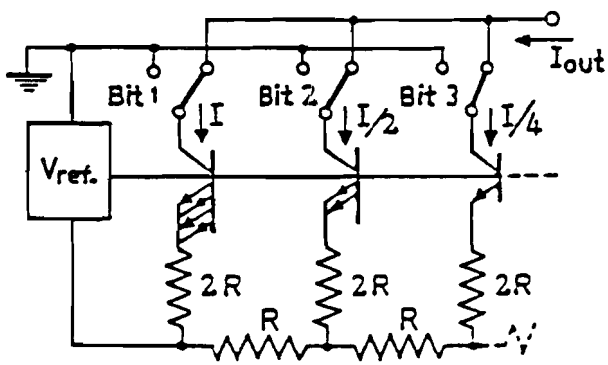

Figure 7.5 : R-2R ladder network D/A converter system

resistor is formed by connecting two resistors in series to obtain the best resistor matching. Because the output currents are binary weighted, the base-emitter voltages of the terminating transistors will decrease if no special measures are taken. From Fig. 7.5 it can be seen that the transistor sizes decrease by a factor two every time the current is reduced. An equal voltage at the emitters of the current source transistors is needed for an accurate operation of the R $2R$ ladder network. The division with such a network depends on a divide by two voltage division every time a section is added. At the time a low bit current value is reached, the voltage drop across the resistors is small compared to the base-emitter voltage of the transistors.

Therefore the current density per transistor must be equal, which results in the scaling of the emitter sizes of the transistors.

7.4.2 Resistor weighting current network

In Fig. 7.6 an example of a network is shown which uses a binary resistor weighting combined with emitter scaling to obtain an accurately binary weighted current network. In this system, however, The total amount of resistance increases to nearly $2^N R$, where R is the resistor value for the MSB bit current generation. The die size even more increases compared to the circuit given in Fig. 7.5.

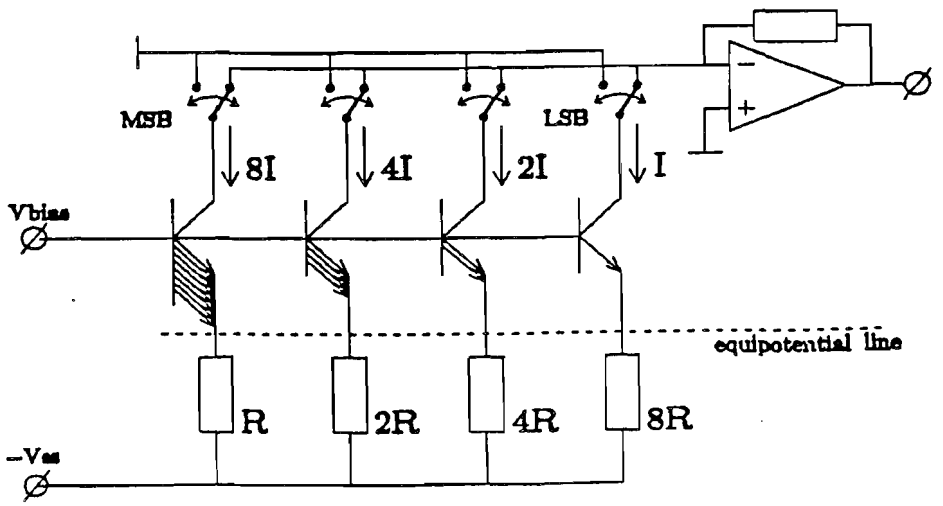

Figure 7.6 : Binary weighted current network using resistor weighting

7.4.3 Equal currents output ladder network

In high-speed converter systems the switching speed is an important parameter. Therefore a network with equal currents is used in combination with an output R $2R$ resistor network to obtain the binary weighting. Mostly the impedance of the R $2R$ network is designed for 75 Ohm or 50 Ohm, depending on the characteristic impedance of the system the converter has to work with. In Fig. 7.7 an example of such a system is shown. The basic idea behind this system is that for every technology there exists a transistor size and current density for which an optimum switching performance

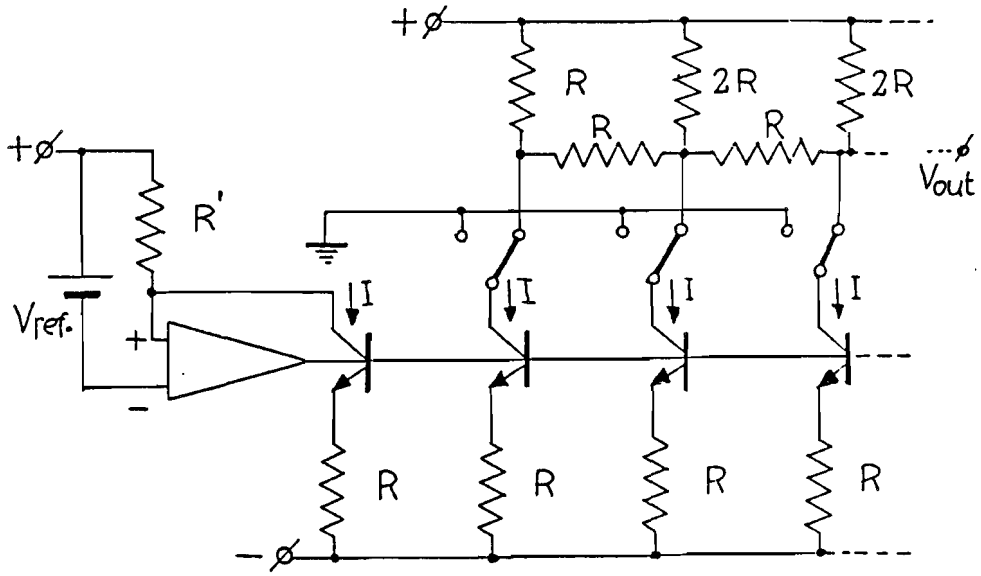

Figure 7.7 : High-speed equal current binary weighted resistor network

is obtained. Therefore equal currents are accurately generated in the lower part of the circuit shown in Fig. 7.7 using equal resistors R. Furthermore the equal current values need only equal transistors. The output capacitance of this network is small and equal to a single transistor capacitance. To accurately couple the reference source V_{ref} with the current value I an extra current source is added in a feedback loop with an operational amplifier. This operational amplifier adjusts the base voltages of the current transistors in such a way that the current I is equal to:

$$I = \frac{V_{ref}}{R'}. \tag{7.3}$$

The digital input information sets the switches in the required position. The current I is applied to an R $2R$ network to obtain a binary voltage weighting depending on the weight of every input bit. With a low value for R e.g., R= 75 Ohm, the delay through the total R $2R$ network is so small that an small acquisition time of the total system is obtained. A disadvantage of this system is that the number of accurately matched elements is increased. This has an influence on the yield of these systems, especially when the resolution of the system is increased to 10 or 12 bits.

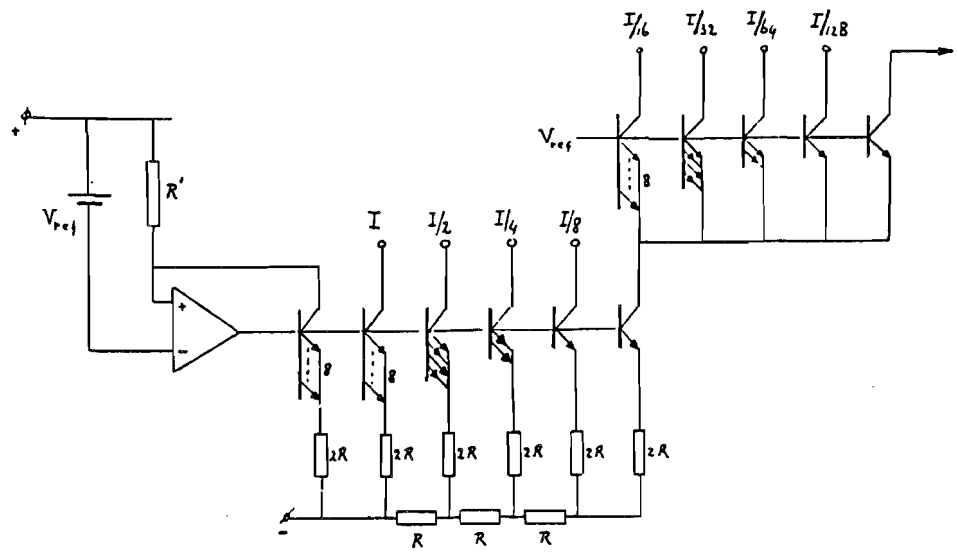

Figure 7.8 : Two step current division network

7.4.4 Two step current division network

By using a two step current division principle a number of problems from the above discussed systems can be overcome. In Fig. 7.8 an example of an 8-bit converter is shown. In the four most significant bit current generation part of the system an $R\ 2R$ current network with emitter scaling is used to obtain the optimum accuracy. The most significant current is repeated to form with the reference source a feedback loop which controls the base voltages of the system in such a way that an accurate relation between the output current I and the reference source is obtained. The current value $\frac{I}{8}$ is repeated. This current is applied to an emitter scaled fine divider network which performs the 4 bit fine division. Note that the current value $\frac{I}{128}$ is two times applied to make the total tail current equal to $\frac{I}{8}$. This second current value is not needed for the binary weighted network and is therefore connected to a supply voltage. Base current is lost in the second divider unit. In some cases this can introduce untolerable errors in the weighting function. To compensate for base current losses, the size of the second transistor which generated a current $\frac{I}{128}$ can be decreased in such away that a compensation for the loss in base currents of the fine divider part is obtained. Such a compensation gives only a limited compensation possibility and must be analyzed for worst case device tolerances and extreme temperature ranges. As can be seen

from this system an optimum in die size and amount of elements is obtained.

7.4.5 Base dropping R $2R$ network with equal sized transistors

An interesting alternative exists by using a base dropping voltage to compensate for the binary emitter size weighting of the current source transistors. As is known from device physics, the difference in base-emitter voltage of bipolar transistors with a current ratio of 1 to 2 and an equal emitter size is equal to:

$$\Delta V_{be} = \frac{kT}{q} \ln 2. \tag{7.4}$$

In Fig. 7.9 an example is shown. In this system an R $2R$ network is used

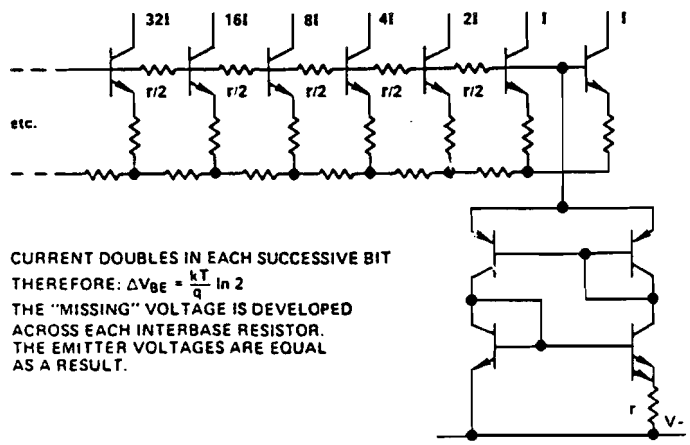

Figure 7.9 : Base dropping voltage compensation technique

to generate the accurately binary weighted currents. Between the bases of the current source transistors, which apply the binary weighted currents to the bit switches, a resistor with a value $\frac{r}{2}$ is applied. Across this resistor a voltage is generated which is equal to: $\frac{kT}{q} \ln 2$. For this purpose a current source is added which generated a current equal to

$$I_r = \frac{2kT}{rq} \ln 2 \tag{7.5}$$

The current mirror action in the current stabilizer doubles the output current. Furthermore a model showing a 1 to 2 ratio in emitter size is used with

the resistor r to obtain the proportional with absolute temperature current I_r. In chapter 10 a more detailed analysis of these type of current sources will be given.

7.4.6 10-bit binary weighted converter system

In Fig. 7.10 an example of a 10-bit binary weighted current converter network is shown. From Fig. 7.10 it can be seen that a combination of tech-

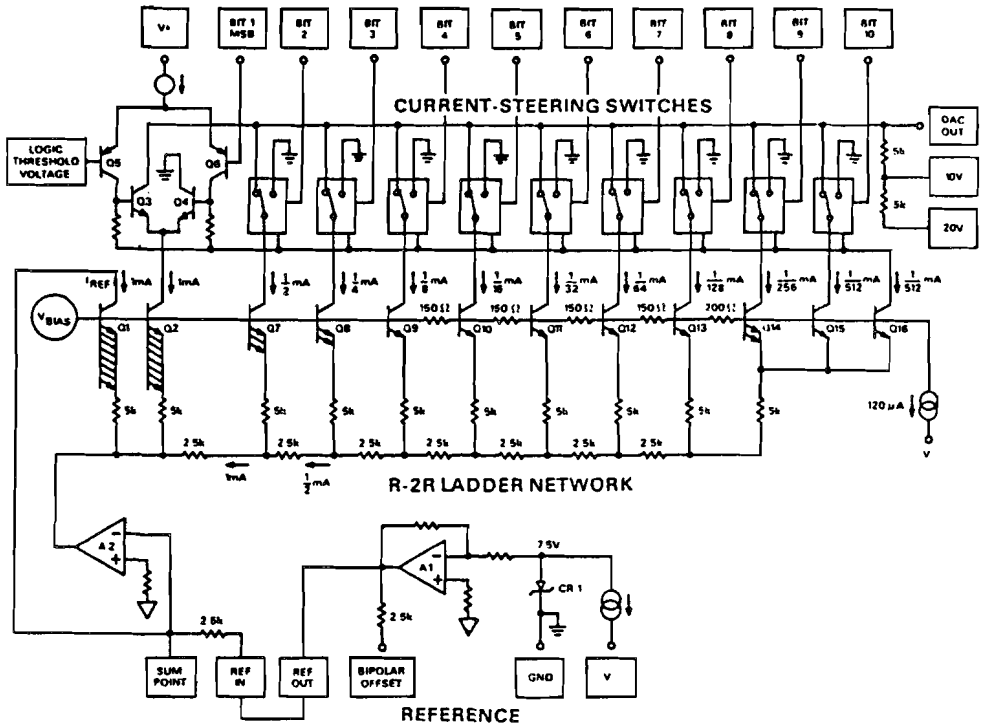

Figure 7.10 : 10-bit binary weighted converter system

niques is used to generate binary weighted currents. In the most significant bit part (4 bits) an R $2R$ ladder network with emitter scaling is used. The next 5 bits use the base dropping voltage technique to compensate for the emitter scaling of the current source transistors. Finally the last two bits use emitter scaling. Note that the LSB bit currents are generated twice. The current source of 120 μA generates a voltage of about 18 mV across the 150 Ohm base dropping resistors. Furthermore the most significant bit is copied

again and compared with the reference source. In this system the bases of the current network are connected to a bias terminal and the operational amplifier A_2 controls the voltage across the R $2R$ network in such away that the MSB current value is equal to the reference current value flowing through the resistor of 2.5 k connected from $Ref\ In$ to the inverting input of amplifier A_2. The zener diode CR_1 generates a reference voltage of about 7.5 V, which via operational amplifier A_1 is applied to the converter. As shown in a part of the circuit diagram the bit switches consists of differential pairs, at the MSB current value called T_3, T_4. These differential pairs are driven from lateral PNP transistors T_5, T_6 in the MSB example. One side of all the switches is connected to the logic threshold level. The other side can be directly driven from TTL logic levels or CMOS levels. Lateral PNP transistors have the advantage that the base-emitter reverse breakdown voltage is practically equal to the collector-base breakdown voltage of an NPN transistor. Therefore lateral PNP transistors can be reverse biased with voltages of at least 10 Volts without distroying the devices. The output terminal of this D/A converter must be connected to an inverting output operational amplifier. Feedback resistors of 5 K are available as current to voltage elements having the same temperature coefficients as the resistors used in the binary weighted current network.

7.4.7 Binary weighted current divider using emitter scaling

Although matching of active elements is limited in the range of 1for two equal transistors, it is possible to use the law of the large numbers to improve the matching. In Fig. 7.11 an example of a 10-bit binary weighted current network using emitter scaling is shown. To obtain the bit weighting for the most significant bit 512 transistors are randomly connected in parallel in the network. The matching with respect to the ideal number of 512 is improved by $\sqrt{5}12$ or about 22 times. This means that a 1.05improves the matching about 11 times. We obtain finally about 0.1Going through the current network shows that the matching of every smaller bit decreases. In a binary weighted network this is more or less allowed because the influence of the LSB bit on the overall integral linearity is much less than the MSB bit. Base current compensation in this system is used by weighting the total base current of the divider using a second simplified emitter scaled current divider. Individually the weighted base current is added to the individual bits to obtain an accurate division of the total tail current I_{in}. The advantage of using emitter scaling is that over a large input current range an accurate

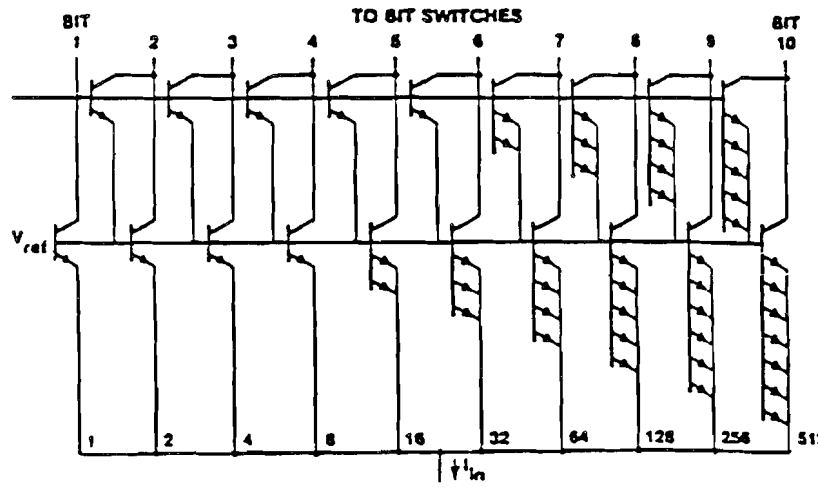

Figure 7.11 : Binary weighted current network using emitter scaling

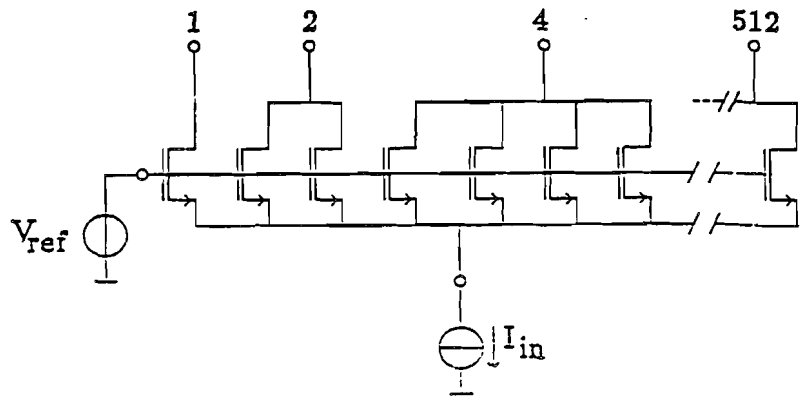

Figure 7.12 : Binary current weighting using MOS devices

weighting is possible. In practice an integral linearity better than $\frac{1}{2}$ LSB is obtained over an input current range from a μA to a few mA. In Fig. 7.12 a binary weighted network using MOS devices is shown. In the MOS system again 1024 devices are used to generate the a binary weighted current division. The connection of devices to generate the MSB current value is made in such a way that a good averaging concerning the matching of the devices is obtained as was the case with the bipolar implementation of this circuit type. In Fig. 7.13 the integral non- linearity of an MOS binary weighted current network as a function of the tail current is shown. Analyzing the measurement results shows that a 10-bit binary weighted MOS network can

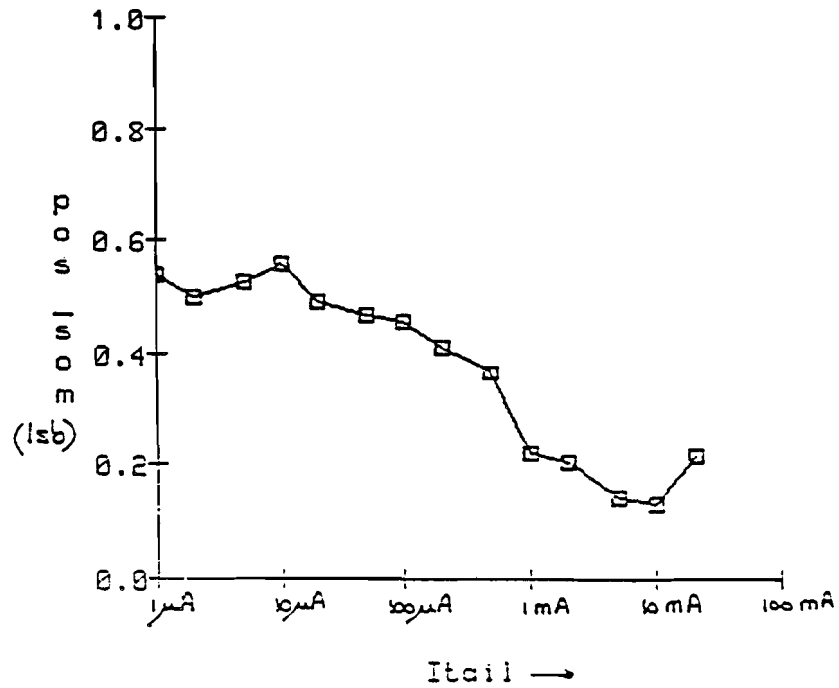

Figure 7.13 : Integral non-linearity measurement result

be designed having $\frac{1}{2}$ LSB integral non-linearity over a tail current value from 1 μA to 20 mA.

7.4.8 MOS ladder network converter system

In an MOS technology a thin film technology to construct the R $2R$ ladder network is used in combination with MOS (complementary P- and N-MOS devices) switches to design a D/A converter. Thin film resistors show a better matching than poly silicon resistors which are available in an MOS technology. Moreover, thin film devices can be trimmed to improve the accuracy of the converter. In Fig. 7.14 a basic circuit diagram of a 10-bit D/A converter is shown. As can be seen from Fig. 7.14, the ON resistance of the MOS bit switches is scaled to obtain a good accuracy of the converter. The reference voltage is applied at the analog input terminal. In this special situation a maximum of 10 Volts is used as reference. The resistor values are chosen depending on the size of the MOS switches and the ON resistance of these switches. A special application of this system is found

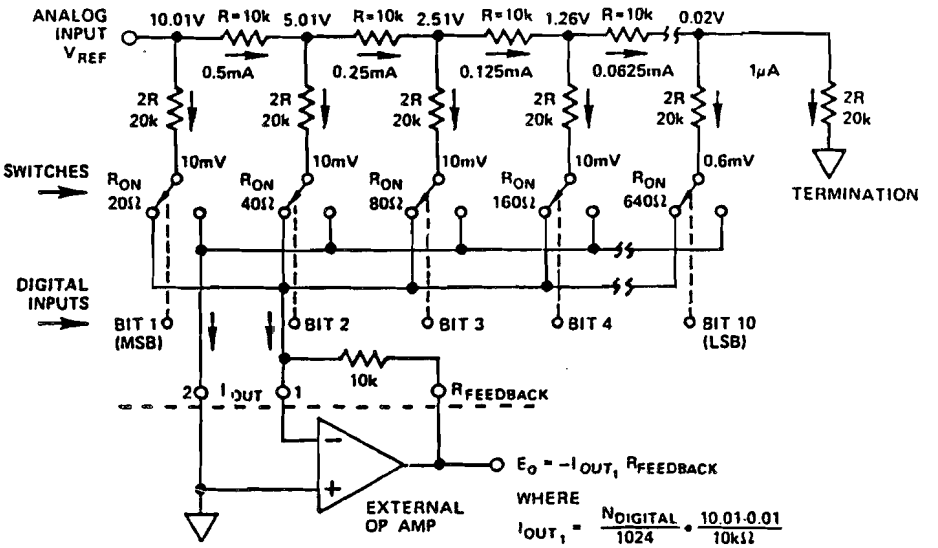

Figure 7.14 : MOS ladder network D/A converter system

if the analog input voltage is modulated. In that case a multiplying D/A converter structure is obtained. Such a construction can be used to increase the maximum dynamic range of the system or for digitally controlling an ac signal which can be used as analog reference voltage. The output signal of the ladder network is a current. This current is converted into a voltage using an external operational amplifier with a feedback resistor $R_{feedback}$. This feedback resistor is included with the ladder resistor network to obtain the same temperature coefficient and the same matching. Note furthermore that an extra termination resistor is included to obtain the required network loading. Using thin film resistor trimming techniques the linearity of this converter can be increased to 12 bits.

7.4.9 Weighted capacitor converter system

In an MOS technology capacitors with MOS switches perform an identical operation as resistors and transistors in a bipolar technology. In Fig. 7.15 an example of a binary weighted capacitor D/A converter system is shown. The system consists of n binary weighted capacitors, an additional capacitor with the unit capacitance, and operational amplifier connected as a follower and a set of switches which can connect the weighted capacitors to the reference voltage V_{ref}. At the start of the conversion all capacitors are discharged as

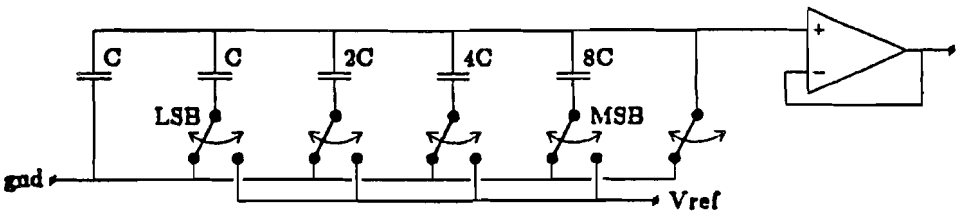

Figure 7.15 : Binary weighted capacitor D/A converter

shown in the switch configuration of Fig. 7.15. Then all the capacitors are connected to the reference voltage to perform a precharge condition. In this case the unit capacitor C is still short circuited to ground. When the conversion starts, every capacitor, depending on the digital input information is connected to ground (gnd) or remains in the reference position. During the conversion the charge is redistributed over the capacitors and a binary weighted D/A conversion is obtained for the generated output voltage.
Suppose that the total capacitance value in the system is equal to: C_{total}, then the unit capacitance C is equal to:

$$C = \frac{C_{total}}{2^N}. \tag{7.6}$$

The value of the capacitor connected to bit n, C_n becomes:

$$C_n = 2^{N-1} \times C. \tag{7.7}$$

The output voltage of the capacitor network can now be expressed in terms of capacitor values and the corresponding digital input code D_i. A calculation of the output voltage gives:

$$V_{out} = \frac{V_{ref}}{C_{total}} \sum_{i=1}^{N} C_i D_i \tag{7.8}$$

This equation can be simplified into:

$$V_{out} = \frac{V_{ref}}{2^N} \sum_{i=1}^{N} D_i \tag{7.9}$$

This equation shows the binary weighting which is obtained by the charge redistribution technique. These techniques can be successfully applied to D/A converters in an MOS technology.

7.4.10 Some remarks about the ladder converter systems

In a 10-bit system, for example, the largest transistor has a size which is $2^{N-1} = 512$ times the size of the transistor in the least significant bit. Such a ratio in transistor size requires a large die size. Moreover, the output capacitance of the most significant bit current source is large due to the parallel connection of 512 transistors. Such a large capacitance has a drawback for the switching of this current to the output terminal. As a result it is difficult to operate all switches at the same speed. This switching at the exact same moment is required to obtain a small output glitch. Mostly a reference source is added to accurately determine the value of the MSB current of the converter. Technology studies in a bipolar or CMOS implementation of these types of converters show that without trimming an accurate converter of up to 10 bits can be designed. In that case this converter does not need any trimming to obtain the required linearity and monotonicity specification. Modifying the design in a multiple equal current generation and switching of two or more of the MSBs improves the monotonicity of the converter. Furthermore, the accuracy is increased by using more elements in parallel to generate the high current values. The law of the numbers increases the weighting accuracy by the square root of the number of elements used. To increase the accuracy of the R-$2R$ system a trimming procedure is needed. With trimming it is possible to obtain the high accuracy. However, the system becomes sensitive to material stresses and therefore needs to be trimmed after the die has been mounted in its encapsulation. An example of a trimmed high-resolution converter is given in reference [40]. Such procedures are fairly expensive. To overcome this problem a different system approach will be used.

7.5 Monotonic by design network systems

7.5.1 Current weighting operation

Sometimes it is not necessary to obtain a converter with a full integral linearity specification, but it is enough to guarantee monotonicity of the system. In that case a different design technique can be adopted. Monotonicity of a converter is obtained if with an increasing digital input signal an increase in analog output signal can be guaranteed. In such a case always a current is added and not switched off and replaced by a larger current value. In Fig. 7.16 an example of a current based *monotonic by design* converter type is

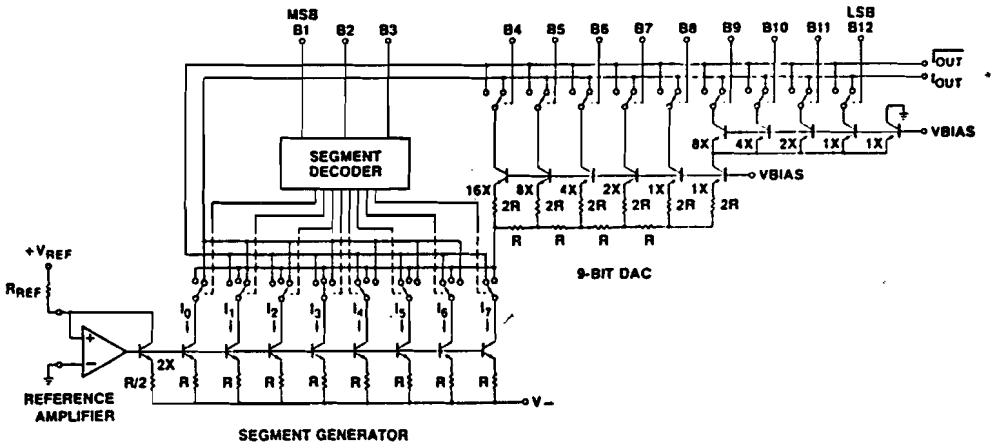

Figure 7.16 : Monotonic current based D/A converter system

shown. In the most significant 3 bits of the converter equal currents are used. The binary digital input signal uses a segment decoder to obtain for six of the eight switches a three position condition. The next 5 bits use an R $2R$ network with emitter scaling to obtain an accurate current division. In the third 3 bit weighting network emitter scaling is used. The implementation of an R $2R$ network does not improve the weighting accuracy because of the small value of the current and the limited value resistors can be given in an integrated circuit. The operation of the system can be explained by supposing that a sawtooth like digital input code is applied at the input of the converter. First the current I_7 is switched to the 9-bit current weighting network. This current is switched to the output node I_{out} by the bit switches B_4 to B_{12}. At the moment the output current I_{out} must be larger than I_7, then the output current I_7 is switched directly to the output terminal I_{out} by the segment current switches. At the same time the current I_6 is switched to the 9-bit current network to perform the next quantization steps until the output currents exceeds $I_6 + I_7$. At that moment the current I_6 is switched directly to the output terminal I_{out} too and the current I_5 is switched to the 9-bit current network. Using this procedure *monotonicity* of the converter can be guaranteed. Integral linearity basically is not guaranteed to be less than $\frac{1}{2}$ LSB.

7.5.2 Voltage division operation

An example of a monotonic by design voltage dividing converter is shown in Fig. 7.17. As can be seen from Fig. 7.17 the system consists of two

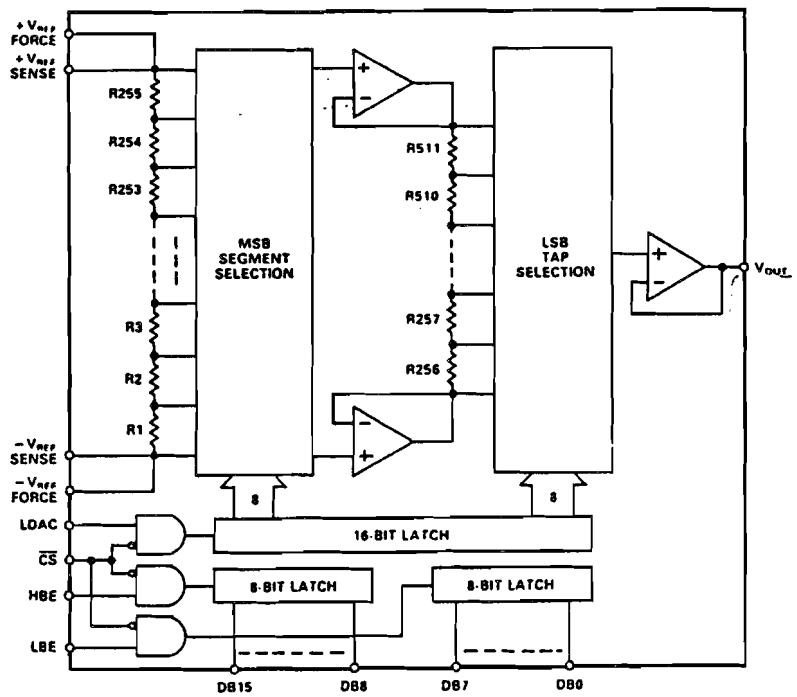

Figure 7.17 : Voltage division monotonic converter

resistor string with 256 taps using resistors R_1 to R_{255} for the coarse divider part and R_{256} to R_{511} for the fine divider part. Two operational amplifiers connected in the follower mode apply the tap voltage of the coarse section across the total resistor string of the fine divider part. The MSB segment selection block consists of two sets of switches which are driven by the segment decoder. In the LSB tap selection block a set of switches is used to select a resistor tap and apply the output voltage to the output buffer. This output buffer consists of an operational amplifier in follower mode. A special operation of the switches in the MSB segment encoder is used to make the system independent of the offset voltage of the voltage followers. In Fig. 7.18 a detailed circuit diagram of the circuit including the switch drivers is shown. From the figure it can be seen that one side of the even numbered coarse switches are connected to voltage follower A_2 while one side of the

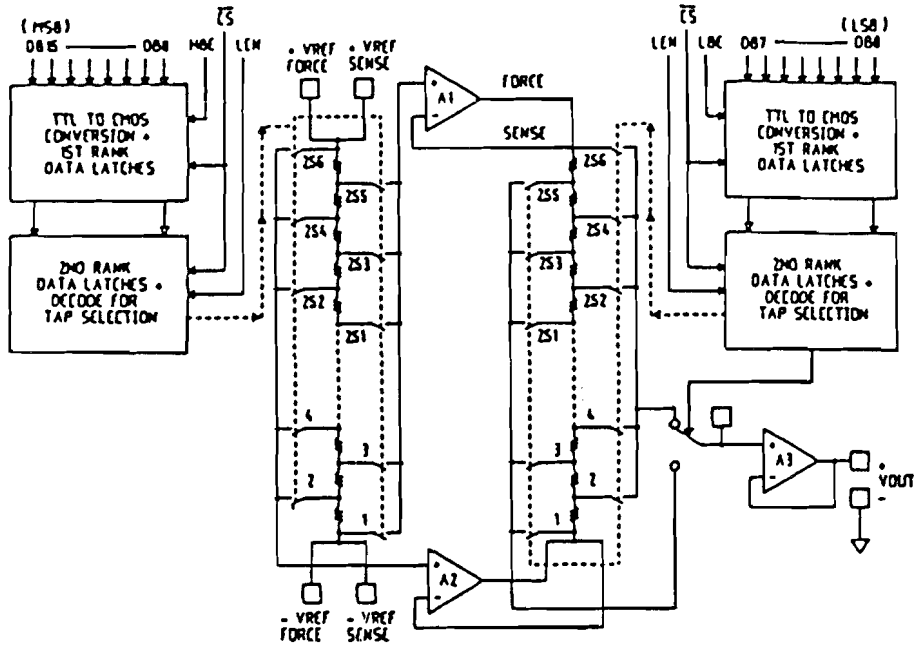

Figure 7.18 : Detailed circuit diagram of monotonic voltage converter

odd numbered switches is connected to voltage follower A_1. An identical connection is obtained for the switches of the fine voltage divider. However, the output lines of the odd and even numbered fine switches are connected to an additional output switch. This decoding is used to minimize the amount of latches and decoding circuitry.
The special connection used in the coarse voltage divider allows the analog signal to "roll-off" against the coarse divider without jumping from one position into another. In this way a continuous output voltage change can be guaranteed independent of the offset voltage of the voltage followers A_1 and A_2. Using this system it is possible to construct a 16-bit guaranteed monotonic converter without needing the high division accuracy to obtain the integral non-linearity of $\frac{1}{2}$ LSB.

7.6 Self calibrating D/A converter system

If D/A converters are not continuously is use, a calibration procedure can be used to eliminate inaccuracies of elements. In Fig. 7.19 an example of a D/A converter system which uses a self calibration cycle is shown. The

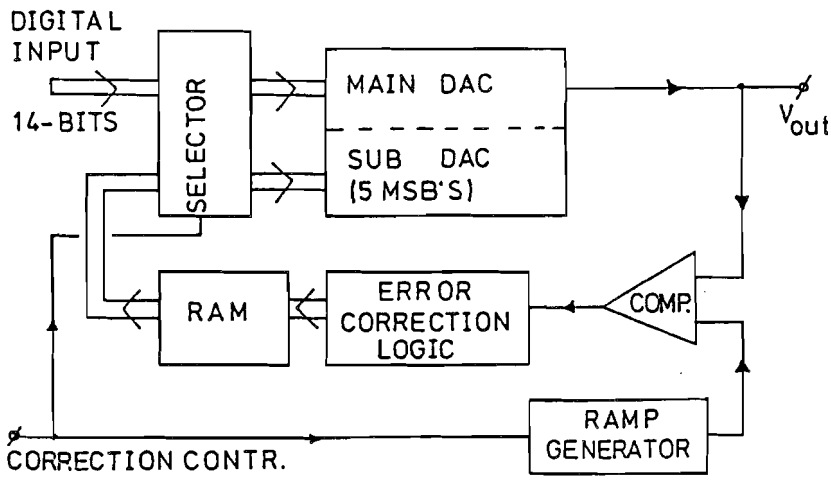

Figure 7.19 : Self calibrating D/A converter system

system consists of a main D/A converter and a sub D/A converter used to eliminate the errors in the main D/A converter. During the calibration cycle an analog ramp is generated using a ramp generator. The output of the main D/A converter is compared with the ramp signal by the comparator. The correction logic generates a digital correction signal which is stored in the RAM unit. The RAM data controls the sub D/A converter to correct the output signal of the total D/A converter function to obtain the full $\frac{1}{2}$ LSB integral non-linearity. In Fig. 7.20 the calibration operation is shown. At the moment the main D/A output signal does differ from the ideal D/A converter output, which is generated by the ramp signal source, then a counting operation starts which controls the output of the sub D/A converter to add a small correction value to the main D/A converter output to obtain the ideal output value. The correction value is stored for every weighting value of the main D/A converter. This means that in a 14-bit system 14 correction values of 6 to 8 bits must be stored to correct the main D/A converter output. When a code is applied to the D/A converter, then the correction value is called from the RAM and applied to the sub D/A to correct the output. Note that during calibration the D/A converter can not be used for conversion. In some applications this can be a disadvantage. To overcome this problem a different method will be used.

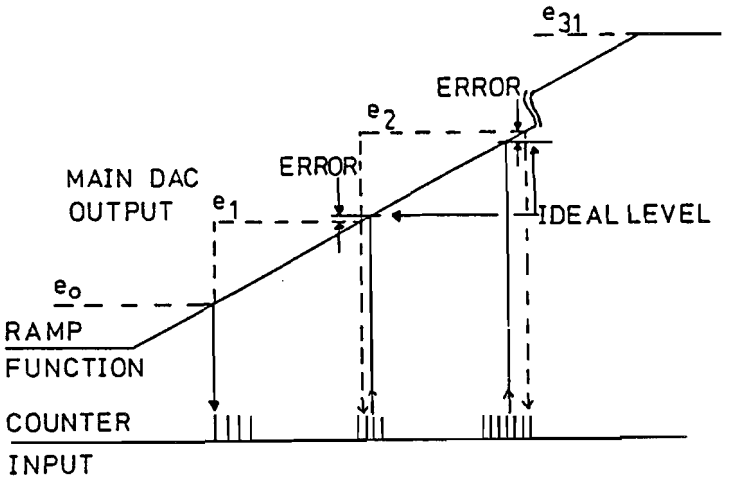

Figure 7.20 : D/A correction cycle

7.7 Basic dynamic divider scheme

A simplified circuit diagram of the basic dynamic current divider is shown in Fig. 7.21. The circuit consists of a passive current divider and a set of

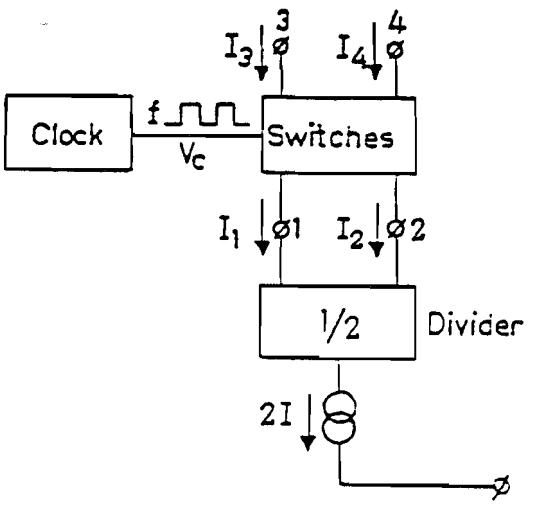

Figure 7.21 : Basic dynamic current divider

switches driven by the clock generator f. The passive divider divides the total current $2I$ into two nearly equal parts: $I_1 = I + \Delta I$, $I_2 = I - \Delta I$. The currents I_1 and I_2 are now interchanged during equal time intervals with

respect to the output terminals 3 and 4. At these terminals currents then flow whose average values are exactly equal and have a dc value I. In Fig. 7.22 the currents as a function of time are shown. The figure shows that a

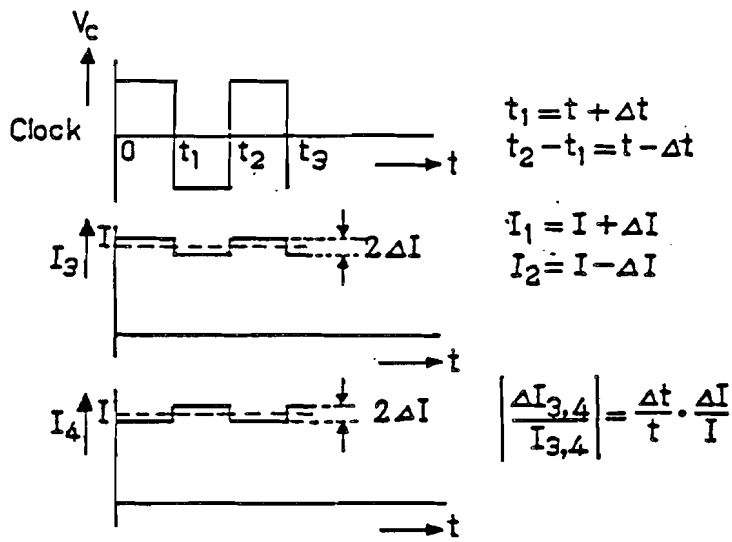

Figure 7.22 : Currents as a function of time in the dynamic current divider

small ripple current with a value of $2\Delta I$ and frequency f is also present at the output terminals. This ripple is a measure of the matching accuracy of the passive divider. With a simple low-pass filter this ripple can be removed from the output current and as a result accurate output currents with a value of I are obtained. In principle, a current divider with an exact division ratio of one-to-two is obtained with this system. Moreover, if the matching of the passive divider stage changed during operation, for example because of a slowly changing temperature, then the accuracy of the system would not change. The only variation which occurs is the increase or decrease of the ripple current value depending on the direction in which the matching in the passive divider changes. In the previous analysis an accurate time division by two is supposed. If there is a slight difference in the timing of the two clock cycles, then a high-accuracy is still possible. Suppose that the clock time periods differ by a value Δt then we obtain:

$$t_1 = t + \Delta t, \tag{7.10}$$

and

$$t_2 = t - \Delta t. \tag{7.11}$$

Also, using the already defined values for I_1 and I_2

$$I_1 = I + \Delta I, \tag{7.12}$$

and

$$I_2 = I - \Delta I. \tag{7.13}$$

The current differences ΔI are equal because the sum of the two currents must be equal to $2I$, which is the starting current of the divider stage. During the first phase of the clock cycle the output currents become:

$$I_{out11} = (t + \Delta t) \times (I + \Delta I) \tag{7.14}$$

and

$$I_{out21} = (t + \Delta t) \times (I - \Delta I). \tag{7.15}$$

In the second phase of the clock cycle the output currents change into:

$$I_{out12} = (t - \Delta t) \times (I - \Delta I) \tag{7.16}$$

and

$$I_{out22} = (t - \Delta t) \times (I + \Delta I). \tag{7.17}$$

Now at every output terminal the currents must be added and averaged over the total clock time $2t$. We obtain:

$$\frac{I_{out11} + I_{out12}}{2t} = I(1 + \frac{\Delta t \times \Delta I}{t \times I}) \tag{7.18}$$

$$\frac{I_{out21} + I_{out22}}{2t} = I(1 - \frac{\Delta t \times \Delta I}{t \times I}). \tag{7.19}$$

As is seen from equations 7.18 and 7.19 the final accuracy in this system is determined by the product of two small errors. In practice it is not difficult to make $\frac{\Delta t}{t} \leq 0.1\%$ and the matching of the passive divider can easily be made smaller than 1% so $\frac{\Delta I}{I} \leq 1\%$. An overall accuracy better than 10^{-5} is obtained without using extremely difficult circuitry or elements which are difficult to match. The ripple which is present at the output of the divider scheme is a measure of the matching accuracy in the passive divider. This method which obtains a high accuracy without using highly matched and highly accurately trimmed elements is called *Dynamic Element Matching*.

The value of the ripple can be reduced by optimizing the matching characteristics of the passive divide-by-two stage. A small ripple on the output values of the circuit allows the use of a simple low-pass filter network to reject this ripple below the quantization noise of the system. Usually such a network consists of a single RC stage.
Generally speaking: *Dynamic Element Matching* can be used to increase the accuracy of a divider scheme when the network can be split up into a number of nearly equal elements. The accuracy improvement is obtained by a continuously cyclic interchanging of the elements with respect to the respective output terminals. The output signals must be averaged over the total interchanging time period. At least an order of magnitude improvement in accuracy is obtained in this way. Furthermore, this system is independent of element aging and does not need highly accurate elements.
In reference [41] an example is shown which does not use binary weighting of current. Instead a decimal weighting is used to generate reference currents for resistor measurements.
Self-calibration techniques of converters have become fairly popular during the last few years. In references [42,43] examples of these techniques are given, applied in a D/A and an A/D converter.

7.8 Practical dynamic divider circuit

In Fig. 7.23 a circuit diagram of a practical divider in a bipolar technology is shown. The passive divide-by-two current division is performed by transistors T_1, T_2. Two cross-coupled differential stages (T_3 to T_{10}) interchange the currents I_1 and I_2 for equal time intervals between the output terminals 3 and 4. The already discussed improvement in division accuracy with respect to the basic current divider T_1, T_2 is now obtained. The base currents of the Darlington switches limit the division accuracy. The *only* criterion determining this overall accuracy for the *whole* circuit is a high current gain of the Darlington circuits (e.g. $\beta^2 > 10^4$ and with $\frac{\Delta\beta}{\beta} \leq 0.1$ a practical limit better than 10^{-5} is obtained. If the current gain of a standard process is not high enough, then an extra processing step to obtain high-gain, low breakdown transistors can be used. The value of the output ripple current depends on the matching of the current mirror T_1, T_2. A problem in this current mirror is the base current of transistors T_1 and T_2, which is added to the current flowing through transistor T_2. This reduces the matching accuracy in the system to about $\frac{2}{\beta}$. An improvement in matching accuracy is obtained

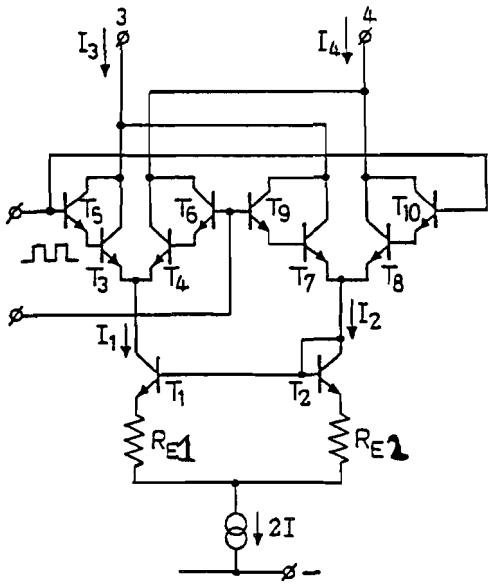

Figure 7.23 : Practical dynamic divider scheme

by inserting emitter degeneration resistors R_{E1} and R_{E2} as shown in Fig. 7.23. An exact compensation of the base currents is obtained by inserting a resistor with a value of $2 \times R_{E2}$ in series with the base of transistor T_2. This results in the same effect as increasing the value of the emitter resistor R_{E2} by a value $2 \times \frac{R_{E2}}{\beta}$. The voltage drop across the resistors is about 5 to 10 times the value of $\frac{k \times T}{q}$, giving a value between 125 mV and 250 mV. The minimum supply voltage drop across the circuit to operate under linear condition is about $3V_{be}$ or between 1.8 and 2.5 V.

7.9 Two-bit dynamic current divider scheme

In the circuit of Fig. 7.23 per dynamic divider stage only one accurately matched bit current is generated. When such stages are cascaded, then the supply voltages will increase to an impractically high voltage level. To overcome this problem a 2-bit system will be used. The basic system diagram is shown in Fig. 7.24. In this system the passive divider is extended to divide a current $4I$ into four nearly equal currents: $I_1 = I + \Delta_1 I$, $I_2 = I + \Delta_2 I$,

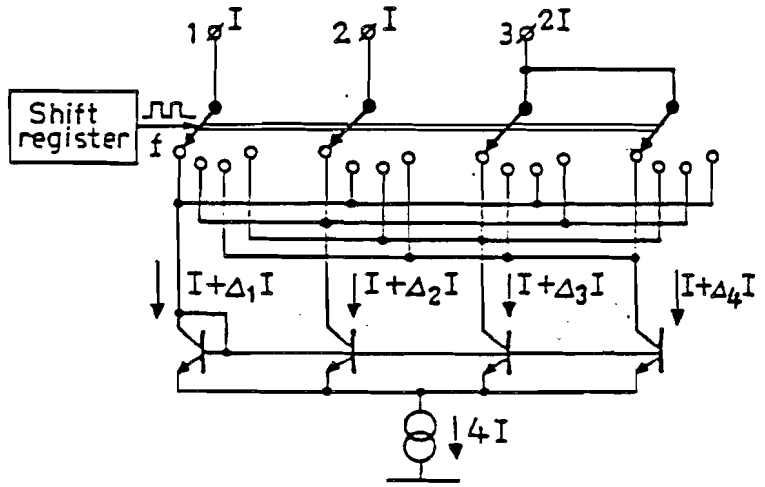

Figure 7.24 : 2-bit current divider scheme

$I_3 = I + \Delta_3 I$, and $I_4 = I + \Delta_4$. Note that $\Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 = 0$, because the total current which is divided into four nearly equal parts is $4I$. These currents are now fed into a switching network that interchanges all currents during equal time intervals with respect to the output terminals 1, 2 and the combined terminal 3. At these outputs averaged currents with values I, I, and $2I$ are obtained. In Fig. 7.25 the output currents as a function of time are shown. From Fig. 7.25 it can be seen that the currents with a value I have the same frequency as the clock f, while the current with a value $2I$ has a ripple with a frequency $\frac{f}{2}$. Timing errors have the same influence as in the one-bit divider scheme. In Fig. 7.26 a circuit diagram of a practical divider circuit is shown. It consists again of a passive divide by four stage using transistors T_1, T_2, T_3, and T_4, with the emitter degeneration resistors R. This stage divides the current $4I$ into four nearly equal values of I. These currents are applied to the interchanging system consisting of Darlington switches to minimize base current losses which might reduce the overall accuracy of the system. In Fig. 7.26 the bases of the passive divider are connected to a reference voltage V_{ref}. Usually this reference voltage is the collector terminal of, for example, transistor T_1. In this way a current mirror circuit with four output signals is obtained. Furthermore, such a system does not lose base currents due to the final current gain of the bipolar transistors used in this system. By tuning one of the emitter resistors a more accurate division in this divide-by-four stage is obtained. The same method

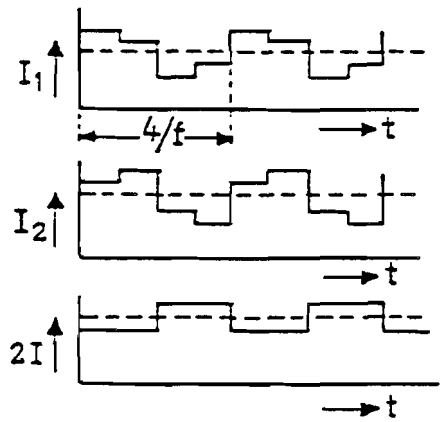

Figure 7.25 : Output currents as a function of time for the 2-bit divider system

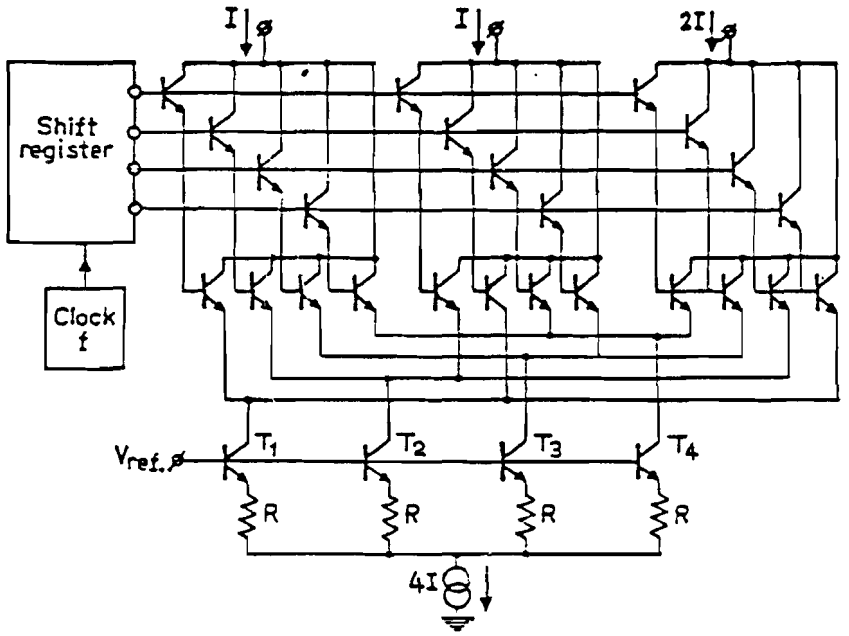

Figure 7.26 : Practical 2-bit dynamic current divider

as used in Fig. 7.24 can be used again for transistor T_1.
A four-stage shift register provides the time-accurate signals for the interchanging of the currents. In this circuit a high time division accuracy is

easily obtained. The only additional criterion to improve the accuracy of the system is a high current gain of the bipolar transistors in the Darlington switches.

7.10 High-speed Darlington switching stages

It is known in general that Darlington stages do not switch accurately and rapidly. In Fig. 7.27 a single Darlington stage consisting of Transistor T_1 and Transistor T_2 is shown. The parameters which determine the switching

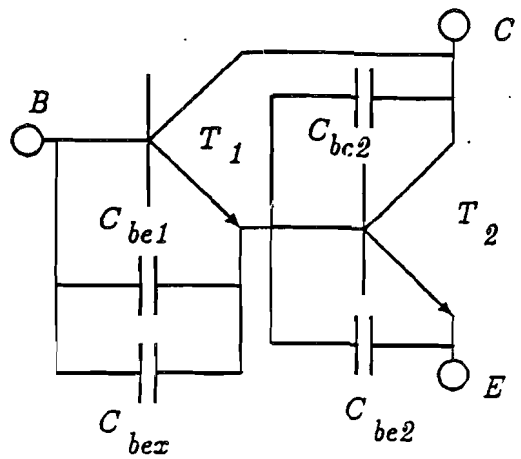

Figure 7.27 : Basic Darlington switch configuration

performance at high frequencies are shown as capacitors C_{be1}, C_{be2}, and C_{bc}. Capacitor C_{bex} is an extra capacitor. The function of this capacitor will be explained later on. Suppose at first that the value of $C_{bex} = 0$. When the switch is conducting and is intended to be switched off, then due to the loading of transistor T_1 with a capacitance of $C_{bc2} + C_{be2} > C_{be1}$ transistor T_1 will be switched off much faster and with a larger voltage variation than the voltage swing across T_2. The capacitive division of the switching voltage is not balanced equally across the transistors $T1$ and T_2. A much smaller variation of the switching voltage across T_2 is obtained in comparison with T_1. Furthermore, due to the forward biasing of transistor T_2 at a much higher level than T_1 the base-emitter capacitance C_{be2} of T_2 is much larger than C_{be1} of T_1. As a result, the capacitor unbalance is increased for high-speed switching signals. To overcome this problem an

extra capacitor C_{bex} is added to the base-emitter capacitance of transistor T_1. The value of this capacitor must be chosen in such a way that an equal switching voltage variation across transistor T_1 and transistor T_2 is obtained. Using an accurate transistor model a simulation can show the exact value of C_{bex}. In a practical application, however, this capacitor is rather difficult to construct and to apply in an integrated circuit layout. Therefore a parameterized model configuration is used in which the size of transistor T_1 with respect to transistor T_2 can be increased. In this way the capacitor matching and implementation are done by properly adjusting the sizes of transistors T_1 with respect to T_2. In Fig. 7.28 an example of a Darlington switch layout is shown.

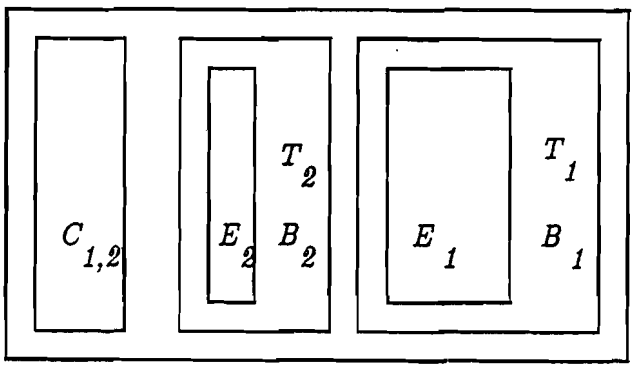

Figure 7.28 : Compensated Darlington switch layout

7.11 Dynamic current mirror circuit

In some applications it is useful to obtain an accurately matched current mirror. A circuit diagram which uses *Dynamic Element Matching* to obtain a device-independent accurate current mirror is shown in Fig. 7.29 The

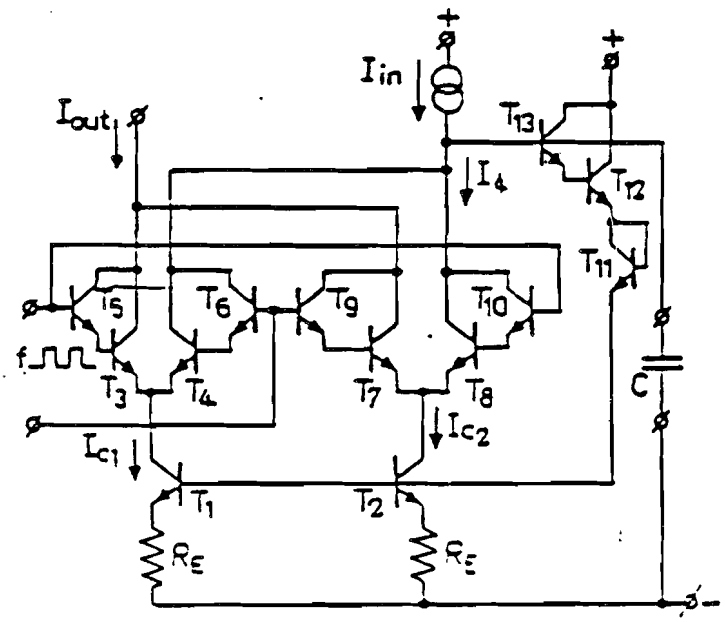

Figure 7.29 : Dynamic current mirror circuit diagram

basic current mirror consists of transistors T_1 and T_2 with emitter degeneration resistors R_E to increase the matching accuracy. Darlington stages T_3 to T_10 interchange the currents of T_1 and T_2 with respect to the sum and output terminal of the mirror. Darlington stage T_{12} and T_{13} with the level-shifting diode T_{11} forms the current-source feedback loop. In the previous circuit diagrams a connection between the collector and the base of a transistor was used to construct a diode which in cooperation with a parallel connected transistor forms a current mirror. Two cases of operation can now be distinguished.

1) An averaging capacitor is connected across the diode connection of the current mirror. This means that the base of transistor T_{13} is decoupled to ground with the capacitor shown as C. The average value of the collector currents I_{c1} and I_{c2} shown as I_4 is made equal to I_{in}. Then the average out-

put current I_{out} is the average value of I_4. As a result an accurate current mirror $I_{out} = I_{in}$ is obtained.
2) The capacitor C is omitted. During the first half period of the clock phase the current I_{c2} is controlled in such a way that $I_{c2} = I_{in}$. By supposing an error Δ between the transistors T_1 and T_2, an output current equal to $I_{out} = I_{in} \times (1 + \Delta)$ is obtained. During the second phase of the clock cycle, I_{c1} and I_{c2} are interchanged, resulting in an output current $I_{out} = \frac{I_{in}}{1+\Delta}$. When Δ is made small, by obtaining a good matching between the transistors T_1 and T_2 then the division by $(1 + \Delta)$ can be approximated by a finite series expansion. As a result we obtain:

$$I_{out} \cong I_{in}(1 - \Delta + \Delta^2) \tag{7.20}$$

After averaging the results over the total clock period we obtain:

$$I_{out} \cong I_{in}(1 + \frac{1}{2}\Delta^2) \tag{7.21}$$

Inserting a value for $\Delta \leq 0.5\%$ the mirroring error term is below 10^{-5}. The current mirror without the capacitor C shows a less accurate performance than the one with a large capacitor C.

7.12 Binary-weighted accurate current network

A binary-weighted current network is formed by cascading current division elements. In Fig. 7.30 a simplified block diagram using single current divider stages is shown. In the first divider stage a combination with a reference current source I_{ref} and a current amplifier A_0 is made to obtain an accurate current mirror.
Now two possibilities exist with respect to the interchanging frequency of the cascaded current divider stages.
1) Every following divider stage is operated at half or double the switching frequency of the first divider stage.
2) Every divider stage obtains the same interchanging frequency.

7.12.1 Binary-weighted current network with divided interchanging clock

In this case digital clock circuitry which accurately divides the interchanging clock frequency by two is needed. Supposing that we lower the interchanging

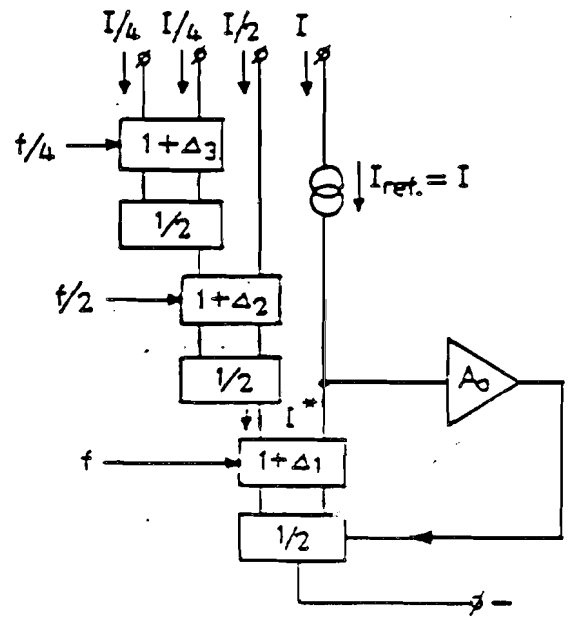

Figure 7.30 : Binary-weighted current network

frequency every time a current is divided by two, then we will not have any interaction between the individual current dividers concerning the finite matching accuracy of every divider. In Fig. 7.31 the currents in the first and second divider stage as a function of time are shown. Suppose that the output current of the first divider I^* shows the inaccuracy Δ_1 as shown in the top part of Fig. 7.31. In the output current $\frac{I}{2}$ of the second divider stage we can recognize the error Δ_2 with a frequency $\frac{f}{2}$ and the error Δ_1 of the first stage with a frequency f in the lower part of Fig. 7.31. During a half period of the clock $\frac{f}{2}$ the average value of the current $\frac{I}{2}$ does not contain an error term originating from the first divider stage of frequency f. The same is valid for the second half clock period of the frequency $\frac{f}{2}$. As a result of this operation no interaction of the division accuracy of the first stage on the second stage is found. If the clock frequency division is continued the same arguments can be used for the next stage and so on. An independent operation of the individual stages in the total divider chain is obtained. A disadvantage of the division of the interchanging clock frequency by factors of two is the large increase in digital circuitry which is needed to accurately drive the individual divider stages. Moreover, the ripple frequency decreases

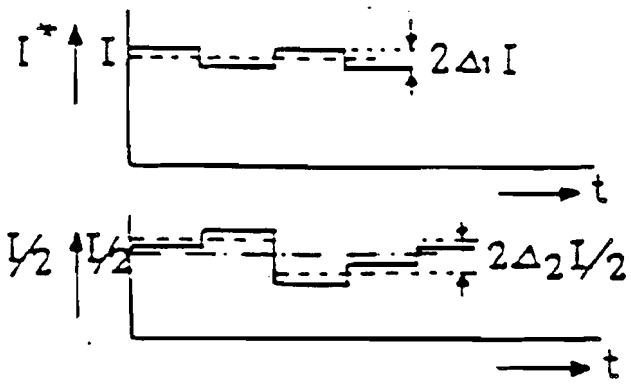

Figure 7.31 : Output currents of first two current dividers as a function of time

with decreasing current value. This means that the filtering capacitors which are used in the passive ripple filter increase and might need impractically large values.

7.12.2 Binary-weighted current network using equal interchanging clock frequencies

When all divider stages are operated with the same interchanging clock then it is expected that in the error analysis interactions between the individual divider stages will occur. Timing errors in this case are equal for all the divider stages. These timing errors can therefore be separated from the division errors in the individual stages.
Suppose the error in the first stage is denoted as Δ_1, then the total error of the first stage including the timing error can be written as:

$$I^* = I_{ref}(1 + \Delta_1 \times \frac{\Delta t}{t}). \tag{7.22}$$

In the expression given in equation 7.22 the filtering capacitor as described with regard to the accurate current mirror circuit is ignored. The average value of the output current of the second stage can be calculated:

$$\frac{I}{2}_{average} = I_{ref}\frac{(1+\Delta_1)(1+\Delta_2)(t+\Delta t)+(1-\Delta_1)(1-\Delta_2)(t-\Delta t)}{4t}. \tag{7.23}$$

This long formula can be simplified into:

$$\frac{I}{2} = \frac{I_{ref}}{2}(1 + \Delta_1\Delta_2 + (\Delta_1 + \Delta_2)\frac{\Delta t}{t}). \tag{7.24}$$

The average value of the output current of the third stage is again determined. The simplified result is shown in the following equation:

$$\frac{I}{4} = \frac{I}{4}(1 - \Delta_1\Delta_2 + \Delta_1\Delta_3 - \Delta_2\Delta_3 + (\Delta_1 - \Delta_2 + \Delta_3)\frac{\Delta t}{t}). \tag{7.25}$$

If the error terms of the individual stages are made small ($\Delta_{1\rightarrow n} \leq 0.5\%$), then the influence of the interactions between the individual divider stages on the overall accuracy of the binary-weighted current network can be kept very small. To increase the resolution of the active divider stages a 2-bit-per-switching-level configuration can be used advantageously.

7.13 14- and 16-bit binary network examples

An example of a 14-bit binary-weighted current network using 2-bit-per-level divider stages is shown in Fig. 7.32. In this system 5 active divider stages are cascaded followed by a 4-bit passive divider using emitter scaling of transistors. In the 14-bit system a choice between 5 active and a 4-bit passive divider has been made to obtain a high circuit yield. The disadvantage of the large number of cascaded active stages is the large supply voltage needed ($V_{supply} > 15$ V). To overcome this drawback the number of active divider stages can be reduced. In Fig. 7.33 a 16-bit binary-weighted network is shown. Here 3 active divider stages are cascaded, followed by a 10-bit passive divider using emitter scaling. To obtain a high matching accuracy in the passive divider the 1024 transistors used are randomly interconnected. In this way the accuracy increases with the square root of the number of transistors connected in parallel. This means for the MSB bit that the practical matching between transistors of about 1% is increased by $\sqrt{512} \approx 20$. This results in a matching accuracy of 0.05 %. Tests on practical dividers built-up from 1024 transistors to obtain a 10-bit divider showed that these circuits can be designed with a high circuit yield. The supply voltage of the total circuit can be reduced to 12 V. In Fig. 7.34 a 10-bit binary-weighted current divider using emitter scaling and base-current compensation is shown. Note that all the bases of the transistors are connected to obtain information about the total base current which would have been lost when no additional

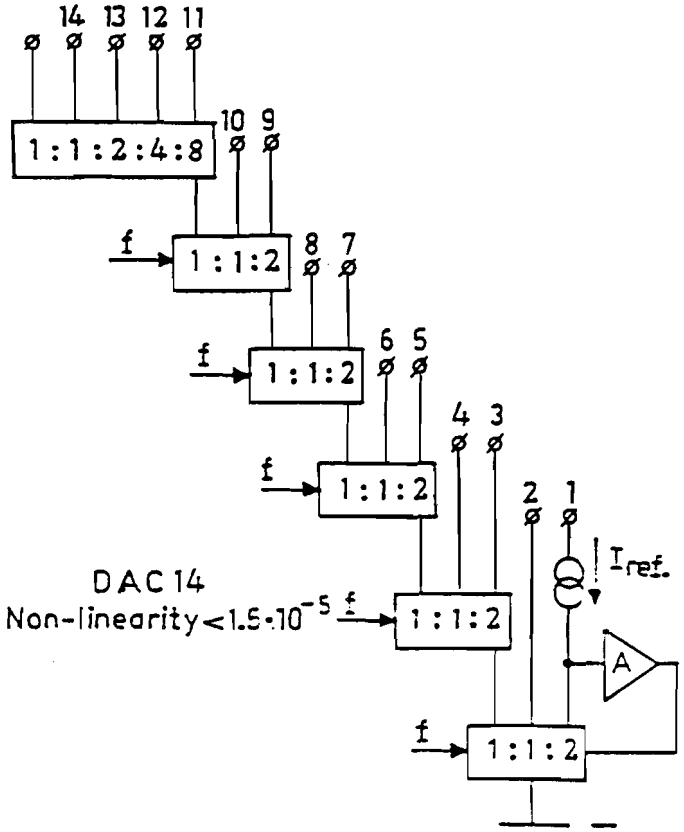

Figure 7.32 : 14-bit binary-weighted current network

circuitry is added. To obtain an accurate base-current compensation a second scaling of the base currents is used with a second passive divider stage, again using emitter scaling to improve the division accuracy. In the case of base current compensation the averaging effect improves the base current compensation again resulting in a high-accuracy base-current-independent passive division network.

7.14 Filtering and switching

In Fig. 7.35 the switching and filtering operation of the bit currents of the active divider stages is shown. A first-order filtering operation using the elements R_1C_1, R_2C_2 is performed to remove the ripple current from the final

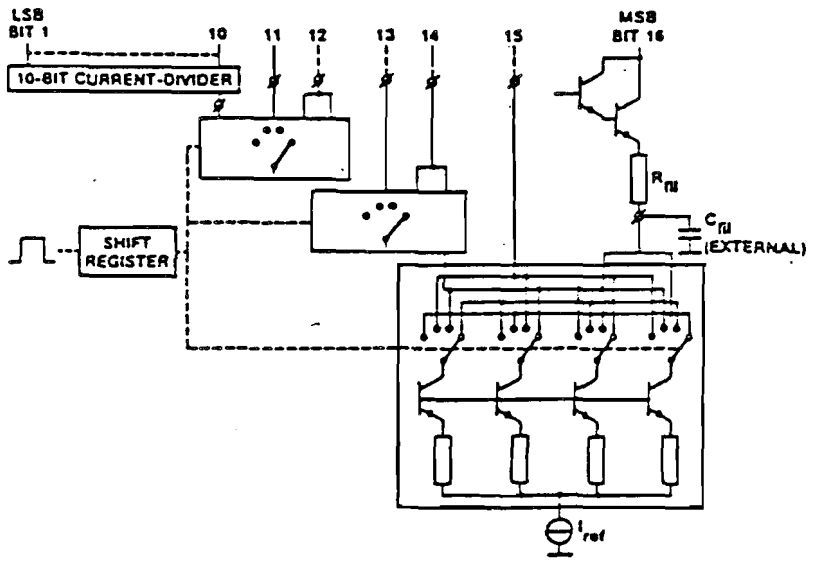

Figure 7.33 : 16-bit binary-weighted current network

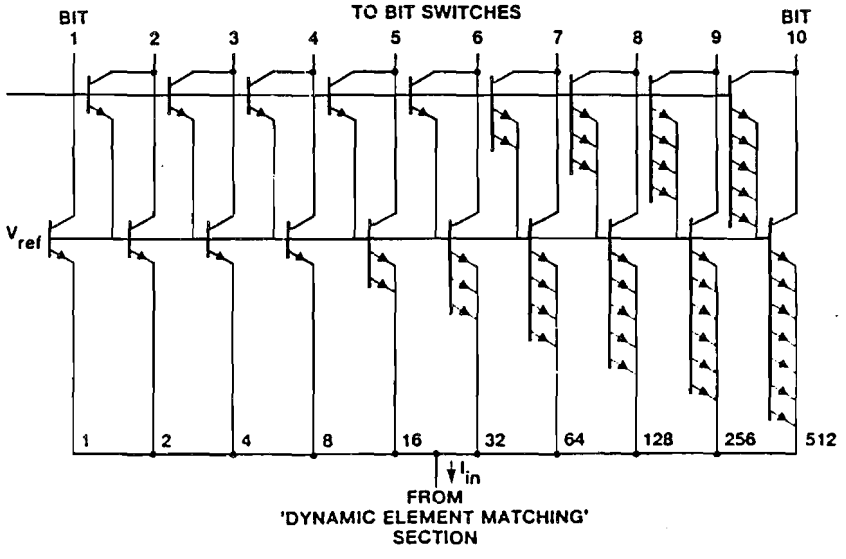

Figure 7.34 : 10-bit binary-weighted current divider using base current compensation

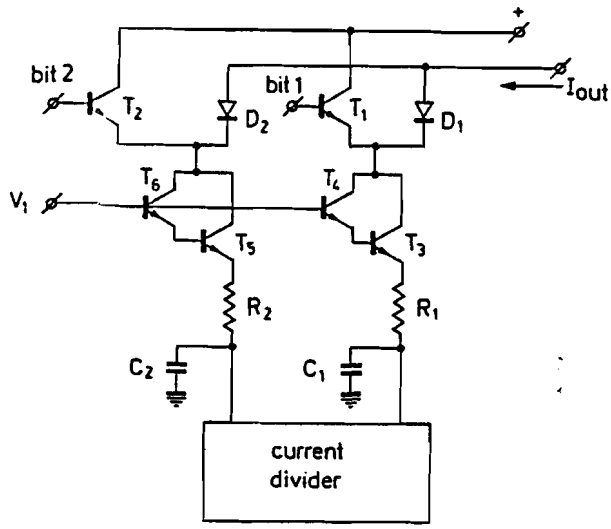

Figure 7.35 : Filtering and switching of bit currents

accurate bit current. The external capacitors C_1 and C_2 are added to the chip for this purpose. Additional Darlington cascode stages (T_3, T_4 and T_5, T_6) isolate the filter operation from the switching of the binary-weighted bit currents. Furthermore, the individual filtering of the bit currents minimizes the noise on the bit output currents, resulting in a high signal-to-noise ratio of the total converter. Bit switching is performed with a diode transistor configuration (T_1, D_1, and T_2, D_2). This switching configuration obtains a very high switching accuracy in steady state because no currents are lost by the final current gain of a bipolar transistor. A diode conducts all the applied input current to the output terminal. One problem, however, is found with this diode-transistor switch. The switching speed at low bit current levels is reduced because of the large capacitive loading in the collector leads of the Darlington stages (e.g. T_6, T_5). This capacitance must be charged before the bit current is connected to the output through the diode D_2. In this example it is supposed that the bit current is NOT flowing to the output terminal at the beginning of the switching cycle. This is the worst condition in this circuit.

7.15 Compensated bit switch

To overcome the speed problem at low current values an additional switching stage is added to the circuit diagram of Fig. 7.35. The objective of this additional switching stage is to maintain the same voltage levels in the switching branch of the circuit. In this way parasitic capacitances do not need to be charged or discharged. In Fig. 7.36 the improved switch is shown. To obtain the compensation effect an extra differential pair T_7, T_8 with the

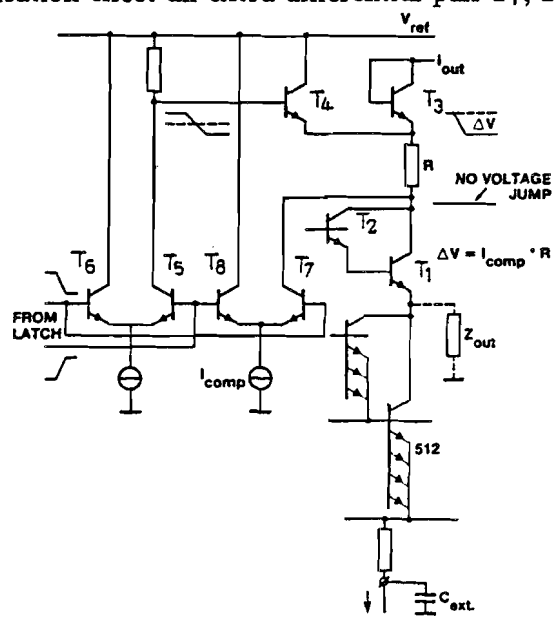

Figure 7.36 : Improved diode-transistor bit-switch

resistor R are added to the circuit from Fig. 7.35. The differential amplifier T_7, T_8 has a tail current with value I_{comp}. The value of this current is chosen in such a way that:

$$I_{comp} \times R = \Delta V \tag{7.26}$$

In this equation the value of ΔV is equal to the voltage swing which is applied to the diode-transistor switch to get a high switching accuracy. In this case this means that the on-off ratio of the switch must be better than 1 to 10^{-6} over temperature and supply voltage ranges for which the 16-bit D/A converter is designed. The operation of the compensation loop is as follows: Suppose first that the bit current is switched to the output terminal of the converter. This means that the diode T_3 is conducting and the compensation current is flowing through transistor T_8 to the supply line.

The voltage level across the diode T_3 and the compensation resistor R is preset. At the moment the bit current must be switched off, the diode T_3 is switched off and transistor T_4 starts conducting because the base voltage of this transistor now equals the supply voltage V_{ref1}. At the same time transistor T_7 starts conduction and a current will flow through the resistor R and transistor T_4. The value of the resistor R with the compensation current I_{comp} is chosen in such a way that the voltage jump in the collectors of T_1 and T_2 is made zero. As a result of this action the parasitic capacitor in the collectors of T_1 and T_2 does not change in voltage level. No charging current is subtracted from the bit current which is switched on or off. A faster operation of the switch is obtained. This faster switching also reduces the possibility of glitches occuring at the output of the converter.

7.16 Output current-to-voltage converter

The diode-transistor switch shows a big advantage in terms of accuracy of switching. One drawback, however, is the coupling of the output voltage level with the switching voltage level applied to the transistor part of the switch. Due to the diode coupling there is a direct connection between the output voltage and the voltage at the emitter of the diode. Voltage variations at this point reduce the effective switching voltage, which might result in a loss in switching accuracy. To overcome this problem an inverting operational amplifier must be connected at the output of the switch. The voltage level around which the switching occurs can now be accurately determined. As a result, the voltage swing which is applied to the switch can be optimized with respect to accuracy, switching speed and minimum glitch output.

7.17 14-bit D/A parallel converter

A complete circuit diagram of a 14-bit D/A converter with parallel data inputs is shown in Fig. 7.37. Note that in the reference input circuit a temperature-compensated current reference source is used in a current mirror circuit to apply this current to the binary current divider network and that the other terminal of the current reference is used as the MSB current of the converter. This current is switched directly by the MSB current switch. A master/slave flip-flop is used to accurately generate time moments for the dynamic matching operation in the circuit. This flip-flop is driven by an emitter-coupled multivibrator to generate clock pulses for the time-dividing

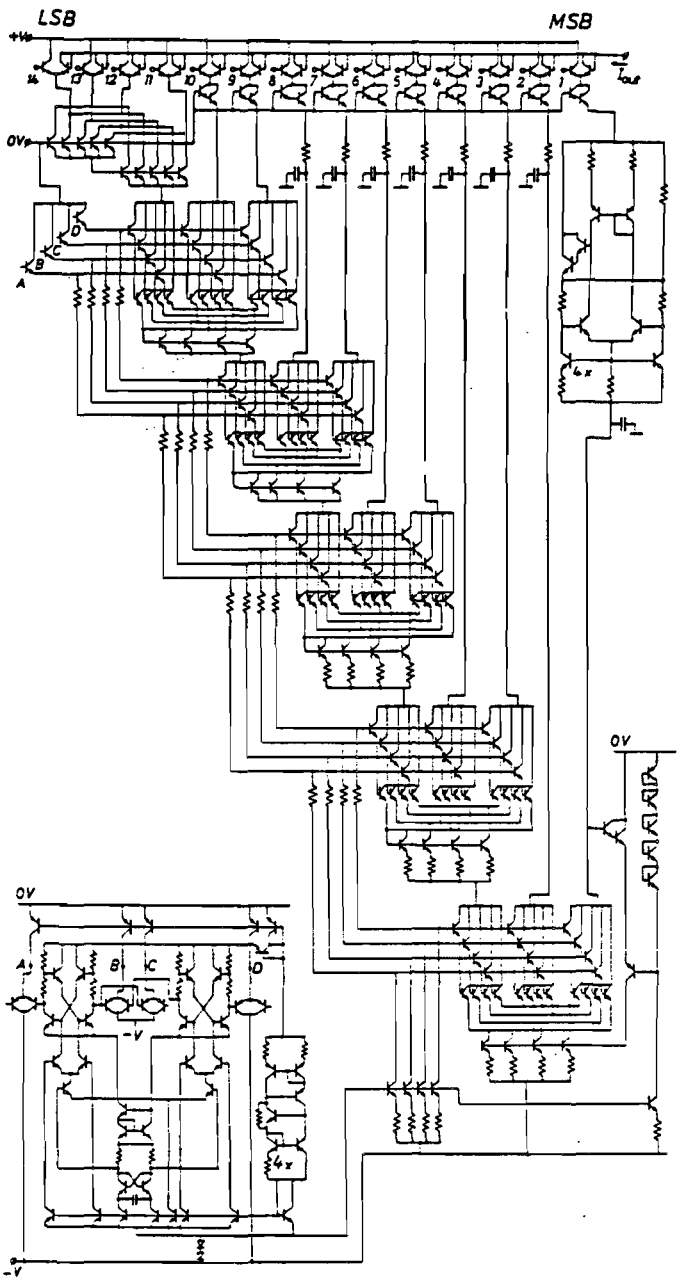

Figure 7.37 : Complete 14-bit D/A converter circuit diagram with parallel data input

flip-flop. To avoid feedthrough of the digital data information to the analog output terminal of the converter, a serial input data system is needed.

7.18 16-bit dual D/A converter system

In Fig. 7.38 a dual 16-bit D/A converter system diagram is shown. The dig-

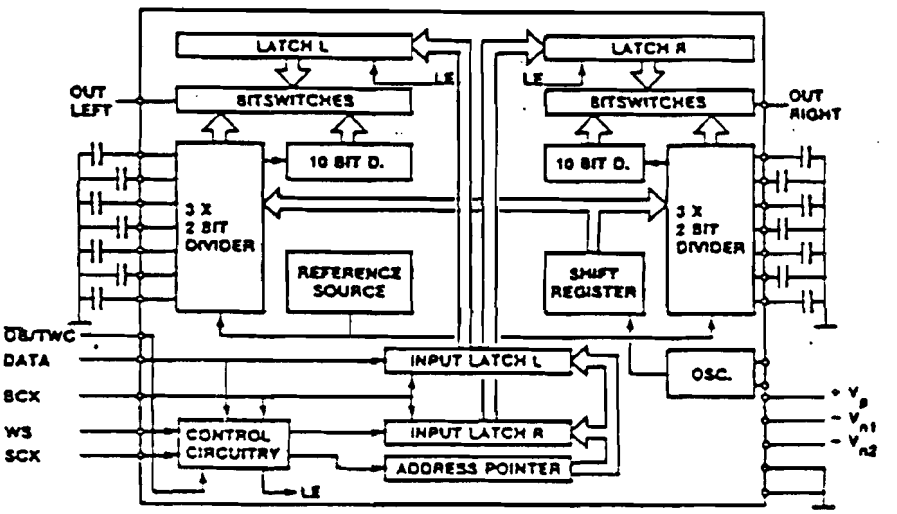

Figure 7.38 : Dual 16-bit D/A converter system diagram

ital TTL-compatible input data are applied to a shift register which transforms the serial input data into parallel format, which is latched and applied to the D/A converter switches. The data transfer between the integrated circuits is according to the Inter IC Signal standard (I^2S). In this system a 6-bit active division is combined with a 10-bit passive division to obtain a 16-bit accurate current network per D/A converter section. The number of external components can be minimized in this way.

7.18.1 16-bit converter data

In Fig. 7.39 the performance data of the dual 16-bit D/A converter TDA 1541 are given. Additional measured data are shown in Fig. 7.40 and Fig. 7.41. These figures show the signal-to-noise plus distortion as a function of amplitude and of frequency. As a result it can be said that using *Dynamic Element Matching* very high performance D/A converters can be built with

RESOLUTION		16	BIT
F.S. OUTPUT CURRENT	TYP.	4.0	mA
TEMPERATURE COEFFICIENT	TYP.	200	ppm/°C
DIFF. LIN. ERROR	MAX.	1.0	LSB
ABSOLUTE LIN. ERROR	MAX.	1.0	LSB
SETTLING TIME TO 1LSB	MAX.	1.0	µsec
CHANNEL SEPARATION	MIN.	90	dB
HARMONIC DISTORTION	MAX.	−96	dB
TEMPERATURE RANGE	TYP.	−20 TO +70	°C
POWER DISSIPATION	TYP.	800	mW
SUPPLY VOLTAGES	NOM	+5, −5, −15	V
PACKAGE	STANDARD 28 PIN PLASTIC DIL		
CHIP DIMENSIONS		3.8 * 5.43	mm

Figure 7.39 : 16-bit D/A converter data

a dynamic performance close to the theoretically attainable maximum. In

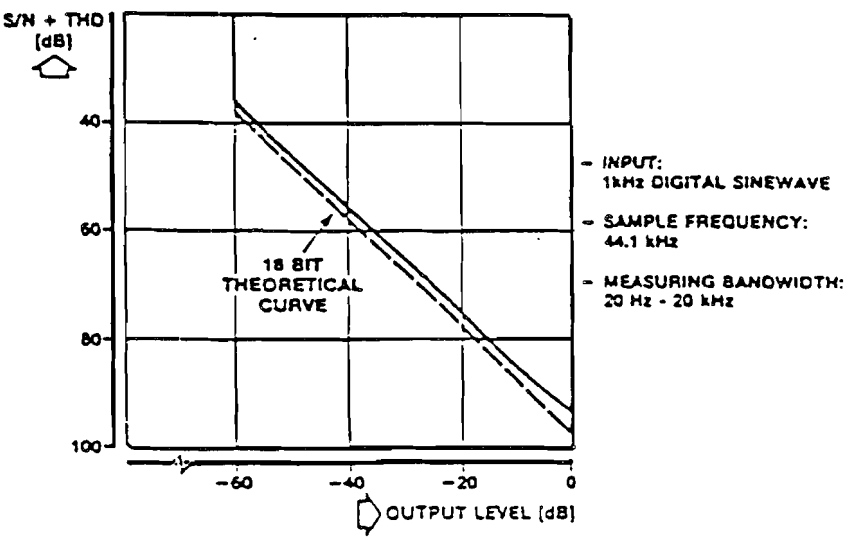

Figure 7.40 : Signal-to-noise plus distortion as a function of amplitude

Fig. 7.42 a die photograph of a 14-bit D/A converter is shown, while Fig. 7.43 shows a die photograph of a dual 16-bit D/A converter. Both converters are made using a bipolar process with double layer metal.

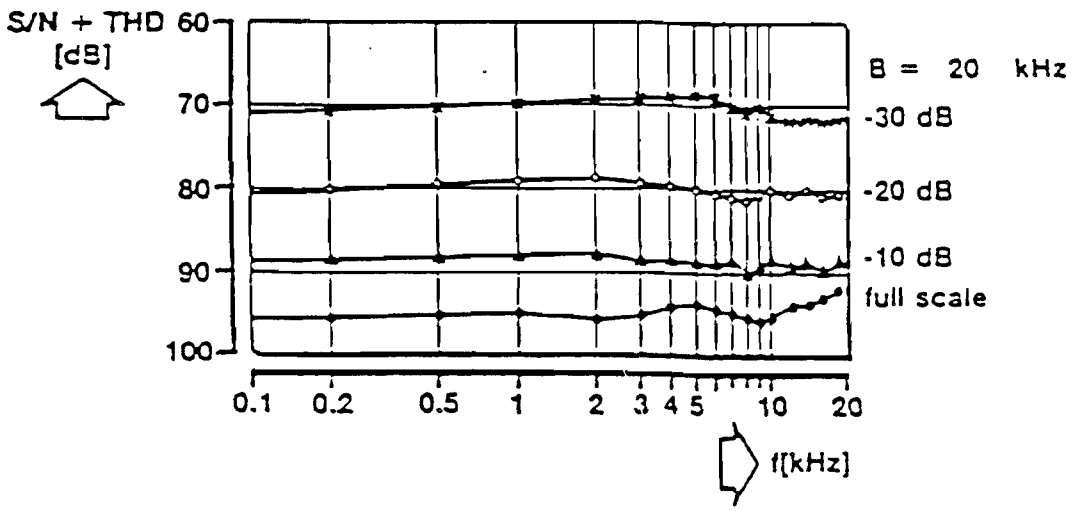

Figure 7.41 : Signal-to-noise plus distortion as a function of frequency

7.19 Current calibration principle.

In an MOS system it is possible to use a charge storage principle in an accurate current calibration system. In Fig. 7.44 the basic operation of the current calibration system is shown. The figure shows the calibration and the operational cycle. During calibration of the MOS current source, the MOS device M_1 is connected as a diode by closing switch S_1. The current I_{ref} is applied to the system and because of the diode connection of M_1, the gate-source voltage V_{gs} is adjusted in such a way that the drain current is made equal to I_{ref}. After the current has been calibrated to the reference value I_{ref} the switch S_1 is opened and the gate-source voltage of the transistor M_1 remains at the calibration value. The output switch S_2 is switched to the output terminal. At that moment a current I_{ref} will start to flow through the output terminal. As long as the capacitor C_{gs} is not discharged, the drain current remains at the value I_{ref}. In a practical configuration, however, the capacitor is discharge because of the gate leakage current of transistor M_1. Moreover, the charge feedthrough of the switch S_1 in case this switch is switched off, is added to the charge in C_{gs}. This means that the output current is not exactly equal to the calibration current value I_{ref}. In Fig. 7.45 the two dominant error sources are shown. The leakage current of the source-to-substrate diode of transistor M_2 discharges

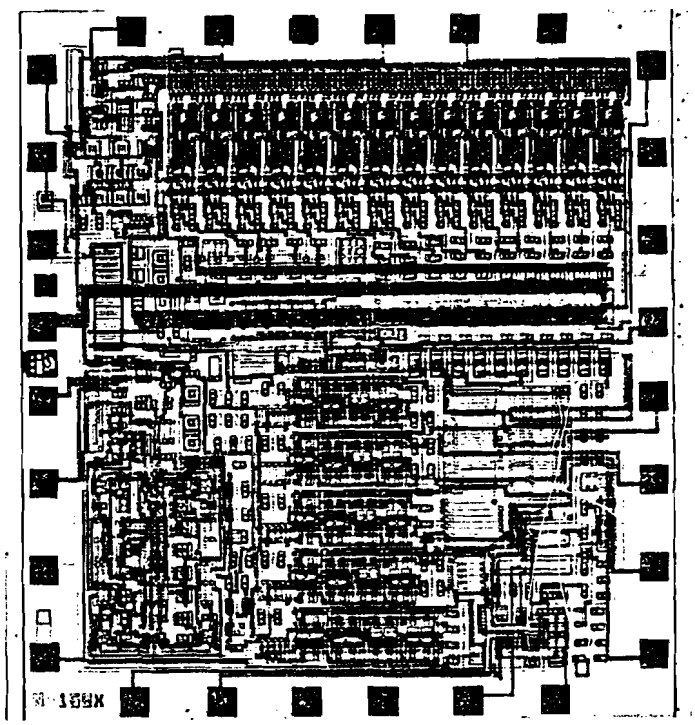

Figure 7.42 : Die photograph of a 14-bit D/A converter

the capacitor C_{gs}, while the charge feedthrough of this switch is added or subtracted from the charge on the capacitor C_{gs}. These error sources result in variations of the gate-source voltage of M_1 which results in output current variations between two repeating calibration cycles. In Fig. 7.46 the drain-source current of M_1 as a function of time is shown. During the time the current is compared with the reference current I_{ref} the same drain current is found. At the moment the switch S_1 is opened, the feedthrough charge is subtracted from the charge on the capacitor C_{gs}. As a result a decrease in output current is obtained. This is shown with the steep decrease in current just after switching of S_1. Then the leakage current discharges the capacitor

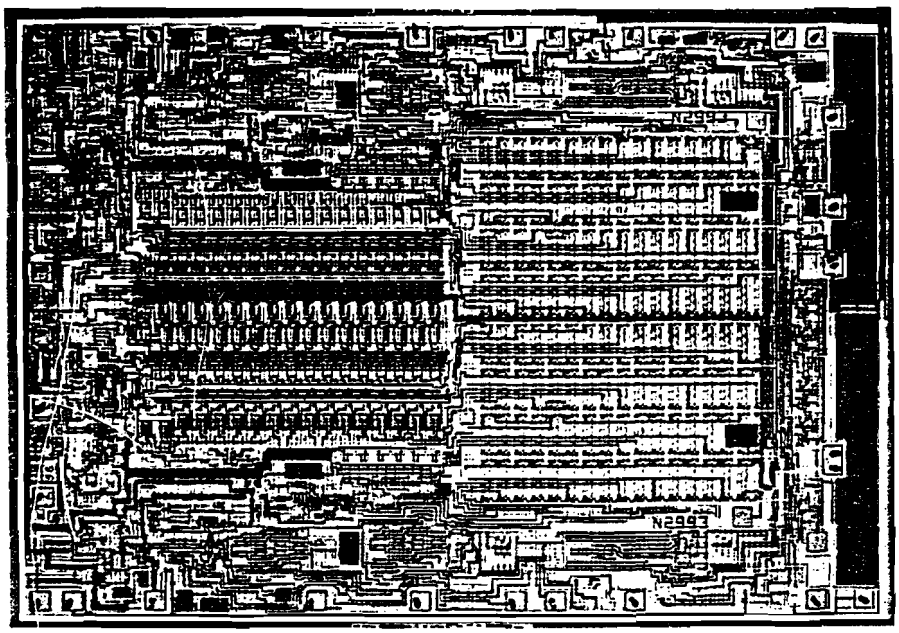

Figure 7.43 : Die photograph of a dual 16-bit D/A converter

resulting in a roughly linear decrease in output current. If at time t_c the calibration cycle starts again, the current is adjusted to I_{ref} and the cycle repeats.

7.20 Improved current calibration principle

To overcome the some of the problems encountered with the system shown in Fig. 7.45, the calibration is applied to the error current value only. The improved system is shown in Fig. 7.47. The basic system is equal to the circuit shown in Fig. 7.45. However, a current source I_m is added to the

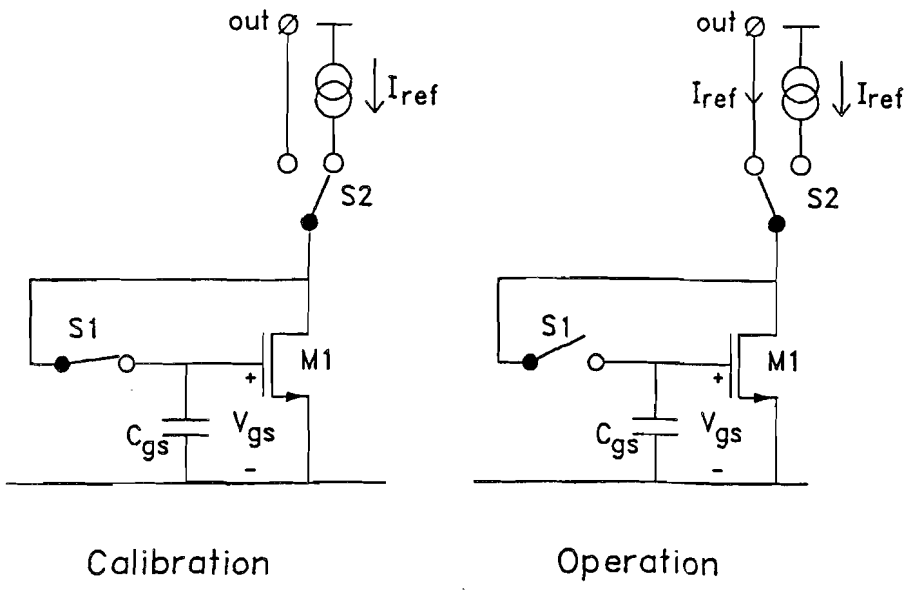

Figure 7.44 : Current calibration principle

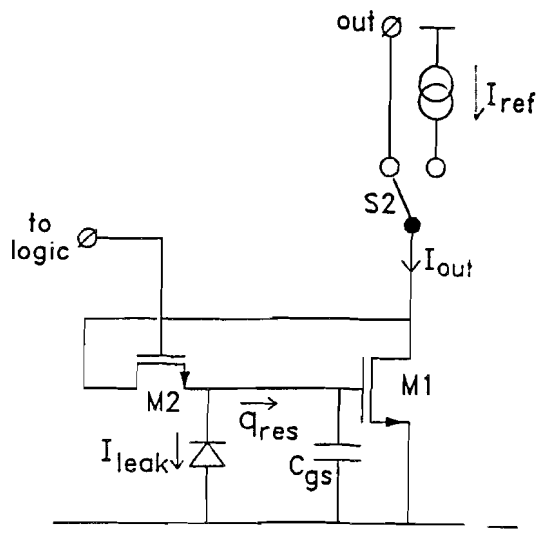

Figure 7.45 : Two dominant error sources

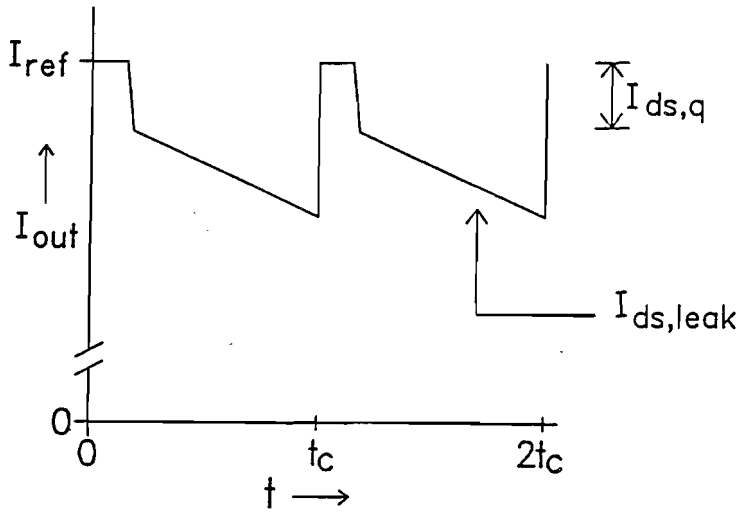

Figure 7.46 : Drain current of calibrated device as a function of time

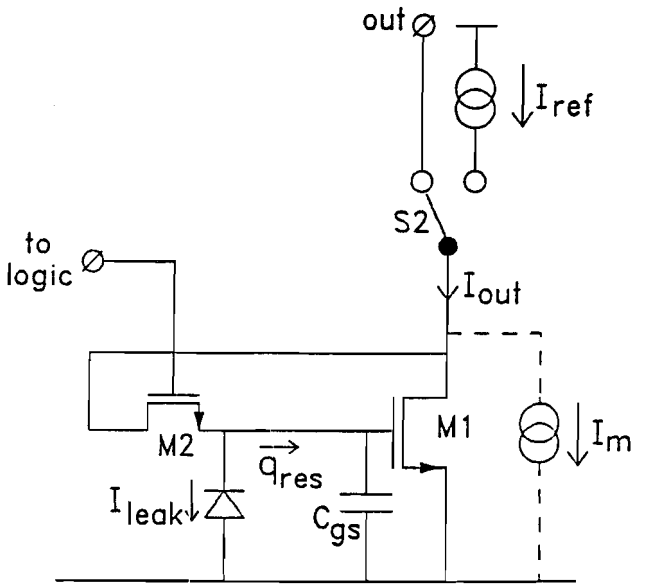

Figure 7.47 : Improved current calibration principle

system. The current value of I_m is close to the value of I_{ref}. The difference between I_{ref} and I_m is stored in M_1 during the calibration cycle. This

means that $I_m < I_{ref}$. In a practical case the difference current which can be stored in M_1 is between 0.1 and 0.05 of I_{ref}. Using this system the $\frac{W}{L}$ ratio of transistor M_1 can be chosen to minimize the g_m of the device. Moreover due to this device choice a large V_{gs} voltage is needed to drive the device. Charge feedthrough and leakage current influences can at least be reduced with a factor ten. As a result the calibrated current is much more accurate then was the case in the former system solution.

7.21 Continuous current calibration system

A system which uses a continuous current calibration is shown in Fig. 7.48. The systems consists of a $N+1$ -bit shift register and $N+1$ current sources.

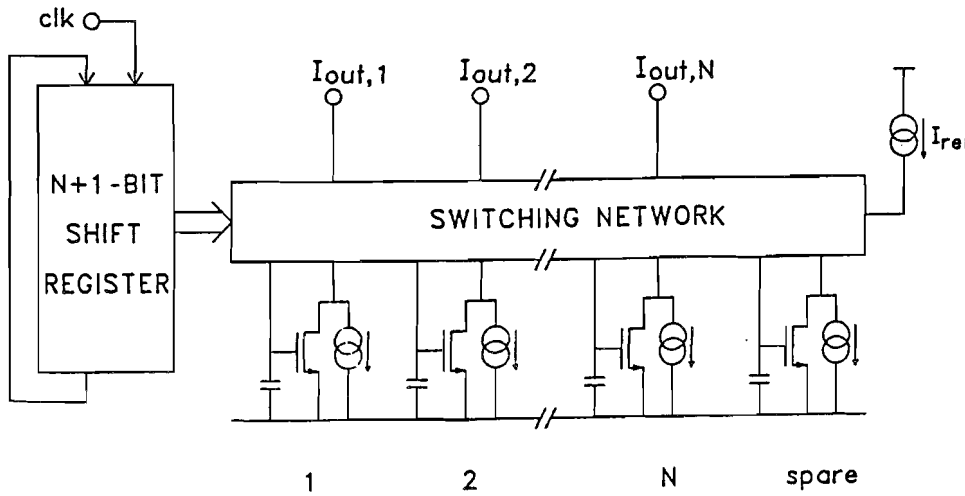

Figure 7.48 : Continuous current calibration system

The $N+1$ current source is called the "spare" source. The output of this system is N calibrated currents. The operation of the system is as follows. The $N+1$ stage shift register determines which current of the network is switched to the calibration source be be adjusted to the reference value I_{ref}. Successively every current is compared with the reference source I_{ref} and then inserted back into the system. The switching network performs the necessary switching operation to perform the calibration of every current source in the system. By using $N+1$ current sources no time is lost during calibration, because the current which is calibrated is replaced by the spare current source. In this way a continuous calibrated current network is

obtained.

7.22 Practical current calibration implementation

In Fig. 7.49 an example of a practical current calibration stage is shown. In

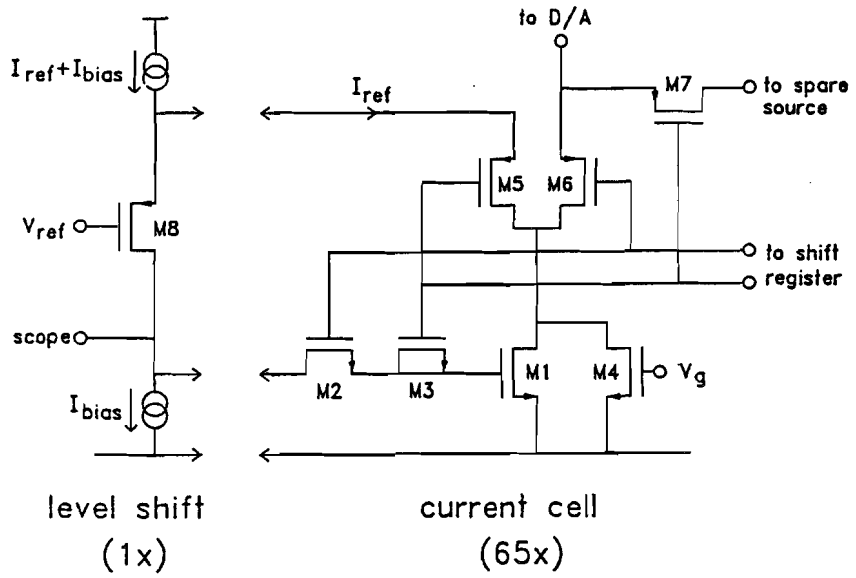

Figure 7.49 : Practical current calibration circuit

the circuit transistor M_4 supplies the current I_m from the previous circuit. This is the main current source. Transistor M_1 holds the calibration current which is added to obtain an accurate value of I_{ref} of the total output current. The switches M_5, M_6 and M_7 perform the switching from calibration to operation of the current cell. When transistor M_5 is switched on, the switch M_7 is switched on too and the spare current is applied to the bit switches in the D/A converter part. At the same time switch M_2 is on and transistor M_8 connects the drain of M_1 with the gate. Note that a current I_{bias} is added to the reference current I_{ref}. This bias current is forward biasing transistor M_8 and is subtracted from this reference current by the current source I_{bias}. In this way a good speed of transistor M_8 is obtained under all conditions. Transistor M_3 is added to the system to compensate for the charge feedthrough of M_2. Therefore the gate of M_3 is connected to the inverse control voltage applied to M_2.

7.23 16-bit D/A converter system

An example of an MOS calibrated 16-bit D/A converter system is shown in Fig. 7.50. The system consists of a 6-bit segmented current calibrated

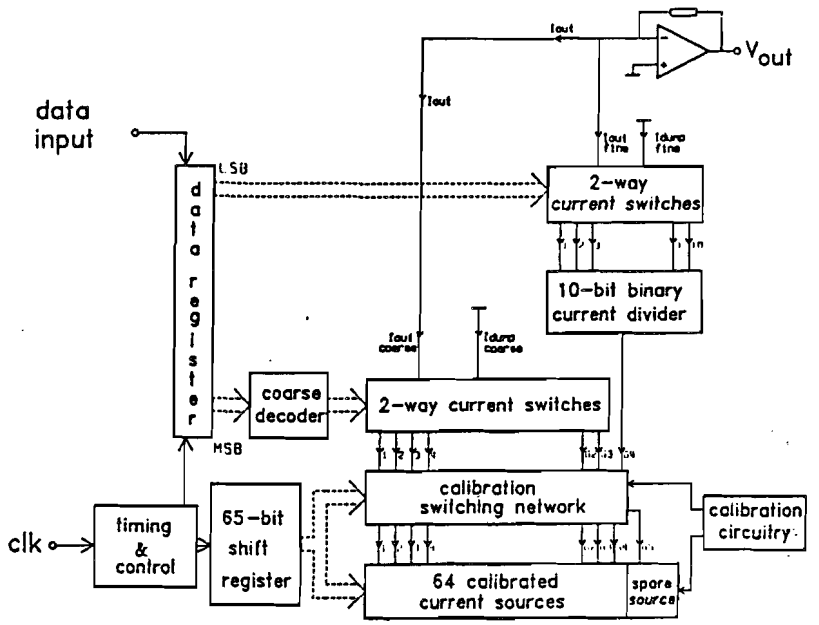

Figure 7.50 : 16-bit current calibrated D/A converter system

network to generate the sis most significant bits. Current "64" is applied to a 10-bit binary weighted network using source scaling. In this way a 16-bit binary weighted current network is obtained. The digital input data which must be converted into an analog value is stored in the data register. The outputs of this data register controls the bit switches which switch the weighted currents to the output to obtain the converted analog value. The output current of the converter is converted into a voltage using an operational amplifier with a resistive feedback. To minimize the glitches which occur during the switching from calibration into output current generation of the MSB calibrated currents a deglitcher can be implemented before the total output current is applied to the current to voltage converting operational amplifier. Another possibility exists by operating the deglitcher and calibration cycle at the same time a the digital data applied to the switches is refreshed. A synchronization between shift register clock and input data

clock is required.

7.24 Measurements

7.24.1 Integral non-linearity measurement

In Fig. 7.51 the result of the integral non-linearity measurement of the system shown in Fig. 7.50 is shown. Due to the segmented construction of

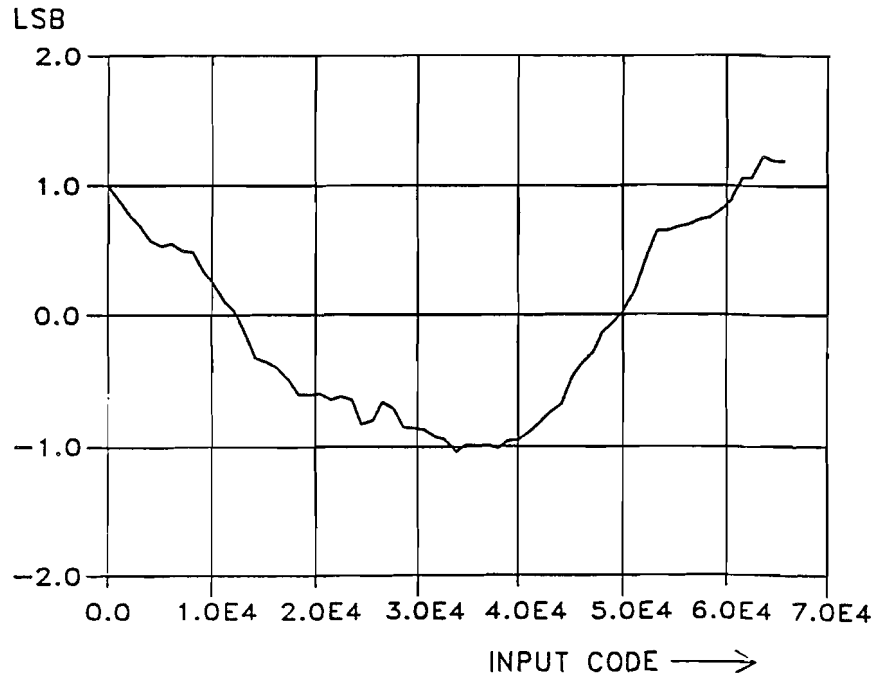

Figure 7.51 : Integral non-linearity measurement result

the converter *monotonicity* is guaranteed while the integral non-linearity in this case equals ± 1 LSB. The curve characteristic shows a strong dependence of the calibration accuracy on the position of the calibrated weighted current values. Improvements are still possible to obtain a full 16-bit accuracy.

7.24.2 Dynamic performance measurement

In Fig. 7.52 the measurement result of signal-to-noise plus distortion is shown as a function of the output amplitude. The measurement result shows that the dynamic performance is close to the expected theoretical value.

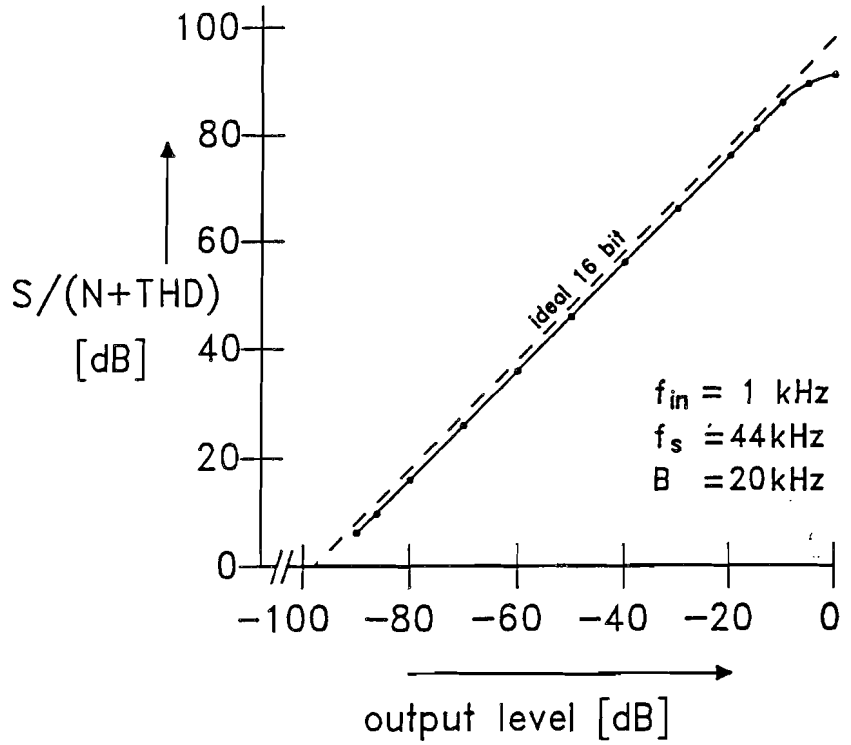

Figure 7.52 : Signal-to-noise plus distortion as a function of amplitude

7.24.3 D/A converter specifications

In Fig. 7.53 the specifications of the complete MOS 16-bit D/A converter are shown.

7.25 High-accuracy A/D conversion

In integrating type of high-resolution A/D converters basically the analog input signal is converted into a time which is proportional to the input signal. Time is measured using a counter with an accurate clock. These systems are relatively slow because of the counting operation in the time-to-number conversion cycle. A speed improvement is obtained by using a coarse- and fine conversion cycle in the time-to-number counting operation. In fast and highly accurate A/D converters, the successive approximation method is commonly used. Accuracy and linearity in this system are de-

resolution	16 bit
dynamic range	94 dB
S/(N+THD) at 0 dB	92 dB
at −10 dB	84 dB
supply voltage range	3 to 5 V
power dissipation	20 mW at 5V
temperature range	−10 to 70 °C
process	1.6 µm CMOS
active chip area	3 mm^2

Figure 7.53 : 16-bit D/A converter specifications

termined by the D/A converter, while the conversion speed depends on the comparator response time and the settling time of the D/A converter. In a successive approximation system the analog input signal is approximated by the step-by-step built-up analog output voltage of the D/A converter, starting with the most significant bit. To obtain the high accuracy for the D/A converter needed to construct a 14- to 16-bit A/D converter *Dynamic Element Matching* is used. In the 14-bit A/D converter, [3], which will be discussed in the following sections the 14-bit D/A shown in Fig. 7.37 is used. Due to the construction of the bit switches, which in the high-accuracy part consist of a diode-transistor configuration, the output voltage swing at the D/A current output must be small. This voltage swing, called output voltage compliance, reduces the effective bit drive voltage of the D/A converter. To avoid problems in this system a special comparator operation is needed. In general-purpose A/D converters, a general non-linear comparator circuit with high gain around the zero-crossing level is used. Such comparators generally have a certain voltage compliance which is above the range needed for the D/A converter from Fig. 7.37. Therefore a wide band, high-speed operational amplifier with diode clamps is applied in the inverting mode. The voltage compliance in this case remains below a few milli volts. This is accurate enough to obtain the full accuracy of the D/A converter.

The ease with which a hold operation can be constructed allows an A/D converter implementation using a cyclic converter algorithm. In the cyclic converter the number of components is drastically reduced and consists of two sample-and-hold amplifier circuits with an accurate 2 times amplifier stage and a subtractor circuit. Per conversion step the remaining signal is compared with a reference signal. If the remainder is larger than the reference signal then a subtraction of the reference signal from the remainder is performed. The error signal which is then generated is amplified by two and compared with the reference signal again. This operation is repeated until the total number of bits which can be converted is obtained.

7.26 Single slope A/D converter system

In Fig. 7.54 a block diagram of a single slope A/D converter is shown. The

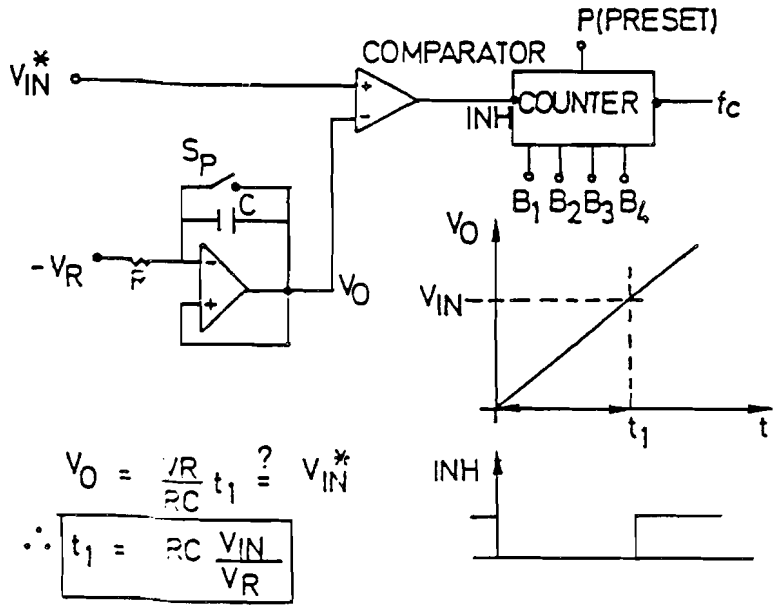

Figure 7.54 : Single slope A/D converter system

circuit consists of a resettable integrator, which generated the accurate reference ramp signal, a comparator and a counter. The input signal is applied to one input of the comparator. At the moment the conversion starts, the counter is set at zero and the integrator is reset by closing switch S_p. When a positive input signal V_{in} is applied, the integrator starts generating the ramp function. In the meantime a gate is opened which applies counting signals

to the counter. At the moment the output signal of the integrator equals the input signal, the gate is closed and the counter stops. The analog input signal is converted into a time which is measured by counting clock pulses during that time. An accurate time-to-number conversion is obtained. The accuracy of the system is determined by the clock generator, the RC time constant of the integrator and the reference source V_R. A simple calculation shows that the time to which an input signal is converted is equal to:

$$t_1 = RC\frac{V_{in}}{V_R}. \tag{7.27}$$

The digital output value then becomes:

$$N_{digital} = t_1 \times f_{clock}. \tag{7.28}$$

Offset of the comparator can be canceled by measuring the offset with a zero input signal. This offset number can be used to preset the counter. In this way an automatic offset compensation is obtained.

7.27 Dual slope A/D converter system

To overcome a number of the accuracy problems encountered with the system from Fig. 7.54 a dual slope system has been designed. A system diagram is shown in Fig. 7.55. The system consists of an input switch, an integrator with a comparator, a clock generator with control logic and a counter. The operation of the system is as follows. Starting from a resetted integrator, the input signal V_{in} is integrated during a time t_1 which corresponds with a full count of the counter. Then the input is switched to the reference voltage V_R having the opposite sign compared to the input signal. The integrator is now discharged. During the discharge time pulses are counted. Counting stops when the comparator detects zero. As a result the counts in the counter represent the digital value of the input signal. A simple calculation shows:

$$V_{in} = V_R \times \frac{T_2}{T_1} \tag{7.29}$$

Here T_2 is the time during which the integrator is discharged from the integrated input signal to zero. As is shown in equation 7.29 the clock is not critical, only the ratios between the charge and discharge times is important. A disadvantage of this system is the low conversion time if a high resolution is required. In digital voltmeters these systems are very popular.

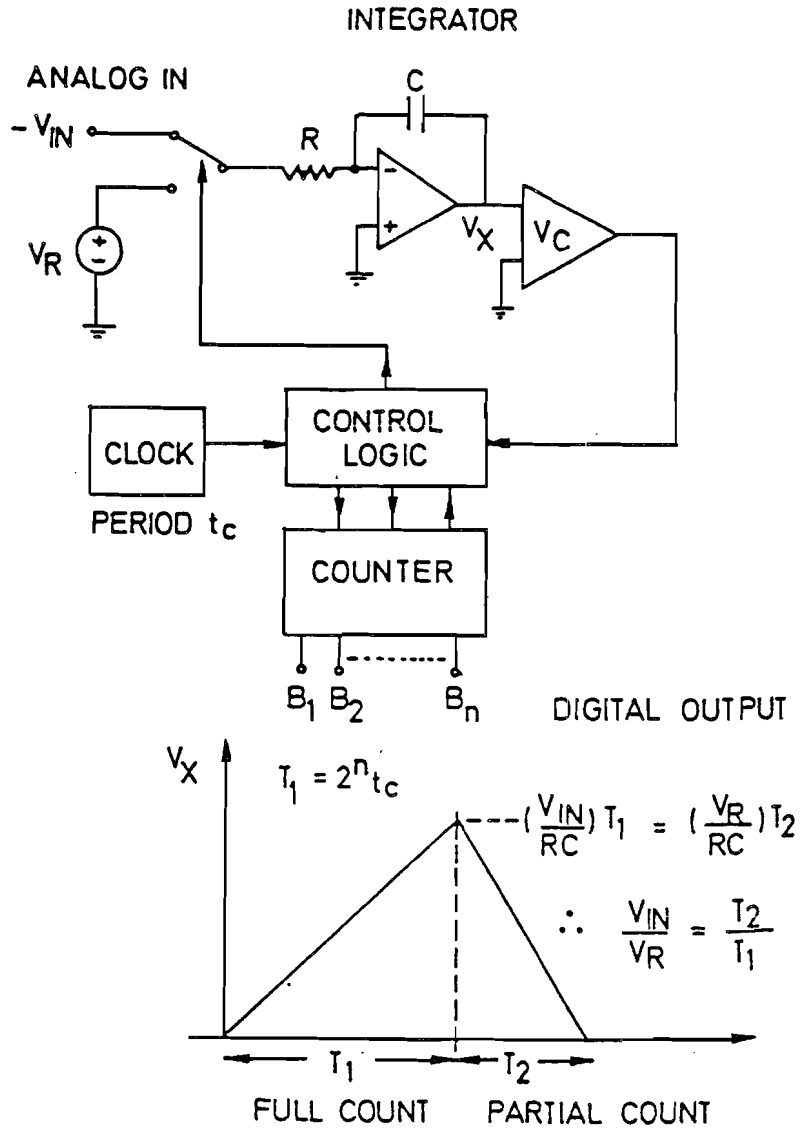

Figure 7.55 : Dual slope A/D converter system

7.28 Dual ramp single slope A/D converter system

To decrease the conversion time of the single slope A/D converter as shown in Fig. 7.54 a dual ramp system has been designed. The block diagram

of the dual ramp converter is shown in Fig. 7.56. The system consists of

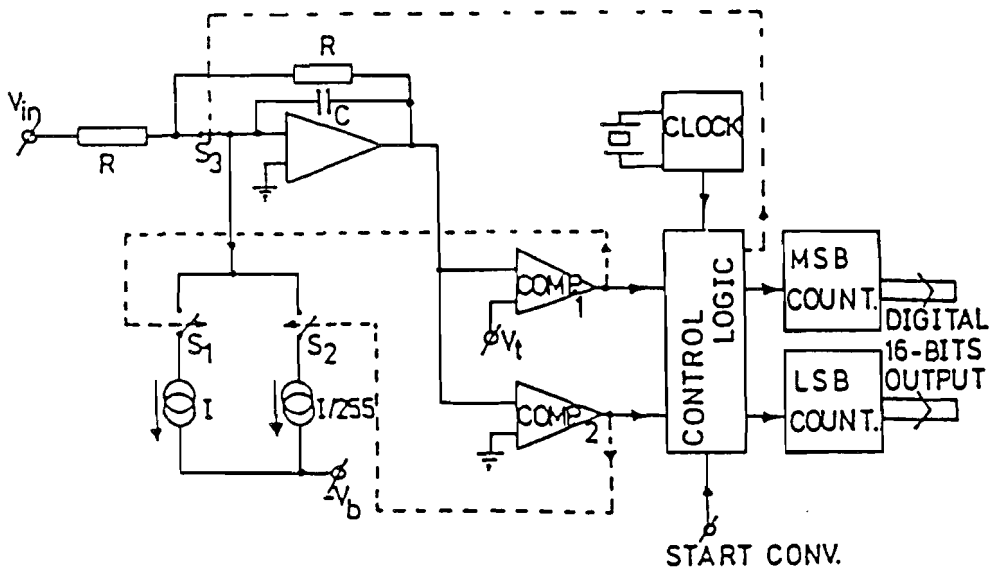

Figure 7.56 : Dual ramp single slope A/D converter system

an inverting sample-and-hold amplifier with feedback resistors R and hold capacitor C, two reference current sources with current values I and $\frac{I}{256}$, comparator $comp_1$ with threshold voltage V_t and comparator $comp_2$ which control the coarse and fine counting operation using the control logic function, a clock generator and a coarse and fine counter. At the start conversion, the counters are set to zero and the switch S_3 is closed. Switches S_1 and S_2 are open, so no current flows into the sample-and-hold integrator. Closing switch S_3 causes the operational amplifier to act as an inverter charging the hold capacitor C. At the moment switch S_3 is opened the input signal is sampled and hold on the capacitor C. Then switch S_1 is closed and the reference current I starts discharging the capacitor until the output signal of the integrator reached the threshold voltage V_t. During the discharge time pulses are counted in the MSB counter which is able to store a maximum of 255 pulses. However, the threshold voltage V_t applied at comparator $comp_1$ is larger than the voltage which can be obtained during a full count of the fine counter (255 pulses) and integrating a current $\frac{I}{256}$ on the capacitor C. This threshold voltage is not at all critical as will be explained later on.
After that comparator $comp_1$ detected the threshold voltage V_t, switch S_1 is opened and switch S_2 is closed. At the same time the fine counter starts

counting clock pulses until comparator $comp_2$ detects zero. If the number of clock pulses applied to the fine counter is larger than the number it can store (in this case 255 pulses), then a carry is generated which is applied to the coarse counter and increases the count of this counter with on count. In this way an automatic adjustment of the threshold voltage V_t is obtained. At the output of this system a 16-bit digital number is obtained which corresponds with the analog input signal. The speed of this system is increased with a factor 256 divided by 2 equals 128 times. Using a very high counting clock it is possible co obtain a 16-bit A/D conversion with a conversion speed of about 44 kHz.
In Fig. 7.57 the output signal of the sample-and-hold amplifier/integrator as a function of time is shown. The coarse and fine discharging period are

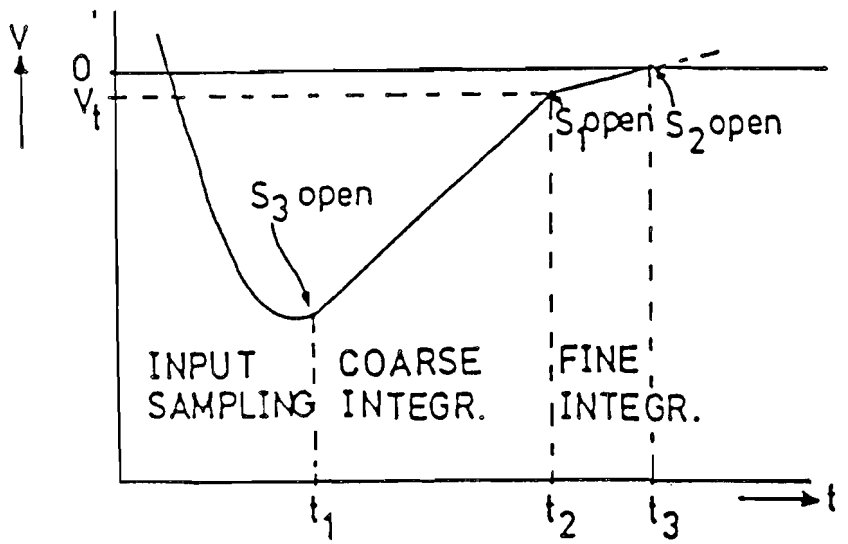

Figure 7.57 : Output signal of the sample-and-hold/integrator amplifier

clearly distinguishable in the figure.

7.28.1 Accuracy analysis of the dual ramp A/D converter

In Fig. 7.58 the output signal of the sample-and-hold amplifier/integrator is shown. Note that the coarse current value is equal to $I + \frac{I}{255}$ and the fine current value is equal to $\frac{I}{255}$. This construction is used because a large current can be switched better at high speeds than a small current. This means that $\frac{I}{255}$ is always switched to the integrator. The ratio between the

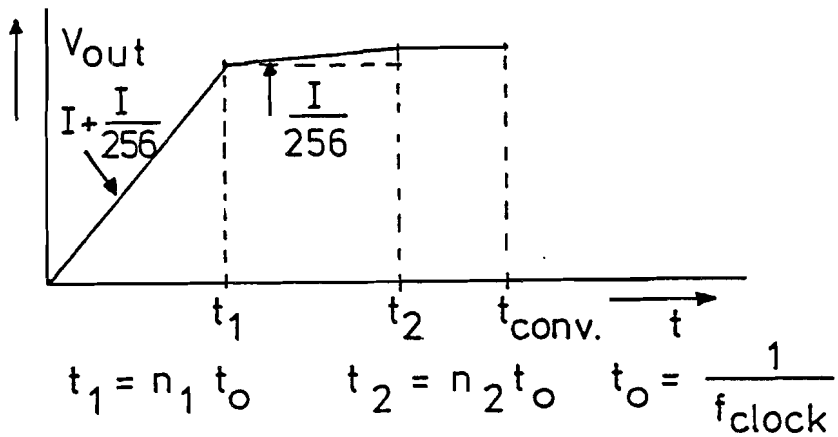

Figure 7.58 : Styled output signal of the sample-and-hold/integrator amplifier

currents is 1 to 256 which is required in this system.
Suppose that the current $\frac{I}{255}$ has an accuracy of $(1 - \delta)$, then after a full count of the fine integrator the error between the coarse current and the full fine integrated current value must be smaller than k LSB or:

$$I + \frac{I}{255} \times (1 - \delta) - 256 \times \frac{I}{255} \times (1 - \delta) \leq k \times \frac{I}{255}, \tag{7.30}$$

or

$$\delta \leq \frac{K}{255} \tag{7.31}$$

In a 16-bits system a matching between the coarse and fine discharge currents better than 0.2 % is needed to obtain $\frac{1}{2}$ LSB differential linearity.
The accuracy with which the currents must be switched can be determined. Suppose that the clock time $t_0 = \frac{1}{f_{clock}}$ then with a time uncertainty in switching the current I of δt we obtain in case the fine full scale integrated value must be smaller than k LSB error:

$$I \times (t_0 + \delta t) + \frac{I}{255} \times t_0 - 256 \times \frac{I}{255} \times t_0 \leq k \times t_0 \times \frac{I}{255}, \tag{7.32}$$

or

$$\delta t \leq \frac{k}{255} t_0. \tag{7.33}$$

With $t_0 = 40$ nsec and k = $\frac{1}{2}$ LSB we get $\delta t = 80$ psec.

7.29 Successive approximation converter system

A block diagram of the A/D converter system is shown in Fig. 7.59. The

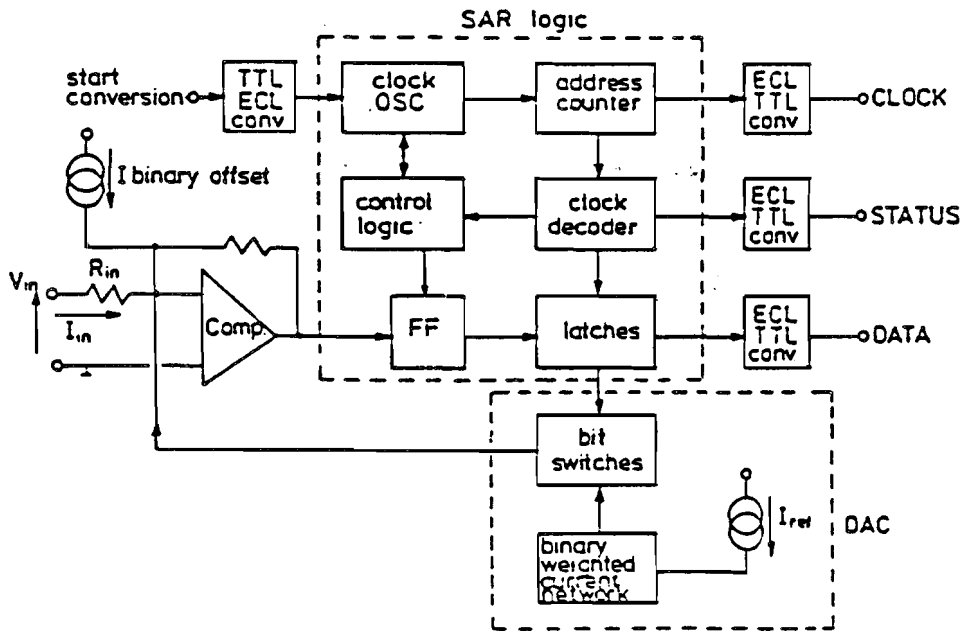

Figure 7.59 : Block diagram of the A/D converter system

most important parts are the successive approximation logic, the D/A converter with the reference current source, the subtractor-comparator circuit using an operational amplifier to convert the analog input signal into a current, and the internal clock generator with the control logic. Digital input and outputs are TTL compatible. In the internal digital part current mode logic (CML) is used for speed. Because of the differential operation of the current mode logic low interference of the switching signals on the power supply lines is obtained. At the input a TTL-to-CML logic converter stage is incorporated, while at the output CML-to-TTL levels converters with output buffers are used. A scheme with addressable latches is used in the successive approximation register to minimize the number of components. Output data flow of the converter is in a serial mode to minimize the number of circuit pins and to reduce the noise generated by the TTL output signals. The start conversion pulse activates the internal clock and control logic for one conversion cycle. A constant "trial-and-decision" time period

is used, except for the most significant bit which has a 50 percent longer decision time. A special output signal, "enable status", is available during the time in which the conversion is performed. With this signal an external sample-and-hold function can be switched from sample into hold mode. The aperture jitter of the enable pulse, which switches the sample-and-hold amplifier from sample into hold mode, is kept below the theoretical limit defined by the resolution and the maximum signal frequency. Then conversion starts. Because of the voltage-to-current input mode configuration, the input voltage signal is converted into a current by the resistor R_{in}. An extra binary offset current equal to the most significant bit value is available at the input of the converter to allow bipolar signals to be converted into offset binary output code.
All circuitry to operate the A/D converter is on chip except the input sample-and-hold amplifier, filtering capacitors to remove the ripple from the interchanging network and gain-setting resistors.

7.30 Comparator-subtractor circuit

As already said, a high-speed operational amplifier in the inverting mode is used for subtraction of the D/A converter output current from the analog input current. A simplified circuit diagram is shown in Fig. 7.60. A wide

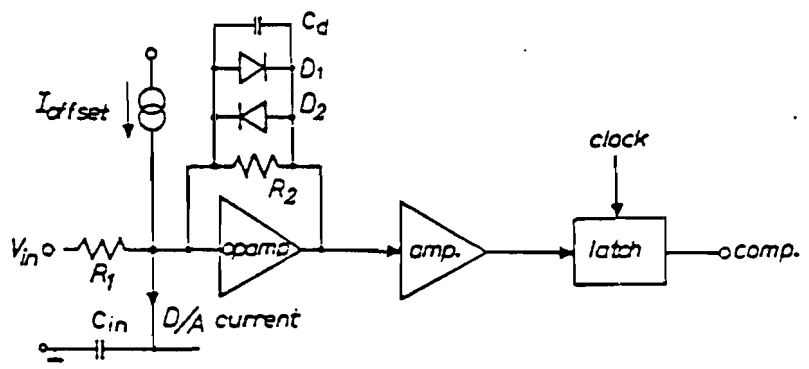

Figure 7.60 : Comparator-subtractor circuit diagram

band feed-forward coupled operational amplifier with a unity-frequency-compensated bandwidth of 75 MHz is used. A high-value feedback resistor R_2 is used to have a large gain around the zero crossing of the signal. Diodes

D_1 and D_2 are connected in parallel with the resistor R_2 to prevent large output voltage swings, which maybe even larger than the applied supply voltage of the converter, being generated at the output. With these diodes, the input voltage excursion remains very small, thus having no influence on the D/A converter performance and the input voltage-to-current transformation. Speed limitations in the system are due to the diode capacitance C_d across the feedback resistor R_2 and the input capacitance C_{in}. The output capacitance of the D/A converter in this case is the dominating contributor to the input capacitance C_{in}. In practice using a standard bipolar process, a value of approx. 20 pF for C_{in} is found. The comparator bandwidth with a diode capacitance C_d of 2 pF is limited to about 4 MHz. To make the bandwidth of the total system only dependent on the feedback and loading elements of the operational amplifier a minimum compensated unit gain bandwidth of 40 MHz is required. With a practical designed limit of 75 MHz this demand is easily fulfilled. The output signal of the operational amplifier is further amplified and then latched into a current mode logic master-slave flip-flop. This flip-flop converts the comparison information into current mode logic levels, which are applied to the successive approximation logic to perform the complete conversion cycle. A total average settling time of the D/A converter currents of 400 nsec to $\pm\frac{1}{4}$ LSB is obtained with this comparator system. The low noise of the filtered bit currents of the D/A converter and a low noise design of the operational amplifier keep the total noise in the system below $\frac{1}{3}$ LSB, which is small enough to obtain a good dynamic performance of the converter.
The low offset voltage of the operational amplifier (below 0.5 mV) does not need an extra offset trim of the comparator with sufficiently large input voltage. An extra current which is equal to the most significant bit current value is available at the input of the operational amplifier to allow a bipolar signal operation of the A/D converter.

7.31 Complete practical A/D converter

The total A/D converter is implemented using a standard bipolar technology and needs a chip size of 3.5x4.4 mm^2. Double-layer metallization simplifies circuit layout and improves performance. A die photograph of the chip is shown in Fig. 7.61. In the layout special guard rings are added to separate accurate and sensitive analog parts from the digital part of the circuitry. Supply connections for the analog and the digital circuit part of the system

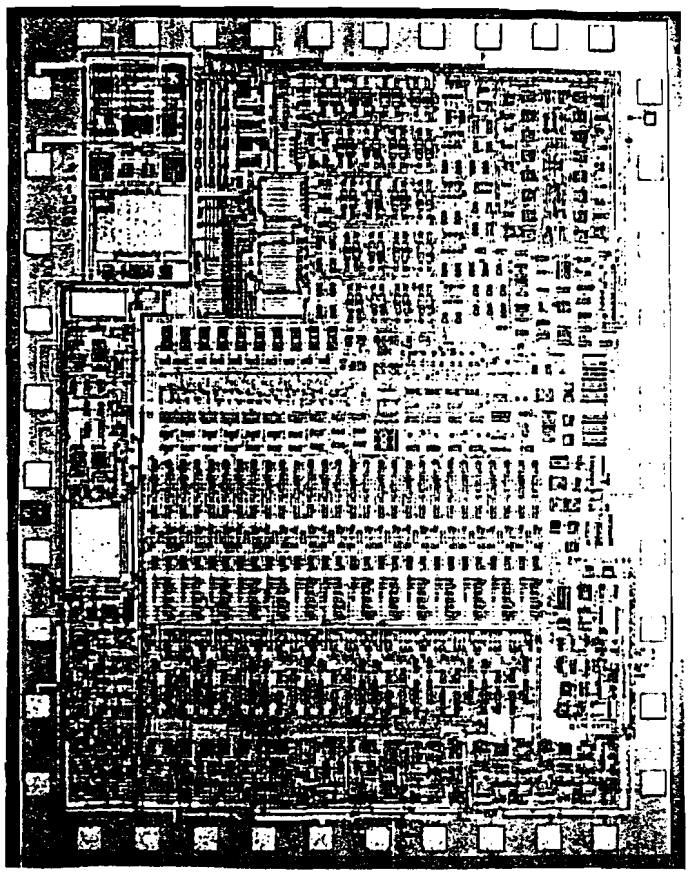

Figure 7.61 : Die photograph of the 14-bit A/D converter

are separated to avoid interference and noise inductions due to the operation of the circuit. To operate the converter, a sample-and-hold amplifier, a number of resistors and some filtering capacitors are needed.

7.32 Measurements

An A/D-D/A converter loop has been built to obtain quick and reasonably accurate information about conversion time, linearity, signal-to-noise ratio, distortion, etc. of the A/D converter. During dynamic measurements a sample-and-hold module with sufficiently high performance is used. Ana-

log low-pass filters have enough stopband attenuation ($\approx$ 100 dB) to allow accurate measurements. In Fig. 7.62 the block diagram of the test set-up with the specified measurement instruments is shown. In Fig. 7.63 the to-

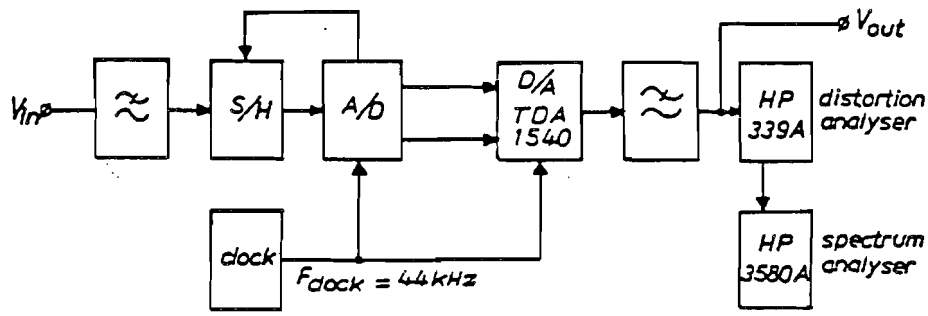

Figure 7.62 : A/D converter measurement test set-up

tal signal-to-noise plus distortion ratio as a function of conversion time is shown. During the measurement procedure of this curve only the conversion time is changed. All other system parameters are maintained at the basic settings. From Fig. 7.63 a conversion time of 7 μ sec is obtained. A loss in S/N with respect to long conversion times of 1 dB is used as a test criterion. In Fig. 7.64 the signal-to-noise as a function of amplitude is shown, while Fig. 7.65 the signal-to-noise as a function of frequency for various amplitude levels is plotted. Additional information about the performance of the A/D converter chip is shown in Table II.

7.33 Algorithmic A/D converter

A block diagram of a cyclic (algorithmic) A/D converter is shown in Fig. 7.67. The system consists of a times two differential amplifier with a built-in hold function, a sum/subtractor circuit, a comparator, a reference source and a sample-and-hold amplifier. The multiplexer at the input switches the input of the times two amplifier between the input terminal of the output of the sample and hold amplifier. The conversion starts by sampling the input signal V_{in} and amplifying this signal with an accurate factor of two. The signal is then apllied to the comparator which subtracts or adds the reference voltage V_{ref} to the two times amplified input signal. A reference source operation is performed when the comparator detects a signal larger

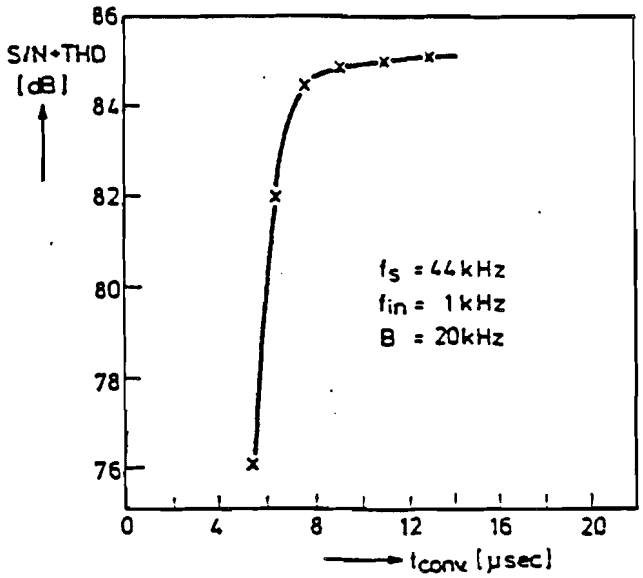

Figure 7.63 : S/N plus distortion as a function of conversion time

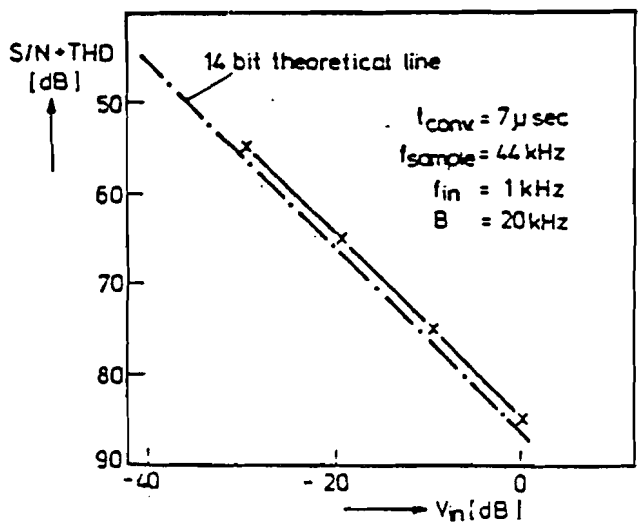

Figure 7.64 : S/N plus distortion as a function of amplitude

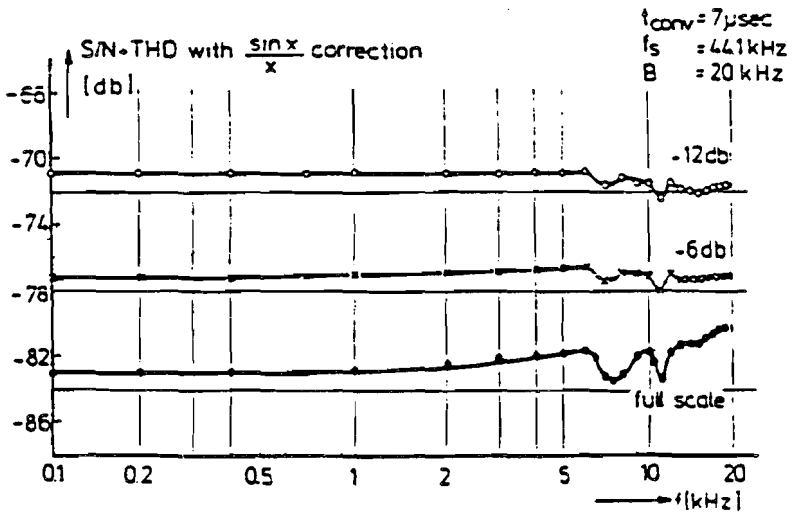

Figure 7.65 : S/N plus distortion as a function of frequency

Resolution	14 bit
Linearity	$\pm\frac{1}{4}$ LSB
Analog input	±2 mA
Minimum conversion time	7 µs
Logic input and output levels	TTL compatible
Output data	Serial/offset binary code
Supply voltages	+5 V, -5 V, -17 V
Power dissipation	450 mW
Temp. coef. ref. source	±0.5 ppm/°C over 100°C
S/N ratio	84 dB, F_{sample} = 44.1 kHz, B = 20 kHz
Distortion f_{in} = 1 kHz	<96 dB
Package	40 pins
Chip dimensions	3.5 X 4.4 mm²

Figure 7.66 : 14-bit A/D converter data

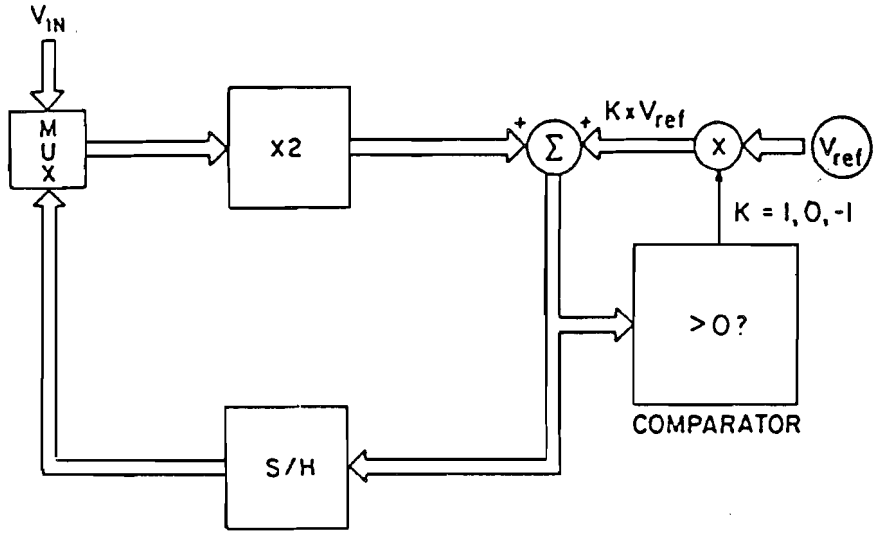

Figure 7.67 : Algorithmic A/D converter system

than zero. The positive error signal is transferred to the sample-and-hold amplifier. In the meantime the multiplexer is switched to the output of the sample-and-hold amplifier. The remaining signal is amplified by the two times amplifier and a reference operation is performed again. This cyclic comparison, subtraction and signal transfer is repeated depending on the number of bits the converter is operating with. A cyclic output code appears at the output of the comparator. The only accurate element in the system is the times to amplifier and the subtractor/summator circuit with the reference source.

In Fig. 30 a detailed operation of the accurate times two amplifier system is shown. The operation of the system is based on the addition of two sampled signals on two capacitors. In Fig. 7.68a the input differential signal is sampled on the capacitors C_1 and C_2 while at the same time the input offset voltage is ampled on capacitors C_3 and C_4. In Fig. 7.68b the input signal charge is transferred from capacitors C_1 and C_2 to capacitors C_3 and C_4. The second input sample is taken as shown in Fig. 7.68c. Capacitors C_3 and C_4 are disconnected and therefore do not get any charge. The input sample is stored on capacitors C_1 and C_2. The repeated addition of the two samples is shown in Fig. 7.68d. The voltage across C_3 is added to the voltage across C_1 and gives a doubling of the input signal. An identical operation is found for the voltages across C_4 and C_2. The sampling of the signal

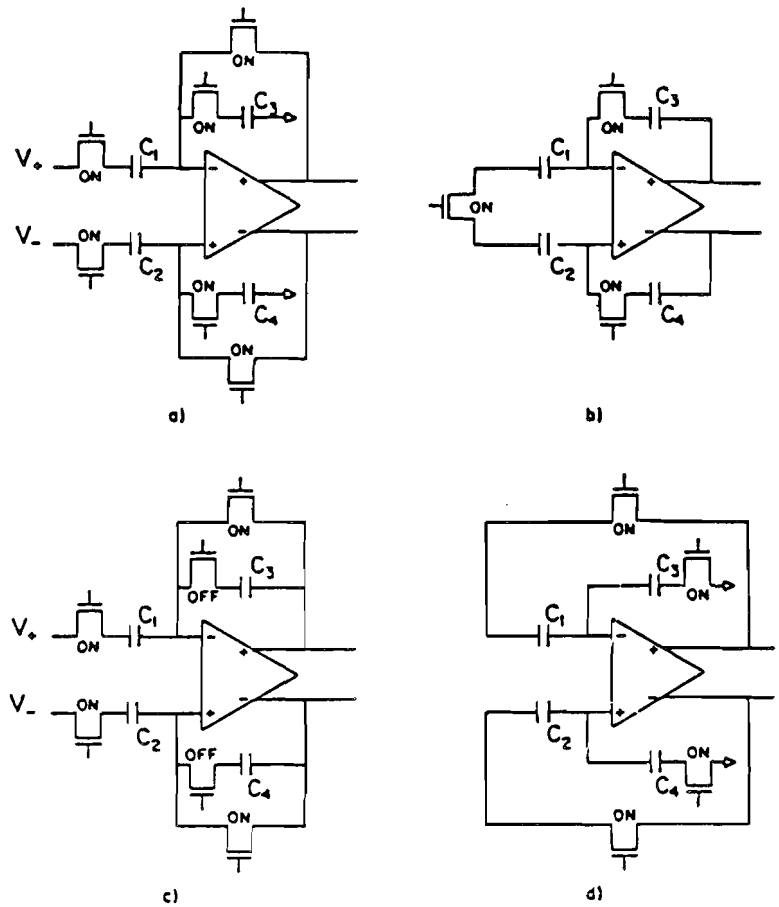

Figure 7.68 : Detailed operation of the accurate times two amplifier

accurately stores the input voltage on a capacitor, while due to the charge transfer it can be shown that an offset correction occurs. Furthermore the system is nearly independent of the capacitor mismatching. In Fig. 7.69 the complete analog part of the A/D converter is shown. Amplifier A_1 with the surrounding switches performs the accurate times two amplification with the subtraction or addition of the reference value. Note that by inverting the reference voltage to capacitor C_5 or capacitor C_6 a subtraction or addition can be performed without loosing accuracy. Amplifier A_2 with capacitors C_7 and C_8 perform an offset independent sample-and-hold amplifier function. Capacitors C_9 and C_{10} with the amplifier perform an accurate comparison with zero. The output signal of the comparator is stored in the output latch

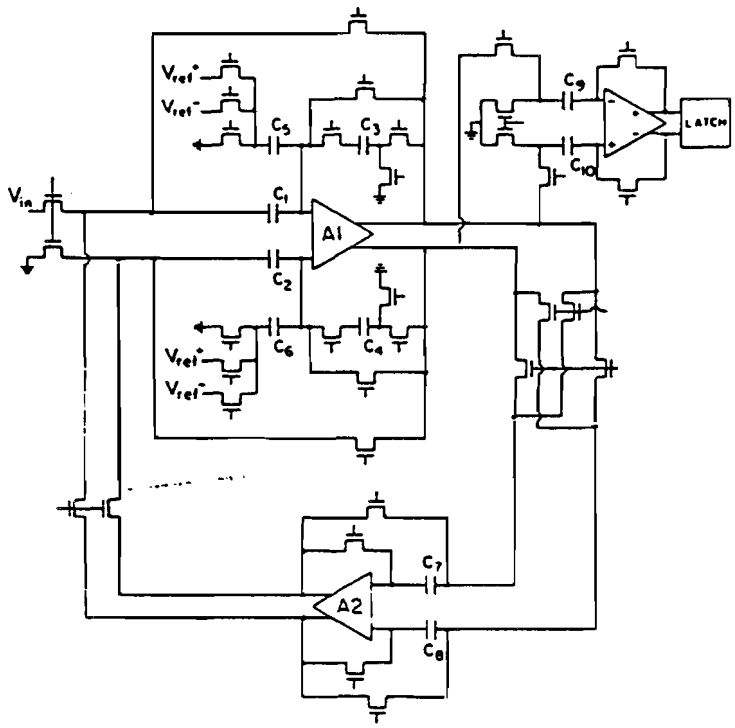

Figure 7.69 : Complete analog part of the A/D converter

and can be transferred as a series output signal of the converter.

7.34 Self-calibrating capacitor A/D converter

In Fig. 7.70 a block diagram of a self-calibrating A/D converter is shown. The system consists of a 10-bit weighted capacitor D/A converter combined with a 5-bit resistive divider sub D/A converter. A 7-bit calibration D/A converter is used to calibrate the errors from the weighted capacitor D/A converter and the resistive divider sub D/A converter. The calibration of the main D/A converter plus the sub D/A converter is performed by comparing every major carry transition of the main D/A converter. In a 10-bit system it is only necessary to calibrate only the 5 to 6 MSB bits. Errors which are found are stored in a RAM memory and the error signal is generated by the calibration D/A converter and added to the main D/A output signal every time an successive approximation is performed. At predetermined time

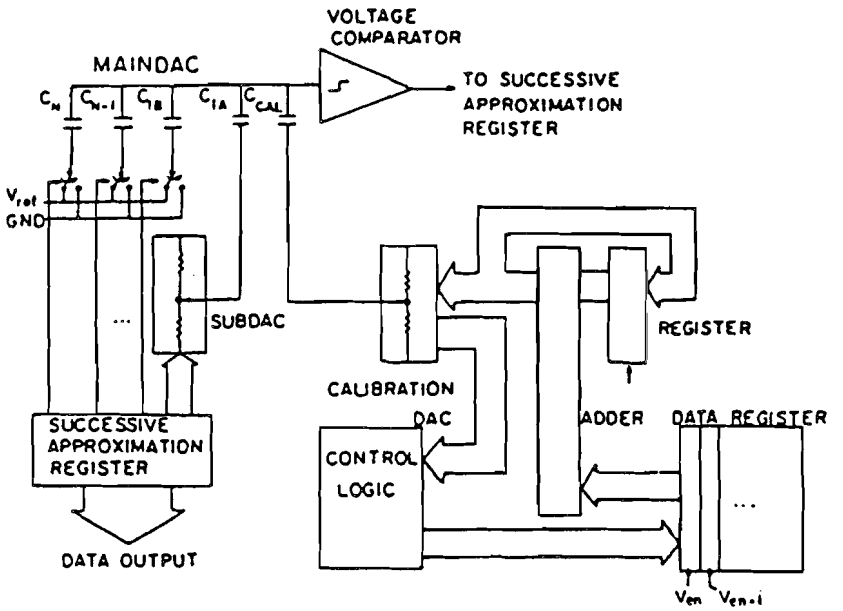

Figure 7.70 : Self-calibrating A/D converter

intervals the calibration of the system is repeated and new data is stored in the calibration data register. In this way A/D with a linearity of 15 to 16 bits can be obtained.

7.35 Conclusion

In this chapter a review of basic circuits are presented. Systems with resolutions up to 10-bits do not require a calibration system. In monotonic designs resolutions up to 16-bits are possible. The only requirement is that with an increasing input code the output at least increases. This can be obtained by special circuit implementations which have a limited absolute accuracy.
At the moment the full specification for the converter is needed, then callibration or trimming procedures are required. A special system is presented which makes it possible to divide currents with a very high accuracy without needing accurate elements. The method presented uses a combination of a passive divider with a dynamic interchanging method to improve the final accuracy. After removing the error ripple by simply using low-pass filter structures D/A and A/D converters with accuracies from 14 to 18 bits can be designed. The circuits presented show a high accuracy and by op-

timizing the dynamic behaviour of the systems an overall performance is obtained which is close to the theoretically possible behaviour. In practice the *Dynamic Element Matching* system can be extended into generally applicable systems to obtain high-accuracy integer ratios of currents. A second method, which uses a calibration principle of a multiple of equal reference current is very suitable for implementations in a CMOS technology. Self calibration systems make a circuit less sensitive to component variations, however, during warming up of the system a recalibration might be needed. During the calibration cycle the system is not able to produce an output signal. This might be a large drawback for many systems.

Chapter 8

Sample-and-hold amplifiers

8.1 Introduction

A sample-and-hold amplifier is a crucial part of a high-resolution A/D converter system. Overall system performance, such as dynamic range, distortion, and noise, is largely dependent on the sample-and-hold amplifier performance. Monolithic versions of these amplifiers are not widely available. A practical example with a 12-bit performance is described in reference [44]. This design does not have the performance required in a digital audio system. Special optimized versions which can, for example, be used in high-dynamic-range digital audio systems with sufficiently low distortion figures are not widely available on the market. A bipolar version of a sample-and-hold amplifier which meets the high demands of digital audio will be described in this chapter. See for more information reference [4]. The circuit uses high-speed operational amplifiers combined with a specially designed switchable class-B output stage to perform the necessary switching operation. The switch is optimized to have a low track-to-hold step.

8.2 General sample-and-hold amplifier circuit

A general sample-and-hold circuit diagram is shown in Fig. 8.1. The system uses two operational amplifiers (A_1, A_2), two switches (S_1, S_2), a hold capacitor C_H and two feedback resistors R. The "hold" part of the system is formed by amplifier A_2 with the hold capacitor C_H. During "track" mode the resistors R perform an inversion of the input signal and apply the sampled signal across the hold capacitor C_H. Amplifier A_1 decouples the

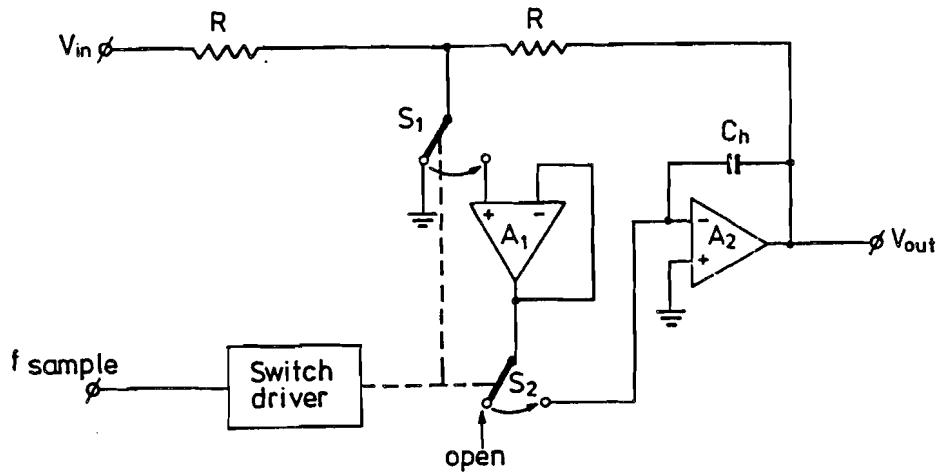

Figure 8.1 : General sample-and-hold amplifier circuit

capacitor C_H from the feedback resistor R thus increasing the bandwidth of the system. This amplifier can also supply a large current to charge or discharge the hold capacitor C_H. In this way a small acquisition time of the system is obtained. Switch S_1 is used to minimize feedthrough of the input signal during hold mode. A low signal feed through is obtained in this way. One disadvantage of this system is that the gain of amplifier A_1 is not used to improve the overall performance of the system. Furthermore the offset voltages of both amplifier are additive, as is the voltage drop across the "on" resistance of the switch S_2. This might result in a larger total offset voltage and a larger distortion of the system. In the system which will be discussed in the following sections some of these drawbacks will be resolved, resulting in a high-performance system.

8.3 Modified sample-and-hold amplifier

The modified sample-and-hold amplifier which uses the gain of amplifier A_1 to reduce offset and distortion is shown in Fig. 8.2. The circuit consists of a wideband operational amplifier A_1 with feedback network R_3, C_2, R_4, and an ultra-low distortion amplifier A_2 with J-FET input devices. Overall gain is determined by the resistors R_1 and R_2. To obtain a high accuracy (for example $\frac{1}{4}$ LSB of 16 bits), the open-loop gain of the cascaded amplifiers is kept flat over the audio band (20 kHz). To come up with a practical circuit solution a second-order roll-off of the total open-loop gain is the only

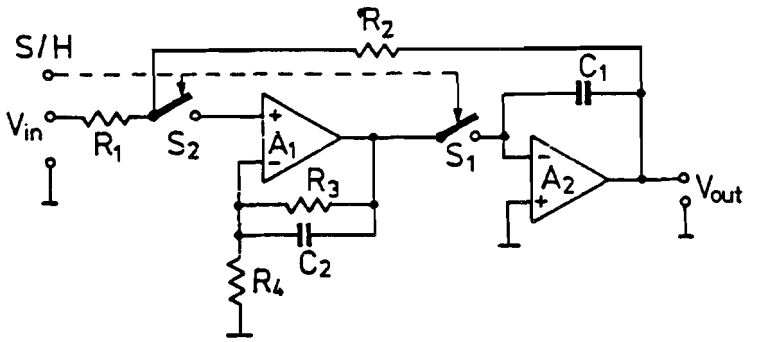

Figure 8.2 : Modified sample-and-hold amplifier

possibility. At the point where the open loop frequency charateristic crosses the feedback characteristic, this roll-off is changed into a first-order roll-off to obtain a stable system. The total open-loop amplitude response as a function of frequency is shown in Fig. 8.3. The gain of amplifier A_1 is set at 250 using the feedback network R_3, C_2, and R_4. The gain of this amplifier is set at 1 in the frequency range from 5 MHz to 70 MHz. The unity gain bandwidth of this amplifier is 70 MHz. Furthermore this amplifier is connected in the non-inverting mode. The open-loop gain of amplifier A_2 is set at 1000 using an internal feedback loop. The unity gain bandwidth of this amplifier is 25 MHz. As a result of this operation a total open-loop gain of about 2.5×10^5, which is flat over the audio band, is obtained.
In the operational amplifiers a special feed-forward frequency compensation technique is used.

8.4 Miller integrator frequency-compensation

When operational amplifiers consist of more than one stage, a frequency compensation mechanism is needed to perform a first-order overall amplitude frequency response. In most cases a so-called "Miller Integrator" compensation technique is used. A basic circuit diagram of this compensation system is shown in Fig. 8.4. The system consists of two amplifier stages. The first stage is a transconductance stage with value gm_1. The second stage is a Miller integrator which converts the output current of the first stage into an output voltage across the compensation capacitor C_2. In standard bipolar processes the input transconductance stage consists of a conglomerate of

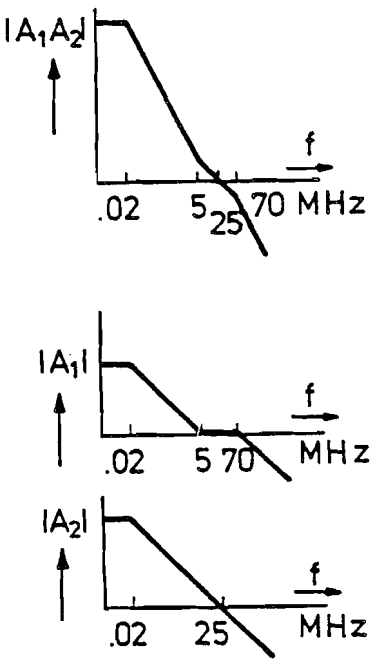

Figure 8.3 : Open-loop amplitude response curves

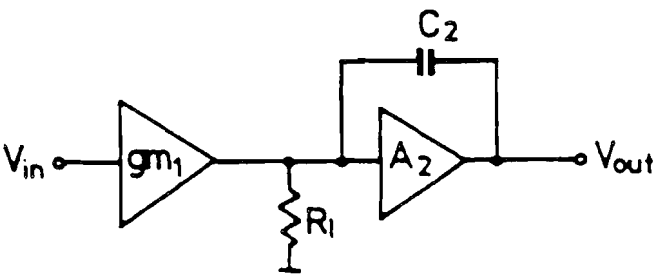

Figure 8.4 : Miller integrator frequency-compensation system

NPN and PNP transistors to combine a dc level shift with the transconductance operation. These PNP transistors are built in a lateral manner and thus have a small transition frequency in comparison with NPN devices. As a result of this construction the overall frequency response of the operational amplifier does not show a first-order amplitude frequency response. The lateral PNP transistors add an extra time constant, which results in the dashed

line shown in Fig. 8.5. In a practical solution using this frequency compen-

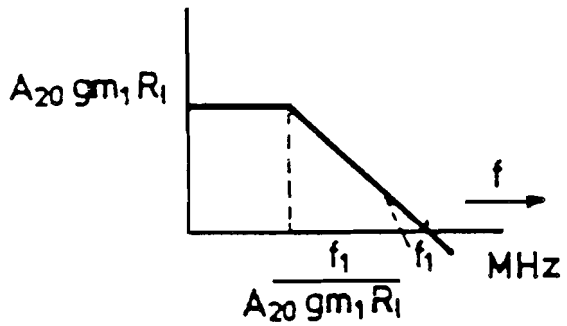

Figure 8.5 : Frequency response of a Miller compensated operational amplifier

sation method a first-order compensated unity gain bandwidth of maximum 5 MHz is possible. However, this bandwidth is not large enough to obtain a building block for a digital audio sample-and-hold amplifier. Therefore a special compensation method will be used as described in the next section.

8.5 Feed-forward wideband frequency-compensation

A block diagram of the basic feed-forward frequency compensation technique is shown in Fig. 8.6. The circuit consists of a voltage amplifier A_1 followed by

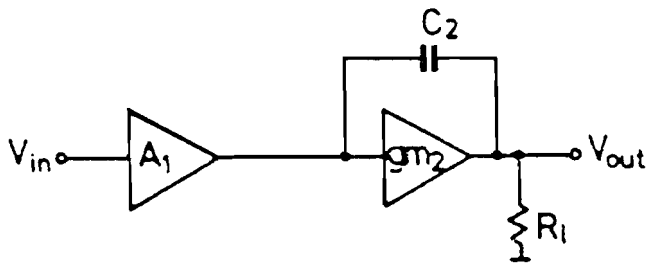

Figure 8.6 : Basic feed-forward frequency compensation technique

a transconductance amplifier with transconductance of gm_2 and loaded with the output impedance consisting of R_L. If no extra measures have been taken the amplitude frequency response of the system shows at high frequencies a second-order roll-off. In stable feedback systems using operational amplifiers

a second-order roll-off is not allowed. To overcome this problem a so-called frequency compensation technique is used which reduces the second-order roll-off at high frequencies to a first-order roll-off. Frequency-compensation techniques result mostly in a much smaller compensated bandwidth than is possible in the basic cascaded two-stage amplifier. The design challenge is to obtain a circuit construction which allows the largest compensated bandwidth possible in a two stage system.
In the circuit shown in Fig. 8.6 frequency compensation is obtained using the capacitor C_2. The operation of this compensation technique can be explained as follows. At low frequencies the influence of the capacitor on the transfer function of the total amplifier can be ignored. A maximum open-loop gain of $A_{openloop} = A_{10} \times gm_2 \times R_L$ is found. Here A_{10} is the dc gain of amplifier A_1. When the signal frequency increases, the capacitor C_2 short-circuits the transconductance stage gm_2 and applies the output signal of amplifier A_1 directly to the output terminal. In this way a first-order amplitude response equal to the high-frequency response of amplifier A_1 is obtained. The unity gain bandwidth depends on the maximum bandwidth of amplifier stage A_1. Note also, that the phase of the output signal of A_1 and the phase of the output signal of the transconductance stage are the same. Due to the low output impedance of A_1, no instability can occur in the transconductance stage gm_2 with the capacitor C_2 as a feedback element.
In Fig. 8.7 the amplitude frequency response with an exact frequency compensation is shown. A simple calculation gives the following equation for

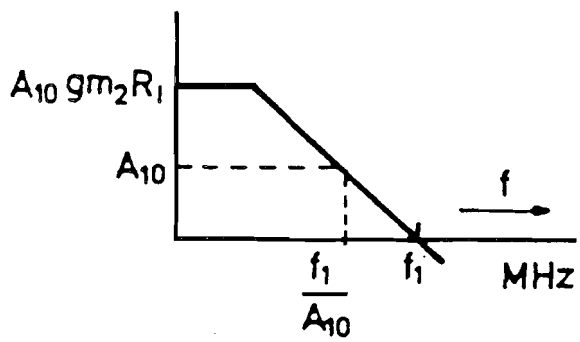

Figure 8.7 : Amplitude frequency response with an exact frequency compensation

the transfer function with $f_1 = \frac{1}{\tau_1}$ where f_1 is the unity gain bandwidth of

amplifier A_1:

$$\frac{V_{out}}{V_{in}} = \frac{A_{10} g_{m2} R_L (1 + pC_2/g_{m2})}{(1 + pA_{10}\tau_1)(1 + pR_L C_2)} \tag{8.1}$$

An exact frequency compensation is obtained when:

$$C_2/g_{m2} = A_{10}\tau_1 \text{ or } C_2 = g_{m2} A_{10} \tau_1. \tag{8.2}$$

Then:

$$\frac{V_{out}}{V_{in}} = \frac{A_{10} g_{m2} R_L}{1 + pR_L C_2} \tag{8.3}$$

In practice, capacitor values ranging from 5 to 15 pF are used and a bandwidth from 10 to 100 MHz with a large phase margin at unity gain can be obtained. This circuit, however, does not give the lowest distortion. The reason for distortion is found in the non-linear capacitance at the output of the transconductance stage. The main part of this capacitance is the collector-substrate capacitance of the transistors used in this amplifier stage. This non-linear capacitance forms along with the capacitor C_2 a non-linear divider at high frequencies resulting in signal distortion. A modification of the basic amplifier structure will be shown in the following section. First a practical example of the simple system will be shown.

8.6 Practical compensated amplifier

A simplified circuit diagram of a practical feed-forward frequency-compensated operational amplifier is shown in Fig. 8.8. In the input stage with transistors T_1 and T_2 a resistive load consisting of resistors R_1 and R_2 is used to obtain a low-noise performance. Emitter followers T_3 and T_4 are further incorporated to obtain the low output impedance needed for frequency compensation. The lateral PNP transistors T_5 and T_6 with the emitter degeneration resistors R_3 and R_5 and an active load consisting of T_7 and T_8 form the transconductance stage.

The capacitor C_1 short-circuiting the transconductance stage at high frequencies gives the necessary frequency compensation. An additional advantage of this method of compensation is the low output noise of the total system at frequencies above the unity gain bandwidth of the amplifier. The emitter follower T_9, which is normally a class-B output amplifier, matches the amplifier output impedance to the externally applied load.

Measurement results of amplitude and phase on a practical integrated amplifier are shown in Fig. 8.9. A phase margin of 45° at unity gain frequency

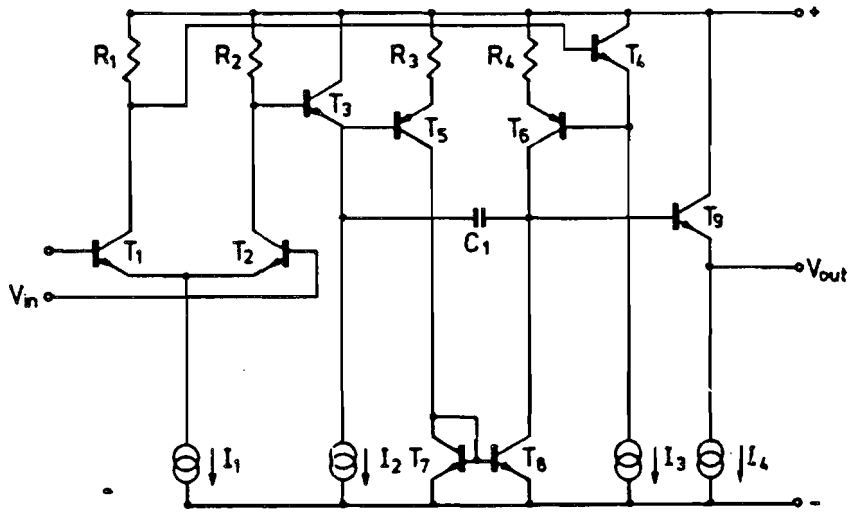

Figure 8.8 : Simplified circuit diagram of a feed-forward frequency-compensated operational amplifier

is found. The bump in the amplitude curve is due to the combination of a low transition frequency of the lateral PNP transistors and the high takeover frequency of the capacitive feed-forward compensation, thus leaving a void in between. This high frequency has been chosen to avoid slow-settling parts in the pulse response of the amplifier due to inaccuracy in the frequency compensation elements. In the final sample-and-hold application which uses this amplifier a negligible effect on the total performance is found.

8.7 Low-distortion frequency-compensation

The block diagram of the low-distortion feed-forward frequency compensation is shown in Fig. 8.10. The system consists of a voltage amplifier A_1 followed by a transconductance stage gm_2 with load resistor R_L and the output voltage amplifier A_3. Frequency compensation is performed using capacitors C_2 and C_3. The operation of the circuit can be explained as follows. At low signal frequencies the influence of the frequency-compensation capacitors C_2 and C_3 on the transfer function of the amplifier can be neglected. The overall dc voltage gain then becomes: $A_{openloop} = A_{10}gm_2R_LA_{30}$. Since the amplifier A_3 with the capacitor C_3 operates as a Miller integrator, the

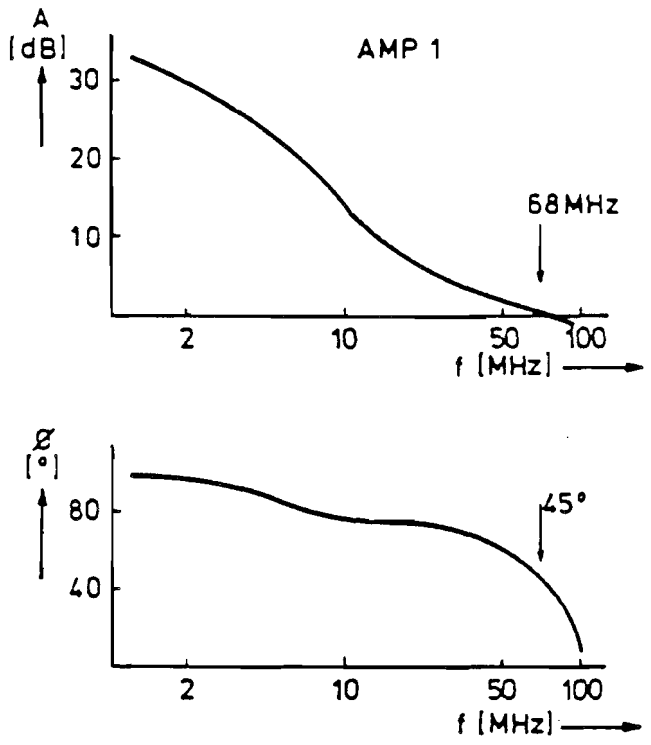

Figure 8.9 : Amplitude and phase measurement results of a practical amplifier

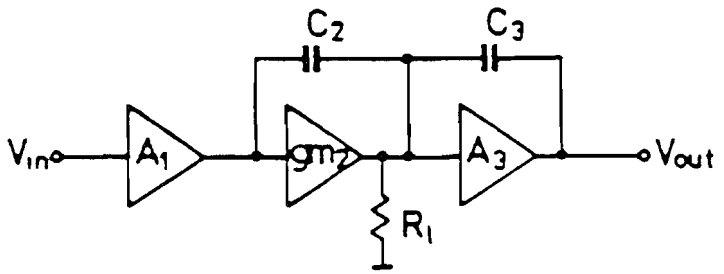

Figure 8.10 : Low-distortion frequency-compensation diagram

output current of the transconductance stage gm_2 is converted into a voltage across C_3. At the same time, however, the capacitor C_2 short-circuits the transconductance stage and forms with C_3 and A_3 an inverter stage with a

gain equal to the ratio between C_2 and C_3. Due to the Miller integrator, a low distortion is obtained because the maximum output voltage swing has to be generated only at the output of A_3. The frequency response of an exactly frequency compensated operational amplifier is shown in Fig. 8.11. The transfer function of the amplifier can be calculated and the result of

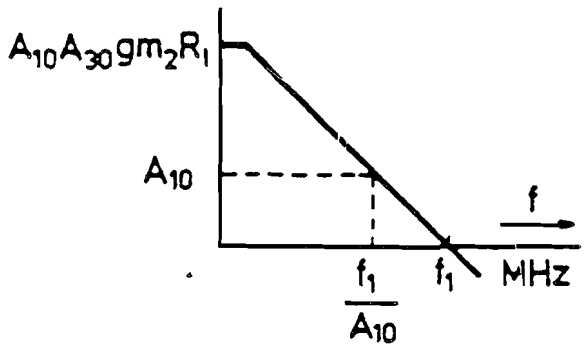

Figure 8.11 : Amplitude frequency response of an exactly compensated amplifier

this calculation is:

$$\frac{V_{out}}{V_{in}} = \frac{A_{10}A_{30}gm_2R_L(1+pC_2/gm_2)}{(1+pA_{10}\tau_1)(1+pR_L(C_2+(1+A_{30})C_3))}. \tag{8.4}$$

An exact frequency compensation is obtained if:

$$A_{10}\tau_1 = C_2/gm_2 \quad or \quad C_2 = A_{10}gm_2\tau_1. \tag{8.5}$$

In that case the transfer function of the operational amplifier becomes:

$$\frac{V_{out}}{V_{in}} = \frac{A_{10}A_{30}gm_2R_L}{1+pR_LC_2(1+(1+A_{30})C_3/C_2)}. \tag{8.6}$$

When the value of the capacitor C_2 is made equal to the value of C_3 then an optimum in overall bandwidth is found.

8.8 Practical low-distortion amplifier

The simplified circuit diagram of a low-distortion feed-forward frequency-compensated operational amplifier is shown in Fig. 8.12. Compared with the circuit diagram of Fig. 8.8, the Miller amplifier stage consisting of transistor T_9 and capacitor C_2 is added. Amplitude and phase measurements of a

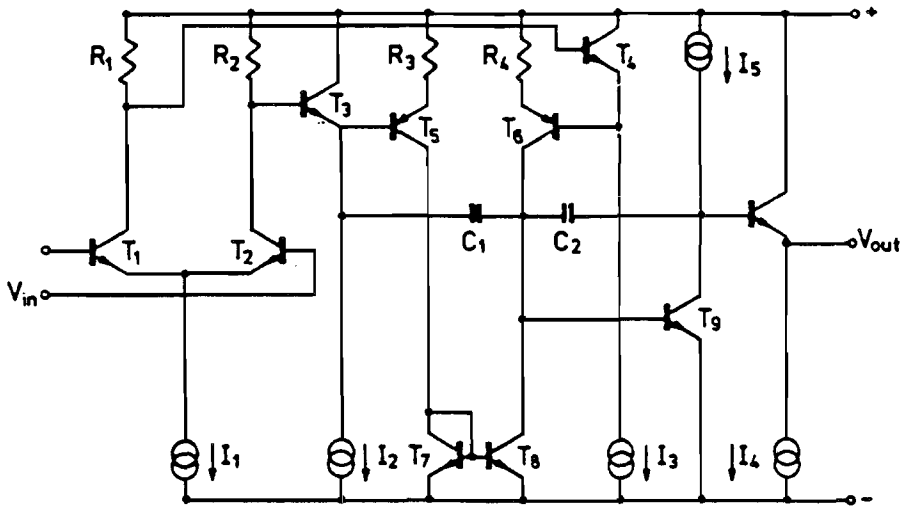

Figure 8.12 : Practical low-distortion operational amplifier circuit

practical integrated amplifier are shown in Fig. 8.13. In this amplifier the phase margin at a unity gain frequency of 27 MHz is 35°. A practically ideal first-order amplitude frequency response is obtained in this circuit.

8.9 Class-B output stage

In wideband operational amplifiers wideband output stages are required. Standard complementary NPN-PNP output stages cannot be used because of the frequency limitations found in the lateral PNP transistors. An all-NPN class-B output stage must be designed to overcome this problem. An example of such a circuit is shown in Fig. 8.14. From Fig. 8.14 it can be seen that transistors T_1 and T_3 are the output devices which deliver the output signal to the external load. Most class-B stages contain a control loop which adjusts the quiescent current and applies the proper signals to the bases of transistors T_1 and T_3. For this purpose, transistors T_2 and T_4, T_5 are added. The bias current flowing through the output transistors is sensed by transistors T_1 and T_2. The sum of the base-emitter voltages of T_1 and T_2 is now compared with the sum of the base-emitter voltages across T_4 and T_5. As a result, the collector current of T_5 is a measure of the bias current flowing through T_1, T_2, and T_3. The collector current of T_5 is compared to

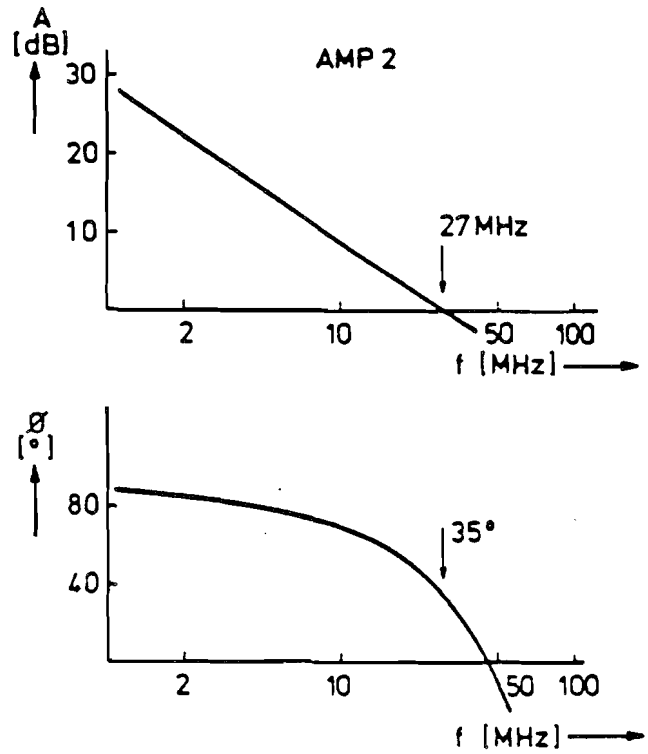

Figure 8.13 : Amplitude and phase measurements of a low-distortion operational amplifier

the reference current I_{ref}, and the lateral PNP transistor T_6 supplies base current to transistor T_3 until a stable operating point is obtained.
The class-B circuit operation is obtained as follows. Suppose an input source is connected to the V_{in} terminal and a load resistor R_L is connected to the output terminal. With a positive-going input signal, T_1 acts as an emitter follower that supplies current to the load resistor. The increase in collector current corresponds to an increase in the base-emitter voltage of transistor T_1. Using the control condition, which was needed to obtain a stable bias current stabilization:

$$V_{be1} + V_{be2} = V_{be4} + V_{be5}, \tag{8.7}$$

it can be shown that the increase of V_{be1}, results in an increase of V_{be4} and V_{be5}, thus giving an increase in the collector currents of T_4 and T_5. More current is subtracted from the reference current I_{ref}, causing a decrease in

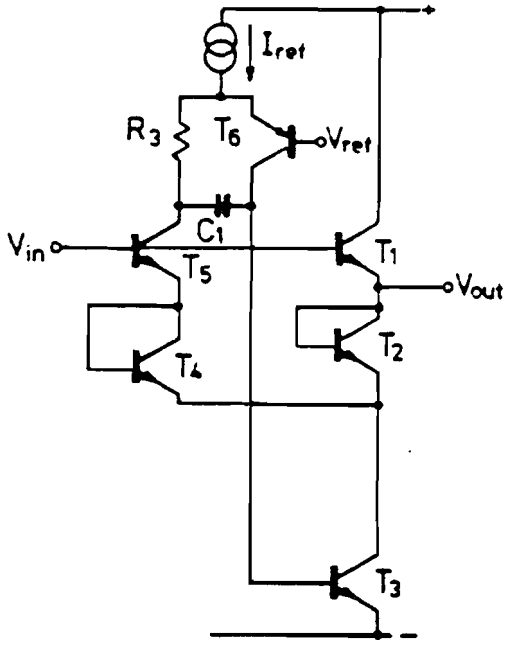

Figure 8.14 : All NPN class-B output stage

the collector currents of T_6 and T_3.
When a negative-going input signal is applied, the collector current of T_1 decreases. At the same time, the collector current of T_5 decreases and more current is applied to T_6. As a result the base current of T_3 increases resulting in an increase in the collector current of this transistor. The output signal is brought down by transistor T_3 to the negative supply voltage.
At high frequencies the frequency response of the PNP transistor is eliminated by a feed-forward coupling using R_3 and C_1. A bandwidth up to 100 MHz is obtained with this output stage. It can be designed to supply output currents with a maximum value of 100 mA.

8.10 Switchable class-B output stage

A class-B output stage which can be switched on and off is shown in Fig. 8.15. To obtain a switching operation in the class-B output stage a differential amplifier stage consisting of transistor T_7 and T_8 and the resistors R_1 and R_2 are added to the circuit diagram of Fig. 8.14. The operation of the

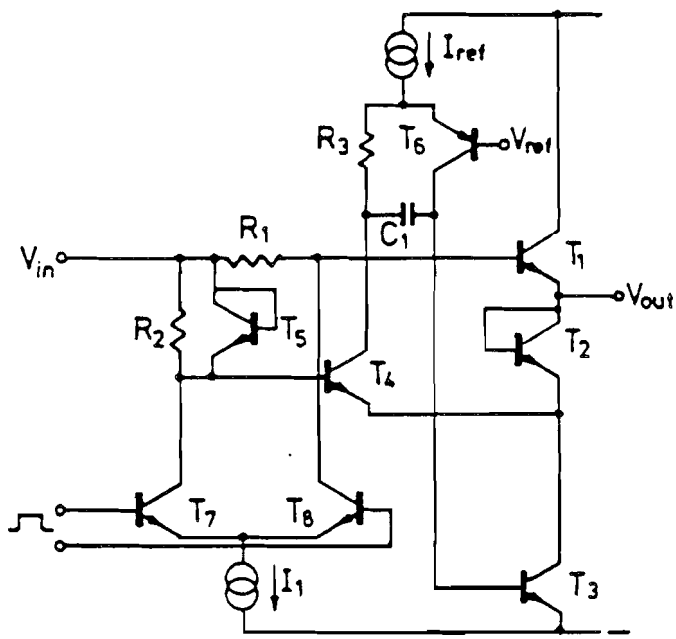

Figure 8.15 : Switchable class-B output stage

circuit can be explained as follows. When transistor T_7 is switched on and the voltage drop across R_1 is zero, then the normal operation of the class-B stage as explained in connection with Fig. 8.14 is obtained. The circuit is switched into the off-mode when transistor T_8 is conducting. Across resistor R_1 a voltage drop equal to a diode voltage is generated. The resistor R_2 reduces the voltage drop across transistor T_5 to zero. In this way, the base-emitter voltages of transistors T_1 and T_2 are made zero and no conductance is possible. The transistor loop consisting of T_3, T_4, and T_6, however, remains active irrespective of the switching condition. The leakage current of the switch can be made very low, while capacitive feedthrough is compensated by equal voltage swings across the base-emitter junctions of transistors T_1 and T_2. The voltage compliance of this switch, however, is small. The reverse biasing of the switching transistors equals about one diode voltage. Therefore only a voltage compliance between 200 mV and 500 mV is allowed at the output of the switch. To overcome this problem the switch is operated at, for example, an inverting input of an operational amplifier. It is known that at these input points a small voltage variation, well below the required

range by the switch, is found. With special circuit configurations, however, it is possible to operate this switch in a non-inverting sample-and-hold mode.

8.11 Complete sample-and-hold amplifier

The complete sample-and-hold amplifier is incorporated on a 1.5x2.5 mm^2 chip using a standard bipolar technology with double-layer interconnect. In this chip all capacitors used in the circuit consist of the capacitance between the two interconnect metal layers. A very linear capacitance-voltage characteristic is obtained in this way. Because of this construction these capacitors require a large part of the chip area. With a special process option using thin oxide/nitride layers a much larger capacitance per unit area can be obtained. In such a process the size of the compensation capacitors can be reduced and the "Hold" capacitor can also be put on the chip.

8.12 Measurements

The result of a signal-to-noise measurement as a function of amplitude is shown in Fig. 8.16. The acquisition time of the circuit is performed by using a full-scale input signal of 19 kHz. The sampling frequency is kept constant, while the hold time is varied in this measurement. The measurement results are shown in Fig. 8.17. A photograph of the hold-track-hold operation of the circuit is shown in Fig. 8.18. The input frequency is taken at one quarter of the sampling frequency to obtain a stable picture. In Table I the measurement results of the total system are shown. A die photograph is shown in Fig. 8.20.

8.13 Conclusion

Using special feed-forward frequency compensation techniques for multi-stage operational amplifiers and an all-NPN switchable class-B output stage, a high-performance sample-and-hold amplifier can be designed for 16-bit digital audio systems. A further advantage of the frequency compensation method used is the low output noise of the compensated amplifiers for frequencies above the unity gain bandwidth of the amplifiers. The application of resistive loads in the input stages in comparison with active loads using current mirrors improves the low noise specification of the system. The system can be designed in a so-called bipolar-fet process. The fet devices

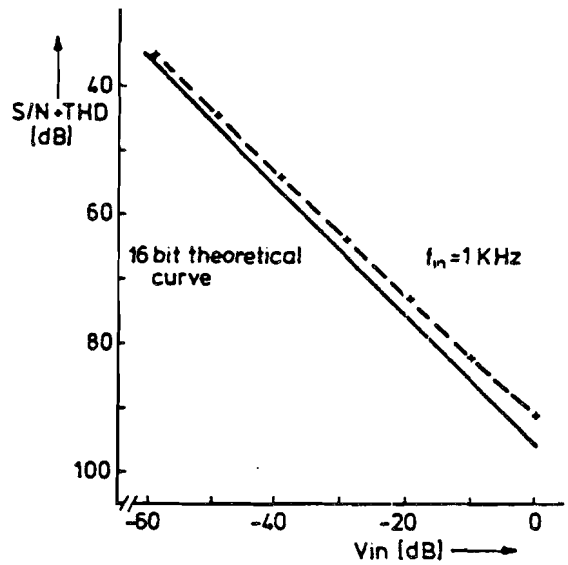

Figure 8.16 : Signal-to-noise measurement as a function of signal amplitude

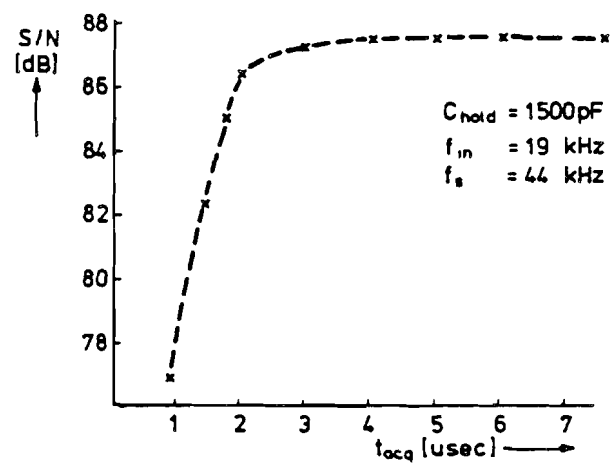

Figure 8.17 : Acquisition time measurement result

are used in the hold amplifier to obtain a low input bias current. Today, however, bi-MOS technologies, which combine bipolar devices with MOS devices can be used advantageously in a sample-and-hold amplifier. The

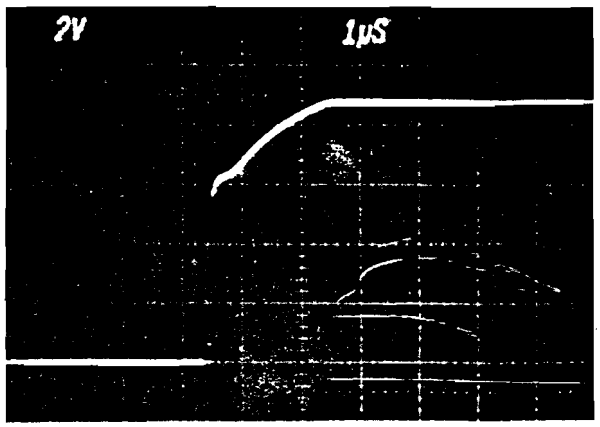

Figure 8.18 : Hold-track-hold operation with an input signal of one quarter of the sample frequency

Acquisition time	1.5 µsec to 0.001 %
Aperture uncertainty	< 0.5 nsec
Small signal bandw	8 MHz
Slew rate	100 V/µsec
Gain	-1 V/V
Distortion	< 0.001 %
S/N ratio	> 90 dB
Hold offset	< 2 mV
Droop rate	5 µV/µsec
Digital input	T.T.L. compatible
Power supply	± 5V to ± 9 V 27mA
Chip size	1.5 * 2.5 mm^2

Figure 8.19 : Sample-and-hold amplifier measurement data

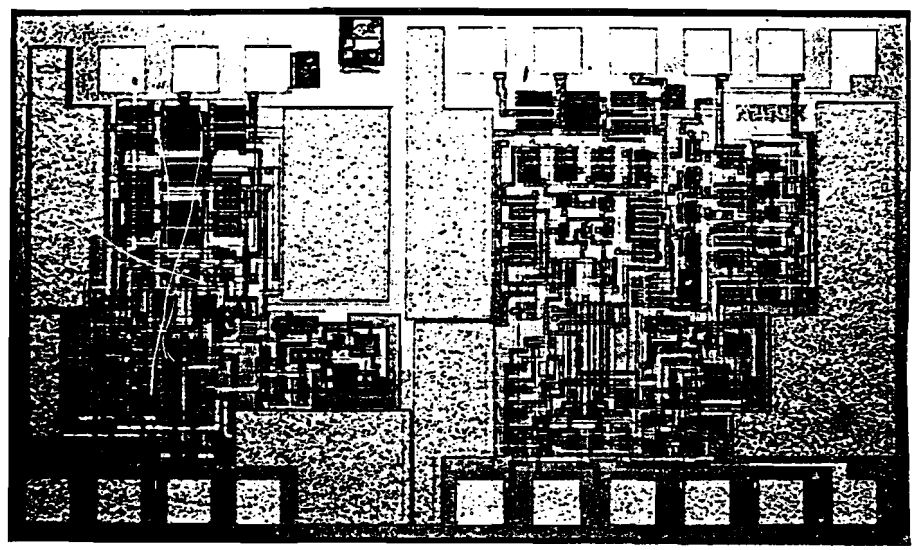

Figure 8.20 : Die photograph of sample-and-hold amplifier

relatively large gain in the first amplifier stage reduces the inherently large low-frequency noise of the MOS devices with respect to the input terminal of the sample-and-hold amplifier. Furthermore, the lateral PNP transistors which are used in the level shift can be replaced by p-MOS devices, which show a better frequency characteristic than these devices.

Chapter 9

Voltage and current reference sources

9.1 Introduction

In A/D and D/A converters the full-scale value is determined by the reference source. A lownoise and low temperature coefficient of the output signal of the reference source is very important for high-resolution, high-accuracy converters. A well-known device for stabilizing a reference voltage is a zener diode. In integrated circuits, however, the zener diode can cause problems with the reliability of the circuit. In modern technologies it is not always possible to reverse-bias the emitter-base junction of a transistor to obtain a zener diode operation. The yield of circuits is reduced by reverse-biasing transistors. Today's reference sources are built using the bandgap voltage of silicon as a low-temperature dependent reference voltage. In this chapter different circuits will be described which use the bandgap principle to stabilize a voltage or a current. Examples of bandgap reference voltages are given in references [45,46,47].

9.2 Basic bandgap reference voltage source

The basic bandgap voltage stabilizer is shown in Fig. 9.1. It consists of a current source with a well-determined temperature relation, a resistor R and a transistor which is switched as a diode. The output voltage of the system is generated across the resistor R and the transistor T_1. The temperature

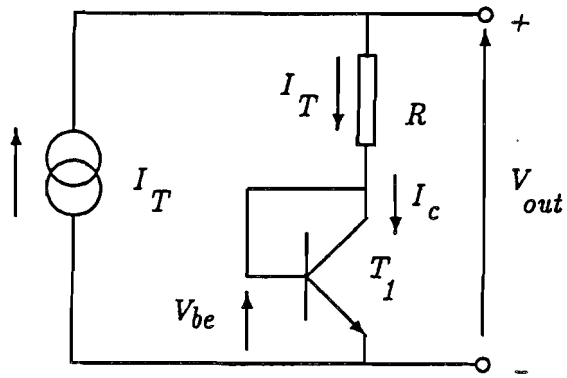

Figure 9.1 : Basic bandgap voltage reference source

dependence of the current source I_T is given by:

$$\frac{1}{I_T}\frac{dI_T}{dT} = \frac{1}{T}. \tag{9.1}$$

The output voltage of the system which is made nearly temperature independent is given by:

$$V_{out} = R \times I_T + V_{be}. \tag{9.2}$$

In the following simplified analysis we suppose that the base current of the transistor can be ignored with respect to the collector current. This simplification does not change the results considerably and makes it much easier to understand the operation of the system. The basic idea behind the bandgap voltage stabilization is the following: With increasing temperature it is known that the base-emitter voltage of a transistor decreases with increasing temperature. At the same time, the positive temperature coefficient of the current source I_T generates a voltage across resistor R which increases linearly with temperature. The output voltage of the circuit can be adjusted to a value which is nearly equal to the bandgap voltage of silicon. The decrease in base-emitter voltage in that case is compensated by the increase in the voltage across the resistor R.
It is known that for a bipolar transistor the following equation is valid for the relation between collector current and base-emitter voltage:

$$I_c = I_0(\exp^{\frac{q}{kT}V_{be}} - 1). \tag{9.3}$$

I_0 is the base-emitter reverse current. The temperature relation for I_0 can be expressed in the following parameters:

$$I_0 = CT^n \times \exp^{-\frac{qV_g}{kT}}. \tag{9.4}$$

In equation 9.4 the value of V_g is given by the bandgap voltage of silicon which is equal to 1.208 V. In silicon n is approximately 1.4 and C is a constant depending on the size of the device.
If we assume that $\exp^{\frac{q}{kT}V_{be}} \gg 1$, then we can approximate equation 9.3 and equation 9.4 by:

$$I_c = CT^n \exp^{\frac{q}{kT}(V_{be}-V_g)}. \tag{9.5}$$

After differentiation of equation 9.5 with respect to temperature we obtain:

$$\begin{aligned} dI_c = CnT^{n-1} \exp^{\frac{q}{kT}(V_{be}-V_g)} dT - \\ CT^n \exp^{\frac{q}{kT}(V_{be}-V_g)} \frac{q(V_{be}-V_g)}{kT}\frac{dT}{T} + \\ CT^n \frac{q}{kT} \exp^{\frac{q}{kT}(V_{be}-V_g)} dV_{be}. \end{aligned} \tag{9.6}$$

This equation can be simplified using the expression given in equation 9.5 We obtain after the insertion:

$$dI_c = \frac{n}{T} I_c dT - \frac{q}{kT} I_c \frac{V_{be}-V_g}{T} dT + \frac{q}{kT} I_c dV_{be}. \tag{9.7}$$

With a negligible base current of the transistor the collector current variation now equals the variation of the current source I_T. Inserting equation 9.1 into equation 9.7 we end up with the following relation for the temperature dependence of the base-emitter voltage of the transistor:

$$\frac{dV_{be}}{dT} = \frac{k}{q}(1-n) + \frac{V_{be}-V_g}{T}. \tag{9.8}$$

The temperature relation of the output voltage V_{out} can be expressed in the following terms supposing that R is temperature-independent:

$$\frac{dV_{out}}{dT} = R\frac{dI_T}{dT} + \frac{dV_{be}}{dT}. \tag{9.9}$$

Inserting equation 9.1 and equation 9.8 into equation 9.9 results in, after rearrangement of the terms:

$$\frac{dV_{out}}{dT} = \frac{I_T \times R}{T} + \frac{k}{q}(1-n) + \frac{V_{be}-V_g}{T}. \tag{9.10}$$

The output voltage of the reference source can be adjusted in such a way that at $T = T_0$ the temperature coefficient of the reference source $\frac{dV_{out}}{dT} = 0$. The following value for the output voltage at $T = T_0$ is obtained:

$$V_{out}(atT = T_0) = V_{beT_0} + I_{T0}R = V_g - \frac{kT_0}{q}(1 - n). \tag{9.11}$$

The remarkable point is now obtained that at $T = T_0$ the temperature coefficient of the output voltage is zero. The temperature dependence of the output voltage can be calculated. By substituting equation 9.11 into equation 9.10, the following result is obtained:

$$\frac{dV_{out}}{dT} = \frac{k}{q}(1 - n)(1 - \frac{T}{T_0}). \tag{9.12}$$

This equation shows that there is a change in sign of the temperature coefficient of the output voltage around $T = T_0$.
After integration of equation 9.12 we obtain an expression for the output voltage of the bandgap reference source as a function of temperature T. The integration and substitution of the boundary conditions result in:

$$V_{out}(T) = V_g - \frac{k}{q}T(1 - n)(1 - \ln\frac{T}{T_0}). \tag{9.13}$$

The expression given in equation 9.13 represents a parabolic temperature dependence around $T = T_0$. The temperature dependence of the reference source as expressed by equation 9.13 is calculated and the result is shown in Fig. 9.2.

9.3 All-NPN bandgap voltage reference source

In Fig. 9.3 a practical example of a voltage reference source which uses only NPN transistors is shown. The circuit consists of a cross-coupled quad transistor unit T_1, T_2, T_3, and T_4 and the current-converting resistor R_1. Transistor T_1 has a p times larger emitter area than the other three transistors in the quad. Via Resistor R_2 a current from the supply source is applied to the circuit. Resistor R_3 is added to obtain an adjustable output voltage. Transistor T_7 acts as a buffer device and results in a smaller current variation through resistor R_2 with supply voltage variations (V_{cc}). Transistors T_6 and T_5 are added to obtain a compensation for supply voltage dependence of the output voltage V_{out}. The operation of the system will be explained

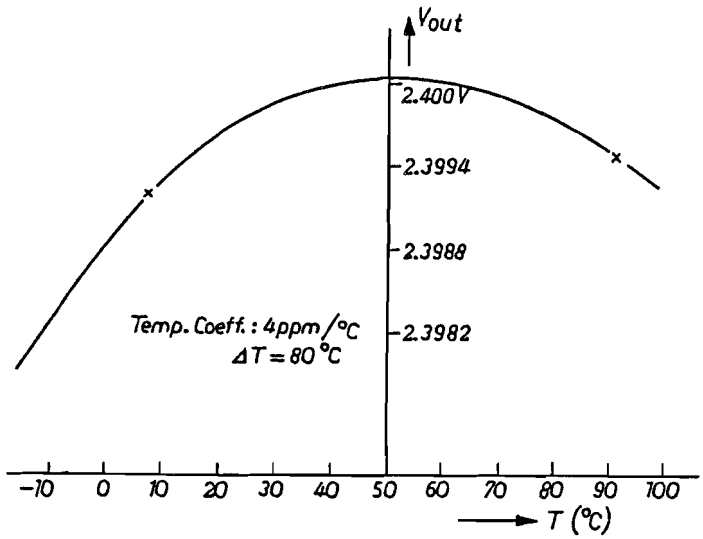

Figure 9.2 : Temperature dependence of a bandgap reference source

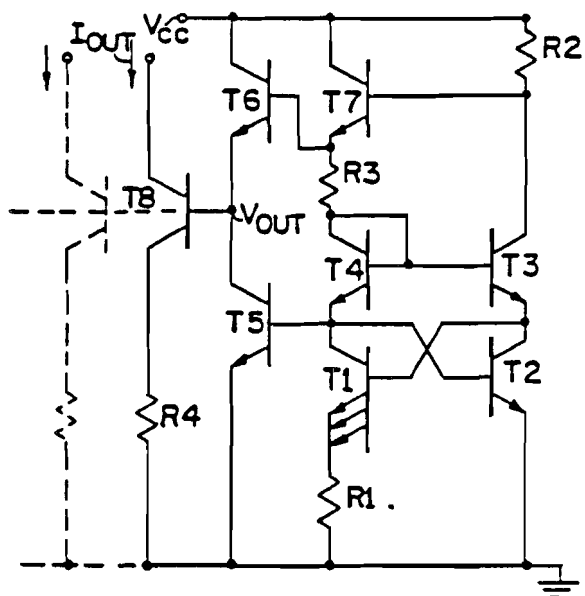

Figure 9.3 : All-NPN bandgap voltage reference source

as follows. The current flowing through transistors T_4, T_1 and R_1 can be

expressed in the following parameter of the quad unit:

$$I_{R1} = \frac{kT}{qR_1}\ln(p). \tag{9.14}$$

Equation 9.14 shows that basically the current is supply-voltage-independent, however, the output voltage at the collector of T_4 shows a variation which contains a supply voltage dependence. This can be explained by the fact that the output voltage at the collector of T_4 equals $V_{be4} + V_{be2}$. The current through transistor T_4 is well stabilized at a value given by equation 9.14 so the base-emitter voltage of this transistor is independent of the supply voltage variation. The current through transistor T_2, however, varies with the supply voltage. Therefore the base-emitter voltage of this transistor shows a supply-voltage-dependent part. To the output voltage at the collector of T_4 a value equal to:

$$V_{R3} = \frac{R_3}{R_1}\frac{kT}{q}\ln(p) \tag{9.15}$$

is added. As can be seen from equations 9.14 and 9.15, the temperature dependence of the current I_{R1} is linear with T and thus the voltage drop across R_3 increases linearly with increasing temperature.
Now transistors T_5 and T_6 are added. Transistor T_5 is connected in parallel with transistor T_2 and forms a current mirror. As a result, the current through T_5 varies exactly in the same way as the current through transistor T_2. This current flows through transistor T_6 too, and therefore the voltage variation of the base-emitter voltage of T_6 is identical to the base-emitter voltage variation of transistor T_2. The voltage variation across transistor T_6 is subtracted from the voltage developed across T_2 and T_4. Therefore the voltage variation at the emitter of transistor T_6 is zero. At the output terminal marked V_{out}, a voltage equal to the base-emitter voltage of T_4 plus the voltage drop across resistor R_3 is obtained. When this output voltage is adjusted to the value given in equation 9.11 a temperature dependence equal to a bandgap voltage source is obtained. This circuit does not contain PNP transistors and is therefore very suitable for use in integrated circuits which use special high-frequency processes. (See [48]). In these processes mostly lateral PNP transistors with poor dc and high-frequency performance are available. The temperature dependence of the resistors R_1 and R_3 is cancelled provided that the temperature coefficients of the resistors R_1 and R_3 are equal and have a good thermal tracking.

9.4 Bandgap reference current sources

A simplified circuit diagram of a reference current source is shown in Fig. 9.4. It consists of transistors T_1, T_2, with the voltage-to-current converting

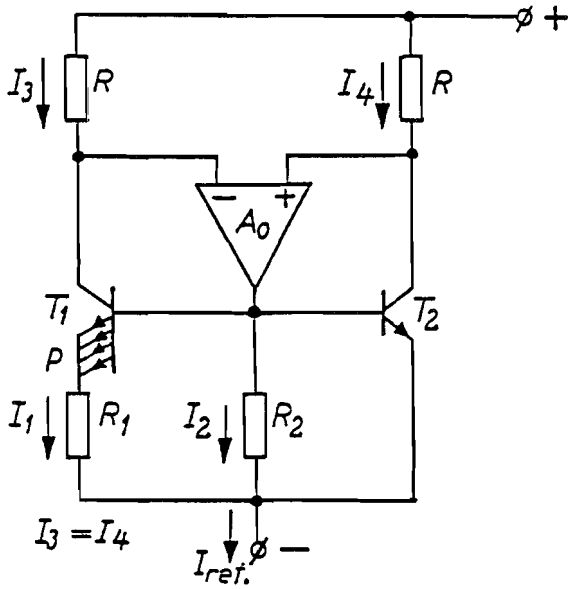

Figure 9.4 : Basic reference current source

resistor R_1. An operational amplifier A_0 with the resistors R controls the current in transistors T_1 and T_2 in such away that equal currents will flow through these transistors. The resistor R_2 is added for temperature compensation and gives an identical temperature dependence, as is the case with the bandgap reference voltage source. This will be explained later on.
Transistor T_1 has a p times larger emitter area than transistor T_2. With equal collector currents flowing in T_1 and T_2, the following expression for the current flowing through R_1 is found:

$$I_{R1} = \frac{kT}{qR} \ln(p). \tag{9.16}$$

As can be seen from equation 9.16, the currents through T_1 and T_2 are linearly dependent on the temperature T.
Now resistor R_2 is added to the circuit. The current through R_2 then becomes:

$$I_{R2} = \frac{V_{be2}}{R_2}. \tag{9.17}$$

With increasing temperature it is known that the base emitter voltage of a transistor decreases. As a result, the current through resistor R_2 will decrease. As already stated before, the currents through T_1 and T_2 will increase with increasing temperature. The resistor value of R_2 can be chosen in such a way that the increase in current flowing through T_1 and T_2 is cancelled, by the decrease in the current flowing through R_2. In this way a temperature independent current source is obtained. Furthermore, the operational amplifier A_0 can be constructed in such a way that it uses only currents which flow through R_2, T_1 and T_2.
The value for which an exact compensation of the temperature coefficients of the currents occur can be calculated. The result of this calculation, which is identical to the calculation given in the basic bandgap voltage reference source, is shown. We obtain:

$$R_2 = (V_g + \frac{kT_0}{q}(n-1))/I_{ref}. \tag{9.18}$$

Moreover, the generated current reference I_{ref} shows the same temperature dependence as the bandgap reference voltage. The output current of this reference source becomes:

$$I_{out} = \frac{V_g}{R_2} + \frac{k}{q}T(n-1)\frac{1}{R_2}(1 - \ln\frac{T}{T_0}). \tag{9.19}$$

9.5 Practical reference current source

In Fig. 9.5 an example of a practical implementation of a reference current source is shown. In this system the operational amplifier is replaced by a differential pair, T_3, and, T_4 with a PNP current mirror consisting of T_5, T_6, and T_7. A Darlington stage, T_8 and T_9, controls the current through the resistors R. An additional resistor R_3 is added to the circuit to obtain a "starting condition" under all circumstances. The resistor R_3 supplies current into the circuit and in this way prevents "zero current" from being a solution to the equations too. The zero solution is not a desired solution. R_C is an extra temperature-compensation resistor which is process-dependent and can give an extra second-order temperature compensation. The advantage of this type of current source is that the current which flows through the "bottom" is the same as the current which flows in the "top" of the circuit. Therefore, this current source can be included in the reference loop of an A/D or D/A converter, to generate at one side the most significant bit current, while at

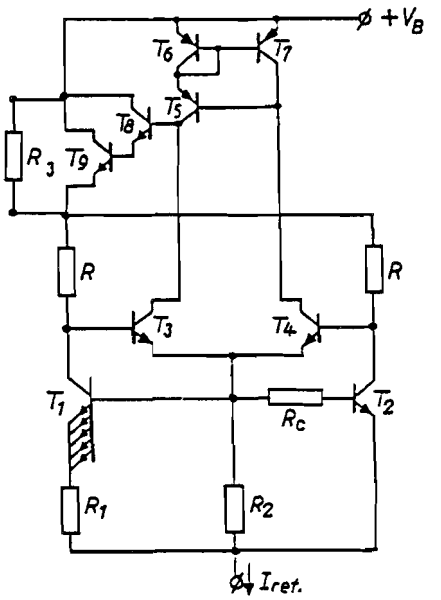

Figure 9.5 : Practical reference current source

the other side this current can be divided in the binary division stage to obtain a binary-weighted current network.

9.6 Second-order temperature compensation

Up till now all described reference sources show a parabolic temperature dependence. In high-accuracy converters this temperature dependence is too great to keep the absolute accuracy within the size of the least significant bit. An additional temperature compensation is therefore needed to overcome this problem. In Fig.9.6 an example of a reference current source with a second-order temperature compensation is shown. The main stabilizer core consists of transistors T_1 and T_2 which have a p times larger emitter area than transistors T_3 and T_4. Resistor R_1 is used to convert the base-emitter voltage difference into a current. The operational amplifier OA with the resistors R forces equal currents to flow through transistors T_1, T_2, T_3, T_4 and the resistor R_1. The resistors R_2, R_3 and transistor T_5 are added to obtain the bandgap current stabilizer with second-order temperature compensation. The output current I_{out} in the bottom part of the circuit is identical to the current which flows in the top part of the circuit. The relation between the

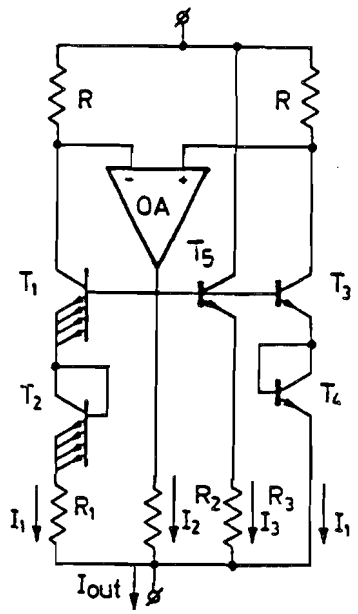

Figure 9.6 : Current reference source with second-order temperature compensation

circuit parameters and the temperature dependence of the reference current source will be calculated. The following equations will be used:

$$I_{out} = 2I_1 + I_2 + I_3 \tag{9.20}$$

$$I_1 R_1 = 2\frac{k}{q} T \ln p \tag{9.21}$$

$$I_2 R_2 = 2\frac{k}{q} T \ln \frac{I_1}{I_0} \tag{9.22}$$

$$I_3 R_3 = 2\frac{k}{q} T \ln \frac{I_1}{I_0} - \frac{k}{q} T \ln \frac{I_3}{I_0}. \tag{9.23}$$

During the calculation we suppose that all transistors are equal, i.e. all emitter-base reverse currents i_0 are equal. Furthermore equations 9.3 and 9.4 will be used to calculate the temperature dependence of the current source.

To obtain analytical expressions for the values of resistors R_1, R_2, and R_3 we have to solve the equations with the requirement that at $T = T_0$, $\frac{dI_{out}}{dT}$ = 0. After differentiation and substitution we obtain:

$$\frac{dI_{out}}{dT} = \frac{I_{out}}{T} - \frac{V_g}{T}\left(\frac{2}{R_2} + \frac{1}{R_3}\right) -$$

$$\frac{k}{q}(n-1)(\frac{2}{R_2}-\frac{1}{R_3}\frac{V_g-I_3R_3(n-1)}{(\frac{k}{q}T+I_3R_3)(n-1)}). \tag{9.24}$$

In this equation a linear temperature relation is shown in the first part, while in the second part a non-linear temperature dependence is shown. This non-linear temperature relation introduces the already shown parabolic temperature dependence of the output current. However, in working through the equations a relation between the resistors R_2 and R_3 is found which can be adjusted in such a way that the parabolic temperature relation is cancelled out. When at $T = T_0$ the non-linear term is made zero we obtain for the ratio between R_2 and R_3:

$$\frac{R_2}{R_3}=\frac{2(n-1)(I_{30}R_3+\frac{k}{q}T_0}{V_g-I_{30}R_3(n-1)}). \tag{9.25}$$

I_{30} is the current value of I_3 at $T = T_0$. At the same time the output current of the circuit at $T + T_0$ can be found from the following equation:

$$I_{out}=V_g(\frac{2}{R_2}+\frac{1}{R_3}). \tag{9.26}$$

This result show a basically "ideal" bandgap reference source. The voltage drop across resistor R_3 which is equal to I_3R_3 is close to the value of a base-emitter voltage of a transistor. This value is much larger than $\frac{k}{q}T$. Therefore equation 9.25 can be approximated by:

$$\frac{R_2}{R_3}\cong\frac{2}{\frac{V_g}{(n-1)I_{30}R_3}-1}. \tag{9.27}$$

This ratio between R_2 and R_3 is obtained at the temperature $T = T_0$. The output current of the total system can be obtained by integrating equation 9.24. This not possible without applying some simplifications. Therefore we suppose that for temperatures which do not differ too much from $T = T_0$ the non-linear term

$$\frac{k}{q}(n-1)(\frac{2}{R_2}-\frac{1}{R_3}\frac{V_g-I_3R_3(n-1)}{(\frac{k}{q}T+I_3R_3)(n-1)}) \tag{9.28}$$

is a constant.
The output current then becomes:

$$I_{out}=V_g(\frac{2}{R_2}+\frac{1}{R_3})+\frac{k}{q}(n-1)\times$$

$$(\frac{2}{R_2} - \frac{1}{R_3}\frac{V_g - I_{30}R_3(n-1)}{(\frac{k}{q}T_0 + I_{30}R_3)(n-1)}) \times (1 - \ln\frac{T}{T_0}). \quad (9.29)$$

When the value of the resistor R_3 is made infinite, a well-known circuit configuration as shown in Fig. 9.3 is obtained. The output current in the case of $R_3 \rightarrow \infty$ becomes:

$$I_{out} = V_g\frac{2}{R_2} + \frac{k}{q}T(n-1)\frac{2}{R_2}(1 - \ln\frac{T}{T_0}). \quad (9.30)$$

Because two base-emitter voltages are connected in series, a factor 2 in output current value with respect to the value predicted by equation 9.19 is obtained.
A second important limit is obtained at the moment the value of the resistor $R_2 \rightarrow \infty$. In that case a parabolic temperature which is opposite with respect to the curve shown in Fig. 9.2 is obtained. The output current in this case becomes:

$$I_{out} = V_g\frac{1}{R_3} - \frac{k}{q}T(n-1)\frac{1}{R_3}(1 - \ln\frac{T}{T_0}). \quad (9.31)$$

When at $T = T_0$ the ratio between R_2 and R_3 is chosen as given by equation 9.27, then an exact relation for the output current is not available. The estimate shows that the cancellation of the parabolic temperature relation must occur. A computer analysis of the basic equation gives the best results.

9.7 Reference current source measurements

A practical current source as shown in Fig. 9.5 is integrated in an A/D converter chip. Measurements have been performed to verify the formulas given above. The very low temperature dependence of this reference source makes it difficult to obtain accurate measurement results because the stability of this source is in the same order as the stability of the reference sources used in digital voltmeters. In Fig. 9.6 the measurement results with an optimum resistor setting and the two extremes are shown. It is clear that the above equations predict the temperature dependence of the reference source rather well. A detailed measurement result, which shows the optimum compensation situation of the reference source is shown in Fig. 9.8. . The result

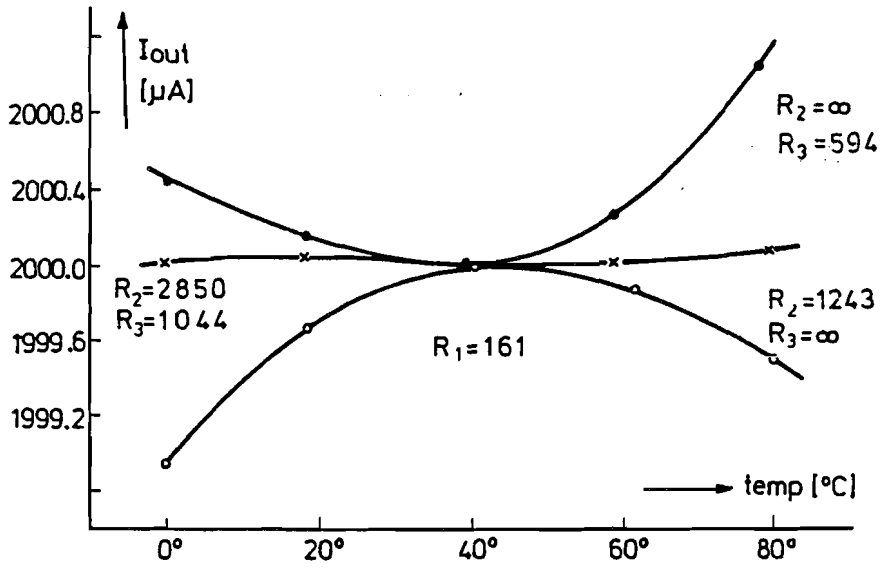

Figure 9.7 : Measurement results of a reference current source

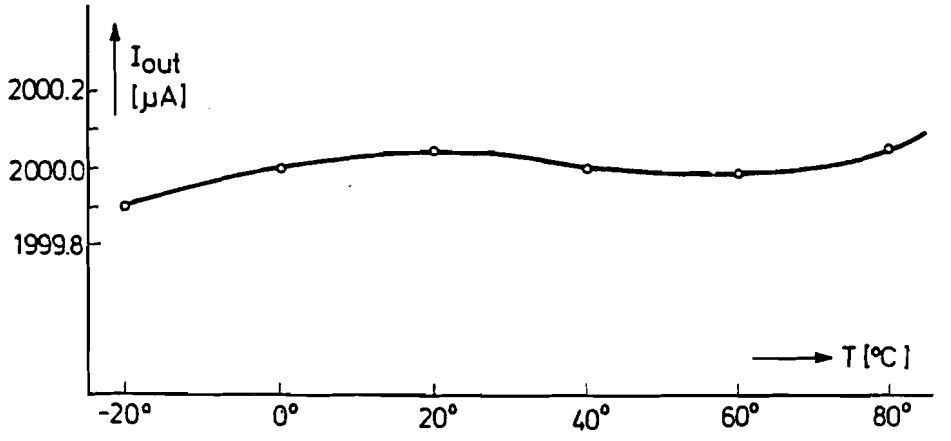

Figure 9.8 : Detailed measurement result of the reference current source

shown in Fig. 9.8 indicates that over a temperature change from -20° to + 85° C, a maximum change of ±50 ppm is attainable. Hysteresis effects over a temperature cycle are very small, < 10 ppm. A temperature coefficient of ±0.5 ppm/°C is obtained over the given temperature range. The output current of the reference source is 2 mA.

9.8 Noise of a bandgap reference current source

When reference current sources are applied in A/D converters, it is very important to know more about the noise behaviour of this source. The bandwidth of comparators is much higher than the analog bandwidth which must be converted. Therefore, in high-resolution A/D converters the reference source might limit the maximum resolution of the converter. To obtain an impression of the maximum resolution which can be obtained the current noise of the reference source shown in Fig. 9.4 is determined by computer simulation. When the value of the output current equals 1 mA, then the output current noise density with transistor sizes for which the internal base resistance $R_{bb} \ll \frac{1}{gm}$ tends to reach $I_{noise} = 30pA$. Supposing that the 1 mA output current is the value of the most significant bit of the converter, then an rms value for a sine wave which fits the full-scale value of the converter equals .7 mA. The signal-to-noise ratio of the current source can be calculated. We obtain:

$$S/N = 20 \times \log \frac{I_{signal}}{I_{noise}}. \tag{9.32}$$

Inserting the values given above results in: S/N = 147 dB root Herz. Over a bandwidth of 20 kHz a value of 104 dB is found.
The same calculation is performed for a current source built up according to Fig. 9.6. The output current is adjusted to 1 mA. In this case the noise current equals 23 pA. Signal-to-noise is calculated in the same way. The result becomes: S/N = 150 dB root Herz, giving over a bandwidth of 20 kHz a value of 107 dB.
The doubling of the voltage drop across resistor R_1 improves the noise performance of the reference current source by 3 dB. A further decrease in noise could be obtaine by increasing the voltage drop across resistor R_1. Such a configuration, however, leads to an impractical circuit solution because of the cascoding of a large amount of transistors requiring a large supply voltage.
From the noise analysis it is found that most noise contributions come from: resistor R_1, transistor T_2 and transistor T_1. Further noise additions are small and can be ignored. It must be noted furthermore that the equivalent input voltage noise of a transistor is:

$$e^2_{rms} = 4kT(R_{bb} + \frac{1}{2gm})\Delta f. \tag{9.33}$$

As a result an increase of the reference current by a factor two results in a decrease in noise current by $\sqrt{2}$ or 3 dB. The base resistors of the transistors must be small with respect to $\frac{1}{gm}$ to validate this statement. The signal-to-noise ratio of the system of Fig. 9.6 amounts to 110 dB over 20 kHz bandwidth.
The noise bandwidth of the current source can be reduced by inserting a capacitor across the collector-base junction of transistor T_3. The noise reduces by a factor ten for frequencies above $f_{band} = \frac{1}{2\pi RC}$.

9.9 Conclusion

In integrated circuits accurate and stable reference sources can be designed. These reference sources use the bandgap of silicon as the reference voltage. This bandgap voltage is nearly temperature-independent. Therefore reference sources which use a second-order temperature compensation with temperature coefficients below 1 ppm/degree C can be built. The noise performance of bandgap circuits is good, but improvements are still necessary to be able to apply these reference sources in wideband, high-resolution A/D converters. The signal-to-noise ratio of the described reference sources is adequate for applications in 16- to 18-bit D/A converters in digital audio systems without the need for additional filtering.

Chapter 10

Noise-shaping coding

10.1 Introduction

When digital signal processing is used to perform operations on signals, such as a filtering, a mixing or demodulation operation, the number of bits will change. Mostly an increase in bits is obtained, from which a number of these bits only have a small influence on the performance of the system. Moreover, a practical system implementation is optimized by using the minimally required number of bits. Therefore a truncation, rounding or noise-shaping is used to minimize the number of *effective* bits. Depending on the application a truncation of bits is the mostly used operation. A maximum loss in performance is obtained in this way. Noise-shaping is used to minimize the loss in system performance. A maximum in noise shaping is obtained at the moment the output signal of the system is a $1-bit$ signal. The only way to obtain nearly the full system performance in the $1-bit$ signal is a large oversampling ratio. Examples of applications in oversampled D/A converter systems will be shown. Depending on the order of the filter function which will be performed on the signal the dynamic range will change. Moreover the noise-shaping operation can be used in an A/D conversion systems. Such a system is called a *Sigma – Delta* A/D converter. Applications of these types of converters will be shown. A special first order system to implement a 5-digit digital voltmeter will be discussed.

10.2 Combined digital-analog D/A output filter

In Fig. 10.1 a combined digital-analog filter for audio applications with the filter response are shown. The system consists of a Finite Impulse Response digital filter followed by an oversampled D/A converter which is followed by a nearly linear phase analog output filter. The digital filter performs the

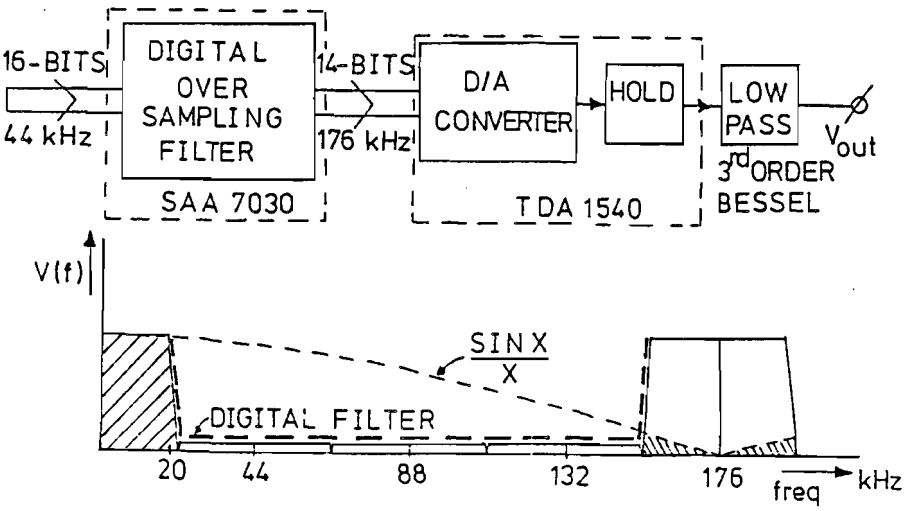

Figure 10.1 : Combined digital-analog low-pass output filter

steep signal filtering at the pass band edge, while the analog filter reduces the repeated spectrum of the input signal at a frequency which is equal to four times the input signal frequency. In this system the input word length is 16 bits. By an oversampling and noise-shaping operation the output word length is reduced to 14-bits without a significant loss in signal-to-noise ratio. In the next sections the noise-shaping operation will be explained.

10.3 Quantization errors

In Fig. 10.2 the quantization errors as a function of frequency are shown. The top part of the figure shows the quantization error of the input signal, while the middle part shows the effect of the four times oversampling operation. As is known from chapter 2, the noise density with a four times oversampling ratio is reduced with a factor four. Limiting the bandwidth of the system to $\frac{1}{2f_s}$ shows a four times reduction in the total quantization error. As a result an increase in dynamic range with one bit is obtained. A

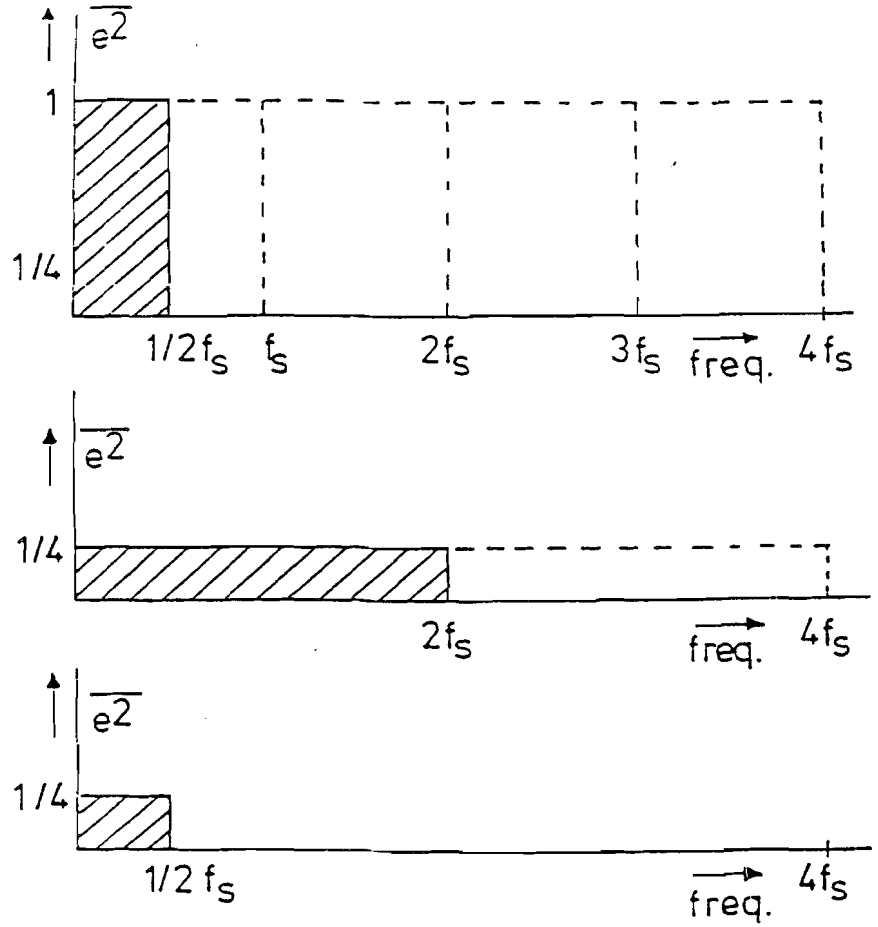

Figure 10.2 : Quantization errors as a function of oversampling ratio

second operation is needed to improve the dynamic range of this system.

10.4 Digital filter configuration

In Fig. 10.3 a simplified block diagram of the oversampling digital low-pass filter is shown. The filter uses a 96 tap FIR structure to perform the low-pass filtering operation. The input word length is 16 bit, while the coefficients have a 12 bit word length. To obtain the oversampling operation, four sets of 24 coefficients having a word length of 12 bits are used to calculate the

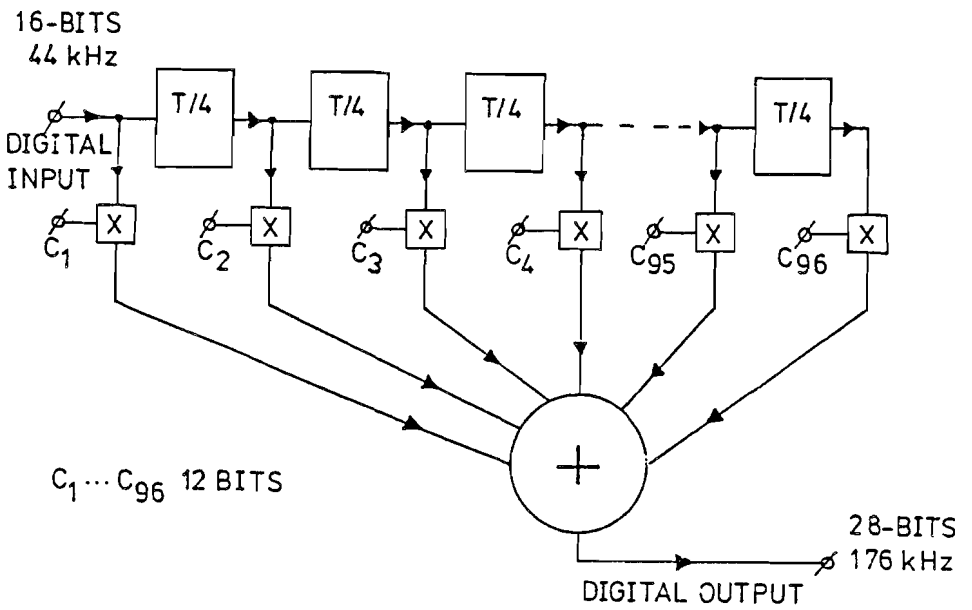

Figure 10.3 : Block diagram of oversampling filter

output words at a four times higher sampling frequency. These words appear at the output with a 28 bit word length. At least 12 of the lower bits do not contribute to the performance of the system. Moreover the D/A converter, which is connected at the output of the filter needs only 14 bits. Therefore an intelligent rounding operation, called noise-shaping will be used to obtain the bit reduction.

10.5 First order noise-shaper

A circuit diagram of the first order noise-shaper is shown in Fig. 10.4. As can be seen from Fig. 10.4 the most significant 14 bits are applied to the output which drives the D/A converter. The lower 14-bits, denoted with ε, are with a one clock delay τ subtracted from the input word. In this way a first order filtering operation is performed. The error which is obtained by this operation can be calculated. We obtain:

$$B_{in} - B_{out} = \varepsilon \times (1 - z^{-1}) \tag{10.1}$$

The first order filter operation reduces the error ε. The total amount of quantization error can be found by integrating the error over the signal

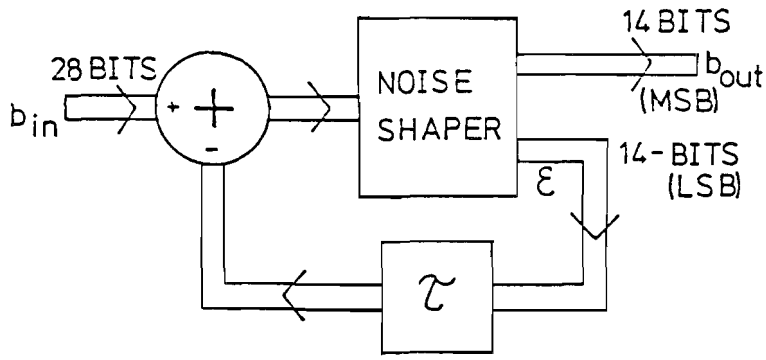

Figure 10.4 : First-order noise-shaper

bandwidth f_b. This results in:

$$e_{tot}^2 = \int_0^{\theta_1} \varepsilon^2 | \, 1 - z^{-1} \, |^2 d\theta \tag{10.2}$$

In this equation $| \, 1 - z^{-1} \, |^2$ corresponds to the amplitude characteristic of the first order noise filter and $\theta_1 = \frac{2\pi f_b}{f_s}$. Inserting for $z = e^{j\theta}$ we obtain:

$$| \, 1 - z^{-1} \, |^2 = \frac{| \, e^{j\theta} - 1 \, |^2}{| \, e^{j\theta} \, |^2} \tag{10.3}$$

Working out equation 10.3 the following result for the amplitude characteristic is obtained:

$$| \, 1 - z^{-1} \, |^2 = 2(1 - \cos\theta) \tag{10.4}$$

In Fig. 10.5 the square of the amplitude response as a function of frequency is shown. Note that at half the sampling frequency the gain in the system is two. Inserting equation 10.4 into equation 10.2 and integrating the function results in:

$$e_{tot}^2 = 2(\theta_1 - \cos\theta_1) \times \varepsilon^2 \tag{10.5}$$

If no noise-shaping was performed then the total uniformly distributed noise over the same bandwidth equal to:

$$e_{uniform}^2 = \varepsilon^2 \int_0^{\theta_1} d\theta = \varepsilon^2 \theta_1 \tag{10.6}$$

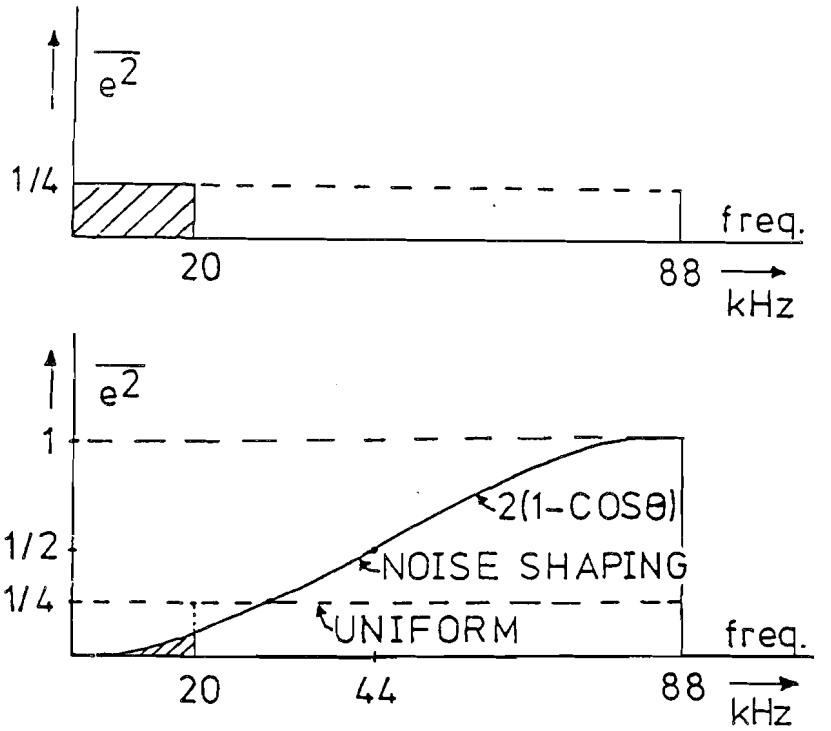

Figure 10.5 : Square of the filter amplitude response

Comparing the results of equations 10.5 and 10.6 the improvement in dynamic range of the system is obtained. Using F as the dynamic range improvement factor we get:

$$F = \sqrt{2(1 - \frac{\sin\theta_1}{\theta_1})} \quad with \quad \theta_1 = \frac{2\pi f_b}{f_s}. \tag{10.7}$$

The oversampling factor obtained by the digital filtering operation introduces an extra decrease in noise with a factor G. This factor can be expressed in terms of sample rate f_s and signal bandwidth f_b or:

$$G = \sqrt{\frac{2f_b}{f_s}}. \tag{10.8}$$

The total improvement H in the signal-to-noise ratio due to noise shaping and oversampling becomes:

$$H = \frac{1}{F \times G} = \frac{1}{2\sqrt{\frac{f_b}{f_s}(1 - \frac{sin2\pi f_b/f_s}{2\pi f_b/f_s})}}. \tag{10.9}$$

Inserting values for $f_s = 176$ kHz and $f_b = 20$ kHz, H becomes 14.2 dB.
The signal-to-noise ratio of a 14-bit D/A converter with oversampling filter and noise shaping becomes 85.8 + 14.2 = 100.0 dB.
At the input of the system a 16-bit input word is applied. As a result of the total operation the signal-to-noise of the system becomes:

$$S/N_{system} = \frac{S/N_{16bits}}{\sqrt{1+k^2}} \tag{10.10}$$

With $k = 0.776$, the signal-to-noise ratio of the system becomes:

$$S/N_{system} = 95.8dB. \tag{10.11}$$

The total operation of noise shaping and a four times oversampling results in an increase of the dynamic range of the 14-bits D/A converter with nearly 2 bits.

10.6 First order noise-shaper with large oversampling factor

When the sampling frequency f_s in a system is much larger than the signal bandwidth f_b, then $\sin\theta_1$ can be approximated by:

$$\sin\theta_1 \approx \theta_1 - \frac{\theta_1^3}{3!} \tag{10.12}$$

Inserting this approximation into equation 10.7 results in:

$$F \approx \frac{\theta_1}{\sqrt{3}} \tag{10.13}$$

Using this result in equation 10.9 the total improvement due to noise-shaping with a large oversampling ratio becomes:

$$H \approx (\frac{f_s}{f_b})^{\frac{3}{2}}\sqrt{\frac{3}{8\pi^2}} \tag{10.14}$$

When the oversampling ratio is increased with a factor two, then the improvement in dynamic range increases with approximately $2^{\frac{3}{2}}$. This method of "rounding" to a limited amount of significant bits does not result in a significant loss in dynamic range of the total system although less bits are effectively used.

10.7 Higher order noise-shaper

To obtain a more effective noise-shaping the order of the filter can be increased. At that time the amount of noise in the system passband is reduced resulting in a larger increase in dynamic range of the system without increasing the sampling rate with respect to the system bandwidth.
Suppose a filter of the order n is used as a noise-shaper, then equation 10.7 changes into:

$$F(n) = [2(1 - \frac{\sin\theta_1}{\theta_1})]^{\frac{n}{2}} \tag{10.15}$$

Taking into account the increase in dynamic range due to the oversampling ratio given by equation 10.8, the total improvement $H(n)$ in signal-to-noise ratio due to an n^{th} order noise shaping filter becomes:

$$H(n) = \frac{1}{F(n) \times G(n)} = \frac{1}{\sqrt{\frac{2f_b}{f_s}}[2(1 - \frac{\sin 2\pi f_b/f_s}{2\pi f_b/f_s})]^{n/2}} \tag{10.16}$$

In Fig. 10.6 the noise-shaping functions as a function of frequency for a first and second order filter operation are shown. Note that over the signal band of interest (0 to B) the total noise is reduced with the second order filtering operation. When the oversampling ratio is large, then equation 10.16 can be simplified using the series expansion as shown in equation 10.12. In this case equation 10.13 changes into:

$$F(n) \approx (\frac{\theta_1}{\sqrt{3}})^n \tag{10.17}$$

The total improvement in signal-to-noise ratio in this case can be approximated by:

$$H(n) \approx \sqrt{\frac{f_s}{2f_b}}(\frac{\sqrt{3}f_s}{2\pi f_b})^n \tag{10.18}$$

When the oversampling ratio ($\frac{f_s}{2f_b}$ is increased with a factor two, then the signal-to-noise ratio increases according to equation 10.18 with a factor:

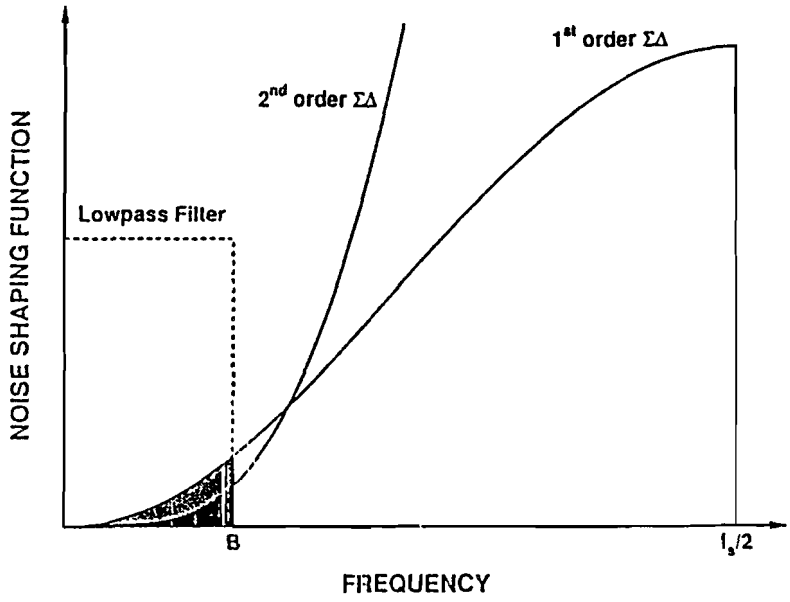

Figure 10.6 : First and second order noise-shaping functions

$2^{n+\frac{1}{2}}$.

The signal-to-noise ratio at the output of the system can easily be calculated. Especially when the amount of output bits is small, then equation (2.12) must be used. Suppose that m effective output bits are used, then the signal-to-noise ratio becomes:

$$S/N = (2^m - 2 + \frac{4}{\pi})\sqrt{1.5} \times H(n) \tag{10.19}$$

m is the number of effective output bits.

In equation 10.19 H(n) represents the improvement in dynamic range due to the n^{th} order noise-shaping filter. When the oversampling ratio is large then equation 10.19 can be expressed as:

$$S/N = (2^m - 2 + \frac{4}{\pi}) \times \sqrt{\frac{1.5 f_s}{2 f_b}}(\frac{\sqrt{3} f_s}{2\pi f_b})^n. \tag{10.20}$$

From this equation it can be seen that the signal-to-noise ratio increases with more than 6 dB per bit when the number of output bits is increased from a 1-bit signal into a multi-bit signal. The non-linear relation of the

signal-to-noise ratio on the number of bits with a small number of used bits causes this phenomenon. In the following table this result is shown.

10.8 Sigma-delta D/A converters

At the moment the number of effective output bits m is reduced to one, a 1-bit digital-to-analog converter or sigma-delta D/A converter is obtained. In Fig. 10.7 the signal-to-noise ratio with large oversampling ratio as a function of the order of the noise-shaper order is shown. When an oversampling

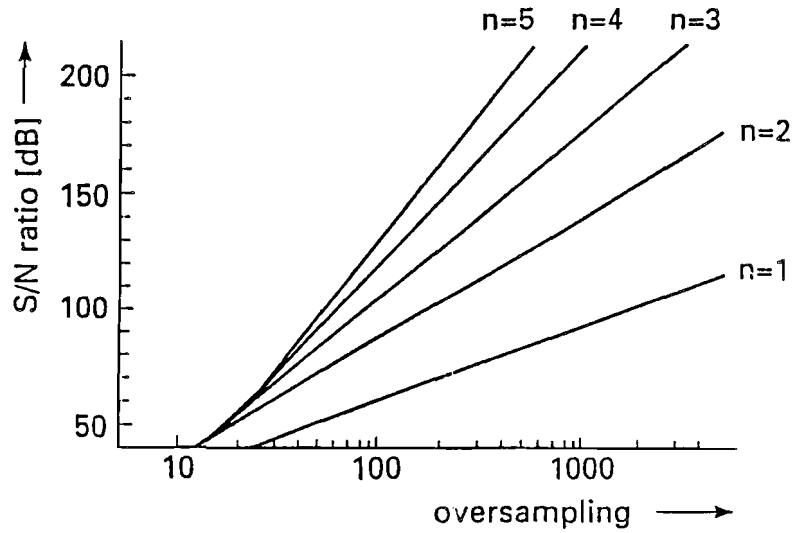

Figure 10.7 : Signal-to-noise ratio as a function of oversampling ratio with the filter order as parameter

ratio of about 100 is used with a second order noise-shaper, then a 16-bit D/A converter for applications in digital audio systems can be designed.
In Fig. 10.8 a block diagram of the total D/A converter is shown. At the input of the converter the 16-bits serial data is converted into a 16-bits parallel data word with a sampling frequency f_s. This conversion is performed by the block called SIPO. The 16-bit parallel data is then increased in sample rate with a factor 4 using the first oversampling filter. This filter can be of the type shown in Fig. 10.3. The output sampling rate is $4f_s$. Then a second oversampling with a factor 64 is introduced. In this filter a linear interpolation with a factor 64 is used between two data points. As a result of this linear interpolation a filtering with a factor $(\frac{\sin x}{x})^2$ is obtained. The

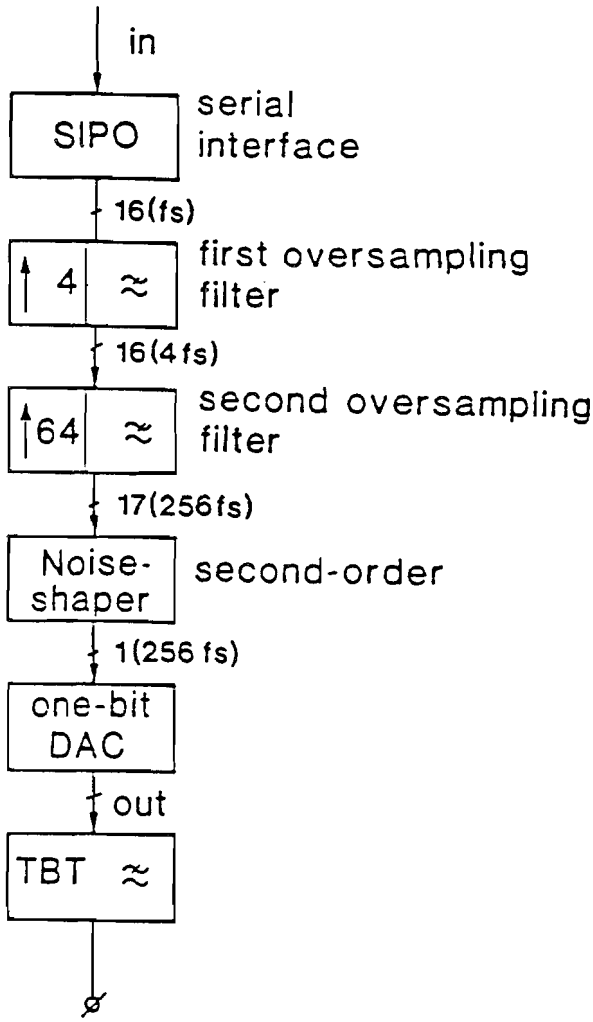

Figure 10.8 : Block diagram of an oversampled D/A converter system

output sample rate is now increased to $256f_s$. The second oversampling filter is followed by a second order noise shaper. The output of this noise shaper is a 1-bit signal with a sample rate of $256f_s$. This signal is applied to a 1-bit D/A converter which reproduces the analog signal. The output of the 1-bit D/A converter is followed by a linear phase low pass filter to remove the high-frequency components of the audio signal.
In Fig. 10.9 the amplitude characteristics of the oversampling filters and

the total D/A converter are shown. The amplitude response of the analog low-pass filter (T.B.T.) is compensated for by an amplitude increase of the digital filter. As a result a very accurate filtering characteristic is obtained with a very small amplitude ripple (less than 0.01 dB). As is shown in Fig.

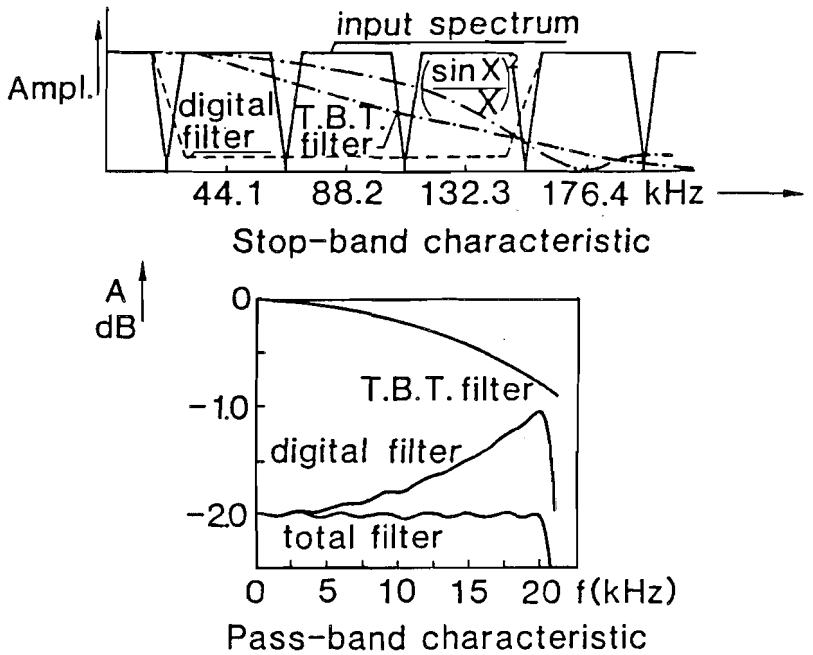

Figure 10.9 : Amplitude characteristics of the D/A converter filters

10.9 a sharp filtering in the first four times oversampling filter is needed to reject the repeated input spectra of the digital signal with frequency f_s = 44.1 kHz. A block diagram of the second order noise-shaper is shown in Fig. 10.11. The quantizer Q in Fig. 10.10 generates the 1-bit signal. In higher order noise shapers it is necessary to implement a limiter function to avoid overloading of the system which may lead to unwanted limit cycles. In normal operation the limiter is transferring the input signal to the subtractor. The output of the subtractor is applied to the noise-shaping filter $H(\omega)$. In a first order noise-shaper $H(\omega)$ is represented by a delay. In a second order system a more complex function for $H(\omega)$ is needed. In Fig. 10.11 a switched capacitor implementation of a 1-bit D/A converter using a single reference voltage V_1 is shown. The system consists of a set of switches driven by the two phases of the clock signal CL. A charge "bucket" is stored in capacitors C_1 and C_2 respectively. The two switches driven by the signals P^+ and P^-

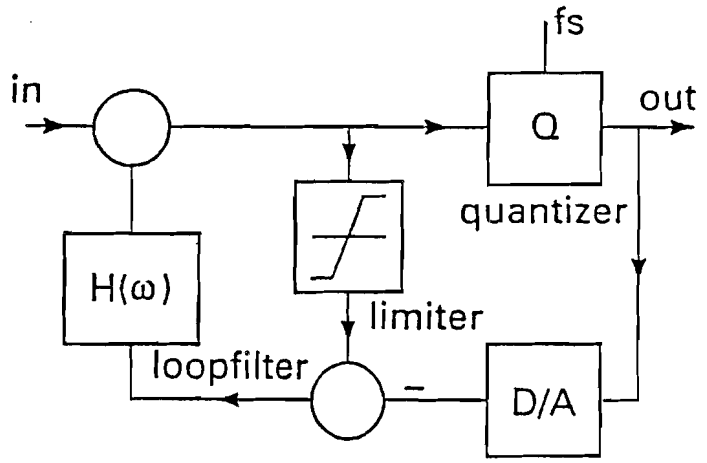

Figure 10.10 : Block diagram of the noise-shaper

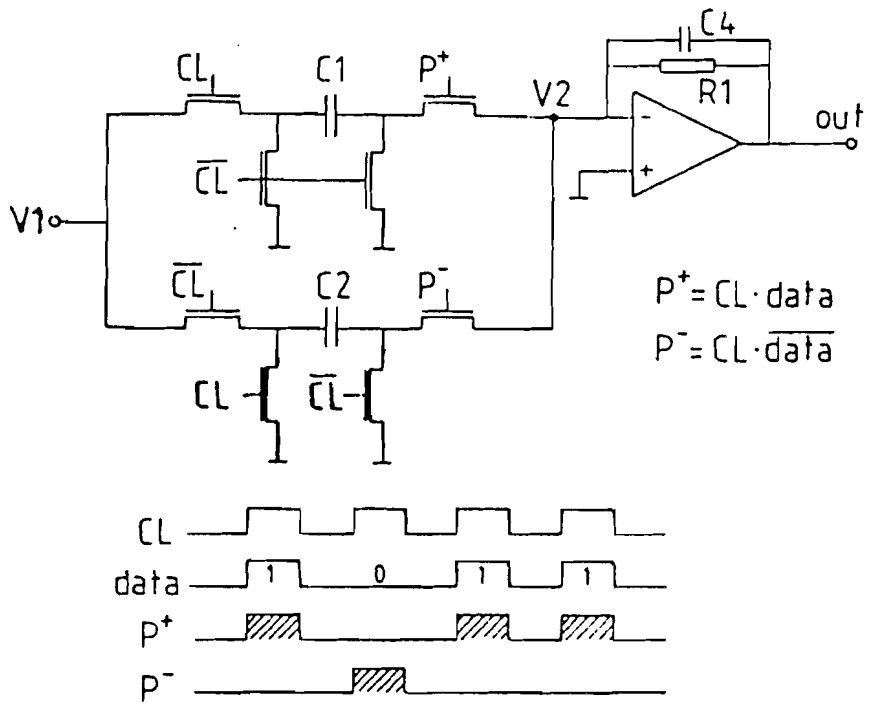

Figure 10.11 : Switched capacitor 1-bit D/A converter

determine if a charge packet ($Q = C_1V_1 = C_2V_1$) is added or subtracted from the output signal. The output signal is generated and filtered by C_4 and R_1 using an operational amplifier to keep the voltage swing V_2 very small. The filter constant C_4R_1 is part of the analog low-pass output filter which suppresses the high frequency spectra of the signal. In Fig. 10.12 the frequency spectrum of the 1-bit D/A converter signal without analog low-pass filtering is shown. From the figure it is seen that the noise in the pass-band is very

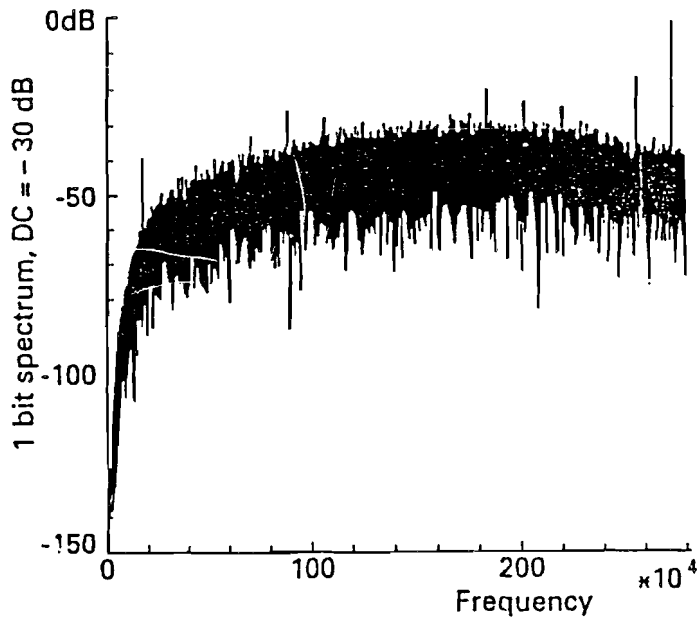

Figure 10.12 : 1-bit D/A converter spectrum

small and "pushed" to higher frequencies. As a result of this filtering effect the dynamic range of the system increases over the (small) signal band of interest. The figure visualizes the noise-shaping operation.

10.9 Sigma-delta A/D converters

In Fig. 10.13 a general form of a sigma-delta A/D converter system is shown. From the input signal the output of the 1-bit D/A converter is subtracted. The difference of these two signals is filtered by the loopfilter and the output signal of the loopfilter is applied to the 1-bit quantizer or A/D converter. The clock frequency of the system is high compared to the maximum analog input frequency while the order of the loopfilter determines the dynamic

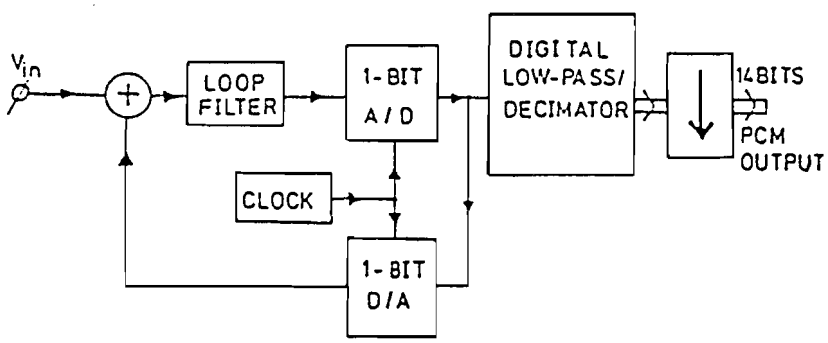

Figure 10.13 : Sigma-delta A/D converter system

range of the system. Identical equations apply for this system as given in the D/A converter section. The output of the 1-bit A/D converter is usually applied to a digital low-pass which rejects signals above the signal band of interest. Then subsampling or decimation is applied. The whole operation results in a binary weighted digital output signal which can have a minimum sampling ratio equal to twice the signal bandwidth.
When the loop filter which is applied in this system consists of a continuous-time filter, then the analog signal band is filtered with the same filtering characteristic as is applied for noise-shaping. A very cost effective solution is obtained in this way. When a discrete-time loopfilter is used, then the ant-alias filtering must be performed before the analog signal enters the A/D converter. Discrete-time filters are mixing the high frequency input signals with the sampling clock resulting in aliasing of signals which is not allowed.
If no analog input signal is applied to the A/D converter. then an idle pattern consisting of "1" and "0" signals at half the sampling clock is obtained. The one-zero pattern changes when an analog input signal is applied to the converter. The number of ones or zeros changes in such away that the analog input signal is nearly equal to the average output signal generated by the 1-bit D/A converter. The maximum output signal can be nearly equal to the positive or the negative reference voltage. As long as the switches in the D/A converter show a nearly ideal performance then the linearity of the converter is not determined by the reference voltages, because by changing the one-zero pattern the output signal of the D/A converter varies according to a straight line between the minus reference voltage and the plus reference

voltage.
In Fig. 10.14 an example of the output signal of the A/D converter with a sine wave analog input signal is shown. To make the figure understandable the one-zero idle pattern at half the sampling frequency is removed with a simple digital filter. Note that in the top of the sine wave a large amount of "ones" is generated while in the bottom part of the sine wave a large amount of "zeros" is obtained. An example of an A/D converter using a continu-

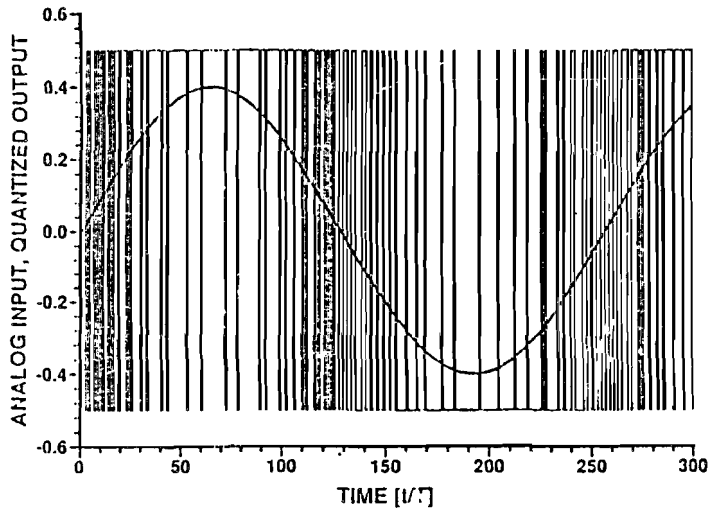

Figure 10.14 : Sigma-delta A/D converter input and output signals

ous time first order filter with a time-discrete 1-bit D/A converter is shown in Fig. 10.15. In the D/A converter a switched capacitor D/A converter approach is used. This construction is less sensitive to sampling clock uncertainties because a charge "bucket" is transferred to the integrator at every clock moment. The amount of charge is determined by the reference voltage V_{ref} and the capacitors C_1. Furthermore the switches in the D/A converter are arranged in such away that only a single reference voltage V_{ref} is needed to transfer a charge or discharge packet into integrator. Note that in this system the analog input signal is filtered by the integrator too. Although the filtering attenuation is small it helps to simplify the anti-alias filter at the analog input (this filter is not shown in the figure).
An example of a third-order noise-shaping A/D converter is shown in Fig. 10.16. In this system a switched capacitor technique is used in the loopfil-

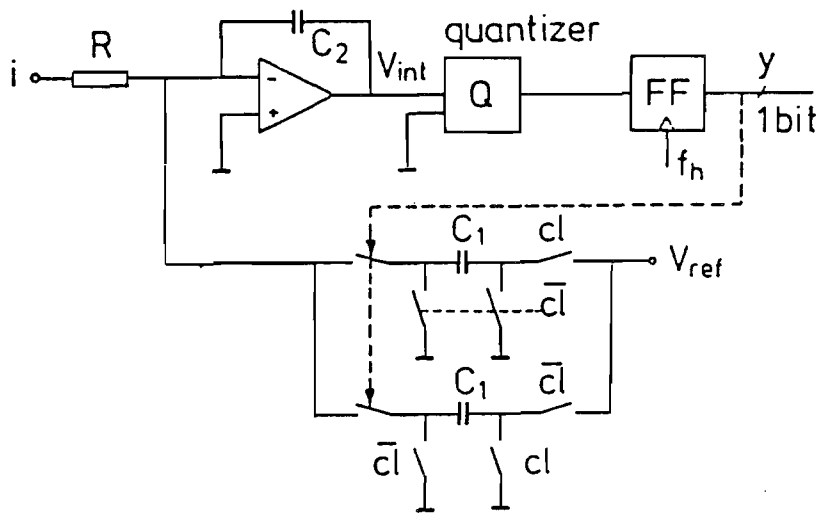

Figure 10.15 : A/D converter with continuous time loopfilter

ter to obtain a high filtering accuracy. Note that in this system the high

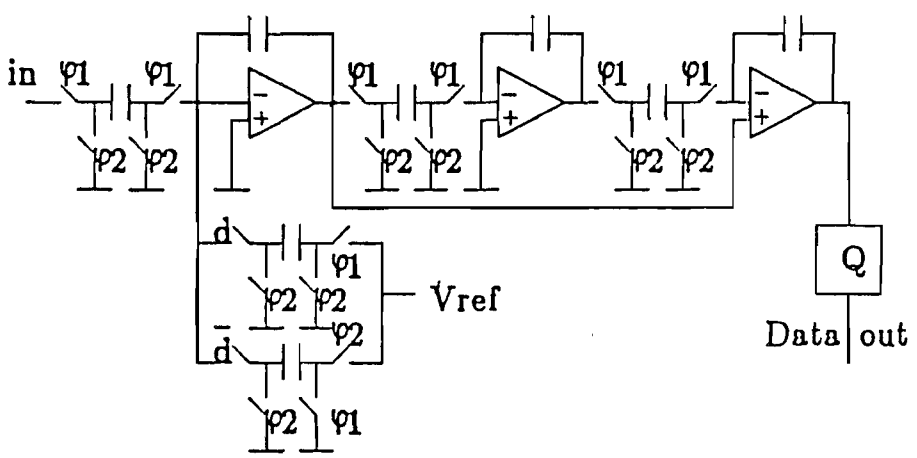

Figure 10.16 : Third order switched capacitor noise-shaping A/D converter

frequency components must be filtered out before an analog signal can be applied to the system to avoid aliasing.

10.10 Different A/D converter configurations

When higher-order noise-shaping filters are applied in sigma-delta converters then problems arise with the "stability" of the system. Mostly with "stability" it is meant that the system shows a stable idle pattern at half the sampling frequency. When signals are applied the idle pattern must remain at half the sampling frequency, which is not always the case.
In Fig. 10.17 examples of a second and third order noise-shaping coder are shown. To avoid the stability problem of for example a third order noise-

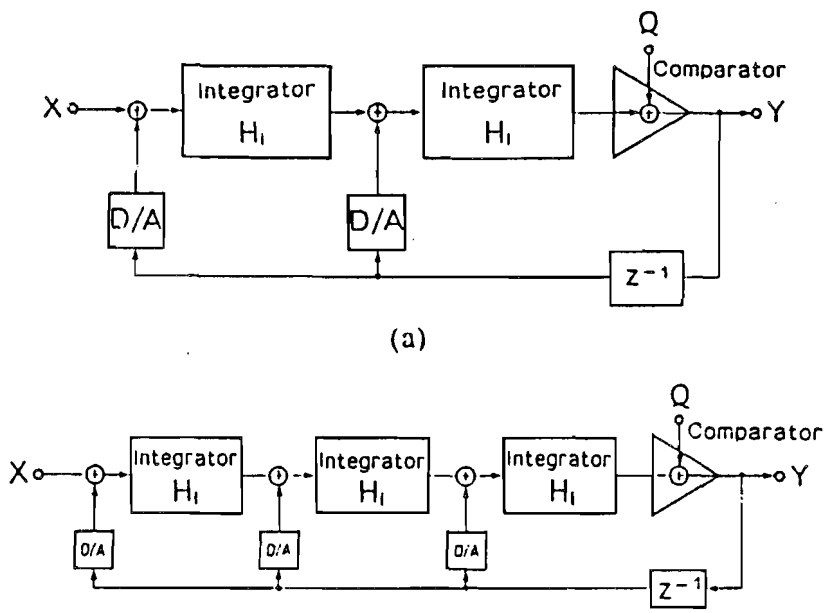

Figure 10.17 : Examples of noise-shaping coder systems

shaping coder a so called "MASH" converter system consisting of three cascaded first order coders is used. In Fig. 10.18 this system is shown. From the figure it is seen that the error signal P_1 of the first first-order noise-shaping coder is applied to the second first-order coder. This second order coder quantizes the error signal with and after differentiation of the output signal the output signal is corrected. Then the error signal P_2 of the second coder is applied to the third coder which quantizes this signal again. After a two times differentiation the signal of the third quantizer is added to the output signal again. As a result of this operation the order of the noise shaping coder is increased from a first order of the first encoder up to a

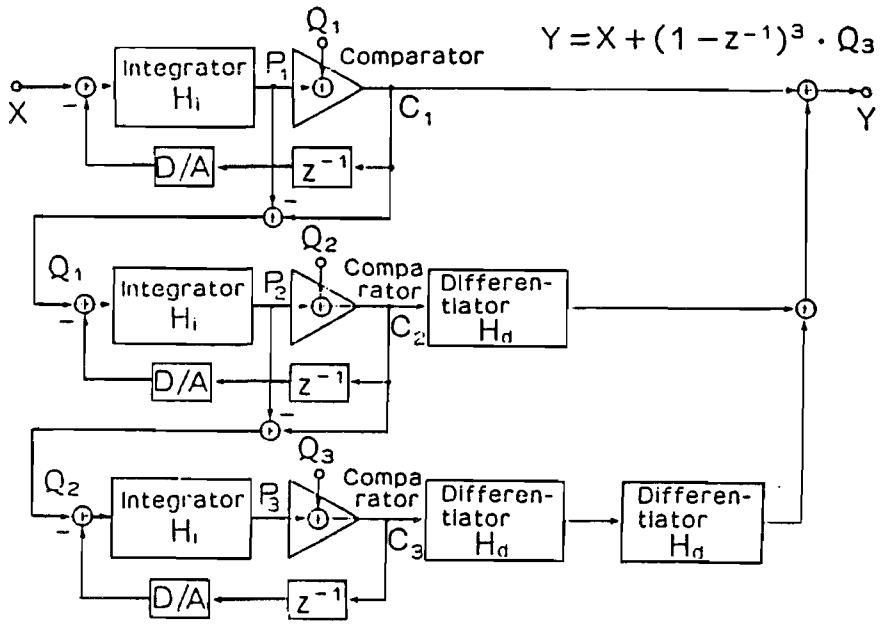

Figure 10.18 : MASH noise-shaping coder system

third order. This increase in noise-shaping filtering performance is obtained without introducing a stability problem because every individual stage of the encoder is a first order noise-shaper. The only problem in this system is the accuracy with which the output signal P_1 is encoded with respect to the full resolution of the total system. Therefore accuracy problems may be found when this system is simply increased to fifth or even higher order noise-shaping filtering.

A disadvantage of the MASH converter structure is found to be the threshold of the first order converter sections. As a result of this threshold no small input signal above a certain input frequency will be coded. In the upcoming section about threshold level this phenomenon will be explained in more detail.

The higher order coders do not suffer so much from the threshold level and are therefore preferred for high performance converters.

10.11 "Follow-the-Leader" A/D converter system

A system which combines the higher-order filter function for small signals with gliding filter order function depending on the signal amplitude tending to reduce into a first-order for large signals is shown in Fig. 10.19. Basically

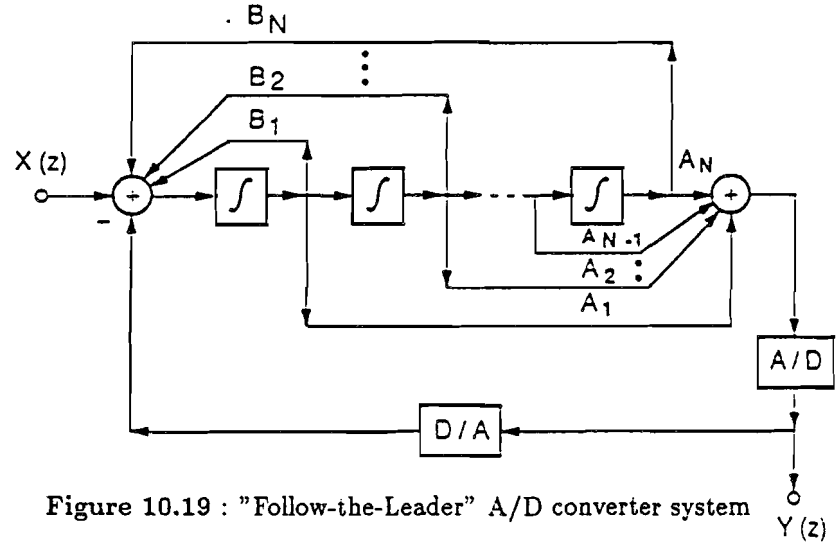

Figure 10.19 : "Follow-the-Leader" A/D converter system

the system consists of a cascade of integrator sections. A feedforward technique using coefficients A_N with N depending on the number of stages, feeds signals directly to the comparator stage (1-bit A/D). When the input signal increases, then the signals amplified so much that a clamping occurs. At that moment the feed-forward operation takes over and a stable system is obtained.

10.12 Idle noise pattern

The idle noise pattern which is generated in sigma-delta converters depends on the order of noise shaping used in the coder. In Fig. 10.20 an example of an idle noise pattern with zero input and with a sine wave input signal are shown. When well determined dc input signals are applied to a first order converter, the some stable patterns can be found. The following analysis

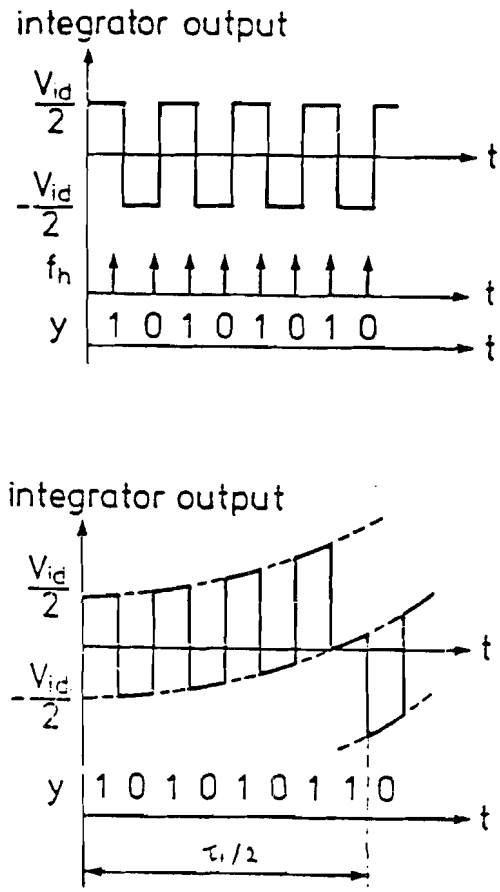

Figure 10.20 : (a) Idle noise pattern of a sigma-delta A/D converter with zero input signal and (b) with a sine wave input signal

gives some of the most common patterns.
Suppose that during n_1 successive clock pulses the capacitor is charged and during n_2 clock pulses the capacitor is discharged. Suppose furthermore that after n_r repetitions of the previous pattern during one clock pulse and additional charge pulse is added then we obtain for the total charge:

$$Q_{charge} = n_r \times n_1(Q_{ref} - Q_{analog}) + Q_{ref} - Q_{analog} \qquad (10.21)$$

The amount of charge which is discharged from the integration capacitor becomes:

$$Q_{discharge} = n_r \times n_2(Q_{ref} + Q_{analog}) \qquad (10.22)$$

The operation of the A/D converter forces the total charge and discharge to cancel, which means:

$$Q_{charge} = Q_{discharge} \tag{10.23}$$

After rearranging we obtain:

$$\frac{Q_{analog}}{Q_{ref}} = \frac{n_r(n_1 - n_2) + 1}{n_r(n_1 - n_2) + 1}. \tag{10.24}$$

Note that if a positive input signal is applied, then the number of discharge pulses n_2 must be equal to 1 to obtain the required idle pattern at half the sampling frequency. At the same time n_1 becomes 1 for a negative input signal.
A special class of stable patterns is obtained when the repetition n_r becomes very large ($n_r \gg 1$). Equation 10.24 simplifies into:

$$\frac{Q_{analog}}{Q_{ref}} = \frac{n_1 - n_2}{n_1 + n_2} \tag{10.25}$$

Again with a positive input signal n_2 is 1 and with negative input signals n_1 is 1.
Using $n_2 = 1$ and varying n_1 from 1, 2, 3 etc. an analog input signal of 0, $\frac{1}{3}Q_{ref}$, $\frac{1}{2}Q_{ref}$ etc. must be applied.
The drawback of stable patterns is found in the non-uniform distribution of the quantization noise. At that moment correlations with the input signal are obtained. Such correlations may results in whistles and birdies in the quantized signal. In audio applications such a correlation is not allowed because the human ear is very sensitive for repetitive signals.

10.13 Input signal threshold of a first-order A/D converter

The idele noise pattern which is generated in a sigma delta A/D converter introduces a threshold level below which no signal quantization is obtained. A signal is quantized at the moment the integrated input signal is equal to half the amplitude of the idle noise pattern. An example of such a quantization is shown in Fig. 10.20(b). The figure shows that at the moment the amplitude of the integrated input sine wave crosses the zero line, then an extra discharge pulse is needed. This extra discharge pulse changes the 1 0 1 0 . . pattern into a 1 0 1 0 1 1 0 pattern. The extra 1 contains the

quantization information.
The threshold level of the A/D converter shown in Fig. 10.15 can rather simply be calculated. Suppose that no input signal is applied to the converter and suppose furthermore that all elements are ideal, then the amplitude of the idle noise pattern becomes:

$$V_{id} = \frac{C_1}{C_2} V_{ref} \tag{10.26}$$

Here V_{id} is the peak-to-peak amplitude of the idle noise pattern and V_{ref} is the reference voltage appied to the converter. The discrete-time D/A converter used results in a gain ratio determined by the capacitors C_1 and C_2. The input signal is integrated using the continuous time integrator with R and C_2.
If a sine wave $V_p \sin \omega_{in} t$ with a small amplitude is applied to the converter, then this signal is integrated and added to the charge generated by the capacitive D/A converter circuit. Suppose that the amplitude of the input signal is so small that it takes a time τ_1 before the idle noise pattern is disturbed. The amplitude of the sine wave signal over the time τ_1 then becomes:

$$\int_0^{\tau_1} \frac{V_p}{R} \sin 2\pi f_{in} t dt = C_2 V_{out} \tag{10.27}$$

After reworking equation 10.27 the output voltage V_{out} becomes:

$$V_{out} = \frac{1}{2\pi f_{in}} \frac{V_p}{C_2 R} [\cos(2\pi f_{in} \tau_1) - 1] \tag{10.28}$$

The minimum value of equation 10.28 is obtained if:

$$2\pi f_{in} \tau_1 = \pi \ or \ \tau_1 = \frac{1}{2 f_{in}}. \tag{10.29}$$

Inserting the value of 10.29 into equation 10.28 results in:

$$V_{out} = -\frac{1}{\pi f_{in}} \frac{V_p}{C_2 R} \tag{10.30}$$

The maximum value of equation 10.28 is obtained when $\cos 2\pi f_{in} \tau_1 = 1$. Then a maximum output signal $V_{out} = 0$ is obtained. The peak-to-peak value of the output signal V_{out} is equal to the value given by equation 10.30. The idle noise pattern is disturbed when the output voltage $V_{out} = \frac{1}{2} V_{id}$. The following result is then obtained:

$$V_{out} = V_{id} \tag{10.31}$$

To obtain a relation between the maximum input signal value V_{max} and the threshold level of the converter, a relation between the reference voltage V_{ref} and the maximum signal level is needed. Using a charge balance equation the following relation is valed:

$$\frac{V_{max}}{R}\frac{1}{f_s} = V_{ref}C_1 \tag{10.32}$$

After combining equations 10.26, 10.27, 10.30 and 10.32 the following result is obtained:

$$V_p = -\pi\frac{f_{in}}{f_s}V_{max} \tag{10.33}$$

The peak threshold voltage can be defined as:

$$V_{th} = \mid V_p \mid \tag{10.34}$$

Inserting equation 10.34 into equation 10.33 results in:

$$V_{th} = \frac{\pi f_{in}}{f_s}V_{max} \tag{10.35}$$

From equation 10.35 it is seen that the threshold voltage linearly increases with the input signal frequency. The result of the threshold is the introduction of signal distortion. This distortion increases with increasing input frequency. The threshold voltage can be reduced by increasing the order of the loopfilter.

10.14 Threshold voltage of a second-order converter

In the second-order sigma-delta A/D converter an extra integrator is inserted in the loop. To obtain stability, which means an idle noise pattern around $\frac{f_s}{2}$ a zero must be added. A good practical approach is found when the frequency f_n of the zero is at about $\frac{1}{10}f_s$. Because of the increased loop gain a reduction of the threshold voltage is obtained at lower frequencies. An estimate of the threshold voltage can be determined. The result becomes:

$$V_{th} = \frac{\pi f_{in}^2}{f_s f_n}V_{max} \tag{10.36}$$

From equation 10.36 it is found that the threshold reduces with a factor $\frac{f_{in}}{f_n}$. With large oversampling ratios the improvement is obtained. However, a

second order system results in an increase in dynamic range. In practive this results in the fact that the frequency for which the threshold is reached is still in the signal band of interest.
At that moment the threshold determines the dynamic range and not the loopfilter. To overcome this problem a dither signal is mostly added. Such a dither signal linearizes and reduces the threshold resulting in an improvement is dynamic range and a lower distortion.

10.15 Dither signals

To avoid correlation of idle patterns with the input signal in an A/D converter a dither signal can be applied. Such a dither signal can be a small noise signal or a signal at half the sampling frequency. The amplitude of this dither signal is small to avoid a reduction in dynamic range of the total converter system. The purpose of the dither signal is to disturb the fixed signal patterns in the converter. In this way no correlation of the quantization noise and the input analog signal exists so a noiselike error signal is obtained. At the same time the dither signal reduces the threshold of the converter resulting in a reduction in distortion of the signal and a coding of low level high frequency input signals. In Fig. 10.21 the frequency spectrum of the error signal of an A/D converter with a sine wave input and no dithering is shown. From the spectrum shown in Fig. 10.21 a large number of correlated signal components can be distinguished. When a small dither signal is applied then the error spectrum is more randomized. The result is shown in Fig. 10.22. As can be seen from the spectrum the amplitude is reduced while the number of correlated components is reduced.

10.16 Threshold signal distortion

When a signal is applied to a transfer function with a threshold around zero then a distortion is obtained. Applying a sine wave at the input of the converter, then the output signal can be approximated by a sine wave minus a square wave with an amplitude equal to the threshold voltage and a frequency equal to the input sine wave.
Using equation 10.35 the amplitude of the square wave is found. This square wave is expanded in harmonic terms. When no dc components are found

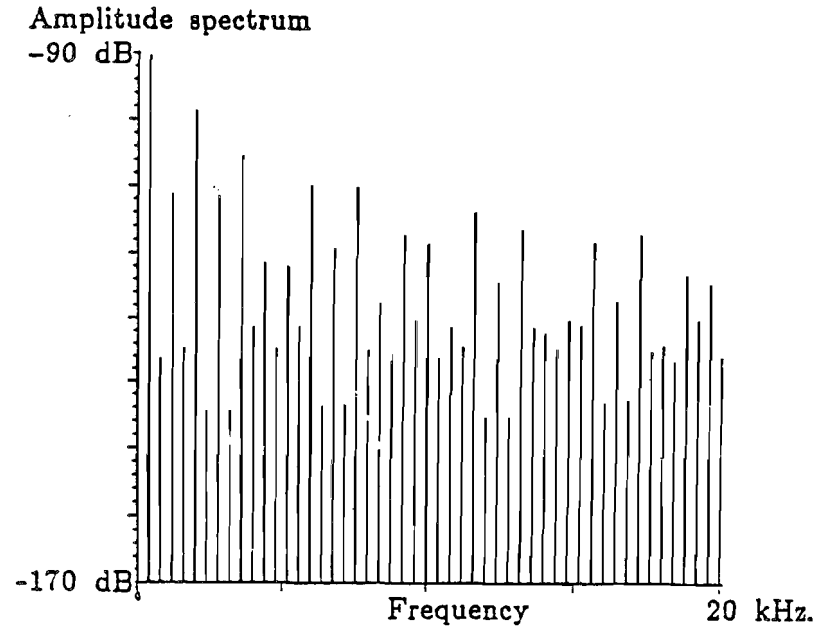

Figure 10.21 : Error signal spectrum of an A/D converter with an undithered sine wave

then the following series exapnsion is found:

$$V_{sq} = \frac{4V_{th}}{\pi}(\sin f_{in} + \frac{\sin 3f_{in}}{3} + \frac{\sin 5f_{in}}{5} + ... \qquad (10.37)$$

From the series expansion shown in 10.37 only odd harmonics are found. This is verified using a simulation of a practical system. In Fig. 10.23 the result of the simulation is shown. In a practical situation the full signal level V_{max} can not be obtained because of overloading of the system. The simulation result shows the increase of the distortion and noise at the high frequency band edge of the system. This is because of the noise shaping. At the moment a dc offset is added to the system, then the series expansion changes and even order terms will appear too. Equation 10.37 now changes into:

$$V_{sqdc} = \frac{Vth}{2}[k + \frac{2}{\pi}(\sin k\pi \cos f_{in} + \frac{1}{2}\sin 2k\pi . \cos 2f_{in} + .. \qquad (10.38)$$

In a practical situation k is between $\frac{1}{2}$ and $\frac{1}{4}$ for a dc offset between zero and about $\frac{V_{th}}{2}$. In equations 10.37 and 10.38 V_{sq} and V_{sqdc} are the amplitudes

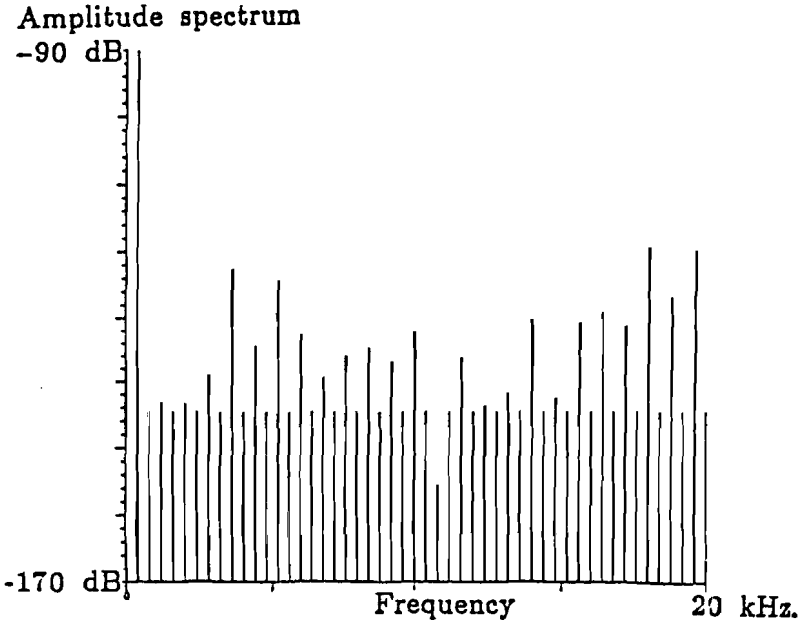

Figure 10.22 : Error spectrum of a dithered sine wave signal

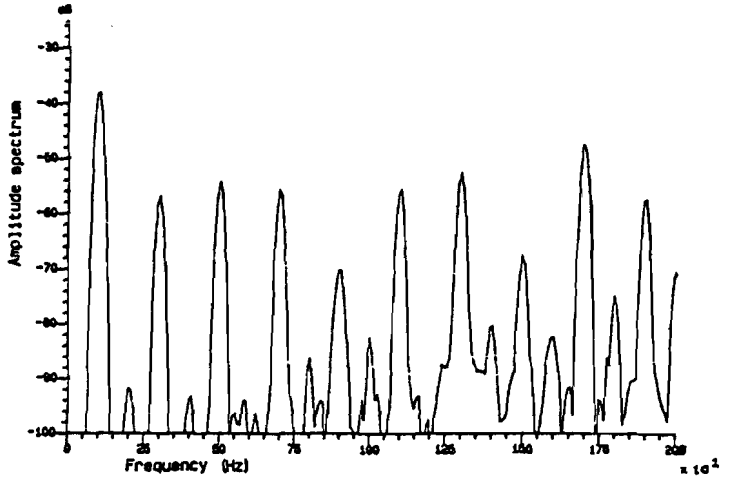

Figure 10.23 : Distortion simulation of a sigma-delta Λ/D converter

of the fundamental and the distortion products introduced by the threshold level of the converter. The ratio between these components and the maximum signal level V_{max} results in the distortion of the converter.

10.17 Sigma-delta digital voltmeter

An example of a first order sigma-delta modulator used as a five digit digital voltmeter A/D converter will be discussed. The system uses full time pulses in the D/A converter together with a continuous time first order filtering operation. The basic converter system is shown in Fig. 10.24. The input

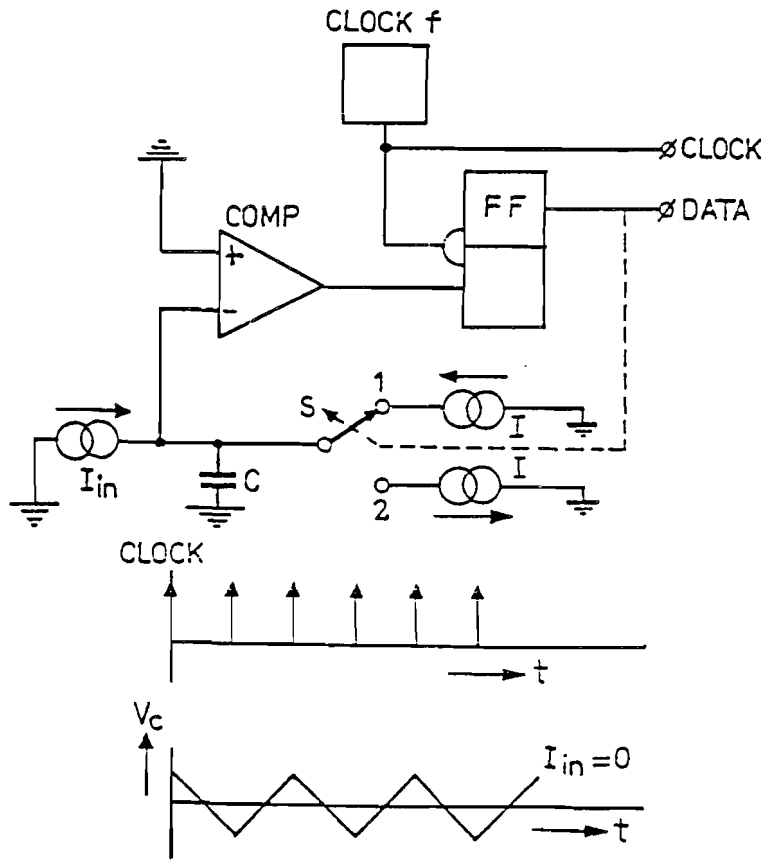

Figure 10.24 : Basic sigma-delta digital voltmeter system

signal is applied to the converter as a current I_{in}. The charge and discharge reference currents are called I. The signal is integrated across the capacitor C. The voltage across the capacitor is monitored by the comparator *comp* which drives the flip flop FF. This flip flop is toggled by the system clock f. The output of the flip flop controls the switch S which switches the charge or discharge currents I to the capacitor C. When no input signal is applied to the system, then a triangular wave is generated across the capacitor C.

The average value of the capacitor voltage is zero. When an input signal is applied, then the one-zero pattern changes. The output of the flip flop called *Data* is applied to an up-down counter which performs the conversion of the 1-bit sigma-delta signal into a binary weighted output signal. In Fig. 10.25 the total digital voltmeter system is shown. The sigma-delta converter

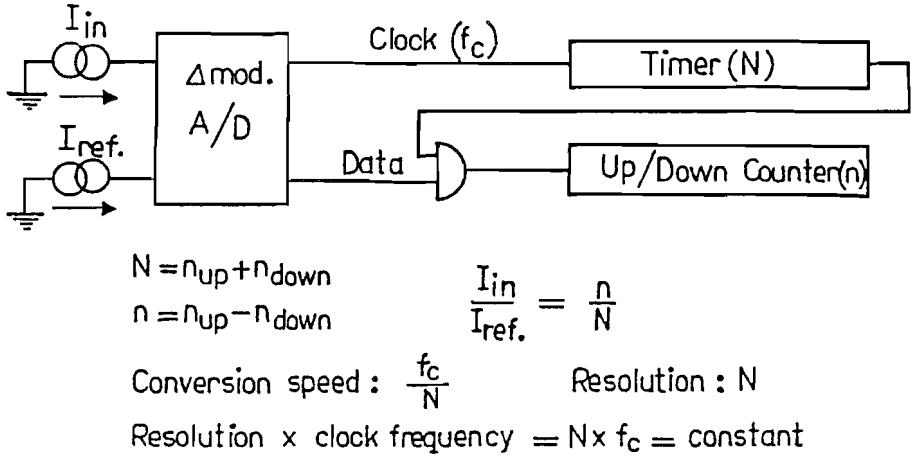

Figure 10.25 : Total digital voltmeter system

is enlarged with a timer (*Timer*(N)), an up/down counter and a gating function. The timer function counts the total amount of up and down pulses $N = n_{up} + n_{down}$. During this time the gate is opened and the difference between the up and down pulses $n = n_{up} - ndown$ are counted in the up down counter. Then the gate is closed and the system must be reseted to start the next conversion cycle. It can be shown that the ratio between the analog input signal I_{in} and the reference current I_{ref} is equal to:

$$\frac{I_{in}}{I_{ref}} = \frac{n_{up} - n_{down}}{n_{up} + n_{down}} = \frac{n}{N} \tag{10.39}$$

The resolution of the converter is determined by the length N of the timer circuit, while the conversion time T_c at a certain resolution N is determined by the clock frequency f_c, so

$$T_c = \frac{N}{f_c} \tag{10.40}$$

When the conversion time T_c is related to the mains frequency, then due to the integration of a full- or a multiple period of the mains frequency a very good rejection of this frequency is obtained.

10.17.1 Auto-zero circuit

In high resolution analog systems dc offset is a problem because it adds or subtracts from small input signals. To overcome the offset problem in the analog circuit part of the converter an auto-zero system is used. The basic configuration is shown in Fig. 10.26 In Fig. 10.26 the offset of the analog

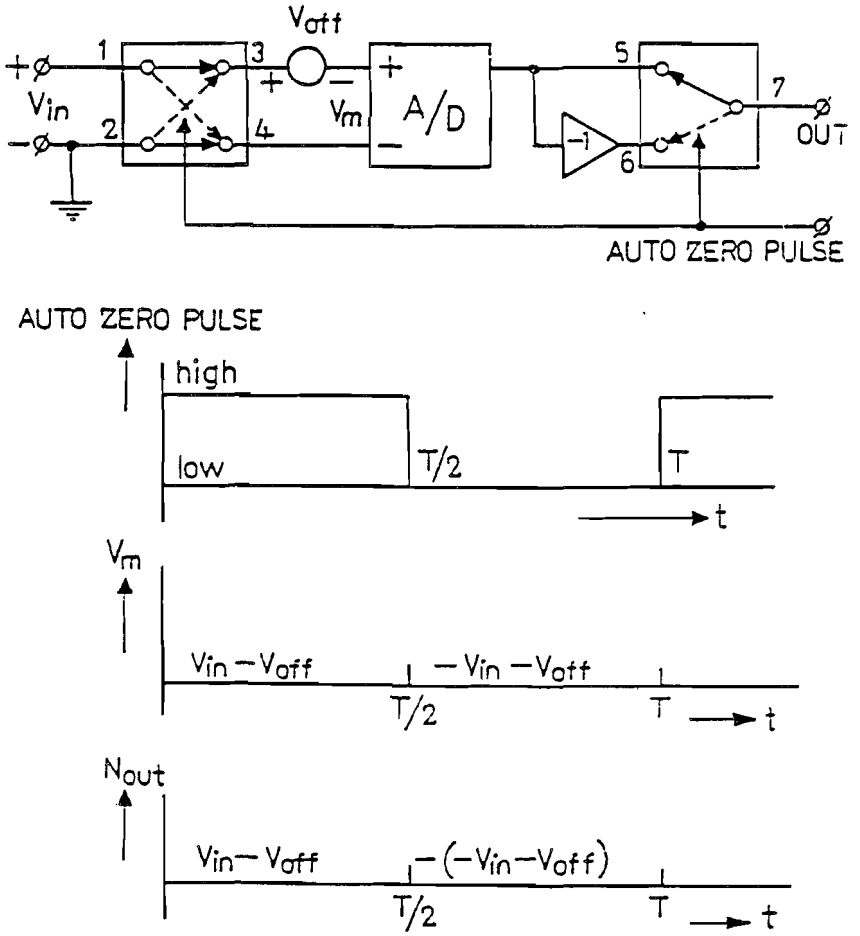

Figure 10.26 : Auto-zero system

subsystem is given by V_{off}. At the input of the system a set of switches is added. These switches invert the analog input signal with respect to the A/D converter. At the output the data pulses are inverted depending on the input switch settings. In this way the input "inversion" is removed from the

data which is applied to the counter section. The system basically operates by dividing the conversion time T_c into two equal parts $T_c/2$. During the first part of the conversion time input terminals 1 and 3 are connected as is done with 2 and 4. In the second part terminals 3 and 4 are interchanged. During the first part of the measuring time, a voltage V_{m1} equal to $V_{in} - V_{off}$ is measured. During the second half of the measuring time a voltage V_{m2} equal to $-V_{in} - V_{off}$ is converted. The difference between V_{m1} and V_{m2} must be calculated. By inserting the data inverter during the second part of the measuring time the data inversion is performed and the subtraction is transformed into an addition. An addition is very easy to implement by counting of pulses. As a result to the measured voltage is equal to:

$$V_m = \frac{1}{2}(V_{in} - V_{off} + V_{in} + V_{off}) = V_{in} \tag{10.41}$$

As can be seen from equation 10.41 the auto-zero circuit ideally cancels the offset voltage without increasing the conversion time. A second advantage of this system is that the measured values for positive and negative signals is exactly equal because there is no difference between measuring a positive signal or a negative signal according to equation 10.41 except from the sign determining algorithm.

10.17.2 Analog subsystem implementation

A simplified diagram of the analog subsystem is shown in Fig. 10.27. The systems consists of a voltage-to-current converter *V to I*, the differential PNP transistor pair T_3 and T_4 controlled by the flip flop FF, a comparator *comp*, the integration capacitor C and the reference current source I_{ref}. An additional operational amplifier *Op. Amp.* controls the current sources I_1 and I_2 in the voltage-to-current converter. The voltage-to-current converter is drawn as the differential amplifier pair T_1 and T_2 with emitter degeneration resistor R_1.

The equal charge and discharge currents are generated by the reference current I_{ref} and the differential pair T_3 and T_4. As long as the base currents are very small (MOS devices) then these charge and discharge currents are exactly equal. The operational amplifier *Op. Amp.* controls the currents I_1 and I_2 in such away that the potential of the collectors of T_2 and T_4 is at zero volt. The sigma-delta converter operation performs the same with the collector voltage of T_1 and T_3. The input system is a full differential system which is required for the auto-zero function. Digital output signals of the

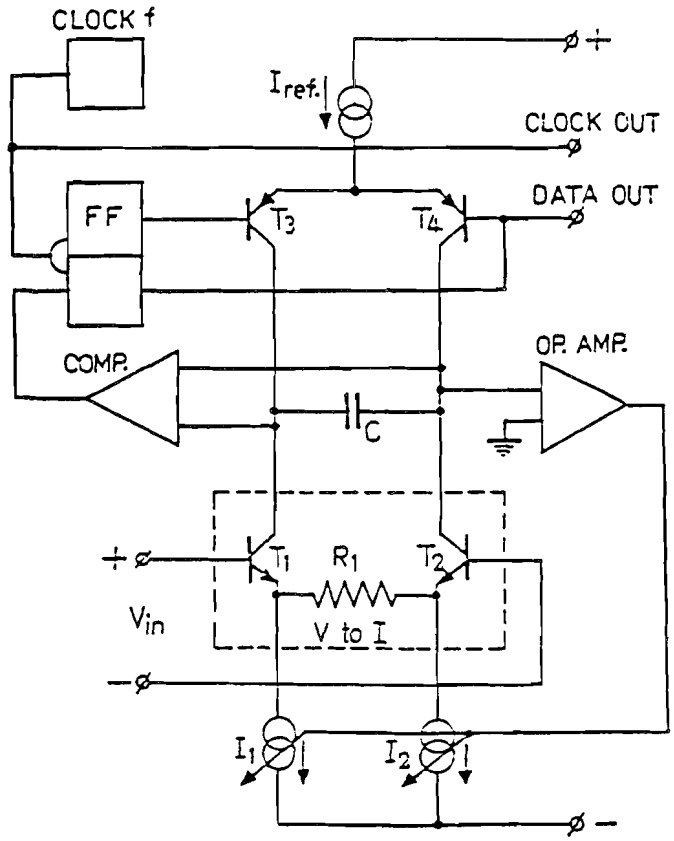

Figure 10.27 : Analog subsystem implementation

conversion section are *clock out* and *data out*. These signals are applied to the digital counting section.

10.17.3 Basic voltage-to-current converter

In Fig. 10.28 a circuit diagram of a basic voltage-to-current converter is shown. The basic voltage-to-current converter consists of the PNP input pair T_1, T_2 and two current mirrors (T_3, T_4, T_5 *and* T_6, T_7, T_8) with biasing current sources I_0. With $V_{in} = 0$, then due to the current mirror action a current I_0 must flow through T_3 and T_4 as well as through T_6 and T_7. Therefore, the currents through T_1 and T_2 are constant and have a value $2I_0$. When an input voltage is applied, this voltage is exactly reproduced across the conversion resistor R, because the voltage drops across T_1, T_3 and T_2, T_6

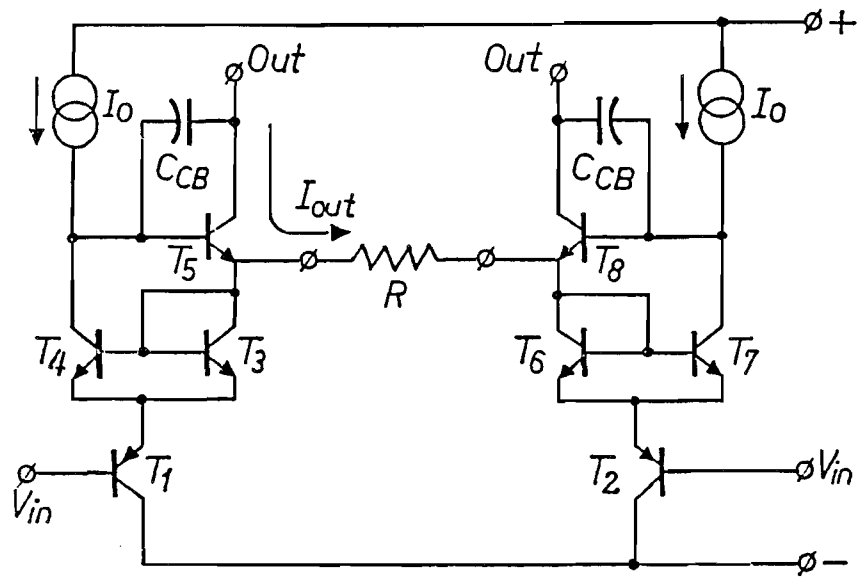

Figure 10.28 : Basic voltage-to-current converter

remain constant. As a result the converted output current I_{out} can only flow through transistors T_5 and T_8. As long as the base currents of T_5 and T_8 are small a constant current will flow through the input devices T_1, T_2 and the diodes T_3, T_6 keeping the voltage drops constant. An accurate voltage-to-current conversion is obtained with this system. In the final system a more complicated circuit based on the same system is used.

10.17.4 Complete digital voltmeter system

The complete digital voltmeter system is implemented in a CMOS digital part for control and display function and a bipolar part which contains the complete sigma-delta A/D coverter section with reference source and gain selection. In Fig. 10.29 the performance of the system is shown. The internal reference voltage is based on the bandgap principle of silicon.

10.18 Conclusion

Noise-shaping and noise-shaping coders are excellent alternatives as analog-to-digital and digital-to-analog converters for applications in digital audio,

Input voltage :	100mV and 1V (bipolar)
Resolution :	5 digits plus sign. ($f_{clock} = 200$ kHz)
Linearity :	$\pm 10^{-5}$ of F.S.
Zero stability :	$< 10^{-6}$/°C (with auto zero)
T.C. of ref. source :	$5 \cdot 10^{-6}$/°C over $\Delta T = 80$ °C
Voltage stab. of ref. source :	$5 \cdot 10^{-6}$/V
Power supply :	$\pm$ 7.5V, 27mW.

Figure 10.29 : Digital voltmeter performance data

digital video and digital voltmeter systems. The sigma-delta system needs only two, or in special configurations one reference voltage to perform the conversion. In these systems an excellent differential linearity with small signals is obtained. The noise shaping action randomizes the quantization noise rather well with small input signals improving the performance of the total conversion system. The combination of the noise shaping filter with the anti-alias function minimizes the components count and seems to be a very attractive alternative for digital audio signal conversion.

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