Polarization converter post-processing and Brillouin sensing optical functionality in generically integrated photonic circuits

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Polarization converter post-processing and Brillouin sensing optical functionality in generically integrated photonic circuits

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Manuela Felicetti

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Polarization converter post-processing and Brillouin sensing optical functionality
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To my family

Contents

Chapter 1

Introduction

Looking to the next stage of photonic integration, the aim of this work is to introduce components and functionality that are not fully supported yet in photonic integrated circuits. This thesis project demonstrates how to introduce experimental devices into complex optical circuits, realized in a standard foundry process. The project is structured in three main subjects. The first is the development of a post-processing technology that allows to test experimental devices using validated components in prefabricated integrated circuits. The second one is the design, post-processing and characterization of a specific experimental device: a new passive polarization converter in an integrated circuit, which contains structures to test the device in a polarization independent SOA configuration. The third subject is the design and characterization of a photonic integrated circuit for Brillouin sensing application.

Starting from the invention of electronic integrated circuits in Section 1.1, Section 1.2 extends the concept of integration to photonic circuits, introducing the idea of multi-project wafer runs. Section 1.3 explains the reasoning behind the development of a post-processing technology for experimental devices, i.e. the polarization con-

verter, in prefabricated photonic circuits. The converter and its relevance in photonic circuits are described in Section 1.4. The interest in designing a photonic circuit for Brillouin sensing is explained in Section 1.5. Finally, Section 1.6 gives an overview of the thesis structure.

1.1 Electronic integrated circuits

The invention of the transistor in 1947 by Shockley, Bardeen, and Brattain was the breakthrough idea that stimulated engineers to propose complex electronic circuits able to perform elaborated functions, containing hundreds or thousands of discrete components such as transistors, diodes, resistors and capacitors [1]. Years later, in a paper celebrating the 10th anniversary of the invention of the transistor, the vice president of Bell Labs, Jack Morton, stated:

> "For some time now, electronic man has known how 'in principle' to extend greatly his visual, tactile, and mental abilities through the digital transmission and processing of all kinds of information. However, all these functions suffer from what has been called 'the tyranny of numbers'. Such systems, because of their complex digital nature, require hundreds, thousands, and sometimes tens of thousands of electron devices."

The 'tyranny of numbers' problem relates to the interconnection between these components. In order to built an electronic circuit, thousands of components required hand-soldering to thousands of wires. This was expensive, time-consuming and impossible to apply on a large scale production. Moreover, every soldered joint was potentially susceptible to breakage. The challenge was to find cost-effective, reliable ways of producing these components and interconnecting them.

In the summer of 1958, Jack Kilby at Texas Instruments hit on the groundbreaking idea that started the microelectronics revolution. As a new employee he did not yet have the right to a summer vacation, so while working alone on a electronic circuits miniaturization project, he saw the solution to built smaller electrical circuits: make all the components and the chip out of the same block (monolith) of semiconductor material. When his co-workers returned from vacation, Kilby presented the first integrated circuit (IC).

Nowadays, ICs are used in computers, mobile phones, and other digital home appliances that are inextricable parts of the structure of modern society. Walking in the foot-steps of microelectronics, photonics is also moving forward with a generic integration technology to low-cost and high-volume manufacturing.

1.2 Photonic integration technology

The challenge of photonics is to integrate complex and advanced photonic functionality on a single chip, overcoming piece-by-piece constructed optical circuits. This significantly reduces the packaging costs for commercial applications. However, the fragmentation of existing fabrication technologies, where every fab develops a technology for a specific application and for a relatively small market, has delayed the breakthrough of integrated circuits. This has prevented an easy standardization and the commercial success of photonic integrated circuits (PICs) [2].

In photonics, by using a set of basic building blocks (BBs), i.e passive waveguides, semiconductor optical amplifiers, phase modulators, photo-diodes and polarization converters, we can form components such as multi-mode interferometers (MMIs), arrayed waveguide gratings (AWGs), lasers, Mach-Zehnder interferometer (MZIs). These components are used to build highly complex PICs with hundreds of basic BBs, for a broad range of functionalities from telecommunication and data communication to non-telecom applications like sensors, medical equipment and metrology.

To make this feasible a more standardized approach is needed, which is called generic integration.

1.2.1 Photonic multi project wafer (MPW) on indium phosphide material

The way to generic integration is to develop a set of BBs on a technology platform, where these basic validated BBs are used to build PICs, for a large variety of applications. PIC designs that share a technology platform can be combined on a so called multi-project wafer (MPW) and fabricated in the same processing run, thus with the possibility of cost-sharing among the platform users [3].

A number of application specific PICs (ASPICs) have been already successfully fabricated and tested on indium phosphide (InP) material. Within the JePPIX organization [4], companies like Oclaro, Fraunhofer HHI and SMART Photonics (a spinoff of the COBRA research institute) offer access to their technology platform through MPW runs. Fig. 1.1 (a) shows an MPW fabricated by Oclaro, where each cell is a PIC. The MPW is cleaved into the single PICs (Fig. 1.1 (b)) in order to be characterized by the users. These MPWs have been fabricated in a semi-commercial production. By analogy with the microelectronics integration path a significant reduction of PICs manufacturing costs is expected in the near future, leading to a promising market growth for integrated photonics. So far PICs are mainly used in telecom applications, but thanks to costs drop they will penetrate the market also through challenging applications i.e. fiber sensors, optical coherence tomography, pico and femtosecond pulse lasers.

Advanced applications can require functionalities which are not fully supported in a specific technology platform. For example, a PIC for fiber sensing can include most of the existing optical functionalities of a commercial strain and temperature analyzer, however polarization handling is still an open challenge since there is no standardized process to include a polarization converter, the basic BB which allows for this functionality, in a PIC during an MPW run.

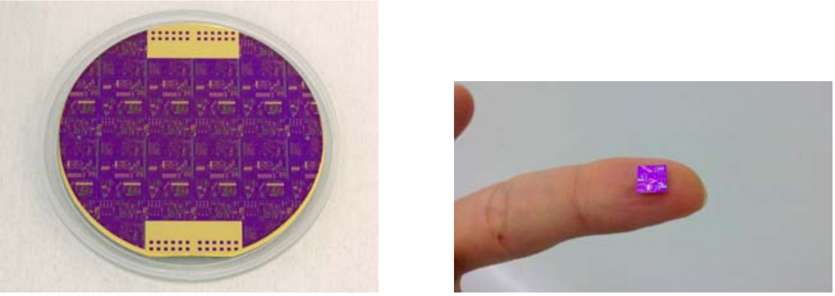
(a) (b)

Figure 1.1: (a) Oclaro InP MPW which contains PICs of different users. (b) InP-based photonic integrated circuit cleaved from the MPW.

1.3 Post-processing of experimental devices

The way to obtain a validated and reliable BB is through the interplay between design, fabrication and testing. Usually during an MPW run, one of the wafer cells is dedicated to test structures, in order to characterize single components for a better understanding of a complex circuit. Not all the BBs can be realized as part of the circuit of an MPW PIC, because for some of them the processing is not yet integrated in the foundry standardized technology. To overcome the limit of PIC design capabilities and include advanced functionalities, there is a need to add such experimental BBs to the MPW PICs after their realizations . Thus, an MPW run can be used as well to test these experimental devices (EDs), not integrated yet in a generic technology platform, exploiting validated BBs contained in prefabricated PICs.

The first part of this project is dedicated to develop a post-processing technology to add EDs in prefabricated PICs. The required post processing technology has two main issues:

1. The PIC-ED connection.

2. The protection of the PIC during the processing of the ED.

A post-processing technology has been developed in this thesis project to interconnect an ED to a prefabricated PIC, while protecting the existing circuit. In the second part of this work, the post-processing technique is applied to the fabrication of a polarization converter, which has not been integrated yet in a generic technology platform, in a prefabricated PIC containing structures to test the device in a polarization independent SOA configuration.

1.4 Polarization converter

Modern telecommunication networks are evolving to support high speed services, which require the use of fiber optic systems. When an optical signal travels in an ordinary fiber, it experiences polarization mode dispersion due to random manufacturing imperfections or thermal and mechanical stresses of the fiber itself. In this case the different polarized modes of the optical signal travel with different propagation constants, causing pulses to spread and overlap. Hence the transmission in the optical fiber degrades. This effect can be mitigated with polarization manipulation, e.g. with an integrated optical circuits. On the other hand, integrated optical circuits should operate independently from the polarization state of the fiber output signal, especially if they are used as add and drop multiplexers, detectors or cross connects [5]. However many circuit components, such as semiconductor optical amplifiers (SOAs) and phase shifters, are usually polarization dependent. There are two strategies to overcome this problem. One is to realize polarization-independent devices; the other one is to manipulate the polarization using devices such as polarization scramblers, splitters and controllers. The first solution brings strict limitations to both the design and the fabrication; hence the second approach is more feasible. In all the polarization handling devices a polarization converter (PC) is present, thus the PC is an essential building block in an integrated optical circuit [6].

A PC rotates the polarization of linearly polarized light by a 90° angle, enabling transfer of optical power between the two polarized modes. Polarization converters are classified as active if the polarization is manipulated by an external signal. Active PCs are based on acousto-optic or electro-optic effects. They are usually fabricated in $LiNbO_3$ [7, 8]. If no external control is required, the converters are defined as passive. Passive PCs can be obtained with geometrical changes of the optical waveguide, such that the incoming transverse electric (TE) (or the transverse magnetic (TM)) mode excites two tilted orthogonal modes that propagate with different propagation constants. By combining these tilted modes with an appropriate phase difference, polarization conversion is obtained. Our purpose is to develop a technology for a PC compatible with the Oclaro foundry process for InP-based PICs. For this reason a passive PC is more suitable, since the electro-optic and acousto-optic effects in InP are quite small.

A number of passive PCs have previously been developed in InGaAsP/InP material. In [9, 10] polarization conversion is obtained with an asymmetric periodic loaded rib waveguide; a PC based on ultra short bends is presented in [11]. Another class of PCs is fabricated with a single section waveguide [**?**]. In this case the mode conversion is obtained by wet etching a slanted wall on one side of the waveguide. The single section PCs are the shortest, thus they are the most promising to be integrated in photonic circuits. However, higher fabrication tolerances and a wider wavelength range than the single section converter can provide are essential for telecommunication applications. This leads to the necessity of a PC device which is tolerant against geometrical deviations together with a process-flow that has a low impact on the PC's most sensitive features.

In the second part of this work a new concept for the PC is proposed, using waveguide with a triangular top cladding. This PC shape is innovative compared to the standard sidewall slope approch presentent for exaple in [12, 13] for COBRA and HHI platforms respectively, and it requires a simplified fabrication technology. First, the performance of a single section PC is evaluated, then a double section PC with two mirrored cross sections is proposed to increase the device fabrication tolerance and operational wavelength range. The PC is post-processed in a PIC and demonstrated in a polarization independent SOA (PI-SOA) configuration.

1.5 Polarization independent SOA

An essential component for all-optical networking is the Semiconductor Optical Amplifier (SOA). In addition to providing amplification, it can also be used for switching/gating and for non-linear functions. An example of the latter is a wavelength converter [14]. For SOAs to operate in a fibre optic network, polarization independence is a prerequisite. Since SOAs are planar devices, often making use of quantum wells or quantum dots as an active medium, TE and TM polarized light usually experience different gains. Furthermore, the use of SOAs in switches and wavelength converters is compromised, since the phase shift and the non-linear response are also polarization dependent. In order to obtain a low Polarization Dependent Gain (PDG), a number of different approaches have been followed. The most common way to reduce PDG is to apply a specific amount of strain to the materials [15]. In this way

PDG in the range of 0.3 dB to 1 dB has been obtained. This technique can however be difficult, and in some cases even impossible, to apply[16]. It also frequently results in compromise with respect to optimal performance of the SOA, since one degree of freedom in the design has to be sacrificed. In this approach the refractive index, and consequently the phase transfer and the non-linear response, are not independent of polarization, implying that this is not a suitable solution for the use of SOA in switches. An alternative method is the use of on-chip polarization handling. In [17] a device is presented which uses an averaging solution. The polarization is converted halfway between two SOA sections and hence the polarization properties are averaged out over the two polarization states. This approach avoids the disadvantages of the strain compensation technique mention above. Using a polarization converter not only eliminates the PDG, it also compensates polarization effects in phase shift and non-linear effects (like SPM or XPM). This compensation is obtained without limiting the design options for the SOA. The performance reported in [17] was however not very good, with a PDG of several dB across the whole C-band. The reason for this was the low polarization conversion in the device.

In this thesis we describe how such a polarization converter can be integrated within an optical circuit fabricated on a standard generic PIC process platform using a post-processing technique. With this integration step a polarization independent SOA is obtained.

1.6 Brillouin optical time domain reflectometry (BOTDR) read out unit

One of the application areas that photonic integration can support is fiber sensing. In recent years, the interest in the monitoring of large-scale constructions has significantly increased. Therefore, fiber-based optical techniques have been developed for remote sensing. By using the Brillouin scattering in a standard single-mode fiber, it is even possible to use the fiber itself as a sensing medium. In this way strain and temperature distributions along the fiber can be determined [18] on a length range from few meters up to 100 km. Detecting structural failures, before they become visible to an outside inspection, can prevent collapse of buildings and other civil infrastructures [19]. Brillouin optical time domain reflectometer (BOTDR) systems have been around for several decades and have evolved into systems such as Brillouin optical time domain analysis (BOTDA) [20], which accesses the measuring fiber from both ends to achieve better accuracy, double-pulse BOTDR [21], and pulse-prepump BOTDA [22] to improve spatial resolution. However, all these systems have not received the same success as, e.g., systems with fiber-based Bragg gratings. The reason for this is that the optical circuitry needed for BOTDR systems is more complex and, therefore, relatively expensive. The emergence of MPW runs in the field of photonic integration could change this picture. As explained in Section 1.2, by sharing the costs of a mass production facility over many market applications, relatively cheap PICs can be obtained that could replace much more expensive piece-by-piece constructed optical systems. The third part of this project introduces the design of a photonic integrated circuit (PIC)[1] capable of providing the basic optical functionality needed for BOTDR systems.

It is important to mention that, since the Brillouin signal travels in a standard single mode optical fiber, its polarization state varies on a time scale of few milliseconds. This causes power fluctuations at the coherent receiver which is detecting only one polarization. The PC device, presented in this work, can be exploited to overcome this BOTDR limitation.

1.7 Thesis outline

This project is structured in three main subjects:

1. development of a post-processing technology that allows to test experimental devices using validated components in prefabricated PICs.
2. design, post-processing and characterization of a new passive polarization converter in a PIC.
3. design and characterization of a PIC for Brillouin sensing application.

It became clear, however, that in the long term these subjects could merge, as the performance of the Brillouin circuit is polarization dependent. This could be remedied with inclusion of polarization handling devices in the circuit.

The structure of the thesis is summarized in the following paragraphs:

Chapter 2 presents the design and simulation of a passive polarization converter (PC), optimized for the Oclaro technology platform, with a complete analysis of the fabrication tolerances. To overcome the limits of the fabrication of the first generation PC, a second generation PC is presented together with a tolerant version,

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[1] Both the PIC for the PC testing and the BOTDR circuit have been realized within an MPW run fabricated at Oclaro [23], following the foundry rules described in the Oclaro design manual and implemented in the Photonic Design Kit (PDK) developed in the European project EuroPIC [24].

which consist of two mirrored sections. Then, the working principle of a polarization independent SOA test structure, obtained by placing a passive PC half-way two identical SOAs is described.

Chapter 3 focuses on the solution adopted to connect an experimental device (ED) to the existing structures of a pre-fabricated PIC and on the technology developed to protect the PIC, during the post-processing. Design, simulation and measurements of the taper connections, that interface devices processed with two different technologies, are presented.

In **Chapter 4**, we report the fabrication technology and measurement results of the polarization converter (PC) device, post-processed in an Oclaro PIC containing structures to test the PC in a polarization independent SOA configuration. The first and second generation PC process-flows together with processing issues and measurement results are presented.

Chapter 5 presents a Brillouin Optical Time Domain Reflectometry (BOTDR) read-out unit whose optical components are integrated in a photonic circuit. The circuit design and working principle are described. The measurements of the optical test structures is reported together with the characterization of the BOTDR circuit pulse generation when the circuit is set to one of its operational modes.

Finally, in **Chapter 6** the main achievements of the thesis project are summarized. Recommendations and outlook are given as well on a future technology development of the PC fabrication and design improvements of the BOTDR circuit, including polarization handling functionality.

Chapter 2

Polarization converter and PI-SOA design

This chapter presents the design and simulation of a passive polarization converter (PC), compatible with the Oclaro platform, and the polarization independent SOA (PI-SOA) concept and design. Such a device is not yet available for that platform. Here a new concept for the PC is proposed, using waveguide with a triangular top cladding. This PC shape is innovative compared to the standard sidewall slope approch presented for exaple in [12, 13] for COBRA and HHI platforms respectively, and it requires a simplified fabrication technology. First, the performance of a single section PC is evaluated, then a double section PC with two mirrored cross sections is proposed to increase the device fabrication tolerance and operational wavelength range. A first generation technology is developed to fabricate the single section PC. Then, a second generation technology with a completely self-aligned process is developed to overcome the limits of the first one, above all in order to keep the symmetry between the two sections of the double converter to ensure its performance. The PC *device is developed to obtain polarization independent SOAs. In Section 2.1 the PC working principle is explained together with the parameters that characterize the performance. Section 2.2 introduces the first generation single section PC with a complete analysis of the fabrication tolerance. In Section 2.3 the second generation PC is presented together with a tolerant version, which consist of two mirrored sections, to overcome the fabrication limits of the single section PC. Section 2.4 describes a polarization independent SOA test structure, obtained by placing a passive PC in between two identical SOAs. Conclusions are drawn in Section 2.5. The technology for experimental device post-processing, to realize a PC in a photonic integrated circuit, will be presented in Chapter 3, while the process-flow of the first and second generation PC together with the measurement results will be treated in Chapter 4.*

2.1 PC working principle

A single section passive PC is an optical waveguide with an asymmetric cross-section, connected to straight input-output waveguides. Fig. 2.1 shows a passive PC with a slanted top cladding, which tilts the modes of the waveguide by a certain angle.

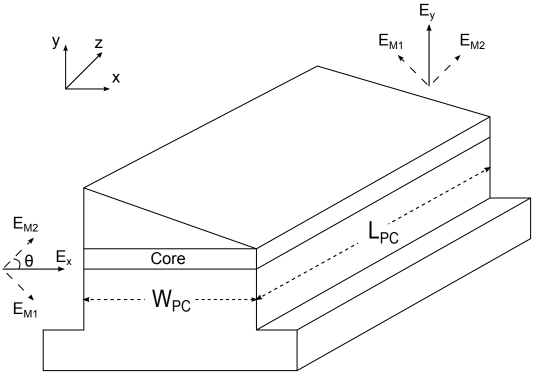

Figure 2.1: Single section passive PC with a sloped sidewall.

The PC acts as a birefringent optical device with a fast optical axis and a slow optical axis. These are respectively polarized parallel and perpendicular to the main axis of anisotropy[1]. The field component that oscillates along the fast axis is the ordinary light wave whilst the component that oscillates along the slow axis is the extraordinary wave. These two components, which are the modes in the waveguide, propagate along the structure with different propagation constants. The two axes should be oriented at 45° with respect to the substrate surface in order to obtain full polarization conversion. Suppose that a TE polarized mode, coming from a straight waveguide, is coupled to a PC waveguide. The TE vector can be represented with the two orthogonal mode field components M_1 and M_2 that are -45° and +45° rotated with respect to the TE vector. The PC waveguide geometry should be such that these angles are obtained, so that the incoming TE mode can excite the two modes M_1 and M_2 equally in power. If this happens the two modes start to propagate in the PC with two different propagation constants. After a half beat length

$$L_{PC} = \frac{\pi}{\beta_1 - \beta_2} \tag{2.1}$$

---

[1] The anisotropy is not the result of the crystal structure, but is created by the waveguide geometry.

with β_n $(n = 1,2)$ the propagation constant of the mode M_n, M_1 is shifted by a phase angle of π with respect to M_2; thus the two modes recombine into the TM mode in the straight output waveguide [12]. By changing the width and the slope angle of the converter, the tilt angle of the modes changes by the relation

$$\theta = arctan\left(\frac{E_{M_1}}{E_{M_2}}\right) \tag{2.2}$$

where E_{M_n} is the electric field of the mode M_n excited by the TE mode.

The PC slope can be chemically etched with HCl, which gives a 36° angle due to the crystallographic properties of InP. The width is optimized to have -45° and +45° tilted modes and the length equal to L_{PC} to obtain TE to TM conversion.

A polarization converter can be characterized by two parameters: the conversion efficiency, C, and the coupling loss, $Loss$. The conversion of the PC is the ratio between the converted power and the total power at the output of the converter:

$$C = \frac{P_{converted_{out}}}{P_{total_{out}}} \tag{2.3}$$

where $P_{converted_{out}} = P_{TE_{out}}$ if the mode at the input of the PC waveguide is TM, whilst $P_{converted_{out}} = P_{TM_{out}}$ if the input mode is TE. The total output power is $P_{total_{out}} = P_{TE_{out}} + P_{TM_{out}}$.

The insertion loss is the ratio in dB between the total output power and the input power:

$$Loss[dB] = 10log_{10}\left(\frac{P_{total_{out}}}{P_{in}}\right) \tag{2.4}$$

with $P_{total_{out}} = P_{TE_{out}} + P_{TM_{out}}$ and $P_{in} = P_{TE}$ or $P_{in} = P_{TM}$, depending on the input polarization.

In the next section, the design of a single section passive PC is presented together with the device tolerance analysis.

2.2 First generation PC design and simulations

To model the polarization converter, the waveguide cross-section is defined in FIMMWAVE, which is a waveguide mode solver. The PC layer stack is the same one used for the Oclaro passive waveguide (Fig. 2.2). A refractive index is assigned to each material according to the foundry specification for the substrate, the core, and the top cladding (Tab. 2.1). For the core layer, which contains a number of sub layers, two different refractive indices are assigned for TE and the TM modes respectively.

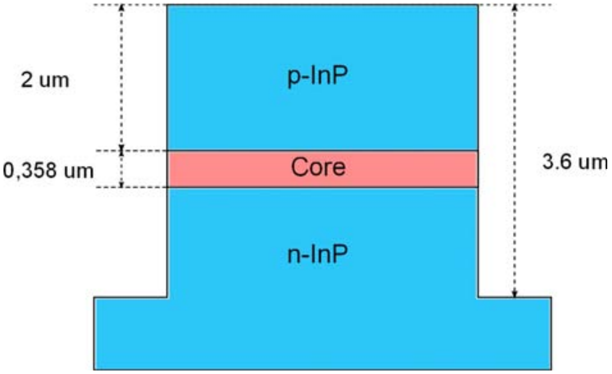

Figure 2.2: Oclaro waveguide cross-section.

	p-InP	n-InP	Core (TE)	Core (TM)
Refractive index	3.173	3.163	3.383	3.378

Table 2.1: Oclaro layer stack refractive indices for λ=1550 nm.

The performance of different PC shapes have been compared; each asymmetrical PC cross-section requires a different technological approach:

- HCl wet etching: a slanted PC sidewall can be obtained by selectively etching the top-cladding InP. The etching stops at the interface with the guiding layer, and the slope has a 36^o angle with respect to the (001) plane, i.e. the substrate surface. This is the device shown in Fig. 2.1.
- Br_2- methanol: this solution etches a sloped sidewall through all semiconductor layers at an angle of 54^o with respect to the (001) plane (Fig. 2.3(a)).
- Dry RIE or ICP InP etching: a staircase profile can be obtained by subsequently etching portions of the top cladding (Fig. 2.3(b)).

The choice of the PC cross-section is a trade off between dimensions, performance and fabrication feasibility. The above mentioned methods can be used to fabricate PCs that are suitable for our purpose, with a conversion efficiency above 99% for $\lambda =$ 1550 nm and a length between 130-250 µm. HCl-based wet etching has been chosen to limit the number of critical processing steps, reducing the risk of deviation from the geometrical parameters of the simulated structure. The details of the fabrication processing will be discussed in Chapter 4.

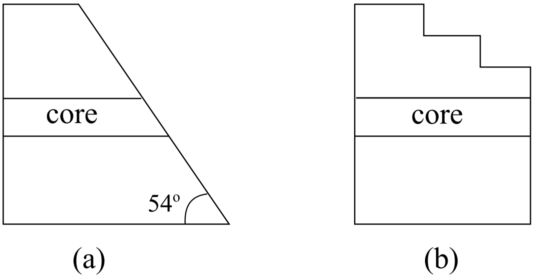

Figure 2.3: Asymmetrical PC cross sections obtained with (a) Br_2- methanol and (b) dry InP etching.

With the film mode matching (FMM) solver[2], the two fundamental modes are determined. The simulation returns the fractional TE-power in percentage of the two modes and the propagation constants.

The first parameter that we choose is the PC waveguide etch depth; to ensure insensitivity of the modes to the etch depth, an etching deeper than 600 nm below the core layer is required. Since the core thickness is a fixed parameter and the slope angle is defined by the selective wet etching, the PC width is the only variable to be optimized in the cross-sectional analysis, in order to obtain the two modes M_1 and M_2 with 45°. A scan of the PC width is performed to find the optimal value that gives a 50 % TE power splitting between the two orthogonal modes. This optimal PC width is 1.11 μm and the PC length is calculated using (eq.1). We analyzed the modes of the input (output) waveguide cross-section as well, starting with a waveguide width equal to the PC width.

Using the modes of the PC and the input/output waveguides, a full device is simulated with the propagation module FIMMPROP in order to calculate the propagated field. The PC device consists of 50 μm long input-output waveguides, and a 139.4 μm long PC section; the waveguides and PC cross-section are perfectly aligned. The PC device has a calculated conversion efficiency C=99.99% and total insertion loss of -0.48 dB (λ=1550 nm). The simulation enables us to analyze the tolerances of the PC device with respect to: width variations, length variations, alignment offset with input-output waveguides, input-output waveguides width variation, and wave-

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[2] FIMMWAVE and FIMPROP have been used for the simulations [25]

length variation. The target that we choose for the polarization conversion is $C > 95\%$. The polarization of the input mode has been set to TE. However, since the PC is a reciprocal device, TM input will lead to the same results.

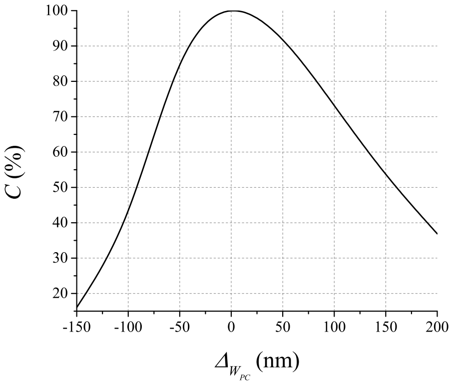


Figure 2.4: Conversion efficiency C (%) as a function of the PC width W_{PC} variation, $\Delta_{W_{PC}}$ (nm).

PC width and length variation

The polarization converter width W_{PC} and length L_{PC} , for the first generation PC, are defined by EBL (see Section 4.2.1). This analysis takes into account width and length deviations from the optimal values of W_{PC}=1.11 µm and L_{PC}=139.4 that can occur during the EBL exposure. The graph of the conversion efficiency C as a function of the PC width W_{PC} variation $\Delta_{W_{PC}}$ (Fig. 2.4) shows that the conversion efficiency drops about 10% for $\Delta_{W_{PC}}$= - 40 nm or $\Delta_{W_{PC}}$= 53 nm. This means that the device performance is quite sensitive to width variations[3], raising the necessity to improve the device tolerance.

The length variation analysis is shown in Fig. 2.5. The length dependence of the PC conversion efficiency (Fig. 2.5(a)) follows the law [5]:

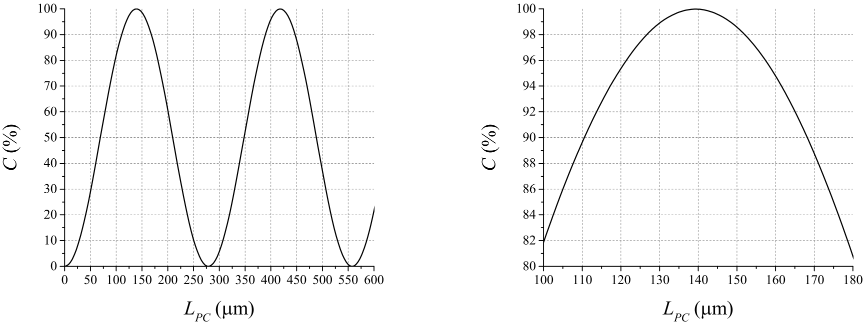
$$C(L_{PC}) = sin^2\left(\frac{\pi}{278.8}L_{PC}\right) \tag{2.5}$$

where L_{PC} is measured in µm (Fig. 2.5(a)). A zoom in (Fig. 2.5(b)) of the previous

---

[3] The alignment accuracy of EBL can be as good as 10 nm. However, the first generation PC (Section 4.2) can lead to a worse alignment (see section alignment offset').

graph shows that the conversion efficiency stays above 95% for a length variation of ±20 µm, thus the PC length is not a critical parameter to control.



(a) (b)

Figure 2.5: (a) Conversion factor C (%) as a function of the PC length L_{PC} (µm). (b) Zoom in.

Input and output waveguides width variation

This analysis has been performed by keeping the PC straight sidewall aligned with one sidewall of the input-output waveguides (Fig. 2.6). Fig. 2.7 (a) shows that C is maximum when W_{WG} = 1.3 µm, but the variation in C is in the order of 10^{-4} in a width range of 1-1.5 µm. For this reason we also look at the insertion *Loss* (Fig. 2.7 (b)). A width W_{WG} = 1.05 µm has been chosen for the design, that gives -0.48 dB insertion loss. The target is to have *Loss*< -1 dB, so a W_{WG} between 1 µm and 1.25 µm is acceptable.

Offset between input-output waveguide and PC

The offset that we consider is the variation of the position of the input and output waveguide cross-section with respect to the PC waveguide, where $Offset = 0$ (nm) is when the PC and the waveguide are aligned on one side, as in Fig. 2.6. Also in this case the variation of C is not relevant (Fig. 2.8 (a)), whilst the insertion *Loss* is minimum when the offset is kept to 0 (Fig. 2.8 (b)). Since in both the first and the second generation PC processing, the straight PC sidewall and the waveguides are etched together (see Chapter 4), this parameter is very easy to control.

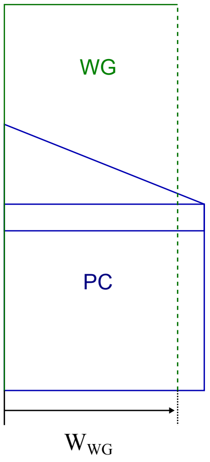
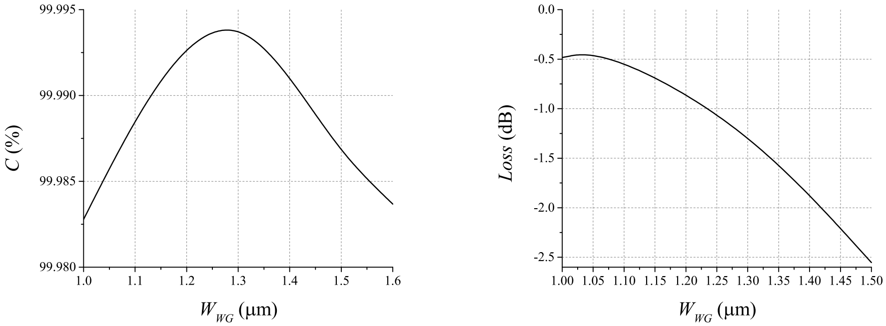
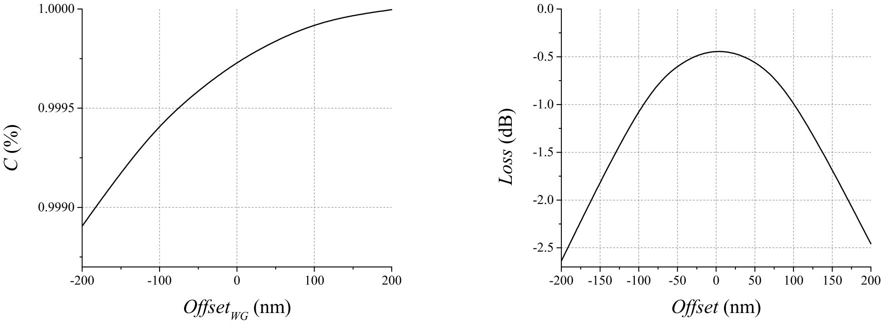


Figure 2.6: Cross-sectional schematic of the input waveguide width W_{WG} variation with respect to the PC width.



(a) (b)

Figure 2.7: (a) Conversion factor C (%) and (b) insertion $Loss$ (dB) as a function of the input and output waveguides width W_{WG} (µm).



(a)

(b)

Figure 2.8: (a) Conversion factor C (%) and (b) insertion *Loss* (dB) as a function of the alignment offset (nm) between the PC and input and output waveguides.

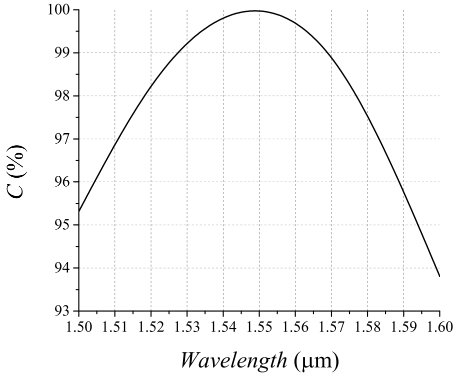


Figure 2.9: Conversion efficiency C (%) as a function of the wavelength (nm).

Wavelength dependence

The graph of the conversion efficiency *C* as a function of the wavelength (Fig. 2.9) shows the good performance of the PC device, with a conversion above 99% over the C-band (1530–1565 nm)[4]. The insertion loss are below -0.5 dB over the C band.

Alignment offset

It is crucial to investigate the tolerance of the PC device in terms of waveguide alignment during the EBL exposure. In the first generation processing, the PC is exposed together with input and output waveguides and the pattern is aligned to the substrate with respect to the slope. (Fig. 2.10) shows a top view scheme of the waveguides (WG) and PC pattern aligned on top of the substrate[5]; the core layer is represented in red. One side of the PC waveguide pattern has to coincide with the slope-core interface. The details of the processing will be discussed in Section 4.2.1. Due to variation of the top cladding thickness (±10%) in different wafers, the position of the PC and waveguide pattern could deviate from the one calculated in the case of a 2 μm thick top cladding, specified by the foundry. We define as a positive offset the one shown in Fig. 2.11 (a), whilst Fig. 2.11 (b) shows a negative offset. In case of a positive offset, the PC cross-section will result in a waveguide whose slope is laterally cut above the guiding layer, whilst in case of a negative offset, the slope ends at the cladding-core interface with the formation of a plateau.

Fig. 2.12 shows the conversion efficiency *C* as a function of the EBL alignment offset (nm). If we consider a top cladding thickness variation of ±2% (40 nm), the projection on the substrate is around 55 nm, due to the 36° angle, which leads to a conversion efficiency close to 90%. For a top-cladding variation of ±5% (100 nm), *C* drops to 50% and it drastically decreases below 20% for a variation of ±10%. Measuring the actual top cladding thickness before the processing can partly prevent the alignment offset.

2.3 Second generation PC design and simulations

Even though the first generation processing requires only a small number of steps, the fabrication tolerances can be certainly improved, especially with respect to geometrical deviations from the simulated device. As it has been reported in [26], a double

---

[4] The TE and TM refractive indices are wavelength dependent. Since the variation of the refractive index, for both TE or TM, is less than 0.01% over the C band, it can be neglected

[5] Note that in reality the waveguides trenches pattern is exposed during EBL

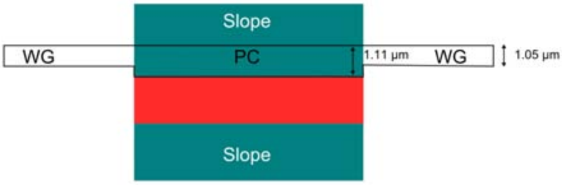
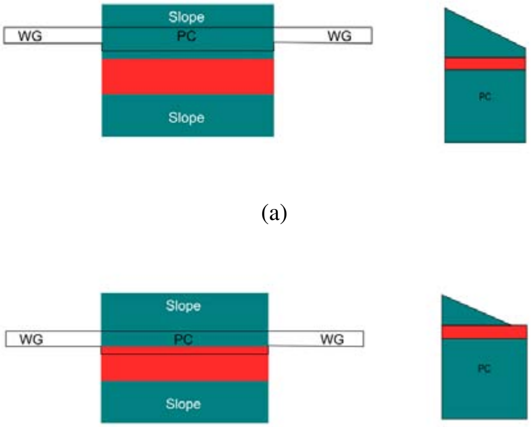


Figure 2.10: PC and waveguides alignment with respect to the slope.



(a)

(b)

Figure 2.11: (a) Positive offset (left) and PC cross-section (left). (b) Negative offset (left) and PC cross-section (left)

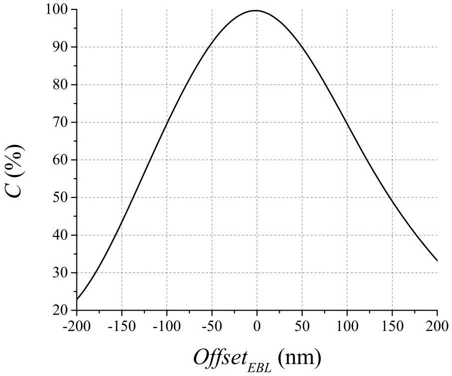


Figure 2.12: Conversion efficiency C (%) as a function of the alignment offset (nm).

section converter can overcome the limited tolerances in fabrication of the single section converter, which are mainly due to errors in the tilt angle of the PC modes. The tolerant device consists of two PC waveguide sections, whose cross sections are mirrored with respect to each other. In this configuration, the two orthogonal modes M_1 and M_2 lead to tilting angles with opposite sign in each section. If the first section has a length of $L_{\lambda\setminus 4} = \pi \setminus 2\,(\beta_1 - \beta_2)$, the phase angle shift between the two modes is equal to $\pi \setminus 2$; a second mirrored section with a length of $L_{3\lambda\setminus 4} = 3\pi \setminus 2\,(\beta_1 - \beta_2)$, has a $-3\pi \setminus 2$ phase shift between the modes, that can be considered as $\pi \setminus 2$ phase shift, so equal in magnitude to the phase shift in the first section. If any error occurs on the tilt angle in the first section, this will be opposite in the second one so on average the tilt angle of 45° will be maintained in the full PC device. The total length of the double section PC is twice the length of the single section device. A waveguide with a rectangular cross section (Bridge) is designed between the two sections to better control the etchant during the angled side-wall etch, as will be discussed in Section 4.3.2. Fig. 2.13 shows a schematic of the double section PC with the bridge connection. Fig. 2.14 shows the conversion efficiency C as a function of the Bridge length; a waveguide section with the same width as the PC and a length of 5 μm has been chosen in the design, which will give a conversion efficiency well above 99%.

An important issue is to keep the mirror symmetry between the two sections. In this case, with the first generation process-flow an alignment offset leads to two different PC cross-sections, decreasing the effect of the tilt angle error compensation between the two sections. This limitation of the first generation PC processing

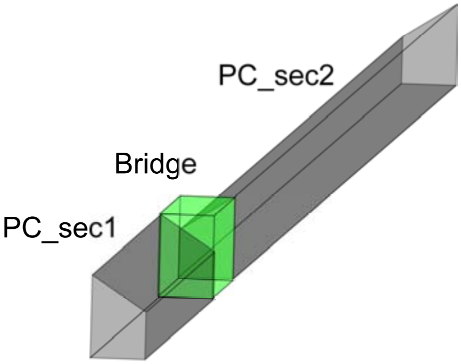


Figure 2.13: Double section PC with bridge connection.

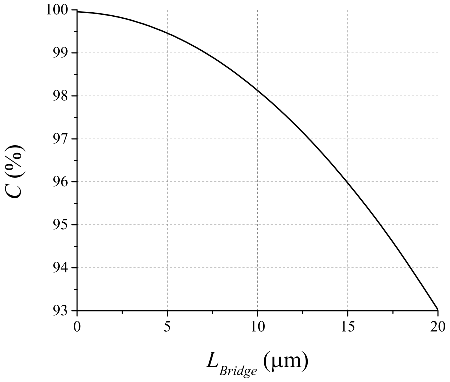


Figure 2.14: Conversion efficiency C (%) as a function of the Bridge length L_{Bridge} (µm), which connects the two PC sections.

has been overcome by making the PC waveguide etching independent from the EBL alignment. In the second generation PC process flow, a self-aligned process is developed, that will be explained in Section 4.3. The new process development leads to a double section PC, whose mirrored sections are always symmetric.

The InP RIE process, used to etch one of the PC sidewalls in the new process, creates two different angles for the core (α_1=11°) and substrate layer (α_2=3°) (Fig.2.15) because of the different etching rate of the materials. The mask erosion is constant, but since the core layer etches slower than InP, the slope on the latter is steeper. his new PC cross-section is 1.05 µm wide and gives a shorter single section PC with a length of 96 µm and a double section PC with a total length of 192 µm. The simulated conversion efficiency is 99.99% and the insertion loss -0.5 dB for λ=1550 nm. Fig.2.16 shows the comparison between the single section PC and the double section PC (2PC) performance in terms of PC width variation tolerance and wavelength dependence. The 2PC shows a doubled width tolerance range for more than 95% conversion efficiency, and a conversion efficiency above 99% over the whole C-band.

2.4 Integration with polarization independent SOA test structures

The first and second generation PCs have been post-processed in an Oclaro chip that contains structures to test the device in a polarization independent SOA configuration (PI-SOA). The first generation PI-SOA consists only of single section PCs, whilst in the second generation PI-SOA the single and the double section PC have been both fabricated and compared in terms of performance.

A polarization independent SOA can be obtained by placing a passive PC between two identical SOAs. The circuit working principle does not depend on the specific gain of TE and TM (which do depend on the band structure and the wavelength), but on an averaging effect. Suppose that a TE polarized mode is injected at the input of the circuit; if the PC gives a full conversion ($C = 1$) from TE to TM and viceversa, the output power is:

$$P_{out} = G(TE)G(TM)P_{in} \tag{2.6}$$

with $G(TE)$ and $G(TM)$ the gain of the SOA in the TE and TM case respectively (Fig.2.17). If a TM polarized mode is injected at the input of the circuit, the output power is:

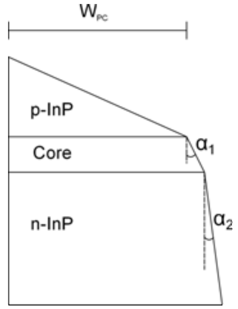
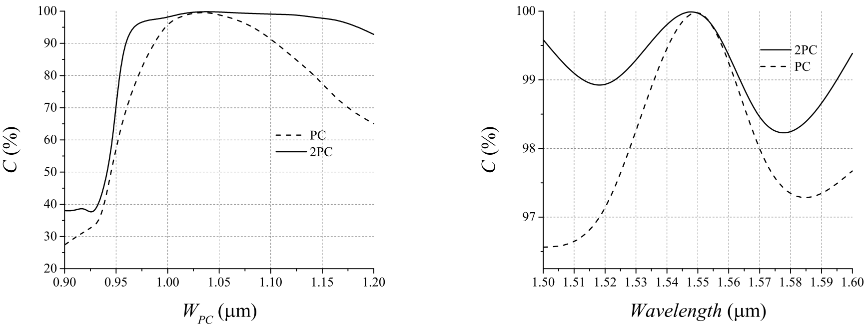


Figure 2.15: Second generation PC cross-section. α_1 and α_2 are the sidewall angles of the core and substrate layer respectively.



(a)

(b)

Figure 2.16: (a) Conversion factor C (%) as a function of the PC width W_{PC} (µm) for the single section PC and the double section PC (2PC). (b) Conversion factor C (%) as a function of the the wavelength (µm) for the single section PC and the double section PC (2PC).

$$P_{out} = G(TM)G(TE)P_{in} \tag{2.7}$$

Thus, by using a full conversion PC, the circuit gives a signal amplification independent of the input polarization (i.e., assuming that the SOAs are not in saturation). If $C < 1$, the output power is:

$$P_{out} = CG(TE)G(TM)P_{in} + (1-C)G(TE)^2 P_{in} \tag{2.8}$$

if the input mode is TE, whilst the output power is:

$$P_{out} = CG(TE)G(TM)P_{in} + (1-C)G(TM)^2 P_{in} \tag{2.9}$$

if the input mode is TM. Thus, in this case, the output power depends on the input polarization (Fig. 2.18). From the polarization dependent gain, the value of the conversion efficiency C can be obtained if the two SOAs are assumed to be identical.

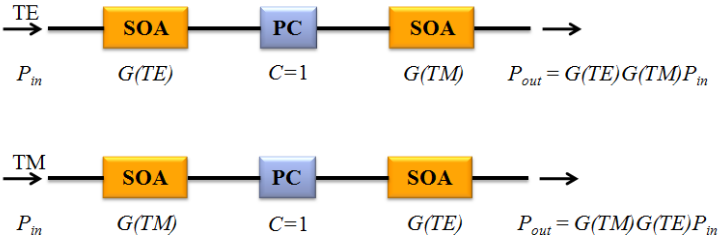


Figure 2.17: PI-SOA schematic in the case of a PC with conversion efficiency $C = 1$.

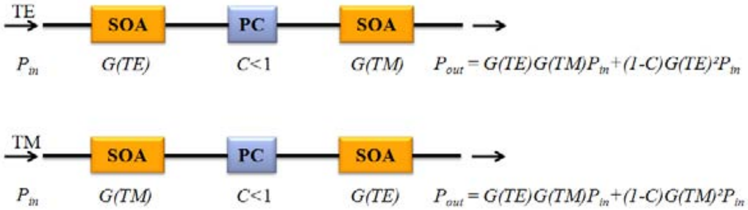


Figure 2.18: PI-SOA schematic in the case of a PC with conversion efficiency $C < 1$.

2.4.1 PI-SOA Design

A chip containing several PI-SOA structures, to test the PC, has been designed and fabricated within an InP MPW run. The test structures consist of passive waveguides (straight, curved and tapered), formed by etching 4 µm deep trenches on both sides, and SOAs (Fig. 2.19(a)); an unprocessed space of 500 µm is left in order to fabricate the PC together with input and output waveguides and connecting tapers (Fig. 2.19(b)). The Oclaro SOA building block (BB) is based on a single mode passive weak waveguide. This weak waveguide is obtained using a wet etch stop scheme, hence the process depends on the crystal orientation. The weak waveguide and the SOA are defined in a direction perpendicular to the major flat of the wafer in order to obtain straight sidewalls [24]. The sloped sidewall of the PC is also obtained with wet etch, and the PC is defined in a direction parallel to the major flat. The post-process technology that has been developed to protect the PIC structures and to connect them to the PC, will be explained in Chapter 3.

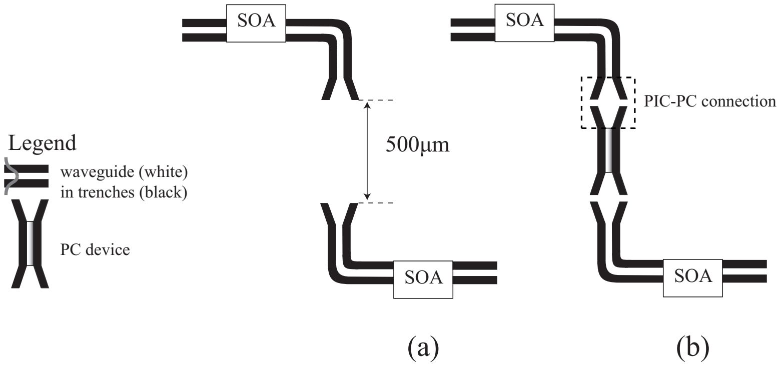


Figure 2.19: (a) PI-SOA test structure. (b) PI-SOA with the insertion of a PC.

The chip is 4x4 mm and it includes:

- 3 PI-SOA test structures with two 500 µm long SOAs each
- 4 PI-SOA test structures with 300 µm long SOAs each
- a PC test structure with one 500 µm long SOA.
- a test structure with two 300 µm long SOAs
- 3 structures with bends and 3 straight waveguides to test the taper connections.

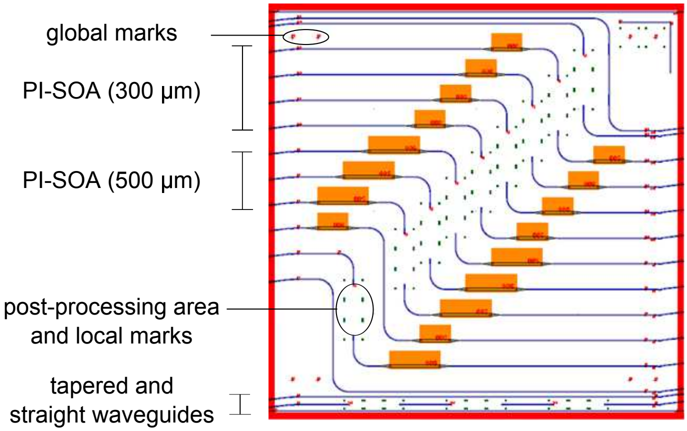


Figure 2.20: PI-SOA chip mask design.

The repetition of the test structures allows for varying the parameters of the single section PC in the first PI-SOA generation, whilst in the second PI-SOA generation both the single and the double section PC can be tested.

The local marks allow the EBL alignment for the PC processing between the Oclaro structures, while the global marks are used both for EBL and photolithography alignment. The details of the fabrication process will be discussed in Chapter 4.

The foundry provides us with a whole 3-inch wafer realized during the MPW run, containing multiple designs of the users that share the platform. The PI-SOA chip is the central cell of a piece with 3x3 cells (12x12 mm); this facilitates handling it during the post-processing.

2.5 Conclusion

A passive single section polarization converter has been designed for the Oclaro platform. The PC device has a calculated maximum conversion efficiency C=99.99% and total coupling loss of -0.48 dB (λ=1550 nm). A complete tolerance analysis is given in terms of width and length variation, wavelength dependence, alignment offset with input-output waveguides, input-output waveguides width variation and alignment offset during the EBL exposure. The PC shows good performance towards length and slope angle variation, however it is quite sensitive to width variations and to top-cladding thickness deviations from the nominal value of 2 μm. To have a conversion efficiency above 90% the width should be controlled in a range of ±40 nm.

The EBL alignment offset, due to the top-cladding thickness variations, has the worst impact on the PC performance. In order to obtain a conversion efficiency above 90% the top-cladding thickness variation should be controlled in the range of ±40 nm, thus a top-cladding thickness deviation in a range of ±2%.

A tolerant version of the PC, which consists of two mirrored section, has been presented to overcome the fabrication tolerance limits of the first generation device. The double section PC has a length which is double the length of a single section PC, a simulated maximum conversion efficiency of 99.99% and insertion loss of -0.5 dB for λ=1550 nm. A new process flow has been developed in order to keep the mirror symmetry between the two mirrored sections, which guarantees the high device performance. The double section PC shows a doubled width tolerance range for more than 95% conversion efficiency, and a conversion efficiency above 99% over the whole C-band.

The PC is developed to obtain polarization independent SOAs by placing the device between two identical SOAs. The polarization is converted halfway between the two SOA sections and hence the polarization properties are averaged out over the two polarization states. Since the PC is not integrated yet in the Oclaro standard platform, the device is post-processed in a prefabricated MPW PIC, which contains SOAs test structures.

The next chapter focuses on the solution adopted to connect experimental devices, the PC in our case, to the existing structures of a pre-fabricated PIC and on the technology developed to protect the PIC, during the post-processing. The PC process-flow is described in Chapter 4.

Chapter 5 present the design and characterization of a PIC for Brillouin sensing, whose performance can be definitely improved by introducing polarization handling functionality. An advanced design of the Brillouin PIC which includes the polarization converter is discussed in Chapter 6.

Chapter 3

Advanced post-processing for experimental devices

This chapter focuses on the solutions adopted to connect an experimental device (ED) to the structures of a prefabricated PIC and on the technology developed to protect the existing circuit, during the ED post-processing. This unique technology opens the possibility to add advanced functionality in PIC, since designs are not limited anymore to a predefined set of building blocks. In this project, the post-processing technique is applied to include a polarization converter (PC) in a PIC which contains polarization independent SOA test structures (Chapter 2). The enormous potentiality of the post-processing is strengthened in the final chapter (Chapter 6), where an advanced design of the Brillouin PIC with polarization handling functionality is presented.

After a brief introduction (Section 3.1), the design and simulation of the taper connections that properly interface devices processed using two different technologies (Section 3.2) is presented. Moreover, at the end of the section, measurements *results that support the taper design choice are shown. In Section 3.3, the processing steps used to protect the PIC, during the PC fabrication (see Section 4.4), are discussed. Conclusions are drawn in Section 3.4.*

3.1 Introduction

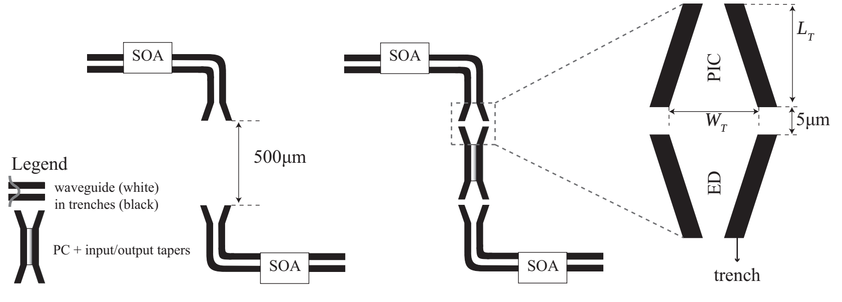
As explained in Section 1.1, the fabrication of an MPW, based on a generic technology platform, leads to cost-effective chips containing validated building blocks that can be exploited to test experimental devices (ED). Therefore, we designed a PIC which contains structures to test the polarization converter in a polarization independent SOA (PI-SOA) configuration (See Chapter 4). The test structure, processed by Oclaro, consists of passive waveguides (straight, curved and tapered), formed by etching deep trenches on both sides of the ridges, and SOAs (Fig. 3.1(a)); an unprocessed space of 500 μm is left in order to fabricate the ED together with input and output waveguides, at COBRA (Fig. 3.1(b)).

The required post processing technology has two main issues:

1. The PIC-ED connection.

2. The protection of the PIC during the processing of the ED.

The connection between the ED and the rest of the circuit is realized with pairs of coupled tapers. The ED is fabricated with tapered input and output waveguides that face the Oclaro tapers (Fig. 3.1(c)). A trade-off between performance and dimensions leads to the choice of the taper length and width; the aim is to have a short pair of tapers with high power coupling (higher than 80%), high fabrication tolerance and



(a) (b) (c)

Figure 3.1: (a) Schematic of a PI-SOA test structure in the PIC. (b) Schematic of a PC post-processed in a PI-SOA test structure, together with input and output tapered waveguides. (c) PIC-ED taper connection.

wide optical bandwidth. The next sections explain the taper design choices based on simulations (Section 3.2) and experimental results (Section 3.2.1).

The PIC protection is discussed in Section 3.3. Three tests have been run with different protection layers to avoid damaging of the existing structures during the ED fabrication.

3.2 PIC-experimental device taper connection

Due to alignment issues and a different technology used for the post processing, we cannot simply connect a straight Oclaro waveguide to a straight COBRA waveguide. To overcome this problem a free propagation region of 5 µm is left between the Oclaro devices and COBRA devices. To limit the divergence of a Gaussian beam propagating in this free propagation region, which is inversely proportional to the mode size in the input waveguide, the standard Oclaro waveguide is tapered out starting from a width $W_T = 1.5$ µm. This leads to an expansion of the size of the optical mode. Then the mode propagates through the free propagation region and couples to the post-processed COBRA taper. To model the taper, we start by defining the waveguide cross-section (Fig.3.2(a)) in FIMMWAVE [25]. The waveguide is constructed with a series of layers that define the epitaxial layer-stack. Thickness and refractive index are set for each layer and the ridge structure is defined by etching through the layers. The solver finds the waveguide modes using the film mode matching (FMM) technique.

A linear taper is defined between two waveguides with the same layer-stack but different widths. The variation along the longitudinal dimension z is modeled by the linear interpolation function $f(z) = az + b$, which generates the intermediate waveguides. Once the taper is designed, the propagated field is calculated using FIMMPROP (Fig.3.2(b)). During the calculation, the taper is dynamically split into sub-sections; the number of the subsections and their length may vary along the taper in order to have a higher discretisation in the numerically more difficult regions of the taper. A propagation scattering matrix is calculated for each subsection and used to compose the overall taper scattering matrix.

To achieve a highly efficient and tolerant design, the guided mode should propagate through the taper adiabatically [27]. Therefore, it is important to characterize the taper through the efficiency η_T, which is defined as the coupling from the fundamental mode at the taper input to the fundamental mode at the taper output, versus the taper length. In the adiabatic limit, modes do not couple.

Fig.3.3 gives an indication of the propagation for the fundamental TE mode;

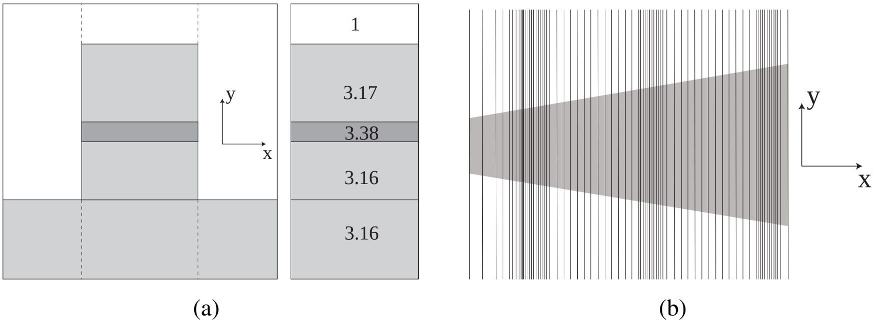


Figure 3.2: (a) Waveguide cross-section in FIMMWAVE. (b) Top view of the taper split into subsections for the calculation of the field propagation in FIMMPROP.

the graphs show the efficiency curves as a function of the taper length , for tapers with a 1.5 µm wide input waveguide and an output waveguide with a width which varies from 3 µm to 7 µm; in this case, the taper top-cladding is designed with the standard Oclaro thickness of 2 µm. The oscillations indicate that there is some conversion to higher order modes, but if the taper is designed with a length that corresponds to the maximum of an oscillation, the power couples back into the fundamental mode. The mode coupling increases with the taper angle, therefore the smaller W_T, the smaller the oscillations. Moreover, for a taper length larger than 100 µm the oscillations start to die out significantly and all the tapers are suitable for our design; so the next step is to characterize the performance of a pair of tapers facing each other. We first built a device consisting of two identical tapers and a free propagation region in between. The performance is evaluated in terms of coupling coefficient $k = \eta_{T_1}\eta_{T_2}\tau$, where η_{T_1} and η_{T_2} are the efficiencies of the first and second taper respectively, and τ represents the transmission through the free propagation region.

Fig.3.4(a) shows the coupling coefficient curves as a function of the taper length L_T for a width W_T which varies from 3 µm to 7 µm; L_T and W_T are equal for both tapers and a 2 µm thick top-cladding has been considered in the simulation. The longer tapers show smaller oscillations, however in order to optimize the number of devices that fit in a chip, a short taper is preferred. A taper coupler with a $W_T = 3$ µm has higher diffraction losses, whilst a taper coupler with a $W_T = 7$ µm has higher conversion losses; therefore, we choose $W_T = 5$ µm and $L_T = 100$ µm with a $k = 0.98$. The pair of tapers with these parameters shows high coupling and low oscillation, thus it is more tolerant to length variations. In Fig.3.4(b) the taper coupler with $W_T = 5$ µm and $L_T = 100$ is compared to a taper coupler with the same

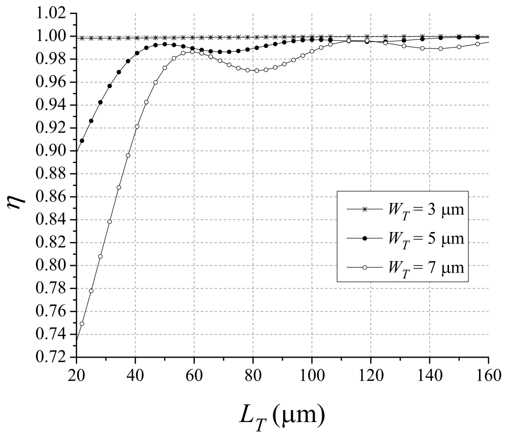
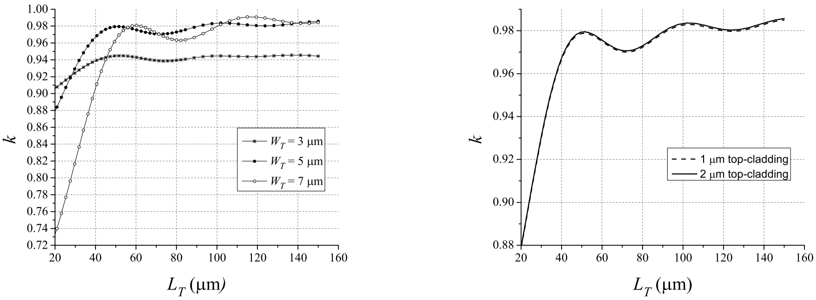


Figure 3.3: Taper efficiency curves as a function of the taper length for different taper width W_T (2 μm thick top-cladding) for TE polarization.

L_T and W_T, but with a top cladding lowered by 1μm starting half way the free propagation region over the whole post-processing area; this structure results from the PIC protection processing (see Section 3.3.3 about the chip protection steps). The graph shows that the difference in the height of the cladding does not influence the coupling between the two tapers. In the PI-SOA test structure the ED is connected to the Oclaro waveguides by two pairs of coupled tapers; thus, the device has 0.18 dB extra losses due to the taper connections.

The tapers that are connected to the ED design are defined using EBL; local markers on the PIC allow for the ED tapers alignment, which can be as accurate as 10 nm, depending on the marker quality. Fig. 3.5 shows that for a misalignment of 50 nm, k is still close to 0.98.

The simulations have been performed also for the TM mode. Due to numerical errors, the TM mode shows an unphysical behavior since the oscillations do not die out for a long taper. To validate the results also in the TM case, we calculate the efficiency with the FDM (finite difference method) solver for a taper with $W_T = 5$ μm and $L_T = 100$ μm. The efficiency value obtained with the FDM is 0.998. Thus the design is also suitable for the TM mode.



(a) (b)

Figure 3.4: (a) Coupling coefficient k calculated for a pair of tapers with the same length for different taper width (2 μm thick top-cladding) for TE polarization. (b) Coupling coefficient k calculated for a pair of tapers, where one taper and half of the free propagation region have a 1 μm thick top-cladding (W_T= 5 μm, TE polarization).

3.2.1 Experimental results

In this paragraph, the measurement results of the taper losses are reported; the device post-processing and the chip characterization will be treated in chapter 4. The results are given in Tab.3.1. The losses in an Oclaro passive test structure without taper connections (PIC_no-tapers, Fig. 3.6(a)) have been evaluated through a transmission measurement. The result is compared to two passive test structures with taper connections. The first one is fully made by Oclaro (PIC_tapers, Fig. 3.6(b)); in the second one the central tapered waveguide has been post-processed at COBRA (PIC-ED_tapers, Fig. 3.6(c)). The comparison between the output powers of PIC_no-tapers and PIC_taper shows that the Oclaro taper connections introduce 0.5 ± 0.1 dB loss; thus the measured losses are about 0.3 dB higher than the simulation result. The post-processed PIC-ED_tapers have another 0.5 dB extra losses, due to extra propagation loss introduced by a guiding layer undercut, which appeared during the post-processing of the first PC fabrication (this will be discussed in chapter 4). Due to the quantum well structure and to some defects in the guiding layer of that MPW run, the propagation through the passive waveguides is polarization dependent; the ratio between the P_{out} associated with and input mode TE and TM respectively is about 10 dB.

We can conclude that with 0.5 dB losses, coupled tapers are still well suitable for the ED-PIC connection.

	P_{in}	P_{out}
PIC_no-tapers	0 dBm	-5.3 dBm
PIC_tapers	0 dBm	-5.8 dBm
PIC-ED_tapers	0 dBm	-6.3 dBm

Table 3.1: Measured output power for passive test structure without taper connections (PIC_bends) and two passive test structures with taper connections (PIC_tapers and PIC-ED_tapers)

3.3 PIC protection technology

The post-processing technology consists of two sequential processes: the protection of the pre-processed circuit and the ED fabrication. This paragraph focuses on the PIC protection process flow. The ED process flow and its integration with polarization independent SOA test structures are explained in chapter 4. During the ED fabrication, the PIC should be protected against chemicals for cleaning and etching of InP. Plasma machines, used for deposition, etching and cleaning processes, must be used at temperatures below the annealing temperature of the contact pads of the active components on the PIC. The difficulty in the protection is mostly due to the

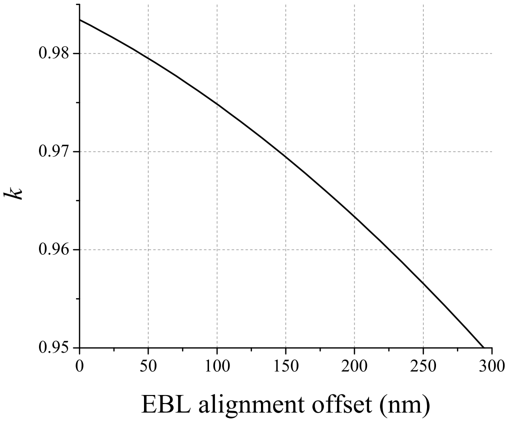


Figure 3.5: Coupling coefficient k as a function of the PIC-ED taper alignment offset in the EBL.

topology of the chip; since the passive waveguides are 4 µm deep-etched, it is not easy to deposit or spin a material uniformly on the PIC surface in order to protect the waveguides ridges. Three different approaches have been sub-sequentially tested for the PIC protection:

1. A double layer consisting of SiNx and ZEP
2. A triple layer consisting of SiNx, BCB and ZEP
3. A triple layer consisting of SiNx, photo-resist and ZEP

The next sections will describe the three procedures that have been tested on dummy samples processed with 4 µm deep-etched waveguides.

3.3.1 SiNx and ZEP protection

The choice for ZEP and SiNx comes naturally, since these materials act as masks during processing; ZEP is an EBL resist used for the waveguide definition and as a mask for the SiNx etching, while the SiNx is used as a mask during the waveguide etching. The test consists of the following steps:

- A 400 nm thick layer of silicon nitride is deposited using plasma-enhanced chemical vapor deposition (PECVD).
- A layer of ZEP is spun for 40 seconds at 5000 RPM and then baked in two steps: first a soft bake of 4 minutes at 150°C, followed by a 2 minutes hard bake at 200°C.

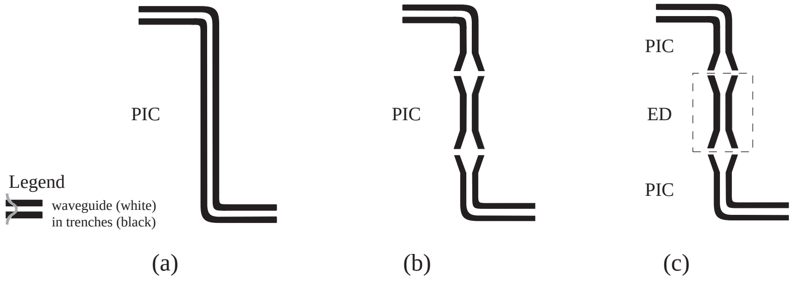


Figure 3.6: (a) Schematic of a passive test structure without taper connections (PIC_no-tapers). Schematics of passive test structures with taper connections (PIC_tapers (b) and PIC-ED tapers (c)).

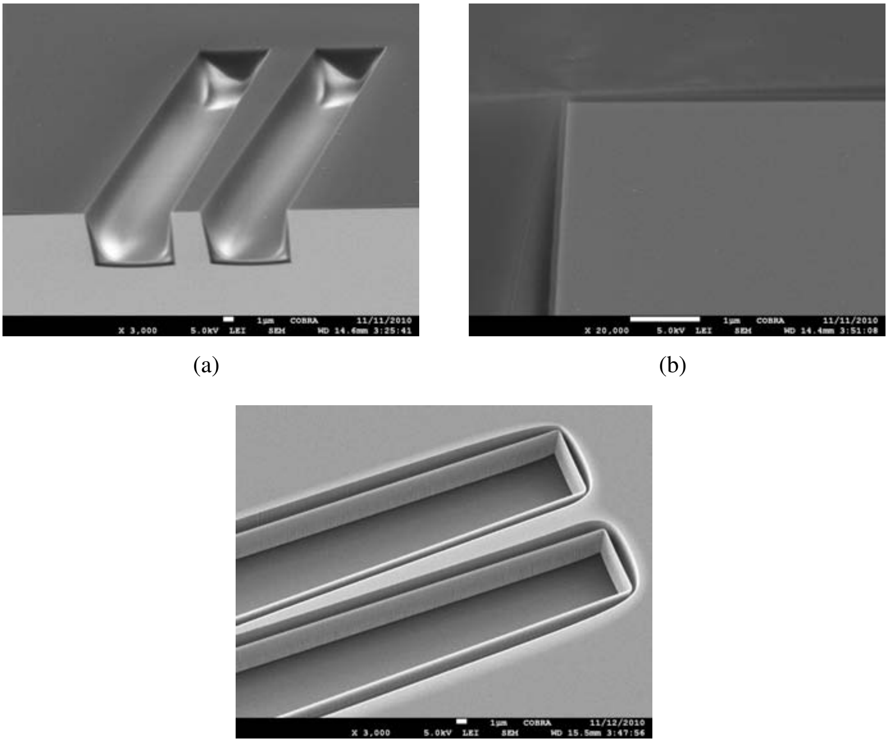
Usually, the ZEP thickness obtained using this recipe is about 350 nm over a flat surface. However, due to the deep-etched waveguides, the ZEP layer is not uniform after the spinning (Fig.3.7(a)) and its thickness on top of the ridge waveguide is not enough to protect the SiNx (Fig.3.7(b)) at the corners. As a consequence, while using the nitride RIE to define the post-processed structures, also the SiNx on the waveguide corners is etched. Therefore the waveguide ridges are exposed to ICP etching, needed to process the ED. Fig.3.7(c) shows an unwanted etched region around the waveguide due to a poor protection of the waveguide ridge.

3.3.2 SiNx, BCB and ZEP protection

To solve the problem of the large waveguide step height, a planarization of the surface is needed. The following recipe has been used:

- A 400 nm thick layer of silicon nitride is deposited using PECVD.
- AP3000 adhesion promoter is spun in two steps: first 30 seconds at 500 rpm, to spin a uniform adhesion layer on the sample surface, followed by 30 seconds at 3000 rpm, that defines the adhesion layer thickness.
- A thick BCB 3022-35 layer is spun over the PIC (Fig.3.8(a)) in two steps: first 20 seconds at 100 rpm, followed by 30 seconds at 500 rpm.
- The BCB is soft baked for 2 minutes at 120°C and then hard baked using a vacuum oven. The temperature is ramped up to 150°C for 30 minutes and afterward to 325°C for 60 minutes.
- The BCB is then etched back in the polymer RIE to the level of the waveguide top surface.

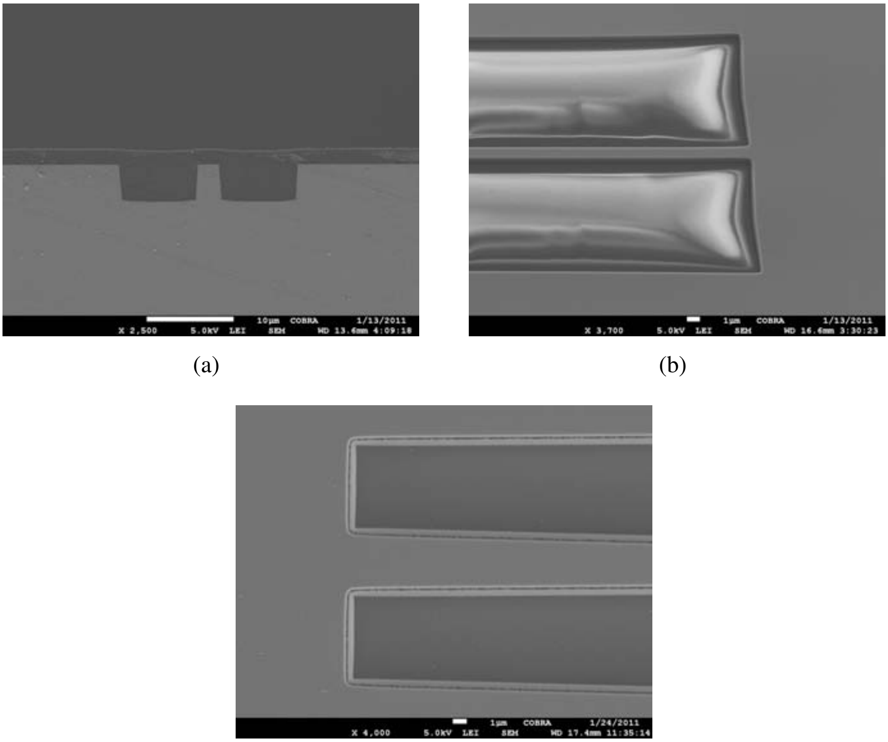
The last step is very difficult to control. Once the waveguides ridges are exposed, the plasma reactants are not consumed anymore on top of the waveguides and the etching rate increases next to the ridges. In order to completely clean the post-processing area, the BCB is etched too far below the waveguide top surface (Fig.3.8(b)), leading again to an inadequate ZEP protection on the ridges (Fig.3.8(c)).



(a) (b)

(c)

Figure 3.7: (a) SEM picture of a PIC taper cross-section after ZEP spinning. (b) Waveguide ridge. (c) PIC tapers damaged during the ICP etching of the post-processed structures.



(a)

(b)

(c)

Figure 3.8: (a) SEM picture of a PIC taper cross-section after BCB spinning. (b) Planarized BCB. (c) PIC tapers damaged during the ICP etching of the post-processed structures.

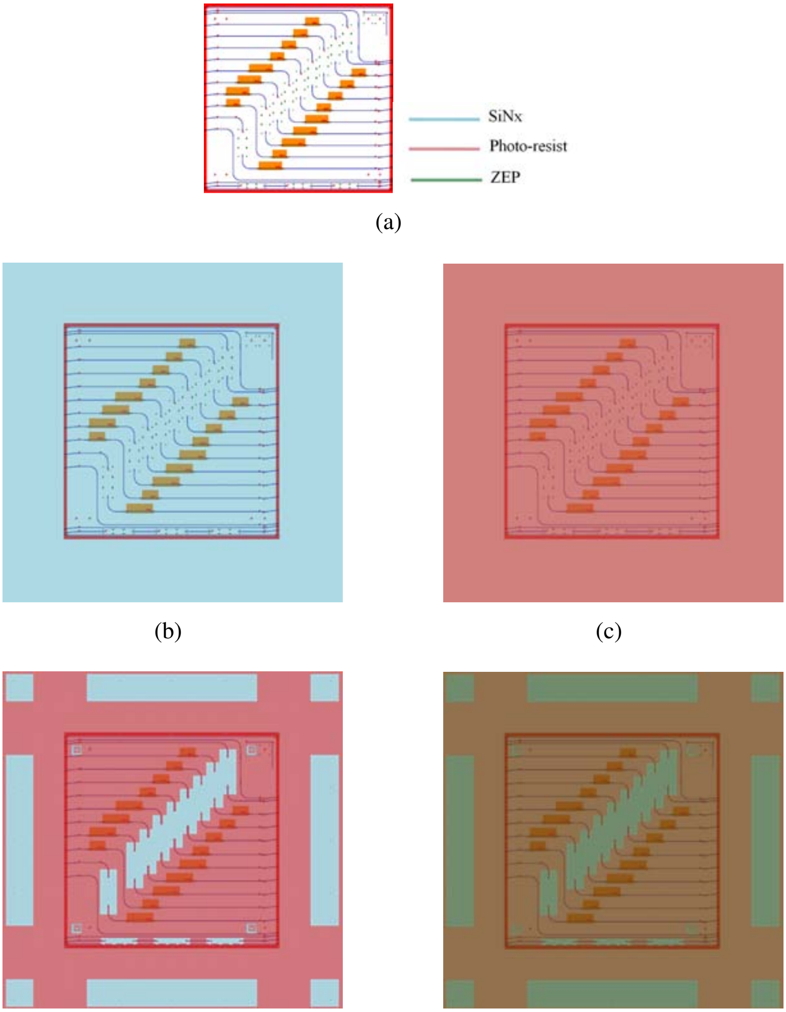
3.3.3 SiNx, photo-resist and ZEP protection

Since the planarization obtained by etching back the BCB did not work properly, a third method, based on photolithography, has been developed. This method consists of spinning photo-resist on top of the PIC (Fig.3.9(a)) covered by SiNx, and then opening the area for the post-processing using a photolithography mask. The chip is protected via the following steps:

- A 400 nm thick layer of silicon nitride is deposited using PECVD (Fig.3.9(b)).
- AZ 4533 photo-resist is spun for 30 sec at 2500 RPM and soft baked for 20 min at 95°C; the spinning speed defines the thickness of the photo-resist (Fig.3.9(c)).
- A photolithography Cr mask is used to open the areas for the PC processing (Fig.3.9(d)). After the exposure, the photo-resist is developed using AZ-developer diluted 1:1 ratio in H_2O for 2 min and 30 sec. The last step is the hard baking of the photo-resist. The temperature is gently ramped from room temperature to avoid strain in the photo-resist, which would cause cracks. At 200°C the photo-resist is baked for 20 min.
- The chip is then ready for the PC post-processing. First, O_2-plasma is applied to promote the adhesion between the EBL resist (ZEP) layer and the AZ resist; afterward, the ZEP is spun on the chip (Fig.3.9(e)).

The ZEP layer remains quite uniform (around 350 nm thick) from the middle of the opened areas to 5 μm away from the PIC tapers, which is indeed the distance between the two facing tapers. Thanks to the homogeneity of the ZEP thickness, the EBL exposure needed to define part of the PC can be performed with the same dose over the whole opened area. The opening for the post-processing starts 2.5 μm away from the Oclaro tapers, so the boundaries between the two different technologies fall in the middle of the free propagation region. This leads to a taper with a lowered top-cladding on the post-processing side; hence the adjustment in the design for the taper simulations (sec. 3.2). Since the protection mask has no critical feature we can easily achieve a good alignment between the protection layer and the PIC with optical lithography. The protection layer is renewed after every InP dry or wet etching step of the ED post-processing; at the end of the post processing, the AZ-resist is removed using O_2-plasma at high power (300 W) for 30 minutes. The photo-resists fills the 4 μm deeply etched waveguide trenches (Fig.3.10(a)) and, together with the SiNx and

ZEP layers, ensures a good protection of the ridges (Fig.3.10(b)). Fig.3.10(c) shows a taper successfully protected during the PC post-processing.



(a)

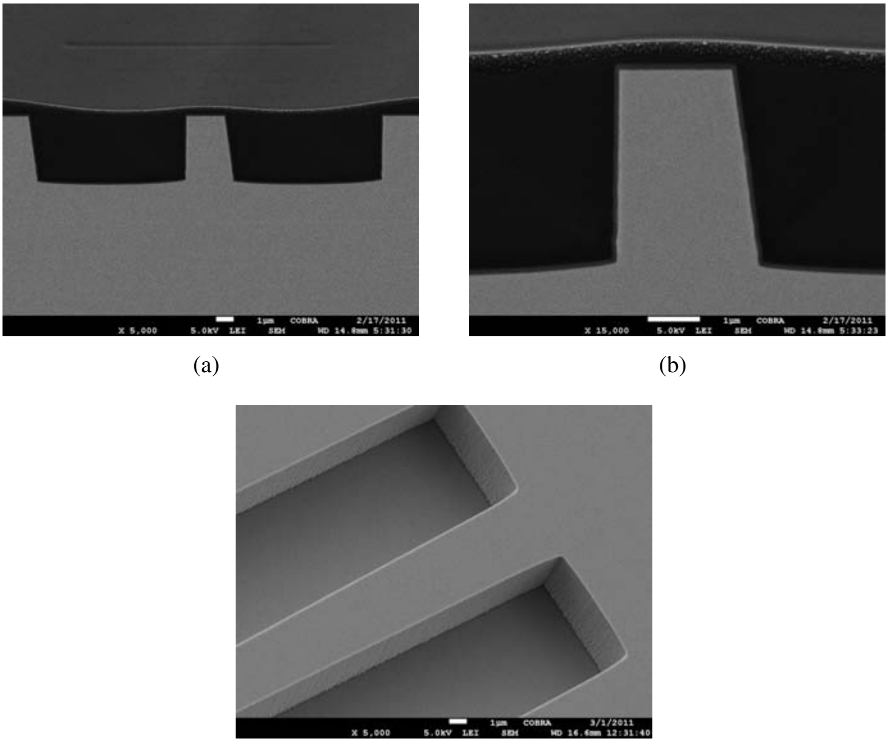
(b)

(c)

(d)

(e)

Figure 3.9: (a) Schematic of the PIC before the post-processing. (b) SiNx layer deposition on the chip surface. Photo-resist spinning (c) and exposure (d) to open the areas for the post-processing. ZEP spinning on top of the photo-resist (e) to define the COBRA structures with the EBL.



(a) (b)

(c)

Figure 3.10: (a) Waveguide cross-section after photo-resist spinning. (b) Zoom in on the waveguide ridge. (c) Protected taper after post-processing.

3.4 Conclusion

In this chapter, we present a unique technology to test experimental devices in prefabricated chips by post processing, taking advantage of validated building blocks, fabricated by a foundry. Advanced functionality can be included in PICs where the design is limited by the available generic technology platform. The connection between devices processed with different technologies is obtained through tapered waveguides. Measurement results show 0.5 dB extra loss for two pairs of coupled tapers, which is about 0.3 dB higher than the simulation result. The PIC is successfully protected, during the post-processing of the experimental device, by SiNx and a thick photo-resist layer. A photolithography mask has been used to define the areas for the post-processing. The post-process technology is used in this project to include a polarization converter in a PIC to achieve polarization independent SOA functionality (Chapter 4). In Chapter 6 an advanced Brillouin sensing PIC is presented to demonstrate how the post-processing can be exploited to improve the circuit performance by adding polarization handling functionality.

Chapter 4

PC fabrication and results

In this chapter, we report the fabrication technology and measurement results of the polarization converter (PC) device (see Chapter 2). The innovative PC with the triangular top cladding is fabricated through a process flow which requires only few extra steps compared to the standard Oclaro platform. In the first generation technology, the PC device is defined using EBL. However, this technique does not ensure the symmetry between the two mirrored cross-sections of the double converter. To solve the problem, a completely self-aligned process is proposed in the second generation technology. EBL is used only to define one PC sidewall, which can be done with photo lithography as well. This leads to the possibility of the PC integration in the standard Oclaro platform in the near future, by easily adapting the process flow. The PC is demonstrated in a PI-SOA configuration, showing a drastic reduction of the PDG with the insertion of the coverter, and the better performance of the double section PC over the single section one are confirmed. Section 4.1 introduces the main technology processes that have been used to fabricate the PC. Section 4.2, starts with a detailed description of the first generation PC process flow, followed by a discus-

sion on the critical processing steps. The section closes with the measurement results of the first generation PI-SOA. The second generation PC process flow, together with processing issues and measurements, is presented in Section 4.3. In the last section, conclusions about the device fabrication and performance are drawn.

4.1 Basic fabrication processes polarization converter

For the fabrication of the PC, together with input and output waveguides, a number of basic processing steps are applied. It is convenient to first briefly explain these basic steps in order to simplify the description of the complete PC process flow [28].

SiN mask deposition and etching

The dielectric layer is used as a mask during wet or dry etching of III-V compounds. This layer is deposited on the sample with plasma enhanced vapor deposition (PECVD). We use the SiN mask during InP reactive ion etching (RIE) and InP inductively coupled plasma (ICP) processes, and for selective wet etching, e.g. with HCl (for PC slope etching) and diluted H_2SO_4 (for contact layer etching). A design is first exposed, using EBL or photolithography, on a positive resist. The resist is developed and the desired pattern is transferred to the nitride mask by SiN RIE process.

Two different SiN RIE recipes have been used in the PC device fabrication: CHF_3:O_2 (SiN etch rate: 115 nm/min) and pure CHF_3 (SiN etch rate: 26 nm/min). Normally, pure CHF_3 is chosen when EBL resist is used as etch mask for the SiN RIE. The reason is that the oxygen, in the standard recipe (CHF_3:O_2), etches away the EBL resist too fast, so that the resist is removed before the nitride is opened.

Lithography

EBL is used for the definition of structures with critical dimensions, writing features below 10 nm accuracy. Here, it is used to define the PC and the input and output waveguides. After the SiN deposition (400 nm), positive ZEP resist is spun on top of the sample at 5000 rpm for 40 sec, resulting in a layer thickness of about 350 nm. The nitride and ZEP thickness influence the required EBL dose for the exposure. The ZEP is soft baked for 4 minutes at 150°C, and then hard baked for 2 minutes at 200°C.

Markers allow for the alignment during the exposure of the design. Markers are usually deeply etched crosses, whose arms are scanned by the electron beam during the alignment procedure. Thanks to the high contrast between the markers and the sample surface, the center of the cross can be found and the pattern design is exposed relatively to the marker coordinates.

Once the design of the pattern has been exposed, the ZEP resist is first developed in n-Amyl acetate for 1 min, then the development is stopped in a methyl isobutyl ketone (MIBK)-isopropanol solution for 45 sec. A short O_2 plasma stripping (1'30" min) at low power (100 W) is recommended to remove possible residues of the ZEP layer.

InP dry etching

The pattern definition in the resist layer is followed by a transfer to the SiN mask layer, and to the semiconductor. InP/InGaAs can be dry etched using methane-hydrogen (CH_4:H_2) either with RIE or ICP process.

- The ICP process requires a thick layer of nitride (400 nm) to etch 2 μm of InP. The etch rate of InP is about 75 nm/min, whilst the etch rate of Q1.25 is slower, 50 nm/min. Those values are monitored over time and they can slightly deviate (in the order of 10 nm/min) depending on the machine condition. After cleaning the etch rate can increase. On the other hand, the SiN mask etch rate (4 nm/min) is very stable over time, this means for ICP etching that it can be accurately controlled (in the order of 10 nm), by simply measuring the starting nitride layer thickness.
- RIE allows for etching with high selectivity between InP and SiN, hence the required nitride mask thickness is much less than with the ICP process; a nitride layer of 50-70 nm is sufficient to etch about 2 μm of InP. The InP etch rate is 55 nm/min, whilst the Q1.25 [1] etch rate is around 30 nm/min.

During etching of semiconductors with a CH_4:H_2 chemistry, deposition of polymers occurs on non-etched surfaces, causing micro-masking which results in roughness. Therefore, both for RIE and ICP processes, a few seconds of O_2 plasma descum[2] is performed after every etching cycle, which lasts 2 min in the RIE and 1 min in the ICP.

Cleaning

The first step of the processing is to remove organic particles using O_2 plasma. This process oxidizes a thin layer (2-3 nm, depending on the stripping time) of the InP surface; diluted H_3PO_4 (10%) for two minutes is used to remove the oxidized film

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[1] The quaternary (InGaAsP) layer Q 1.25 has a bandgap of 1.25 μm. This value gives a high refractive index contrast with respect to InP, a high electro-optical phase modulation, and a low absorption loss for a wavelength of 1.55 μm [12].

[2] Plasma stripping is used to remove layers of polymers, whilst plasma descum is a gentler process at lower temperature, mainly used to remove polymer residuals.

layer. H_3PO_4 is used every time that the InP is oxidized, i.e. after removing resists by stripping the sample.

An additional cleaning step is performed after SiN RIE etching. The presence of oxygen in the CHF_3:O_2 etching recipe can lead to the formation of oxidized silicon molecules on the ZEP or AZ-resist mask sidewalls. When the resist is removed with stripping, these residuals fall on the InP surface, creating micro-masking during InP dry etching. To avoid this, after stripping and H_3PO_4, it is recommended to clean the sample in diluted HF (1%) for a few seconds.

The above listed basic steps have been used in the process-flow of the polarization converter, which will be described in the next section.

4.2 First PI-SOA generation

4.2.1 Process flow

To post-process the first generation PC devices, we combine two sequential processes: the PIC protection and the PC processing. The PIC protection technology has been reported in Section 3.3.3, whilst the PC fabrication steps are described in the following and shown in Fig.4.1. The PC is processed together with input/output waveguides, however for simplicity reasons these are not represented in the process-flow schematic. At the beginning of the process and after O_2 plasma treatments, a new protection layer is applied to the PIC.

a) The fabrication process starts with the InP/InGaAsP/InP layer-stack from Oclaro (Fig.2.2), with the addition of three layers: an InGaAs contact layer (500 nm), a SiN/SiO_2 passivation layer (260 nm)[3] on top of the wafer, and a backside metallization Cr/Pt/Au (205 nm). The wafer is thinned down to 350 μm.

b) The SiN/SiO_2 layer is removed using a CHF_3:O_2 RIE process, next the contact layer is selectively wet etched in a 10 H_2O: 1 H_2SO_4: 1 H_2O_2solution. A 400 μm SiN mask layer is deposited with PECVD. The PIC is then protected according to the process described in Section 3.3.3 and ZEP is spun on top of the sample. Due to the protection process, the ZEP is spun on top of two different materials: the nitride, that covers the post-processing area, and the AZ resist protection layer. An O_2-plasma is first

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[3] After processing at Oclaro the wafer contains a 260 nm thick SiN/SiO_2layer on the post-processing area.

applied using the barrel etcher (1 min at 100 W) to promote the adhesion between the EBL resist (ZEP) layer and the AZ resist. Without this O_2-plasma treatment, openings in the ZEP layer close to the edges of the AZ resist pattern appear, preventing a correct pattern definition.

c) In this step, a rectangular area for the PC slope etching is defined using EBL. After exposure and development of the ZEP layer, the SiN mask pattern is dry etched using a pure CHF_3 RIE process.

d) The InP top cladding is wet etched in a 4 H_3PO_4: 1 HCl solution. The selective etching starts from the SiN mask edges and stops at the interface with the guiding layer, producing a 35^o degree slope w.r.t the chip surface.

e) After removing the ZEP with a long O_2-plasma recipe (30 min) at high power (300 W) and the nitride layer with the CHF_3:O_2 RIE process, a new layer of nitride (400 nm) is deposited with PECVD, the PIC protection step is performed again, and ZEP is spun after a O_2-plasma treatment.

f) A second EBL step is performed to define the PC, together with input and output tapered waveguides, using ZEP resist. Then the pattern is transferred to the SiN layer with dry etching in a pure CHF_3 RIE process.

g) Finally, a CH_4:H_2 ICP plasma is used to deeply etch (4 μm) the PC and input-output waveguides through the InP/InGaAsP/InP layers.

h) The remaining ZEP, as well as the protection layer, is removed using O_2 -plasma (stripping for 30 min at 300 W) and the SiN is etched away from the top surface in a CHF_3:O_2 RIE process.

Although this processing appears straightforward, a number of problems have been encountered. These will be discussed in the next section.

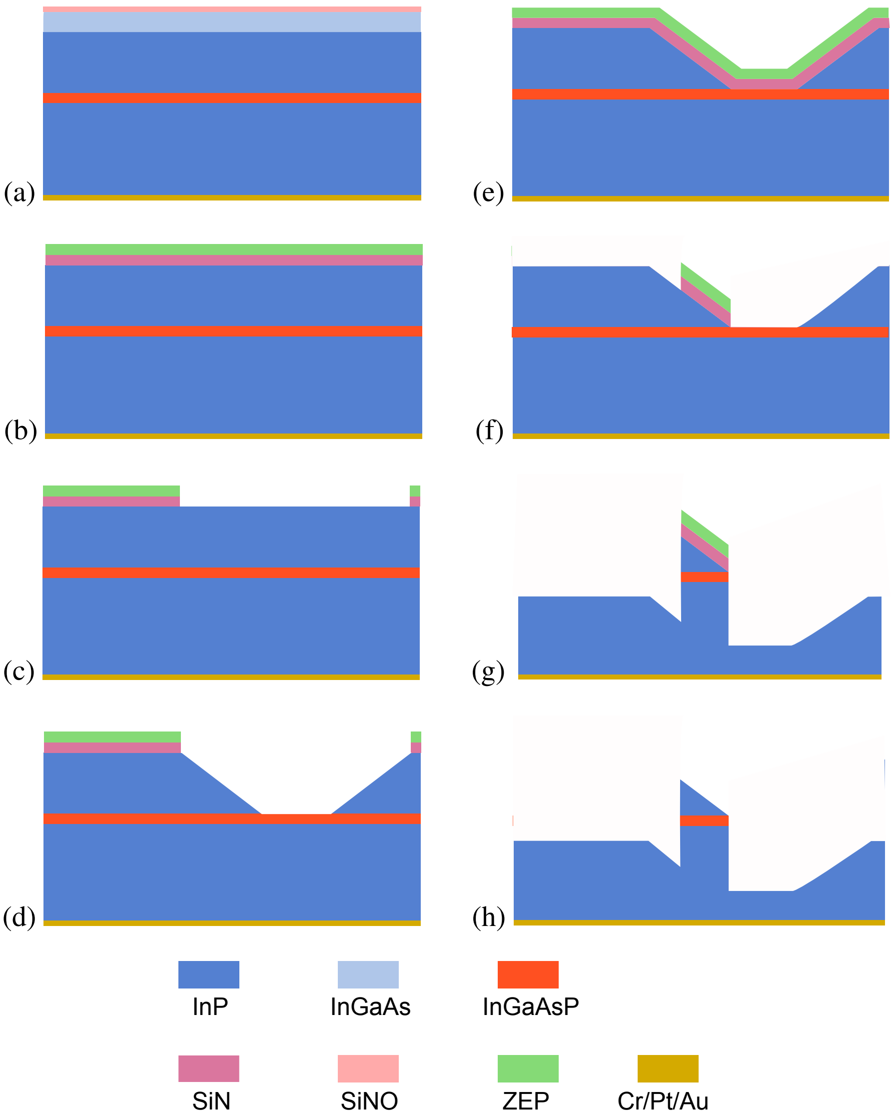
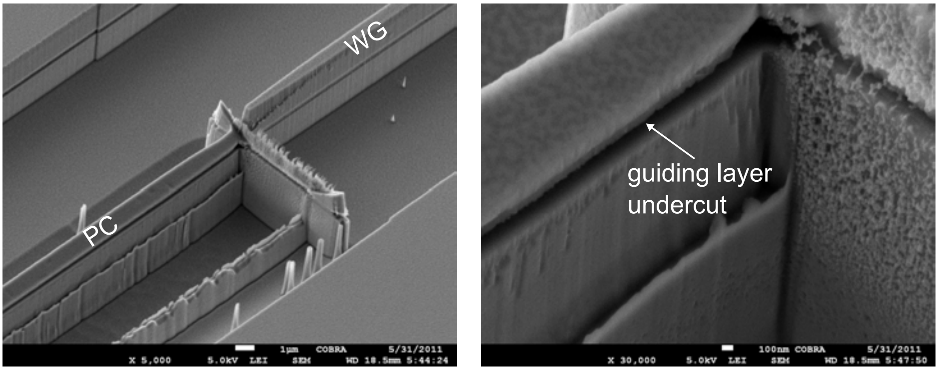


Figure 4.1: Process flow for the fabrication of the first generation PC.

4.2.2 Fabrication problems

Using the process flow that has been presented in the previous paragraph, the first generation PC, together with input and output waveguides, has been fabricated. In this section a description of the problems that have been encountered during the fabrication is given together with the technology that has been developed to overcome these problems. Fig. 4.2(a) shows a SEM picture of the final device.



(a) (b)

Figure 4.2: (a) First generation PC device. (b) Zoom in of the guiding layer undercut.

As we can see, there are three main issues that affect the processing:

- The PC waveguide shows an undercut in the order of 100 nm into the guiding layer (Fig. 4.2(b)).
- The PC waveguide becomes narrower at the connection with the input waveguide.
- The input waveguide sidewalls are quite rough over a length of about 5 μm.

Guiding layer undercut

The guiding layer undercut has the largest impact on the device performance, leading to high propagation loss and to a significant deviation from the simulated polarization conversion (see Chapter 2). The undercut of the guiding layer is a consequence of the galvanic corrosion in metallized III-V wafers, cleaned in acid solution (e.g. diluted HF, diluted H_3PO_4) [29]. InP/InGaAsP/InP semiconductor layers are anodic to the backside metallization[4]. As a result InP and InGaAsP both oxidize and dissolve into the electrolyte solution as Ga^{3+} and In^{3+} ions, along with the formation of some type of complex arsenate or phosphate. Since InP is less anodic to the metallization compared to InGaAsP, the corrosion of the second compound is significantly faster than the first one. The corrosion process is further aggravated by the large ratio between the backside metallization and InGaAsP area ($\approx 10^3$).

Another important issue is that the corrosion of InGaAsP in electrolyte solutions is also a photo-electrochemical process, meaning that the presence of light enhance this process, exciting free electrons that flow from the semiconductor to the backside metallization and react with the electrolyte.

This analysis raises two different but related problems: 1) the reaction that takes place when a semiconductor is cleaned in an acid solution, 2) the effect of light during the cleaning. The first test that has been done to better understand the nature of the guiding layer undercut consists in cleaning two samples in different light conditions and checking the effect on the waveguide cross-section: one sample is cleaned with a short O_2-plasma stripping (10 min) at high power (300 W), then rinsed in a 10 H_2O: 1 H_3PO_4 solution (2 minutes), and finally in HF 1% (2 seconds); the other sample undergoes the same procedure but the wet cleaning steps are performed in the dark, switching off the neon lighting on the working bench and using a dark plastic cover. Fig.4.3 shows two SEM images of the waveguide cross-sections; the guiding layer undercut does not appear when the cleaning steps are performed in the dark.

A second device has been post-processed in a PIC, again following the process-flow of Fig.4.1, but now using the dark cleaning technique. However, after the processing the guiding layer undercut appeared again. The relevant difference between this processing and the light/dark cleaning test is that the latter was performed on samples approximately ten times smaller than the PIC used for the PC post-processing. This result shows the relevance of the amount of metal present on the sample backside.

Combined with the dark cleaning, the solution to solve this problem is to isolate the metallization from the electrolyte by shielding the backside with 100 µm of SiN. This step will be better explained in the section dedicated to the second generation PC process flow (Section 4.3).

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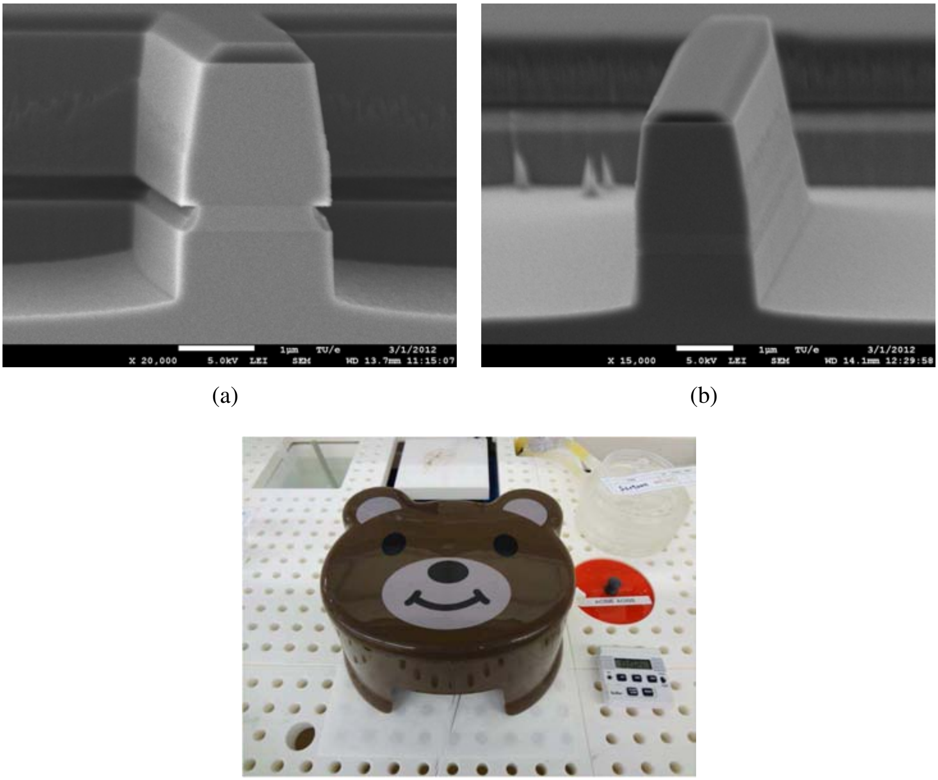
[4] The semiconductor is anodic also to the contact pads. Here, this can be neglected for two reasons: the pad area is 3 orders of magnitude smaller than the backside metallization and moreover the pads are protected by AZ photoresist during the processing, so that there is no electrical contact with the acids.



(a)

(b)

(c)

Figure 4.3: (a) Waveguide cross-section after cleaning the test sample in acid solutions in normal light conditions. (b) Waveguide cross-section after cleaning the sample in the dark, using a plastic cover (c) and switching off the bench lighting.

Waveguide narrowing at the PC-waveguide connection

The second processing issue, found from the SEM pictures of Fig. 4.2, concerns the narrowing of the PC waveguide width at the connection with the input and output waveguides. This effect, which extends over a length of 2 µm, doesn't really influence the conversion (see Fig. 2.5). However, it could end up in an air gap at the PC-waveguide connection, leading to unwanted reflections.

After using HCl (Fig. 4.1(d)), the bottom of the slope is 2 µm below the top surface; thus, the PC pattern is exposed on a level which is 2 um lower than the surface where the input and output waveguides are defined. Fig. 4.4 shows how ZEP, spun over the 2 µm step, forms a bridge with a narrower width compared to the waveguide pattern in the nitride on the top surface. The bridge width is then transferred with an etching process to the nitride and afterward to the InP/InGaAsP/InP layer (Fig. 4.1(f) and (g)).

Sometimes the bridge can be a thin foil, sensitive to fractures; if this happens, the nitride mask is etched and the InP/InGaAsP/InP layer as well, creating a gap between the PC and the input waveguide. The ZEP bridge can be avoided by lowering the top cladding by about 1 µm after etching the SiN/SiO$_2$ layer and the contact layer (Fig. 4.1(b)). This reduces the step height between PC and input waveguide, allowing for a better ZEP distribution on the sample surface.

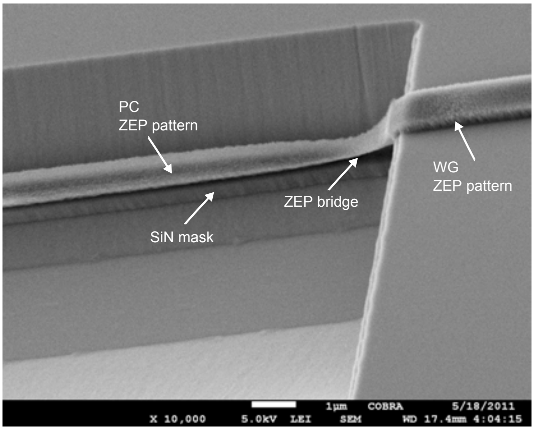
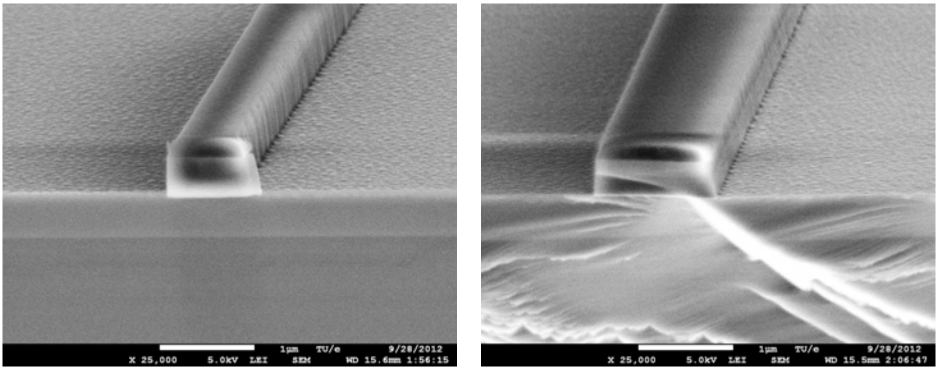


Figure 4.4: ZEP waveguide pattern on a 2 µm step.

Waveguide roughness

The last problem to solve is the waveguide roughness, which will increase the propagation loss over a length of 5 µm. The PC and input-output waveguide patterns are defined by EBL, using ZEP 520A, which is a positive resist. During the exposure, the electrons dissociate the polymer molecule bonds, causing scission that breaks the original polymer into segments of a lower molecular weights, which are more readily developed [30]. This fragmentation causes roughness in the ZEP pattern sidewalls after the development, that is subsequently transferred to the SiN and to the InP layer during dry etching.

Nevertheless, ZEP has the property to re-flow at a temperature above 145°C , changing its profile from reentrant to a rounded shape, and smothering the sidewall roughness [31]. Several tests have been performed to find out the optimal temperature and timing of the reflow process [32]; Fig.4.5 shows the waveguide pattern after ZEP development and SiN RIE etching. In the left picture the ZEP has been developed and the SiN has been etched; in the right picture, the ZEP has been developed and baked before etching the SiN. After stabilizing the hotplate temperature at 154°C, the sample is positioned on a silicon carrier wafer, placed on top of the hotplate and the ZEP is baked for 2 minutes. This procedure clearly reduces the roughness.



(a) (b)

Figure 4.5: (a) Etched SiN waveguide pattern without baking the ZEP and (b) after baking the ZEP.

A second device has been fabricated, applying all the above mentioned adaptations in order to improve the processing. As it is shown in Fig.4.6, in the second fabrication the guiding layer does not present any undercut, the PC waveguide doesn't become thinner at the PC-input waveguide connection and finally the input waveguide sidewall has no significant roughness. Thus, it appears that the adapted processing indeed results in high quality post-processed devices.

Unfortunately, a misalignment occurred during the EBL exposure of the PC and the input/output waveguides pattern, leading to the case of a PC with a plateau at the bottom of the slope (see Chapter 2). The plateau has a a width of about 200 nm, implying that the polarization conversion is drastically reduced.

The characterization of the first generation PC is presented in the next section.

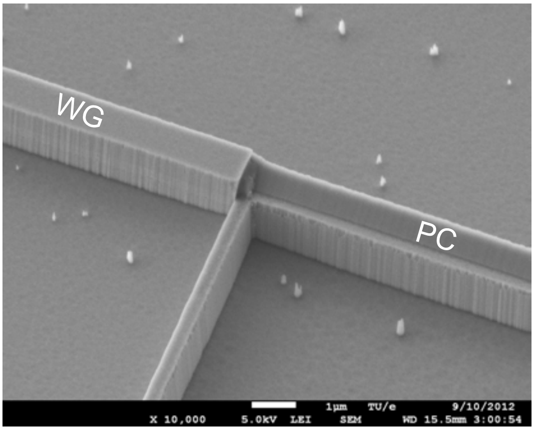


Figure 4.6: Second fabrication of the first generation PC device.

4.2.3 Measurements

We choose to characterize the first fabricated PC device, which presents higher propagation loss but better performance in terms of polarization conversion compared to the second device. Unfortunately, some PC waveguide sections were severely damaged at the end of the processing during step height measurements, performed with a surface profiler. The profiler stylus can damage deeply etched waveguides (4 µm) with a relatively thin width (1 µm). For this reason, it was not possible to compare test structures with and without polarization converters, and having the same SOA length. The measurement result is nevertheless relevant to experimentally prove the PI-SOA principle.

In the measurement setup (Fig. 4.7) the output polarization maintaining (PM) fiber of a tunable laser, working at λ=1550 nm, is connected to a polarization controller. The polarization controller is used sub-sequentially to minimize and maximize the PI-SOA output power in order to obtain $P_{out_{Max}}$ and $P_{out_{min}}$, associated with P_{TE} and P_{TM} respectively. We calculate the TE-TM extinction ratio $P_{TE} - P_{TM}$ (dB) for two test structures: one with the PC (PI-SOA) and one without PC (SOA_noPC). In SOA_noPC the PC section is replaced with a deeply etched passive waveguide, 1.5 µm wide. The measurement results (Tab.4.1) show that the polarization dependence of two SOA's in series reduced from 14 dB to 3 dB with the PC in-between, indicating the presence of a sizable polarization conversion. The estimated polarization conversion is about 80%.

Since the PC is not realized within the specifications in this circuit, no further characterization was done. Instead, attention was focused on the new fabrication technology of the second generation, which does not have alignment issues.

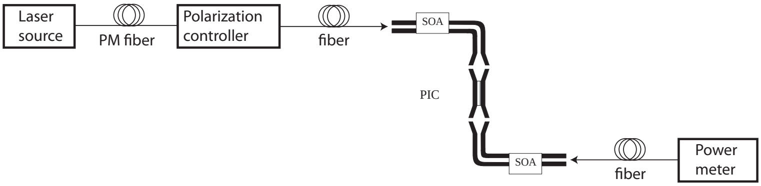


Figure 4.7: Measurement setup of the first generation PI-SOA

	SOA_L(µm)	I_{SOA}(mA)	P_{in}(dBm)	$P_{TE} - P_{TM}$(dB)
SOA_noPC	500	35	5	14
PI-SOA	300	25	0	3

Table 4.1: Measurement results of the first generation PI-SOA

4.3 Second PI-SOA generation

The main goal of the technology, developed for the post-processing of the second generation PC, is to obtain robustness against geometrical deviations of the PC shape that can occur during fabrication. In Chapter 2, it has been explained that width variations in the PC waveguide, as well as a misalignment during the EBL exposure of the PC waveguide on top of the slope, have the most severe impact on the polarization conversion. This fact together with the necessity to keep the symmetry between the two section of the double section converter, leads to the development of a new self aligned process flow, applied for the fabrication of the second generation PC.

4.3.1 Fabrication

To fabricate the second generation PC together with input and output waveguides, the following process flow (Fig. 4.8) has been developed:

a) The fabrication process starts with an InP/InGaAsP/InP layer-stack (Fig. 2.2), with the addition of three layers: an InGaAs contact layer (500 nm) and a SiN/SiO_2 passivation layer (260 nm) on top of the wafer, and a backside metallization of Cr/Pt/Au (205 nm). The wafer is thinned down to 350 µm.

b) A thick layer of AZ resist is spun on top of the surface and soft backed at 120°C for 10 min. Then, the PIC is placed upside down in the PECVD chamber and a layer of SiN is deposited (100 nm). The AZ resist is then removed using acetone and isopropanol. Afterward, as in the first generation process flow, the SiN/SiO_2 is dry etched using a CHF_3:O_2 RIE process, then the contact layer is selectively wet etched in a 10 H_2O: 1 H_2SO_4: 1 H_2O_2 solution. The top cladding is lowered to the PC top height (763 nm) with a CH_4:H_2 ICP plasma. A 400 µm SiN mask layer is deposited with PECVD. The PIC is then protected and ZEP is spun on top of the sample. An O_2-plasma is applied using the barrel etcher (1 min at 100 W) to promote the adhesion between the EBL resist (ZEP) layer and the AZ resist.

c) In this step one of the vertical sidewalls of the PC is defined together with input and output waveguides using EBL. The waveguide bridge in between the two sections of the double section converter is defined as well. After exposure and development of the ZEP layer, the SiN mask is dry etched using a pure CHF_3 RIE process. An CH_4:H_2 ICP plasma is used to deep etch (4 µm) the mesa trenches and input-output waveguides.

d) A layer of silicon nitride (50 nm) is deposited with PECVD.

e) Since during the SiN RIE process the direction of the plasma is perpendicular to the sample surface, it is possible to control the etching time in order to the remove the nitride on top of the mesa, but to keep it on the vertical sidewalls. This allows for the etching of the slope in a solution of 4 H_3PO_4: 1 HCl, using the nitride on the sidewall as a mask.

f) The sample is then covered with a thick layer of SiN (1000 nm) with PECVD.

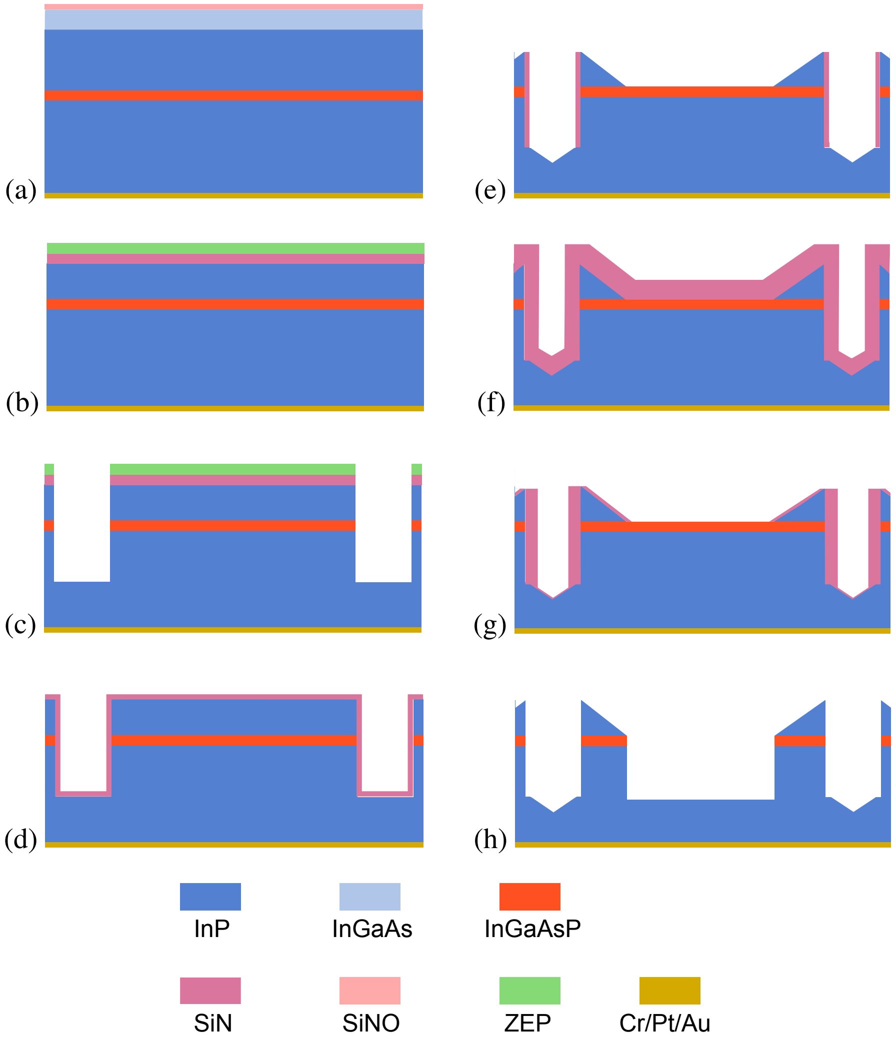


Figure 4.8: Process flow for the fabrication of the second generation PC.

g) At this point we etch the nitride in CHF_3:O_2 RIE process. Since PECVD is conformal, the nitride thickness on the slope will also be 1000 nm, but in the direction normal to the slope. This means however that in the vertical etching direction the thickness becomes 1250 nm (Fig. 4.9). Controlling the etching time, the nitride can be completely removed from the horizontal surface while a thin layer of nitride (around 70 nm) is kept on top of the slope (Fig. 4.10(a)).

h) The remaining layer of nitride is used as mask to etch the second vertical sidewall in the CH_4:H_2 InP RIE process (Fig. 4.10(b)). This process has a high selectivity between SiN and semiconductor, so it is possible to deeply etch the InP (about 1.3 μm) with this thin layer of nitride. However, the etched sidewall forms an angle, with respect to the vertical direction, which is 7 degrees for rectangular waveguides. In this case, as can be seen from SEM image in Fig. 4.10(c), after the RIE etching the vertical sidewall presents two angles: 11 degrees for the InGaAsP layer, and 3 degrees for the InP layer. The PC design has been adjusted before the processing, based to this new geometry (see Chapter 2).

i) The remaining nitride is finally removed using HF 10%.

Fig. 4.11 shows SEM pictures of the fabricated single section PC (a) and double section PC (b) devices, that have been successfully post-processed. Fig. 4.11(c) shows an overview SEM picture of the PIC, containing the PI-SOA test structures, after the post-processing.

The second generation PC fabrication is independent of alignment offsets (Section 2.2), that can occur during the EBL exposure. These alignment offsets would lead to a PC with a different cross section than the designed one (Fig. 2.11) and affect the conversion efficiency (Fig. 2.12). This issue is also very critical for the double section converter since it breaks the symmetry between the two mirrored sections. Another advantage of the new process-flow is the increased tolerance against PC width variations. The most relevant improvements of the second generation process-flow are the following:

- The ICP etching (Fig. 4.8(b)) to lower the top cladding is the only step that defines the PC width. This etching stops at 763 nm (±10nm), which is the PC top height calculated for the optimal PC width of 1 um. Once the initial nitride mask layer thickness is known, this etching can be controlled within 10 nm. A monitor sample is etched together with the real chip to accurately

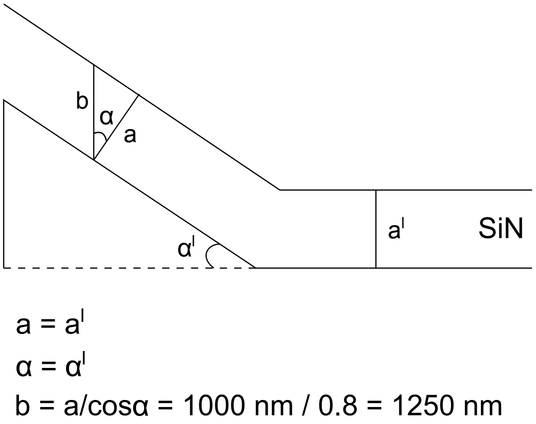


Figure 4.9: SiN thickness on the flat surface and on the slope.

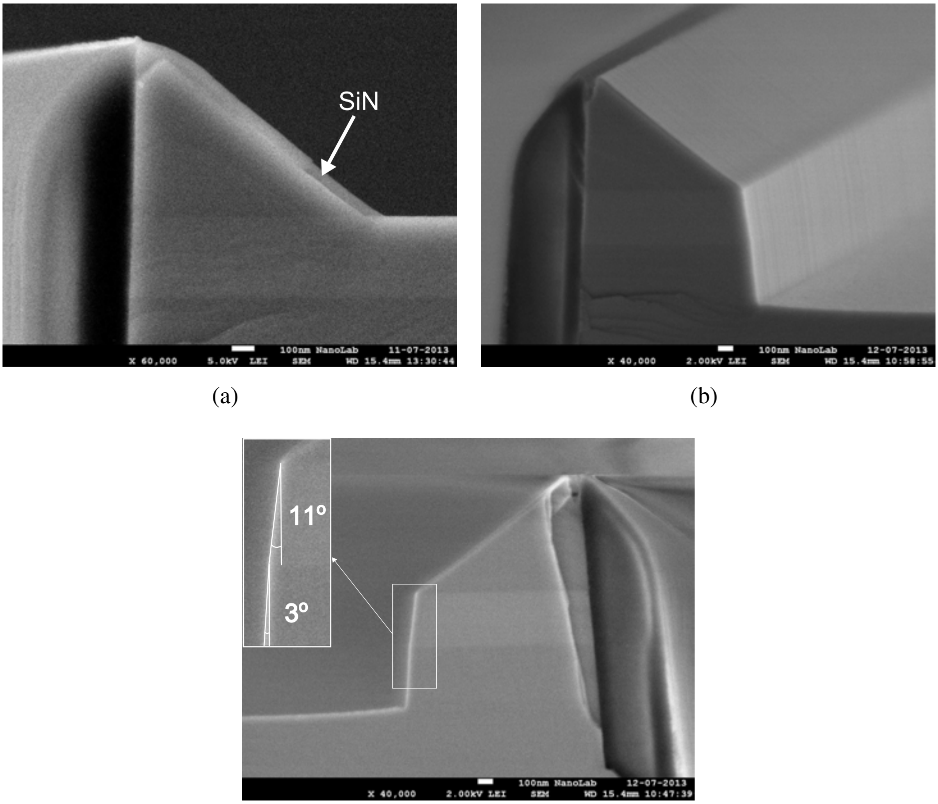
control the etching level. Etching variations within the range of 10 nm have been measured across the monitor sample (15x15 mm).

- The EBL exposure (Fig.4.8(c)) does not define the PC cross-section as for the first generation PC. It defines one of the PC vertical sidewalls together with input and output tapered waveguides and their position with respect to the Oclaro tapers. The alignment accuracy can be within 10 nm [28], leading to a coupling above 98% (Fig.3.5).
- The HCl etching (Fig.4.8(e)) creates a slope with a fixed angle of 36 degree; thus if the PC top height (763 nm) is defined within 10 nm, the PC width is defined within 14 nm. For a PC width variation within 14 nm, the conversion efficiency *C* is still above 95% for a single section PC.
- The second straight sidewall is etched with RIE process starting from the bottom of the slope, which is protected with a SiN layer. This can never lead to a PC with a different cross section than the designed one and it ensures the symmetry between the two mirrored section of the double section PC.

A few minor problems have been encountered during the processing. These are discussed in the next section.

4.3.2 Fabrication problems

Different issues have been encountered during the second generation processing PC.

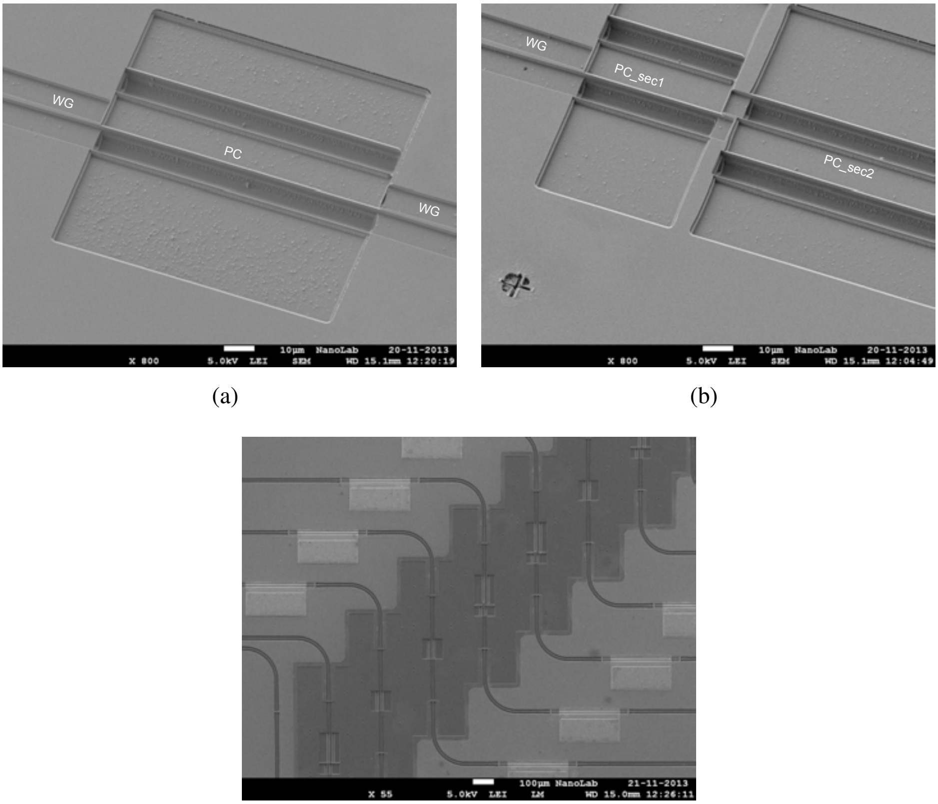


(a)

(b)

(c)

Figure 4.10: (a) SEM picture of the nitride thickness on top of the slope after SiN RIE etching (Fig.4.8 step (g)). (b) SEM picture of the PC cross-section after InP RIE. (c) Sidewall angles after InP RIE. In all the pictures the SiN sidewall cover is present.



(a)

(b)

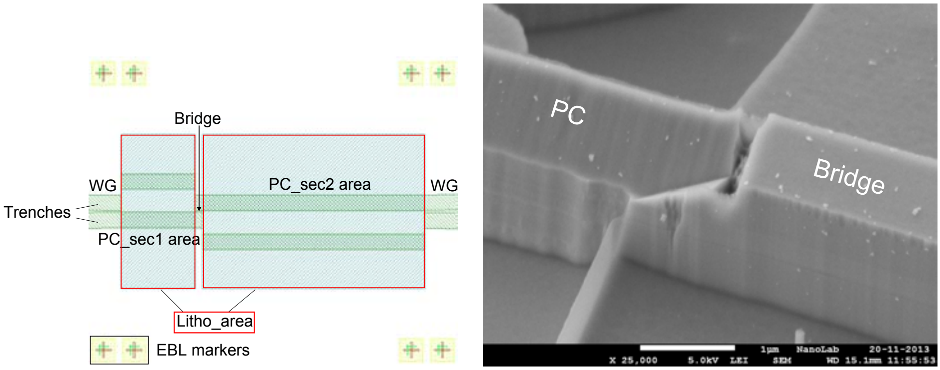
(c)

Figure 4.11: (a) SEM pictures of the fabricated single section PC and (b) double section PC. (c) SEM picture of the PIC SOA test structures after the PC post-processing.

Input-output waveguides and double section PC bridge protection

During the fabrication of the second generation PC, a photolithography mask has been used to protect input and output waveguides as well as the bridge that connects the two sections of the double section PC. The photolithography step is performed after step (d) and (f) of the process flow (Fig. 4.8) to prevent the InP wet and dry etching of the input-output waveguides and the bridge. Fig. 4.12(a) shows the design of the protection photolithography mask; Litho_area rectangles are open areas in the chromium mask, meaning that the positive AZ resist underneath the mask will be exposed and developed there, while the surrounding area will be covered with resist. If the mask is not well aligned to the substrate, along the waveguides direction, part of the waveguide can be exposed to the etchants. This leads to short sections of waveguides which are partially etched, causing possible reflections (Fig. 4.12(b)).

This problem can be easily solved by extending the mask cover about 200 nm outside the input and output waveguides and bridge edges, at the PC connection sides. In this case, if the mask is perfectly aligned, a 200 nm free propagation region region will be created at the input-output waveguides and PC connection (as well as at the bridge-PC connections). This has no impact on the device performance, since the region is much smaller than the conversion length. On the other hand, if the mask has an alignment shift of about 100 nm, the waveguides will still be protected.



(a) (b)

Figure 4.12: (a) Photolithography mask (delimited by red lines) to protect PC input and output waveguides as well as the bridge connection between the two section of the double section PC. (b) SEM picture of an hole between PC and bridge, due to a mask misalignment.

SiN removal at the end of the processing

During the PC fabrication, SiN mask layers are deposited in several steps of the process flow. Therefore, at the end of the processing a thick layer of nitride covers the waveguide and PC sidewalls. This affects the polarization conversion: the thick nitride layer exerts strain that can deform the PC shape and changes anisotropically the refractive index in the waveguides, thus causing polarization dependent effects. For these reasons, it is necessary to remove the nitride from the sample at the end of the processing.

In order to preserve the SiN/SiO_2 adhesion layer, deposited by the foundry between the contact layer and the SOA contact pads, an isotropic CF_4 plasma process has been tested, using the barrel etcher, to remove the sidewall SiN. Fig. 4.13 shows a SEM picture of a waveguide after SiN etching using CF_4. The process creates residuals which are difficult to remove. Even though this doesn't significantly influence the device performance, a cleaner solution has been found.

The second approach, consists in removing the nitride layer using diluted HF (10%). In this process it is important to stop the etching as soon as the InP substrate becomes visible to the bare eye, in order to avoid underetch of the SiN/SiO_2 isolation layer. IV curves of a 500 µm long SOA (Fig. 4.14), recorded before the processing and after SiN etching with 10% HF, show that the contacts are not attacked. Hence HF can be used to remove the thick nitride layer at the end of the processing.

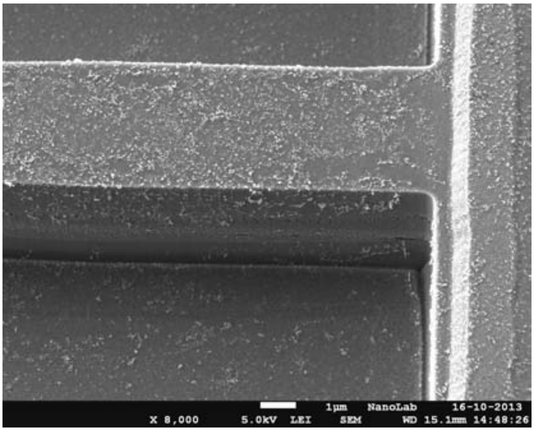


Figure 4.13: SEM picture of a waveguide after SiN CF_4 plasma etching.

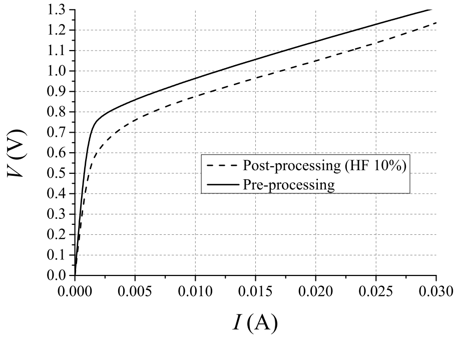


Figure 4.14: IV curves of a 500 μm long SOA before and after 10% HF.

Etching rate stabilization for SiN RIE

To test the nitride etching on top of the slope, quarters of a two inch wafer have been used, covered with nitride. The etch rate was uniform and with the standard value of 115 nm/min using a CHF_3:O_2 process. To remove the nitride from the horizontal surface, keeping a thin layer on the slope for the InP RIE etching, first a relatively long CHF_3:O_2 etch is performed until about 250 nm of nitride is left on the slope and 50 nm on the flat surface. The last step consists of a 30 sec etching cycle, which includes about 10% overetching, to completely clean the top surface, leaving about 70 nm of nitride on the slope. A dummy sample has been etched in parallel to check the cross-section step by step.

The PIC is smaller than the test sample and furthermore the nitride mask is mostly covered with AZ resist, used for protection of the existing structures during the post processing. The nitride surface on the dummy sample, exposed to the CHF_3:O_2 plasma, is approximately 10 times larger, which implies a higher and not really reproducible SiN etch rate on the PIC. In this situation it becomes very difficult to control the etching in order to keep 70 nm of nitride on the slope; the last step should be less than a half RIE cycle, and such a short time prevents the stabilization of the plasma.

To reduce and stabilize the etch rate, a large 3 inch silicon wafer covered with nitride is used as a carrier wafer inside the process chamber. The samples are placed on this carrier during the etching, so the process becomes independent on the size of the nitride openings on the PIC. In this way the etch rate goes down to 90 nm/min, which makes the SiN etching easier to control. The reproducibility of this technique allows for performing this step even without a test sample to control the cross-section, as long as the initial SiN thickness is known.

4.3.3 Measurements

The second generation PC measurement setup and procedure are identical to those used to characterize the first generation device (Fig. 4.7). Fig. 4.15(a) shows the polarization dependent gain (PDG) as a function of the wavelength for a test structure consisting of 300 µm long SOAs without polarization converter. $P_{TE} - P_{TM}$ is between 13 and 18 dB over the C band, and the behavior as a function of the current, injected in each of the SOA sections, indicates that the TE gain becomes larger than the TM gain as the current increases. This can be expected, since the SOAs are designed to work for TE polarized light. The PDG has also been measured in the case of a PI-SOA, consisting of 300 µm long SOAs and a double section PC (Fig. 4.15(b)). The graph shows the $P_{TE} - P_{TM}$ behavior for different current settings; in this case, the PDG decreases to only 0.05-0.9 dB over the C band.

The last graph (Fig. 4.15(c)) compares the PDG of a test structure without PC (no_PC) and with a double section PC (2PC) in the case of 300 µm long SOAs with an injected current of 30 mA. The PDG is drastically reduced when the PC is placed halfway two SOAs; $P_{TE} - P_{TM}$ for $\lambda = 1.55$ µm goes from 17 dB (no_PC) to only 0.35 dB (2PC).

Fig. 4.16 [5]shows a comparison between two PI-SOA devices with a double section PC, but with different SOA lengths (300 µm and 500 µm). The PDG is below 0.9 in both cases. The graph in Fig. 4.17(a) shows $P_{TE} - P_{TM}$ as a function of the wavelength, for two PI-SOA devices (300 µm long SOAs, 30 mA of injected current): one with a double section PC (2PC) and the other with a single section PC (PC). Even though both devices show a low PDG, the double section converter has an improved performance with a PDG below 0.4 dB over the C band.

The last graph is an estimation of the averaged PC conversion efficiency C, based on the measurement results, over the C band. The conversion efficiency C has been calculated as follow.

We start from the equations of the output power of a PI-SOA structure (Section 2.4). Dividing eq. 2.8 by eq. 2.9, if $C = 0$:

$$\frac{P_{out_{TEin}}}{P_{out_{TMin}}} = \frac{G(TE)^2}{G(TM)^2} = a \tag{4.1}$$

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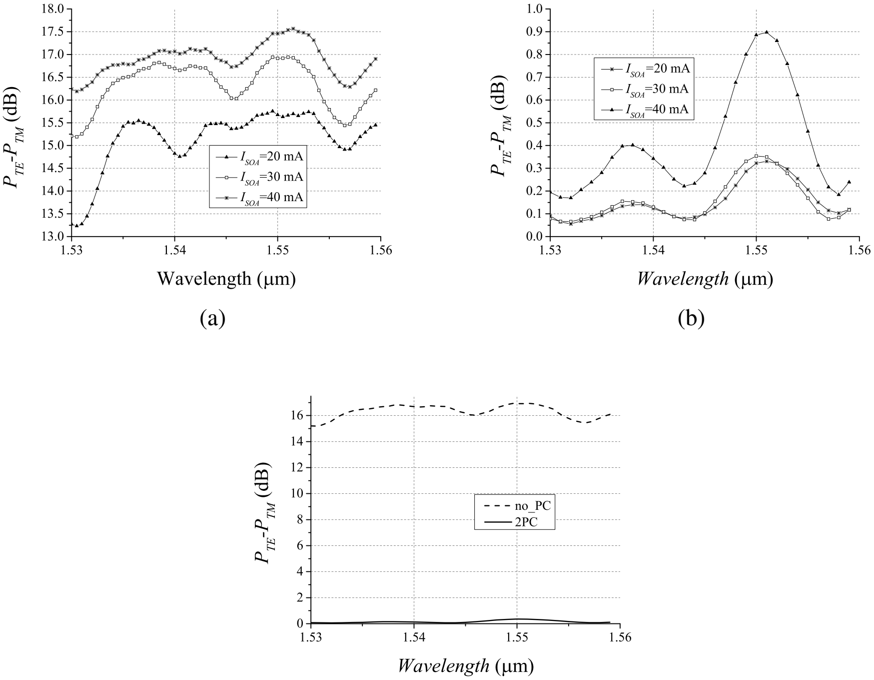
[5] The apparent oscillations in the curves could point to a reflection cavity in the circuit, with a cavity length of around 20 um. However, such a cavity has as yet not be identified with certainty.



(a)

(b)

Figure 4.15: (a) $P_{TE} - P_{TM}$ (dB) as a function of the wavelength (μm) for a 300 μm long SOAs test structure without PC and (b) with the insertion of a double section PC, for different current settings. (c) Comparison between the PDG of a test structure without PC (no_PC) and with a double section PC (2PC) as a function of the wavelength (μm) (300 μm long SOAs, 30 mA of injected current).

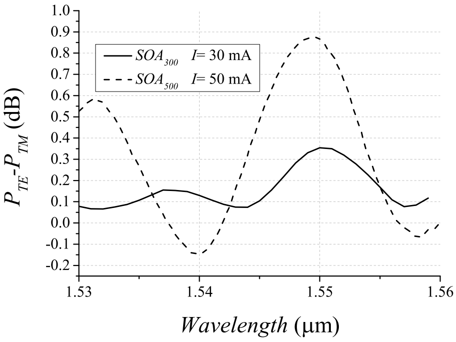


Figure 4.16: Comparison between the polarization extinction ratio $P_{TE} - P_{TM}$ (dB) of a test structure with a double section PC as a function of the wavelength (µm), for different SOA lengths.

and if $C \neq 0$:

$$\frac{P_{out_{TEin}}}{P_{out_{TMin}}} = \frac{CG(TE)G(TM) + (1-C)G(TE)^2}{CG(TE)G(TM) + (1-C)G(TM)^2} = b \tag{4.2}$$

where $P_{out_{TEin}}$ is the PI-SOA output power when the input mode is TE, and $P_{out_{TMin}}$ is the PI-SOA output power when the input mode is TM. Therefore b can be written as:

$$b = \frac{C\sqrt{a} + (1-C)a}{C\sqrt{a} + (1-C)} \tag{4.3}$$

hence C is calculated as:

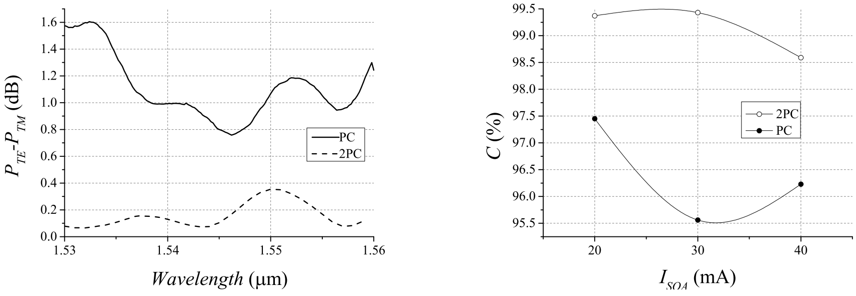
$$C = \frac{a-b}{a-b+b\sqrt{a}-\sqrt{a}} \tag{4.4}$$

For a and b averaged values over the C band are taken.

For different current settings, the polarization conversion is between 98.5% and 99.5% in the case of the double section PC, whilst it is between 95.5% and 97.5% for the single section PC. The result confirms the tolerant properties of the double section converter. The averaged C, determined in this way, is the minimum estimated polarization conversion, assuming that the two gain sections of the PI-SOA device are identical.

The observed current dependence in Fig.4.17(b) indicates that the two gain sections are not fully identical, implying that the actual conversion is at least equal to the maximum of these curves.

The comparison between a passive test structure and a test structure with two 300 μm SOAs (both without PC) shows a gain of each SOA of 10 dB for TE mode and 3 dB for TM mode. Comparing a test structure with a double section PC and and a test structure without PC (both with 300 μm SOAs), a device insertion loss below 0.5 dB has been estimated.



(a) (b)

Figure 4.17: (a) Comparison between $P_{TE} - P_{TM}$ (dB) of PI-SOA (300 μm long SOAs, 30 mA of injected current) with the insertion of a single section PC (PC) and a double section PC (2PC), as a function of the wavelength (μm). (b) Estimated minimum polarization conversion efficiency C (averaged over the C band) as a function of the SOA injected current (I_{SOA}(mA)), for a PI-SOA with a single section PC (PC) and a double section PC (2PC).

4.4 Conclusion

An experimental device such as a polarization converter can be post-processed and tested in a PIC (Chapter 3). In this chapter two different PC fabrication techniques have been presented, together with the device measurement results. The first generation PC characterization shows that the polarization dependence of two SOA's in series reduced from 14 dB to 3 dB with a single section PC in-between, indicating the presence of a sizable polarization conversion. However, due to the presence of a guiding layer undercut and to the difficulty of achieve a device within the designed tolerances, a full device characterization was not possible.

In order to overcome the problems encountered in the first generation process, and to fabricate a tolerant double section PC, a second fabrication process flow has been developed. The new process allows for a fabrication where the PC dimensions are independent of the EBL alignment. The accuracy is only related to the first ICP etching used to lower the top cladding to the PC top height, and this can be accurately controlled within 10 nm.

Measurements results show that the PDG is drastically reduced, with the insertion of a double section PC between two SOAs in series, from 17 to 0.35 dB ($\lambda = 1.55$ μm). Moreover, the better performance of the double section PC has been confirmed, since for $\lambda = 1.55$ μm the single section shows a PDG of 1.1 dB, and the minimum estimated conversion efficiency C is above 99.5% in the case of the double section PC, whilst it is above 97.5% for the single section PC. The estimated PC device insertion loss is below 0.5 dB.

Chapter 5

BOTDR circuit

In this chapter we present a Brillouin Optical Time Domain Reflectometry (BOTDR) read-out unit whose optical components are integrated in a photonic circuit (PIC). The circuit has been designed using commercial BOTDR systems [33, 34] as a reference for the specifications. Due to bulk optics, these strain analyzers are expensive (> 50.000 euro) and heavy (20 kg). The aim is to include all the optical functionalities in a PIC and to generate optical pulses to scan the fiber and detect the Brillouin backscattered light. The PIC has been fabricated by Oclaro within an MPW run, thus with the possibility of cost-sharing among the platform users. Section 5.1 shows the circuit design and describes the working principle, focusing on the optical components. The measurements of the optical structures are reported in Section 5.2 together with the characterization of the BOTDR circuit set to one of its operational modes. Conclusions are drawn in Section 5.3.

5.1 Working principle and design

When light is injected into a fiber with low optical input powers, it encounters acoustic phonons which are generated by thermal agitation. In this regime, spontaneous Brillouin scattering takes place from the interaction between the light and acoustic waves that propagate along the fiber. Since the phonons represent sound waves, the scattering can be interpreted as a reflection from a moving grating. Therefore, the resulting signal is shifted in frequency by an amount ($\sim$11 GHz), which depends on the velocity of sound in the fiber. In the case of spontaneous scattering, the thermally activated phonons do not have a preferred direction of movement, and thus equally strong reflected signals can be found with positive and negative frequency shifts. However, at higher powers, due to electrostriction, the lower frequency Brillouin signal, corresponding to a sound wave that co-propagates with the light, is amplified, while the higher frequency signal is depleted. This is the regime of Stimulated Brillouin Scattering (SBS). Because the induced frequency shift depends on the velocity of sound, which in turn depends on the temperature and strain in the optical fiber, Brillouin scattering is very well suited to determine these properties [35]. In order to separately detect strain and temperature variations, usually two fibers are applied to the structure, one connected to a protective tube, the other loosely placed in it. To extract information about the distribution of strain and temperature, the spectrum of the Brillouin scattered light needs to be determined as a function of time delay after launching an optical pulse (Fig.5.1). Fiber strain and temperature variations shift the Brillouin frequency (493 MHz/% and 1 MHz/ºC [36] respectively, @ λ=1550), thus a spectral analysis of the Brillouin signal combined with OTDR provides localized information of the fiber condition, which can be used for a distributed monitoring of large constructions.

The BOTDR PIC[1] is designed in a 6x6 mm cell (Fig.5.2). The mask design includes the full BOTDR circuit and test structures. The optical passive circuit is based on deeply etched 1.5 μm wide waveguides in an InP/InGaAsP/InP double heterostructure (See section 2.2, Fig.2.2). The aim is to generate optical pulses to scan the fiber and detect the Brillouin backscattered light. The circuit has been designed following the specifications of an existing BOTDR system [33] and adapting the requirements to available optical components.

In the following sections a number of subcircuits in the PIC design will be explained.

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[1] The circuit has been designed by R. F. Klein Breteler, M. Felicetti, B. Sasbrink and J. J. G. M. van der Tol.

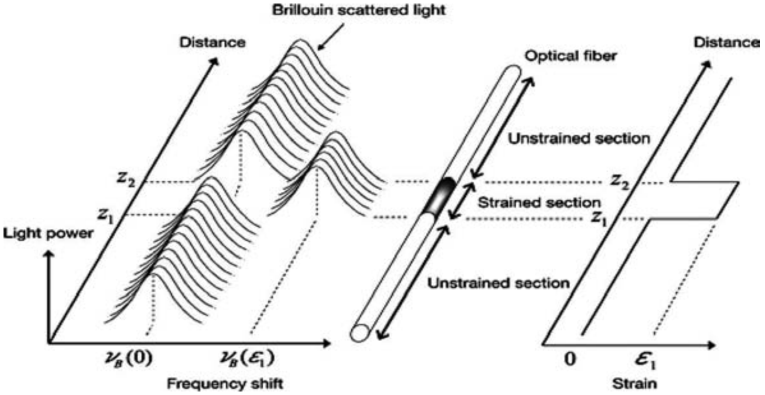

Figure 5.1: Principle of the use of Brillouin scattering for determining the strain distribution along a fiber. In the strained sections, the Brillouin frequency ν_B is shifted by a quantity ε proportional to the strain and temperature variation in the fiber. Distance is determined from the time delay of the backscattered light with respect to the injected pulse.

5.1.1 Switching network

The BOTDR circuit (Fig.5.3) allows for three distinct measuring methods of strain and temperature variations in an optical fiber thanks to an MZI switching network [37]. Each of these methods is used in BOTDR measurements, since they they all have their specific advantages and disadvantages. The chip is designed for a broad applicability, and therefore supports all possible BOTDR systems. The BOTDR switching network consists of two MZI switches, Switch_1 and Switch_2, with 500 µm long phase sections, that enable the use of these different methods. The MZI switches connect two tunable DBR lasers (TL_1 and TL_2, separated by about 11 GHz in frequency), a coherent receiver and a sensing fiber. The first MZI selects the pump laser; the second one allows for the transition from the pulse generation state, when the pump light is sent into the fiber, to the measuring state, when the backscattered light is sent to the coherent receiver. Tab.5.1 gives and overview of the switching network configuration in the three different methods that are discussed below.

Method 1

Switch_1 (cross state) selects TL_1 as operational laser. By shortly switching (during 25 ns) Switch_2 from the cross to the bar state, a pulse is created and injected into

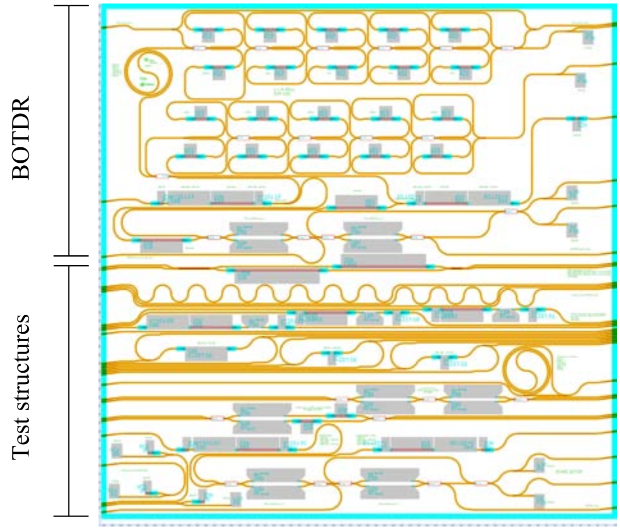

Figure 5.2: BOTDR and test structures mask design.

Method	Pulse creation		Measuring state		
	Switch_1	Switch_2	Switch_1	Switch_2	Detection
1	X	=	X	X	heterodyne
2	=	=	X	X	homodyne
3	X	=	X	X	heterodyne + BOTDA

Table 5.1: Switch configuration during the pulse creation and measuring state for the different measuring methods. X indicates the cross state and = the bar state

the fiber (side A). Then Switch_2 (cross state) selects the light from TL_1 to enter the coherent receiver. The resulting beating with the Brillouin backscattered signal is detected and the electronic signal with a frequency of about 11 GHz is mixed with a local electronic oscillator to detect the Brillouin frequency shift.

Method 2

TL_2 (up-shifted in frequency w.r.t. TL_1) is used to create the pulse (Switch_1 is in the bar state). To inject a pulse into the fiber, Switch_2 is shortly switched from the cross to the bar state. TL_1 is used as well in a frequency locking configuration. The frequency spacing of the locked lasers is fixed by an electronic feedback loop.

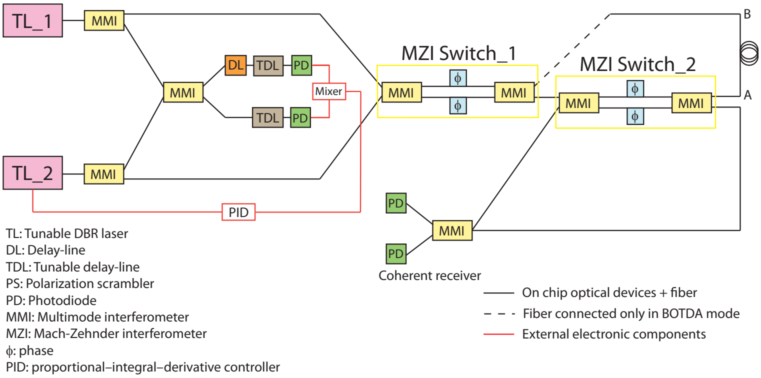

Figure 5.3: BOTDR working principle scheme.

For this, light from the two lasers is split over two branches of a tunable delay line (TDL) in a 2×2 MMI coupler and then detected with two photo-diodes. The phase difference φ between the laser beating signals from the detectors is determined with an electrical mixer and used as an input for a PID controller [38]. The controller minimizes the phase difference by adjusting the laser frequency of the tunable laser TL_2 through current injection in one of the DBR gratings. The phase difference of the two detected signals is minimal if the length difference of the two branches equals half the beat-length of the mixed light signals; Fig. 5.4 shows the laser locking principle scheme. To shift one signal by a half beat-length we use a fixed spiral delay (DL) and a tunable delay line (TDL) which is used to tune the frequency of TL_2 over a range of 2 GHz around the Brillouin frequency. The frequency difference between the two lasers is:

$$\Delta f = \frac{c}{2n_{eff}L} \tag{5.1}$$

where c is the speed of light in vacuum, n_{eff} is the effective index of the waveguide, and L is the length of the tunable delay. The tunable delay line working principle is described in section 5.1.5.

During the measurements, both switches are set to the cross state. The light from TL_1 (now with Switch_1 in the cross state) is mixed with the backscattered light in the coherent receiver and homodyne detection is performed.

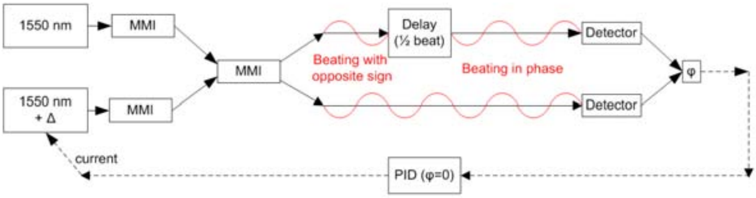

Figure 5.4: Principle of the laser frequency stabilization scheme.

Method 3

The chip has an extra output available to connect to the other side of the fiber (side B). This allows a third mode of operation: BOTDA (Brillouin Optical Time Domain Analysis). Light that matches the frequency of the Brillouin backscattered light enters from the side B of the fiber. This leads to an amplification of the Brillouin backscattering from the pulses.

TL_2 is used to inject light from side B in the fiber, while TL_1 enters Switch_2, which creates the pulse by shortly switching from cross to bar state. The frequency difference between the lasers is controlled with the TDL, as in method 2. The detection uses TL_1 as local oscillator, and is heterodyne as in method 1.

5.1.2 Laser locking feedback system analysis

The mathematical description[2] of the feedback system (Fig.5.4), used in the BOTDR operational methods 2 and 3, is given below. It will be used in Section 5.2.5 to model the effect of crosstalk that appears in the digital delay-line.
The optical wave generated in TL_1 is described by:

$$A(t) = A_1 e^{i\omega t} \tag{5.2}$$

Similarly, the wave associated with TL_2 is:

$$A(t) = A_2 e^{i(\omega+\Omega)t} \tag{5.3}$$

where Ω is the frequency difference between the lasers. Note that, since the scheme is described in terms of time delay, the propagation term $e^{i\beta z}$ is identical in all wave expressions, and can therefore be removed from the equations. The signals from eqs.5.2 and 5.3 are mixed in the 2x2 MMI coupler, which splits the light equally

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[2] Mathematical description by dr. J. J. G. M. van der Tol

from each input over the two output ports. The cross-coupled signal experiences a phase shift of π/2 radians with respect to the bar-coupled signal. Thus, the wave amplitude in the upper and lower output ports in Fig. 5.4 can be found as follows:
Upper path

$$A_{up}(t) = \frac{1}{\sqrt{2}}\left(A_1 e^{i\omega t} + iA_2 e^{i(\omega+\Omega)t}\right) \tag{5.4}$$

Lower path

$$A_{low}(t) = \frac{1}{\sqrt{2}}\left(iA_1 e^{i\omega t} + A_2 e^{i(\omega+\Omega)t}\right) \tag{5.5}$$

Here, i indicates the π/2 coupler induced phase shift. In the upper path the signal is delayed by an amount Δt, so the amplitude becomes:

$$A_{up}(t) = \frac{1}{\sqrt{2}}\left(A_1 e^{i\omega(t+\Delta t)} + iA_2 e^{i(\omega+\Omega)(t+\Delta t)}\right) \tag{5.6}$$

The lower path signal does not change from the expression given in eq.5.5. The signals from both paths are then detected and converted in electrical signals. The current obtained from the detector is proportional to the power P (by $I = RP$, with R the responsivity), which in turn is proportional to the product of the amplitude with its complex conjugate. Leaving out all the proportionality constants, we can find the relation between the two beating signals B_1 and B_2. For the upper path:

$$B_1 = A_{up}(t)A^*_{up}(t) = \frac{1}{2}\left(A_1 e^{i\omega(t+\Delta t)} + iA_2 e^{i(\omega+\Omega)(t+\Delta t)}\right)\left(A_1 e^{-i\omega(t+\Delta t)} - iA_2 e^{-i(\omega+\Omega)(t+\Delta t)}\right) \tag{5.7}$$

If we consider the output powers of the lasers as $P_1 = A_1^2$ and $P_2 = A_2^2$ respectively, eq.5.7 can be written as:

$$B_1 = \frac{1}{2}(P_1 + P_2) - \sqrt{P_1 P_2} sin\left[\Omega\left(t + \Delta t\right)\right] \tag{5.8}$$

A similar expression is found for the lower path:

$$B_2 = \frac{1}{2}(P_1 + P_2) + \sqrt{P_1 P_2} sin\left[\Omega t\right] \tag{5.9}$$

The two electrical signals B_1 and B_2 go into an electrical mixer. After filtering out the DC-components ($1/2(P_1 + P_2)$ in both), the sine terms are multiplied. The result is C:

$$C = P_1 P_2 \left(-sin\left[\Omega\left(t+\Delta t\right)\right] \times sin\left[\Omega t\right]\right) \tag{5.10}$$

Using the trigonometric sum formula $sin\left[\Omega\left(t+\Delta t\right)\right] = sin\left[\Omega t\right] cos\left[\Omega \Delta t\right] + sin\left[\Omega \Delta t\right] cos\left[\Omega t\right]$ in eq.5.10 and averaging over time[3], the final output of the mixer is:

$$C = -0.5 P_1 P_2 cos\left[\Omega \Delta t\right] \tag{5.11}$$

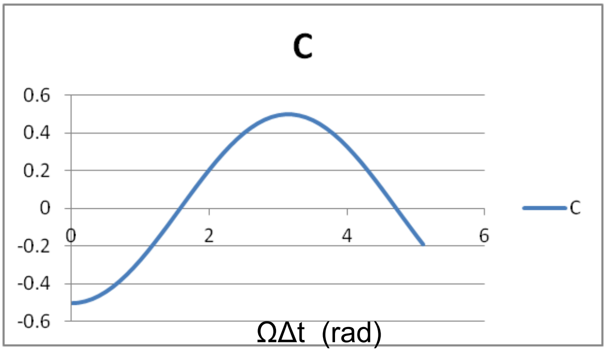

Figure 5.5: Output signal of the mixer, versus $\Omega\Delta t$

This function is shown in Fig.5.5. The operation point can be chosen on one of the zero crossings of this curve, e.g. on π/2 radians. Any deviation from the condition $\Omega\Delta t = \pi/2$ results in an error signal which will be used to correct the frequency of TL_2 by adjusting the current through its DBR grating. Thus a stabilization of Ω is obtained. Furthermore, by adjusting Δt the frequency difference can be adjusted, so that the Brillouin spectrum can be scanned by changing Δt. However, in the digital tunable delay-line, spurious interfering signals influence the stabilization system. The crosstalk generated by the interfering signals is analyzed in Section 5.1.5.

5.1.3 Coherent receiver

During the measuring state described in Section 5.2.1, two optical signals (one from the laser TL_1 as the local oscillator, the other the backscattered signal from the fiber) enter the coherent receiver, included in the BOTDR design (Fig.5.3). Fig.5.6 shows a schematic of the coherent receiver. After mixing, two output signals are obtained from the 2x2 MMI coupler. The coherent receiver consists of two photo-detectors

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[3] The linear sine and cosine terms depending on t drop out and the sin^2 and cos^2 terms become 0.5

(PD) with a bandwidth which is estimated to be larger than 10 GHz by the foundry. These two signals are detected and electronically subtracted (balanced detection). This provides a high sensitivity and low noise detection.

The beating signal is detected and generates an electronic signal with a frequency of about 11 GHz that is down-converted with a local electronic oscillator and filtered to detect the Brillouin frequency.

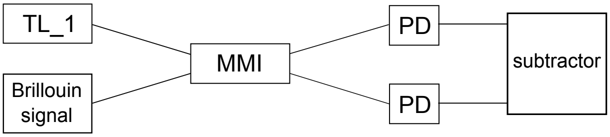

Figure 5.6: Coherent receiver schematic.

The mathematical model of the coherent system is very similar to the one of feedback system, presented in the previous section. The optical wave generated by TL_1 is described by:

$$A(t) = A_1 e^{i\omega t} \tag{5.12}$$

and the Brillouin signal is described by:

$$A(t) = A_B e^{i(\omega+\Omega)t+\varphi} \tag{5.13}$$

where Ω is the frequency difference, equal to zero in case of homodyne detection, and φ the phase difference. Here as well the propagation term $e^{i\beta z}$ is identical in both wave expressions, and can therefore be discarded. The signals from eqs. 5.12 and 5.13 are mixed in the 2x2 MMI coupler in the same way as the signals from eqs. 5.2 and 5.3. Applying the same mathematical model that describes the mixing of the signals as in Section 5.2.1, but now without time delays, the following expressions for the lower (1) and upper (2) MMI output ports are derived:

$$B_1 = \frac{1}{2}(P_1 + P_B) - \sqrt{P_1 P_B} sin\left[\Omega t + \varphi\right] \tag{5.14}$$

$$B_2 = \frac{1}{2}(P_1 + P_B) + \sqrt{P_1 P_B} sin\left[\Omega t + \varphi\right] \tag{5.15}$$

The two electrical signals B_1 and B_2 are fed into an electrical comparator (subtractor), whose output is the difference signal C:

$$C = 2\sqrt{P_1 P_B} sin\left[\Omega t + \varphi\right] \tag{5.16}$$

Balanced detection noise reduction

The use of a balanced receiver for the coherent detection leads to a reduction of both the effect of power fluctuations from the local oscillator and detector noise. To see the effect of the balanced detection on power fluctuations from the local oscillator, we compare the detection of the signal from eq. 5.14 directly (without balanced detection), with the detection of the signal from eq. 5.16. Assume there is a noise δP_1 on the power of the local oscillator. Then the deviation in B_1 becomes:

$$\delta B_1 = \left[\frac{1}{2} - \frac{1}{2}\sqrt{\frac{P_B}{P_1}} sin\left[\Omega t\right]\right] \delta P_1 \tag{5.17}$$

Since the power of the local oscillator is much larger than the small BOTDR signal, $P_1 \gg P_B$, the second term can be neglected. Thus we find that $\delta B_1 = 0.5\delta P_1$. However, if we look at the result of the balanced detection, the variation in the signal C becomes:

$$\delta C = \left[-\sqrt{\frac{P_B}{P_1}} sin\left[\Omega t\right]\right] \delta P_1 \approx 0 \tag{5.18}$$

So the use of balanced detection in the coherent receiver, which removes the constant power terms P_1 and P_B, also removes the effect of power fluctuations from the local oscillator.

Concerning the detector noise, [39] shows that the signal to noise ratio (SNR) in case of coherent balanced detection, with the noise coming from the detector, is at least two times as high as for a direct detection scheme.

5.1.4 Laser

The two frequency locked lasers are tunable DBR lasers. Both consist of three separate sections: a front DBR grating, a gain section, and a rear DBR grating (Fig.5.7). The front and rear grating provide the laser cavity. The rear grating should be long enough to ensure high reflection and single-mode operation, while the short front grating is used as a broadband low reflector to provide the output of the laser. The laser parameters have been optimized taking into account the foundry rules. In order to achieve a high reflectivity, we choose a rear grating with the maximum allowed length of 500 µm.

Figure 5.7: Schematic of the tunable DBR laser.

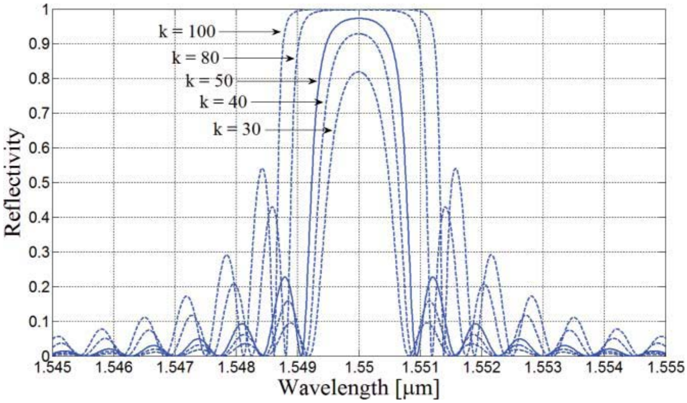

Figure 5.8: Reflectivity of a 500 μm long DBR grating versus the wavelength (μm) for different values of the coupling coefficient k.

Fig. 5.8 shows the calculated reflectivity spectrum of the rear DBR grating for different values of the coupling coefficient k [40]. The central wavelength of the reflectivity spectrum is the wavelength that is most strongly reflected from the grating (i.e., the Bragg wavelength λ_B). The grating period of TL_1 is chosen as $\Lambda_1 = 237.51$ nm in order to have $\lambda_B = 1.55$ μm. The choice of k is a trade-off between a high reflection for the rear grating and the single-mode behavior of the laser. Simulation results obtained by modeling the laser cavity show that $< 10\%$ suppression of the side modes, with respect to the lasing mode, is enough to achieve single-mode operation [41]. Therefore, the mode spacing should be at least comparable to (or larger than) the half width at 90% of the maximum reflection of the DBR grating. The mode spacing is calculated as follows:

$$\Delta\lambda = \frac{\lambda_B^2}{2(N_{g_{SOA}} L_{SOA} + N_{eff_{DBR}}(L_{eff_{rear}} + L_{eff_{front}}))} \tag{5.19}$$

where $N_{g_{SOA}}$ is the group index of the semiconductor optical amplifier (SOA) waveguide, L_{SOA} is the length of the SOA in μm, $N_{eff_{DBR}}$ is the effective group index of the passive waveguide structure used for the gratings, and $L_{eff_{rear}}$ and $L_{eff_{front}}$ are respectively the effective lengths of the rear grating and the front grating. These effective lengths define the penetration depths of the light into the grating mirrors.

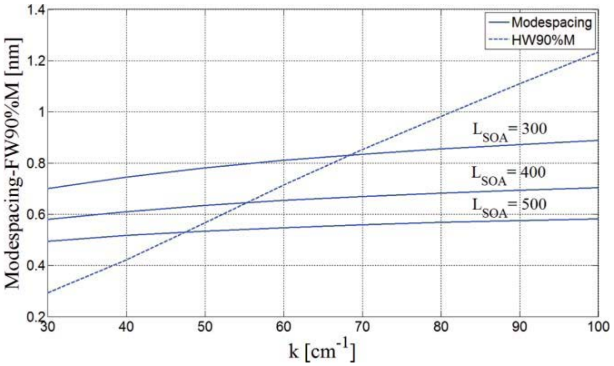

Figure 5.9: Mode spacing compared to the half width at 90% of the maximum (HW90%M) as a function of k for a 500 μm long DBR rear grating and a 100 μm DBR front grating, both with λ_B = 1.55 μm. The mode spacing is calculated for different SOA lengths (μm).

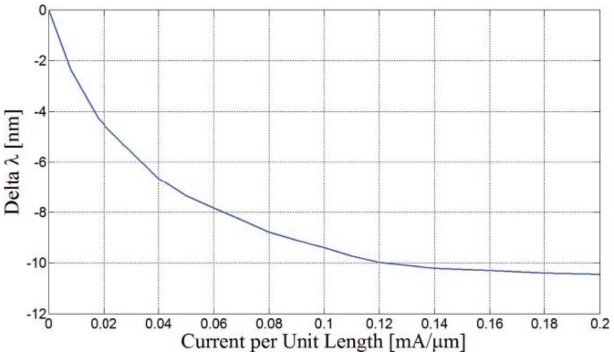

Figure 5.10: Change in λ as a function of the tuning current per unit length (Oclaro design manual[24]).

Fig.5.9 compares the mode spacing and the half width at 90% of the maximum, as a function of k for different SOA lengths. From Fig.5.8, it follows that k should be> 40 cm^{-1} to have a high reflectivity for the rear grating. However, Fig.5.9 shows that for a k > 50 cm^{-1}, the bandwidth of the reflectivity spectrum becomes too wide to reliably expect single-mode operation with a long SOA. On the basis of these considerations, we choose $k = 50\ \mathrm{cm}^{-1}$, resulting in the highest reflection while single mode behavior can still be expected. The length of the front grating is chosen to be 100 μm long so that with $k = 50\ \mathrm{cm}^{-1}$, it has a reflectivity equal to 20%. The reference laser TL_1 operates at a wavelength λ_B = 1.55 μm and is used for the coherent detection of the Brillouin signal backscattered from the fiber. TL_2 is up-shifted in frequency with respect to the reference laser by 8 GHz (Λ_2= 237.51 nm)[4]. Tuning is obtained by current injection in the rear grating. In Fig.5.10, the change in λ as a function of the tuning current density is given. From this graph, it can be learned that only very small current (22.9 mA for a DBR grating of 500 μm length) is needed for tuning of the lasers over the required frequency range. Therefore, free carrier losses can be neglected in the gratings. Temperature variations in the lasers do not influence the accuracy of the frequency shift detection in the fiber. The Brillouin spectrum is scanned with the difference frequency of the two tunable lasers; thus, this difference must be stable. Temperature variations can influence a single laser (0.1 nm wavelength shift per degree temperature change), but because the two lasers are identical, realized on the same chip at short distance of each other, and their frequency difference is controlled by a locking system, a stable frequency difference can be expected.

5.1.5 Tunable delay line

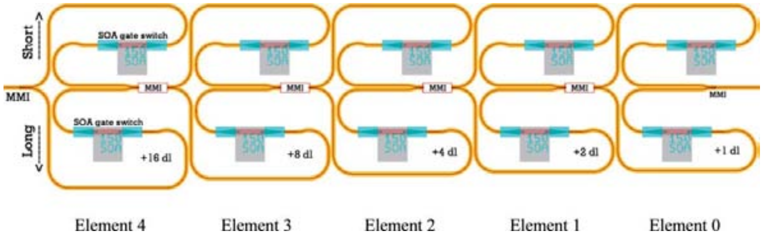

Figure 5.11: Part of the switchable delay line, showing 5 of the 10 elements.

In order to use the laser locking system (Section 5.1.2) for tuning the frequency difference of TL_2 over a range of 2 GHz around the Brillouin frequency, the delay should also be tunable. This is achieved with a 10-bit switched delay line. To achieve a broadband delay line on a chip that has tuning capabilities, a switchable structure

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[4] Since the gratings are processed together, an accuracy of 10 pm in the difference of the grating period can be expected. The actual frequency difference between TL_1 and TL_2 can however always be corrected using current injection in the gratings.

has been designed that allows stepwise tuning of the delay by directing light through a network of paths (Fig. 5.11). The circuit consists of a chain of delaying elements connected together. In each delaying element light is split over two optical paths with an MMI splitter. Each path contains a SOA that can be operated as a gate switch: either blocking or amplifying the light. By controlling the SOAs, light can be selected from either the longer or shorter path of the delay element. The path-length difference is related to the element number I as follows:

$$L = \delta l \cdot 2^{I} \tag{5.20}$$

where δl is equal to the length difference in element 0. The optical path length of a chain consisting of 10 delaying elements can then be tuned over 1024 different values in steps of δl. Each of the 1024 delay lengths corresponds to a unique setting of the SOA gate switches, similar to the binary counting system (with "1" implying the longer path and "0" the shorter one in an element). Thus, to set a desired delay length, control of 20 SOA gate switches is required. In the chip design, we have implemented two five-element delay lines into both branches of the locking circuit. A delay in the lower branch can be viewed as a negative delay. Together they act as a 10-element delay line. Optimizing the layout of the elements resulted in a delay line covering an area of 4×2 mm. This is shown in the layout of the chip design in Fig. 5.12.

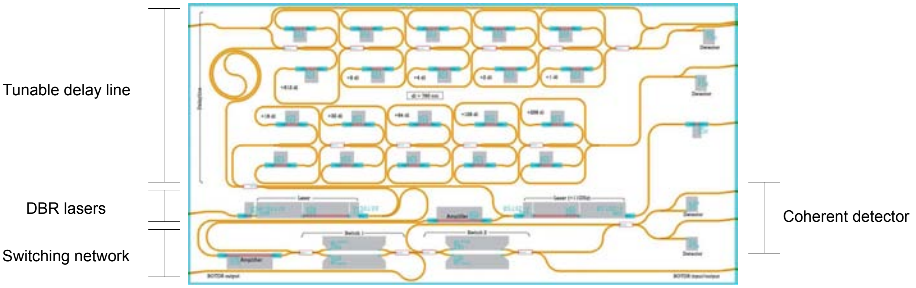

Figure 5.12: Layout of the integrated BOTDR chip.

The smallest delay step δl is chosen to be 0.76 μm, which corresponds to steps of 2 MHz between subsequent frequency settings. This frequency spacing matches the accuracy of modern BOTDR systems and corresponds to a strain resolution of 0.004% or a temperature resolution of 2 ºC in the BOTDR or BOTDA measurement. With a frequency step size of 2 MHz, the complete desired frequency range of 2 GHz can be achieved with a delay line consisting of 10 elements. A fixed spiral delay is added to one of the arms (DL) of the delay line to set the center of the tuning range at 11 GHz.

5.2 Characterizations

Half of the BOTDR mask design (Fig.5.2) is dedicated to test structures for components used in the BOTDR circuit. These test structures include basic building blocks (BBs) (DBR grating, photo-diode, SOA[5]), composite building blocks (DBR tunable laser, waveguide bends) [3] and a BOTDR sub-circuit. This section is dedicated to the characterization of these components, to provide an understanding of the full circuit capabilities and limits. Fig.5.13 shows the BOTDR PIC mounted on a copper chuck and ready for the measurements, with probes and coupling fibers[6].

5.2.1 DBR grating

The DBR grating test structure (Fig. 3 (a)) allows for the characterization in terms of reflectance (R) and transmittance (T), while correcting for the input and output losses α_i (i=1,2,3,4). T and R are calculated as follows:

$$T = \frac{1}{1+\sqrt{\frac{P_{23}P_{14}}{P_{13}P_{24}}}} \tag{5.21}$$

and

$$R = 1 - T \tag{5.22}$$

Here it is assumed that the losses in the grating can be neglected. Measurement results agree well with simulations: R is about 98% for the 500 µm long grating (Fig.5.15 (a)) and 20% for the 100 µm long one (Fig.5.15 (b)). The measured λ_B is blue-shifted by about 1 nm with respect to the simulated one. This is not relevant for the BOTDR application, because we are only interested in the frequency difference between the pump laser and the backscattered light. The ripples in R and T spectra are caused by reflections from the MMIs that are estimated to be around -22 dB. The cavity length has been calculated as follows:

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[5] Although the SOA building block has been included in a different test chip, here the results are reported for the relevant connection with the BOTDR performance.

[6] The measurements results have been presented in [42, 43]

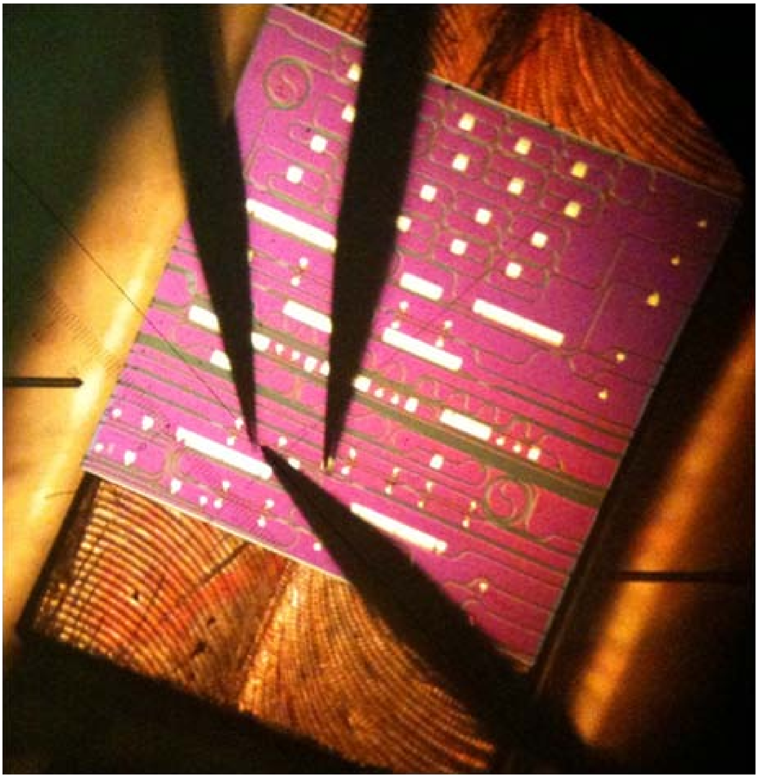

Figure 5.13: BOTDR PIC bonded with epoxy on a copper sub-mount for the measurements.

$$L = \frac{\lambda^2}{2n_g\Delta\lambda} = 535\,\mu\text{m} \tag{5.23}$$

where $\lambda = 1.55$ µm, n_g=3.74 is the group index and $\Delta\lambda$=0.6 µm is the ripple period. This cavity length corresponds with the distance between the DBR and the MMI. The linear change in λ_B as a function of the temperature is 1nm/7°C; the change in λ_B as a function of the current is shown in Fig. 5.16. The measured λ shift is about 30% less than the simulated one[7], which is possibly due to a deviation in the fabrication of the circuit.

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[7] The simulated curve has been obtained using the Oclaro specifications in the design manual

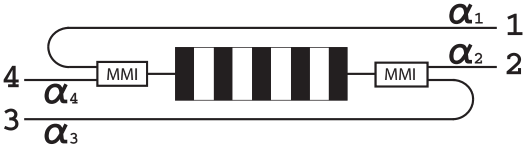
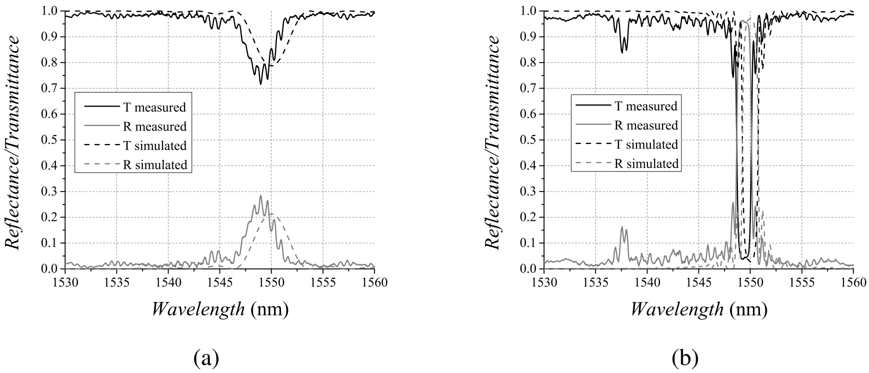


Figure 5.14: Schematic of the DBR grating test structure.



(a)

(b)

Figure 5.15: 100 µm (a) and 500 µm (b) long DBR gratings simulated and measured Reflectance/Transmittance as a function of the wavelength (nm).

5.2.2 DBR laser

The DBR laser test structure consists of a 500 µm long rear DBR grating, a 500 µm long gain section and a 100 µm long front DBR grating, so it is identical to the designed laser from Section 5.1.4. The tunable laser has been characterized in terms of the L-I curve at different temperatures. The laser output power coupled into a fiber is shown in Fig. 5.17. At 10º C the L-I curve shows the highest output power: 4.5 mW for 150 mA injected in the SOA. The threshold current is 14 mA. The output power is too low for the application, where at least 10 mW[8] is required. However, at the

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[8] If an input pulse (25 nm) of 10 mW is injected in a single mode fiber (50 km and SBS gain factor $1.68 \cdot 10^{-11}$ m/W) the power level of the backscattered Brillouin signal is few pW. The signal is

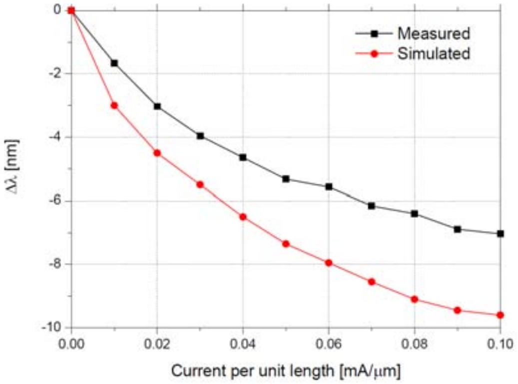

Figure 5.16: Measured and simulated change in the R/T peak wavelength (Δλ) as a function of the current per unit length (mA/µm).

output of the tunable lasers of the BOTDR circuit booster amplifiers has been placed in order to improve the output power level (about 15 dB gain). Fig. 5.18 shows the laser wavelength shift which is 0.7 nm/mA for a SOA length of 500 µm. This means that 22.9 µA is needet to tune the frequency over a 2 GHz range.

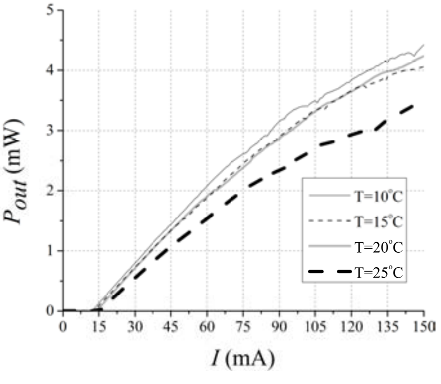

Figure 5.17: L-I curves for different temperature settings

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then mixed with the local oscillator, with a power level of 10 mW, for the coherent detection. VPI has been used for the simulations which have been performed by R. K. Breteler.

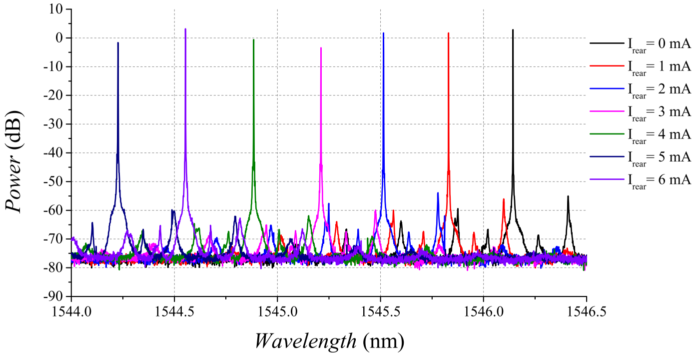

Figure 5.18: Current tuning of the DBR lasers by injecting current on the rear grating (I_{SOA}= 70 mA).

5.2.3 Spiral delay

Since one laser is shifted in frequency by about 11 GHz with respect to the other laser, the beating signals in the delay line have a frequency of 11 GHz. The period of a signal at 11 GHz is 90 ps; in order to keep the two laser beating signals in the laser locking system of Fig. 5.4 at the same phase, we need to delay one of them by a half beat. This is achieved by using a spiral waveguide; the spiral included in the BOTDR circuit gives a true time delay of:

$$t = \frac{Ln_{eff}}{c} = 45.5\,\text{ps} \tag{5.24}$$

with $L = 4.04$ mm the spiral length, n_{eff}=3.38 the TE effective index (@ λ=1550 nm) and $c = 3 \cdot 10^8$m/s the speed of light in vacuum. The spiral delay has been characterized using a test structure (Fig. 5.19 (a)) which consists of a waveguide that splits in two paths, a straight one and a spiral one; then the two paths recombine. In this way, we can detect the relative group delay between a pulse traveling along the straight path and a pulse traveling along the spiral path.

The measured delay from the test structure is shown in Fig. 5.19 (b)[9]. The blue line represents the pulse recorded directly from a broad band source, whilst in red there is the test structure output. Since the measurement is done with optical pulses, here the

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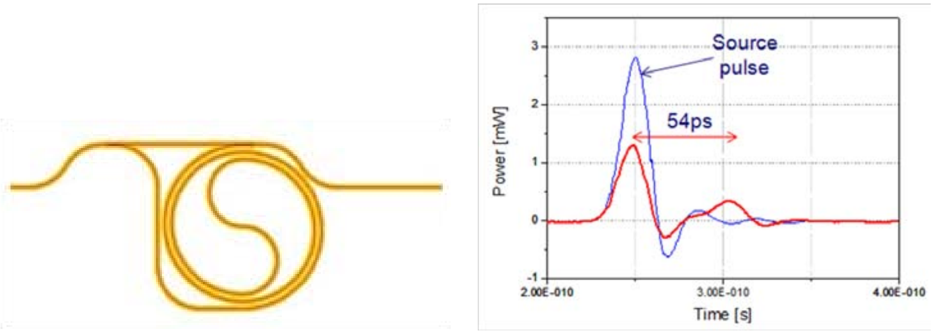
[9] The apparently negative power is due to the display voltage, which originates from receiver oscillations. The spiral delay test structure has been characterized by MSc A. Chighine

group delay is determined. The spiral gives a delay of 54 ps. The measured delay is in good agreement with the calculated group delay:

$$t = \frac{Ln_g}{c} = 55.07\,\text{ps} \tag{5.25}$$

with $L = 4.47$ mm the spiral length [10], n_g=3.69 the group index for deeply etched waveguide (@ λ=1550 nm) and $c = 3 \cdot 10^8$ m/s the speed of light in vacuum.

This result shows that there is sufficient control over the delay value to be used in the laser locking system of Section 5.1.2.



(a) (b)

Figure 5.19: (a) Spiral delay; (b) time delay given by the spiral.

5.2.4 Curved waveguides

Figure 5.20: Bends test structure.

The tunable delay-line of the BOTDR unit contains bends with 100 µm bending radii in order to fit into the 6x6 mm cell, whilst the foundry advices to have a bending radius ≥ 150 µm. The design choice could lead to polarization conversion in the bends, which can interfere with the operation of the laser locking system. For

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[10] The spiral test structure is longer than the spiral of the actual BOTDR circuit because it has to be connected with another waveguide to estimate the extra delay.

this reason we provide the design with test structures to investigate whether the polarization changes in the bends. We characterized three series of waveguide structures (Fig. 5.20), with a varying number of concatenated 90° bends: 8, 16 and 32. For 32 bends (the number used in the BOTDR delay-line) the total polarization conversion is found to be below 0.5% (Fig. 5.21).

The bends extra loss have been measured as well and they are 0.13 dB/90° for the TE mode and 0.15 dB/90° for the TM mode[11].

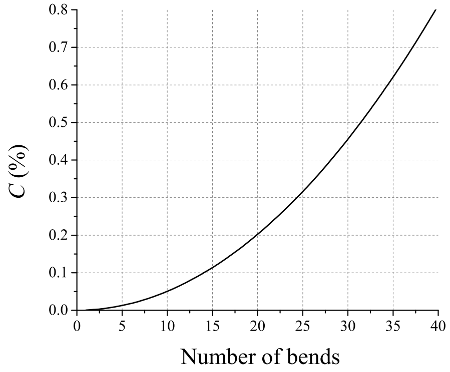

Figure 5.21: Conversion efficiency C versus the number of bends.

5.2.5 Tunable delay line SOA gates

The SOAs used to build tunable delay-line gate switches are characterized by a certain extinction ratio. Depending on this extinction ratio, spurious interfering signals can leak through the SOA set to block the light and affect the stabilization of the feedback system (Section 5.1.2). In this section, the crosstalk generated by the interfering signals of the delay-line SOA gates is analyzed and the SOA extinction ratio measurement results are reported.

The digital delay-line selects one out of 1024 paths with different lengths. The length differences between these paths corresponds to frequency steps of 2 MHz, which is only useful if these steps can be defined with an accuracy of 1 MHz or better. The frequency scan for obtaining the Brillouin spectrum is from 10 to 12 GHz, so the relative accuracy of the frequency definition, by the control feedback

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[11] The bends extra loss have been measured by MSc A. Chighine.

loop described in Section 5.1.2, is 1MHz/11GHz, or 0.9 x 10^{-4}. This implies that the relative error made on the set point (the zero crossing in Fig. 5.5) from the combined crosstalk signals should be less than this value. So the required accuracy is < 0.9 x 10^{-4} $\pi/2$, which is < 1.4 x 10^{-4}.

Single crosstalk signal

For simplicity we start with a single disturbing signal. This signal comes from one of the blocking gate switches (SOA-gates) and leaks into the selected path. We allow this disturbing signal to enter the lower path in the system shown in Fig. 5.4 (in reality the delay segments are split over both the upper and the lower path, so disturbing signals can occur on both, with similar effects). The amplitude of the disturbing signal, which is a weakened and additionally delayed version of the main lower branch signal, is given as:

$$A_d(t) = \frac{\varepsilon}{\sqrt{2}}\left(iA_1 e^{i\omega(t+N\delta t)} + A_2 e^{i(\omega+\Omega)(t+N\delta t)}\right) \tag{5.26}$$

with ε the strength of the disturbing signal, and $N\delta t$ the specific delay for this leaking path. This signal is added to the A_1 from eq.5.5, and the combination is photodetected. Since ε should be small ($\varepsilon \ll 1$), we can assume that only those terms which are linear in ε are of importance. This leads to the following result:

$$B_2^d = (A_l + A_d)(A_l + A_d)^* \approx A_l A_l^* + A_l A_d^* + A_l^* A_d = B_2 + XT \tag{5.27}$$

with B_2 the electrical signal given in eq.5.9, and XT the crosstalk term. This is evaluated from equations eq.5.5 and eq.5.26 to be:

$$\begin{gathered} XT = A_l A_d^* + A_l^* A_d = \varepsilon\left[A_1^2 cos\left(\omega N\delta t\right) + A_1 A_2 sin\left(\Omega t + \Omega\delta t + \omega N\delta t\right) + \right. \\ \left. -A_1 A_2 sin\left(-\Omega t + \omega N\delta t\right) + A_2^2 cos\left(\omega N\delta t + \Omega N\delta t\right)\right] \end{gathered} \tag{5.28}$$

Mixing B_2^d, as before, with the B_1 signal from the upper branch (eq.5.8), removing DC-terms and averaging over time (so that only the time dependent sin^2 and cos^2 terms are kept, being 0.5), results in the disturbed mixer output C^d as:

$$\begin{gathered} C^d = C + 0.5\varepsilon P_1 P_2 cos\left(\Omega\Delta t\right)\left[cos\left(\omega N\delta t\right) - cos\left(\omega N\delta t + \Omega N\delta t\right)\right] + \\ 0.5\varepsilon P_1 P_2 sin\left(\Omega\Delta t\right)\left[sin\left(\omega N\delta t\right) - sin\left(\omega N\delta t + \Omega N\delta t\right)\right] \end{gathered} \tag{5.29}$$

with C the undisturbed mixer output (eq.5.11). This can be simplified by realizing that $\Omega\Delta t \approx \pi/2$, since the effect of the crosstalk should be small. Thus $cos(\Omega\Delta t)$ is approximately zero and $sin(\Omega\Delta t)$ is approximately 1. Then eq.5.29. transforms into:

$$C^d \approx C + 0.5\varepsilon P_1 P_2 \left[sin\left(\omega N\delta t\right) - sin\left(\omega N\delta t + \Omega N\delta t\right)\right] \tag{5.30}$$

The difference in the two sine functions between the brackets is maximally 2, so the worst case condition for C^d is:

$$C^d \leq -0.5 P_1 P_2 \left[cos\left(\Omega\Delta t\right) - 2\varepsilon\right] \tag{5.31}$$

The error made in setting $C^d = 0$ is $\Omega\Delta t = \pi/2 + \delta$, with $\delta<1.4 \times 10^{-4}$, according to the delay-line specifications. A simple Taylor expansion of the cosine around $\pi/2$ shows that ε should be smaller than 0.7×10^{-4}. However, ε refers to the amplitude strength of the disturbing signal; to find the isolation in terms of power the value should be squared. This corresponds to a required isolation of the leaking path of -83 dB.

Multiple crosstalk signals

The problem becomes much more complicated if all the 1023 possible leaking paths are taken into account. However, this is not necessary. Most of these paths are isolated by at least two SOA gates, so that any leakage should be extremely small. There are 10 spurious paths (one in each of the 10 segments of the digital delay-line) which are isolated by only one SOA gate. These 10 leakage paths will provide almost all the crosstalk signal. Each path gives a term similar to the extra term added to C in eq. 31. This implies that the combined worst case effect of the 10 disturbing signals is 10 times the effect of a single source. Consequently, to cover the worst case of the combined effect, the isolation of each SOA gate should be a factor of 100 better (because ε should be a factor of 10 lower). In that case the required isolation in each gate should be better than -103 dB.

We measured the SOA extinction ratio for three SOA test structures with different length (100 μm, 200 μm, 400 μm) for TE and TM polarization. The 150 μm long SOA gates of the delay line present an extinction ratio of around 25 dB, which does not satisfy the isolation requirement for the delay-line. In order to reach the required isolation levels, much longer SOAs need to be used, in the order of 1 mm. This would require a PIC design much bigger that the actual one.

The isolation resulting from the analysis is a worst case number, and it is possible that with less strict requirements also a workable system can be made. However,

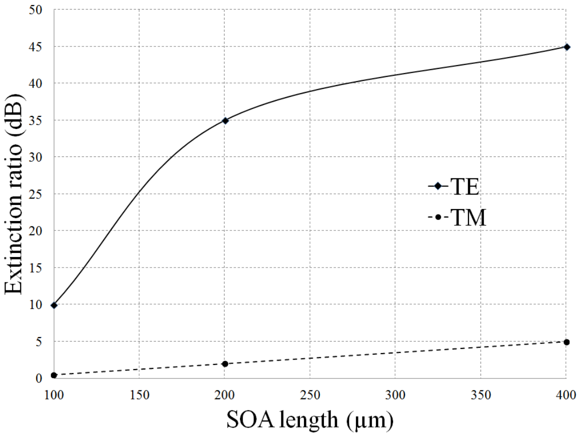


Figure 5.22: SOA extinction ratio as a function of the SOA length.

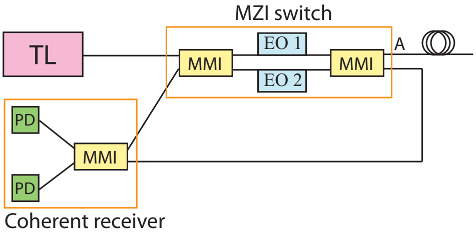
if one assumes a random averaging of the 10 disturbing signals, and a halved value for the disturbing terms in eq. 31, only about 16 dB (a factor of 6 higher value of ε) relaxation is obtained, leading to a required isolation of -87 dB. A more relaxed requirement can be obtained by using a zero crossing in Fig.5.5 at a much higher value, which would allow ε to be proportionally larger as well. However, this implies a much larger Δt, for the same Ω values, so a much longer delay-line would be needed,

Although the switchable delay-line does not satisfy the BOTDR requirements, some of the circuit functionality, e.g. the pulse generation of the switching network, can be still evaluated in the case of the BOTDR operational method 1 (Section 5.1.1). This is reported in the next section.

5.2.6 Pulse generation for BOTDR operational method 1

Here we analyze the switching network of the BOTDR circuit in the case of the operational method 1 (Fig.5.23). The MZI switch is formed using two 2x2 MMIs and 500 µm long electro-optic phase shifters on the two arms. The CW light from the TL enters the MZI switch. By shortly switching from the cross to the bar state, short pulses are created and injected into the fiber (side A). When the MZI switch is in the cross state, the back scattered light from the fiber enters the coherent receiver together with the light from the TL.

We first analyze the switching curves of the MZI switch obtained by sweeping



TL: Tunable DBR laser
PD: Photodiode
MMI: Multimode interferometer
MZI: Mach-Zehnder interferometer
EO: electro-optic phase shifter

Figure 5.23: BOTDR circuit schematic for the operational method 1 (see Table 5.1).

the voltage (reverse bias) from 0 to 10 V on phase shifter EO 2 while grounding phase shifter EO 1 (dotted line of Fig. 5.24 (a)) and measuring the output power at port A. The value of the voltage needed to obtain a π phase shift is 6.5 V. However, by adding the power from the two output ports, an electro-absorption of the phase shifters of 3 dB is found at this voltage (Fig. 5.24 (b)). To obtain short light pulses, a pulsed reversed voltage in the range of [2, 6] V is applied to EO 2 while EO 1 is grounded. The generated pulses show no appreciable delay with respect to the trigger signal applied on the switch, and have an FWHM=25 ns which leads to a measurement distance resolution in the fiber of about 2.5 m[12] (Fig. 5.25). The pulse width is reduced w.r.t. the electrical pulse due to the non-linear switching curve of the MZI.

5.2.7 Photo-diode

The responsivity (R) of the photo-diode has been measured for $\lambda = 1550$ nm. Considering the fiber to chip coupling loss (in a range from 5 to 7 dB), R is in the range 0.8-0.9 A/W which agrees with the foundry specification. Oclaro also estimates a bandwidth larger than 10 GHz, which is required for the BOTDR application.

5.3 Conclusion

A BOTDR circuit to detect strain and temperature distribution along an optical fiber has been fabricated within an InP MPW run, with the possibility of a significant cost reduction in comparison with the existing sensing systems. The optical components have been characterized with dedicated test structures. The measured DBR gratings

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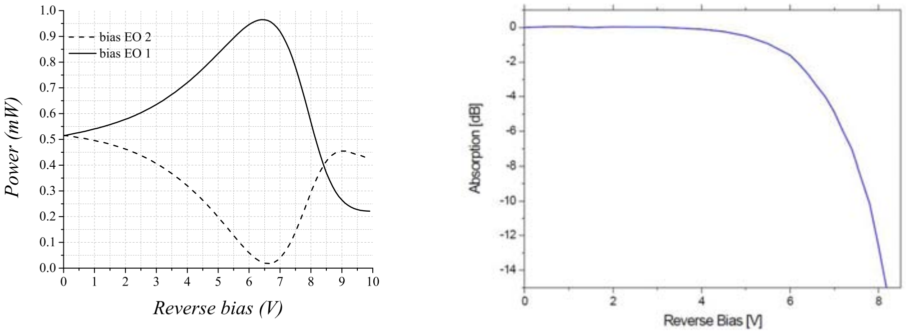
[12] In the switching network test structures there are two 2x2 MMIs between TL and the pulse output port. This lowers the power level of 6 dB.



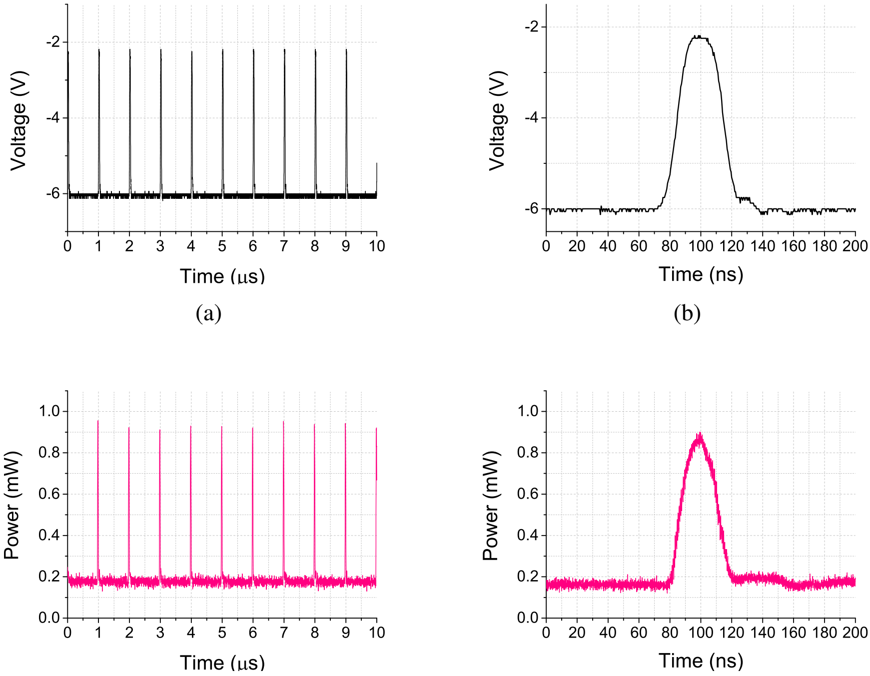
(a)

(b)

Figure 5.24: (a) Switching curve of the MZI switch applying a reverse bias on EO 1 and EO 2 respectively; (b) Phase shifter absorption as a function of the applied voltage.

reflectance (98% for the rear grating and 20% for the front grating) show a good agreement with simulations. The DBR lasers have a relatively low output power (4.5 mW) for the application (10 mW required), however, with 500 μm long booster amplifiers the lasers output power should gain about 15 dB. The fixed spiral delay shows a measured group delay (54 ps) in agreement with the expected value (55.07 ps). This implies that a controllable true time delay can be obtained. The bends with a radius of 100 nm show negligible polarization conversion: the total polarization conversion for 32 bends (the number used in the BOTDR delay-line) is below 0.5%. The bends extra losses are 0.13 dB/90° for the TE mode and 0.15 dB/90° for the TM mode.

The SOA gates of the delay line give a poor isolation (-25 dB for TE polarization for a 150 μm long SOA) compared to the requirement for the frequency stabilization system in the BOTDR application (-103 dB). However, since the BOTDR circuit offers three distinct operational modes, the switching network has been characterized during the operational method 1, that doesn't require the use of the tunable delay-line. Measurements show that 25 ns wide light pulses can be generated using a DBR laser and a MZI switch. This is limited in the experiment by the electrical pulse generation. In this way temperature and strain variation can be detected with a measurement distance resolution of 2.5 m along a sensing fiber. The photo-diodes used for the coherent detection shows a responsivity of about 0.-8-0.9 A/W and the foundry estimates a sufficient bandwidth larger than 10 GHz.



(a) (b) (c) (d)

Figure 5.25: (a) Pulsed voltage applied to the switch on EO 1 (c) and generated light pulses; (b) voltage pulse with a FWHM=30 ns and (d) light pulse with a FWHM=25 ns.

It is important to mention that, since the Brillouin signal travels in an optical fiber, its polarization state varies in a time scale of few milliseconds. This causes power fluctuations at the coherent receiver which detects only one polarization. The PC device, presented in Chapters 2 and 4, can be exploited to overcome the BOTDR limit related to the polarization state dependence in an optical fiber. A description of BOTDR circuit design improvements together with polarization handling capabilities will be presented in Chapter 6.

Chapter 6

Conclusions and outlook

This thesis treats the following subjects:

- *test of experimental devices through post-processing technology exploiting validated building blocks*
- *fabrication technology of new a tolerant polarization converter device*
- *design and measurement of a photonic integrated circuit for Brillouin sensing.*

The first one is presented in Chapter 3 as a unique technology to add experimental devices to prefabricated PIC. This opens the possibility to add advanced functionality in PIC, since designs are not limited anymore to a predefined set of building blocks. The post-processing technique is then applied to include a polarization converter (PC) in a PIC which contains polarization independent SOA test structures. The potentiality of the post-processing is strengthened in the final chapter (Chapter 6), where an advanced design of the Brillouin PIC with polarization handling functionality is presented. Chapter 2 presents the design and simulation of a passive polarization converter (PC), compatible with the Oclaro platform, and the polarization *independent SOA (PI-SOA) concept and design. A new design for the PC is proposed, which is compatible with the Oclaro platform. The PC shape with a triangular top cladding is innovative compared to the standard sidewall slope approach compatible with COBRA and HHI platforms, and it requires a simplified fabrication technology. A Brillouin Optical Time Domain Reflectometry (BOTDR) read-out unit is presented in Chapter 5. Compared to the bulk optics of the existing sensor systems, the aim is to integrate the optical functionalities in a compact photonic circuit (PIC). Furthermore, the PIC is fabricated within an MPW run with the possibility of a significant cost reduction. In this final chapter, we summarize the main results of this work in section 6.1. In section 6.2, recommendations and outlook for future improvements are given.*

6.1 Conclusions

An InP MPW run allows for the fabrication of photonic integrated circuits (PICs) with different functionalities that share the same technology platform. This process leads to cost-effective chips and most important it relies on validated building blocks for the realization of complex circuits. Another advantage of the generic technology approach is that it can be exploited to test experimental devices (ED), such as the polarization converter (PC), using validated structures. One of the aims of the project reported in this thesis is the design, post-processing and characterization of a PC in a PIC which contains structures to test the device in a polarization independent SOA (PI-SOA) configuration.

The second part of this work is the design and characterization of a PIC whose optical functionality is applied in a Brillouin Optical Time Domain Reflectometry (BOTDR) system, to detect strain and temperature variations in an optical fiber. Polarization handling capabilities of the BOTDR circuit, that combines both parts of this project, will be presented in the outlook section below.

The main achievements of this thesis project are listed in the following paragraphs.

Post-processing technology

A method to connect post-processed devices to prefabricated circuits has been developed, together with a technology to protect the PICs during post-processing. Tapered waveguides allow for the connection between devices processed with different technologies. Measurement results show 0.5 dB extra loss for two pairs of coupled tapers, which is about 0.3 dB higher than the simulation result. The PIC is successfully protected, during the post-processing of the experimental device, with SiNx and a thick photo-resist layer. A pholithography mask defines the areas for the post-processing.

Polarization converter device

Two different PC fabrication process flows have been presented, together with the measurement results on the devices. The PC experimental devices have been post-processed in a PIC which contains structures to test the device in a polarization independent SOA (PI-SOA) configuration. The characterization of the first generation PC shows that the polarization dependence of two SOA's in series reduced from 14 dB to 3 dB with a single section PC in-between, indicating the presence of a sizable polarization conversion. However, due to the presence of a guiding layer undercut and to the difficulty of achieving a device within the required tolerances, a full device characterization was not possible.

A second generation process flow has been proposed, to overcome the problems encountered in the first generation processing, and to fabricate a tolerant double section PC. With the new technology, PC dimensions are insensitive to EBL alignment errors. The accuracy is related only to the first ICP etching, used to lower the top cladding to the PC top height, and this can be accurately controlled to ± 10 nm.

With the insertion of a double section PC between two SOAs in series, the SOA polarization dependence gain is significantly reduced from 17 to 0.35 dB ($\lambda = 1.55$ μm). The better performance of the double section PC compared with the single section device has been confirmed. At $\lambda = 1.55$ μm the single section shows a polarization extinction ratio of 1.1 dB, and the minimum estimated conversion efficiency C is 99.5% in the case of the double section PC, whilst it is 97.5% for the single section PC.

Photonic integrated circuit for Brillouin sensing application

A BOTDR circuit to detect strain and temperature distributions in an optical fiber has been fabricated within an InP MPW run. This potentially gives a significant cost reduction in comparison with existing sensing systems. Test structures are included for the BOTDR optical components characterization. The measured DBR gratings reflectance is 98% for the 500 μm rear grating and 20% for the 100 μm front grating. The DBR lasers output power (4.5 mW) is too low for the application which requires at least 10 mW, however, booster amplifiers (500 μm long SOAs) at the lasers output can improve the power level of about 15 dB; in this case the output power will be approximately 130 mW.

The fixed spiral delay shows a measured group delay (54 ps) in agreement with the expected value (55.07 ps), which implies the possibility to accurately control the true time delay, used in the BOTDR circuit for laser frequency stabilization. The total polarization conversion for 32 bends (the number used in the BOTDR delay-line) with a bending radius of 100 μm is below 0.5%. The SOA gates of the delay line give a poor isolation (-25 dB for TE polarization for a 150 μm long SOA) compared to the BOTDR requirements (-103 dB). This implies that the laser stabilization circuit cannot be used.

Since the BOTDR circuit offers three distinct operational mode, the switching network has been characterized during the operational method that doesn't require the use of the tunable delay-line. A 25 ns wide light pulse can be generated using a DBR laser and a MZI switch. This is limited in the experiment by the electrical pulse generation. In this way temperature and strain variation can be detected with a measurement distance resolution of 2.5 m along a sensing fiber. The photo-diodes used for the coherent detection shows a responsivity of about 0.8-0.9 A/W with an estimated bandwidth larger than 10 GHz [design manual].

6.2 Recommendations and outlook

In this section we list some recommendations to improve the technology developed during the thesis project together with an outlook on further development both for the PC process flow and the BOTDR circuit design.

Post-processing and PC technology

The main processing issues of the post-processing technology and the PC process flow have been treated in Chapter 3 and Chapter 4 respectively. However, here we consider improvements to the technology that couldn't be performed during the project since they involve upfront changes in the PIC before the PC post-processing.

Guiding layer undercut

In Section 4.2.2 we explain how the guiding layer undercut has a large impact on the device performance, leading to high propagation loss and to a significant deviation from the simulated polarization conversion (Chapter 2). The undercut of the guiding layer is a consequence of the galvanic corrosion in metallized III-V wafers, cleaned in an acid solution (e.g. diluted HF, diluted H_3PO_4). This has been solved by shielding the back-side metallization from the electrolyte with 100 µm of SiN, and cleaning the wafer in the dark.

The undercut can be prevented without extra processing steps if the fabrication of the wafer, intended for the post-processing, stops just before the back-side metal deposition. This step, together with the annealing, can be added as last step of the experimental device process-flow. However, some damage to the wafer top metal contacts can occur. To verify if the contact pads experience any damage during deposition and annealing of the back-side metallization, we performed a test on a Oclaro wafer with annealed top contact, but without back-side metallization. The IV curves of a 700 µm SOA were measured before and after back-side contact deposition and annealing (Fig.6.1). The reported IV curves shows no damage to the SOA contact. Thus, the guiding layer undercut can be prevented by performing the back-side metal deposition and annealing at the end of the experimental device post-processing. With

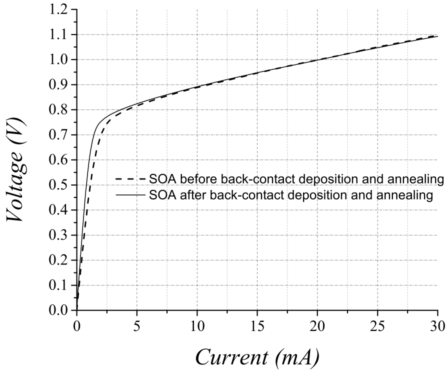


Figure 6.1: IV curves of an SOA before and after back-side contact deposition and annealing.

top contact pads present, it is recommended to always clean the wafer in the dark. As explained in Section 4.2.2, if the wafer area is about 3 orders of magnitude larger than the total metallized area this is sufficient to prevent the undercut.

Etch stop layer for ICP top-cladding etching

One of the first steps of the second generation PC process-flow (Section 4.3.1), is the cladding etching to the PC top height (763 nm) with a CH_4:H_2 ICP plasma. The etching can be accurately controlled in the order of 10 nm. An alternative approach would be to insert a quaternary etch stop layer (20 nm) at the desired PC top height in the cladding, and to use a solution consisting of HCl and H_3PO_4 in a 1:4 mixture to wet etch the cladding. The advantage of this approach is that there is no need of a monitor sample to control the etch depth.

New approach for PC processing and future PC integration in a standardized technology platform

During the monitoring of the second generation PC fabrication (Section 4.3) it has been found on a test sample that both vertical sidewalls of the PC can be etched simultaneously using RIE, while protecting the slope with nitride. In this test (Fig. 6.2), the etching of one of the sidewalls stops above the guiding layer, but the process can be tuned to etch deeper into the InP substrate. The advantage of this approach would

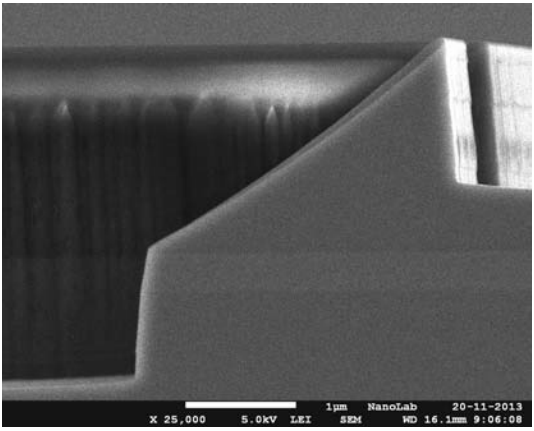


Figure 6.2: SEM picture of RIE etched PC vertical sidewalls.

be the reduction of the number of processing steps. However, the sidewall roughness needs to be evaluated.

One of the future challenges is the integration of the PC device in the generic InP technology platform. A combination between the post-processing technology and the PC process flow could be implemented to realize the PC integration in a standardized platform. Starting from the second generation PC process flow, we propose the following steps:

1. The definition of one of the vertical sidewalls of the PC together with input and output waveguides (see section 4.3.1, step (c)), can be performed using photolithography, instead of EBL, during the chip deep-etched waveguides definition. This step, in fact, doesn't influence neither the PC shape nor the symmetry between the mirrored section of the double section converter, so the EBL accuracy is not really required. Moreover, in a generic integration process-flow, all the deep-etched waveguide of a circuit are defined together and since there is no post-processing, the taper connections alignment is not an issue anymore. This implies that photolithography can definitely be used for the PC vertical sidewall definition instead of EBL.

2. A protection step with photoresist needs to be performed before the PC slope HCl etching (see section 4.3.1, step (e)) and before the SiN dry etching from the top surface to define the second PC straight sidewall (see section 4.3.1, step (g-h)).

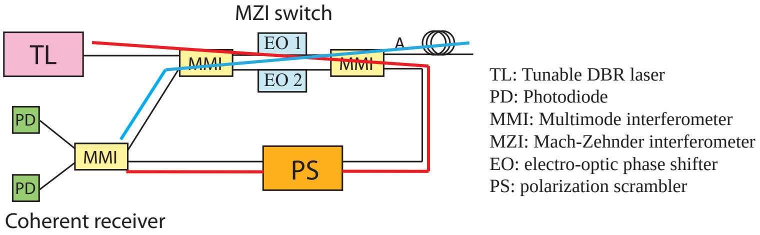


Figure 6.3: BOTDR schematic with the insertion of a polarization scrambler.

Once a fundamental component like the PC becomes a validated building block, polarization handling on chip will be possible for complex circuits. This will improve the performance of PICs designed for different applications i.e. the BOTDR circuit. The next section describes the advantage of adding polarization handling to the BOTDR circuit.

BOTDR circuit outlook

Since the Brillouin signal travels in an optical fiber, its polarization state varies on a time scale of a few milliseconds. This causes power fluctuations at the photo-receiver which detects only the TE polarization. The PC device, presented in Chapters 2 and 4, can be exploited to overcome this limitation.

The polarization induced power fluctuations can be averaged at the photodetector with the insertion of a polarization scrambler in the BOTDR circuit[1] (Fig. 6.3). The polarization of the local oscillator signal is scrambled before it enters the coherent receiver (red path) and mixes with the back-scattered Brillouin signal (blue path). Schematics of the polarization scrambler are shown in Fig. 6.4. The SOAs are used as gates to select either a direct path to the coherent receiver (Fig. 6.4(a)), where the TE polarization of the TL source is kept, or a path where the polarization is converted to TM (Fig. 6.4(b)). In this way the coherent receiver will detect subsequently the TE and the TM part of the back-scattered signal. When the switching is fast enough, the BOTDR signal can be effectively averaged over the polarization states. Considering that the back-scattered light polarization state varies in the order of ms, a SOA switching speed of 100 µs is a safe choice. Such a speed is easily achievable.

The BOTDR circuit presented here is the first PIC realized for sensing applica-

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[1] For simplicity reasons, we report the schematic of the BOTDR circuit in operational method 1 (see Section 5.2.1). The polarization scrambler concept can be extended to all three operational methods.

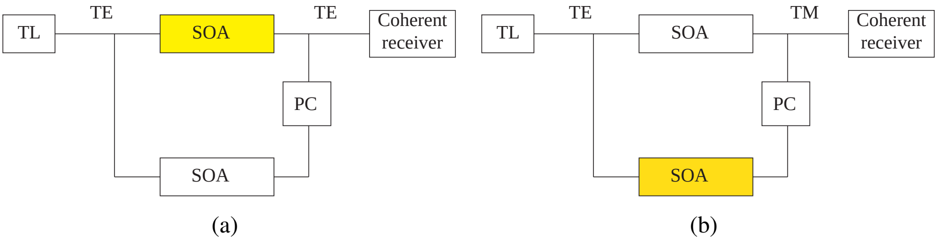

Figure 6.4: Polarization scrambler schematic. The TL light goes into the coherent receiver through the path with the biased SOA (yellow). The left picture shows the active path for the TE polarization, whilst the right picture shows the path for the TM polarization.

tion. The circuit design can be improved including longer phase shifters to decrease the 3 dB electro-absorption for π phase shift and DBR lasers with an output power of at least 10 mW [2]. A further step is to built the BOTDR system that includes the PID feedback loop to control the laser tuning, the coherent receiver and signal processing for the time and frequency analysis of the Brillouin frequency shift, towards a fully functional, compact and cost effective BOTDR integrated circuit.

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[2] During the thesis project Oclaro proposed DBR lasers with different combinations of rear grating, front grating and gain section lengths; new laser configurations that improve the output power level (above 30 mW) [design manual].

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List of Abbreviations

ASPIC	Application Specific Photonic Integrated Circuit
AWG	Arrayed Waveguide Grating
BB	Building Block
BCB	Benzo-Cyclo-Butene
BOTDA	Brillouin Optical Time Domain Analysis
BOTDR	Brillouin Optical Time Domain Reflectometry
CF4	Tetrafluoromethane
CHF3	Fluoroform
COBRA	COmmunication technologies, Basic Research and Applications
DBR	Distributed Bragg Reflector
DFB	Distributed FeedBack
EBL	Electron Beam Lithography
ED	Experimental Device
EDFA	Erbium-Doped Fiber Amplifier
FIMMWAVE	FIlm Mode Matching for dielectric WAVEguides
H3PO4	Phosphoric Acid

HCl	Hydrogen Chloride
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
InGaAsP	Indium Gallium Arsenide Phosphide
InP	Indium Phosphide
JePPIX	Joint European Platform for Photonic Integration of InP-based Components and Circuits
LiNbO3	Lithium Niobate
MMI	Multi-Mode Interference
MPW	Multi Project Wafer
MZI	Mach-Zehnder Interferometer
OSA	Optical Spectrum Analyzer
PC	Polarization Converter
PDG	Polarization Dependent Gain
PECVD	Plasma Enhanced Chemical Vapor Deposition
PIC	Photonic Integrated Circuit
PS	Polarization Scrambler
RIE	Reactive Ion Etching
RPM	Revolutions Per Minute
SEM	Scanning Electron Microscope
SiN	Silicon Nitride
SOA	Semiconductor Optical Amplifier
SPM	Self Phase Modulation

TE	Transverse Electric
TM	Transverse Magnetic
XPM	Cross Phase Modulation
ZEP	ZEP520A, Electron-sensitive resist

Summary

Polarization converter post-processing and Brillouin sensing optical functionality in generically integrated photonic circuits

Looking to the next stage of photonic integration, the aim of this work is to introduce components and functionality that are not fully supported yet in photonic integrated circuits. This thesis project demonstrates how to introduce experimental devices into complex optical circuits, realized in a standard foundry process. The project is structured in three main subjects. The first is the development of a post-processing technology that allows to test experimental devices using validated components in prefabricated integrated circuits. The second one is the design, post-processing and characterization of a specific experimental device: a new passive polarization converter in an integrated circuit, which contains structures to test the device in a polarization independent SOA configuration. The third subject is the design and characterization of a photonic integrated circuit for Brillouin sensing application. It became clear, however, that in the long term these subjects could merge, as the performance of the Brillouin circuit is can be definitely improved adding polarization handling devices in the circuit.

After an introduction on the thesis aim, subjects and structure (**Chapter 1**), **Chapter 2** presents the design and simulation of a passive polarization converter (PC), compatible with the Oclaro platform, and the polarization independent SOA (PI-SOA) concept and design. A new concept for the PC is proposed, using waveguide with a triangular top cladding. This PC shape is innovative compared to the standard sidewall slope approach and it requires a simplified fabrication technology. First, the performance of a single section PC is evaluated, then a double section PC

with two mirrored cross sections is proposed to increase the device fabrication tolerance and operational wavelength range. The double section PC simulations show a doubled width tolerance range for more than 95% conversion efficiency, and a conversion efficiency above 99% over the whole C-band. The PC is developed to obtain polarization independent SOAs by placing the device between two identical SOAs. The polarization is converted halfway between the two SOA sections and hence the polarization properties are averaged out over the two polarization states. Since the PC is not integrated yet in the Oclaro standard platform, the device is post-processed in a prefabricated MPW PIC, which contains SOAs test structures.

Chapter 3 focuses on the solutions adopted to connect an experimental device (ED) to the structures of a prefabricated PIC and on the technology developed to protect the existing circuit, during the ED post-processing. The connection between devices processed with different technologies is obtained through tapered waveguides. Measurement results show 0.5 dB extra loss for two pairs of coupled tapers, which is about 0.3 dB higher than the simulation result. The PIC is successfully protected, during the post-processing of the experimental device, by SiNx and a thick photo-resist layer. A photolithography mask has been used to define the areas for the post-processing. This unique technology opens the possibility to add advanced functionality in PIC, since designs are not limited anymore to a predefined set of building blocks. In this project, the post-processing technique is applied to include a polarization converter (PC) in a PIC which contains polarization independent SOA test structures. The potentiality of the post-processing is strengthened in the final chapter, where an advanced design of the Brillouin PIC with polarization handling functionality is presented.

In **Chapter 4** the fabrication technology and measurement results of the PC device are reported. The innovative PC with the triangular top cladding is fabricated through a process flow which requires only few extra steps compared to the standard Oclaro platform. In the first generation technology, the PC device is defined using EBL. However, this technique does not ensure the symmetry between the two mirrored cross-sections of the double converter. To solve the problem, a completely self-aligned process is proposed in the second generation technology. EBL is used only to define one PC sidewall, which can be done with photo lithography as well. This leads to the possibility of the PC integration in the standard Oclaro platform in the near future, by easily adapting the process flow. The PC is demonstrated in a PI-SOA configuration, showing a drastic reduction of the polarization dependent gain (PDG) with the insertion of the double converter, from 17 to 0.35 dB ($\lambda = 1.55$ µm). The better performance of the double section PC has been confirmed, since for

$\lambda = 1.55$ µm the single section shows a PDG of 1.1 dB, and the minimum estimated conversion efficiency C is above 99.5% in the case of the double section PC, whilst it is above 97.5% for the single section PC. The estimated PC device insertion loss is below 0.5 dB.

Chapter 5 presents a Brillouin Optical Time Domain Reflectometry (BOTDR) read-out unit whose optical components are integrated in a photonic circuit (PIC). The aim is to include all the optical functionalities of existing Brillouin sensors in a PIC to generate optical pulses to scan the fiber and detect the Brillouin backscattered light. The PIC has been fabricated by Oclaro within an MPW run, thus with the possibility of cost-sharing among the platform users. Measurements show that 25 ns wide light pulses can be generated using a DBR laser and a MZI switch. In this way temperature and strain variation can be detected with a measurement distance resolution of 2.5 m along a sensing fiber.

In **Chapter 6**, firstly recommendations on the post-processing technology are given. Then, a combination between the post-processing technology and the second generation PC process flow is proposed in order to achieve the challenging integration of this device in the Oclaro technology platform. Finally, an advanced design of the Brillouin PIC with polarization handling functionality is presented.

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List of Publications

Journal articles

- J.J.G.M. van der Tol, M. Felicetti, M.K. Smit, "Increasing tolerance in passive integrated optical polarization converters", Journal of Lightwave Technology, 30(17), 2884-2889.
- R.F Klein Breteler, J.J.G.M. van der Tol, M. Felicetti, G.D.J. Sasbrink, and M.K. Smit, "Photonic integrated brillouin optical time domain reflection readout unit", Optical Engineering, 50(7), 07111-1/8.
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Conference contributions

- M. Felicetti, J.J.G.M van der Tol., R.F. Klein Breteler, D. Szymanski and M.K. Smit, "InP photonic integrated circuit for BOTDR fiber sensing", OSA's 2013 Advanced Photonics Congress, Rio Grande (PR), 2013.
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- J.J.G.M. van der Tol, R.F Klein Breteler, M. Felicetti, G.D.J. Sasbrink, and M.K. Smit, “Design of a Photonic Integrated Circuit (PIC) for a BOTDR readout unit”, Proceedings of the 15th Annual Symposium of the IEEE Photonics Benelux Chapter, November 2010, TNO, Delft, The Netherlands.

Curriculum Vitae

Manuela Felicetti was born on 7 March 1983 in Rome, Italy. She received the B.Sc. and M.Sc. degrees in electronic engineering in 2006 and 2009, respectively, from Roma Tre University in Rome (Italy). After graduating in 2009, she moved to the Netherlands and started a four years PhD project in the COBRA research group of the Eindhoven University of Technology. Her research was focused on polarization converter post-processing technology and Brillouin sensing optical functionality in indium phosphide photonic integrated circuits. The results of her project are presented in this dissertation. In 2014 she joined the optical devices group at Mitsubishi Electric Research Laboratories in Cambridge (Massachusetts) for a six months internship. Here she worked on the design of polarization splitters, the assembly of an optical measurement setup and the characterization of photonic integrated circuits.