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Dielectric Material Options for Integrated Capacitors

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Future MIM capacitor generations will require significantly increased specific capacitances by utilization of high-k dielectric materials. In order to achieve high capacitance per chip area, these dielectrics have to be deposited in three-dimensional capacitor structures by ALD or AVD (atomic vapor deposition) process techniques. In this study eight dielectric materials, which can be deposited by these techniques and exhibit the potential to reach k-values of over 50 were identified, prepared and characterized as single films and stacked film systems. To primarily focus on a material comparison, preliminary processes were used for film deposition on planar test devices. Measuring leakage current density versus the dielectric constant k shows that at low voltages (≤ 1 V) dielectrics with k-values up to 100 satisfy the typical leakage current density specification of $<10^{-7}$ A/cm^2 for MIM capacitors. At higher voltages (3 V) this specification is only fulfilled for dielectrics with k-values below 45. As a consequence, the maximum achievable capacitance gain by introducing high-k dielectrics depends on the operating voltage of the application, such as DRAM capacitors or RF and blocking capacitors. To meet the reliability requirements for RF and blocking capacitors, high-k dielectric film thicknesses of up to 50 nm are necessary.
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Metal–Insulator–Metal (MIM) capacitors are widely used in ICs for many applications, such as DRAM storage capacitors, RF capacitors, blocking capacitors and many more. As the demand increases for shrinking device dimensions (e.g. DRAM capacitors) as well as the integration of surface mounted device (SMD) capacitors from printed circuit boards into System-in-Package (SiP) architectures, capacitor devices with significantly improved specific capacitances C_f (capacitance per surface area) are required. Capacitance is defined by the capacitor area A, the dielectric thickness d and the dielectric permittivity $\varepsilon_0 k$:

$$C = \varepsilon_0 k \frac{A}{d} \qquad [1]$$

The previous solution of increasing capacitor area A by utilizing three-dimensional capacitor structures, like trenches, runs out of steam due to limitations of the etch processes and increasing limitations of the silicon chip thickness, which goes down to the 100 μm range e.g. for power devices. Increasing capacitance by decreasing dielectric thickness leaves little room for improvement, as it is limited by the ratio of the device-defined breakdown voltage (U_{bd}) to the material-defined breakdown field strength (E_{bd}) of the dielectric. Also a sufficiently low leakage current density of typically $\leq 10^{-7}$ A/cm^2, which increases with decreasing dielectric thickness, must be maintained upon scaling. Thus the only degree of freedom left is the increase of the dielectric constant k. A large variety of high-k dielectrics have been investigated in the past. However, integrating these materials into three-dimensional MIM capacitors requires suitable deposition techniques, such as ALD or pulsed MOCVD (AVD).[1] Also these capacitors require film thicknesses in the range of 100 nm and below, where many dielectrics behave differently than the bulk material. In this study, a large number of high-k dielectric materials has been evaluated, and selected by the following criteria: a) potential

k-value of over 50, b) non-ferroelectric behavior at ambient temperatures, c) suitable precursors available for ALD or AVD deposition techniques. In this evaluation study the dielectrics were implemented into planar MIM capacitors with a variety of electrode materials.

Experimental

The dielectric material films were deposited using an ASM Pulsar 2000 ALD reactor (SrTiO$_3$, NbTaO$_x$, Al$_2$O$_3$), an ASM experimental PEALD reactor (PEALD SrTiO$_3$), a modified ASM A400 ALD batch reactor (Al$_2$O$_3$, AlTiO$_2$), an AIXTRON Tricent AVD reactor (SrTiO$_3$, BaSrTiO$_3$, TiTaO$_x$, SrTaO$_x$) and a home-built laboratory reactor (CeAlO$_3$). The electrode material films were deposited on an AIXTRON Tricent AVD reactor (TaN, Ru), an ASM Pulsar 2000 ALD reactor (TiN), Aviza Sigma-fxp AHF PVD tool (TaN) and Temescal 51192 E-beam evaporation tool (Au, Pt). Besides commercially available ALD precursors also precursors especially optimized for this study were used. More details can be found elsewhere.[2–4]

Film thicknesses were determined by spectroscopic ellipsometry and TEM. Generally the dielectric film thickness was adjusted to 50 $\pm$ 5 nm, the additional dielectric in the stacked film variants were minimized to a few nm. The electrode film thicknesses were set to 50 nm for TiN, TaN, Au, Pt and 20 nm for Ru. As for highly uniform step coverage on a particular three-dimensional test design ALD and AVD processes generally have to be adapted with respect to cycle and purge times. Thus in order to primarily focus on a material comparison, this time consuming procedure was abandoned and preliminary processes were used for film deposition on planar test devices. These devices were prepared from highly n-doped Si wafers coated with the bottom electrode material, either TaN, TiN or TaN/Ru on a 5 nm Ti contact layer. The dielectric material was deposited on this electrode and annealed appropriately. Post-deposition anneals at around 600°C under inert or oxygen-containing atmosphere for typically 30 minutes were necessary. On top of the dielectric layer, Au or Pt top electrodes were deposited in a structured manner utilizing a lift-off process.

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Table I. Potential high-k materials resulting from literature study.

Material	k	Leakage current density [A/cm^2]	Breakdown field [MV/cm]	Film thickness	Crystallization temperature	Reference (representative)
TiO_2	80...115	$5 \cdot 10^{-6}$	0.9	35 nm	750°C	5
$(Nd,Tb,Dy)TiO_2$	50	$<10^{-7}$ @ E_{bd}	2.1–2.5	35 nm		5
$TiAl_{0.67}O_3$	30	5 @ 1V		4 nm		6
$Ta_2O_5C_{0.07}$	24	10^{-8} @ 3 MV/cm		70 nm		7
$Ta_2Ti_{0.08}O_5$	14...20	10^{-9} @ 4 MV/cm		30 nm	600...900°C	8,9
$Ta_2Ti_{0.08}O_6$	126...189			bulk	<1400°C	10
$Ti_{0.6}Ta_{0.4}O$	45	10^{-6} @ 0.6 MV/cm		17 nm		11
$(Ba,Sr)TiO_3$	220...1000		0.5...15	100 nm	300...500°C	12
$SrTiO_3$	150	$5 \cdot 10^{-7}$ @ 1 V	0.6	50 nm	450°C	13
$BaTiO_3$	220				600°C	14
$(Pb,Sr)TiO_3$	560	10^{-8} @ 1 V		100 nm	<630°C	15
$Bi_4Ti_3O_{12}$	200	$3 \cdot 10^{-7}$ @ 0.1 MV/cm			600°C	16,17
$Bi_2Ti_2O_7$	600	$2 \cdot 10^{-8}$ @ 0.2 MV/cm			550°C	18
$SrTa_2O_6$	100...110	$5 \cdot 10^{-8}$ @ 3 V		40 nm	800°C	19
$BiTaO_3$	50...70	$10^{-2}...10^{-8}$ @ 1 V	3	4–110 nm		20
$BiTaO_x$	50	10^{-8} @ 1 V	3	50 nm		21
$SrBi_2Ta_2O_9$	70...140	10^{-7} @ 0.4 MV/cm		200 nm	800°C	17,22
$Bi_5Nb_3O_{15}$	71	10^{-9} @ 1 V	0.7	80 nm		23
$Sr_2Nb_2O_7$	40	10^{-7} @ 5 V		150 nm	<950°C	24
$NbTaO_x$	120					25
$KTaO_3$	250			bulk		26
$LiTaO_3$	400			bulk	450°C	27
$Pb_{0.64}La_{0.28}TiO_3$	850...1400	$5 \cdot 10^{-7}$ @ 0.2 MV/cm		500 nm		28
$CeAlO_3$	3000			bulk	<1600°C	29

The electrical characterization was performed with an HP 4140 ampere-meter and an Agilent 4294A impedance analyzer, contacting the Si substrate wafer and the structured top electrodes designed with varying surface areas. By changing the polarity of the measurement voltage, electron injection from either bottom or top electrode was applied. The leakage current densities were measured at variable bias voltages. Capacitance measurements for k-value determination were performed at 0 V bias voltage with 50 mV modulation. A measurement frequency of 10 kHz was chosen to yield reliable results also for low-quality dielectrics.

Results and Discussion

Material selection.— An initial literature study yielded several potential high-k dielectrics listed in Table I with representative references. However, some of these materials cannot be deposited by ALD or AVD due to lack of suitable precursors. Available Bi precursors, for instance, tend to decompose into metallic Bi rather than oxides, preventing formation of defined Bi oxides.[30] Taking into account the defined boundary conditions the following dielectrics and the corresponding deposition techniques have been selected for this study as shown in Table II. Within this study the principal capability of ALD processes for providing high-k films with excellent step coverage has been demonstrated earlier for AlTiO$_2$.[3]

The corresponding metal electrode materials were chosen from low (TiN, TaN) and high work function materials (Ru, Pt, Au). The values of the work functions of these electrodes are given in Table III. As for Au and Pt no ALD or AVD processes were available in this work, these materials were used as PVD deposited references. The corresponding work functions of the as-deposited materials were characterized by Ultraviolet Photoelectron Spectroscopy (UPS). In order to analyze work function changes during film deposition as well, measurements were done after a 300°C O$_2$ anneal simulating the high-k deposition during an ALD or AVD process. No significant degradation was observed after this O$_2$ treatment.

Leakage current density.— The basic technological issue for a dielectric material is its insulating behavior. A dielectric material cannot technologically be used as a capacitor dielectric if a certain maximum leakage current density (typically 10^{-7} A/cm^2) is exceeded. Thus the leakage current density J_{leak} vs bias voltage V was chosen as the critical parameter of the dielectric screening in this study. Figure 1 shows a large variation in the measured leakage current characteristics of the different dielectrics. Generally, leakage current density is increasing with decreasing dielectric bandgap and decreasing electrode work function. This is reflected in the asymmetry of the I-V curves when introducing different work function electrode materials. Here, negative bias voltage means electron injection from the high work function top electrode, leading to lower leakage currents. In contrast,

Table II. High-k dielectrics and corresponding deposition techniques evaluated in this study.

Dielectric material	Deposition method
$SrTiO_3$	ALD, PEALD
$BaSrTiO_3$	AVD
$BaTiO_3$	ALD
$TiTaO_x$	AVD
$SrTaO_x$	AVD
$NbTaO_x$	ALD
$CeAlO_3$	AVD
$AlTiO_2$	batch ALD
Al_2O_3 (combination layer)	ALD, batch ALD

Table III. Metal electrode materials and corresponding deposition techniques evaluated in this study. Work functions were measured by UPS as deposited and after anneal in O$_2$ environment to simulate the high-k film deposition process.

Electrode material	Deposition method	Work function (eV)	Work function (eV) (O$_2$, 300°C)
TiN	ALD	4.2	4.8
TaN	PVD, AVD	4.3	4.4
Ru	AVD	5.7	5.5
Au	PVD	5.4	
Pt	PVD	5.6	
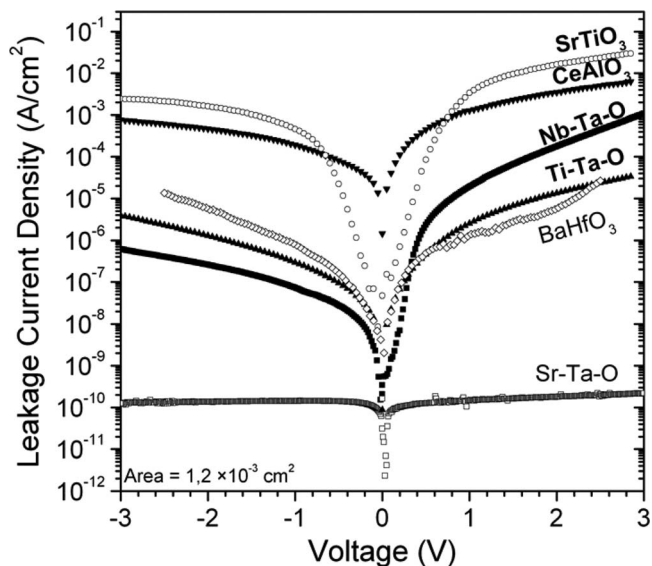
Figure 1. Leakage current characteristics of different high-k dielectric materials. Reprinted with permission from ECS J. of Solid State Sci. Technol. 1, N1 (2012). Copyright 2012 Electrochemical Society.

positive a bias voltage means electron injection from the low work function bottom electrode, leading to higher leakage currents. As can be also seen in Figure 1, some dielectrics yield high leakage current densities already at moderate voltages. Thus one strategy is to introduce additional low-leakage current dielectrics as blocking layers. However, generally these materials have lower k-values leading to a lower overall effective k-value due to serial combination of capacitances. Figure 2 illustrates the effect of such current blocking layers. Here, 50 nm of high-leakage current $SrTiO_3$ ($k = 95$) layer is combined with low-leakage current layers of amorphous $SrTaO_x$ ($k = 20$) with varying film thicknesses. Figure 2a clearly shows that the introduction of the blocking layer dramatically reduces leakage current density compared to a single high-k dielectric layer. However, a saturation of this effect is observed. On the other hand, Figure 2b shows that the capacitance density and thus the derived effective k-value decreases in the same direction. As a consequence, there will always be a trade-off between these two effects. For the evaluation of this behavior, the stacked dielectric systems $SrTiO_3/Al_2O_3$, $SrTiO_3/SrTaO_x$, $SrTiO_3/SrO$, $BaSrTiO_3/Al_2O_3$ and $AlTiO_2/Al_2O_3$ were included in
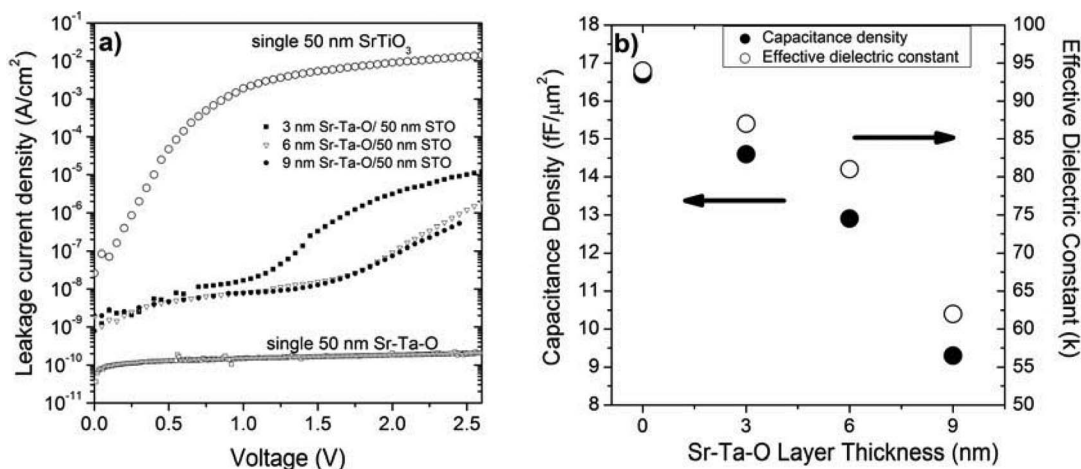
the study. For comparability reasons, only double layer stacks with the blocking layer between the low work function electrode and the high-k dielectrics were included in this paper. The effects of the location of the leakage current blocking layer within the stack have been published elsewhere.[31]

As evident from Figure 1, there are generally two different voltage regions with varying gradients within the leakage current density graph. Thus first a comparison of leakage current density of the investigated dielectrics was generated for the low-voltage region. For this purpose a voltage of 1 V was chosen, which is a typical value for DRAM applications. This comparison also includes measurements with injection from high- and low-work function electrodes. Typical values of the k-value and leakages current combinations of each material and stoichiometry out of a large number of data points are displayed. The thickness of dielectric in MIM stack was always kept at 50 nm. Despite still high data scattering in Figure 3, general trend can be drawn that an increase of leakage current density is observed when the dielectric constant of the MIM stack is also increasing. This is caused by the inverse relation between dielectric constant and bandgap of the dielectric.[32] The diagram clearly indicates that materials with a dielectric constant k of up to 100 can meet the leakage current density specification ($<10^{-7}$ A/cm^2) without a clear dependency on the electrode material. It is probably effects caused by interface and other charge traps mask the effect of the electrode's work function on leakage current. In addition to that, bulk limited conduction mechanisms might be also more dominant in this case. The rather high data scattering of the results from one material in several test devices might support this assumption. There is also no clear advantage of stacked over single-layer dielectrics. The optimization of the dielectrics stacks for the trenched DRAMs was reported in another study.[33]

For the higher voltage regime a bias voltage of 3 V was chosen. This is the highest voltage at which all investigated dielectrics show leakage currents low enough for reliable capacitance measurements. The overview diagram in Figure 4 for higher operating voltages looks significantly different from that in Figure 3. Leakage current density specifications ($<10^{-7}$ A/cm^2) for applications with higher operating voltages, such as RF or blocking capacitors, are now only met for dielectrics with k-values below about 45. As for the 1 V regime also in the 3 V regime no clear advantages of stacked dielectrics or dependency on electrode material were found.

Another important result is that the high literature k-values of bulk materials are mostly not reproduced in thin films. Generally, the films needed a post-deposition anneal above 600°C to crystallize and yield high k-values.[2] Even when the films were generally crystalline, there were probably differences in crystal size, crystal structure and
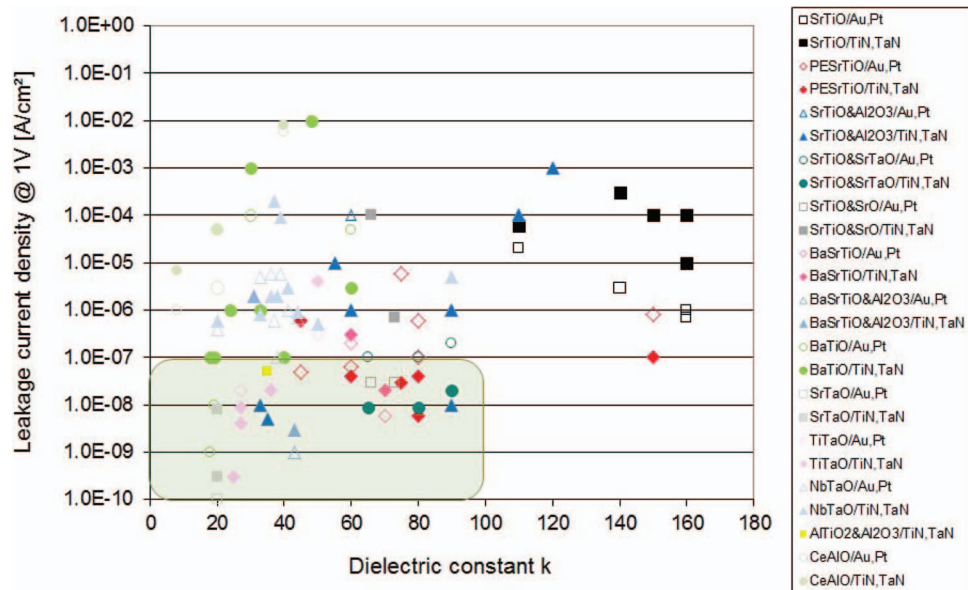

Figure 2. a) Leakage current density characteristics of a high-leakage current dielectric ($SrTiO_3$) combined with low-leakage current dielectric ($SrTaO_x$) layers, b) Resulting effective dielectric constants of these layer stacks. Reprinted with permission from ECS J. of Solid State Sci. Technol. 1, N1 (2012). Copyright 2012 Electrochemical Society.

Figure 3. Overview on leakage current density at 1 V bias voltage for several high-k dielectrics.

orientation, stoichiometry and possible contaminations caused by the deposition techniques leading to significantly lower dielectric constants than those for "ideal" bulk materials.

Breakdown field strength.— The second important parameter for technological suitability of a dielectric is the breakdown field strength E_{bd}, determining the dielectric film thickness d for a given breakdown voltage U_{bd} by

$$d = \frac{U_{bd}}{E_{bd}} \qquad [2]$$

Consequently, the breakdown field strength was also subject of investigation in this material study.

An empirical relationship between breakdown field strength and dielectric constant k has been found by McPherson et al.[34] From this finding they developed a model describing this relationship by an exponential law:

$$E_{bd} = 22.511 \cdot k^{-0.5424} \qquad [3]$$

In this study the breakdown field strengths could not be determined for all materials, due to high leakage currents in many cases, making the observation of clearly defined breakdown events impossible. Fig. 5 shows the measured breakdown field strengths compared with McPherson's model. Our measured data mostly lie below the predicted E_{bd} of the model, probably due to effects of the measurement voltage ramp and extrinsic effects, like defects or other impurities. However, the general trend found in our study follows the model.

As a consequence, the McPherson model can be used to estimate the required dielectric film thicknesses for integrated capacitors utilizing different k-values. An example calculation for capacitor is made for an operation voltage of 3 to 5 V. To meet typical
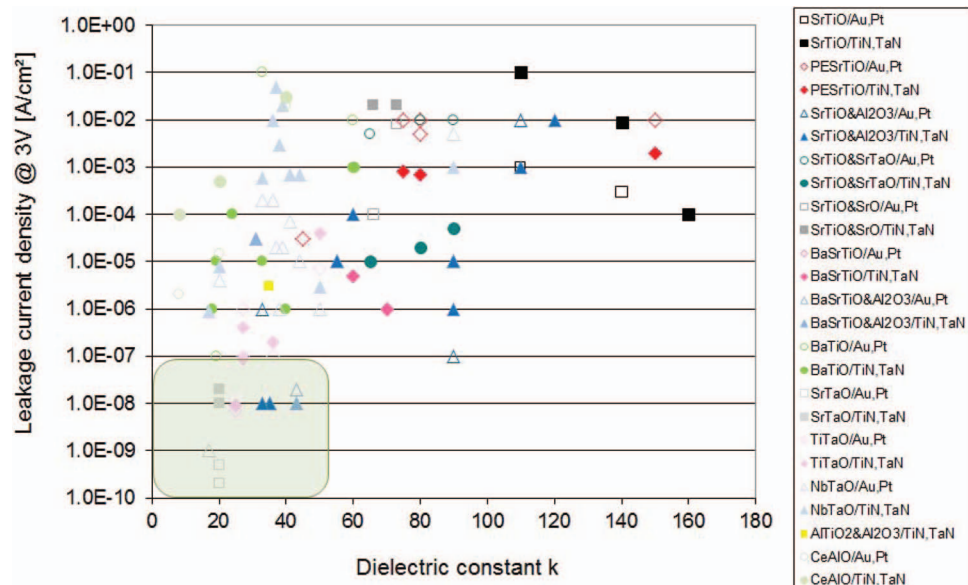
Figure 4. Overview on leakage current density at 3 V bias voltage for several high-k dielectrics.
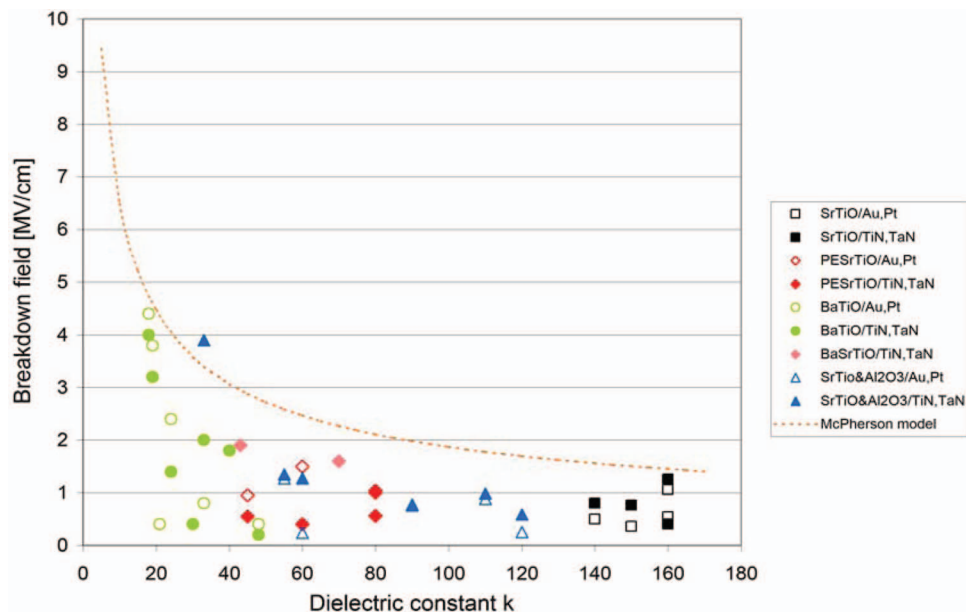
Figure 5. Measured breakdown field strengths compared with the McPherson model.

reliability requirements for capacitors, the breakdown voltage U_{bd} has to be increased by a so-called rating factor of 3 to 4 times larger than the operation voltage. Thus a breakdown voltage specification of 15 V is assumed for this calculation. Figure 6 shows two consequences from the calculation results. First of all, the gain in specific capacitance C_f with the k-value is not increasing linearly, making the effort for development of high-k dielectrics less efficient with higher k-values. Secondly, the required dielectric film thicknesses for the desired high-k dielectrics ($k \leq 45$) are in the range of up to 50 nm. This poses the question for cost of ownership of the deposition processes. As especially ALD is a low-throughput process, the gain of capacitance density in three-dimensional capacitors, which need a highly conformal deposition process, is opposed by the increasing cost of these deposition processes. One possible way out of this dilemma is the use of batch ALD[3] or spatial ALD[35] processes with a significantly higher throughput than single-wafer ALD processes. Also AVD processes have higher throughput than ALD, but with drawbacks in conformality, which however can be sufficient for some applications.

Stacked dielectrics are expected to show more complex breakdown behavior due to the electrical field distribution between the different
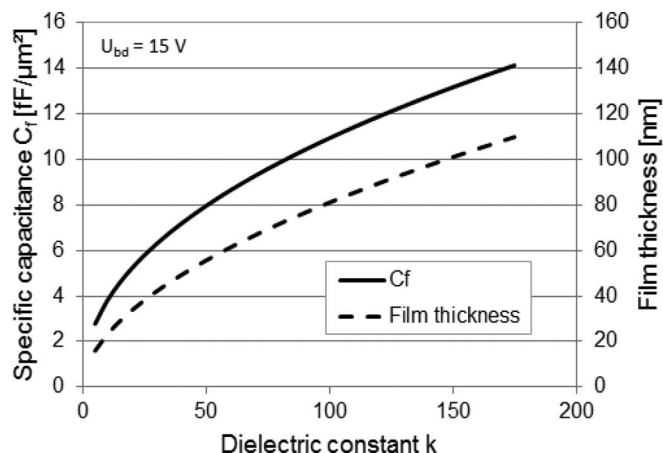
Table IV. Calculated breakdown voltage distribution in bilayer stack dielectric.

d_1	U_{bd1}	U_{bd2}
3 nm	1.3 V	9.5 V
6 nm	2.7 V	9.5 V
9 nm	4.0 V	9.5 V

dielectrics. As stacked dielectrics can be modeled as serially connected capacitors, the electric field across the lower-k blocking dielectric increases with the dielectric constant k and the film thickness of the higher-k dielectric. Thus assuming that the breakdown of the weakest dielectric determines the breakdown of the whole stack, the breakdown voltage of the dielectric stack can be estimated. A model calculation based on a $SrTaO_x$ ($k_1 = 20$, $d_1 = 3...6$ nm) / $SrTiO_3$ ($k_2 = 95$, $d_2 = 50$ nm) bilayer stack used in the leakage current blocking experiments yields the breakdown voltages U_{bd1}, U_{bd2} over both dielectrics as shown in Table IV. Comparing these values with the measured I-V characteristics of the stack dielectrics in Figure 7 shows that there

Figure 6. Required film thickness d and resulting specific capacitance C_f for a planar capacitor with breakdown voltage of 15 V at different k-values.

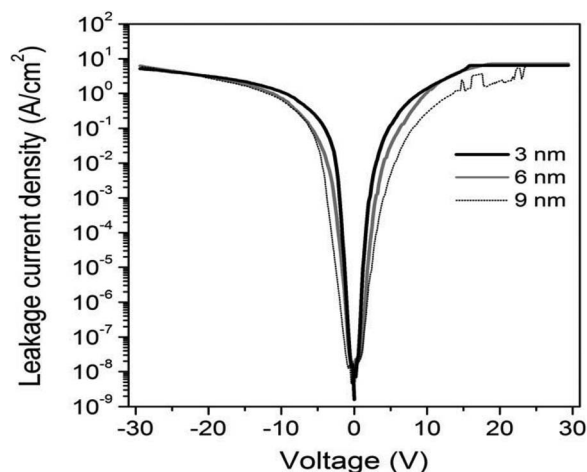**Figure 7.** Current-voltage characteristics of a $SrTaO_x/SrTiO_3$ stack with different $SrTaO_x$ blocking layer thicknesses.

are no clear breakdown events at the expected voltages. Moreover, the current through the stack seems to be dominated by the leakage current of the high-k dielectric, possibly masking the breakdown of the blocking layer.

At first view, the breakdown behavior of a dielectric stack does not seem to be significantly different from a single layer high-k dielectric. This is also consistently shown in Figures 3 and 4. However, more detailed studies will be required here to elucidate the picture.

Conclusions

In our material screening study we could show that a variety of high-k dielectrics up to $k = 150$ can be deposited by high-step coverage deposition methods, such as ALD and AVD. The results of our study indicate two different application regimes for high-k dielectrics in MIM capacitors. For low operating voltages (≤ 1 V), typical for DRAM storage capacitor applications, dielectrics with a k-value of up to 100 do meet typical leakage current density specifications of below 10^{-7} A/cm^2. For higher operation voltages (3 to 5 V), typical for RF or blocking capacitors, these leakage current density specifications are only met by dielectrics materials with a k-value below 45. This means that the use of HfO2 or ZrO_2 based dielectrics is most probable way for the optimization of future MIM capacitors. For the latter case the calculated capacitance increase, using the McPherson model for breakdown field strength, is a maximum factor of 2.7 compared to a standard ONO dielectric ($k = 5$). The application of stacked dielectrics with low-k leakage current blocking layers does not give significant advantage over single-layer dielectrics, as the improved leakage behavior is counterbalanced by the resulting lower effective dielectric constant. High-k dielectrics generally need to be crystalline to achieve their high dielectric constant. However, in most cases these dielectrics are amorphous after deposition and thus need a post-deposition anneal to achieve their desired properties. In our study we found that the necessary post-deposition anneals for dielectrics with $k > 30$ generally are in the range of 600°C or above. This makes integration of these dielectrics in the BEOL part of the chip difficult. If high-k MIM capacitors cannot be integrated in the FEOL part, a system-in-package (SiP) solution will be the integration solution for higher k-value dielectrics. We also could show that noble metal electrodes do not have significant advantages over TiN or TaN electrodes.

The decrease of the breakdown field strength with increasing k-value demands increasing dielectric film thicknesses for a given breakdown voltage. In the typical operating voltage range of RF and blocking capacitors dielectric film thicknesses of up to 50 nm are necessary for the relevant dielectrics (k < 45). This makes ALD, which has typically low growth rate, a potentially expensive deposition method for these applications. One solution could be the use of batch-ALD processes with several tens of wafers coated at the same time, or spatial ALD with ten-fold to hundred-fold deposition rates. Also, for lower aspect ratios of the capacitor structures and/or certain material systems, pulsed MOCVD (AVD) can provide good step coverage as well.

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