High-level synthesis of massively parallel vision architectures for 100000 frames-per-second visual servo control

Embedded Vision Architecture

Technische Universiteit Eindhoven University of Technology

High-Level Synthesis of Massively Parallel Vision Architectures

for 100000 Frames-per-Second Visual Servo Control

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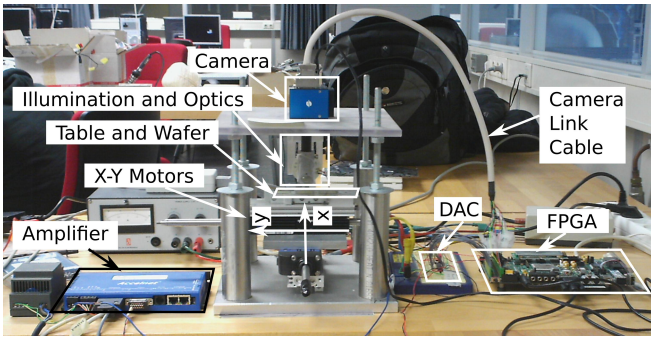
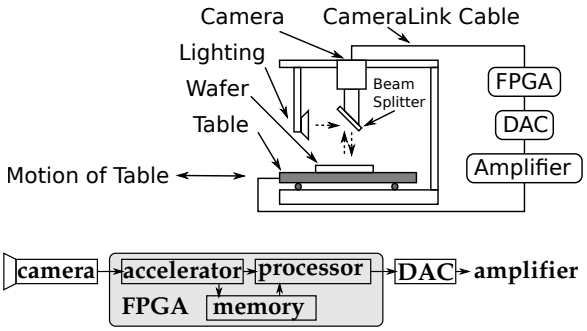
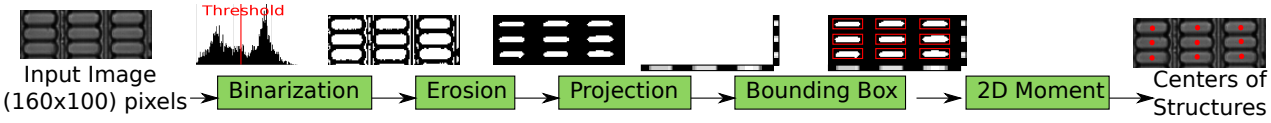
Vision-Based Wafer Positioning at Micrometer-Scale



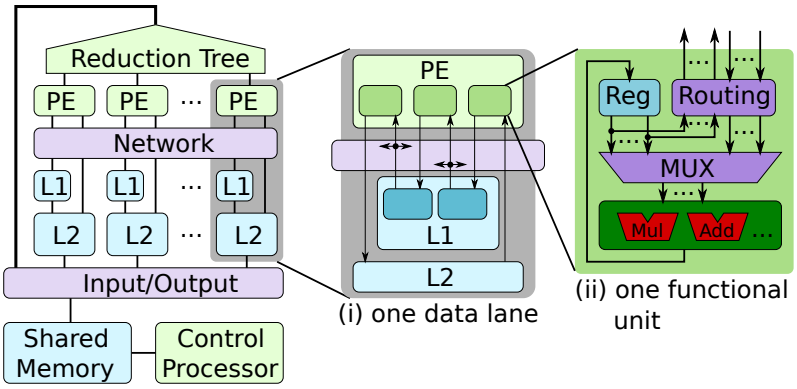
Overview of Setup and FPGA-based Vision System



Vision Pipeline. Goal: Detect Centers of Repetitive Structures



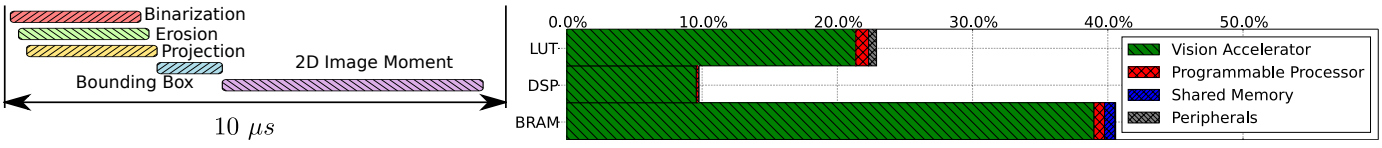
Vision Accelerator: Architecture Template and Its Instantiation Using High-Level Synthesis (Xilinx Vivado)



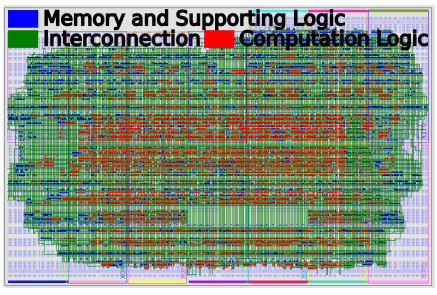
Instantiate 160 data lanes for images of 160x100 pixels

```
/* L2 memory: 160-bank, 100 entries each */
static unsigned char mem[160][100];
#pragma HLS ARRAY_PARTITION
variable=mem block factor=160 dim=1
/* L1 memory: 160-bank, 3 entries each */
unsigned char linebuf[160][3];
#pragma HLS ARRAY_PARTITION
variable=linebuf block factor=160 dim=1
... /* Other L2 and L1 memory */
for(i = 0; i < 100; i++) /* image height */
  for(j = 0; j < 160; j++) /* image width */
#pragma HLS UNROLL factor=160 /* 160 PEs */
    Operations /* 1 PE processes 1 column */
```

Timing and Resource Breakdown on a Virtext 7 FPGA (xc7vx485t)



Bottleneck of Architecture Scaling: Interconnection



According to place & route results (left), interconnection limits:

1. critical path
2. resource usage

Conclusions: High-Level Synthesis is Effective for

- Non-trivial vision applications.
- Instantiation of parallel architecture templates.
- Reduction of design time from months to weeks.
- Exploration of design alternatives in hours.

However, knowledge of architecture is required.