

High-level synthesis of massively parallel vision architectures for 100000 frames-per-second visual servo control

Citation for published version (APA):

Ye, Z., Jonker, P. P., Corporaal, H., & Nijmeijer, H. (2013). *High-level synthesis of massively parallel vision architectures for 100000 frames-per-second visual servo control*. Poster session presented at ICT Open 2013, Eindhoven, Netherlands.

Document status and date:

Published: 01/01/2013

Document Version:

Accepted manuscript including changes made at the peer-review stage

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

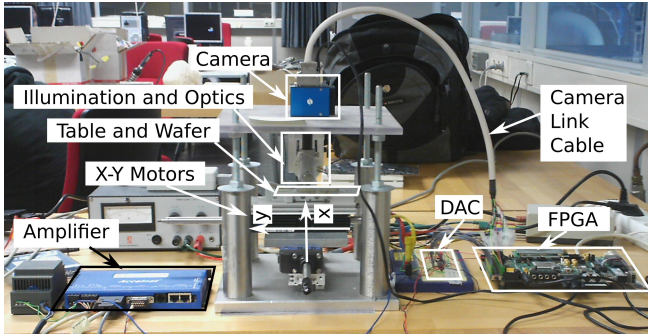
providing details and we will investigate your claim.

High-Level Synthesis of Massively Parallel Vision Architectures for 100000 Frames-per-Second Visual Servo Control

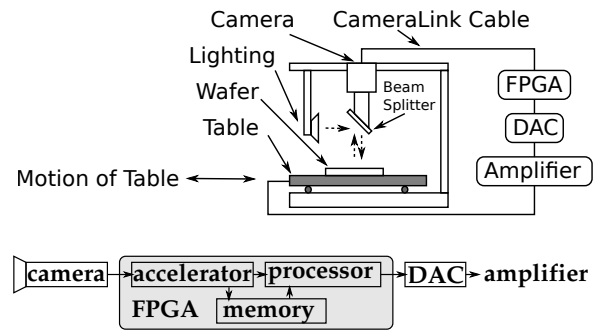
Zhenyu Ye
 Email: z.ye@tue.nl
 Advisers:
 Prof. Pieter Jonker
 Prof. Henk Corporaal
 Prof. Henk Nijmeijer



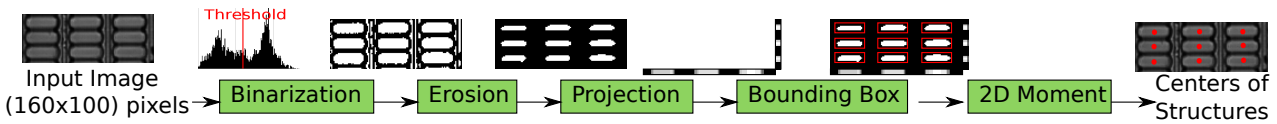
Vision-Based Wafer Positioning at Micrometer-Scale



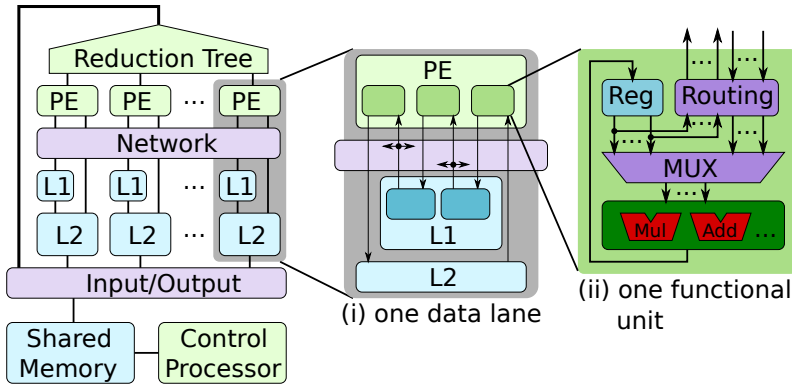
Overview of Setup and FPGA-based Vision System



Vision Pipeline. Goal: Detect Centers of Repetitive Structures



Vision Accelerator: Architecture Template and Its Instantiation Using High-Level Synthesis (Xilinx Vivado)

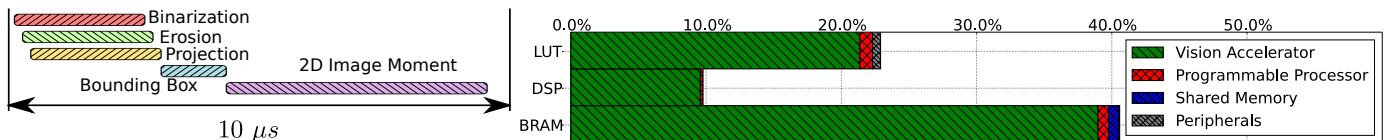


Instantiate 160 data lanes for images of 160x100 pixels

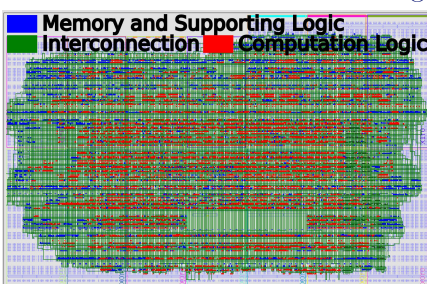
```

/* L2 memory: 160-bank, 100 entries each */
static unsigned char mem[160][100];
#pragma HLS ARRAY_PARTITION
variable=mem block factor=160 dim=1
/* L1 memory: 160-bank, 3 entries each */
unsigned char linebuf[160][3];
#pragma HLS ARRAY_PARTITION
variable=linebuf block factor=160 dim=1
... /* Other L2 and L1 memory */
for(i = 0; i < 100; i++) /* image height */
  for(j = 0; j < 160; j++) /* image width */
    #pragma HLS UNROLL factor=160 /* 160 PEs */
    Operations /* 1 PE processes 1 column */
    
```

Timing and Resource Breakdown on a Virtex 7 FPGA (xc7vx485t)



Bottleneck of Architecture Scaling: Interconnection



According to place & route results (left), interconnection limits:

- critical path
- resource usage

Conclusions: High-Level Synthesis is Effective for

- Non-trivial vision applications.
- Instantiation of parallel architecture templates.
- Reduction of design time from months to weeks.
- Exploration of design alternatives in hours.

However, knowledge of architecture is required.