

Technology aware circuit design for smart sensors on plastic foils

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TECHNOLOGY AWARE CIRCUIT DESIGN FOR SMART SENSORS ON PLASTIC FOILS

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. C.J. van Duijn, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op donderdag 19 juni 2014 om 16:00 uur

door

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geboren te Milaan, Italië

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List of abbreviations

AC	Alternating Current	20
AD	Analog to Digital	4
ADC	Analog to Digital Converter	11
ALU	Arithmetic Logic Unit	46
AMOLED	Active-Matrix Organic Light-Emitting Diode	11
CAD	Computer Aided Design	4
СВ	Conduction Band	24
CMOS	Complementary Metal Oxide Semiconductor	12
CPU	Central Processing Unit	1
CS	Current Steering	90
DA	Digital to Analog	4
DC	Direct Current	19
DFF	Data Flip Flop	99
DNL	Differential Non-Linearity	93
DOS	Density of States	25
DPCA	Differential parametric capacitor amplifier	73
DR	Dynamic Range	42
DRC	Design Rule Checker	20
EDA	Electronic Design Automation	19
ENOB	Effective Number Of Bits	21
FW	Finger Width	70
GBW	Gain BandWidth	45
GIZO	Gallium-Indium-Zinc-Oxide	89
HD	High Definition	2
IC	Integrated Circuit	1
INL	Integral Non-Linearity	44
IPMC	Ionic Polymer Metal Composite	11
LED	Light-Emitting Diode	12
LS	Level Shifter	106
LSB	Least Significant Bit	44
LTPS	Low Temperature PolySilicon	90
LVS	Layout Vs Schematic	20
MEC	Maximum Equal Criterion	46
NOSFEI	Metal-Oxide-Semiconductor Field Effect Transistor	10
IVISB	Most Significant Bit	94
	Multiple Trapping and Release	24
	Noise Margin	47
	Output Unaracteristic	29
USC OTA	Organic Semiconductor	/0
	Operational Transconductance Amplifier	21
		16
rl	Parametric Capacitor	67

PCell	Parameterized Cell	20
PLS	Positive-feedback Level Shifter	106
PTG	Planar Top-Gate	16
RF	Radio Frequency	5
RFID	Radio Frequency IDentification	2
SAM	Self-Assembled Monolayer	24
SAR	Successive Approximation Register	21
SBG	Staggered Bottom-Gate	16
SFDR	Spurious Free Dynamic Range	95
SNDR	Signal to Noise and Distortion Ratio	44
SNR	Signal to Noise Ratio	42
STG	Staggered Top-Gate	16
тс	Transfer Characteristic	29
TCTG	Top-gate Transfer Characteristic	29
TFT	Thin-Film Transistor	2
VCO	Voltage Controlled Oscillator	46
VRH	Variable Range Hopping	25

List of symbols

C _{dec}	Decoupling capacitor	[F]	80
C _i	Insulator capacitance per unit area	[F/μm²]	27
CL	Load capacitance	[F]	52
C _p	Parasitic capacitance	[F]	81
C _{SG}	Source to gate capacitor	[F]	70
C _{TGG}	Top-gate to gate capacitor	[F]	70
C _{TGS}	Top-gate to source capacitor	[F]	70
Ei	Energy level of the i th localized state	[J]	26
Ep	Pinch-off electric field	[V/cm]	28
f _t	Cut-off frequency	[Hz]	37
FW	Finger Width	[µm]	38
G _{diff}	Differential gain	[V/V]	87
G _m	Transconductance of the operational amplifier	[A/V]	52
g _m	Transconductance of the transistor	[A/V]	37
K _B	Boltzmann constant	[J/K]	25
L	Channel length	[µm]	28
L _G	Length of the gate metal in the PC	[µm]	70
Nt	Number of localized/trap states	-	25
\mathbf{Q}_{D}	Channel charge at the drain side	[C]	27
Qs	Channel charge at the source side	[C]	27
R' _{sub}	Substrate resistance	[Ω]	29
RL	Load resistance	[Ω]	52
SC	Sub-Channels	-	38
Т	Working temperature of the transistor	[K]	27
To	Semiconductor disorder characteristic temperature	[K]	25
T _{CLK}	Clock period	[s]	45
VD	Drain voltage	[V]	27
V _{DD}	Supply voltage	[V]	49
V _{DS}	Drain-source voltage	[V]	28
V _{FB}	Flat-band voltage	[V]	27
V _G	Gate voltage	[V]	27
V _{OD}	Overdrive voltage	[V]	28
V _p	Equivalent Early voltage	[V]	28
Vs	Source voltage	[V]	27
V _{ss}	Sub-threshold slope	[V]	28
V _{TG}	Top-gate Voltage	[V]	31
W _G	Width of the gate metal in the PC	[µm]	70
Wosc	Width of the OSC in the PC	[µm]	70
γ	Traps coefficient	[K/K]	32
ε ₀	Electric constant	[F/m]	68
ε _r	Dielectric constant	-	68
η	Top-gate coupling parameter	[µm/ µm]	34
θ	Heaviside unit step function	-	25

The truth is not fact or reason. The truth is just what everyone agrees on.

The Wizard of Oz

1 Introduction

1.1 Background

In 1965 Gordon E. Moore reported in his famous paper [1] that the number of transistors on an integrated circuit between 1958 and 1965 doubled every two years. He predicted the same trend to continue for at least ten years after his paper but his prediction turned out to be pessimistic. As a matter of fact, the integrated circuit industry adopted the well-known law named after him as the roadmap for its research and development, therefore Moore's trend has been followed till our days.

The exponential growth in the number of transistors per IC, fuelled by an impressive effort in device miniaturization and by outstanding achievements in the manufacturing processing, is tightly coupled to an exponential decrease of the unity cost of the transistor, which has enabled a pervasive presence of electronics in human lives. The downscaling of the feature size of silicon technologies allows not only more integration, but also higher speed, reduced power-delay product, and improved reliability of the integrated circuits.



Figure 1. Moore's law in microprocessor: transistor count vs. history [2].

A classical example of Moore's law development can be found in the microprocessors, since the first Intel's i4004 in 1971. That first central processing unit (CPU) was built with a 4 bit architecture, it was manufactured with the first self-aligned technologies, and could work at a clock frequency of 740 kHz. Nowadays multi-core CPUs based on 64 bit architectures are on the market, they integrate graphic processors, and their clock runs at multi-GHz frequencies. As shown in Fig. 1, the number of transistor per IC has been growing exponentially in time in line with Moore's prediction, thanks to the impressive progress in the manufacturing process. Indeed the i4004 used a pioneering 10 μ m minimum feature size self-aligned technology for its 2,300 transistors; while nowadays the most advanced lithography processes for in microprocessors reach 22 nm minimum feature size and these ICs count up to 2.6 billion transistors.

The ever growing computational power we witnessed fuelled plenty of applications, like HD compact cameras, digital television, personal computers, laptops, game consoles, memories, tablets and smartphones. All these applications provide more and more functionalities even in portable devices, and achieve these results at a constant or even decreasing cost, thanks to Moore's development.

On the other hand, there are many applications of electronics that do not require high computational power, and cannot be addressed by standard IC technologies due to the high cost per area and to mechanical limitations. The typical example of such applications is a flat-screen display. Displays are intrinsically large-area. Their remarkable growth and irresistible commercial success are based on the development of a specific electronic technology, TFTs (Thin-Film Transistors) on glass, which aims at decreasing the cost per unit area (and not the cost per transistor, as it is the case in IC technology). TFTs are transistors manufactured on large glass carriers using thin semiconductor films deposited on the glass surface (amorphous or polycrystalline silicon, in most cases).

In the last 15 years a clear trend towards lowering the processing temperature of large-area TFT processes has also been emerging. Lower temperatures indeed enable the use of thin, flexible plastic substrates that are much more attractive than the fragile and expensive glass sheets used nowadays. These developments have been fuelled by research on semiconductor materials that can be processed at near-to-ambient temperature, like organic and metal oxide semiconductors [3], [4].

Large-area electronics processed at low temperature on flexible substrates enable two sorts of innovative applications: on the one hand, applications that exploit together large area, flexibility and ruggedness, like touch screens, Braille displays [5], pedometers [6], strain gauges, artificial skin [7], [8] and more [9], [10]; on the other hand, applications that exploit these technologies for their simplicity and high throughput, aiming at achieving cost competitiveness with silicon for very cost-sensitive applications with low computational intensity. To this latter category belong, for instance, item-level Radio-Frequency Identification (RFID) tags [11] augmented with sensors, able to monitor the storage and distribution chain of food, pharmaceuticals or expensive chemicals.

Unfortunately large-area electronic processes on foil are still in an initial state of development, and the design of circuitry exploiting this technology must cope today with several drawbacks in terms of variability, ageing and low-performance. In this thesis, large-area technologies will be used to design building blocks suitable for smart sensors (which integrate electronics along with the actual sensor), with particular focus on the techniques adopted to face the several limitations that still affect the manufacturing process and the transistors on foil.

1.2 Problem statement

Processing TFTs on large area at near-to-ambient temperatures is normally associated with poor control on the thickness of the single layers, on the spot temperature during the process,

and other boundary conditions. For this reason, the variability among different TFTs is very pronounced, and it is difficult to match devices even if they are identical and close-by [12].

The variability and poor matching around the foil are not only due to process parameters varying from point to point, but also to the solid state structure of semiconductors suitable for low temperature processing. These materials are indeed normally disordered micro or nanocrystalline materials, rather than perfectly uniform mono-crystals like in Silicon ICs. Another source of variability is the contact resistance between source/drain contacts and the semiconductor film [13], [14].

The intrinsic poor performance of semiconducting films processed at low temperature is closely related to their disordered packing. Disorder in the periodicity of the lattice prevents the charge transport from taking place in extended states; on the contrary charge carriers are in localized energy states [15] or "hop" [16] among them. For this reason, mobility typically ranges between 0.1 and 10 cm2/Vs [17], which is two or three orders of magnitude smaller than in crystalline silicon.

The reduced mobility translates in small TFT transconductance, while the output resistance is strongly limited by short-channel effects [18], [19], [20]. Indeed, in standard thin-film transistor technologies on flexible foils, the gate insulator cannot be scaled down to very thin layers and the control of the gate on the channel is heavily affected by the longitudinal electric field. These two aspects of large-area TFTs result in a maximum intrinsic gain typically ranging between 20 and 26 dB.

All these intrinsic TFT limitations are not the only issues concerning low-temperature semiconductor materials and their process technology. Indeed another important aspect of large-area TFT technologies on foil is the availability of p-type, n-type or complementary transistors. Traditionally, low-temperature processes have been using only p-type organic semiconductors and thus p-type TFTs only [3]. Later on, also n-type TFTs have been processed at low temperature using organic materials [21] or metal oxides (like ZnO [15] or InGaZnO [22]). Even though metal-oxide semiconductors are rapidly becoming a standard technology in display backplane [23], their use in circuits is still in its early infancy.

Only recently, complementary processes have been demonstrated [24], [25] combining two organic materials or exploiting "hybrid technologies" that combine organic p-type with inorganic n-type semiconductors [26]. These processes are inherently more complex than unipolar ones, and typically result in higher defectivity. The most reliable (low defectivity and variability) TFT technologies fabricated at low temperature nowadays still offer, at the state of the art, only p-type normally-on organic TFTs and capacitors. State of the art p-type-only organic TFT circuits have reached a complexity level of 4,000 transistors [27], while complementary organic technologies offer a maximum complexity of about 100 TFTs in functional circuits [28].

P-type TFTs in low-temperature technologies are typically normally-on devices. Semiconductors with such property are preferred since higher gain, better noise margins and thus higher circuit complexity can be achieved using a logic gate when the active load is implemented with a Zero-Vgs connected load (i.e. shorting gate and source of the TFT), compared to the diode-connected load which is the only viable solution for normally-off TFTs. However, normally-on TFTs represent an awful solution for switches or pass-transistors and do not necessarily work in saturation when diode-connected. Therefore, the design of current mirrors is not trivial on one supply rail (V_{DD} for p-type and gnd for n-type), and it is impossible at all on the other. The availability of only one type TFT poses strong limitations to the freedom of

design for analog and digital circuits, and makes the design of reliable digital functions extremely challenging.

A final important issue, which has been only partially solved till now with material research, is the sensitivity of large-area low-temperature TFTs to aging and bias stress in air.

1.3 Aim of the thesis

The aim of this thesis is to investigate the following major issues relevant to analog, digital and mixed-signal circuit design in large-area TFT technologies:

- Modeling and characterization of the devices and their implementation in a Computer Aided Design (CAD) environment
 - Technology aware design at different abstraction levels:
 - o Architecture level
 - Circuit level
 - Layout level
 - o Device level
- Feasibility of circuit solutions that reach sufficient complexity to enable ultra-low-cost applications using unipolar TFTs on foil
- Long-term sustainability of unipolar technologies versus complementary ones

From a practical point of view, the main design goals can be summarized in:

• Improvement of the performance of analog, mixed-signal and digital circuits and their robustness against process variations and mismatch

and more specifically:

- Improvement of AD and DA converters accuracy
- Improvement of digital logic robustness.

1.4 Scope of the thesis

The work presented in this thesis focuses on circuit and system solutions for smart sensors manufactured using low-temperature large-area TFTs. The "smart sensor" is herewith defined as a system capable of physical measurements, first analog signal conditioning, data conversion and wireless data communication to a base station (Fig. 2).



Figure 2. Smart sensor schematic.

Among the required building blocks, the sensor and the RF transceiver fall out of the scope of this thesis, while circuits necessary to the sensor frontend, as it is defined here, have been studied and compared to the literature. More specifically the following functions have been implemented:

- Analog signal conditioning
- Data conversion
- Control logic

In order to design the aforementioned interfaces, two different technologies have been employed:

- An organic double-gate p-type-only technology
- A metal-oxide n-type-only technology

1.5 Outline of the thesis

The circuit complexity of analog, digital and mixed-signal blocks made with emerging technologies can appear trivial to the eye of a silicon IC designer. For this reason, Chapters 2 and 3 introduce large-area applications and technologies, and state of the art in circuit design in these technologies, comparing this to the situation in standard silicon, and clarifying advantages and limitations of both. Highlighting these differences is fundamental to understand the challenges imposed by low-cost low-temperature high-throughput manufacturing.

The electrical characterization and modeling of a double-gate p-type TFTs is presented in Chapter 4 with general remarks on process variations, mismatch, bias stress and ageing.

Chapter 5 illustrates the main building blocks necessary to build a smart sensor frontend and the architectural choices made for each taking into account features and drawbacks of the technology.

Chapters 6, 7, and 8 deal with the design of the sensor frontend at a circuit level: from the analog signal conditioning, through the analog to digital data conversion, to the design of a new logic style suitable for robust digital processing in unipolar technologies.

Finally, conclusions are presented in Chapter 9.

1.6 Own contributions

Different techniques to improve the reliability and the performance of analog, digital, and mixed signal circuits on plastic foils have been proposed during this research activity and will be extensively explained throughout this manuscript. The author's main contributions are summarized in this section.

In Chapter 6 is presented a G_mC filter that provides a gain which is independent from the absolute value of any process parameters [29]. This result was achieved creating a transconductor where both transconductance and output resistance depend on the channel length modulation of identical transistors. An additional voltage control was included to be able to correct any variations on the filter cut-off frequency due to process variations and aging.

In Chapter 6 is also described a new parametric capacitor design and its use in a discrete-time parametric amplifier [30], [31]. The gain of this amplifier depends on the distance between two metal layers. This parameter is typically better controlled than the electrical properties of the semiconductor. Moreover variations of the distance between the two layers are averaged on the capacitor area. In the used technology, a gain of 10 is achieved together with a time response which is much faster than continuous time amplifiers manufactured in the same technology and characterized by the same gain.

Data conversion is tackled in Chapter 7. Firstly, a synchronous latch is proposed that, unlike state-of-the-art large-area comparators, achieves at once short comparison time and full-scale output range thanks to a regenerative positive feedback loop [32]. The differential signal is provided through the second gate (see Chapter 4) of the input TFTs. This approach also guarantees a low input capacitance and a large input common mode range, simplifying the design of the comparator driver.

The DAC converter described in Chapter 7 [33] takes advantage of a different technology from the one used in all other circuits. In this case, a metal-oxide semiconductor (Gallium-Indium-Zinc-Oxide - GIZO) was used. This material provides higher mobility and better matching than organic semiconductors. For this reason, a current-steering (CS) topology was chosen to attain the fastest converter on foil reported. The measured 6 bit CS-DAC achieves an SFDR larger than 50 dB up to 10 kHz input frequency. Mainly due to the capacitive load posed by the measurement setup, a single pole roll-off at 80 kHz is observed. The best previously reported SNDR for DACs made with large area process (32 dB @ 3.1 kHz, 100 kS/s [24]) is thus improved up to an input frequency of 300 kHz (sampling rate of 10 MS/s).

To perform analog-to-digital conversion with high linearity and low area consumption, an integrating ADC was designed [34]. The chosen topology requires only two building blocks: a VCO and a counter. The VCO is realized by means of a ring oscillator including a tunable-delay buffer. The delay cell was designed aiming a linear time-voltage characteristic despite the limits posed by a technology, which misses linear passives and complementary devices. The designed VCO achieves an SNR = 48 dB and a linearity better than 1 LSB at 6 bit resolution (DNL = 0.6 LSB and INL = 1 LSB). The area occupation was reduced by more than 10 times compared to ADCs reported in the same technology [35] and by more than 30 times compared to ADCs exploiting state-of-the-art complementary technologies made with large-area processes [36].

A Positive-feedback Level Shifter (PLS) logic style (Chapter 8) was used to design the counter of the VCO-based ADC and other digital blocks (e.g. a 240-stage shift register demonstrating, to the author's knowledge, the most complex circuit in terms of transistor count reported [37]). Large-area electronics aims to ultra-low-cost portable devices realized with technologies which nowadays suffer nowadays from large process parameter variations. For this reason, the logic style proposed improves the state-of-the-art in terms of input-output characteristic symmetry, maximum gain (> 76 dB) and noise margin (maximum noise margin NM_{max} ~ 8.2 V @ V_{DD} = 20 V and average NM_{avg} = 6.82 V @ V_{DD} = 20 V over 288 measured inverters). These results could be possible thanks to a careful use of positive-feedback and to a strong control on the threshold voltage of the logic gate.

In order to design these circuits, a design flow for each technology process in use has been developed. The complete Cadence environment was set up from scratch; starting from the description of the technology (in terms of layers, design rules and PCells), to the configuration of Layout-vs-Schematic (LVS) and Design Rules Checker (DRC) tools. Specific structures have been taped out, measured, and analyzed to characterize the technology process using the physical

model developed in house by Post Doc. Fabrizio Torricelli (an example of data analysis and model characterization is provided in Chapter 4). The static physical model proposed by Torricelli was then augmented with a geometrical description of the parasitic capacitance between the terminals.

Besides this activity, the cooperation with Torricelli also led to the design and the characterization of two innovative TFT devices described in two European patent applications [38], [39].

All circuits and devices, unless otherwise specified, have been realized by the project users (Holst Centre, PolymerVision and imec) and measured in house. The measurement instrumentation was setup to interface with Matlab in order to easily acquire large amounts of data and provide on-the-fly analysis of the measurements.

2 Applications of large-area electronics on foils

Applications addressed by large-area electronics give the motivation pushing the research on large-area TFT manufacturing processes and circuit design. Since the birth of electronics, the main research goals have been miniaturization and increasing computational power. Today's focus is turning back to people, and electronics aims now to pervade daily life. From this prospective, standard transistor technologies do not provide anymore a solution suitable to all demands. For innovative applications mechanical properties may become more important than performance, or cost must be sometimes evaluated with respect to the area and not to the complexity of the function realized. In this chapter several applications enabled by large area electronics on foil will be reviewed.

2.1 From miniaturization to flexible substrates

The first integrated circuits date back to the early '60s. Since that moment the miniaturization of the metal-oxide-semiconductor field effect transistors (MOSFETs) has enabled enough computational power for lots of applications ranging from medicine to gaming, from aviation to video editing, from automotive to telecommunications, and many others.

Nevertheless, more recently, different applications have also attracted the attention of academic and industrial researchers. In this case, the key features are represented by the mechanical properties of the electronics (large area and flexibility) and by the low-cost of the manufacturing process.

For this reason, new materials and deposition techniques suitable for cheap substrates, like paper, plastic foils and fabrics [40], have been investigated, which can be processed in ambient environment with potentially high throughput. Different technologies were developed to realize a wide set of devices such as physical sensors [41], [42], [43], photo detectors [44], light emitters, plastic actuators [5] and general purpose flexible electronics [45]. Not all these components can be integrated on the same substrate and manufactured within the same process yet, but they share common manufacturing techniques and materials, hence the way to a full integration can be discerned at the horizon.

Of course, these new technologies do not aim to replace silicon ICs in high performance applications. Indeed, due to the low temperature nature of the process and to the use of materials suitable for deposition from solution, the electrical performance of large-area electronics is typically much lower than standard silicon technologies. The mobility of organic and metal-oxide semiconductors is usually about three orders smaller than that in silicon; the intrinsic gain of these transistors is a few tens; often only p- or n-type device are available; TFTs typically suffer from poor uniformity, bias stress and aging, which affect the parameters of thin-film transistors increasing the deviation from their nominal values.

2.2 Applications

Applications exploiting cheap flexible substrates, and cheap manufacturing process, can be divided at first glance in two main groups: large-area applications and low cost applications. The first one aims to a reduction of the cost per area, while the second one to a reduction of the cost per transistor/function.

2.2.1 Large-area applications

In the last two decades, the major force driving the innovation around large-area electronics was the industry of flat-panel displays. For this sort of applications indeed, electronics need to be manufactured on a surface much larger than common semiconductor wafers in order to drive all the pixels composing the display. In this domain the most interesting technology from a commercial viewpoint is thus the one achieving lower cost per area, not the one achieving lower cost per transistor (Moore's law).

In the beginning, TFT technologies developed for this purpose used to exploit glass substrates and polycrystalline or amorphous silicon [46], [47] as semiconductors. When materials suitable

for low-temperature deposition enabled the integration of circuits on foils, lots of new applications became possible.

In the sphere of display applications, technologies on flexible substrates can be used for portable devices due to their higher ruggedness compared to the standard silicon ones. For example, if the display backplane is manufactured on flexible substrates, the touch screen would not crack if the portable device is accidentally dropped on the floor or if someone seats on it. Also, plastic foils are much lighter than glass substrates: a very convenient feature not only for wide screen televisions, but also for music players, tablets, e-book readers and smartphones. One of the most successful combinations of flexible electronics for display backplanes with new light-emitting materials can be found in Active-Matrix Organic Light-Emitting Diode (AMOLED) displays which can be used in bendable, rollable and foldable portable systems, achieving at the same time low cost, large area, high resolution and low power consumption [48].

The interaction between light and charge carriers in semiconductors can also be exploited in flexible lighting surfaces [49] and solar cells [50]. In the first case, the semiconductor is used to convert electrical power in photon emission, while in the second it converts light into electric current. The use of large-area technologies for these applications would cut off a lot of costs due to materials, production and shipment. Solar panels manufactured with these technologies are lighter and rugged; moreover the disposal of old cells would be easier, safer and thus cheaper.

The integration of electronics with plastic polymers enables actuating surfaces as Braille displays [5]. A matrix of organic transistors, similar to a display backplane, is used for pixel addressing. A dielectric elastomer can be bent applying a certain bias voltage to create a Braille symbol. When the ionic polymer-metal composite (IPMC) strip is properly biased, the plastic hemisphere connected to its untied end is pushed against the top surface and can thus be read by the blind person.

Large-area electronics can also be employed together with many kinds of surface sensors, to enable sensing surfaces, like sheet-sensors [10], pocket scanners [51], and others [5], [6], [9], [10], [52], [53]. For this sort of applications, mechanical flexibility plays a much more important role than the single TFT performance. For instance, surface pressure sensors on a bendable plastic foil that can be curved up to a radius of 2 cm were used to realize the first e-skin, providing tactile inputs to a human sized robot hand [7], [8]. Organic light sensors have also been used to realize a portable black&white scanner, where the matrix of light sensors along with their readout transistors was manufactured on a transparent bendable plastic foil. The light shining on the sheet-type scanner can either be reflected by the bright surface or absorbed by the dark colors. Functional peripheral organic ADCs (Analog to Digital Converters) could then be used to convert the current generated by the sensors in a grayscale digital picture.

All these applications give only a flavor of the potential use of large-area electronics on flexible foils. They show indeed how large-area electronics can interact in many different ways with both nature and human beings. It can sense different quantities, transmit electrical signals and irradiate light, and even provide mechanical actuation through dielectric elastomers.

2.2.2 Low-cost applications

Exploiting technologies suitable for large area, many kinds of sensors have been demonstrated, also beyond the domain of smart surfaces. Temperature, strain, chemical, and biomedical sensors [54] can also be used for ultra-low-cost applications like circuits integrated in

packaging at item level. A unique process integrating sensors and electronics paves the way towards disposable smart sensors: systems aiming at the detection of a physical quantity and able to perform simple actions when required.

In these applications the electronic function becomes more important, since many building blocks needs to be designed in order to process the sensor analog signal and make it amenable for post processing. Analog, digital and mixed-signal circuits must be designed based on technologies that are often superficially characterized, affected by large mismatch and process variations, and unstable under bias and environmental aggressions. Once these issues will be overcome, with the help of circuit and technology solutions, we will witness smart sensors integrated in the package of food or pharmaceuticals to test their conservation quality, monitoring the level of bacteria in water, and robots equipped with conformable electronic skin [8] sensing roughness, softness, temperature and other qualities of our world.

Let us consider a smart sensor in the package of food. Every single item in a refrigerating room, or in the trailer of a truck, could detect locally its own temperature. This information could be used for instance to notify the final customer either if the desired product suffered multiple defrosts, or if it was perfectly stored and freshly delivered to the grocery shelf.

A chemical sensor integrated in a can of tomato sauce could reveal an excessive acidity and switch on an expiration LED. Or, in pharmaceuticals, it could monitor some excessive chemical levels in the medicine and communicate the automated storing system to withdraw the item from the market.

In order to perform such activities, the simplest smart sensor only requires a few building blocks (Fig. 2): a sensor, the sensor frontend, and a link to the base station that can perform more complex data processing and control more elaborated actions. In the following, the "sensor frontend" will be investigated as the whole circuitry necessary to convert the sensed data into digital words.

The frontend chain begins with an analog signal conditioning interface: first, to reduce the noise coming along with the signal and introduced by the electronics; second, to amplify the analog signal to a voltage range compatible with the data conversion. These operations are not trivial since the supply voltage of large-area electronics can reach several tens of volts and the intrinsic gain of the transistors is usually low. Moreover the lack of a complementary technology prevents the use of almost all the well-known architectures used in CMOS technology for operational amplifier designs. Indeed, the low intrinsic gain of TFTs makes negative-feedback systems design very challenging, hampering the effectiveness of linearity-enhancement and offset-reduction techniques.

The second step is the analog-to-digital conversion, required to achieve a robust data transmission to the base station. Also in this case, the poor performance of the electronics poses severe hurdles for the design of analog-to-digital and digital-to-analog converters. Even between closely-placed transistors, the process parameter variations and the large TFT mismatch reflect in significant offset at the input of e.g. comparators and OpAmps, hampering their use in ADC topologies like flash or pipelines. Only ADC architectures which are more resilient to comparator offset and exploit the relatively better matching of passives like SARs have been shown in literature, but even in this case the maximum linearity achieved was of about 5 bit [55]. When following oversampling and noise-shaping approaches, the designer has to deal with the low cut-off frequency of the organic transistors, which reflects on a limited gain-bandwidth product in the OpAmps, so that the linearity achieved at the state of the art with these approaches is even lower [35].

Digital building blocks are also required in order e.g. to control the data flow, to restore signal synchronization, or to assist the data conversion. In this case, the limited static performance of the TFTs and the lack of complementary transistors affect the robustness of the digital circuits, resulting in a relatively high chance of non-functional circuits due to both hard and soft faults (i.e. errors due respectively to hardware faults like shorts and lines stuck at V_{DD} or gnd, or simply to excessive parameter variations). For this reason, the design of a robust digital logic is also mandatory.

Nowadays unipolar technologies are by far the most reliable in terms of hard faults and, for this reason, they provide the best solution for complex circuit design. However, with increasing process reliability, also complementary technologies will eventually offer similar hard-yield. At that point, soft faults will limit the maximum circuit complexity and unipolar technologies will need smart solutions to achieve yield levels comparable to the ones that can be achieved with complementary ones. This may still be interesting for practical applications, because of the far cheaper process that unipolar technologies enable.

3 State of the art in circuit design

The technologies that have been developed to address large-area and low-cost applications have been developed very recently and still pose severe limitations to the complexity achievable by integrated circuits. The transistor performance is limited and the process variations still represent a concrete issue with respect to circuit yield. In this chapter, the state of the art of large-area technologies is described, highlighting the main differences with respect to the most common standard silicon technologies. An overview is provided on the effort spent to build up a design flow platform easily configurable to address different and future technologies. The chapter concludes summarizing the state of the art in circuit design, which actually demonstrates all the difficulties that are experienced in this field when exploiting these technologies.

3.1 Introduction

Providing a complete survey of all different large-area technologies is a challenging task. The variety of substrates and semiconductors, deposition techniques and patterning processes is almost countless. Anyway, the most relevant characteristic that all large-area electronics share is the low maximum temperature reached during the manufacturing process (typically below 200 °C). This feature is fundamental to integrate circuits on flexible substrates like paper, fabrics and plastic foils without deforming or damaging them, and it is also mandatory to allow innovative processes as printed electronics, which enable at the same time high throughput and low costs.

Semiconductors processable at low temperatures do not have excellent electrical performance (mobilities are about three orders smaller than those in silicon) and cannot easily be doped [56] in order to select the polarity of the charge carriers. For this reason, the most mature processes are usually unipolar, while the manufacturing of different types of TFTs requires the use of different semiconductor materials [24], [25], [55], [36]. Also, neither diodes nor linear resistors are normally available. The processing of different semiconducting materials on the same substrate to create complementary TFT technologies on foil is complex since the first material deposited easily degrades as a consequence of the second deposition. Only recently significant progress has involved complementary technologies. Some of them exploit printed approaches [25] and also provide resistors obtained through the deposition of carbon pastes. Nevertheless these technologies still suffer from the presence of many hard faults and large variability, which hamper the realization of complex circuits; hence, they have not overtaken the most reliable unipolar processes yet. On the contrary, it is presently a matter of strong debate if complementary technologies are really the right choice for the future of circuits manufactured on plastic films.

Unipolar TFTs are typically manufactured through the deposition and patterning of four functional layers: a gate metal layer, a gate insulator layer, a source-drain metal layer and a semiconducting layer. Depending on the order the different layers are processed, four TFT structures can be defined: planar bottom-gate (PBG), staggered bottom-gate (SBG), staggered top-gate (STG) and planar top-gate (PTG) (Fig. 3).



Figure 3. Different thin-film transistor structures.

Even if staggered structures typically have better contact resistance, since they provide a larger injection surface between source/drain contacts and the semiconductor, it is not possible to simply state which structure is the best. Indeed, on top of carrier injection, several other properties play a role in the overall TFT performance: examples include semiconductor ordering on surfaces with different hydrophobic/hydrophilic behavior or the use of different patterning processes (e.g. printing, photolithography, shadow masking). In general, for one application mobility could be the most important figure of merit of a transistor, for another the cut-off frequency or the longevity. Moreover different structures have different costs and suit better different materials. Indeed, the optimal choice should also be tailored to the specific materials and deposition process used for each layer and keeping in mind thermal budget and stack integrity.

For organic TFTs (OTFTs), the PBG structure is very popular, since this structure can achieve shorter channel length and the semiconductor deposition is the last step of the process. This simplifies the manufacturing process and avoids the degradation of the semiconductor due to further processing. First attempts using metal-oxide semiconductors and graphene also exploited the same structure, however we also assisted to the migration to top contact structures. Moreover this structure provides an attractive solution for printed and roll-to-roll technologies, which achieve at the same time the highest throughput and the lowest cost [57], [58].

Unfortunately the short channel length combined with the weak vertical electric field, due to the relatively thick gate insulator (typically above 200 μ m), causes a large channel modulation in low-temperature TFTs [18], [19]. Moreover, the small surface available for charge injection between contacts and accumulated channel reflects in a high contact resistance [59], [60]. These two effects considerably degrade the static performance of TFTs and the consequences are clearly visible e.g. in the output and transfer characteristics (Fig. 4a and Fig. 4b respectively).



Figure 4. Contact resistance affecting the a) output (Fig. 6 in [61]) and the b) transfer characteristic (Fig. 4 in [62])¹.

The interest in TFTs for display backplane applications also encouraged the research on a process providing a third metal layer [63]. Indeed, in some technologies, two additional layers, an insulator and a third metal layer, are deposited atop, taking care to avoid any degradation of the semiconductor and its electrical properties. The most important drive beyond the adoption of this metal layer was in the fact that it enables a very good aperture ratio² when fabricating display backplanes, as the pixel driver can be covered with the pixel electrode (Fig. 5).



Figure 5. a) Low aperture ratio achieved by two metal layers technology and b) maximum aperture ration achieved by three metal layers technologies.

¹ Currents and voltages are shown in line with n-type conventions, even when the device is a p-type.

² The aperture ratio of a pixel is defined as the ratio between the emitting area over the whole surface occupied by the pixel (including wiring, space between adjacent pixels, and pixel driver)

The same three-metal-layers technology can be advantageously used for circuit design, as the third metal layer can be employed as a second gate (Fig. 6). This additional TFT control terminal is useful to design innovative circuit topologies that can solve some of the issues mentioned in this work. The second gate indeed influences the electrical properties of the semiconductor underneath and hence a tunable-threshold TFT is obtained. This feature is paramount to achieve at the same time a low-cost process and robust circuit designs, as it will be shown in Chapters 6, 7 and 8.



Figure 6. Cross-section of a dual-gate thin-film transistor.

3.2 Design-environment setup

The most important application of large-area electronics is in "active matrices" for display backplanes. In this sort of application, TFTs are exclusively employed as switches that provide the right currents or voltages to the pixels in the display. For this reason, a characterization of the TFT transfer and output characteristics with the level of detail that is needed for the design of complex analog and digital circuits is often not provided along with the technology. Beside this, state of the art compact models are often limited to the DC behavior, are not portable among different technologies, and are not openly available in a standard EDA (electronic design automation) environment.

To enable circuit design with TFTs, which is the focus of this work, a physical model for each of the technologies used for our designs was developed in house. To this aim, the state of the art in the field of physical and compact TFT models [64], [65], [66], [67] was taken as a reference.

In addition to the lack of a unified portable current model, a very important practical problem is that a proper design kit, implemented in a convenient EDA environment for the simulation, layout and verification of our circuits is almost never available. For this reason, a complete design environment for all the technologies used in this thesis was set up from scratch in order to provide at least the basic functionalities required during the most important phases of the physical design (Fig. 7).


Figure 7. Design flow created for all the technologies used for circuit design.

Each TFT technology has been characterized based on the measurements of the transfer and output characteristics of many TFTs with different channel lengths and widths. This is needed to characterize the scaling of the transistor parameters with TFT dimensions and to characterize properties, like carrier injection and short-channel effect, which are strongly dependent on the TFT length. A compact model suitable for each specific technology (e.g. the one described in Chapter 4) is used to extract the parameters, and embedded in a commercial EDA tool by suitably writing it in Verilog-a. The Verilog-a macro is then used within the Spectre simulator. To enable meaningful transient and AC simulations, the main parasitic capacitances were also modeled based on the specific layout geometry of the single device.

The model is then associated to the symbol used in the schematic editor which allows the simulator to fetch the TFT design parameters. These parameters typically define the geometry of the device and can also be read by the PCell (Parameterized Cell). The PCell is used during the layout phase to automatically adjust the dimensions of the different layers accordingly to the design parameter set defined in the simulated schematic and to the layout design rules.

Based on the indications of the technology providers, also the Layout Vs Schematic (LVS) tool and the Design Rules Checker (DRC) were configured to verify our designs and achieve a reliable design flow even for complex circuits.

3.3 Circuit design

In the first large-area applications for flexible electronics, TFTs were mainly used as a switch in active matrices. These switches were used to carry the suitable voltage to pixels in displays or to collect the signal from sensor surfaces [68]. The circuit design was limited to small digital circuits, rectifiers and simple single-stage amplifiers.

The analog and mixed-signal design is a complex design area to tackle with unipolar technologies. Unipolar OTFTs are typically normally-on and this makes impossible to use current

mirrors either as an active load (since it should be complementary to the input) or to provide reference bias currents (since the sink TFT does not work in saturation [29], when diode connected). The gain of a single stage voltage amplifier is usually below a few tens [69], [70] and the phase margin decreases rapidly in multistage amplifiers due to the presence of large parasitic capacitances [35]. Of course nested compensation techniques can be used to achieve stability in negative feedback configurations (achieving unity gain bandwidths typically below 2 kHz [71], [72]), but these approaches dramatically increase the circuit complexity with a detrimental effect on the hard/soft faults, and thus yield. For this reason, even discrete-time amplification techniques are difficult to implement. Indeed, a switched-capacitor amplifier requires voltage amplifiers that are internally compensated and have large gain in order to provide a good virtual ground and to switch quickly between the different phases. Moreover, using unipolar normallyon TFTs, charge pumps to turn the devices completely off are required, and transmission gates cannot be implemented. For this reason normally-on TFTs are an awful solution to implement switches when all voltage levels must be generated within the circuit itself. In display applications indeed, the drive voltage applied to the switches in the active matrix are applied from outside and exploit e.g. large negative voltages in order to completely switch off the n-type TFTs.

Limitations in the stability of multistage amplifiers are not necessarily an issue in open loop circuits like comparators. Nevertheless, comparators for data converters are difficult to realize due to the large mismatch between devices and to the difficulties in the design of offset-zeroing techniques. A differential pair supplied at 30 V can easily reach an input offset of 1 V [70], hence limiting in principle the linearity of analog to digital converters to less than 5 bit in architectures like flash and pipeline converters which, for this reason, have never been demonstrated.

Other attempts to build analog to digital converters concentrated so far on SAR topologies. As expected, however, the matching of passive devices used to implement the DAC [24], [55] limits the linearity of the source reference signal and hence of the SAR converter. In this case, even exploiting a C-2C approach and external calibration and logic, the resulting converter reaches less than 6 bit linearity [36].

An alternative solution to overcome the issues related to low performance OTAs is to exploit oversampling converters. Unfortunately in this case, the low cut-off frequency of TFTs poses a strong limit to the speed of the comparator, which is detrimental for the maximum oversampling factor achievable. For this reason, the $\Delta\Sigma$ modulator reported in [35] achieves an ENOB just a little higher than 4 bit.

In the context of digital design, much more effort has been spent and more relevant achievements have been shown. Digital design with unipolar technologies is however very cumbersome, due to the low intrinsic gain and the availability of only normally-on devices with a single threshold. These limitations result in a poor static behavior of logic gates in terms of gain, symmetry and noise margin. This in turn causes the yield to be too low, which is a concern for single prototypes and much more for mass production of circuits aiming to commercial applications. For this reason, several techniques have been investigated to improve the static characteristics of logic gates manufactured on plastic films, with some benefits and drawbacks.

For instance, in the first plastic RFID demonstrator [11] a diode-load inverter was driven by a level shifter to make the transfer characteristic more symmetrical. Then Pseudo-CMOS logic [73] was applied to many different applications and exploited with different technologies [6], [9], [10] but this approach requires three different supply rails. The lowest supply can be used in principle to counteract unavoidable process parameter variations which are the most important cause of

soft faults. Nevertheless, being a supply, it is cumbersome to design an automatic correction system on chip.

The most impressive results were anyway achieved taking advantage of a double-gate technology. The dual-gate enhanced logic style [74] was indeed used to fabricate the first organic microprocessor [27], counting more than 3,000 transistors on the same foil. This approach exploits the second gate to control the threshold voltage of the pull-up network. Unfortunately the second gate has a weak influence on that parameter. Therefore, voltages even higher than three times the supply (typically 20 V) are required.

In the next chapter, this very same double gate technology will be described more in detail, as it will be used extensively for analog, digital and mixed-signal designs in this work. Firm belief of the author is that a low-defect unipolar technology providing dual-gate feature is the only way to achieve low cost, high density (compared to other large-area electronics solutions) and high yield circuits, all factors needed to enable the adoption of such technology in real life applications.

4 Device modeling and characterization

Any reliable circuit designs is based on compact models able to describe accurately the behavior of the TFTs in a given technology. With our modeling, accurate simulation of analog circuits in a CAD platform is aimed to, and deeper insight in the underlying transport mechanisms is achieved. Thus, a physical model was developed in house that guarantees the continuity and the derivability among the different working regions, ensuring as well the symmetry between source and drain in the channel current. In this chapter, the implemented model will be explained first, and characterized afterwards. Parts of this chapter have been published in [29], [75].

4.1 Transistor model

In the previous chapters, has often been highlighted that semiconductors used for lowtemperature electronics have worse electrical performance compared to silicon technologies. The lower mobility and uniformity are intrinsic consequences of the non mono-crystalline nature of the semiconductor, which is a consequence of the low-temperature deposition methods (as solution processing and RF sputtering) that are suitable to flexible substrates. For this reason, higher mobilities have been measured in TFTs processed at low temperatures, where a selfassembled monolayer (SAM) was deposited before the semiconductor [76]. A SAM can be indeed used to quickly produce a structured substrate and favor ordering of the semiconducting organic molecules [77].

In mono-crystalline semiconductors, atoms in the regular crystal structure interact creating allowed and forbidden energy levels for their electrons, i.e. bands and gaps respectively. Due to the crystalline ordering, these levels are shared over the whole crystal and for all charge carriers, hence they are referred to as *extended* states. With increasing material disorder, the well-known concept of bands (as the valence and the conduction ones) separated by an energy gap needs to be reconsidered, since different phenomena have to be taken into account. For instance, opposite to crystal lattice are polymer materials, where the molecular disorder completely hampers the generation of globally shared energy levels, and charge carriers can only occupy physically *localized* states. In the light of this consideration, also the charge transport has to be supported by different theories.



Figure 8. Multiple Trapping and Release transport in metal-oxide and amorphous semiconductors [**15**].

In the case of amorphous metal-oxides materials, the semiconductor is typically described as a system consisting of valence and conduction bands; however localized energy states in the energy gap can trap the charge carriers. If the majority of the charge carriers remains trapped in these localized energy states, the charge transport in the semiconductor can be modeled by means of the Multiple Trapping and Release (MTR) theory [**15**]. According to the MTR, a trapped carrier can be activated thermally (Fig. 8), and move in the conduction band (CB) until it falls in a trap again.



Figure 9. Variable Range Hopping transport in organic semiconductors [78].

In most organic semiconductors, typically bands are not associated to the system. In this scenario, all the free carriers are trapped in localized states and the charge transport can take place by "charge hopping" between different localized states. This mechanism is referred to with Variable Range Hopping (VRH) [16]. According to VRH, the probability of a hop event depends on the phonon frequency, on the difference in energy between the initial and final state (which can either favor or disfavor the hop), and on the spatial separation between the states (Fig. 9). Other factors also play a role in the hopping probability: the Density of States (DOS) at different energy levels, the free carrier wavefunction, etc. All these factors need to be taken into account when evaluating the conductivity of the semiconductor and writing the expression of the static currents in organic TFTs.

Although the DOS for disordered materials governed by VRH is typically assumed to be Gaussian [79], most models adopt an exponential relation between the number of states and the given energy

$$g(E) = N_t \exp\left(\frac{E}{K_B T_0}\right) \theta(-E)$$
⁽¹⁾

this is a reasonable approximation since the energies involved typically concern the tails of the Gaussian bell, which are very well approximated by an exponential function. In this expression, N_t is the total number of localized/trap states, K_B the Boltzmann constant, T_0 the characteristic temperature (related to the width of the exponential distribution, which accounts for the level of disorder) and θ is the Heaviside unit step function ($\theta(x) = 1$ if x > 0, otherwise $\theta = 0$).



Figure 10. Localized states with respect to energy level of the semiconductor.

This DOS shape has very important consequences in the physical understanding of the current law that will be eventually derived. Let us consider, indeed, two different bias conditions (Fig. 10) such that all localized states are filled up till the energy level E_1 in the first case and up to E_2 in the second, with $E_1 < E_2$. In the first case, the number of carriers that can be thermally activated is much lower than in the second case, and, most important, increasing the base energy level by the same energy step ΔE , an exponentially larger number of localized states can be reached. Due to this phenomenon, the hop probability rises dramatically in the case where the charge carriers have higher energy. Hence, the mobility is not constant, but increases with the energy level of the occupied states in the semiconductor. In a field effect transistor, this means that the mobility increases with the voltage applied to the gate.



Figure 11. a-b) Top-view and c-d) cross-section of a thin-film transistor manufactured with a-c) single and b-d) double-gate technologies.

In order to better understand the mathematical expression of the current, besides MTR and VRH, it is useful to illustrate the most important difference between silicon and unipolar thin-film transistor technologies on foil. This kind TFTs typically work in accumulation and not in inversion. Therefore, even if the semiconductor layer is intrinsic, it causes a major source of leakage current between source and drain, with a detrimental effect on the on-off current ratio. On the other hand, accumulation TFTs are typically normally-on, which is a very important feature to enable reliable circuit design with unipolar technologies, as it will be shown in Chapters 6, 7 and 8. The recurring issue of organic transistors stability in air is also due to this aspect of large-area technologies. Indeed water molecules in the air, are inclined to interact with the semiconductor, and behave like dopants both worsening mobility and threshold voltage (i.e. the on current), and increasing the leakage in the substrate (i.e. the off current). Moreover, since leakage can take place, in a real circuit, also between nearby transistors, the semiconductor is typically patterned and sized within the gate (Fig. 11a) and, when available, within top-gate (Fig. 11b).

In order to find an expression for the TFT channel current, let us consider first the most widely used TFT structure used for large-area electronics, namely the planar bottom-gate one (Fig. 11c). The case of TFTs with double gate (Fig. 11d) will be investigated later. Even if the technology here characterized is p-type-only, for the sake of simplicity the model will be written assuming n-type TFTs. Accordingly to [78], using the coordinate system shown in Fig. 11, the current above threshold can then be derived considering accumulated carriers at the interface between insulator and semiconductor (x = 0), and a current flowing in the y direction from the source (y=0, $V_{ch} = V_s$) to drain edge (y = L, $V_{ch} = V_p$). Applying drift and diffusion relationship:

$$J_n(x,y) = qn\mu_n E + qD_n \nabla n \simeq \sigma(x,y) \frac{dV_{ch}}{dy}$$
⁽²⁾

where σ is the conductivity of the semiconductor, which takes into account the specific DOS and transport mechanism, and V_{ch} is the channel potential. The diffusion term will be neglected here, as a biasing above the sub-threshold region will be assumed, since the main current contribution is due to drift.

The above threshold channel current can be modeled following the standard approach used also silicon technologies. Eq. (2) needs to be integrated in both the x and y directions to obtain the drain-source current

$$I_{DS} = \frac{W}{L} \int_{V_S}^{V_D} \int_0^{t_p} \sigma(x, y) dx dV_{ch}.$$
(3)

Here, W and L are respectively the channel width and the channel length of the device and t_p is the thickness of the semiconductor. After the proper math [80] on the expression of the conductivity, it is possible to write the drain-source current as a function of the charge accumulated in the channel at the source and at the drain contacts (Q_s and Q_p):

$$I_{DS} \simeq \frac{W}{L} \frac{\zeta}{c_i} \frac{T}{T_0} \left[Q_S \frac{2T_0}{T} - Q_D \frac{2T_0}{T} \right]$$

$$\tag{4}$$

where ζ includes all the electrical parameters characterizing the transport, C_i is the insulator capacitance per unit area between the semiconductor and the gate, T is the working temperature of the transistor, and T_0 is a characteristic temperature related to the disorder of the system, i.e. defining the exponential DOS.

In order to express the static current as a function of the voltage applied to the terminals, the charge accumulated at the insulator-semiconductor interface can be written as:

$$Q_X = C_i (V_G - V_{FB} - V_X) \tag{5}$$

where V_G and V_X are the voltages applied respectively to the gate and to the X terminal (source or drain). The voltage V_{FB} is an equivalent flat-band voltage that accounts for the charge neutrality in the metal-insulator organic-semiconductor structure. The model for the drain source current is thus:

$$I_{DS} \simeq \frac{1}{2} \frac{W}{L} \frac{2T}{T_0} \zeta C_i^{\frac{2T_0}{T} - 1} \left[(V_G - V_{FB} - V_S)^{\frac{2T_0}{T}} - (V_G - V_{FB} - V_D)^{\frac{2T_0}{T}} \right].$$
(6)

It is worth noting that the ratio $2T_0/T$ is typically larger than 2. The cause of this exponent in the dependence of the current from the gate voltage is in the variation of the mobility with the gate voltage, which has been discussed above.

This formulation of the channel current holds both for triode and for saturation regions, if the factor $V_G - V_{FB} - V_D$ is neglected when it would become negative, but it does not take into consideration the channel length modulation effect. For this purpose, an additional scaling factor can be included, paying attention to preserve the continuity of the characteristic and its derivatives between the linear and the saturation regions. Also in this case, the procedure to evaluate this additional term is the same as for silicon technologies and it can be expressed as:

$$K_{sat} = 1 + \frac{V_{DS}}{E_{PL}} \tag{7}$$

where the equivalent Early voltage V_p is expressed as the product of the pinch-off field E_p and the channel length L, to enable scaling with the dimensions of the device.

The last two biasing conditions that still need to be taken into account are the sub-threshold region and the finite off-current due to the resistance of the bulk (remind that, as explained before, these devices work in accumulation). The latter can be simply modeled with a shunt resistor between source and drain that scales with the geometrical dimensions of the transistor:

$$I_{off} = \frac{W}{L} \frac{V_{DS}}{R'_{sub}}.$$
(8)

The sub-threshold behavior of these devices is exponential: some attribute the exponential behavior to the diffusion term, others explain it with the dependence of the charge carrier injection probability with the gate voltage. Indeed, the gate voltage strongly affects the energy of the semiconductor in the sub-threshold region and consequently it modifies the barrier height at the metal-semiconductor interface. In any case, the exponential current in the subthreshold region can be empirically modeled writing the overdrive voltages on the source and drain sides ($V_{OD,X} = V_G - V_X - V_{FB}$) as:

$$V_{OD,X}(V_X) = V_{SS} ln \left[1 + exp \left(\frac{V_G - V_{FB} - V_X}{V_{SS}} \right) \right]$$
(9)

This mathematical approach allows to fit the sub-threshold slope to the characteristic of the device using the parameter V_{ss} , and preserves the continuity and derivability of the characteristic above threshold.

In the presence of a second gate, all the above considerations still hold. On top of that, the voltage applied to the top-gate also has an influence. If an accumulation layer is not created between top insulator and the semiconductor, the electric field generated by the top-gate interacts with the one generated by the bottom gate, shifting the onset of accumulation in the channel. Due to the different thickness of the top-gate and bottom gate insulator layers, the top-gate voltage needs to be properly weighted [74]. In presence of the second gate, thus, the V_{FB} used in Eq. (5), (6) and (9) should be substituted by:

$$V_T = V_{FB} - \eta (V_{TG} - V_S)$$
(10)

where the scale factor η is the ratio between the thickness of the bottom-gate and top-gate insulator [63].

4.2 Measurements and characterization

Once the physical model of the current that applies to our technology is defined, the proper value of each parameter needs to be determined based on the actual device measurements. For this purpose, a comprehensive set of devices was designed with different channel lengths and widths. The channel length of the devices was scaled from 5 μ m (the minimum feature size) to 100 μ m in order to investigate contact effects, channel properties and device scalability. On the other hand, in order to measure suitable currents, the channel width was scaled accordingly. Due to the presence of four terminals, three types of characteristics were measured:

- Bottom-gate transfer characteristic (TC)
- Top-gate transfer characteristic (TCTG)
- Output characteristic (OC)



Figure 12. a) Bottom-gate and b) top-gare transfer characteristics, and c) output characteristic of a double gate OTFT with W = 56 μ m and L = 5 μ m¹.

For each case, the independent variable was swept forward and backward in order to identify possible hysteresis and other stress effects, while many measurements have been performed for different bias applied to the remaining three terminals. An example of the three characteristics is reported in Fig. 12.

Despite the variety of phenomena occurring in the OTFT, as discussed in the previous section, the current model can be expressed by means of a compact expression including only seven parameters.

$$I_{DS} = \frac{W}{L} \beta \left[V_{OD,S}^{\gamma} - V_{OD,D}^{\gamma} \right] \left(1 + \frac{V_{DS}}{E_{PL}} \right) + \frac{W}{L} \frac{V_{DS}}{R'_{sub}}$$
(11)

$$V_{OD,X} = V_{SS} ln \left[1 + exp \left(\frac{V_G - V_X - V_{FB} + \eta (V_{TG} - V_S)}{V_{SS}} \right) \right]$$
(12)

where the overdrive voltage has been written separately for the sake of readability. All needed parameters are listed in Table I, together with their typical value for the p-type-only organic technology used in this work and their units.

4.2 Measurements and characterization

	Symbol	Value	Unit
Current prefactor	β	3x10 ⁻¹⁰	[A/V ^γ]
Traps coefficient	γ	2.37	[K/K]
Sub-threshold slope	V _{ss}	1	[V]
Flat-band voltge	V _{FB}	1.2	[V]
Bulk resistance	R' _{SUB}	1x10 ⁺¹⁴	[Ω]
Pinch-off field	Ep	1.5x10 ⁺⁵	[V/cm]
Top-gate coupling	η	0.25	[μm/μm]

Table I. Model parameters for the double-gate p-type organic technology

In order to tailor the model to suit our specific technology, a comprehensive set of routines, described using Matlab, was applied to all measured data. The first step to quickly analyze thousands of measured characteristics was the creation of a uniform scheme for data storage (Fig. 13). For each device, a structured variable was created containing the relevant information about the device (foil, technology, tapeout date, et cetera), all the necessary parameters, and all the measured data (organized by characteristic type). In the multidimensional array, each plane contains the current and voltage values measured or applied to each terminal during the measurement of a single characteristic. In this plane, each row corresponds to a point of the characteristic (red box in Fig. 13), hence for each row Kirchhoff's laws can be verified and used to check the data consistency. Different planes are data collections that have been retrieved for instance at different times or different bias. Accordingly to the characteristic type each plane is then stored in the right sub-variable (OC, TC or TCTG).



Figure 13. Structured variable used in Matlab for quick semi-automated characterization.

Based on this data structure, a specific value for each parameter listed in Table I was identified for each measured device. The output characteristic was used to detect the pinch-off electric field E_p , the top-gate transfer characteristic to estimate the top-gate coupling factor η and the bottom-gate transfer characteristic for all the other parameters.

The extraction routine also allows to store in the proper location the values of the parameters that fit the model to each device. Due to the variability of the technology, every device has a different set of parameters. Hence, in order to choose the value which is most representative for the technology, the median value of each parameter was picked. The median provides the best statistical estimate of the mean value when the central limit theorem cannot be applied due to a limited data set, since it effectively excludes the outliers.

4.2.1 Parameters extraction

In this section, the extraction of the parameters for a typical device will be discussed. For the sake of synthesis and simplicity, the case of transfer characteristics measured in the saturation region will be detailed, however similar considerations hold if the device under test works in its linear region. The semi-automatic routine can detect the correct algorithms to be applied based on the fetched bias of the device and on the extracted threshold voltage.



Figure 14. The blue line shows the measured OC used for the evaluation of the pinch-off field E_p . The red line fits the saturation region of the characteristic and allows the estimation of the Early voltage V_p . Dashed lines show the interpolation range1.

The only parameter that can be extrapolated from the output characteristics of the device under test is the Early voltage V_P. For a low bias of V_G and of V_{TG}, and around the highest drain voltages applied to measure the OC, the TFT surely works in saturation. In that region (see Fig. 14), the OC can be extrapolated with a straight line crossing the horizontal axis in V_{DS} = -V_P. In order to extract a parameter value independent of the channel length, the equivalent pinch-off electric field E_p can be obtained simply dividing V_P by the channel length of the measured device.



Figure 15. Traps coefficient evaluation. The blue line represents the function $w = w(V_{GS})$ (Eq. (13)) based on the measured TC in Fig. 12a. The red line is the linear fit in the saturation region, between 0 V and 15 V1.

4.2 Measurements and characterization

The first parameters that can be extracted from the transfer characteristic of a device are the traps coefficient γ and the threshold voltage V_T . For this purpose, can be used the function $w = w(V_{GS})$ defined as [81]:

$$w = \frac{\int I_{DS} dV_{GS}}{I_{DS}}.$$
(13)

Indeed, when the TFT works in saturation, using Eq. (11), Eq. (13) can be approximated by:

$$w_{sat} = \frac{V_{GS}}{\gamma + 1} + \frac{V_T}{\gamma + 1}.$$
 (14)

In Fig. 15 the evaluation of w based on a measured TC is shown. In the sweep region between $V_{GS} = 0$ V and $V_{GS} = 15$ V the OTFT works in saturation since $V_{DS} - V_{GS} > V_T$ and $w \simeq w_{sat}$. Approximating $w = w(V_{GS})$ with a straight line $y = mV_{GS} + q$ (red line in Fig. 15), can be immediately derived

$$\gamma = \frac{1}{m} - 1. \tag{15}$$

$$V_T = -\frac{q}{m}.$$
 (16)

It is worth noting that this threshold voltage is not one of the seven parameters, but it is a function of V_{FB} and η , whose values will be evaluated later in this section.



Figure 16. Evaluation of the prefactor β . The continuous line is obtained through the manipulation of the z function, while the dashed line is its average within the range of interest1.

In a way similar to the evaluation of γ , it is possible to estimate the prefactor β . In this case can be used the function:

$$z = \frac{\int I_{DS}^2 dV_{GS}}{I_{DS}}.$$
 (17)

Over the same gate voltage range where the traps coefficient has been extracted, we can also identify a $z_{sat} = z_{sat}(V_{GS})$ approximation of $z = z(V_{GS})$:

4.2 Measurements and characterization

$$z_{sat} = \frac{W}{L} \frac{\beta}{\gamma + 1} (V_{GS} - V_T)^{\gamma + 1}$$
(18)

Therefore, dividing the z_{sat} by $\frac{W}{L} \frac{1}{\gamma+1} (V_{GS} - V_T)^{\gamma+1}$, the value of the prefactor β is obtained. The value of β as a function of V_{GS} is shown in Fig. 16 along with its average value (dashed line).



Figure 17. Evaluation of the sub-threshold slope V_{SS} 1.

For the evaluation of the sub-threshold slope V_{SS} , the first aspect to highlight is that the slope of the logarithm of the sub-threshold current (see TC of Fig. 17) is, in the case of saturation regime, proportional to $1/V_{SS}$. Indeed while in saturation, the Eq.s (11) and (12) of the drain-source current can be simplified to:

$$I_{DS,SS} \simeq k V_{SS}^{\gamma} ln \left[1 + exp \left(\frac{V_{GS} - V_T}{V_{SS}} \right) \right]^{\gamma}$$
⁽¹⁹⁾

where k includes the geometry of the device W/L, the prefactor β and the channel length modulation factor (V_{DS} is constant during the measurement of the TC). Moreover, the argument of the exponential is much smaller than zero, hence the logarithmic expression can be replaced with the exponential only (ln(1+x) \simeq x when x \simeq 0) resulting in:

$$I_{DS,SS} \simeq k V_{SS}^{\gamma} exp\left(\gamma \frac{V_{GS} - V_T}{V_{SS}}\right).$$
⁽²⁰⁾

Applying the base 10 logarithm to both sides, a linear function of V_{GS} in the semi-logarithmic plane Log(I)- V_{GS} is obtained:

$$Log(I_{DS,SS}) \simeq \gamma Log(kV_{SS}) + \frac{\gamma Log(e)}{V_{SS}} (V_{GS} - V_T).$$
⁽²¹⁾

The green line of Fig. 17 ($y = mV_{GS} + q$) approximates the characteristic exactly in the region of interest, hence the sub-threshold slope V_{SS} can be expressed through its angular coefficient m and reads:

$$V_{SS} = \frac{\gamma Log(e)}{m}.$$
 (22)



Figure 18. Evaluation of the coupling factor η . The thick line represents H evaluated from measured data, while the thin line represents a credible extension of H for an input range larger than V_{TC}^* 1.

The top-gate coupling parameter models the effect of the voltage applied to the top-gate on the drain-source current. Therefore, this parameter was evaluated based on the top-gate transfer characteristic. In this case, for each measured point within the top-gate sweep, the value of η is found such that the modeled current equals the measured one. However, since the extracted value of the flat-band voltage V_{FB} is still missing, it was expressed as a function of V_T and η :

$$V_{FB} = V_T + \eta (V_{TG}^* - V_S)$$
(23)

where V_{TG}^* is the voltage applied to the top-gate when the TC used to evaluate γ and V_T was measured. Since the TCTG is measured in saturation, the modeled drain-source current, i.e. Eq. (11) and Eq. (12), to be compared with the measured TCTG, can be rewritten as:

$$I_{DS} = k \left[V_G - V_S - V_T + \eta (V_{TG} - V_{TG}^*) \right]^{\gamma}$$
(24)

where k is the same prefactor as used in Eq. (19). Aware of Eq. (23), to evaluate η a functional H can be defined equal to

$$H = \frac{\sqrt[Y]{I_{TCTG}/_{k} - V_{GS} + V_{T}}}{(V_{TG} - V_{TG}^{*})}$$
(25)

where I_{TCTG} represents the measured data. Figure 18 plots H obtained from the TCTG data shown in Fig. 12b and for a threshold voltage V_T extracted applying $V_{TG}^* = 20$ V. Equation (25) draws a hyperbola in the H-V_{TG} plane with asymptotes in $V_{TG} = V_{TG}^*$ and H = η (i.e. value to be used in the final model). Since the measured data in Fig. 12b have been obtained for a top-gate voltage range lower than the vertical asymptote, $\eta = H(V_{TG} = -20 \text{ V})$ was chosen. In the case of an input

voltage range sweeping across the vertical asymptote, η can be computed as the average between the extreme values $\eta_1 = H(V_{TG,min})$ and $\eta_2 = H(V_{TG,max})$.



Figure 19. Evaluation of the bulk resistance R'_{sub} 1.

The last parameter to be extracted is the bulk resistance, R'_{sub} . Its value can be estimated by the off-current I_{off} measured in a TC (Fig. 19). The only remark about this parameter is that many devices should be measured in order to be sure that the lowest value of the current is indeed the off-current of the transistor, scaling accordingly to W and L, and not the noise related to the measurement setup. Referring to Fig. 19 and in line with Eq. (8), R'_{sub} is given by:

$$R'_{sub} = \frac{L}{W} \frac{V_{DS}^{*}}{I_{off}}$$
(26)

where V_{DS}^* is the voltage applied between drain and source during the measurement of the TC.



Figure 20. Comparison of the characterized model (red dashed line) with the measured a) TC and b) TCTG (blue line). The insets show the percentage error1.

After the extraction of all parameters, the agreement between the measured data and the model can be evaluated. Figure 20 shows the transfer characteristics sweeping both bottom-gate and top-gate (blue lines) together with the modeled characteristic (red dashes). In the inset, the error percentage is shown on a logarithmic scale.

The model was then validated for all the measurements performed on the same device. In Fig. 21 each panel shows, together with the top-gate voltage, the TCs measured for three different drain-source voltages ($V_{DS} = 2 V$, 10 V and 20 V). Figure 22 shows different TCTGs obtained with the same drain-source voltages as before and for four different gate-source voltages (reported in the inset). The OCs measured for $V_{GS} = 0 V$, 2 V, 10 V are shown in Fig. 23. In these three figures (Fig. 21, 22 and 23), the measured data are represented with a blue line, while the model is plotted in red.



Figure 21. Model validation over all the measured TC of the device characterized1.

4.2.2 Dynamic behavior

The characterization of the technology so far illustrated only takes into account the static properties of the transistor behavior. In order to perform transient simulations however, overlap capacitances between gate, source and drain (Fig. 24) have also been introduced in the model. Both gate-source and gate-drain capacitors consist of a constant component $C_{overlap}$ due to the overlap between gate and contact fingers (much larger than in self-aligned silicon technologies), and of a variable component depending on the channel accumulation state.



Figure 22. Model validation over all the measured TCTG of the device characterized1.



Figure 23. Model validation over all the measured OC of the device characterized1.

These parasitic capacitors influence the dynamic behavior of the TFTs. Also for TFTs manufactured at low temperature, the cut-off frequency is proportional to the ratio between transconductance g_m and input capacitance C_i [82]:

$$f_t = \frac{g_m}{2\pi C_i} \tag{27}$$



Figure 24. a) Stack and b) layout of the implemented double-gate TFTs.

However, contrary to self-aligned technologies, overlap capacitances are not negligible and they should also be taken into account when evaluating the maximum cut-off frequency, especially for minimum channel length devices. For this reason, a scale factor, depending on the number of sub-channels SC, needs to be included to take into account the source and drain overlap capacitances. Since the minimum finger width FW and the minimum channel length L typically have same dimensions (FW = $L_{min} = 5 \ \mu m$ for our lithography process), the maximum cut-off frequency can be expressed as:

$$f_{t,max} = \frac{g_m}{2\pi C_i} \simeq \frac{SC}{2SC+1} \frac{\mu(V_G - V_T)}{2\pi L_{min}^2}$$
(28)

where the scaling factor depending on SC ranges between 1/3 and 1/2. The relatively thick gate dielectric used in TFTs on foil (from 100 nm to 1.5 μ m typically) requires overdrive voltages around 10 V to obtain sufficient currents. Therefore, large-area TFT cut-off frequency results are limited to about 200 kHz (i.e. most advanced silicon MOSFETs have a cut-off frequency in excess of hundreds GHz).

The final capacitance model considers in detail the device geometry specified in the parameterized cell (PCell). For instance, the PCell developed for our CAD system only accepts an even number of sub-channels SC (see Fig. 24b), leading thus to a smaller gate-drain capacitance C_{GD} compared to the gate-source C_{GS} one:

$$C_{GS} = C_{GD} \left(1 + \frac{2}{sc} \right). \tag{29}$$

In a double-gate TFT, the parasitic capacitances between top-gate and channel, source and drain have, in first approximation, the same geometry as the ones associated to the gate contact. However, the different thickness of the insulator requires an additional scale factor which is once more the top-gate coupling factor η . Therefore, the top-gate capacitances result:

$$C_{TGX} = \eta \ C_{GX} \tag{30}$$

where the subscript X represents any among source (S), drain (D) and channel (ch). All the required parasitic capacitances are taken into account by the Verilog-a model simply including a capacitance between each terminal pair.

The final model was implemented in the environment setup and used for static and transient simulation, helpful to the design of the circuits shown in the next chapters. The statistics concerning matching and variability are not available yet from manufacturers, these aspects of the modeling fall out the scope of this research activity. However in the future, improved versions of this model will integrate the characterization of process variations, indeed the Verilog-a model can easily parse parameters from the design environment. To make Monte Carlo simulations possible, a Spectre model including the Verilog-a one can be used. Spectre will generate automatically, for each transistor in the schematic, a unique parameter set in line with the average and the standard deviation of every parameter in the Verilog-a model.

5 Sensor frontend architecture

In this chapter, the three main functional blocks in the smart sensor (analog signal conditioning, analog to digital conversion, and logic) are analyzed. It will be shown that most of the system, architectural, and circuital choices must be based on technology constraints and not on the target application, as it usually happens in standard technologies. First the analog signal conditioning chain is considered from a system point of view, choosing an architecture suitable for our dual-gate p-type only TFT technology. A deeper insight into analog interface limitations and solutions will be given in Chapter 6. Next, the reasons for choosing an integrating ADC are discussed. In Chapter 7, experimental data will confirm that this approach performs very well when compared to prior art solutions. Eventually, an extensive analysis on the state of the art in digital logic styles is carried on, and the main objectives for a new logic style which is robust to TFT variability are drawn. In Chapter 8, this new logic will be presented in detail and characterized with extensive statistical measurements.

5.1 Analog signal conditioning

In smart sensor applications, the analog signal coming from the sensor needs to be converted and sent to a base station where, taking advantage of higher computational power, data can be processed to extract meaningful information. Conversion to a digital format that enables robust radio transmission to the base station is essential to enable a practically usable system. Before doing so, the analog signal needs to be amplified and filtered to improve, or at least preserve, the signal to noise ratio (SNR) present at the sensor output, and to adjust the signal to the dynamic range (DR) of the analog-to-digital converter. This is called signal conditioning (Fig. 25).

Ideally, the transfer function of the whole conditioning chain is independent of the ordering chosen for the main functional blocks (i.e.: amplification, filtering, and sampling), but in practice a suitable order in the actual implementation must be chosen, taking into account the specifications and the limitations arising from the chosen technology. In sensor applications, typically the signal is first amplified and then filtered, sampled and quantized (Figure 25a). In this way, the noise introduced by the electronics after the low-noise amplifier affects the SNR at the input of the signal conditioning chain only in a negligible way.



Figure 25. Two possible signal conditioning chains.

However, also other factors play a role in the quality of the analog signal processing and of the analog-to-digital conversion. In large-area electronics, for instance, it is very difficult to implement continuous-time amplifiers with sufficient gain and linearity: indeed linear resistors are typically not available, the TFTs have low intrinsic gain, and often only normally-on p-type transistors are available in a given technology.

In order to achieve enough gain to enable negative feedback circuits, the cascade of many amplifiers should be exploited. However, in unipolar technologies it is very cumbersome to match the DC output of one stage with the DC input of the following stage, resulting in a small gain improvement with increasing number of stages (e.g. from single to three stage amplifier respectively 12 dB, 20 dB, and 23 dB [35], [71], [83]). Each stage, however, introduces additional singularities in the transfer, with a detrimental effect on the stability of the circuit when a

feedback is applied. For this reason, nested compensations would be mandatory causing a strong increase in the circuit complexity and a drop in circuit reliability. The DC level issue can be solved by exploiting complementary technologies. However, the large TFT threshold voltage often experienced in this kind of processes demands supply voltages as large as 50 V, while the large parasitics typical of these technologies limit the gain bandwidth product in amplifiers to a few tens of Hz [72].

In Chapter 6, is demonstrated a discrete-time amplifier which is based on a new device acting as parametric capacitor. This solution enables in our technology a gain of 20 dB, without detrimental effect on speed, and it is suitable for a larger input common mode range. This is possible because the amplification is achieved without charge transfer between different capacitors, but just by changing the value of the capacitor itself. As the gain of the parametric amplifier is only related to two capacitance values, the linearity is intrinsically guaranteed for any input voltage.

This interesting approach to improve the gain with negligible loss in speed and linearity is intrinsically discrete-time, and thus it can be implemented only after sampling, as will be discussed in more detail in Chapter 6. For this reason, a continuous time filtering is mandatory at the input of the conditioning chain, to avoid aliasing effects. Therefore, in this work is proposed the signal processing chain schematically shown in Fig. 25b.

In Chapter 6, for each function in Fig. 25b, a circuit design specifically adapted to our doublegate unipolar technology is proposed. On the one hand, our designs improve the robustness of the circuits against hard/soft faults and mismatch, favoring circuit simplicity and compactness. On the other hand, electrical tunability is proposed as a solution to counteract process parameter variations and aging.

The anti-alias filter is embodied by a G_mC filter that exploits a tunable transconductor made of only five double-gate TFTs. The transconductance of the circuit is tunable over one order of magnitude providing resilience to process parameter variations and control on the cut-off frequency of the filter. Unfortunately, the solution proposed is open loop (due to the difficulty to create large gain and to use feedback stabilization in our technology). As the filter in our discrete-time implementation of the signal conditioning chain is preceding the signal amplification, linearity issues due to the amplitude of the signal should be negligible. It is true, however, that the DC level of the signals that can be handled by the proposed G_mC filter is limited and signals having a DC component close to the ground or to the power supply level must be avoided. All details of the proposed G_mC filter are discussed in Chapter 6.

The filtered signal is then sampled on the parametric capacitor in the first synchronous phase and amplified in the second phase, as will be discussed in more detail in Chapter 6. Then the discrete-time analog signal can be fed to the quantizer which converts the analog sample into a digital word.

5.2 Data conversion

The design of data converters represents a delicate topic in any manufacturing technology due to their mixed-signal nature. Indeed this kind of circuits link different signal domains, converting a continuous-time and continuous-amplitude signal into a discrete-time quantized word (analog to digital converter - ADC), or vice versa (digital to analog converter - DAC).

In order to preserve the signal to noise and distortion ratio (SNDR) of the input signal, the converter should satisfy specific requirements in terms of resolution, linearity and speed. According to the application addressed and to the properties of the process in use, different architectural and circuit solutions can be chosen to favor one requirement or the other.

In the sphere of flexible electronics, speed is not an essential issue since the quantities that must be sensed in these applications are most often quasi-static (temperature, chemical levels, large-area strains, etc...). For this reason, the few examples of ADC and DAC in the state of the art focus on resolution and linearity.



Figure 26. Building block schematic of an ADC based on a DA in the feedback.

A large category of ADCs are based on the comparison between the output of a DAC and the analog input, according to the general architecture shown in Fig. 26. For this class of ADCs, resolution and linearity are limited by the characteristics of the DAC used. In the DAC, a suitable reference is usually divided in smaller parts using matched unit elements (passives, like resistors and capacitors, but also actives, like TFTs). Due to the poor matching offered by the available passives and especially by the TFTs in large-area technologies manufactured at low temperature, ADCs built following this approach led, at the state of the art, to a maximum integral nonlinearity (INL) of 2.6 LSB at 6 bit resolution level [36]. In particular, a 6 bit resolution DAC exploiting a C-2C approach [36] or a current-steering topology [24], have been demonstrated. In the case of the C-2C DAC, the converter was also used to realize a successive approximation register (SAR) ADC [36]. The non-linearity before calibration was larger than 3 LSB, and calibration was performed using external logic controlling an additional integrated 2 bit thermometric coded DAC. At last, a maximum INL of 0.6 LSB @ 10 Hz and 1.5 LSB @ 100 Hz is achieved. More recently also an ADC based on an integrated, printed R-2R DAC has been demonstrated [28]. The DAC ensured good linearity (0.4 LSB linearity at 7 bit resolution level in the most recent reports [84]), but it was limited to only 4 bit resolution due to the low level of circuit complexity that can be achieved with acceptable yield in the state of the art complementary organic technology used for this design.

In the architectures that can be described according to Fig. 26, the ADC resolution is equal to the resolution of the DAC. A well-known method to increase the ADC resolution far beyond the resolution provided by the DAC is the use of oversampling and noise shaping, exploiting the feedback architecture schematically depicted in Fig. 27, which is called a $\Delta\Sigma$ modulator. This converter topology performs well when OTAs with large gain-bandwidth product and good DC

AD Converter

gain (typically above 40 dB) are available, to create a loop filter with sufficient gain at the (over)sampling frequency.

Figure 27. Building block schematic of a first order $\Delta\Sigma$ modulator used as an AD converter.

DAC

Unfortunately, this is difficult to achieve using large-area electronics on foil. As a consequence of the small GBW available from OTAs manufactured with OTFTs (even when using complex multi-stage amplifiers [35]), the oversampling ratio is low, limiting the effectiveness of the $\Delta\Sigma$ approach. On top of this, the filter order is limited, because of the maximum circuit complexity that can be achieved with reasonable yield, limiting even more the advantage of using a $\Delta\Sigma$ structure. The equivalent number of bits obtained by the only example available in literature of a $\Delta\Sigma$ modulator made with OTFTs on foil was thus slightly higher than 4 bit [35].



Figure 28. Building block schematic of a dual-slope integrating ADC and time behavior of the integrator output.

A special case of DAC-based ADCs is represented by the dual-slope integrating ADC (Fig. 28). This topology is intrinsically robust to mismatch, since the conversion is provided as a ratio in the time domain, based on a stable reference in the time domain, the clock period, T_{clk} , rather than in the amplitude domain. During a first phase, the analog signal to be converted is integrated for a fixed number of clock periods. In the second phase, the integration of a reference analog signal is subtracted from the final value obtained in the first phase, and the number of clock cycles needed to zero the output of the integrator (N in Fig. 28) provides (together with the number of cycles in the first counting phase) the converted data. Following this approach, the matching problems in the integrator can be cancelled out and all the design effort can be focused on the linearity of the integration process.

A similar approach was followed in this work, further aiming a reduction of the complexity of the converter and the area occupied. The solution proposed is a VCO-based ADC, where the analog signal is converted in a proportional frequency by a linear VCO. The integration of this output in a counter for given, fixed time, returns a quantized value proportional to the signal to be converted. This ADC requires only two building blocks: a VCO and a digital counter, moreover, the converter is not affected by TFT mismatch (see Chapter 7). However, it requires a stable time source, i.e. an integration time which is constant over the single measurement interval. This is the only constraints imposed by the system if the gain and offset correction approach suggested in Chapter 7 is followed. Under this approach, two integration times are required to generate the reference and one to convert the signal. If the stability of the time source is known to be sufficient over long enough times, more consecutive signal conversions can be performed with only one reference generation.

The proposed ADC stands out for its simplicity. Indeed, the reduced complexity allows a much more compact design compared to the state of the art ADCs, and can improve the linearity beyond state of the art performance even without calibration. A more detailed discussion on this data converter will be given in Chapter 7.

5.3 Robust digital blocks

Digital circuits are important in almost every integrated circuit, addressing the most diverse applications. In some cases, they implement the core functionality of the circuit (e.g. with finite-state machines, CPUs, ALUs, code generators, shift registers, digital filters, and many more basic building blocks), while sometimes they assist analog circuits (as it is the case of the VCO-based ADC presented in Chapter 7) or they implement control and synchronization tasks.

Unfortunately, the same characteristics of large-area technologies that pose strong limitations on the performance of analog signal conditioning and data conversion functions, cause poor static performance in digital circuits, typically resulting in low gain and limited noise margin in the logic gates. For this reason, alternative logic styles must be developed to ensure better static performance and higher robustness by exploiting suitable circuit techniques.

The poor static performance of large-area digital electronics on foil eventually results in bad yield. Indeed, each logic gate in a digital circuit should ensure a sufficient noise margin, if the complete digital circuit must have a high probability to operate correctly. However, this may not be the case due to the combination of large TFT variability and small noise margin that is observed in unipolar logic gates for large-area low-temperature technologies.

Many different definitions of noise margin are available in literature [85]: for all of them however, both a large gain and a symmetric input-output characteristic are required to achieve high noise margin. In this thesis, is adopted the Maximum Equal Criterion (MEC) that defines the noise margin as the side of the maximum square that can be inscribed between the static input-output characteristic and its mirrored version.

A simple way to design an inverter in a p-type-only technology is to use a common-source TFT for the pull-up and a TFT in diode configuration to implement the pull-down (Fig. 29a, inset). This inverter is rather fast, as both the pull-up and the pull-down actions are performed by strongly-on transistors. However, due to the small output resistance (in the order of 1/gm) the maximum gain of this inverter implemented in our technology is just about two. Due to the normally-on nature of our TFTs, the trip point is located around 3/4 V_{DD}. This fact, in combination

with the small gain, results in a noise margin (NM) close to 0 V (Fig. 29a and Table II). For this reason, a level shifter in front of the diode load inverter is often mandatory to make the transfer characteristic of the inverter more symmetrical and increase the noise margin [11].



Figure 29. Schematic and transfer characteristic of a diode loaded inverter a) without and b) with level shifter. Dashed lines show the mirrored characteristic.

The experimental transfer characteristics of two diode load inverters manufactured in our technology without and with level shifter are shown, together with their schematics, in Fig. 29a and Fig. 29b. Due to the gain lower than 6.4 dB, the measured noise margin is in both cases zero.



Figure 30. Schematic and transfer characteristic of a Zero-Vgs loaded inverter a) without and b) with level shifter. Dashed lines show the mirrored characteristic.

A first solution to improve the static noise margin of the previous inverter topologies is to replace the diode load with a Zero-Vgs connected TFT working in saturation (Fig. 30a). The

increased output resistance and thus the larger gain improves the noise margin, but the time response is slower due to the weak pull-down action. For the Zero-Vgs load inverters with and without level shifter (Fig. 30a and Fig. 30b), the measured gain was respectively of 11.6 dB and 13 dB. However the maximum noise margin decreased from 3 V to 2.8 V due to the excessive shift provided by the level shifter, which had in practice different TFT parameters from the ones used to simulate the design (Fig. 30 and Table II).

Despite this problem that was due to excessive variability, the use of a level shifter appears an effective solution to centre the inverter's characteristic within the input range. This is especially true if the shift can be controlled to cope with the actual TFT parameters.



Figure 31. a) Schematic of a Pseudo-CMOS inverter. b) Schematic of a dual-gate enhanced inverter with diode (left) and Zero-Vgs (right) load.

Another interesting approach to design unipolar logic circuits exploits a two-stage inverter (Fig. 31a) [86], also called a pseudo-CMOS inverter. The output transistor M4 of the second stage is driven by a diode load inverter (M1-M2) supplied by V_{DD} and V_{SS} (which is below the ground voltage, gnd). In this way, when the input is low and M3 pulls the output up to the high logic state, the internal voltage V_i disables the pull-down action of M4, pulling its gate up. On the other hand, when the input is high, V_i goes low and M1 brings the gate of M4 below gnd, pulling effectively the output node to ground.

Since both pull-up and pull-down actions are performed in this inverter by a strongly-on TFT, both good dynamic characteristics and a reasonable gain (15.6 dB [86]) can be achieved. The main disadvantage is that to achieve a good noise margin (trip point at 7 V and NM = 2.5 V [86]) this configuration needs a large negative supply ($V_{ss} = -24$ V), hence the design of a circuit able to automatically control the value of V_{ss} to adjust the trip point of the inverter is not trivial and must include switching power-management circuits.

The last noteworthy logic style used for TFTs on foil is the dual-gate enhanced inverter [74] that exploits the double-gate technology presented in Chapter 4 to shift the transfer characteristics on the input-output plane. The load TFT can be either diode or Zero-Vgs connected (Fig. 31b). The simple idea behind the dual-gate enhanced logic is to use the top-gate bias V_{bg} to vary the threshold voltage of the pull-up TFT, making it a normally-off transistor, and

thus shifting the inverter transfer characteristic to the left, towards the center of the input range. This approach provides outstanding results in terms of symmetry of the transfer characteristics: choosing V_{bg} suitably, it is indeed possible to shift the trip point exactly to the center of the input range, improving dramatically the noise margin (NM ~ 1.4 V for diode load and NM ~ 6 V for Zero-Vgs load [**74**], see Table II). Unfortunately, due to the weak effect of the top-gate voltage on the TFT threshold, large values for V_{bg} , typically above V_{DD} , are needed. Moreover the top-gate bias reduces the gate overdrive of the pull-up TFT and hence the speed of the pull-up action.

	Diode Load ⁽¹⁾		Zero-Vgs load ⁽¹⁾		Pseudo CMOS	Dual-gate enhanced		PLS ⁽¹⁾
	w/o LS ⁽²⁾	w LS ⁽²⁾	w/o LS ⁽²⁾	w LS ⁽²⁾	-	Diode	Zero-Vgs	-
Supply	20 V	20 V	20 V	20 V	20 V	20 V	20 V	20 V
NM	-	-	3 V	2.8 V	2.5 V	1.4 V	6 V	8.2 V
Gain	6.4 dB	1.6 dB	13 dB	11.6 dB	15.6 dB	6 dB	20 dB	76 dB
V _{trip}	15 V	10.5 V	13 V	6 V	7 V	10 V	10 V	10 V
V_{high}	18.6 V	17.5 V	19 V	17.7 V	19.9 V	16 V	18 V	19.5 V
Vlow	4.2 V	4.7 V	0.1 V	0.4 V	0.1 V	0.1 V	0.1 V	0.1 V
L _{min}	5 µm	5 µm	5 µm	5 µm	5 µm	5 µm	5 µm	5 µm

Table II. Benchmark among state-of-the-art logic styles applied to similar technologies

(1) Fabricated in the same double-gate technology (2) Level Shifter

Reviewing the most popular state-of-the-art logic styles used with TFT processed at low temperature, it was shown that high gain and a symmetrical transfer characteristic are required to achieve large noise margin in an inverter. Moreover, in a large digital circuit, each logic gate should have sufficient noise margin to guarantee robust functionality and enable good yield in spite of the variability of TFT parameters. For this reason, a circuit technique allowing postfabrication tuning of the trip point to maximize the noise margin would be very beneficial to manufacture on foil digital circuits of some complexity and still acceptable yield. The solutions known from prior art and discussed in this section require tuning voltages outside the supply range, which are cumbersome to generate in typical large-area applications, as they require switching circuits and large, high-quality passives. In fact, the pseudo-CMOS inverter requires a negative supply as large as $V_{SS} = -24 V$ (with $V_{DD} = 20 V$), while, in line with the V_T in Eq. (10), to shift the dual-gate enhanced inverter characteristic of $\Delta V_{trip} = 8 V$, and center the input-output characteristic (Fig. 7 in [**74**]) in the supply range, the top-gate of the driver should be biased at $V_{bg} = V_{DD} + \Delta V_{trip}/k \sim 52 V$.

To avoid the need for additional complexity and allow self-correction on chip, a new logic style is proposed that exploits positive feedback to enable tuning voltages within the supply rails while ensuring higher gain and larger tunability of the input-output characteristic than state of the art solutions. The details of this new logic style will be described in Chapter 8.

6 Circuit design for analog signal conditioning

In Chapter 5, have been explained the architectural choices for the design of the signal conditioning chain for smart sensors based on the application addressed and on the electrical characteristics of the TFTs manufactured on foil. In this chapter, each of the blocks in the signal conditioning chain is discussed separately, providing a deeper insight in the technology-aware circuit design techniques that have been developed to improve robustness and performance. Following the signal through the front-end path, the low-pass filter is introduced first, and then the continuous-time and the discrete-time amplifiers. Parts of this chapter have been published in [29], [30], [32], [31].

6.1 Filter based on a tunable transconductor

Emerging technologies on foils still have huge room for improvement in terms of transistor performance, process uniformity, matching and stability. Indeed, the reliability of the process and the performance of TFTs are much inferior to what analog designers are used to in standard silicon technologies. In light of this consideration, the continuous-time low-pass filter, which is needed at the input of the signal conditioning chain for the reasons explained in Chapter 5, was designed targeting low circuit complexity, and enabling electric tuning to provide resilience to the large process variation typical in large-area electronics.

6.1.1 The proposed G_mC filter

A G_mC filter is a continuous-time low-pass filter that, in its simplest implementation, employs only a transconductor and a capacitive load (Fig. 32a).



Figure 32. a) Schematic of a G_mC filter and b) its transfer function $v_{out}/v_{in}.$ In a real implementation, the output resistance limits the DC gain of the circuit.

The small-signal output current i_{out} is proportional to the small-signal input voltage through the transconductance G_m of the transconductor (not to be confused with the TFT transconductance g_m). The output current is afterwards integrated by the loading capacitor and thus converted in the output voltage v_{out} (signals will be expressed as $v_x = V_x + v_x$, that is the sum of a DC component V_x and a small signal v_x). Due to the integration operation, the amplitude Bode plot of the voltage transfer v_{out}/v_{in} (Fig. 32b) has a -20 dB/dec slope and crosses the 0 dB amplification line at a frequency proportional to the ratio between transconductance G_m and the loading capacitance C_L . Moreover, at the output node there is always a resistive load R_L (typically due to the channel length modulation of the transconductor output devices) which limits the DC gain at low frequencies.

The block diagram of the GmC filter proposed in this thesis is shown in Fig. 33a. A voltage buffer is used to apply the input voltage to a linear resistor R. In the case of an ideal buffer and current mirror (which have zero output and input impedance, respectively), the whole input voltage drops over the linear resistor and the current that is generated is mirrored to the output port using the output branch of the mirror, which is loaded with the capacitor. Therefore, the ideal transconductance of this circuit is:

$$G_{m,ideal} = \frac{1}{R}$$
.

(31)

In the transistor level implementation of the circuit (Fig. 33b), transistor M1 implements the buffer, the current mirror is made of M3, M4 and M5, and the linear resistor is embodied by M2. Transistor M6, connected in parallel to the load capacitor C_L , is required to bias correctly the filter and, in first approximation, its large output resistance does not affect the small-signal behavior of the circuit.



Figure 33. a) Building block diagram and b) schematic of the proposed G_mC filter.

6.1.2 Transconductor analysis

The core of the transconductor is the linear resistor R, which converts the voltage applied by the buffer in a proportional current (Fig. 33a). In our technology, like in almost all large-area electronics, passive linear resistors are not available, hence a transistor has to be used for this purpose. Two possible choices are available: a TFT exploited in its linear region or in saturation. The G_mC filter proposed here targets low-frequency applications, hence a low transconductance and a low cut-off frequency are pursued by selecting the second option, i.e. M2 in saturation. Indeed, since the drain-source resistance of the TFT determines the actual transconductance G_m of the transconductor, the larger drain-source resistance obtained when M2 is used in saturation causes a smaller transconductance and allows, for a given cut-off frequency, a smaller load capacitance. Also, from the linearity point of view, the current with respect to the (drain-source) voltage is more linear in the saturation region than in the triode one.

In order to achieve saturation already for a small drain-source voltage, source and gate of transistor M2 are connected together (as before, this configuration will be referred to with Zero-Vgs connection, i.e. $v_{GS} = 0$ V). This is a viable solution in organic unipolar technologies, since OTFTs are typically normally-on devices, as underlined in Chapter 4. If Zero-Vgs connected, the TFT enters the saturation region when the applied drain-source voltage is larger than the threshold voltage of the transistor. In our p-type double-gate technology, the threshold voltage of the device can be controlled by means of the voltage applied to the top-gate. In fact, making the voltage applied to the top-gate more and more positive shifts the threshold to more negative

values, hence it reduces the channel current, increases the output resistance of the OTFT, and extends the width of the saturation region (Fig. 34). Due to the actual implementation of the linear resistor, its resistance R in Eq. (31) can be replaced with the small-signal output resistance of M2 in saturation, i.e. $r_{0,2}$. Moreover, thanks to the influence of the control voltage V_{bias} on the output resistance the $G_{m,ideal}$ of the transconductor can be effectively tuned.



Figure 34. Simulated output characteristic of a Zero-Vgs connected p-type OTFT for different top-gate bias V_{bias} = -20 V, -15 V, -10 V, -5 V, 0 V.

In a real implementation of the circuit, however, the actual transconductance G_m is smaller than $G_{m,ideal}$. The main reason for this reduction is the actual small-signal mirroring factor which is smaller than 1 even if M3 and M4 have the same W/L ratio, the same voltage bias, and the same current bias. This peculiar behavior can be explained considering at first the simplest current mirror topology shown in Fig. 35. Since transistor M3 is normally-on, connecting together drain and gate always forces a linear regime (and not saturation). Therefore a small-signal applied to the terminal v_{in} causes a current i_{in} made of two contributions: the first one due to the usual gate transconductance, the second due to the drain conductance. In standard technologies the drain conductance depends on the channel length modulation and it is typically negligible, while in our case it depends on the (much larger) triode conductance. This contribution however is not mirrored to the output branch, since the drain of the output transistor is biased at a constant voltage V_{OUT} (i.e. $v_{out} = 0$ V). Under this assumption, the small-signal output current is always smaller than the input one.



Figure 35. Basic p-type-only current mirror schematic.

This circuit can be analyzed using the TFT equations discussed in Chapter 4. For the sake of simplicity, the analysis is made for an n-type current mirror, since the equations derived in Chapter 4 are also written for n-type transistors. Applying a small input signal v_{in} and considering our current model (Eq. (4)), the small-signal input current i_{in} flowing through the sink transistor M3 can be expressed as a function of the gate transconductance ($\delta I_{DS}/\delta V_{GS}$) and the drain conductance ($\delta I_{DS}/\delta V_{DS}$):

$$i_{in} = \frac{\delta I_{DS}}{\delta V_{GS}} v_{gs} + \frac{\delta I_{DS}}{\delta V_{DS}} v_{ds} = \frac{W_3}{L_3} \beta \gamma \left[\left(V_{G,3} - V_{S,3} - V_{FB} \right)^{\gamma - 1} - \left(V_{G,3} - V_{D,3} - V_{FB} \right)^{\gamma - 1} \right] v_{in}$$

$$+ \frac{W_3}{L_3} \beta \gamma \left(V_{G,3} - V_{D,3} - V_{FB} \right)^{\gamma - 1} v_{in}$$
(32)

where $V_{G,X}$, $V_{S,X}$ and $V_{D,X}$ are the DC gate, source and drain voltage of MX (X is 3 or 4), and V_{FB} is the flat-band voltage.

On the other hand, the small-signal output current of the mirror only depends on the voltage variation at the gate of M4, since its drain voltage is assumed to be constant (i.e. $v_{out} = 0 V$), hence it reads:

$$i_{out} = \frac{W_4}{L_4} \beta \gamma \left[\left(V_{G,4} - V_{S,4} - V_{FB} \right)^{\gamma - 1} - \left(V_{G,4} - V_{D,4} - V_{FB} \right)^{\gamma - 1} \right] v_{in}$$
(33)

From the ratio between these two equations, the mirroring factor T can be expressed as:

$$T = \frac{i_{out}}{i_{in}} = \frac{\frac{W_4}{L_4} \beta \gamma \left[\left(V_{G,4} - V_{S,4} - V_{FB} \right)^{\gamma - 1} - \left(V_{G,4} - V_{D,4} - V_{FB} \right)^{\gamma - 1} \right]}{\frac{W_3}{L_3} \beta \gamma \left(V_{G,3} - V_{S,3} - V_{FB} \right)^{\gamma - 1}}.$$
(34)

Considering $V_s = V_{s,3} = V_{s,4}$, $V_G = V_{G,3} = V_{G,4}$ and $V_D = V_{D,4}$, and assuming identical W and L for M3 and M4, Eq. (34) can be then simplified as:

$$T = 1 - \left(\frac{V_G - V_D - V_{FB}}{V_G - V_S - V_{FB}}\right)^{\gamma - 1}.$$
(35)

Equation (35) clearly shows that T is always smaller than 1 even when the voltage bias is the same for the input and the output nodes, i.e. $V_D = V_G$, and the bias currents are identical. Moreover, Eq. (35) holds for both saturation and linear regimes; in fact, in order to derive it no assumption was made on the working region of the two devices.
6.1.3 Transconductor design

From the simplified expression of T, it can also be inferred that a mirroring factor close to unity is obtained when the drain voltage of the output transistor is biased around V_G . For this reason, in the final implementation of the current mirror, the additional transistor M5 (Fig. 33b), with the same dimensions of M2, was included to keep the output TFT in the linear region like M3. The transistor M5, however, acts as source follower with respect to the small-signal variation v_{in} . Therefore, the drain of M4 is not constant anymore and its drain conductance also contributes to the mirrored current. It is easy to derive that the mirroring factor T_{M5} in presence of M5 becomes:

$$T_{M5} = 1 - \frac{1}{1 + g_{m,5}/g_{m,4}} \left(\frac{V_G - V_D - V_{FB}}{V_G - V_S - V_{FB}} \right)^{\gamma - 1}$$
(36)

Indeed, the small-signal variation of the drain of M4 is given by the partition of the input voltage ($v_{5,2}$ in Fig. 36) between the channel resistance of M5 and the channel resistance of M4 (see Appendix for further details).

Besides imposing the right bias to the output device of the mirror and buffering a portion of the input voltage to the output, the transistor M5 also determines the output resistance of the transconductor. It is worth noting however that the presence of M5 does not increase the output resistance as the cascode configuration would suggest. Indeed, since the source degeneration of M5 is weak and the resulting gain of the local negative feedback is low, the output resistance of the transconductor is, at first order approximation, equal to the output resistance of M5.



Figure 36. Unloaded transconductor for intrinsic voltage gain evaluation.

Aware of the parameters that affect the transconductance and the output resistance of the circuit, interesting considerations can be drawn about the small-signal voltage gain of the transconductor. Indeed, when the output is loaded with an ideal current source (a condition that will be referred to as 'unloaded'), the transconductance and the output resistance are determined by the output resistance r_0 of the two OTFTs M2 and M5 respectively. Therefore, with reference to the voltages v_{in} and v_{out} defined in Fig. 36, the unloaded voltage gain reads:

$$G = \frac{v_{out}}{v_{in}} = T_{M5} \frac{r_{05}}{r_{02}}$$
(37)

This equation shows that the gain mainly depends on the channel length modulation affecting the transistors M2 and M5. For this reason, in order to increase the voltage gain, it is possible to change the dimensions of M5 to decrease its channel length modulation with respect to the one of M2. Table III summarizes the results of different simulations where the channel width W and the channel length L of M5 have been scaled up by the same factor S.

and same aspect ratio W/L of the output cascode device						
S	W [μm]	L [μm]	G _m [nA/V]	R_{out} [M Ω]	Gain	
1	1k	5	4.55	228	1.03	
2	2k	10	4.51	491	2.21	
4	4k	20	3.8	927	3.52	
8	8k	40	2.9	1800	5.22	

Table III. Simulated gain for different channel lengths (for constant W/L) for M5 and same aspect ratio W/L of the output cascode device

The values of $R_{out} = v_{out}/i_{out}$, extrapolated from simulation data obtained for different channel lengths, show that increasing the channel length, the output resistance R_{out} raises and so does the gain G. This scaling however does not produce a proportional increase in the gain of a factor S, as it would be expected from Eq. (37); in fact, increasing the channel length of M5 varies its saturation behavior with respect to M2, and larger gate-source and drain-source voltages are needed to compensate for the smaller channel length modulation. For this reason the drain voltage of M4 gets closer to V_{DD}, causing a drop of the mirroring factor T and consequently of the overall transconductance G_m. This drop can also be seen in Eq. (37). Indeed, the drain voltage of the n-type equivalent of M4 will decrease for longer channel lengths of the output device M5, and the numerator of the fraction in Eq. (37) will increase. In the circuit implementation of the transconductor that has been fabricated was chosen S equal to 1.

So far was considered only the dimensioning of the symmetric devices in the input and output branch, i.e. M2 compared to M5 and M3 with respect to M4. However, the dimensions of M2 also need to be carefully optimized accordingly to the dimensions of M3 and M1, in order to avoid excessive voltage drops over these devices. In this case, indeed, the gain and the transconductance remain unchanged, but the DC input range for which the transfer characteristic can be considered linear is reduced.

Figure 37 depicts indeed three possible scenarios for different relative dimensions of the input branch devices. If M2 is much wider than M1 and M3, the voltage drops V_{GS1} and V_{GS3} will be large, decreasing the linearity for high input voltages and drastically reducing the linear input range (Fig. 37, blue line). On the other hand, if M3 is wider than M2 this would result in a waste of area, while a wide M1 would cause non linearities for low input voltages (Fig. 37, green line). Indeed, for low inputs, the source of M1 would saturate to ground due to the positive threshold voltage. Hence the linear part of the characteristic would not start for $v_{IN} = 0$ V, but for $v_{IN} > V_{GS1}(I_{MAX})$. According to these considerations the final design adopts the same dimensions for all the devices of the input branch (Fig. 37, red line).



Figure 37. Voltage drop on the transconductor device as a function of the input voltage for different choices of the transistor dimensions.

In line with these considerations, all the devices in the transconductor are dimensioned with equal channel widths and channel lengths. However, also the transistor threshold plays a role in the performance of the circuit. Hence, in order to keep the electrical matching among the different devices, the bias voltage V_{bias} is applied to all transistors M2, M3, M4 and M5.

6.1.4 Transconductor realization

The proposed transconductor was realized and measured. The layout of the circuit is shown in Fig. 38.



Figure 38. Layout of a tunable transconductor.

6.1 Filter based on a tunable transconductor

According to the discussion in Section 6.1.3, the TFTs in the circuit all have the same dimensions. In order to get a feeling of the real circuit dimensions, the width of the test pads is given. The transconductor occupies an area of about 200 μ m x 400 μ m.

6.1.5 Transconductor measurements and simulations

The circuit was designed to operate at 20 V supply, which is a relatively large value compared to the standard silicon technologies due to the thick dielectric layer. In order to get an insight in the influence of the control voltage, many different measurements have been taken for $V_{\text{bias}} = 0 \text{ V}$, 5 V, 10 V, 15 V, 20 V. In the following plots, the step used for the independent variable was 100 mV for both the measurements and the simulations.



Figure 39. a) Measured (continuous lines) and simulated (dashed lines) output current as a function of the output voltage V_{out} for different values of $V_{blas} = 0 V$, 5 V, 10 V, 15 V, 20 V $(V_{in} = 5 V)$ and b) output resistance estimated from the measured data.

From the measurements of the output current obtained applying a constant voltage $V_{IN} = 5 V$ and sweeping v_{OUT} from ground to V_{DD} (Fig. 39a), the output resistance of the transconductor can be evaluated (Fig. 39b). As it has been shown already in Fig. 34, also in this case the control voltage V_{bias} can be used to modify the current and the output resistance of the transconductor. When the bias gets closer to ground, the output current raises and hence the output resistance drops. The maximum output current that was measured, exploiting a control bias between the rails, ranges from 4.098 μ A for $V_{bias} = 0 V$ to 337 nA for $V_{bias} = 20 V$. The relative variation is about one order of magnitude and the same variation can be seen also in the output resistance.

The transfer characteristic of the transconductor was also measured for the same values of V_{bias} (0 V, 5 V, 10 V, 15 V, 20 V), see Fig. 40a. The input node was swept from ground to V_{DD} while the output node was biased by an ideal voltage source at $V_{OUT} = 5$ V. The resulting transconductance as a function of the input voltage v_{IN} is shown in Fig. 40b. Also in this case the output current increases when the control voltage approaches ground and so does the transconductance of the circuit: for instance, varying the control voltage from ground to V_{DD} , the minimum transconductance $G_{m,min}$ goes from 19 nA/V to 2 nA/V.



Figure 40. a) Measured (continuous line) and simulated (dashed line) output current as a function of the input voltage V_{in} for different values of V_{bias} = 0 V, 5 V, 10 V, 15 V, 20 V (V_{out} = 5 V) and b) transconductance estimated from the measured data.

From Fig. 40 the influence of V_{bias} on the linearity of the circuit can also be evaluated. The higher the control voltage (i.e. lower current), the larger is the linear input range or, with the same input range, a higher linearity is achieved. Although in Fig. 40b the plots are less clean due to the low current and to the derivative operation required to extrapolate the transconductance, it is still possible to evaluate qualitatively the linearity of the transconductor for varying input bias by inspecting the shape of the curve. Indeed for larger V_{bias} (i.e. lower current), the small-signal transconductance G_m increases linearly with the bias point V_{IN} which results in a dominant second-order non-linearity in the v_{in} -i_{out} characteristic. For lower V_{bias} (i.e. higher current), the transconductance G_m increases more than linearly raising the input bias V_{IN} , revealing the higher V_{bias} allows more linear v_{IN} -i_{OUT} characteristic.

V _{bias} [V]	R_{out} [M Ω]	G _m [nA/V]	Gain
0	27	51	1.37
5	44	32	1.4
10	76	18	1.36
15	153	9.5	1.45
20	342	4.7	1.6

Table IV. Measured transconductor parameters for different bias voltages

The set of data in Fig. 39 and 40 (summarized in Table IV for $V_{IN} = 5$ V and $V_{OUT} = 5$ V) also confirms that the unloaded gain of the circuit is almost independent on the bias voltage (and hence on V_T), since it depends on the ratio between the output resistances of the devices M2 and M5. The two devices have here the same W/L ratio and the same channel length hence the voltage gain is about one. The actual gain value is slightly higher than 1 because the output resistance of the circuit is not only due to the output resistance of M5, but also to the output resistance of M4. This contribution could be taken into account in Eq. (37) replacing $r_{0,5}$ with the complete output resistance $g_{m,5}$ $r_{0,5}r_{0,4} + r_{0,5} + r_{0,4}$. Decreasing the output current (i.e. larger V_{bias}), the output resistance of M4 increases constantly, and this effect more than compensates the reduction in transconductance G_m due to the actual transfer factor T_{M5} and to the source follower M1.



Figure 41. Measured (continuous line) and simulated (dashed line) current flowing out of the transconductor with V_{in} connected to V_{out}, as a function of the input voltage V_{in} for different values of V_{bias} = 0 V, 5 V, 10 V, 15 V, 20 V.

Connecting together input and output nodes, a tunable resistor connected to V_{DD} is obtained. The measured current of this configuration is shown in Fig. 41 for different values of the control voltage V_{bias} .

6.1.6 Tunable filter

After analyzing in depth the static performance of the transconductor, the behavior of this circuit can be shown when employed in a G_mC filter, according to the schematic of Fig. 42.



Figure 42. Bode magnitude plot of the tunable transconductor. Varying the control voltage V_{bias} within the supply range, the first pole can be shifted over one decade of frequencies.

The main feature of the proposed transconductor is the possibility of varying the transconductance of the circuit without affecting its unloaded voltage gain. For this reason, a filter can be implemented of which bandwidth is tunable over a decade of frequencies and, accordingly, the frequency response is shifted rigidly (Fig. 42).

6.1 Filter based on a tunable transconductor



Figure 43. Bode magnitude plot of the circuit with Zero-Vgs load (continuous line) and transfer function using an ideal current source instead of transistor M6 (dashed line).

The unity DC gain is retained, because the current source employed in the simulations of Fig. 42 has an infinite output resistance. If the load is implemented with a Zero-Vgs connected TFT (M6 in Fig. 43) to embody the current source, due to its finite output resistance, a reduction of the gain is observed (Fig. 43), while the gain-bandwidth product is preserved.

6.2 Amplifiers

The most frequent build block in analog and mixed-signal design is probably the differential voltage amplifier, often called Operational Amplifier (OpAmp) since it can be used to implement the four arithmetical operations (addition, subtraction, multiplication and division) and many more functions. Indeed, since it provides negative-feedback systems with the needed high gain, this is a key element in integrators, differentiators, peak detectors, comparators, zero-crossing detectors, switched-capacitor circuits, sample and holds, and more.

6.2.1 Continuous-time amplifier

In large-area electronics, due to the many limitations posed by the technology, the design of high gain OpAmps is very cumbersome, and involves large circuit complexity that can be very detrimental for reliability.

On the one hand, due to the low intrinsic gain of TFTs, the use of multiple stages becomes mandatory to achieve high gain. On the other hand, the availability of only p-type TFT causes two main issues: first each stage has a p-type input pair, thus suitable level shifters should be employed to match the input and the output voltage ranges, or AC coupling must be used; second, no self biasing load can be exploited, i.e. n-type current mirrors are not available. Moreover, telescopic solutions do not help, since cascoding can be applied only to the input pair.

The supply budget dedicated to each TFT in a stack is limited, and also with a supply voltage of about 20 V it is difficult to keep all transistors in saturation (remember that normally-on TFTs require much larger drain-source voltage to enter saturation than normally-off TFTs, typically larger than 6-8 V in our technology, see Fig. 34) and linear resistors are not available. For this

reason, even when only three TFTs are stacked between gnd and V_{DD} , like in fully-differential amplifiers exploiting Zero-Vgs active loads (Fig. 45b), the differential gain is very sensitive to input common mode and TFT biasing. Thus, compared to standard silicon technologies, the differential gain can decrease drastically with bias variations due to mismatch and/or common-mode shifts.

The proposed amplifier

Given these considerations, was chosen as continuous time amplifier a basic structure which can only achieve low gain, but ensures relatively fast response and high robustness. Indeed a fully-differential amplifier was chosen that exploits a tail current source, a p-type input pair and active loads (Fig. 44a)



Figure 44. a) Schematic of a single-stage fully-differential amplifier, here b) the gain between differential input and differential output also depends on c) the common mode of the differential input.

The gain of the amplifier is the ratio between differential output v_{out} (which is given by the difference between the positive and the negative outputs, $v_{out,p}$ and $v_{out,n}$ in Fig. 44b) and the differential input v_{in} . Other requirements, like the input and the output common-modes, need to be taken into account. Indeed this circuit works properly if the tail, the input and the load devices all work in saturation; however, the gain can drastically decrease if the input common mode $V_{CM,IN}$ approaches V_{DD} or gnd (Fig. 44c).

Amplifier analysis

The many limitations imposed by the technology restrict the design choices for a voltage amplifier. In our case, since the technology is p-only, the input pair can only be p-type (M2 and M4 in Fig. 45).



Figure 45. Schematics of two fully-differential amplifiers exploiting a) diode or b) Zero-Vgs active load.

The tail current source should also be a p-type TFT and work in saturation, but unfortunately it cannot be the output transistor of a current mirror (as explained in Section 6.1.2). However, it can be easily embodied by a p-type TFT used in a Zero-Vgs configuration (M3 in Fig. 45) to provide high output resistance and thus a relatively supply-independent bias current I_{tail} .

Neither passive loads nor self biasing solutions are possible, due to the lack of resistors and complementary devices. Therefore the output loads can only be implemented with diode-connected or Zero-Vgs TFTs (M1 and M5 in Fig. 45a and Fig. 45b respectively). The first solution, although very fast, limits the gain to about 2 and keeps the output common mode very close to ground, making almost impossible the use of additional level shifters. In the second case, the speed worsens, but higher gain can be achieved (up to 40dB with some design effort and the output common mode voltage can be designed to be closer to half the supply. For these reasons, Zero-Vgs loads have been exploited.

A third solution was also proposed in literature: the AC-coupled configuration [71]. However, this requires a considerable increase in circuit complexity and the gain improvement is, in our opinion, not so substantial to justify the additional potential yield loss.

Amplifier design and simulation

The first step in the design of the amplifier shown in Fig. 45b is the choice of proper current bias, i.e. the dimensioning of the tail device M3 with respect to the load TFTs, M1 and M5. As starting point, the current variation due to channel length modulation effects can be neglected, and the DC current in the amplifier can be considered independent of the drain-source voltage drop on the loads and on the tail. Since the three devices work in a Zero-Vgs configuration, the tail M3 should provide twice the current provided by M1 and M5. For this reason, the aspect ratio of M3 is chosen $W_3/L_3 = 2 W_{1.5}/L_{1.5}$. If the input common-mode approaches ground, and both the input transistors are strongly on, the output common mode will approach $V_{DD}/2$.

When the input common-mode approaches V_{DD} , the tail current drastically decreases since the drain-source voltage gets close to zero, i.e. $V_{D,3}$ close to V_{DD} (Fig. 46a). However, the DC

current will never completely switch off, since the source voltage of the input devices can be even lower than the input common-mode (i.e. $V_{SD,3} > 0 V$ even if $V_{CM,IN} = V_{DD}$) and the drain voltage of M3 ($V_{D,3}$) never reaches V_{DD} .



Figure 46. a) Bias values of the drain of M3 $(V_{D,3})$, of the input voltage $(V_{CM,IN})$ and of the output voltage $(V_{CM,OUT})$. b) Differential gain as a function of the input common-mode for different dimensioning of the input TFT width.

The variation of the bias current due to a different input common-mode affects also the output common-mode and the gain of the amplifier. As shown in Fig. 46a, when the input common-mode $V_{CM,IN}$ is low, both the drain of M3 and the outputs are around $V_{DD}/2$, as expected. When the input common-mode $V_{CM,IN}$ becomes larger than half the supply, $V_{D,3}$ follows the inputs and the output common-mode drops, together with the DC current.

From Fig. 46b, the consequences on the gain can be observed. For a low input commonmode, the input transistors work in the linear region ($V_{DS} \sim 0 V$ and $V_{GS} >> 0 V$) and the output resistance of the amplifier drops. On the other hand, when $V_{CM,IN}$ is too high, the bias current drops, the load transistors M1 and M5 exit the saturation region, and provide a low output resistance. In both cases, a detrimental effect on the gain is obtained.

Varying the dimension of the input devices causes a different overdrive voltage on the input TFTs (Fig. 46b), and hence it shifts the gain plateau to the right for larger widths. Increasing the width of the input devices also increases the gain due to the larger transconductance g_m . Unfortunately, the difference between input and output common-mode increases too, making the design of level shifters for multi-stage DC coupled amplifiers more complicate. Since lowering the width of the input devices also lowers the differential gain (which is already small), the final differential amplifier was designed with input device as wide as the load ones.

None of these considerations are affected by the presence of the second gate. However, some interesting observations can be made for double-gate technologies. Connecting together gate and top-gate of M2 and M4 increases the input transconductance by a factor $1+\eta$ (in line with Eq. (10), while, concerning the devices used in a Zero-Vgs configuration (M1, M3 and M5), the top-gates should be connected to their own source terminal, in order to prevent detrimental effects on the output resistance due to the threshold voltage variation.

The top-gate voltage could also be used for more sophisticated purposes. For instance, the tail top-gate could be used within a common-mode feedback network to control the output common-mode, and the load top-gates could be used e.g. to zero the offset of the amplifier due to mismatch between M2 and M4, and between M1 and M5.

Amplifier realization

Figure 47 shows respectively the layout and the photograph of the realized circuit. Both the input TFTs and the output loads have been dimensioned with the same W/L ratio and with the same channel length. Therefore, also the number of sub-channels was chosen the same.



Figure 47. Layout and photograph of the fully-differential amplifier.

Moreover, the tail source should provide exactly the same current provided by the two load transistors. In order to avoid systematic errors that could worsen the performance of the circuit in addition to process variations, the tail transistor was not implemented with a single device exploiting a double width and a different number of sub-channels, but with two devices identical to the loads.

In the final layout, also two output buffers were included. These are required to perform transient measurements without affecting the circuits with external capacitive or resistive parasitics due to the measurement setup.



Figure 48. a) Measurement of the differential output and b) maximum gain as a function of the positive input voltage. The negative input was biased at 12 V.

Measurements

The tapeout includes several instances of the proposed continuous-time amplifier, and in Fig. 48 the differential output and gain measured on 14 of them are shown.

For these measurements, the positive input was swept from ground to V_{DD} , while the negative input was kept constant at 12 V. In this way, the differential output was measured and the maximum random offset could be estimated to be about 0.8 V. From these measurements also the maximum differential gain could be evaluated. Indeed, when the positive input reaches 12 V, the input common-mode is also 12 V and, according to the simulations, the maximum gain is achieved. However, the measured gain was much smaller than the simulated one, probably due to the degradation of the semiconductor mobility, and consequently to the reduced input transconductance, after a few weeks shelf-life time. Also its variability is not negligible, showing once more that, even after a careful design process, variations and aging strongly impact analog circuit performance.

6.2.2 Discrete-time amplifier

The performance of continuous-time amplifier suffers from various limitations: low gain, small input range, low speed, low linearity, large mismatch, to mention the most relevant. Many of these drawbacks can be partially solved with a considerable increase in the circuit complexity [35], which can impact negatively the yield. Moreover, in our interface, in order to preserve the SNDR achieved by the filter, the amplification should respect constraints on linearity and noise. To achieve these goals, a discrete-time solution has also been investigated.

In feedback-based systems, discrete-time amplification can potentially allow better linearity than continuous-time amplification, as it uses only capacitors as passive devices. Capacitors, contrary to linear resistors, are available in basically any TFT technology on foil, as they can be formed between the two interconnection layers. Unfortunately, the poor performance of large-area technology TFTs makes also the design of discrete-time circuits difficult. High-quality switches cannot be embodied by normally-on transistor without large voltages to switch them off (low off-resistance) and the on-resistance is typically large (causing voltage drops and slow response). Moreover, the most known structures to cancel charge injection, to reduce offsets and leakages, all exploit negative feedback configurations, which are almost impossible to realize as discussed before. For these reasons, a new device was designed to minimize the number of switches required for the sampling, to amplify the signal and to enable faster response.

The proposed amplifier

In order to perform fast analog amplification a discrete-time parametric amplifier was designed. The amplifier works in two phases (Fig. 49). During the first phase the input signal is connected to a parametric capacitor (PC) and the output voltage $v_{out,\phi1}$ follows the input v_{in} .

At the beginning of the second phase, the switch opens and the charge accumulated on the capacitance C_{b1} is fixed:

$$Q = C_{\varphi_1} \cdot v_{in,\varphi_1}.$$

(38)



Figure 49. Discrete-time amplification exploiting a parametric capacitor.

where the value $v_{in,\varphi1}$ is the last input voltage before the switch is opened. The second phase also triggers the variation of the capacitance value of the parametric capacitor. For this reason, the charge accumulated in the capacitor in the second phase can be expressed as:

$$Q = C_{\varphi 2} \cdot v_{out,\varphi 2}. \tag{39}$$

Imposing charge conservation the gain of the circuit results:

$$G = \frac{v_{out,\varphi_2}}{v_{out,\varphi_1}} = \frac{C_{\varphi_1}}{C_{\varphi_2}}.$$
(40)

Since the two values of the parametric capacitor are independent of the applied voltage, the gain is always signal independent providing intrinsic linearity. Moreover, compared to switched-capacitor discrete-time solutions, the parametric amplifier requires fewer devices (no OpAmps are needed) and needs no charge transfer in the gain phase, with an inherent benefit with respect to robustness and speed.

A proposed parametric capacitor

In order to implement the parametric capacitor, a new device was designed specifically oriented to three-metal-layer technologies. The capacitance value C can be expressed as function of its geometric parameters using the well-know parallel plates formula:

$$C = \varepsilon_0 \varepsilon_r \frac{WL}{h} \tag{41}$$

where ε_0 and ε_r are the electric and the dielectric constant respectively, W and L are the width and the length of the two facing plates, and h is their distance. In a double-gate technology, normal capacitors can be realized between gate and source layers, between gate and top-gate layers, and between the source and top-gate layers. Each couple of layers is characterized by a different value of the parameter h.



Figure 50. Vertical section of the parametric capacitor (PC). The actual width of the second conductive layer depends on the accumulation status in the semiconductor (green layer) and varies from the source finger width (FW) to the gate width (W_G).

Combining in a single device the three types of capacitor, a novel parametric capacitor can be designed. Its cross-section is shown in Fig. 50. In this device the dimensions of top-gate and gate plates are defined by the geometry of the metal armatures; the middle plate, on the other hand, has a parametric width. In our application, a synchronous signal will be applied to the device in order to accumulate or to deplete the semiconductor. These two states correspond to different dimensions to the central plate, hence the three capacitors can be switched from their minimum to their maximum capacitance value and vice versa. This variation will be used afterwards to amplify the sampled signal.



Figure 51. V_{TG} - V_G plane with charge accumulation regions defined by Eq. (42).

For our purpose, the top-gate voltage was used to control the accumulation state in the semiconductor underneath. Combining Eq. (10) and the channel accumulation condition $V_{OD} >> 0 V$ (Eq. (9)), two different regions can be found, in the V_{TG} - V_G plane (Fig. 51): on the right hand side of the straight line

$$V_{TG} = -\frac{V_G}{\eta} + \frac{V_{FB}}{\eta} \tag{42}$$

the semiconductor is accumulated, while on the left hand side it is depleted.

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The new device can be modeled (Fig. 52) with three variable capacitors connecting all plate pairs formed by the three metal layers: a top-gate to source (C_{TGS}), a top-gate to gate (C_{TGG}) and a source to gate (C_{SG}) capacitor.



Figure 52. a) Equivalent model of the parametric capacitor. Three variable capacitors connect top-gate to source (C_{TGS}), top-gate to gate (C_{TGG}) and source to gate (C_{SG}). An increase of C_{TGS} and C_{SG} is associated with a decrease of the capacitance C_{TGG} . b) Symbol of the parametric capacitor.

Based on geometrical considerations it is possible to define for each capacitor the value of its capacitance when the semiconductor is accumulated and when it is depleted. In the case of a depleted channel we have:

$$\begin{cases} C_{TGS} = FW \ L_G \ \eta \ C_{ox} \\ C_{TGG} = (W_G - FW) \ L_G \ \frac{\eta}{\eta + 1} \ C_{ox} \\ C_{SG} = FW \ L_G \ C_{ox} \end{cases}$$
(43)

On the other hand, for an accumulated channel, we find:

$$\begin{cases} C_{TGS} = W_G L_G \eta C_{ox} \\ C_{TGG} = 0 \\ C_{SG} = W_G L_G C_{ox} \end{cases}$$
(44)

In the previous equations, W_G is the width of gate (G), top-gate (TG) and semiconductor (OSC) layers, FW is the width of the source metal strip (Fig. 52) and L_G is the length of the device (in the plane perpendicular to the picture of Fig. 52). The PC design of Fig. 50 does not take into account the variations due to the lithographic process and to mask misalignments. However, these problems can be easily overcome slightly changing the design of the device accordingly to the specific use. For instance, in our case, the top-gate was used to control the charge accumulation in the semiconductor (and thus the width of the central plate). Therefore a pyramidal layout can be used, designing $W_G = W_{OSC} + E_{OSC}$ and $W_{OSC} = W_{TG} + E_{TG}$, where W_X is the width of the layer X (G, TG or OSC) and E is the minimum enclosure imposed by the design rules. Following this approach, the plate width W_G in Eq. (43) and (44) has to be replaced by W_{TG} , but the ratio between the capacitance values in the two different phases remains the same, and the following discussion remains valid.

Each pair of voltages $V_{G}-V_{TG}$ determines a capacitance value for each of the capacitors in the schematic of Fig. 52a. These values are plotted in a three dimensional space in Fig. 53 ($W_G = 50 \ \mu m$, $L_G = 50 \ \mu m$, FW = 5 μm , $C_{ox} = 9.5e^{-17} \ F/\mu m^2$), on the left hand side. This picture shows that far enough from the roll off, the value of the capacitance is almost independent of the voltage applied to the plates. The right hand side of the same figure shows the value of each capacitor as a function of only one voltage, while the others are biased at 0 V. The more gradual transition as a function of V_{TG} reflects the weaker coupling due to the higher distance of the top-gate from the semiconductor.

A behavioral model of the PC has been implemented in Verilog-A to enable analog simulation. As well as for the TFT models, the implemented PC instance can parse the width and length of the device from the circuit schematic. In the model, this information is used to tune the capacitor values (C_{TGS} , C_{TGG} , C_{SG}) as a function of the voltage applied to the device.



Figure 53.Capacitance values for CSG, CTGG and CTGS: on the left as a function of both gate and top-gate voltages, on the right separately as a function of the gate voltage for $V_{TG} = 0 V$ (top panels), and as a function of the top-gate voltage for $V_G = 0 V$ (bottom panels).

Parametric amplifier analysis

Based on the former considerations, the PC device can be used to design a discrete-time parametric amplifier. The circuit does not involve active elements and thus does not introduce additional noise, apart from the thermal noise due to the switches involved in the sampling of the analog signal. Moreover, the gain is insensitive to the absolute value of the parametric capacitance, which can be designed to address other requirements like speed ($\tau = C_{PC}R_{switch}$) or noise level (kT/C_{PC}).

The charge accumulated in the first phase does not need to be transferred to a different capacitor, thus it does not require additional settling time for transport. On the other hand, some time is required to commute the semiconductor state. However, the semiconductor works in accumulation and not in inversion, hence the charge carriers do not need to be borrowed by the contacts as in standard silicon technologies, but just need to be collected at the semiconductor-dielectric interface. For this reason, it is possible to create gain without detrimental effects on speed.



Figure 54. Schematic of the discrete-time amplifier exploiting a differential parametric capacitor amplifier and a continuous-time differential amplifier.

An important point has to be considered: the switching activity of the top-gate metal layer of the new device causes important charge injections on the other plates. The use of two parametric capacitors in a differential amplifier configuration is thus needed to cancel out the spikes due to the charge injection, as the disturbance appears then as a common mode for the differential amplifier that follows them. In the embodiment of Fig. 54, a continuous-time differential signal at the output of the parametric capacitor amplifier and drive the following stages of signal conditioning chain, or to provide a suitably large input directly to the analog to digital converter.

In the differential parametric capacitor amplifier DPCA (Fig. 54), during the first phase the switches S1 connect the differential input $V_{diff_{in}} = V_{in+} - V_{in-}$ to the two PCs. For one of them V_{in+} is connected to the gate and V_{in-} to the source, while for the second PC the gate is connected to V_{in-}

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and the source to V_{in+}. After the capacitors are charged, the switches S1 are disconnected and the value of the capacitance can be changed varying the control voltage applied to the top-gate. The differential voltage $V_c = V_{c+} - V_{c-}$ is immune from the injection due to the switching control voltage and can be further amplified by the following continuous-time differential amplifier.

Before evaluating the gain provided by the differential PC amplifier, it is important to discuss the missing switch between the differential input and the source terminal of the PCs. Indeed this configuration allows, in the second phase, a direct path from the time variant input to the amplified sampled output. However, the small-signal input applied to the source plate affects the gate plate voltage divided by a capacitive partition (between C_{SG} and C_{TGG} , see Fig. 52a) and it is not amplified by the PC; for this reason, its contribution to the differential output should be negligible with respect to the sampled value. If it is not the case, an additional switch exploiting the same function of S1 can be also included, though the new switch would require a different synchronization from S1 and the control signal. In fact, if the switches were opened together, all devices would be floating and all potentials would shift with an equal amount of the control voltage, leaving the state of the semiconductor unchanged. For this reason, the second switch would require a delayed trigger providing enough skew to let the semiconductor commute its state.

Considering the low quality of the TFTs on foil as switch, the reliability issues for complex circuits, and the small accuracy of data converters (that will be discussed in more detail in next chapter), the influence of the direct path of the input to the output was evaluated a second order effect and a solution without additional switches was preferred. Based on this choice, the gain of the differential PC amplifier can be calculated evaluating the output voltage V_c in the second phase applying charge conservation at the output node of the variable capacitors, i.e. the gate plate. Naming V_{low} and V_{high} the two possible levels of the control voltage applied to the top-gate plate, and referring to Fig. 52a and 54 for the capacitance names and for the voltages in the discrete-time amplifier, first the behavior of V_{C+} can be evaluated between the two phases. The charge on the gate plate of the device connected to the positive terminal of the continuous-time amplifier reads:

$$Q_1 = (V_{in+} - V_{low})C_{TGG,\varphi_1} + (V_{in+} - V_{in-})C_{SG,\varphi_1}$$
(45)

$$Q_2 = (V_{C+} - V_{high})C_{TGG,\varphi_2} + (V_{C+} - V_{in-})C_{SG,\varphi_2}$$
(46)

Imposing the charge conservation, i.e. $Q_1 = Q_2$, V_{C+} can be expressed as:

$$V_{C+} = V_{in+} \left(\frac{C_{TGG,\varphi_1} + C_{SG,\varphi_1}}{C_{TGG,\varphi_2} + C_{SG,\varphi_2}} \right) - V_{in-} \left(\frac{C_{SG,\varphi_1} - C_{SG,\varphi_2}}{C_{TGG,\varphi_2} + C_{SG,\varphi_2}} \right) + \frac{V_{high}C_{TGG,\varphi_2} - V_{low}C_{TGG,\varphi_1}}{C_{TGG,\varphi_2} + C_{SG,\varphi_2}}$$
(47)

The first two terms on the right hand side of this expression represent the effect of the differential input, while the last one gives the common-mode contribution due to the switching activity at the top-gate plate.

At the negative input of the continuous time amplifier, the same process takes place, but the inputs are inverted. Therefore:

$$V_{C-} = V_{in-} \left(\frac{C_{TGG,\varphi_1} + C_{SG,\varphi_1}}{C_{TGG,\varphi_2} + C_{SG,\varphi_2}} \right) - V_{in+} \left(\frac{C_{SG,\varphi_1} - C_{SG,\varphi_2}}{C_{TGG,\varphi_2} + C_{SG,\varphi_2}} \right) + \frac{V_{high}C_{TGG,\varphi_2} - V_{low}C_{TGG,\varphi_1}}{C_{TGG,\varphi_2} + C_{SG,\varphi_2}}$$
(48)

The amplified signal $V_c = V_{c+} - V_{c-}$ as a function of the differential input V_{in} can thus be written as:

$$V_{C} = V_{in} \left(\frac{C_{TGG,\varphi_{1}} + C_{SG,\varphi_{1}}}{C_{TGG,\varphi_{2}} + C_{SG,\varphi_{2}}} + \frac{C_{SG,\varphi_{1}} - C_{SG,\varphi_{2}}}{C_{TGG,\varphi_{2}} + C_{SG,\varphi_{2}}} \right)$$
(49)

The differential gain of the differential parametric capacitor amplifier G_{DPCA} results:

$$G_{DPCA} = \frac{c_{TGG,\varphi_1} + 2C_{SG,\varphi_1} - C_{SG,\varphi_2}}{c_{TGG,\varphi_2} + c_{SG,\varphi_2}}.$$
(50)

The subscript '1' indicates the value of the capacitance in the sampling phase, which takes place with accumulated semiconductor (Eq. (43)), and the subscript '2' indicates the value of the capacitance in the second phase, when the semiconductor is depleted (Eq. (44)).

Amplifier design and simulation

The expression of the discrete-time gain G_{DPCA} can be rewritten, remembering Eq. (43) and Eq. (44), as a function of the geometry of the device:

$$G_{DPCA} = \frac{\frac{2W_G}{FW}}{\frac{W_G}{FW} + \frac{1}{\eta}} \frac{\eta + 1}{\eta}$$
(51)

This equation analytically shows that the gain is independent of the absolute value of the capacitance; indeed, the length of the device L_G is cancelled out in the ratio between numerator and denominator. In our technology, the coupling of the top-gate is $\eta = 0.25$, which leads, if $W_G >>$ FW, to a maximum theoretical gain equal to

$$G_{DPCA,max} = 2 \, \frac{\eta + 1}{\eta} = 10$$
 (52)



Figure 55. Transient simulation of the proposed parametric capacitor-based frontend compared to one exploiting a normal S&H when a 10 mV differential input is applied. The output signals of the two frontends (blue lines) refer to the y-axis on the left, while the control signal and the clock (black lines) refer to the y-axis on the right.

The gain of the DPCA increases proportionally the gain of the continuous-time differential amplifier (Fig. 54) without any detrimental effect on its speed. Indeed, the bandwidth of the parametric capacitor is much higher than any normal continuous-time differential amplifier topology known in this technology. The increased gain and preserved speed are confirmed in Fig. 55, where two simulated transients are shown. The continuous line corresponds to the system exploiting the differential parametric capacitor amplifier together with the continuous-time differential amplifier, while the dashed line is obtained using a just normal capacitor instead of the parametric capacitor. The differential input was set to 10 mV and the simulated gain of the continuous-time differential amplifier $G_{DiffAmpl}$ is about 11. The shape of the step response is the same in both cases, but the amplitude of the output signal is almost ten times larger using the differential parametric capacitor amplifier, as one would expect from Eq. (52).

6.3 Conclusions

In this chapter, some building blocks suitable for analog signal conditioning have been presented. The proposed use of these blocks, in an actual interface for smart sensor applications, exploits an analog filter first and a discrete-time amplifier afterwards. In this way, the linearity requirements on the filter are relaxed, while the amplifier also implements sampling functionality useful for the following analog to digital converter without suffering from aliasing.

The proposed low-pass filter is a G_mC filter, where an innovative transconductor design has been proposed. In order to cope with the considerable variability affecting TFTs manufactured at low temperature, the double-gate feature of our technology was used to provide the circuit with tenability and increase robustness. The transconductance and output resistance tunability was measured to be larger than one order of magnitude. This flexibility can also be used, in more uniform processes, to realize filters with electrically controlled bandwidth. Moreover, the unloaded gain of the circuit is independent of the transconductance, since the output resistance scales accordingly. The tuning effect is thus a rigid shift of the characteristic along the frequency axis.

The filtered signal needs to be amplified to achieve a full scale range compatible with the input range of the analog-to-digital converter. Unfortunately, linear amplifiers are difficult to implement in large-area technologies exploiting unipolar TFTs, and a continuous-time amplifier can only reach a gain of a few tens with a very small common-mode input range. To overcome the performance limits of TFTs, a discrete-time parametric amplifier was also proposed. This amplifier exploits a new parametric capacitor, which was designed specifically for our technology, but can be applied to any three-metal-layer thin-film process. The parametric amplifier has intrinsic linearity and allows for a larger input common-mode since the amplification is independent of the DC input and output voltages. Also with respect to process variations, the proposed device should perform better than conventional differential amplifiers, since the amplification only depends on the thickness of the insulator layers and not on masks alignment or lateral dimensions, neither on device parameters like semiconductor mobility and threshold voltage.

7 Circuit design for data conversion

After the physical signal is converted to the electric domain, filtered and amplified, it must be quantized and converted into a digital word. The analog to digital conversion can be performed following many different approaches; the chosen one should take into account various aspects, like application specifications and signal properties. In our case, the main constraints come from the technology of TFTs on foil. In this chapter, circuit implementation for some building blocks commonly used for data conversion according to the scheme of Figure 26 will be proposed: first a synchronous comparator and then a current-steering digital- to-analog converter. In the last part of this chapter, a complete integrating analog-to-digital converter is analyzed, designed and characterized. Parts of this chapter have been published in [32], [33], [34].

7.1 A synchronous latched comparator

Comparators are among the most common and most critical building blocks in ADC architectures (Fig. 26). Indeed, in a careful converter design, they play a significant role in determining the noise level, conversion speed and, depending on the architecture, linearity of the ADC. A very explanatory example is the basic flash architecture, which requires just one clock cycle to convert the analog signal in a thermometric digital word, and whose accuracy and linearity is limited by the input noise and the offset statistics of the 2ⁿ-1 comparators (and by the statistical variation of the reference voltages).

7.1.1 Comparator topology and analysis

A common solution [87] to implement a fast comparator, able to resolve small differential input signals and achieve logic output levels, is shown in Fig. 56.



Figure 56. Comparator exploiting a preamplifier with output offset cancellation and synchronous latch for logic levels generation.

The logic levels are regenerated by the latch that, exploiting a positive feedback, forces the two outputs to saturate to different supply rails, according to the differential input. When designing a comparator for high speed, latches must have small input devices to reduce parasitic capacitance, but, for this reason, their input offset (i.e. the input voltage required to compensate for all causes of mismatch and obtain zero output voltage) is typically large (in IC silicon technologies the mismatch between the input devices, which typically is the dominant cause of offset, has a standard variation inversely proportional to the square root of the channel area [88]). In order to improve the accuracy of the comparator, a preamplifier (Fig. 56) can be employed to reduce the input equivalent offset due to the latch with a factor equal to the gain of the preamplifier G_{preampl}. The amplifier can be optimized for speed too, i.e. choosing low gain (below 10) and high bandwidth, since its offset can be easily cancelled out after sampling it at the preamplifier output, on the capacitances C2 in Fig. 56, using the scheme that is typically called output offset cancellation.

Following this approach, the continuous-time fully differential amplifier shown in the previous chapter could be used, while the design of a synchronous latch taking advantage of the double-gate technology is shown in the rest of this section.

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Figure 57. Cross-coupled latch topology: a) schematic and b) transistor level implementation in our double-gate technology.

A basic way to implement a latch is to connect two transconductors G_m in a positive-feedback configuration (Fig. 57a). In our technology, a transconductor can be implemented employing a Zero-Vgs connected TFT as active load and a common source TFT as a driver. Figure 57b shows the transistor level implementation of the cross-coupled G_m , where the gate and the top-gate terminals of the driver are connected together to improve the transconductance by a factor 1+ η , according to Eq. (10) [29]. In this implementation, the transconductance G_m in Fig. 57a is equal to the transconductance g_m of the drivers D1 and D2 in Fig. 57b. The resistance R in Fig. 57a represents the output resistance of the Zero-Vgs loads L1 and L2 in parallel with the output resistance loading at the output nodes V_x and V_y .

These three parameters (G_m , R and C) define the time behavior of the circuit, which can be evaluated solving the differential equations at nodes V_x and V_y . Indeed, when a small imbalance ΔV_0 is applied between the output nodes x and y, the positive feedback regenerates the imbalance, eventually bringing the outputs to the opposite rails. In order to derive analytically the trend of the initial imbalance, first the behavior of V_x and V_y mast be written as

$$V_x = -\frac{c}{G_m} \frac{\delta V_y}{\delta t} - \frac{V_y}{G_m R},\tag{53}$$

$$V_y = -\frac{c}{G_m} \frac{\delta V_x}{\delta t} - \frac{V_x}{G_m R}.$$
(54)

Subtracting Eq. (54) from Eq. (53), a differential equation in $\Delta V = V_x - V_y$ is obtained:

$$\Delta V = \frac{c}{G_m} \frac{\delta \Delta V}{\delta t} + \frac{\Delta V}{G_m R}.$$
(55)

Then, the transient behavior of ΔV can be written as:

$$\Delta V = \Delta V_0 e^{t/\tau},\tag{56}$$

where the time constant τ is expressed as:

$$\tau = \frac{RC}{G_m R - 1}.$$
(57)

In order to take real advantage of the positive feedback the gain G_mR of the single transconductor needs to be much larger than 1. Under this assumption, Eq. (57) can be simplified as:

$$\tau \sim \frac{c}{G_m}.$$
(58)

This formulation of the time constant associated to the circuit highlights that the speed achieved by this circuit is only limited by the technology. Indeed, it depends on technology features like the parasitic capacitance of the transistors and on their transconductance, which is proportional to the semiconductor mobility.

The time t_f for the output to reach a certain differential voltage ΔV_f , however, does not only depend on the time constant τ , but also on the value of the initial imbalance ΔV_0 , and can be calculated from Eq. (56):

$$t_f = \tau \log \frac{\Delta V_f}{\Delta V_0}.$$
(59)

The variation of the comparison time Δt_f due to the variation of the initial unbalance ΔV_0 will be referred to in the following as time-walk. The comparison is slower when a small differential input is fed to the circuit, and faster when the differential input is larger.

7.1.2 Proposed latched comparator

In a synchronous implementation of the latched comparator, the cross-coupled inverter latch requires an additional transistor MC, connected to the clock reference CLK, to synchronize the comparison, and two capacitors C_{dec} to provide the first imbalance and allow the output nodes to diverge Fig. 58.



Figure 58. Schematic of the cross-coupled inverter based latch.

Unfortunately, the Zero-Vgs load charges the output with a large parasitic capacitance C_p (due to its gate and top-gate); in fact, in order to reach correct output logic levels, the load must be designed with a W/L much wider than that of the driver (in this case a factor 12.5 provides good results in simulation). The large parasitic capacitance on the output nodes is a major drawback of the topology shown in Fig. 58. The capacitors C_{dec} indeed isolate the output nodes from the input source and apply the input differential voltage to the latch. The input signal is thus divided between the total output capacitance of the latch (shown in Fig. 58 with $C_p \sim 2.6 \text{pF}$) and the decoupling capacitance C_{dec} , reducing the initial imbalance ΔV_0 . In order to avoid a significant loss of signal, the decoupling capacitances have to be much larger than C_p . If the $C_{dec} = DC_p$, the input imbalance becomes about ΔV_0 (1-1/D) and the actual time constant τ' of the circuit can be expressed as:

$$\tau' \sim D\tau = \frac{C_p + C_{dec}}{C_p} \frac{C_p}{G_m}.$$
(60)

This equation shows that if a voltage division of a factor (1-1/D) can be allowed at the input, an increase of the time constant time by a factor D have to be accepted. Another issue related to this topology is that the input signal has to be applied almost together with the active clock transition to avoid the discharge of C_p through the Zero-Vgs load transistors, which are always slightly on.



Figure 59. Schematic of the input-decoupled latch.

To solve this problem, advantage can be taken of the double-gate feature of our technology and design a new latch where inputs and outputs are decoupled without the need for explicit capacitors. As depicted in Fig. 59, in this solution the input is applied directly to the driver of the inverters through the top gates of M5 and M6. This avoids the use of the large decoupling capacitances C_{dec} and brings a considerable gain in area, yield and speed.

In the circuit of Fig. 58, the input capacitance was large due to the parasitics at the gate and at the top-gate of the wide load transistor. In the circuit of Fig. 59, where the signal is fed to the top-gate of the much smaller driver device, the input capacitance of the circuit is strongly

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reduced. Thanks to this solution, the input capacitance can be made about two orders of magnitude smaller, and also the circuitry driving the comparator will need to source a correspondingly lower current. Furthermore the differential voltage applied to the top-gate of the input pair M5-M6 creates an imbalance in the threshold voltage on a fully isolated node, thus this comparator does not required a synchronous input, but can perfectly work also with quasi-static input signals.

The drawback of the configuration in Fig. 59 is that it reduces the transconductance of the input devices. Therefore, the positive feedback becomes weaker and the settling time is increased, since the transconductance in Eq. (58) is lower. Moreover the output logic level "high" of the comparator becomes dependent on the input common mode and worsens due to the weaker pull up. This can result in the need for an additional stage to regenerate full-swing digital levels.



Figure 60. Schematic of the synchronous rail-to-rail latch.

The two topologies shown so far present both some interesting features, such as high gain and good output logic levels in the cross-coupled inverters (Fig. 58), and high speed and low input capacitance in the input-decoupled one (Fig. 59). However, the first is slow and the second less robust.

By merging the two previous topologies, the final latched comparator shown in Fig. 60 achieves higher global performance. In fact, it adopts both a driver pair with gate connected to the top-gate (M1-M2) and top-gate input transistors M5-M6. By means of this merging, the latched comparator guarantees enough gain to reach a full swing of the outputs still without compromising the speed of the response.

7.1.3 Latch design and simulation

In order to prove the actual speed improvement of the proposed latch (Fig. 60) with respect to the basic implementation (Fig. 58), the transient simulations of both circuits are shown in Fig. 61.





When the clock signal commutes from V_{DD} to ground, the two output signals grow and the positive feedback starts splitting the outputs accordingly to the first imbalance. The proposed latch (Fig. 60) reaches the same logic levels as the basic one (Fig. 58), providing robust propagation of the comparison result, and it can complete both comparison and output reset in less than 5 ms (Fig. 61a), compared to about 35 ms (Fig. 61b) required by the basic latch topology. This difference is mainly due to the presence, in the basic latch (Fig. 58), of the decoupling capacitances which allow the output nodes to regenerate logic levels independently from the constant differential input. In the new topology, since the signal is fed through the top-gates of M5 and M6, the decoupling capacitors are not required. Thus, the response is about ten times faster even if the ratio between drivers (M1, M2, M5 and M6) and loads (M3 and M4) is the same. Indeed, for the proposed comparators, the loads have the same dimensions as for the basic one, i.e. $W_{3,4}/L_{3,4} = 2,000 \,\mu\text{m}/20 \,\mu\text{m}$, while in the former case $W_{1,2,5,6}/L_{1,2,5,6} = 40 \ \mu\text{m/5} \ \mu\text{m}$ and in the latter $W_{1,2}/L_{1,2} = 80 \ \mu\text{m/5} \ \mu\text{m}$. In other words, in the proposed latch, the original input device is split in two parts, one to generate the positive feedback gain and the other to read the input. Also the reset phase is very important, because a residual voltage on one of the outputs would reflect in signal dependent memory effects. The

simulation in Fig. 61 was launched for different initial imbalances ($\Delta V_0 = 1 \mu V$, 10 μV , 100 μV , 1 mV), and the consequent time-walk (Eq. (59)) can be estimated.

Figure 61a shows, with continuous lines, the simulated time evolution of the differential output voltage of the latch (after the buffers) for a constant common mode V_{cm} =18 V and varying the differential input ΔV_0 . The comparison starts when the clock signal switches from high to low, and, in line with Eq. (59), a time-walk as a function of the differential input ΔV_0 is observed. Fitting Eq. (59) to the simulation results, a time constant τ = 210 µs is obtained, while the delay to reach 50% of the output for ΔV_0 = 100 mV is 1.6 ms.

Measuring a circuit that bases its performance on the large output resistance and the small parasitic capacitance is a delicate task. Indeed, a measurement setup for dynamic characterization typically loads the measurement pad with a relatively low resistance (1 M Ω) and large capacitance (up to 100 pF, due to the long interconnects). For this reason, an inverter and a custom designed buffer [89] were integrated after each output. Even using these circuits the effect of the measurement setup is not negligible and was also inserted in the simulation after the circuit realization to estimate the quality of the dynamic model.

The simulation results in presence of the output buffer and measurement load are shown in Fig. 62a, in the lower plot.



Figure 62. Simulated time-walk (Δt_f) a) due to varying differential input ($\Delta V_0 = 10 \ \mu V$, 100 μV , 1 mV, 10 mV, 100 mV) and same input common mode ($V_{CM} = 18 \ V$), and b) due to varying input common mode ($V_{CM} = 0 \ V$, 5 V, 10 V, 15 V, 20 V) and same differential input ($\Delta V_0 = 10 \ mV$). Dashed lines represent the synchronization signal.

7.1 A synchronous latched comparator

An important feature of the proposed latch is the broad common mode input range allowed. Indeed the input common mode influences two (G_m and R) out of three parameters (see Eq. (57)) determining the comparison time and, in some circumstances, it can also prevent a successful comparison (if $G_m R < 1$), as shown in Fig. 62b for $V_{cm} < 10$ V.

For a differential input ΔV_0 set at 10 mV, the transient of the outputs was simulated for common-mode voltages V_{cm} varying from 0 V to 20 V in steps of 5 V. In this case, a faster response is obtained with higher input common mode levels, and for $V_{cm} \leq 10V$ the comparison does not take place at all. This behavior is coherent with the effects the top-gate has on the TFTs. Indeed, for low top-gate voltages, the threshold of TFTs becomes so positive that M5 and M6 start working in the linear region. In this case, the positive feedback is too weak (or absent), and the resulting response slow. On the other hand, when the input common mode is high, the two input devices work in their saturation region providing the necessary output resistance to make the positive feedback effective.

7.1.4 Latch realization

The latch was realized and measured. The layout and the photograph are shown in Fig. 63.



Figure 63. Layout and photograph of the proposed latch. The proposed latch is placed in the middle, while on each side are one inverter and one buffer to drive the measurement setup.

In the layout, the inverter and the buffer integrated to drive the measurement setup are highlighted, while, in the photograph of the circuit, the position of each transistor is shown.

On the bottom, the pads reveal the fragility of the surface of the plastic foil. Indeed, each pad has a clear sign were the probe landed. Also, the number of pads is larger than the inputs and outputs of the circuit. In fact, additional pads have been included to be able to measure each transistor separately and compare their electrical properties, and to get a feeling of the matching between input devices and between output devices.



7.1.5 Latch measurements

Figure 64. Measured time-walk a) due to varying differential input and constant input common mode (V_{CM} = 18 V), and b) due to varying input common mode and constant differential input (ΔV_0 = 100 mV).

The corresponding measurements on the actual circuit, after the buffers, are shown in Fig. 64. Figure 64a shows the time-walk for a constant $V_{cm} = 18$ V and a varying differential input ($\Delta V_0 = 2.5$ V, 1.5 V, 0.5 V, 0.3 V, 0.1 V - values corrected for offset³). Figure 64b plots the time response for $V_{cm} = 10$ V, 12 V, 14 V, 16 V, 18 V and a constant $\Delta V_0 = 100$ mV. The results show, in agreement with simulations, that for common-mode voltages lower than 10 V the comparator does not work properly. In the two plots, the black lines show the clock signal that synchronizes the comparison.

7.1 A synchronous latched comparator

³ The offset was estimated while measuring the output voltage as a function of the input common mode (Figure 65). It was evaluated as the average between the minimum initial imbalance that always provides a positive comparison result and the maximum initial imbalance that always provides a negative comparison result. If the initial imbalance is between these two, the input noise randomly determines the polarity of the comparator output.



Figure 65. Measured output voltage as a function of the input common mode V_{cm} with a constant $\Delta V_0 = 100$ mV (after subtracting the offset). The blue, red and black lines represent respectively the positive, the negative and the differential output.

To get deeper insight in the dependence of the gain on the common mode input voltage, the single-ended and the differential outputs are shown in Fig. 65, as a function of the input common mode, applying a static differential input $\Delta V_0 = 100 \text{ mV}$. The latched comparator, measured using a semiconductor parameter analyzer with extremely high input impedance, can amplify the small differential input to a rail-to-rail differential output, meaning that the small-signal differential gain must be higher than $G_{diff} = 20 \text{ V}/100 \text{ mV} = 200 \text{ V/V}$. Such high gain, enabled by the positive feedback, is very beneficial to reduce the effect of the noise of the input devices on the comparison. Still from Fig. 65, the minimum input common mode needed for proper operation is estimated around 10 V, in line with what was concluded based on the CAD simulations and dynamic measurement. It is worth noting that the differential gain is not the slope of the black line; indeed each point in Fig. 65 represents the value of the outputs (or their difference) after the transient is completed, and the steady state has been reached.



Figure 66. Evaluation of the matching between a) input and b) output transistors. The corresponding relative error is shown in their own inset.

As stated in the beginning of the chapter, an important requirement on the comparators static performance is the input referred offset which in some converter topologies sets the

linearity limit. Since matching simulations could not be run due to the lack of suitable characterization, some additional test pads were included in the layout to be able to measure each transistor in the latch individually.

In this way, it was possible to measure and compare (Fig. 66a) the currents flowing through the input devices when diode connected (i.e. with inputs and outputs to ground) and the relative error of one current with respect to the other (inset). In a similar way, the output currents of the loads were compared. In this case however, the currents do not have the shape of a diode current, but of a Zero-Vgs connected TFT (Fig. 66b). The mismatch between the two drivers and between the two loads causes an offset of the latch of about $V_{off} = 3.4$ V. This offset is particularly large, even for large-area low-temperature technologies. One reason can be found in the weak top-gate transconductance. Indeed, let us consider, for instance, the flat-band mismatch ΔV_{FB} affecting the input devices. It contributes to the input offset with $V_{off,gate} = \Delta V_{FB}$ if the input is applied to the gate, but it is $1/\eta$ times larger (i.e. $V_{off,top-gate} = \Delta V_{FB}/\eta$, in our case $1/\eta = 4$) if the input is applied to the top-gate.

Exploiting the preamplifier shown in the previous chapter, which average gain is $G_{preampl} = 12$, the comparator can achieve an input referred offset of about $V_{off,input} = 280$ mV. Considering an input common-mode range of 10 V, this offset value makes the comparator suitable for a 5 bit flash ADC with a full scale input range. A continuous-time amplifier with higher gain would allow lower offset and higher accuracy, but the speed of the circuit would decrease too. A better solution would be to interpose between the preamplifier and the latch a differential parametric-capacitor amplifier (DPCA) like the one shown in Section 6.2.2. Indeed, the common-mode signal generated by the switching activity of the DPCA would be cancelled out by the differential input of the latch, and the low input capacitance of the latch would influence the output of the DPCA even less than the classic differential pair.

The latch dissipates a static power of about 30 nW when holding the result of the comparison. Due to the switching activity, a dynamic power depending on the capacitance loading at the outputs of the latch is also dissipated. For instance, for f_{clk} = 100 Hz the dynamic power dissipated is $P_{dyn} \sim 100$ nW.

7.2 A digital to analog converter based on a metal-oxide technology

At the end of the previous section, the linearity achievable by AD converters exploiting a flash topology was related to the statistics of the input offset of the latch. If the variability is too large, alternative topologies should be considered. For instance, in SAR ADCs, only one comparator is used and the input offset of the comparator only causes a rigid shift of the static characteristic without any detrimental effects on the linearity. On the other hand, linearity is determined by the linearity of the reference signal which is compared to the input signal, and that is generated by a DA converter. C-2C DACs for SAR ADCs have already been explored, leading to a maximum INL of 3 LSB for a resolution level of 6 bit before calibration [55], [36]. In the intent of investigating other DAC solutions, a current-steering DAC was analyzed, designed and characterized as described in this section.

7.2.1 GIZO technology

For this purpose, a current-steering topology was investigated exploiting a metal-oxide technology that has been recently proposed [90]. This technology employs Amorphous Gallium-Indium-Zinc-Oxide (GIZO or IGZO), which is an interesting semiconductor for manufacturing TFTs on foil because its mobility ($\mu \sim 20 \text{ cm}^2/\text{Vs}$) is superior to other common materials for large-area electronics (organic and a-Si have mobility $\mu \sim 1 \text{cm}^2/\text{Vs}$). The amorphous nature of GIZO grants also a good uniformity, contrary to Low Temperature Polycrystalline Silicon (LTPS), which still offers the best mobility among large-area TFT technologies ($\mu \sim 100 \text{ cm}^2/\text{Vs}$), but at the cost of larger variability. The optical transparency and the relatively low fabrication temperature (< 150°C) make this technology also especially suitable for display backplanes and related driving electronics [91], as well as for any kind of large-area applications on plastic foils, e.g. biomedical sensors, non-volatile memories [92], RFIDs [4], and alike.



Figure 67. Measured (symbols) and modeled (lines) a) transfer and b) output characteristics of a GIZO TFT (W = $1000 \mu m$, L = $100 \mu m$).

For circuit simulations, a physics-based analytical model of the GIZO TFTs has been developed in house similar to the one proposed in Chapter 4, and taking into account a Multiple Trapping and Release (MTR) charge transport in the channel of the transistor, instead of Variable Range Hopping (VRH). Also in this case, the Density of States can be considered exponential. The model is fully symmetrical and accurately describes (Fig. 67) the below-threshold, the linear and the saturation regimes via a unique formulation.



Figure 68. a) Stack and b) layout of the implemented GIZO TFTs.

For transient simulations, overlap capacitances between gate, source and drain have also been included (Fig. 68). In our simple model, both gate-source and gate-drain capacitors have a constant overlap component $C_{overlap}$ (much larger than in self-aligned silicon technologies), proportional to the finger width (FW) of the source and drain contacts, and a component depending on the channel accumulation which is divided between the two contacts. The parameterized cell (PCell) developed for our CAD system, only accepts an even number of subchannels SC, leading thus to a smaller gate-drain capacitance C_{GD} compared to the gate-source C_{GS} one:

$$C_{GS} = C_{GD} \left(1 + \frac{2}{sc} \right). \tag{61}$$

Moreover, the source metal is also connected to the periphery of the semiconductor layer that hence contributes only to the capacitance between gate and source.

7.2.2 Proposed current-steering DAC

Besides the possible use in smart sensors, one of the most promising applications for GIZO technologies are display backplanes where a DAC exploiting GIZO TFTs is integrated at the periphery [93], [94] of a display to generate the analog signals that define the image content. The adoption of the same technology for electronics and backplane avoids the use of separate silicon chips and complex interconnects, resulting in large potential cost savings. Crucial to this application are resolutions between 6 bit and 8 bit along with adequate speed (e.g. the row selection time for a video QVGA display is $68.3 \,\mu$ s). GIZO TFTs are suitable to build DACs due to their good mobility and uniformity, but so far only simple amplifiers, and no data converters, have been reported in literature [95], [96].

Switched capacitor, resistive or current-steering (CS) approaches can be adopted to implement a TFT DAC in this context. The first two implementations [93], [94] rely on the relative accuracy of passive components, and are thus suited to the LTPS technology, which offers poor TFT uniformity. On the other hand, the CS approach is particularly interesting in combination with AMOLED displays, as it allows current programming in the pixel [33], which can effectively compensate for both threshold and mobility variations in the backplane: an attractive solution to obtain excellent OLED uniformity and increase resilience to ageing.

Current-steering DAC analysis

The current-steering DAC is a converter that produces a current proportional to the digital input word. In our implementation, every bit of the digital input D_{IN} controls a binary weighted current so that, for N bit resolution, it is possible to generate 2^{N} -1 current levels. In the case a voltage signal is required at the output, the current can be converted into a voltage by means of a linear resistor, as depicted in Fig. 69.



Figure 69. Current-steering DAC topology exploiting a resistor in a negative feedback for linear I-V conversion. The output voltage V_{DAC} is proportional to the output current I_{DAC} .

In our case, linear resistors are not available and negative feedback configurations are problematic. Moreover, for display applications the DAC is typically loaded by a diode, hence a diode connected load was used to convert the current in a voltage (TFT M4 in Fig. 70).



Figure 70. Transistor level schematic of the unity current source and building block schematic of the 6bit CS-DAC.

Of course this kind of load is far from linear and, thus, a differential approach (Fig. 70) was used to cancel the even non linearities. The two input devices switch the unity current (corresponding to a single LSB) completely to the one branch or to the other, with one of TFTs M2 always strongly on and the other strongly off. In this way, however, the bias of the drain tail
transistor M1 depends on the output voltage, and hence on the input signal, creating non linearities and distortion. Moreover, the switching activity of the input device causes a considerable charge injection to the output nodes due to the large overlap capacitances associated with TFTs (in particular the gate-drain capacitance C_{GD}).

In order to solve these two problems, cascode transistors M3 have been included in the design of the unity cell (Fig. 70). Indeed, they increase the output resistance of the cell (without diode load), making the unity current less sensitive to different output voltages, and they reduce the effect of the charge injection from the differential input to the differential output.

These cascode devices allow also an easy solution to apply post-fabrication calibration (which was not exploited here though). Indeed, controlling independently the bias V_{cas} of each binary weighted cell, the current can be adjusted.

Current-steering DAC design

To avoid complex control logic, a CS-DAC with unary current source and binary selection has been chosen (Fig. 70). In this case, the maximum DNL can be related to the statistical current error Δ I in the unity current sources of the DAC (Eq. 3.41 in [97]):

$$DLN_{max} = \pm 2 \, 2^{\frac{n-1}{2}} \frac{\Delta I}{I} \tag{62}$$

where n is the number of bits and I the unity current. At a first approximation, the maximum normalized current error $\Delta I/I$ is due to threshold and mobility variations, thus $\Delta I/I > \Delta \mu/\mu$, $\Delta \mu/\mu$ being the maximum normalized mobility variation. In the GIZO technology used for this design, on an area comparable to the one occupied by our DAC, $\Delta \mu/\mu$ has been measured to be 4% [4]. Based on this information and Eq. (62), the DNL_{max} of a 7 bit DAC would be worse than 0.64 LSB. For the sake of compactness and simplicity, a 6 bit resolution was preferred. In this way, half the amount of unity cells and interconnection is required, with a great save in area and better hard faults probability. Moreover, from this implementation a DNL better than half LSB would be expected.

In this unipolar technology, like in the one described in Chapter 4, transistors are normallyon. For this reason the implementation of current mirrors is inaccurate (as discussed in Chapter 6), and the unity current cannot be provided by an external reference. Therefore, the current of the unity cell is defined by means of the W/L ratio and threshold of the Zero-Vgs connected device M1. With this approach, the only way to change the unity current after fabrication is by means of the cascode bias V_{cas} . As it will be shown later, the cascode bias is used here to correct the static characteristic of the converter, but it can also be used to define the full scale output current. This value should be chosen considering the application addressed, and the unity current should be scaled accordingly. A larger current could drive more easily the parasitic capacitive load enabling better dynamic performance of the converter. On the other hand, a smaller current would dissipate less power.

Current-steering DAC realization

Also for this technology, information on matching and parameter variations was very limited. However, it is reasonable to expect that, due to the large-area nature of the process, in addition



to short-distance Gaussian variations, also long-distance gradients affect the process parameters, and thus the matching between the devices (and eventually the DAC linearity).

Figure 71. a) Layout and b) photograph of the measured current-steering DAC manufactured in amorphous GIZO technology.

For this reason, a common centroid criterion was followed to place the 63 unity current sources of the converter. In Fig. 71a, the common centroid floor plan is shown. For instance, the third bit controls four unity cells (boxes numbered with 4), which are located symmetrically with respect to centre of gravity of the layout.

In this way, however, unity cells connected to the same input bit can be located quite far and interconnections among them become very long and resistive. Multiple interconnections have been drawn (Fig. 71b), to reduce their resistance and to avoid circuit failures due to scratches on the surface of the plastic foil. Indeed, the surface of the circuit can be damaged easily, causing a hard fault if an interconnection is broken (e.g. the white spots in Fig. 71b). The final circuit occupies an area of $6.5 \times 9.5 \text{ mm}^2$.

Measurements

For the sake of simplicity, the DAC has been characterized measuring the differential output voltage V_{diff} with an oscilloscope. The circuit is supplied at V_{DD} = 3 V and the measured full scale current is 380 μ A.

From the comparison between the single ended and the differential output, shown in Fig. 72, it is clear that the differential readout cancels the even non-linearity of the diodes avoiding a strong increase in INL. Without any additional correction the maximum integral non linearity is $INL_{max} = 0.7 LSB$ and the maximum differential non linearity is $DNL_{max} = 1.2 LSB$. In the specific measured instance, the largest contribution to the DNL was not caused by the commuting of the

7.2 A digital to analog converter based on a metal-oxide technology



MSB, as it would be expected, but by the MSB-1. This unusual result is most probably due to a soft/hard fault on a unity current source connected to the MSB-1.

Figure 72. Measured characteristics of the CS-DAC a) before and b) after the MSB-1 adjustment and corresponding INL and DNL in the inset.

For this reason, to investigate the effects of possible calibration schemes, the (MSB-1) current has been tuned by reducing the corresponding driving logic '1' voltage from V_{DD} to 2.6 V, as proposed in [24]. The correction was applied in this case directly to the input TFTs M2 of the unity cell. However, in an actual self-calibrating system, a similar correction could be applied to the cascode voltage V_{cas} used to bias the gate of M3. Indeed when the differential switch directs the unity current, one transistor M2 acts like an open circuit and the other shortens the source of the cascode device M3 to the tail transistor M1. In this way the drain-source voltage on the tail device depends on V_{cas} (i.e. $V_{DS,1} = V_{cas} - V_{GS,3}$) and a reduction of V_{cas} allows the reduction of the unity current in the cell. After the adjustment of the current of the (MSB-1) bit, an INL_{max} of 0.2 LSB and DNL_{max} of 0.3 LSB have been measured (Fig. 72b).



Figure 73. Measured DAC output spectra for a signal frequency of 30 kHz and 300 kHz normalized to the output signal amplitude (V_c). Sampling rate $f_{SAM} = 1$ MS/s.

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The output spectra of the differential voltage V_{diff} , measured using a sampling rate $f_{SAM} = 1$ MS/s, are shown in Fig. 73a for a 30 kHz and in Fig. 73b for a 300 kHz full-scale sinusoidal input signal. The amplitude of the 30 kHz output is about 0.25 V.



Figure 74. Measured Spurious Free Dynamic Range (SFDR) as a function of the input frequency for different sampling frequencies f_{SAM} .

A first order roll-off after ~ 80 kHz, due to the capacitive loading offered by the measurement setup ($C_P \sim 100$ pF which is much bigger than the internal parasitics), is observed at higher signal frequencies. Figure 74 displays the measured SFDR (Spurious Free Dynamic Range) of the DAC output, shown for sampling rates f_{SAM} going from 10 kS/s to 10 MS/s. An SFDR better than 50 dB can be achieved for input frequencies up to 10 kHz and better than 30 dB for input frequencies up to 300 kHz.



Figure 75. Measured time response to a single bit step. For the lower line, only the LSB was switched from '0' to '1', while for the lager step only the MSB changes.

Another way to estimate the DAC dynamic behavior, especially relevant to the application of the column signal generation in displays, is the time-domain response. The transient of V_{diff} , when a single digit of the input word switches to '1' (Fig. 75), settles in about 4 μ s. Considering for instance QVGA applications (display matrix of 320x240 pixels at 30 frames per second), the CS-DAC is then suitable for a 20x multiplexing factor among pixels of the same row.

Considering the DAC linearity and speed, this component could also be used to design a 6 bit resolution SAR converter with a conversion rate in the order of 100 kS/s (allowing 6 μ s for

	[24]	[<i>93</i>]	[94]	This work	
Technology	p-type OTFT	a-Si:H	LTPS	GIZO	
DAC implementation	Current steering	Capacitive	Resistive	Current steering	
DAC resolution	6b	7b	8b	6b	
Area	2.6x4.6 mm ²	8 mm ²	0.12x3 mm ² (1)	6.5x9.5 mm ²	
Voltage supply	3.3 V	20 V	N.A.	3 V	
Full scale output current	79 µA	N.A.	N.A.	380 µA	
DNL _{max}	0.69 LSB	0.6 LSB	1 LSB	0.3 LSB	
INL _{max}	1.16 LSB	1 LSB	> 1 LSB	0.2 LSB	
SFDR _{max}	32 dB	N.A.	N.A.	55 dB	
Max. Sampling rate	100 kS/s	N.A.	N.A.	10 MS/s	
Settling time	N.A.	~40 µs	~3 µs	~4 µs	

comparison and logic). A benchmarking among the GIZO DAC and organic [24], a-Si [93] and LTPS [94] state of the art DACs for large-area applications is presented in Table V.

7.3 VCO-based analog to digital converter

The two main causes of non-linearity in several ADC topologies are a variable offset among different comparators, and a nonlinear reference. In case of flash ADCs both of these contributions need to be taken into account, while for SAR ADCs only the linearity of the reference source plays a role on the overall static characteristic. As shown in Chapter 5, a solution that overcomes also the issue of a linear voltage reference can be found in the integrating ADCs. In this case, the design effort is mainly focused on the linearity of the integration and on the realization of a low-complexity logic. This approach brought us to obtain the smallest large-area converter reported in literature, and to achieve the highest linearity to date without any analog calibration technique, just applying an offset-gain correction on the output data.

7.3.1 Proposed VCO-based ADC

The integrating AD converter proposed is a VCO-based ADC where the matching issue is avoided basing the resolution on the conversion time, and the conversion linearity on the linearity of the voltage-frequency characteristic of a single Voltage Controlled Oscillator (VCO). Indeed, the conversion principle is based on amplitude-to-frequency conversion first and on a frequency-to-phase conversion afterwards. Moreover, in ultra-low cost applications, like smart sensors integrated in packaging of food or pharmaceuticals (see Chapter 2), the system complexity needs to be low in order to achieve high circuit yield against hard and soft faults. For this reason, digital post-processing is left to the base station that retrieves the digitalized data, while the proposed ADC is mostly digital, and exploits only one VCO and a 10 bit ripple counter (Fig. 76a).

Converter analysis

The VCO-based ADC is made of only two building blocks (Fig. 76a) reducing drastically the circuit complexity and the hard/soft fault probability.



Figure 76. a) Building block schematic of the implemented VCO-based ADC and b) conversion principle.

The conversion principle is explained visually in Fig. 76b. The input signal controls the oscillation frequency of the voltage controlled oscillator f_{VCO} . The ripple counter is used as a digital integrator to count the number of full periods during the integration time T_{INT} and the count number gives the digital output word. Since the linearity is not based on matching, in first approximation it is not affected by process variations, which can only cause offset and gain errors. The size of these errors can be estimated by the base station that receives the raw data and adjusts, for instance, the integration time to correct the gain error. Another solution is to preserve a constant integration time (for instance generated by a local oscillator) and to convert, in the beginning, an input signal equal to the extremes of the input range. In this way the base station can easily extract for the specific VCO-based ADC the right offset and gain errors, which are trivial to correct in the digital domain by the base station. It is important to notice that the local oscillator generating the integration time does not need to be long-time stable, if the base station applies the gain and offset corrections frequently enough.

Converter design and simulation

This section deals with the design of the VCO-based ADC. First, the voltage controlled oscillator and the linear transconductor used to control the oscillation frequency are presented. The logic style used for our digital circuits will be extensively studied in Chapter 8, thus only a short discussion on the ripple counter is given here.

Voltage controlled oscillator

The VCO designed for our converter comprises 7 fixed-delay inverting stages and a noninverting tunable delay cell (Fig. 77a). The tunable delay is much larger than the delay of the seven inverters, and hence it dominates the oscillation output frequency. The fixed-delay chain made by the seven inverters accomplishes two tasks. First, it defines the temporal width of the negative pulse (that should last enough to reset the output node 'out'); second, it squares the



saw tooth signal provided by the tunable delay cell in order to trigger the clock input of the ripple counter with a squared signal.

Figure 77. a) Building block schematic of the voltage controlled oscillator and b) simulated temporal behavior of the output of the tunable delay cell (black) and the output of the VCO (gray).

After the capacitor C has been reset, a current proportional to the input voltage V_{in} is provided by a linear transconductor, generating a linear ramp at the output of the delay cell (Fig. 77b). When the linear ramp reaches the threshold voltage of the first inverter of the chain of seven inverters, an edge starts propagating through the fixed delay line. After the fifth inverter the negative pulse triggering the counter is generated and after the seventh the capacitance C is reset by the switch. At this point a second edge starts propagating through the delay line, the trigger is brought back to the logic state "high", and the switch opens allowing the capacitor to charge up again.

The pull-down of the non-inverting element is performed connecting the output node to ground by means of a low impedance, hence it is very fast and introduces a negligible delay compared to the one of the delay cell. On the other hand, the pull-up time depends on the load capacitance (C = 500 fF) and on the small output current provided by the transconductor. Therefore, the negative pulse width is independent of the input signal, and the maximum and minimum output frequencies of the oscillator mainly depend on the maximum and minimum currents provided by the transconductor.

Linear transconductor

The transconductor used in this circuit improves the one presented in the previous chapter: it requires only two OTFTs instead of five and achieves better performance in terms of linearity and output resistance. Another feature of this transconductor is that the input signal is fed through the top-gate, which provides extremely low capacitance (the top gate dielectric is $1.4 \,\mu$ m thick), minimizing the sensor capacitive load to just about 34 fF.



Figure 78. Schematic of the transconductor used in the VCO.

In this transconductor (Fig. 78), the current source M1 is used to bias the common gate TFT M2. Varying the top-gate voltage of the input transistor M2, its threshold voltage changes linearly, as shown in Chapter 4, and so does the gate-source voltage of M2 (biased with an almost-constant current). This variation affects only the source voltage of M2 since its gate is connected to the supply, hence a linear relation is created between the source-drain voltage of M1 and V_{in}. The channel length modulation of M1 will then generate a linear variation of the current in M1 (and thus of the output current) with V_{in}. The connection of the top-gate of M1 to its drain adjusts the value of the output resistance, further improving the linearity. One should also remind that our p-type OTFTs are normally-on, and thus the source voltage of M2 can indeed be lower than its gate bias, V_{DD} , while keeping correct circuit functionality.

Ripple counter

The digital counter performs the integration that converts the analog input frequency into a digital output; for this reason, the number of stages of this circuit determines the maximum resolution of the circuit. In our case, a 10-stage ripple counter was designed employing 10 data flip flops (DFF), hence 10 bit is also the maximum resolution achievable when the correct integration time is allowed for the integration. It is worth noting, however, that the effective number of bits (ENOB) can be less, due to thermal noise in the voltage controlled oscillator that causes jitter at the input of the counter, and to the non-linearity of the VCO.



Figure 79. Building block schematic of the ripple counter in use.

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The building block schematic of the ripple counter is shown in Fig. 79. The output signal of the VCO triggers the first stage, while all the others are triggered by the output of the previous one. From a system point of view, the only requirement on the ripple counter is the speed, since the counter has to be able to increment its output of one unit at the maximum frequency achievable by the VCO. Due to the slow VCO output the ripple counter speed is more than sufficient and this counter structure, which enables the smallest amount of logic for a given maximum count, could be used.

The logic used to design this circuit is analyzed in depth in the Chapter 8, as well as the schematic of the DFF.

Converter realization

The photograph of the complete converter is shown in Fig. 80. Thanks to the simplicity of the circuit topology, the analog circuitry is reduced to the minimum and most of the area is occupied by the digital counter.



Figure 80. Photograph of the VCO-based ADC on foil.

The whole converter, including contact pads, occupies less than $3.5 \times 5.7 \text{ mm}^2$. This is by far the smallest converter realized with large-area technologies (see Table 7.2). In fact, the area is 19.4 mm², almost 14 times smaller than previous works [35] that reaches lower effective resolution and uses the same TFT technology.

Converter measurements

In this section, first are shown the measured data characterizing the linear transconductor since they are fundamental for understanding the measurement results on the VCO that are shown afterwards. Then, they are related to the static performance of the full converter. Unfortunately an error in the layout of the ripple counter hampered the measurement of the whole system and an external counter has been used instead. However, the functionality of the same data flip-flop is experimentally demonstrated in Chapter 8.

Linear transconductor



Figure 81. a) Transfer and b) output characteristics of 54 transconductors measured: the thick lines are measured from the transconductor closest to the VCO characterized.

With respect to the topology shown in the Chapter 6, higher linearity and higher output resistance have been reached by trading them off with the tunability to cope with parameter variability. To this extent, Fig. 81 shows the measurements of 54 transconductors manufactured on the same foil and affected by the typical variability that cannot be, in this case, corrected. The maximum current, for instance, varies of about one order of magnitude among all samples, causing gain and offset variations in the ADC characteristic. These variations however can be corrected in the digital domain on the digital output. In fact, offset correction could be easily performed using an up/down counter, and the gain can be adjusted by means of a digital divider. This circuit anyway demands too complex digital logic to be integrated on chip with our technology, as this would introduce yield and area issues. An effective solution to variability would be thus to convert first the two rail voltages, and then the voltage of interest, letting the base station correct the offset and gain after transmission of these three digital values.



Figure 82. Normalized current linearity error for the 54 samples measured. The thick line is measured from the transconductor closest to the VCO characterized.

7.3 VCO-based analog to digital converter

Following this approach, the only residual linearity error comes from the integral nonlinearity (INL). The variability of the linearity is remarkably smaller than the absolute variation of the current. This can be seen in the graph showing the normalized current linearity error in Fig. 82. In this plot, the error current of each transconductor is first evaluated as the difference between the measured current and the linear interpolation through the extremes. Then it is divided by the current corresponding to an input voltage equal to half the input range. The outcome of this elaboration shows a systematic behavior of the error, due to the nonlinear relation between the output current and the drain-source voltage applied. This non linearity is due to the channel length shortening which is less sensitive than other process parameter to variations, as for instance the threshold voltage or the mobility. For this reason, the variability of the normalized current linearity error (Fig. 82) among the various transconductors is much less than the variation of the absolute current.

The thick lines in Fig. 81 and 82 represent the measurements performed on the transconductor closest to the VCO that was fully characterized. The transconductance for a DC input voltage V_{in} of 10 V, and in saturation regime, is ~ 8.5 pA/V. The output resistance for $V_{in} = 5 \text{ V}$ is ~ 4.8 T Ω .

Voltage controlled oscillator

Figure 83 shows an example of the output signal coming from the VCO and triggering the counter.



Figure 83. Measured output of the VCO for maximum (blue line) and minimum (red line) input voltage, for respectively $V_{in} = 20$ V and $V_{in} = 0$ V.

For the measured sample, the VCO output frequency goes from 4.15 Hz (red line) to 37.65 Hz (blue line) for a rail-to-rail V_{in} variation (0 V to 20 V).

The full converter

As shown at the beginning of this section, the digital output can be obtained integrating the VCO output for a fixed time T_{INT} . Since integration is a linear transformation, the linearity of the final converter can be estimates by the linearity of the VCO voltage-frequency characteristic (Fig. 84).

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Figure 84. Measured voltage-frequency characteristic of the VCO characterized. Circles show the measured data while the red line is the linear fit through the extremes.

A longer integration time improves the resolution of the conversion, as it reduces the effects of thermal noise. In our case, was measured an SNR between the VCO period and its jitter of ~ 48 dB, corresponding to an ENOB due to noise only: $ENOB_{noise} = 7.7$ bit. As the resolution N of the converter depends on the frequency range f_{span} of the VCO and on the conversion time T_{INT} , the minimum conversion time needed to exploit the noise-limited SNR is $T_{INT} = 6.2$ s. The INL and DNL of the converter are plotted in Fig. 85 with the resolution of the converter fixed to 6 bits and for a rail-to-rail input range. The worse-case INL is 1 LSB, while the maximum DNL is 0.6 LSB. Measurements were performed using an external counter, due to the layout problems affecting the integrated one.



Figure 85. Measured INL and DNL of the converter at 6 bit resolution exploiting a rail-to-rail input range.

In the realized chip, ten DFFs, designed according to the logic style that will be discussed in Chapter 8, are connected to implement the 10 bit ripple counter that was integrated with the VCO. To guarantee the correct behavior of the circuit, the counter needs to be functional up to the maximum frequency that can be generated by the VCO, which is, in this case, \sim 40 Hz.

The VCO draws a current of ~ 300 nA, while the current consumption of the counter (based on the measurements performed on the shift register shown in Section 8.1.4) is almost ~ 2.1 μ A. The SNR and linearity demonstrated improve the state of the art [35], [36] (Table VI) and could be obtained exploiting the linearity of the proposed transconductor, rather than the poor matching of organic technologies, together with digital-only offset and gain corrections.

munajuctureu with low-temperature technologies on jon									
	Architecture	Resolution	SNR [dB]	DNL [LSB]	INL [LSB]	Current Consumption	Area [mm ²]		
[35]	ΣΔ Μ	4.1bit	26.5	N.A.	N.A.	100μΑ	260		
[36]	SAR (C2C-DAC)	6 bit	N.A.	2.6 ⁽¹⁾	3 ⁽²⁾	1.2μΑ	616		
[34] This work	VCO-based	6 bit	48	0.6	1	2.4µA	19.4		

Table VI. Benchmark among this work and state-of-the-art ADCs manufactured with low-temperature technologies on foil

(1) ENOB evaluated from the SNR

(2) Of the C2C-DAC before calibration

7.4 Conclusions

In this chapter, the design of data converters in large-area unipolar technologies was discussed. In particular, a latched comparator was first analysed, since it is needed in all ADC architectures of the type shown in Fig. 26 and which forms the fundamental building block in a flash ADCs. Indeed, in flash converters, a large number of comparators (exponentially increasing with the resolution N, i.e. 2^{N} -1) compare the input signal to the same number of reference voltages. This topology targets fast applications, hence a fast comparison is required. For this purpose, the design started from a standard latch design and its time response was improved approximately by ten times (from 50 µs to 5 µs), achieving the limits imposed by the technology. Differently from other comparators manufactured with large-area technologies [71], the proposed one also provides rail-to-rail outputs with a great benefit for the circuitry following. Some design choices have lower the load for the circuit driving the latch. To this end, exploiting the double-gate feature of the technology, the input capacitance was reduced more than two orders compared to the basic latch implementation. This result makes the latch compatible with the differential parametric amplifier shown in the previous chapter: a perfect solution to reduce the input referred offset of the latch and achieve higher ADC linearity.

To improve the converter linearity, different ADC topologies can be employed. For instance, SAR converters adopt only one comparator. Hence, the non linearities only depend on the reference generated by the DAC. For this reason, a current-steering DAC was designed, that can be employed both for AD conversion in SAR ADCs or as a pixel driver in display applications. The final design demonstrates good linearity (of about 6 bit) and high speed, due to the high mobility of the metal-oxide technology exploited. The better linearity, compared to other current-steering DACs demonstrated in large area electronics, is achieved thanks to a differential approach, to a common centroid layout, and to a technology providing better uniformity and thus matching.

Finally, an integrating ADC was discussed. Indeed smart-sensors manufactured with largearea electronics mainly target quasi-static applications and this converter topology provides, for such applications, better linearity and less complexity. A VCO-based ADC was exploited that consists of only two building blocks: a VCO and a digital counter. The proposed VCO is based on a linear transconductor that improves linearity and output resistance of the one discussed in Chapter 6. The proposed ADC achieves better linearity than other ADCs reported in literature and occupies a considerably smaller area, with beneficial effects on the yield.

8 Circuit design for digital processing

Digital circuits are extensively used in any integrated system, sometimes to assist analog or mixed-signal functions and sometimes to perform logical operations. In both cases, logic gates should achieve high gain and large noise margin in order to provide robustness and enable high circuit yield. In this chapter, a new logic style is proposed that, compared to known approaches, improves gain, noise margin, and yield. Furthermore, exploiting only control signals within the power supply range, the proposed logic enables the integration of control circuits to automatically correct for process variations and aging. The content of this chapter has been published in [37].

8.1 The proposed Positive-feedback Level Shifter logic

The detailed analysis of the state of the art logic styles shown in Chapter 5 allows to point out a few issues which concern present digital logic manufactured with TFTs on foil. First of all, the gain and the symmetry of the input-output characteristic should be large enough to guarantee the necessary noise margin. Next, process variations should not compromise the functionality of the logic. As this is not the case in large-area low-temperature technologies, a post-processing tuning control is desirable.

To enable practical applications of large-area electronics on foil, the post-processing tuning should be performed automatically by the circuit, and not use arbitrary-large voltage sources in the laboratory. To enable the integration of such control circuitry, a Positive-feedback Level Shifter (PLS) logic is proposed. This logic only exploits control signals that are within the power supply range, to control the symmetry of the characteristic and achieve high noise margin despite the considerable process variations.

8.1.1 PLS logic analysis

For our PLS logic, a two-stage topology is exploited where the output stage is a double-gate enhanced logic gate with Zero-Vgs connected load (see Chapter 5), and the first stage is a tunable level shifter LS (Fig. 86). As explained in Chapter 5, in the dual-gate enhanced output stage the threshold between the input logic "zero" and input logic "one" is controlled by a tuning input. If the voltage applied to this input (- ΔV) increases, the threshold voltage becomes lower. In the level shifter, two inputs control the amount of shift between the input and the output signal: when the control inputs increase, one (- ΔV) increases the shift and lowers the threshold voltage V_{trip}, while the other (+ ΔV) decreases the shift and increases V_{trip}. The output stage determines the function of the whole logic gate: in Fig. 86a is shown the block-level schematic of our PLS inverter, while in Fig. 86b is shown the schematic of a PLS NAND. These two gates were designed and used in our digital circuits: any other logic function can be implemented based on these two, as known from the Boolean algebra.



Figure 86. Building block schematic of a) a PLS inverter and b) a PSL NAND gate.

In these circuits, V_{tr} is a control voltage that varies the position of the logic threshold, and thus the symmetry of the characteristic. It is applied in both the shifter and the inverter so that, for increasing V_{tr} , the threshold between login "zero" and logic "one" at the input is shifted to

lower input voltages. In this way, the effectiveness of the trip-point control is strongly improved with respect to the double-gate enhanced logic, and the transfer characteristic of the inverter can be shifted almost over the full input range, while still exploiting a control voltage within the supply rails.

The second input of the level shifter, the one decreasing the shift, is connected to the output of the inverter. In this way, a positive feedback is created around the trip point that drastically boosts the gain of the inverter. Let us consider, for instance, a transition low-high of the input, the normal operation of the level shifter and of the inverter respectively increases the intermediate voltage V_i (the level-shifted version of the input voltage) and brings the output down. As in the PLS logic the inverted output is connected to the $-\Delta V$ input of the level shifter, the voltage difference between V_i and the input voltage V_{in} further increases when the output drops. The voltage V_i raises more than what the input alone would be able to do, making in turn the output drop more. A positive feedback loop is thus generated and a considerable increase of the gain is achieved.

In order to describe the features of the PLS logic, the PLS inverter will be considered; however, all the concepts that follow directly apply also to the NAND gate.



Figure 87. Two different embodiments of the PLS inverter: a) one that achieves wider trip point tunability, b) another that achieves larger gain and noise margin.

Two transistor-level implementations of the schematic in Fig. 86a are shown in Fig. 87. The output inverter is embodied by transistors M3 and M4, while the level shifter is formed by M1 and M2. In the embodiment of Fig. 87b, the combination of transistors M2 and M2b allows a higher gain for the positive feedback loop.

To analyze the circuit behavior, it is first investigated qualitatively how the control voltage V_{tr} shifts the characteristic, and then how the positive feedback affects the inverter gain. Equation (10) shows that the voltage applied to the top-gate of TFTs M2 and M4 causes a variation of their threshold voltage and thus of $V_{SG,1}$ and $V_{SG,3}$. Moreover, the variation of $V_{SG,3}$ also affects the bias current in the level shifter, thus reinforcing the effect on the shift between V_{in} and V_{i} .



Figure 88. Simplified small-signal equivalent circuit for the evaluation of the loop gain G_{loop}.

In order to evaluate if the gain in the positive feedback loop is larger than 1, and thus sufficient to guarantee regeneration, we can assume that V_{in} has a fixed value, open the circuit on the gate of the output pull-up transistor M3, place a small-signal voltage source v_s on this node, and evaluate the gain between v_s and v_i .

As shown by the small-signal equivalent circuit in Fig. 88, the pull-down TFT M4 and the source follower M1 can be replaced with an equivalent resistor. Indeed the first TFT works in saturation with a constant overdrive ($V_{GS} = V_{TGS} = 0 V$) and can be replaced with its output resistance $R_4 = r_{0,4}$, while the second one has both gate and top-gate connected to bias points, and can therefore be replaced with a resistor equal to:

$$R_1 = \frac{1}{g_{m,G1} + g_{m,TG1}} \tag{63}$$

where $g_{m,G1}$ and $g_{m,TG1}$ are the transconductances associated respectively to the gate and to the top-gate. Also the gate and the top-gate transconductance of M2 play a role in the smallsignal loop gain. The gate is connected to the drain and thus the gate transconductance can be replaced by a resistor $R_2 = 1/g_{m,G2}$. The effect of the top-gate is modeled as a voltage controlled current source with transconductance $g_{m,TG2}$. Using the simplified equivalent circuit in Fig. 88, the loop gain G_{loop} can be evaluated as:

$$G_{loop} = \frac{v_i}{v_s} = -g_{m,G3} r_{0,4} \left(-\frac{g_{m,TG2}}{g_{m,G1} + g_{m,TG1} + g_{m,G2}} \right)$$
(64)

Considering that both M1 and M2 work in saturation, since they have the same dimensions $(W_1/L_1 = W_2/L_2 = 10 \,\mu\text{m}/5 \,\mu\text{m})$ and are biased by the same current, can be assumed $g_{m,G1} = g_{m,G2}$. Furthermore, $g_{m,TG} = \eta g_{m,G}$ due to the different impact of the gate and the top-gate voltages on the channel current (Eq. (9) and (10)). Therefore, Eq. (64) can be rewritten as:

$$G_{loop} = \frac{\eta}{2+n} g_{m,G3} r_{0,4} \tag{65}$$

In order to take effective advantage of a positive feedback, the loop gain G_{loop} should be larger than 1, which can be easily achieved increasing the channel width of M3 or the channel length of M4.

8.1 The proposed Positive-feedback Level Shifter logic

If the loop gain is larger than one, the positive feedback also causes hysteresis, as it will be clear from the measurements. Indeed, at the beginning of the low-high transition of the input, the voltage applied to the top-gate of M2 is high: the small current in M2 causes a small shift between V_{in} and V_i , thus the trip point of the inverter is slightly closer to V_{DD} . On the other hand, when the input transition is high-low, M2 is more conductive in the beginning: the shift between V_{in} and V_i is larger and the trip point is closer to ground. However this hysteresis is not detrimental, but beneficial for the noise margin of the single inverter (Section 8.1.4). Some issues are related to the combination of a large hysteresis loop together with large process variations, as explained in Section 8.1.4.

8.1.2 PLS inverter design

The choice of the dimensions of each transistor can be investigated now, being aware of the main mechanisms taking place within the PLS inverter. Our assumption is that, in the ideal case, the trip point should be around $V_{DD}/2$ with a control voltage $V_{tr} = V_{DD}/2$. Also the fan out of the inverter is assumed to be minimum, thus the minimum channel width will be chosen.

Considering the output stage, it is clear that the W/L ratio of M3 has to be much smaller than that of M4. Indeed, when a low output voltage is required, both M3 and M4 have Zero-Vgs (M4 because of the connection; M3 because V_i equals V_{DD}) and M4 needs to drive much more current than M3 to effectively pull down the output node. On the other hand, when the output has to be high, M3 can take advantage of a source-gate voltage as large as approximately V_{DD}, which results in a much larger current than the one provided by M4. For this reason, in gates with minimum fan out (i.e. designed to drive only one other logic gate), M3 is designed as minimum size TFT and M4 is chosen to ensure a good logic low output. For this reason, the final dimensions are $W_4/L_4 = 700 \,\mu\text{m/5} \,\mu\text{m}$ for M4, and $W_3/L_3 = 10 \,\mu\text{m/5} \,\mu\text{m}$ for M3. A final remark is that the product $g_{m,G3} r_{0,4}$ must be large enough to ensure a positive feedback loop (Eq. (65)). If this would not be the case, a longer channel for M4 should be chosen.

The level shifter devices can be designed with the same aspect ratio for both M1 and M2. Indeed, the amount of DC shift is independent of the absolute dimensions of the devices and even for equal dimensions for M1 and M2, M2 provides enough current to create the required amount of shift between V_{in} and V_{i} . Moreover, as the node V_i is lightly loaded by the small transistor M3, the current in the input branch does not need to be increased because of speed considerations. For this reason, M1 and M2 are also designed as minimum size TFTs to minimize the area occupied by the PLS inverter.

Obviously, if the fan out of the gate must be increased, all TFT widths can be scaled up, keeping the W/L ratios constant.

8.1.3 Test foil design

In order to design a digital circuit with high yield, it is also extremely important to understand how the spread of the technology parameters affects a large number of logic gates.



Figure 89. Floor plan of the measured 50x70 cm² plastic foil enclosing four 15x10 cm² tiles. The four groups included in each tile have 18 repetitions of the PLS inverter.

To be able to get such an insight, many inverters were placed on a plastic foil of $50x70 \text{ cm}^2$. The measured inverters can be divided in 16 groups of 18 inverters close to each other. As depicted in Fig. 89, the 16 groups are divided on four tiles which are spread on the foil surface and each tile includes 4 groups of inverters. The tiles have a surface of $15x10 \text{ cm}^2$ while each group occupies an area of $4x26 \text{ mm}^2$. For a fair comparison, an equal number of PLS and Zero-Vgs load inverters was designed for measurement on the same foil and in the same regions.



Figure 90. Photograph of one $10x15 \text{ cm}^2$ tile. The PLS test structures and the some of the circuits presented in the previous chapter have been measured on foils like this.

On the same foil, also some analog and digital circuits have been placed: among them a 240-stage shift register made using the PLS logic style (Section 8.1.4). This is, to our knowledge, the circuit with highest transistor count ever realized with organic semiconductors (Fig. 90).

8.1.4 Test foil measurements

In this section, are first shown the measured data characterizing a single PLS inverter. Then a statistical analysis will be provided to analyze the improvement that the PLS approach offers with respect to the most common inverter topology, i.e. the Zero-Vgs loaded inverter.

Single PLS inverter

The measured data shown here prove the strong features of the PLS inverter. First, the trip point tunability and the gain are characterized. Then their relation to the improved noise margin and other benefits of the PLS topology are discussed.

Trip point



Figure 91. Measured transfer characteristics of a PLS inverter sweeping V_{tr} from 0 V (rightmost plot) to 20 V in steps of 1 V. V_{tr} = 14 V returns for the measured instance the most symmetric characteristic and hence the highest noise margin. The black line shows the characteristic obtained applying the ideal bias V_{tr} = V_{DD}/2 = 10 V.

As shown by the measured inverter transfer characteristics in Fig. 91 (in continuous lines for the forward measurements and dashed lines for the backward ones), using V_{tr} to vary at the same time the threshold of M1 and M3 results indeed in an effective control of the inverter trip voltage, which can be shifted from about gnd to V_{DD} while keeping the control voltage V_{tr} within the supply range (the different transfer characteristics have been measured for V_{tr} sweeping from 0 V, the rightmost curve, to V_{DD} , the leftmost curve, in steps of 1 volt).

It is worth noting that, as a consequence of parameter variations and aging [98], the designed bias ($V_{tr} = 10$ V) produces, in this particular inverter, a transfer characteristic switching at about 15 V (black line in Fig. 91). Applying a control voltage $V_{tr} = 14$ V corrects this asymmetry: the inverter transfer characteristic becomes perfectly symmetric with respect to the input range.

Gain

A large gain is mandatory in an inverter to regenerate weak signals and to achieve high noise margin. Organic TFTs suffer from low output resistance and small-signal transconductance, hence the maximum gain of the basic inverter is typically limited to about 20 dB. Moreover, in order to achieve saturation for both the pull-up and pull-down devices at the same time, a large supply voltage is required.



Figure 92. a) Measured transfer characteristic of the PLS inverter and b) estimation of the gain. The forward characteristic is represented with a continuous line, the backward one with a dashed line.

Thanks to the positive feedback, the gain of the PLS inverter increases dramatically. Fig. 92a shows the measured forward and backward transfer characteristics of the PLS inverter, while Fig. 92b focuses on the transition region, showing a maximum gain of about 76 dB. This value is limited by the 200 μ V resolution of the voltage source used at the input; still, to the best of our knowledge, it is more than 26 dB larger than any other organic inverter on plastic foil reported in literature, even if the best previous result exploits ultra-thin dielectric layers (and thus has potentially a larger transconductance and a better output resistance, due to the better electrostatic control that the gate has on the channel) [10].

Noise margin

The transfer characteristic of the PLS inverter has a very symmetric shape and high gain (Fig. 92). Therefore, a good noise margin is expected. Considering, in line with Section 5.3, the Maximum Equal Criterion (MEC) in the case of a static characteristic with hysteresis, the noise margin will be given by the side of the largest square that can be inscribed between the forward characteristic and the mirrored backward one. Indeed when the output is high, an unexpected noise source should overcome the backward threshold to cause an error; while when the output is low, the noise should overcome the forward threshold.



Figure 93. Transfer characteristic and MEC noise margin evaluation for the PLS inverter a) in Fig. 87a and b) in Fig. 87b. The noise margin is respectively 8.2 V and 10.3 V. The insets illustrate the width of the hysteresis loop.

For this reason, a clockwise hysteresis is not detrimental for the noise margin, but actually beneficial [99], [100], [101]. In Fig. 93, the noise margins for the two PLS schematics of Fig. 87 are shown. For the first PLS topology (Fig. 87a) the noise margin is 8.2 V, while the embodiment with higher gain and larger hysteresis (Fig. 87b) reaches a noise margin equal to 10.3 V (which is even larger than half the supply). However, if the process variations affecting many different gates are condidered, increasing the width of the hysteresis loop reduces the allowed random shift of the characteristic to less than half the difference between the supply V_{DD} and the width of the loop. Hence the probability of soft faults, over a large number of digital gates, increases.

The proposed PLS inverter enables outstanding static performance in case of nominal process parameters and supply conditions. Nevertheless, organic technologies suffer from strong process parameter variations and ageing, and the supply voltage, which can be generated in RFID tags by a rectifier connected to an antenna, can also vary. One of the most important features of the PLS inverter is its tunability, which can effectively counteract all these potential problems.



Figure 94. PLS inverter supplied at V_{DD} = 5 V, 10 V, 20 V. The control voltage V_{tr} was biased respectively at V_{tr} = 0 V, 10 V, 20 V.

This flexibility of the PLS design also allows the very same inverter to be functional for a large range of supply voltages. Figure 94 shows the transfer characteristics of a PLS inverter measured for three different supply voltages, $V_{DD} = 5 V$, 10 V, 20 V. In all three cases the tuning voltage V_{tr} was kept within the supply range and was set respectively to $V_{tr} = 0 V$, 10 V and 20 V. Even at 5 V supply (which is extremely small for unipolar logic on foil using conventional dielectric layers) the measured PLS inverter still has a noise margin of about 100 mV.

Statistical inverter characterization

After the characterization of the single device, we can move further and analyze the data measured on 288 PLS and 288 Zero-Vgs inverters.



Figure 95. Histograms of trip point and noise margin distributions of 288 PLS inverters measured on the same plastic foil applying the same tuning voltage to all inverters. Two different tuning voltages are shown: $V_{tr} = 10 V$, 20 V.

The measured data show that all the 288 PLS inverters are functional and can be tuned, choosing V_{tr} individually, to achieve a minimum noise margin of 5.8 V. Two of the 288 Zero-Vgs inverters instead switch for an input voltage around 25 V (for V_{DD} = 20 V), but in this case no voltage control is available to deal with the excessive TFT variability and the soft faults cannot be corrected. The histograms of Fig. 95 show the distributions of trip point and noise margin measured on the PLS inverters for two different values of the tuning voltage, namely V_{tr} = 10 V and 20 V. Applying the nominal bias V_{tr} = 10 V, only 207 inverters show a positive noise margin. Indeed, due to ageing and process parameters variation, the average switching point measured for V_{tr} = 10 V is around 17 V instead of half the supply. A large improvement is achieved applying a higher tuning voltage: indeed, forcing V_{tr} = V_{DD}, 285 working inverters have been measured. The switching point of the remaining three inverters was shifted for V_{tr} = V_{DD} to negative input voltages, but these inverters work correctly with a lower V_{tr}.



Figure 96. a) Histograms of measured trip point (inset) and noise margin distribution of 288 PLS and Zero-Vgs inverters measured on the same plastic foil. For the PLS inverters, the tuning voltage has been chosen suitably for each group of 18 inverters. b) Yield evaluation based on the measured average and standard deviation of the noise margin (Fig. 96a) for PLS (continuous line) and for Zero-Vgs (dashed line) inverters.

This result shows that a single control voltage is not enough, in our technology, to effectively cope with parameter variations on the entire foil. However a smaller area is likely to be affected by smaller absolute variations, hence the control voltage was also applied separately to each of the sixteen groups of inverters (Fig. 89). The histograms of noise margin and trip point (inset) evaluated in this way are compared with the Zero-Vgs ones in Fig. 96a. Due to the smaller parameter variations within the same group, the majority of the trip points for the PLS inverters is very close to average value $V_{DD}/2$ with a great benefit for the yield.

The average noise margin and its standard deviation can also be used to evaluate the yield of a digital circuit as a function of the number of digital gates in use. As a first-order approximation, it is neglected the effect of the hard faults caused by defects in the TFTs and the interconnections, and it is assumed that the yield is the probability that all gates in digital circuits have a positive noise margin. Following the approach used in [102], [103] a Gaussian probability distribution can be assumed for the noise margin of all the inverters and thus the yield of a digital circuit of an arbitrary number N of inverters can be estimated based on the average and standard deviation of the measured noise margin. Following this approach, the forecasted yield is plotted in Fig. 96b as a function of N. The average and standard deviations of the noise margin are obtained from Fig. 96a, both for Zero-Vgs and for PLS inverters. For the latter inverter thus, the case in which the tuning voltage is separately optimized per group of inverters is considered.

To give an example, aiming at a 90% yield from a digital circuit exploiting the Zero-Vgs logic can be found, from the intersection with the dashed line (average noise margin μ_{0Vgs} = 2.58 V, standard deviation σ_{0Vgs} = 0.8 V), that the number of inverters in the circuit must be smaller than 200. On the other hand, considering the PLS logic (continuous line - average noise margin μ_{PLS} = 6.82 V, standard deviation σ_{PLS} = 1.18 V), a maximum of N ~ 24 million inverters can be employed. Of course these figures overestimate the actual yield as they do not take into account the yield loss due to hard faults, since, due to the rather small sample size, no hard faults were detected.



Figure 97. Photographs of the measured a) PLS inverter and of the b) Zero-Vgs inverter.

However, assuming that the probability of hard faults is proportional to the area occupied by the digital circuit, the PLS inverter would provide an improvement on the Zero-Vgs one also from this perspective, as it occupies only 66,150 μ m², against the 77,775 μ m² of the Zero-Vgs one (Fig. 97). The Zero-Vgs inverter indeed adopts a much wider output device, since this is the only way to make the static transfer characteristic more symmetric. In the PLS inverter, the symmetry is provided by the level shifter and the output load can be dimensioned only considering the output logic levels. Moreover, the dynamic behavior of the PLS inverter is not negatively affected; indeed the rise time is negligible with respect to the fall time, and the fall time is independent of the load width. In fact, most of the parasitic capacitance is determined by the load transistor (which is Zero-Vgs connected and very wide); hence, the pull-down current and the capacitive load are both proportional to the width of the pull-down transistor. The comparison between Zero-Vgs and PLS logic proves that our circuit approach dramatically improves the yield of digital circuits, decreasing the number of soft faults, and enables functional circuits on foil with an unprecedented transistor count. These outstanding achievements can be obtained with a per-group trip point control approach that represents a low-cost solution providing significant yield improvement at the cost of little additional complexity.

Digital building blocks and circuits

The PLS logic style was applied to the basic digital building blocks required to design more complex functions. Ring oscillators have been measured to investigate the speed of the logic and data flip flops (DFF) have been designed to demonstrate a functional 240-stage shift register. However, a NAND gate is required to implement all these digital functions. For this reason, a 2-input NAND gate was also designed following the same approach used for the inverter. The schematic of the PLS NAND gate is shown, in Fig. 98, together with its transfer characteristic measured keeping the B input to V_{DD} .



Figure 98. Schematic of a NAND gate in PLS logic. The n-type-only counterpart would employ the devices M3A and M3B in series.

Ring oscillators

In order to evaluate the dynamic performance of the PLS inverter, different ring oscillators were designed. Figure 99 shows a picture of a 9-stage ring oscillator exploiting PLS inverters plus an output inverter and a buffer helpful to drive the measurement setup.



Figure 99. Photograph of a 9-stage ring oscillator.

The plot of Fig. 100a shows the time behavior of a 15-stage ring oscillator output. The measured inverter delay was $T_d \sim 45 \ \mu s$ which is comparable with the fastest Zero-Vgs inverter reported in [74]: indeed in both cases the delay is dominated by the weak pull-down action of the output stage.



Figure 100. Measured output of different ring oscillators: a) a 15-stage ring oscillator, b) a ring oscillator supplied by different voltages V_{DD} = 20 V, 10 V, 8 V (after six months shelf-life), and c) a ring oscillator biased by different control voltages V_{tr} (inset).

PLS inverters can add more functionality to a simple ring oscillator. Indeed, the presence of a tunable trip-point guarantees the functionality of the circuit even with reduced supply voltages. Figure 100b shows the plot of the output voltage of a ring oscillator measured at different supply voltages, between 8 V and 20 V. Moreover, the tunable trip point allows to implement a VCO [75]. In Fig. 100c the output frequency is varied from 300 Hz to 560 Hz tuning the control voltage $V_{\rm tr}$.

The three measurements shown in Fig. 100 reveal a different average delay for the inverters in the ring oscillator. For instance, the average inverter delay, observed during the measurement of the ring oscillator in Fig. 100b, was about $660 \,\mu$ s. This delay is more than one order of magnitude larger than the one observed in Fig. 100a. Such a big difference in speed is not due to the process variability, but depends on the ageing of the semiconductor. Indeed the ring oscillator of Fig. 100a was measured right after its realization, while the one in Fig. 100b was measured after the samples were kept for more than 6 months on a shelf. Aging was also confirmed by mobility measurements on test devices: after a few months mobility was found to be more than two orders of magnitude smaller.

Data Flip Flop

The Data Flip Flop (DFF) is an important building block since it can be used as a storage element in sequential logic, it can be employed as a delay element in digital filters, it can be used to synchronize asynchronous data, etc.



Figure 101. Schematic of a synchronous DFF.

In our case, the DFF is used to build a 240-stage shift register. Our synchronous data flip flop includes 6 NAND gates and one inverter, for a total of 52 OTFTs using the PLS style (Fig. 101).

Shift Register

In order to demonstrate the actual improvement of the yield with a large functional circuit, a 240-stage shift register was designed using the PLS logic style. This circuit employs 13,440 p-type OTFTs achieving (to our knowledge) the largest transistor count ever demonstrated in a functional organic circuit. Our circuit features almost four times more p-type OTFTs than the microprocessor discussed in [27], which has been fabricated in the same technology.



240-stage Shift Register 10-DFF Module

Figure 102. Photographs a) of the 240-stage shift register and b) of the 10-DFF module.

The photographs of the full 240-stage shift register and of a 10-stage module are shown in Fig. 102a and Fig. 102b respectively. The shift register occupies an area of about 26 mm x 26 mm including 384 pads to allow the measurement of the output of each stage. One additional output buffer is included at the output of each DFF in order to avoid excessive load due to the measurement setup. The shift register is divided in 4 blocks, each containing six 10-stage modules.

Figure 103a represents the input (red) and output (green) of one 60-stage shift register block at 70 Hz. On the other hand, Fig. 103b shows the measurement at 30 Hz of all four blocks building the 240-stage shift register. Due to the presence of a buffer, the output swings between 7 V and 17.5 V. For the first measurement, the trip point control was set at $V_{tr} = 16.5$ V and a digital input pulse was provided every 100 periods of a 70 Hz clock.



Figure 103. a) Measured output after 60 stages at 70 Hz. b)Measurements of all the four blocks building the shift register. The four plots show the output signals respectively of the 60th, 120th, 180th, 240th stages. In both cases, the reduced swing of the output data is due to the buffer included to drive the measurement setup.

8.1 The proposed Positive-feedback Level Shifter logic

The control voltage V_{tr} was then varied to investigate the voltage range and the accuracy that would be required by a control circuit able to provide automatic tuning of the trip point for maximum yield. For the measured foil, the full shift register was functional, at 30 Hz, for V_{tr} changing from 14 V to 20 V. For instance the four plots in Fig. 103b show the input and the output signals for all the four 60-stage blocks of the same 240-stage shift register when the bias is V_{tr} = 18 V and the clock runs at 30 Hz frequency.

The current drained from the 240-stage shift register supply is almost independent of the control V_{tr} applied to the shift register and amounts to about 400 μ A.

8.2 Conclusions

Digital circuits are always present in integrated circuits either to implement digital functions or to serve other purposes. In this chapter, was discussed the design of a digital logic style suitable for three metal layers unipolar TFT technologies.

The proposed logic style achieves outstanding results with respect to the most common problems shown by large-area technologies manufactured at low temperatures. Indeed, the general aims of high gain and symmetric transfer characteristic are very difficult to reach when using these technologies even disregarding process variations and aging effects; and providing all the logic gates required by a functional circuit with a sufficient noise margin easily becomes a prohibitive task in actual prototypes.

The proposed logic style achieves the largest gain reported in literature using TFTs on film, exploiting positive feedback to overcome the low intrinsic gain of organic transistors. Moreover, to cope with the strong process variations that characterize TFT technologies on foil, a control voltage is included to tune the static characteristic of the logic gates. We firmly believe that no logic style will allow a widespread use of smart circuits on plastic foils, if such kind of control will not be available. Moreover, the needed control voltage is kept, with the proposed PLS logic style, within the supply rails.

The statistical behavior of 288 PLS inverters was compared to the one of the same number of Zero-Vgs inverters manufactured in the same area. Using the control voltage, it was possible to measure a noise margin larger than 5 V for all the PLS inverters under test (for $V_{DD} = 20$ V). Aiming at a soft yield of 90%, the better noise margin leads to an improvement in the achievable circuit complexity, which goes from 200 TFTs when using Zero-Vgs inverters to about 24 million TFTs when using PLS inverters (and adjusting the tuning voltage per group of inverters on a $4 \times 26 \text{ mm}^2$ area).

In order to prove the actual yield improvement in a functional circuit, a 240-stage shift register was also designed. The fully functional circuit exploits over 13,440 TFTs, which is the highest complexity ever reached in organic electronics on foil to our knowledge.

These remarkable results to our opinion can pave the way to a widespread use of large-area electronics in more and more complex applications.

9 Conclusions

This thesis illustrates innovative contributions to the design of electronic circuits for large area and low cost applications. This sort of applications is enabled by a cheap, low temperature process to manufacture electronics on flexible substrates. Unfortunately this kind of process only offers TFTs with electrical performance far below the silicon standards, and enables only poor uniformity and reliability. For these reasons, state of the art circuit designs based on these technologies are still at their infancy and only first steps have been moved towards of the implementation of complex analog functions, the accurate conversion of analog signals to the digital domain, and the creation of large digital circuits with satisfactory yield.

With this work, we demonstrate that all these important aspects can be substantially improved while exploiting the same technologies used so far. Technology-aware solutions have been found facing the technology issues from the architectural, circuital, layout and device points of view.

Concerning analog circuit functions the following conclusions can be drawn:

- 1. Circuit simplicity should be pursued to avoid strict bias constraints, and to achieve sufficient yield despite the large process parameters variability.
- 2. Exploiting suitable topologies, circuit performance should be disentangled as much as possible from absolute parameter values, as it has been done in this work for the gain of the tunable transconductor and of the parametric amplifier.
- 3. An additional control can be a simple but very effective solution to tune some key performance to the wanted target in spite of process variations, e.g. the cut-off frequency in a G_mC filter presented in Chapter 6.

In order to design circuits for data conversion with better linearity:

- 1. Careful layout in DACs, to cancel where possible gradient effects, should be pursued. With respect to matching properties, increasing the unity cell area must be done carefully, as it can soon be detrimental due to high probability of hard faults typical of these processes.
- 2. A rational choice should prefer converter architectures where the amplifier and comparator offsets do not affect the linearity, as successive approximation register (SAR) and integrating ADCs.
- 3. ADC topologies based on matching should be avoided, since matching is obviously one of the weakest points of large-area electronics. In case matching is exploited, rely on matching of passives (eg. resistors, capacitors) or exploit TFTs manufactured with amorphous semiconductors like GIZO. TFTs based on nano-crystalline semiconductors like pentacene should be avoided.
- 4. Integrating architectures can drastically improve linearity and, at the same time, reduce area and power consumption, especially when integration is performed in the digital domain. Compact area is beneficial also for resilience to hard/soft faults.

Digital circuits play a very important role in any integrated circuits, and the same will be the case for the large-area low-cost applications we target in this work. About digital circuits:

- 1. Noise margin is the key figure of merit to be improved. Wafer-to-wafer variability, mismatch, bias stress, aging are not fully characterized yet, but still represent the major hurdle for (digital) circuit design. Noise margin should be robust against all these factors.
- 2. A symmetric input-output characteristic is mandatory to achieve acceptable noise margin, and a trip-point control can make the difference with respect to the yield of a logic style. An effective trip-point control using voltages within the power supply can allow self-calibration solutions.
- 3. Positive feedback has been shown as a viable way to provide a robust logic style improving voltage gain.

Following these guidelines, relatively complex circuits can be designed with an acceptable confidence on robustness even quantitative data on matching and statistical process veriations are not provided along with the technology.

Also investigations around innovative device designs can result in better performance. To this extent, a parametric capacitor was designed to be used in a discrete-time amplifier, which provides a voltage gain comparable to continuous-time solutions in the same technologies, but achieves faster response.

This work proves the feasibility of complex circuit designs with large-area electronics and shows the sustainability of unipolar technologies (especially if featuring double-gate) against complementary ones in the prospective of addressing low-cost applications.

Appendix

The additional presence of the transistor M5 to the simple current mirror schematic of Fig. 35, adds to the drain of M4 a signal which depends on the input voltage. In order to evaluate the effect of this small-signal to the output current, M4 can be considered as a resistive $(1/g_{m,4})$ source degeneration of M5. The voltage drop on this resistor can be expressed as:

$$v_d = v_{in} \frac{1/g_{m,4}}{1/g_{m,4} + 1/g_{m,5}} = v_{in} \frac{g_{m,5}}{g_{m,4} + g_{m,5}} = Sv_{in}.$$

If we define

$$A = \frac{W_3}{L_3} \beta \gamma (V_G - V_S - V_{FB})^{\gamma - 1} \text{ and } B = \frac{W_3}{L_3} \beta \gamma (V_G - V_D - V_{FB})^{\gamma - 1},$$

still considering that $V_S = V_{S,3} = V_{S,4}$, $V_G = V_{G,3} = V_{G,4}$ and $V_D = V_{D,4}$, Eq. (32) and Eq. (33) can be expressed as:

$$\begin{split} i_{in} &= \frac{\delta I_{DS}}{\delta V_{GS}} v_{gs} + \frac{\delta I_{DS}}{\delta V_{DS}} v_{ds} = A v_{in} \quad \text{and} \\ i_{out} &= \frac{\delta I_{DS}}{\delta V_{GS}} v_{gs} + \frac{\delta I_{DS}}{\delta V_{DS}} v_{ds} = A v_{in} - B v_{in} + B S v_{in}. \end{split}$$

From the ratio between these two currents, $T_{\rm M5}$ can be obtained as:

$$T_{M5} = \frac{Av_{in} - Bv_{in} + BSv_{in}}{Av_{in}} = 1 - \frac{B}{A}(1 - S) = 1 - \frac{B}{A}\left(1 - \frac{g_{m,5}}{g_{m,4} + g_{m,5}}\right) = 1 - \frac{B}{A}\left(\frac{g_{m,4} - g_{m,5}}{g_{m,4} + g_{m,5}}\right) = 1 - \frac{1}{1 + \frac{g_{m,5}}{g_{m,4}}} \left(\frac{V_G - V_D - V_{FB}}{V_G - V_S - V_{FB}}\right)^{\gamma - 1}$$

which is Eq. (36).

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Acknowledgments

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List of Publications

Journal articles:

- 1. D. Raiteri, P. v. Lieshout, A. v. Roermund and E. Cantatore, "Positive-Feedback Level Shifter Logic for Large-Area Electronics," *IEEE Journal of Solid-State Circuits,* vol. 49, no. 2, pp. 524-535, 2014.
- 2. W.S.C. Roelofs, S.G.J. Mathijssen, J.C. Bijleveld, D. Raiteri, T.C.T. Geuns, M. Kemerink, E. Cantatore, R.A.J. Janssen, D.M. de Leeuw, "Fast ambipolar integrated circuits with poly(diketopyrrolopyrrole-terthiophene)," in *Applied Physics Letters*, vol. 98, no. 20, p. 203301, 2011.
- 3. D. Raiteri, A. H. M. van Roermund, E. Cantatore, "A Discrete-Time Amplifier based on Thin-Film Trans-Capacitors for Sensor Systems on Foil," *submitted to Microelectronics Journal.*
- 4. F. Torricelli, L. Colalongo, D. Raiteri, Z. Kovacs-Vajna, "Field-Induced Contact Organic Field-Effect Transistor," *submitted to Nature*.

Proceedings and conference contributions:

- 5. D. Raiteri, A. H. M. van Roermund, E. Cantatore, "A Discrete-Time Amplifier Based on Thin-Film Trans-Capacitors for Organic Sensor Frontends," in *IEEE International Workshop on Advances in Sensors and Interfaces*, 2013.
- 6. D. Raiteri, P. van Lieshout, A. H. M. van Roermund, E. Cantatore, "An organic VCO-based ADC for quasi-static signals achieving 1LSB INL at 6b resolution," in *IEEE International Solid-State Circuits Conference*, 2013, pp. 108-109.
- 7. D. Raiteri, F. Torricelli, P. van Lieshout, A. H. M. van Roermund, E. Cantatore, "A Synchronous rail-to-rail latched comparator based on double-gate organic thin-film-transistors," in *IEEE European Solid-State Circuits Conference*, 2012, pp. 141-144.
- 8. D. Raiteri, F. Torricelli, K. Myny, M. Nag, B. v. d. Putten, E. Smits, S. Steudel, K. Tempelaars, A. Tripathi, G. Gelinck, A. v. Roermund and E. Cantatore, "A 6b 10MS/s current-steering DAC manufactured with amorphous Gallium-Indium-Zinc-Oxide TFTs achieving SFDR > 30dB up to 300kHz," in *IEEE International Solid-State Circuits Conference*, 2012, pp. 314-316.
- 9. D. Raiteri, F. Torricelli, E. Cantatore, A. H. M. van Roermund, "A tunable transconductor for analog amplification and filtering based on double-gate organic TFTs," in *IEEE European Solid-State Circuits Conference*, 2011, pp. 415-418.

Patent applications:

- 10. F. Torricelli and D. Raiteri, "Ambipolar transistor device and method of operating the device," European Patent 13186901.8 1552, Oct. 1, 2013.
- 11. F. Torricelli and D. Raiteri, "Transistor device and method of manufacturing such a device," European Patent 13186889.5 1552, Oct. 1, 2013.

Other contributions:

- 12. D. Raiteri, S. Abdinia, A.H.M. van Roermund, E. Cantatore, "Analog and mixed-signal circuits for smart sensors on plastic foils," in *ICT.OPEN 2012*.
- 13. D. Raiteri, F. Torricelli, A.H.M. van Roermund, E. Cantatore, "Design of a voltage-controlled oscillator based on organic TFTs," in *International Conference on Organic Electronics*, 2012.
- 14. D. Raiteri, E. Cantatore, A. H. M. van Roermund, "A digital buffer for AC measurements of unipolar organic TFT circuits with microprobes," in *ICT.OPEN*, 2011.
- 15. F. Torricelli, D. Raiteri, L. Milani, L. Colalongo, Z.M. Kovacs-Vajna, P.J.G. van Lieshout, E. van Veenendaal, K. Myny, J. Genoe, G.H. Gelinck, E. Cantatore, "Quantitative physical analysis of gate-insulator/organic-semiconductor interaction and its impact on the OTFT performance," in *International Conference on Organic Electronics*, 2012.
- 16. S. Abdinia, D. Raiteri, S. Jacob, R. Coppard, P. van Lieshout, G. Palmisano, A. Scuderi, A.H.M. van Roermund, E. Cantatore, "Analog-to-digital converters on plastic foils," in *International Conference on IC Design and Technology*, 2013.
- 17. M. Zanuso, S. Levantino, D. Tasca, D. Raiteri, C. Samori, A. L. Lacaita, "A glitch-corrector circuit for low-spur ADPLLs," in *IEEE International Conference on Electronics, Circuits, and Systems,* 2009, pp. 595-598.

Summary

The research activity reported in this thesis concerns many aspect related to the design of smart sensors manufactured on plastic foils. Two technologies have been used for the design of analog, digital, and mixed-signal circuits: one is an organic p-type-only three-metal-layers technology featuring double gate TFTs; the other is a metal-oxide n-type TFT technology exploiting a semiconductor which provides relatively high mobility and good uniformity.

In both cases, a deep characterization of the technology was required, together with the implementation of a suitable design flow in a CAD design environment (Chapter 3). The design rules provided by our technology providers were implemented in a CAD and used to design, at first, characterization masks. Many devices with various channel lengths and widths were taped out, allowing the measurement of a data set sufficient for the complete characterization of a physical model of the DC currents (Chapter 4).

This model was described in Verilog-A language to enable simulations within the design framework, and used to design the circuits required by smart sensors. In particular, we focused on the design of analog circuits for signal filtering and amplification, on mixed-signal circuits for data conversion (analog-to-digital and digital-to-analog converters), and on a new logic style to make digital circuits more reliable.

The keystone to understand the circuit design challenges is the nature of the technology process in use. Indeed, TFT technologies on foil suffer from large process parameter variations, large mismatch, relevant hard fault probability, bias stress and aging. The set of devices is typically limited to a single transistor device (either p- or n-type) and capacitors. To complicate the design of reliable circuit even more, transistors exhibit low mobility (three orders of magnitude less than silicon) and low intrinsic gain, making operational amplifiers very difficult to implement.

For this reason, many known circuit topologies are not suitable for the implementation of circuit functions on a flexible substrate. In Chapter 5, we explain our architectural choices to design a smart sensor on foil, including analog and digital processing, and data conversion.

In the framework of analog signal conditioning (Chapter 6), was designed a tunable transconductor (*IEEE ESSCIRC 2011* [29]) suitable for G_mC filtering that provides an additional control to electrically tune the cut-off frequency of the filter over one decade or to effectively counteract process parameter variations. In order to identify the best solution for analog signal amplification, were designed a simple differential amplifier and a discrete time amplifier based on a new device which provides parametric amplification (*IEEE IWASI 2013* [30]). The measurement of a number of simple differential amplifiers helped pointing out the issues related to mismatch and variability.

After amplification and filtering, the analog signal must be converted to the digital domain (Chapter 7). The first mixed-signal circuit presented in Chapter 7 is a synchronous latched comparator (*IEEE ESSCIRC 2012* [32]). This basic block, needed in most ADC architectures, exploits the double-gate feature of our technology to drastically reduce the input and the output capacitive loads, with great benefits on the comparison speed. Then, is show the design of a digital-to-analog converter (*IEEE ISSCC 2012* [33]) manufactured in a technology providing higher semiconductor mobility and better uniformity than the one used for the other circuits designs. Finally, is demonstrated an analog-to-digital converter (*IEEE ISSCC 2013* [34]) based on an

integrating approach in the digital domain, which achieves robustness together with state of the art SNR and linearity in a compact and simple circuit.

Digital circuits are fundamental for several other functions on chip, including analog-to-digital conversion. In Chapter 8, a new logic style (*IEEE JSSC* [37]) is developed which provides much larger yield compared to the state of the art technologies. This was possible designing logic gates with extremely high gain, and providing an additional voltage control to adjust the symmetry of the transfer characteristic.

The limitations of technologies integrating circuits on foils have also been tackled from a device prospective. This effort led e.g. to the design of a parametric amplifier (Chapter 6), and to two patents on novel TFTs architectures [38], [39]. The related publications are in the pipeline [104].

This work demonstrates the feasibility of integrated circuits on plastic foils achieving adequate performance to enable low-cost smart-sensor applications with acceptable yield: this in spite of the many limitations posed by low-temperature processes on foil, with their variability and poor electrical performance. These technology challenges were overcome using a holistic approach and finding solutions at architectural, circuital, layout, and device level.

Curriculum Vitae

Daniele Raiteri was born on September 24th, 1984 in Milan, Italy.

After completing high school at the "Liceo Scientifico Albert Einstein" in 2003 in Milan, he studied electrical engineering at Politecnico di Milano University, Milan, Italy. In 2009, he received his Master's degree cum laude and moved to the Netherlands to pursue a Doctoral degree at Eindhoven University of Technology.

Since his Master's, his main interest focused on microelectronic circuit design. During his Master's project, he worked on an All-Digital Phase Lock Loop (AD-PLL): an integrated circuit for frequency synthesis which replaces all analog blocks in the loop with digital ones. The studied PLL targeted WiMAX specifications and was realized in a 90 nm CMOS technology. More specifically, he developed a new theory on the effects of quantization on the output phase power spectrum in counter-assisted AD-PLLs. The analytic model he developed relates amplitude and frequency of the limit cycles to the resolution of the digital blocks (digital filter, phase detector and digitally controlled oscillator) and to the thermal noise affecting the analog ones.

During his PhD, he focused on the design of analog, digital and mixed-signal circuits for largearea electronics manufactured on plastic foils using organic and metal-oxide TFTs. The results of his effort on this topic are described in this dissertation.