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Citation for published version (APA):

Gilardi, G., Yao, W., Rabbani Haghghi, H., Leijtens, X. J. M., Smit, M. K., & Wale, M. J. (2014). Deep trenches for thermal crosstalk reduction in InP-based photonic integrated circuits. *Journal of Lightwave Technology*, 32(24), 4262-4268. <https://doi.org/10.1109/JLT.2014.2366781>

DOI:

[10.1109/JLT.2014.2366781](https://doi.org/10.1109/JLT.2014.2366781)

Document status and date:

Published: 01/01/2014

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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Deep Trenches for Thermal Crosstalk Reduction in InP-Based Photonic Integrated Circuits

Giovanni Gilardi, Weiming Yao, Hadi Rabbani Haghighi, Xaveer J. M. Leijtens, Meint K. Smit, *Fellow, IEEE*, and M. J. Wale, *Member, IEEE, OSA*

Abstract—We numerically and experimentally investigate an on-chip solution to reduce the thermal crosstalk in indium phosphide-based photonic integrated circuits. We introduce deep trenches, fabricated through wet etch, between active and passive components. The current injected in active components and the geometry of the trenches are the parameters considered in our analysis. The trenches thermally isolate the passive components from the heat generated by active components. The thermal crosstalk is quantified by measuring the effects on the electro-optical response of an MZ modulator considered as a test structure. The heat sources are represented by semiconductor optical amplifiers placed at different distances with respect to the position of the MZ. Our experiments show how both the geometry and the position of the trenches, play a role in the reduction of the thermal crosstalk.

Index Terms—Crosstalk, indium compounds, thermo-optic effects.

I. INTRODUCTION

SINCE the introduction of the Arrayed Waveguide Grating (AWG) in 1988 [1] the complexity of Indium Phosphide (InP) chips has increased exponentially from a few to a few hundred components. Significant progress in the development of complexity in photonic integrated circuits (PIC) was reported with the introduction of WDM receivers in 1993 [2] and 1996 [3], WDM lasers in 1994 [4] and 1996 [5] and more complex WDM receivers in 2004 from ThreeFive Photonics [6] and transmitters 2005 from Infinera [7]. The most complex PIC reported so far is a PM-DQPSK transmitter [8].

However, the present technology cannot ensure a further major increase in chip complexity. In passive devices the unavoidable losses of the passive components limit the total number of components that can be cascaded, while in active PICs the number of Semiconductor Optical Amplifiers (SOA) is typically restricted up to a maximum of a few hundreds, because of heat sinking limitations.

Chip designers always try to reduce the chip size. The aims are to increase the circuit functionality for a fixed chip size and to reduce the necessary chip area allocated for a specific design, since this directly affects the chip costs. Within the

building block approach [9], [10], where the performance of a specific component (i.e. basic building block, such as phase shifter, AWG, MMI, SOA) is well known and optimized for specific geometries, the main approach to reduce the chip size is the reduction of the distance between components.

However, the distance between the building blocks cannot be freely reduced because the components interact with each other. The interactions between components are commonly identified with the term *crosstalk*.

The crosstalk limits the maximum component density achievable in a single chip. The most critical crosstalk contributions in a PIC are the radiofrequency crosstalk, mostly related to the inductive and capacitive coupling of RF signals; the optical crosstalk, related to the light scattering and then light coupling between nearest waveguides; and the thermal crosstalk, due to the heat transfer from active components, i.e. SOA, to passive components, i.e. phase modulators, AWG, and so on. This paper is focused on the thermal crosstalk in InP based PICs.

The literature offers both theoretical and experimental [11]–[13] investigations of thermal crosstalk in an array of lasers and also thermal crosstalk interaction between active and passive components [14], but a few technological solutions have been proposed so far to reduce the thermal crosstalk.

In practical applications the most common approach used to avoid the effects of the thermal crosstalk is based on the introduction of design rules related to the definition of a minimum distance between components. To increase the distance between components is a conservative solution but it is not a solution to increase the PIC density.

A technique to reduce the thermal effects, consists in the fabrication of a dummy SOA close to the main SOA to maintain a constant sum of the injected current in both SOAs. The effect is to have the temperature around the SOAs area constant. This approach does not improve the miniaturization of the PIC since the dummy SOA requires a specific chip area for its definition and moreover the dummy SOA dissipates power without adding functionality. The introduction of conductive shunts to improve the thermal dissipation has been reported in [15]. In [16] an approach to eliminate the temperature sensitivity of Mach-Zehnder (MZ) modulators is investigated by adjusting the thermo-optic effects of their interfering arms through their waveguide width and length optimization. Liquid Crystals, that are mainly implemented to develop electrically tunable device [17]–[19], are also emerging for temperature stabilization in photonic circuits [20], [21].

A powerful approach to reduce the heat transfer from active components is based on the definition of trench structures.

Manuscript received July 28, 2014; revised September 25, 2014; accepted October 30, 2014. Date of publication November 7, 2014; date of current version November 25, 2014.

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Digital Object Identifier 10.1109/JLT.2014.2366781

A few cases of structures including trenches are reported in silicon based PICs [22] and in polymer waveguides [23] where the thermo-optic effect is enabled by including metallic heaters on the chip.

In InP the integration of trenches is new as it represents the core of this paper. The aim of the trenches is to reduce the thermal crosstalk between active and passive components.

In active InP based PICs the thermal crosstalk effects are inherently present when the SOAs are operated. This paper is organized as follows: in Section 2 we describe the model used to evaluate the thermal crosstalk effects in active InP based PICs; the model is applied to a test structure reported in Section 3 to simulate the thermal crosstalk effects; in Section 4 we report the experimental results obtained when no trenches are included in the testing structure. Section 5 shows, the fabrication of the deep trenches via wet etch and the effects of the trenches to the thermal crosstalk.

II. ELECTRO-THERMAL MODEL

To investigate the effect of the thermal crosstalk we have developed a model to analyze the electro-thermal interaction in active components and to evaluate the conductive heat transfer. In our model, first a current is injected into the SOA and the Joule's heating is calculated by considering the electrical and thermal properties of the materials used in the SOA; second the heat transfer from the injected SOA to the rest of the photonic circuit is evaluated by solving the heat transfer equation; third, the local temperature in every relevant point of the PIC is evaluated.

In detail, both the Joule's effect and the heat transfer phenomena are simulated by a 3D finite element method [24]. We simplify the heat transfer equation by neglecting the convective and the radiative heat transfer and considering the steady state regime [25]. The equation governing the pure conductive heat transfer in a solid becomes:

$$C_p \rho \frac{dT}{dt} + \nabla \cdot (-k \nabla T) = Q \quad (1)$$

where the derivative of the temperature with respect to time is zero, k [W/(m · K)] is the thermal conductivity, ρ [kg/m³] is the material density, C_p [J/(kg · K)] is the specific heat capacity at constant pressure, T [K] is the absolute temperature. Q [W/m³] contains the heat sources and it is related to the Joule's effect:

$$Q = \frac{I^2 R}{hcl} \quad (2)$$

Both active and passive waveguides are made by growing several layers of InP with a controlled doping level, as shown in Fig. 1. The aim is to create a refractive index contrast able to confine the light in the core of the waveguide. In (2), R is the total resistance that depends on the resistivity and geometry of the layers passed by the injected current I . For each layer we consider its geometry parameters h (thickness), c (width) and l (length) and its resistivity.

The resistivity of each layer depends on the type of doping, p or n , and on the doping concentration. The doping modifies the heat sources since it modifies the electrical resistivity of the InP.

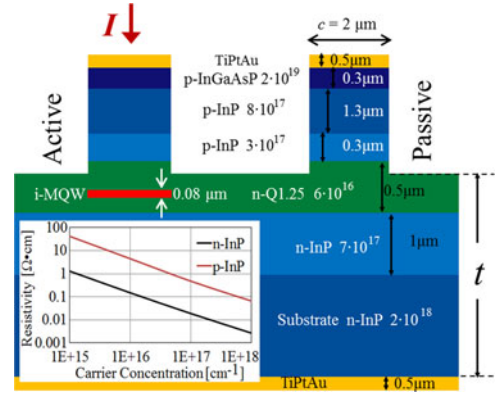


Fig. 1. Shallowly-etched waveguide layer-stack considered for active and passive components. In red is the active region. I is the current injected in the active components. The relation between doping concentration and the resistivity is indicated in the inset.

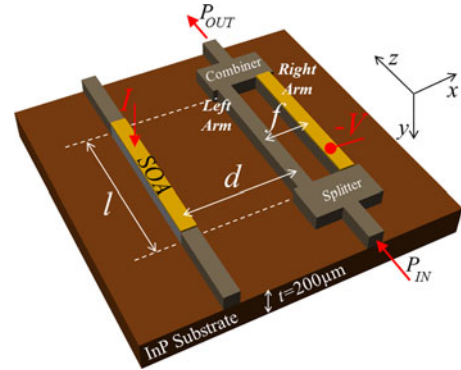


Fig. 2. Photonic integrated circuit considered in our model.

To evaluate the resistivity in relation to the doping, we consider a fitting of the values reported in [26], also reported in the inset of Fig. 1.

III. DEVICE DESCRIPTION AND WORKING PRINCIPLE

To investigate the thermal crosstalk we apply the model developed so far to a test structure based on one SOA and one MZ modulator, as shown in Fig. 2.

The SOA is part of a more complex section of the PIC but it is not related to the MZ. To reduce the number of geometrical variables we consider the same length, l , for the SOA and for the MZ arms. The substrate thickness is $t = 200 \mu\text{m}$. Moreover, we keep the distance between the arms of the modulator fixed: $f = 310 \mu\text{m}$. It is a safe value to avoid both optical [27] and radiofrequency [28] coupling between the arms of the MZ. In principle the reduction of f allows the reduction of the thermal crosstalk effects due to the reduction of temperature mismatch between the left and the right arm. On the other hand the reduction of f also leads to an increase of the optical crosstalk and to an increase of the radiofrequency crosstalk. $f = 310 \mu\text{m}$ allows to neglect the optical and the radiofrequency crosstalk thus avoiding misunderstandings and perhaps wrong interpretation of the results.

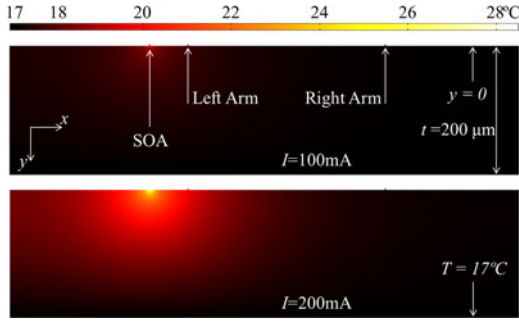


Fig. 3. Heat transfer from the SOA when the injected current is $I = 100$ mA and $I = 200$ mA.

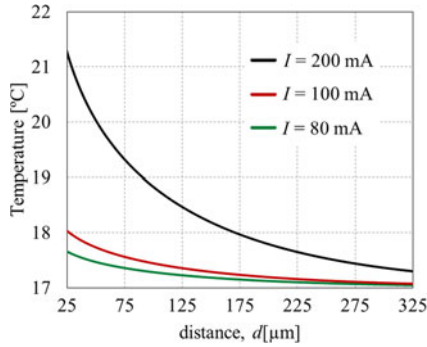


Fig. 4. Temperature distribution along the x -coordinate and $y = 0$.

Fig. 3 shows the heat distribution for two values of injected current and the temperature evaluated for both arms of the MZ. For instance, $I = 200$ mA corresponds to a current density of 10000 A/cm² since the SOA length is $l = 1$ mm while its width is $c = 2$ μ m. A temperature of 17 °C is imposed at the bottom side of the chip by a copper heat sink (not shown in the Figures) whose thermal conductivity (400 [W/(m · K)]) is high enough to clamp the temperature.

By increasing the injected current density up to 200 mA, the temperature of the SOA reaches about 28 °C. The temperature increases with the square of the injected current according with (2), and it is higher in the active region where the electrical resistivity is higher compared with the other layers. Due to the heat transfer, also the temperature in other points of the PIC results higher.

Fig. 4 shows the temperature distribution along the x -coordinate (for $y = 0$) for three values of injected current.

The left and right arms are at a distance d and $d+f$, respectively, from the SOA. With the terms labeled in Fig. 1, the output optical power from the MZ can be expressed as:

$$P_{OUT} = E_0 \cdot E_0^* \quad (3)$$

E_0 is the output electrical field and can be described as:

$$E_0 = \frac{E_{in}}{2} \left[e^{j\frac{2\pi}{\lambda}n_L l} + e^{j\left(\frac{2\pi}{\lambda}n_R l + \Delta\phi(V)\right)} \right] \cdot e^{-\alpha l} \quad (4)$$

α represents the optical losses for the passive waveguides and the measured value is 3 dB/cm. $\Delta\phi(V)$ is the phase shift induced by the reverse DC voltage applied to the right arm. By exploiting

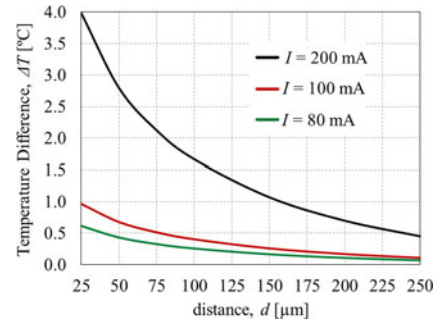


Fig. 5. Temperature difference between the left and right MZ arm versus distance from the SOA evaluated for $f = 310$ μ m and $y = 0$.

the linear electro-optic effect, it can be expressed as:

$$\Delta\phi(V) = \Delta V \frac{\pi}{V_\pi} \quad (5)$$

where ΔV is the voltage variation in the right arm of the modulator and V_π is the voltage necessary to commutate the output power, P_{OUT} , from its maximum to its minimum.

In (4), E_{in} is the field amplitude considered as MZ input, while n_L and n_R are the effective index for the left and right arm, respectively. Both n_L and n_R depend on the temperature as follows:

$$n_L = n_0 + \eta\Delta T_L \quad (6)$$

$$n_R = n_0 + \eta\Delta T_R \quad (7)$$

$n_0 = 3.25$ is the effective refractive index considered for each arm at 17 °C, while ΔT_R and ΔT_L are the temperature variation for the arms with respect to the temperature imposed by the cooling system. The coefficient $\eta = 2.5 \cdot 10^{-4}$ 1/K is the thermo-optical coefficient for the InP [29]. The constructive interference in the combiner occurs when the phase shift in the right arm ($\Delta\phi_R$) equals the phase shift in the left arm ($\Delta\phi_L$):

$$\Delta\phi_L = \Delta\phi_R \quad (8)$$

$$\frac{2\pi}{\lambda}n_0 l + \frac{2\pi}{\lambda}\eta\Delta T_L l = \frac{2\pi}{\lambda}n_0 l + \frac{2\pi}{\lambda}\eta\Delta T_R l + \Delta V \frac{\pi}{V_\pi} \quad (9)$$

by solving (9):

$$\Delta V = \frac{2\eta V_\pi l}{\lambda} (\Delta T_L - \Delta T_R) \quad (10)$$

Equation (10) quantifies the DC MZ switching curve drift due to the temperature difference between the arms. We will refer to this quantity with the term ΔV^i to indicate that it is *induced* by the thermal crosstalk, i.e. it is induced by the difference in temperature between the two arms of the modulator: $\Delta T = \Delta T_L - \Delta T_R$.

Fig. 5 shows the difference in temperature between the two arms as a function of d for three values of injected current. ΔT is always positive because in presence of heat transfer from the SOA, the temperature in the left arm is always higher than the temperature in the right arm.

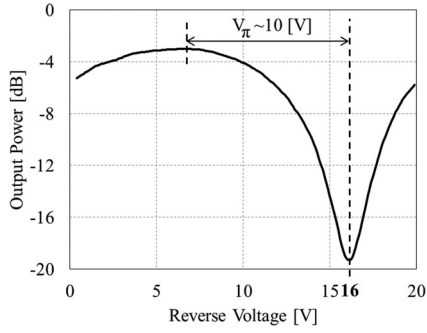


Fig. 6. Measured MZ DC switching curve when $I = 0$ (ground state). The voltage step is 0.1V. The minimum output optical power is for $V = 16$ V.

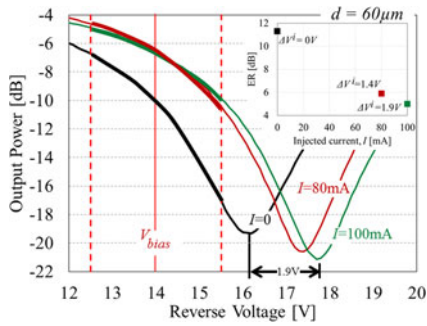


Fig. 7. Measured DC switching curve drift due to heat transfer from the SOAs for $d = 60 \mu\text{m}$. The inset shows the ER drop due to the switching curve drift.

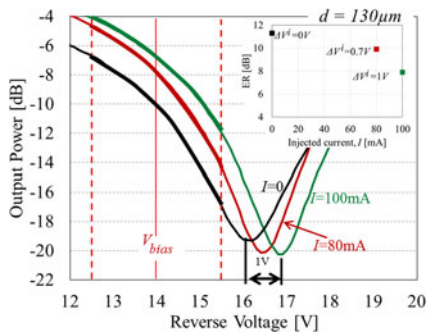


Fig. 8. Measured DC switching curve drift due to heat transfer from the SOAs for $d = 1300 \mu\text{m}$. The inset shows the ER drop due to the switching curve drift.

IV. THERMAL CROSSTALK MEASUREMENT

While no current is injected into the SOA (ground state, $I = 0$ mA), a reverse voltage is applied to the right arm to measure the MZ DC switching curve reported in Fig. 6: it shows a switching voltage (V_{π}) of about 10 V. The voltage step considered in the experiment is 0.1V. The DC switching curve drift is defined with respect to the minimum power *transmission*. It corresponds to $V = 16$ V for the ground state.

Next, the SOA is injected with the current I . According with Fig. 4, the heat transfer from the SOA to the MZ causes the variation of the temperature T_L and T_R , and thus the refractive index changes as formulated in Equations (6) and (7).

The refractive index variation, causes the DC switching curve drift, ΔV^i . Figs. 7 and 8 show the measured switching curve

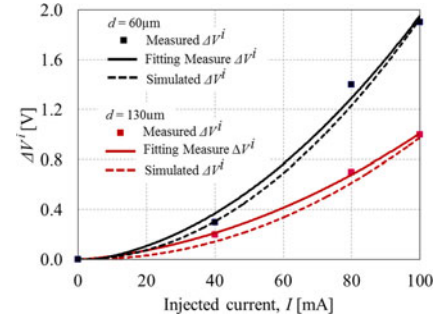


Fig. 9. Measured and simulated DC switching curve voltage drift for $d = 60 \mu\text{m}$ and $d = 130 \mu\text{m}$.

drift due to the thermal effects for $d = 60 \mu\text{m}$ and $d = 130 \mu\text{m}$, respectively.

When MZ is used as fast optical modulator, the switching curve drift limits the performances of the MZ, because it results in the degradation of the optical extinction ratio (ER). The ER is a key parameter in optical communications since the quality of the transmission, i.e. the bit error rate, is strictly related to the ER value. To measure the ER at low frequency (e. g. 1 GHz), we consider a voltage bias of 14 V (red vertical line in Fig. 7 and Fig. 8), while the range of the RF signal is 3V (range represented by the dashed lines). In this condition the measured ER is about 11.3 dB when no current is injected in the SOA.

The inset in Fig. 7 and Fig. 8 show the measured ER values and the corresponding ΔV^i . While the swept of the RF signal is constant, the swept of the optical output power, i.e. the ER, is reduced as showed in the bolder portion of the switching curves.

Fig. 9 summarizes the experiments performed to evaluate ΔV^i , and it also includes the simulated results obtained using the model described in Section II. The simulated curves have been plotted considering $\eta = 2.5 \cdot 10^{-4}$ 1/K, $V_{\pi} = 10$ V, $\lambda = 1.55 \mu\text{m}$, $l = 1000 \mu\text{m}$ in (10).

ΔV^i increases with the square of the injected current: it is inherently related to (2). For particular PIC topologies it is possible to calibrate the circuit with respect the thermal crosstalk effects. For instance for the PIC proposed in Fig. 2 one may consider to tune the bias voltage according with the ΔV^i induced by I , to keep constant the ER. However this solution increases the complexity of the measurement when, in particular, the PIC is crowded and more active and passive components are operated simultaneously. Moreover in complex passive components (i.e. AWGs, Ring Resonators), the thermal effects may lead to non-uniform variation of the refractive index and it cannot be compensated.

V. TRENCHES FABRICATION

We investigate an on-chip solution to overcome the limit in miniaturization imposed by the thermal crosstalk. We define deep trenches between optical components to modify the heat transfer path. The trenches are intended as a deep aperture between the components.

Fig. 10 sketches the basic fabrication steps to define the trenches: (a) SOAs and passive waveguide structures are

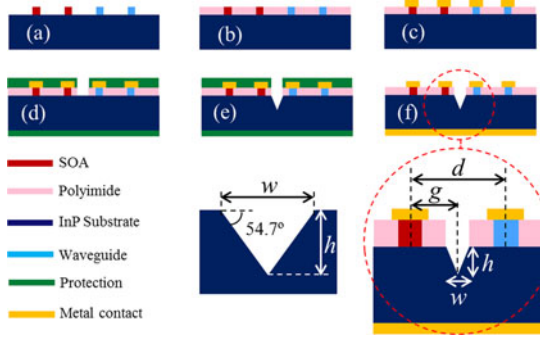


Fig. 10. Process flow to define trenches between active and passive components.

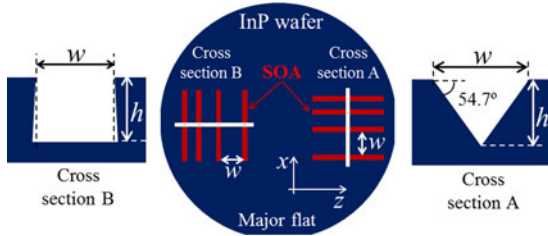


Fig. 11. Trench geometry versus crystallographic orientation.

already defined; (b) a thin layer of polyimide and SiO_2 are used to planarize the structure and to improve the routing of the metal electrodes; (c) the metal electrodes are defined through lift-off; (d) a photoresist mask is defined to protect the wafer on both sides and is left open where the trenches need to be defined. The polyimide is then etched through the polymer reactive ion etching process; (e) the sample is then wet etched with a solution of $4\text{H}_3\text{PO}_4\cdot 2\text{HCl}$; (f) the protection layers are removed.

The presence of the trench does not modify the optical properties of the waveguides since it is far from the guiding structures. Due to the crystallographic properties of InP, the wet etch allows the definition of two different trench shapes, as indicated in Fig. 11.

When the cross section under consideration is perpendicular to the major flat (cross section A), the trench results in a triangular shape (V-groove), Fig. 12, due to the preferential etching along the (111) InP crystallographic orientation. While the aperture, w , depends on the mask aperture in the photolithographic process, the trench maximum depth is precisely defined by:

$$h = \frac{w}{2} \tan \alpha \quad (11)$$

where α is 54.7° . When the cross section is parallel to the major flat (cross section B), the resulting trenches have a rectangular-like (U-groove) shape, Fig. 13.

We have fabricated deep trenches for both cross sections by considering different apertures: $w = 20 \mu\text{m}$, $50 \mu\text{m}$, $100 \mu\text{m}$, $150 \mu\text{m}$, $200 \mu\text{m}$, $250 \mu\text{m}$ and three different etching times: $t_1 = 30 \text{ min}$, $t_2 = 70 \text{ min}$, and $t_3 = 100 \text{ min}$.

In general both V-groove and U-groove are feasible and can be applied to isolate passive and active components. However,

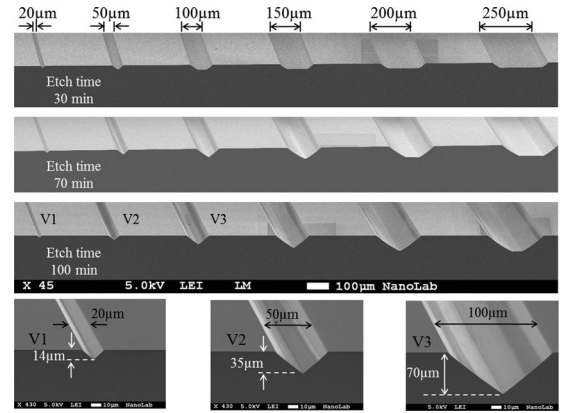


Fig. 12. SEM pictures of deep trenches fabricated in InP. From the top, the etch time are respectively 30, 70 and 100 minutes. The bottom pictures report the zoom of a few V-groove trenches.

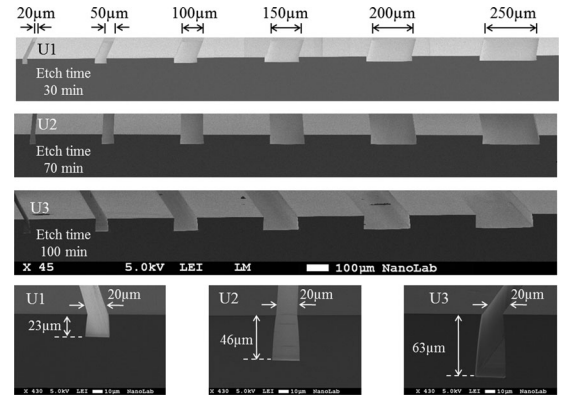


Fig. 13. SEM pictures of deep trenches fabricated in InP. From the top, the etch time are respectively 30, 70 and 100 minutes. The bottom pictures report the zoom of a few U-groove trenches.

to validate the trench effects we consider just the V-groove (V1, V2 and V3) because in our PIC the SOAs are parallel to the major flat of the InP wafer.

In detail Fig. 14 shows the heat distribution when the trenches V1 and V2 are applied in the same test structure described in Fig. 2, in comparison with the case without trench.

In Both cases the trenches are positioned in the middle between the SOA and the left arm of the modulator: it means that the parameter g , as defined in Fig. 10 is: $g = d/2$.

The air gap introduced through the aperture of the trenches represents a thermal isolation between the SOA and the MZ. Fig. 15, shows how for both cases, $d = 60 \mu\text{m}$ and $d = 130 \mu\text{m}$, that the introduction of the trenches is beneficial to reduce ΔV^i . $w = 0$ is the case without trenches already discussed experimentally and numerically in Section IV.

The current injected in the SOA is $I = 100 \text{ mA}$. For instance, when $d = 60 \mu\text{m}$, the trench V2 allows the reduction of ΔV^i from 1.9 V (ER = 5 dB) to 1.2 V (ER = 7 dB), indicating the improvement of the ER of 2 dB.

The deepest trench considered in our fabrication has depth $h = 70 \mu\text{m}$ ($w = 100 \mu\text{m}$). It is still not critical from the

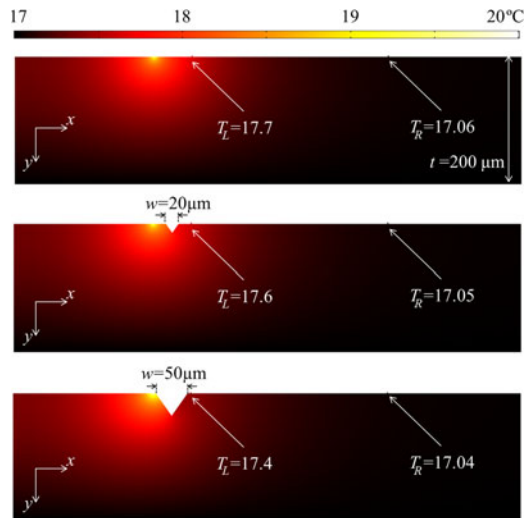


Fig. 14. Heat transfer from the SOA in presence of triangular trenches. The trenches considered are V1 and V2 (bottom picture). In all the cases above reported is $d = 60 \mu\text{m}$ and $I = 100 \text{ mA}$.

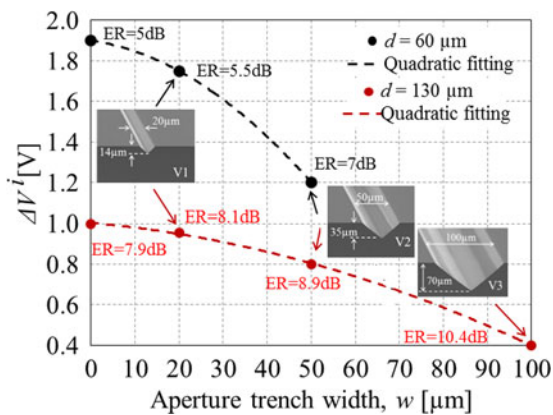


Fig. 15. ΔV^i reduction due to the introduction of V-groove trenches. The trenches are positioned in the center between the SOA and the MZ. $w = 0$ is the case without trenches. The injected current is $I = 100 \text{ mA}$,

mechanical point of view and we did not notice any chip damage. Moreover the trenches are localized around the active components and they do not affect the whole chip area.

By means of simulations, we also show how the position of the trenches affects the thermal crosstalk.

As a benchmark we consider the data reported in Fig. 16 for $d = 130 \mu\text{m}$. The trenches considered in Fig. 16 are V1 and V2. The parameter g , has been varied up to $30 \mu\text{m}$ in both positive and negative values along the x -coordinates. In both cases a slight reduction of ΔV^i with respect to the case $g = 0$ is reported. Intuitively, when the trench is closer to the SOA, it forces the heat to diffuse in the direction of the substrate, while the trench closer to the MZ reduces the temperature mismatch between the MZ arms, resulting in a lower ΔV^i .

However, the estimated variations are not relevant to further reduction in thermal crosstalk and we feel it is preferable to define the trench mid-way between SOA and MZ to release

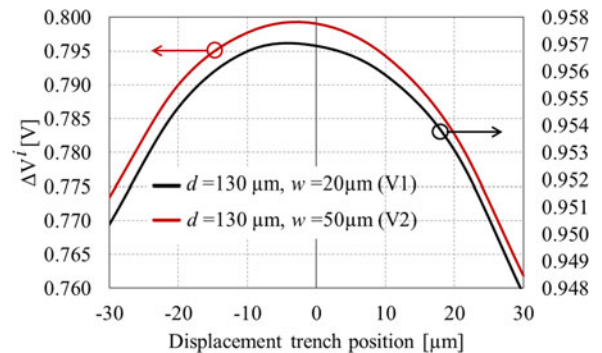


Fig. 16. Trenches position variation. The trench is shifted of $30 \mu\text{m}$ in both left and right directions respect to the initial configuration $g = 0$.

the fabrication constraints related to the alignment of the lithographic mask used to define the trenches.

VI. CONCLUSION

Deep trenches have been fabricated in indium phosphide by wet etching and used as solution to reduce the thermal crosstalk between active and passive components. An electro-thermal model has been developed to model the phenomena. The good agreement between the measured and the simulated data show how deep trenches improve the thermal isolation between components.

It results in a) reduction of unwanted thermal effects that may lead to malfunction or out of specification performance of a PIC, b) possibility to reduce the distance between components and then to increase the PIC density: it also means the reduction of the PIC cost. The definition of the deep V-groove through wet etching is a fast and reproducible process and we did not notice mechanical problems up to the etch depth of $70 \mu\text{m}$. Conversely, the main limitation of the V-groove is related to the impossibility to have the width and the depth of the trenches independent with each other: a deeper trench also corresponds to wider trenches that intrinsically limit the achievable minimum distance between components.

Another solution to investigate is based on the dry etch of the InP to makes the width and the depth of the trenches independent to each other. The best approach to isolate as much as possible the passive components, consists in etching completely the InP around them. In that sense the introduction of deep rectangular shaped trenches will be necessary to further reduce the thermal crosstalk effects."

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