Shifting the frontiers of analog and mixed-signal electronics

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Review Article

Shifting the Frontiers of Analog and Mixed-Signal Electronics

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Nowadays, analog and mixed-signal (AMS) IC designs, mainly found in the frontends of large ICs, are highly dedicated, complex, and costly. They form a bottleneck in the communication with the outside world, determine an upper bound in quality, yield, and flexibility for the IC, and require a significant part of the power dissipation. Operating very close to physical limits, serious boundaries are faced. This paper relates, from a high-level point of view, these boundaries to the Shannon channel capacity and shows how the AMS circuitry forms a matching link in transforming the external analog signals, optimized for the communication medium, to the optimal on-chip signal representation, the digital one, for the IC medium. The signals in the AMS part itself are consequently not optimally matched to the IC medium. To further shift the frontiers of AMS design, a matching-driven design approach is crucial for AMS. Four levels will be addressed: technology-driven, states-driven, redundancy-driven, and nature-driven design. This is done based on an analysis of the various classes of AMS signals and their specific properties, seen from the angle of redundancy. This generic, but abstract way of looking at the design process will be substantiated with many specific examples.

1. Introduction

The performance of analog and mixed-signal (AMS) electronics is characterized by a multitude of function and resource related parameters, like speed, bandwidth, accuracy, linearity, resolution, phase noise, dynamic range, SN(D)R, power dissipation and efficiency, robustness, chip area, yield, and design time. Moreover, most of them are dependent on each other. This leads to a high order of complexity and highly dedicated designs. In future technologies this complexity will further increase. The definition of "figures-of-merit" (performance parameter combinations) helps, but lack of insight slows down the shift of frontiers and even leads to wrongful "boundaries" and intuitive design approaches that are difficult to carry over to other designers.

The purpose of this paper is, in line with the invitation, to show the scientific view and vision on AMS that has been built up in my research group in the past 15 years, a vision that we see as crucial for further shifting the frontiers in AMS, and to elucidate with examples how it drives our research.

In contradiction to the hundreds of papers we published on all kinds of specific AMS IC designs for various applications, this paper tries to formulate our high-level view on designing analog mixed-signal ICs. In this generalized view we leave out the (important) details of specific designs and focus on the fundamental properties, including all kinds of boundaries and restrictions of the various AMS signal representations, of the various IC technologies (the physical aspects) in which we want to implement the system functions, and of the design environments that provide us with the resources to do the design. As such, we deliberately make an abstraction by leaving out specific design properties and focus on the underlying fundamental and generic properties of signals and hardware. This makes it a scientific analysis that can be subsequently used in the synthesis of a plurality of existing and new applications and can support the designer to make scientifically founded choices and to structure his design approach, of course within the constraints of the specific system specifications at hand. Many references to practical designs from our group, which comprise all practical details that go with these specific designs, support the reader to link this high abstraction view to the lower implementation levels of specific designs.

Following this approach, we will argument that the primary role for AMS circuitry in general will be to provide a technology-matching function, and, in practice, this takes

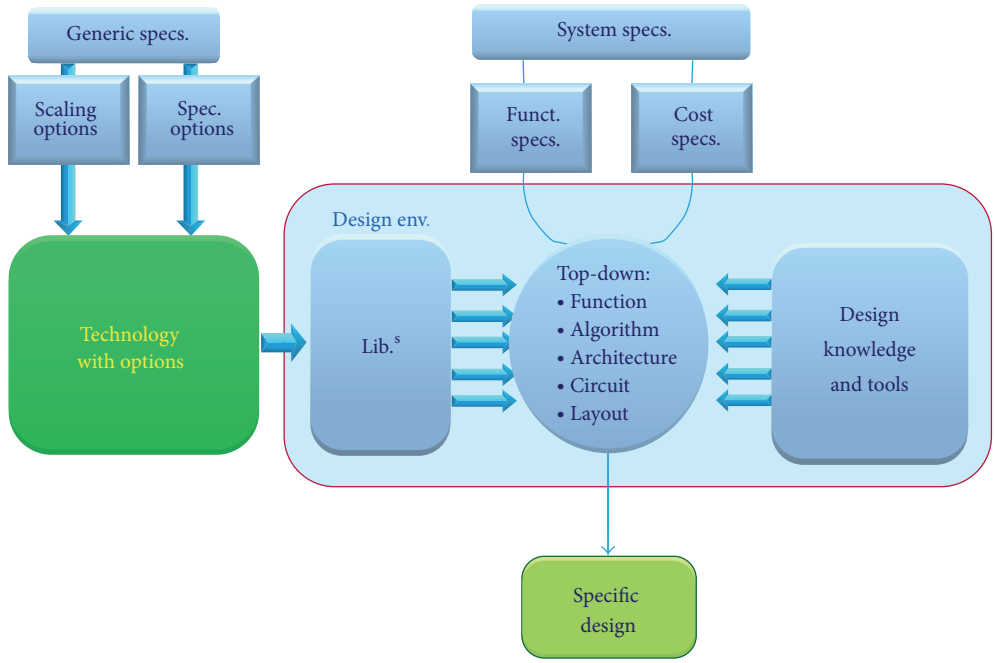

Figure 1: Generic design process.

place in the so-called frontend. As such, the word frontend is defined here as any interface between an analog communication channel, sensor, or actuator, on the one hand, and the digital processing chip, on the other hand. The reasoning behind that is that the information processing that is required by the system function (not to be confused with the above-mentioned signal-conditioning functions in the frontend) is usually best done in the digital domain, after having the signal domain and signal carrier optimally matched, in the frontend, to the technology.

We will also introduce the fundamental concept of redundancy and explain that this plays a crucial role in this matching function. We will use for this reasoning the high-level concept of channel capacity, as introduced long ago by Shannon [1]. In this paper we will show that this concept also applies to IC design.

Based on all of this, we propose four complementary "matching-driven" design procedures for AMS frontend design that differ fundamentally from the top-down approaches used for the implementation of the system function in the digital domain:

(i) *technology-driven matching;*

(ii) *states-driven matching;*

(iii) *redundancy-driven matching;*

(iv) *nature-driven matching.*

The paper also includes a forward-looking analysis of the issues that we believe will drive future research in this field.

The paper starts with a generic view on IC-design procedures and discusses how often promoted function-driven top-down approach leads to wrongful boundaries for AMS design (Section 2). To find out how the design approach should be changed in order to shift the frontiers across these "boundaries," we discuss and classify in Section 3 the various AMS signal representations and explain the crucial roles of abstraction and redundancy and relate that to Shannon's definition of channel capacity [1]. In Section 4, we describe the primary AMS function, matching the communication channel to the digital core via the frontend, and explain that the inevitable mismatch occurring inside the frontend itself requires a smooth and stepwise matching based on transformations in and between the various AMS domains. In Section 5 we elaborate on the proposed four complementary matching-based AMS design procedures: technology-, states-, redundancy-, and nature-driven matching. Section 6 addresses shortly the future of AMS and in Section 7 we will draw conclusions. For reasons of clarity and paper size, we restrict ourselves in this paper to intuitive discussions, rather than to exact formulations.

2. IC-Design and Boundaries

The generic IC-design process is visualized in Figure 1. System specifications, both functional and cost-related, are directing the design process towards a specific design. To reduce complexity, various abstraction layers are defined, each decoupling further details from lower levels. At all levels, libraries providing generic technology-related information (like clearance rules, transistor models, and IP blocks) are available, and general design knowledge and tools. Technology development is a decoupled process, driven by generic design-independent specifications; scaling plays an important role here, and special process options might be provided for certain performance domains, like low power or high speed.

The commonly preferred design procedure follows a top-down approach, allowing iterations where necessary, going step by step from high functional level towards final layout level. Intrinsically, higher level requirements are given preference over lower-level details, to further reduce design complexity. This "*function-driven approach*" is, for sure, the recommended approach for implementing complex functionality in digital systems.

For AMS design too, this *function-driven* approach is usually followed, but this paper will dispute its preference. Indeed, in non-state-of-the-art AMS designs, far enough away from the boundaries, you might follow a function-driven approach, but for such non-state-of-the-art designs implementation in AMS instead of digital is questionable at all, as we will explain. On the other hand, for state-of-the-art AMS designs, the appearance of a "boundary" is *not* due to technological limitations per se, as is often thought, but rather to a *nonoptimal match* between the functional requirements and the (limited) properties of the hardware. Proper transformations can provide an optimal match (For example, the "Walden FoM" for AD converters [2] is not technology constrained, as often assumed, but design constrained: a consequence of nonoptimal matching to the technology.) The design process must therefore principally be *matching driven*. By the end, performance is always resource limited, how much power, chip area, design time, and so forth do we want to spend.

To find an optimal match between functional requirements and technological properties, we first need to know what are the characteristic properties of AMS signals and how these enable signal-domain transformations.

3. AMS Subdomains, Shannon Capacity, and Redundancy

The double-log curves in Figure 2 show relative costs (here in terms of power dissipation) versus accuracy, for analog and digital. For analog, costs increase with (at least) a factor 4 for every factor of 2 in accuracy, whereas for digital relative cost increase diminishes with word size: every factor 2 in accuracy requires just 1 bit extra. This suggests that for accurate functions we better use digital and for simple functions analog. However, this is only partly true. First, all physics-related accuracy problems have been shifted to the (required, but here neglected) converter. Second, the difference is more fundamentally related to redundancy; digital is just an example of (low-level) redundancy.

Redundancy can be applied at all design layers (Figure 1), as will be discussed in Section 5, but already at the (abstract) signal level we can distinguish four classes of signal representations, leading to different types of hardware redundancy, depending on whether or not the time domain and/or the amplitude domain of the (abstract) signal is discrete; see Figure 3(a), with red for continuous and blue for discrete. For simplicity we will use in this paper the short names as mentioned within brackets. The three classes that have at least one continuous subdomain together belong to the AMS domain (Figure 3(b)).

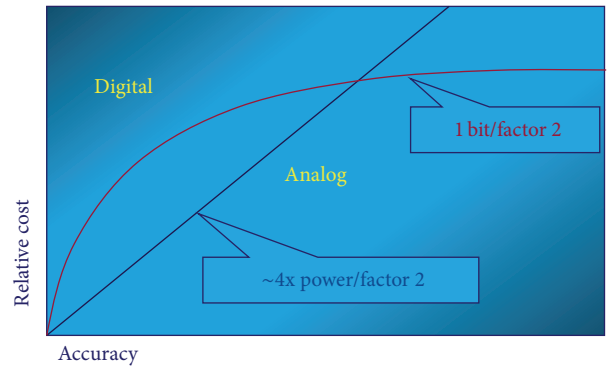

Figure 2: Relative cost versus accuracy for analog and digital.

Note that Shannon [1] already explained that every "propagation channel," generalised here to every "physical processing medium," and hence every IC, is limited in information-handling capacity, defined by its SNR and bandwidth: $C = \mathrm{BW} \log_2(1 + \mathrm{SNR})$. Note that BW and SNR are resources (particularly power dissipation) related and thus expensive, especially when working at the frontiers. The difference between this *available* channel capacity and the amount of the capacity that is actually *used* to represent the signal information makes up the hardware *redundancy*. This redundancy provides a margin that makes the capacity-limited channel robust, not only to unwanted signals that "eat up" part of the capacity in an actual implementation but also to uncertainties in hardware capacity due to limited model accuracy at design time, technology variations at processing time, and environmental, system, application, and user variations at runtime.

Note that any *physical* carrier, independent of the *abstract* signal domain chosen to represent the information, is purely analog by nature and that the capacity of any hardware system is given by the Shannon formula. In case of discrete-time or discrete-amplitude representation, a large part of the time, respectively, amplitude domain of the physical carrier will not be used by the abstract signal, which leaves extra redundancy in the hardware that can be translated to robustness in those specific domains. Digital signals are in general so robust, in both domains, that they allow full abstraction from carriers and hardware; see (Figure 3(c)). Staircase and asd signals allow abstraction in their discrete domain.

It should be mentioned that, besides the well-known discrete-time and discrete-amplitude domain signals, there are many more signal representations that use only restricted subparts of time and/or amplitude domain. These representations can also be used to provide robustness and also belong to the class of AMS domains. Examples are pulse width or period modulation and amplitude multiplex (e.g., power amp per subrange). Visualizing this by more than just four AMS domains seems more correct, but impractical in this case, as it will fuzzify the message of this paper. Therefore we will stick here, without loss of generality, to the four mentioned domains and consider the other domains as inside subdomains.

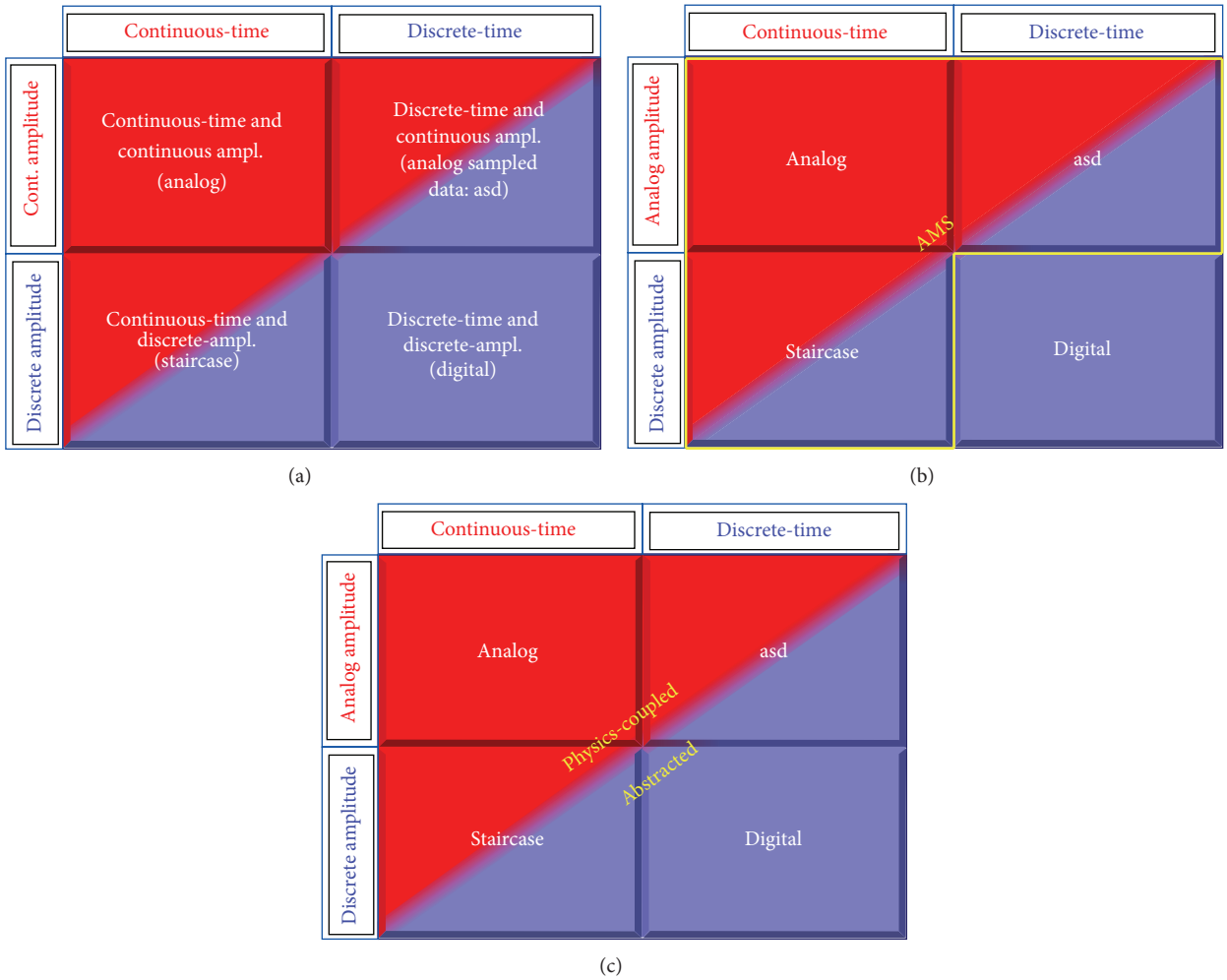

FIGURE 3: The 4 signal-representation classes (a), the 3 AMS classes (b), and the physics-coupled and abstracted domains (c).

4. The Matching Function as Primary Task for AMS

It is out of the question that digital is by far the best implementation for nowadays' complex functions on a chip, as it provides decoupling from hardware impairments and from hardware architectures, primitives, and structural properties. This provides process insensitivity (thus allowing generic CMOS processes), robustness, scalability, data bandwidth scaling, portability, flexibility, adaptivity, high yield, low design cost, high design reuse, and so on. It shows the power of the redundancy, and therefore the abstraction, in the digital signal waveforms.

However, most digital systems communicate with the outside world via communication channels, sensors, and/or actuators; see Figure 4. Therefore, data conversion is required. The benefits of digital usually justify this overhead, except for a small class of low complexity systems, where a full AMS implementation might outperform a digital one. However, the problem is far more than "just" data conversion: the signals from outside are optimized for their own medium (sensor, communication channel) and the on-chip digital signals for the IC-technology. (For simplicity reasons, we will neglect in this paper the third medium, the antenna. If on-chip, it should be taken into account with the frontend [3, 4]). As these media are different, the signal properties at both sides do not match (in terms of frequency, bandwidth, signal strength, SNR, interferences, etc.), and a "matching network" is required to perform signal transformations in time, amplitude, or frequency domain.

Figure 5 shows this problem suggestively: the information "package" should be transformed to fit the "straitjacket" of the silicon or vice versa, to fit the propagation medium. This is where AMS, with its *intra- and interdomain* transformations, plays its primary and very crucial role.

Note, however, that this matching network, the frontend (including data converters), is also implemented on-chip; see Figure 6, so *the signals in this frontend by definition show a strong mismatch to the (silicon) medium.* The figure visualizes this in "Shannon language": we have three channel sections, but only two media; the left and right sections are optimized; the frontend is not.

The mismatch is the strongest at the input of the IC and decreases along the frontend. Brute-force direct digitizing

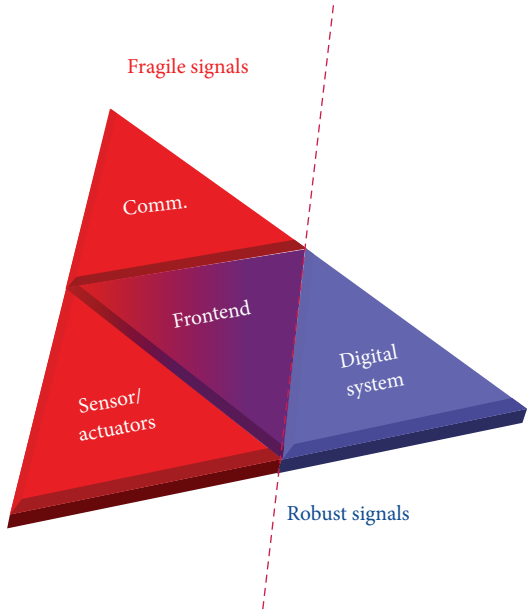

Figure 4: The AMS frontend in between digital system and sensor/actuator/communication channels.

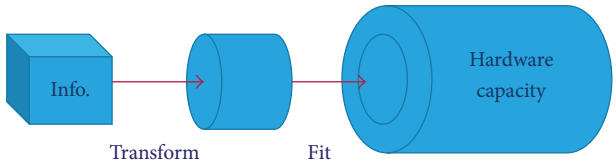

Figure 5: Signal transforms to fit the information to the hardware.

would create an abrupt mismatch in time and/or amplitude within the frontend, forming a bottleneck that can only be counteracted by increasing power dissipation. As a chain is not stronger than its weakest link, this is clearly not the optimal solution. We have to carefully *(re)distribute redundancy* over amplitude, time, and frequency, providing a better balance of robustness over the domains "channel coding," to achieve higher overall robustness.

5. Matching-Based Design

As discussed, we need to match the signals in the AMS domain gradually between communication medium and digital processing medium (silicon), taking into account that these matching steps themselves take place inside the (as yet unmatched) silicon medium. The question is now: *how do we design this AMS matching system, the frontend, such that we have an optimal smooth match between signal properties on the one hand and technology properties (the medium) on the other hand, via appropriate signal transformations and hardware changes and adaptations*? To answer this, we go back to the design process and look more in detail to it, Figure 7. The function-driven approach is exchanged now for a "matching process," as the primary goal should be to match smoothly the functional specifications with the technology properties.

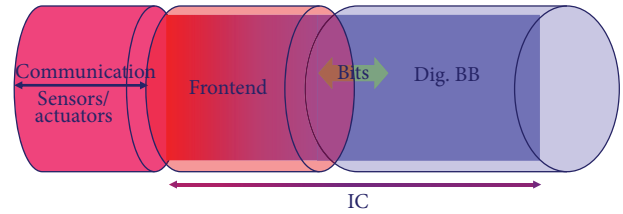

Figure 6: Three channel sections in the overall chain, implemented in two media.

This matching procedure can still be driven from different angles. Here we will discuss four design approaches (2A–2D in the figure), each complementary to the others:

(A) *technology-driven matching;*

(B) *states-driven matching;*

(C) *redundancy-driven matching;*

(D) *nature-driven matching.*

Besides adapting our hardware by proper design, we can also adapt the technology, to achieve a better match, by adding specific options (1A in Figure 7) or even by using a technology with special options for the frontend (1B in Figure 7). The last approach would require a separate IC for the frontend or a technology overhead for the overall IC. This paper focuses, however, on the design process.

(A) Technology-Driven Matching. Technologies are defined by foundries; the only freedom for the designer is in the choice of technology. "Hardware" is based on technology and therefore is subject to technology limitations but also implies all circuit and architecture choices, defined by the designer. By proper hardware design and signal-processing choices an optimal matching with technology can be achieved. The technology properties form therefore the hard constraints that should be taken into account directly from the beginning of the design. These properties (e.g., signal ranges and noise levels) should then be compared to the system-level specifications (e.g., required signal resolution). Architecture, circuit design, and signal-domain transformations should provide the optimal match to the medium in the different (physical) domain and at all intermediate steps in the frontend.

As capacity limitations related to technology (and resources) are a fundamental problem, it seems in the first instance paradoxical to further restrict ourselves to go over to AMS signal domains that use only subsets of time and amplitude. However, as mentioned, these restrictions provide robustness. This allows decoupling from imperfections, which creates options for reducing, for example, the power dissipation.

Moreover, the abstraction it allows enables decoupling of individual algorithmic operations, creating a lot of freedom in assigning operations to hardware and in scheduling in time, as we very well know from digital. This in turn creates options to balance the time-domain and amplitude-domain redundancies to provide a better match. Finally, it enables using more hardware to increase the overall capacity.

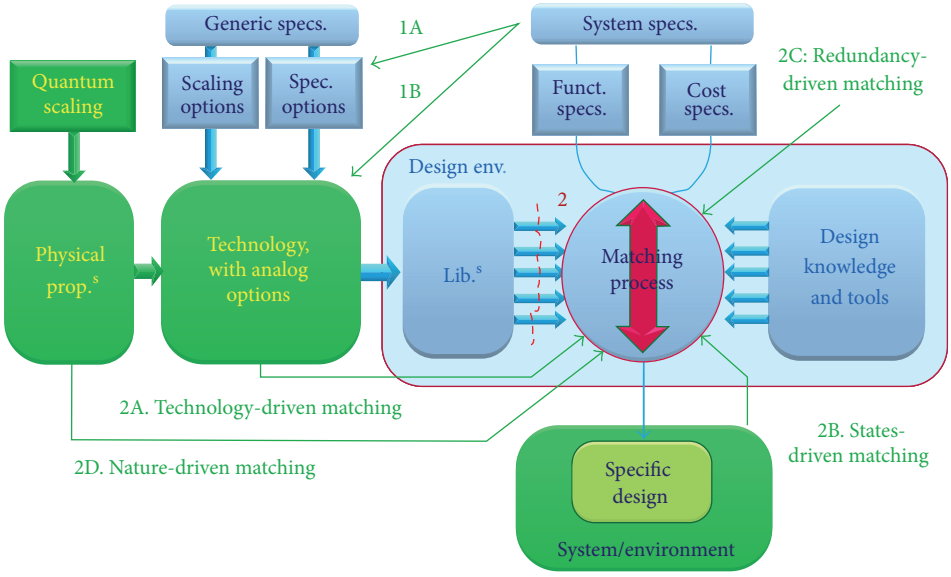

Figure 7: The four design approaches shown in relation to the generic design process.

So, redundancy and abstraction enable far better matching between functional requirements and technology properties, which more than compensates the loss in used capacity "per amount of hardware." Note that technology capacity is limited, but hardware capacity is not: it is finally only subject to cost, as expressed in Section 2: "final performance is not technology but is resource limited." For example, we can cross the "bandwidth boundary" of the hardware by switching over to discrete-time and parallelize operations in time interleave or the "resolution boundary" by sequencing the algorithm in lower-resolution suboperations that better match hardware resolution, like in pipelined data conversion. Redundancy created by restrictions in the signal domains thus generates many new options for transformations. Here we will discuss very shortly, with a helicopter view, a number of intra- and interdomain transformations; to elucidate this, see Figure 8. For details we refer to the references.

Figure 8(a) refers to all transformations within the purely analog domain. Most of them are well known, for example, offset, gain, compression, and expansion in the amplitude domain; frequency offset (mixing) and bandwidth compression or expansion in the frequency domain; amplitude-frequency transformations (AM-to-FM modulation); and so forth. (Note that intra-time-domain transformations are severely restricted in the purely analog domain, as information is continuously present and we cannot go back in time. Redundancy can therefore only be applied in time to come for example, by positive time shifts or time stretching. Transformations to discrete-time signals and hence to the second column of Figure 8 create time redundancy and enable many intra-time-domain transformations.) For power amplifiers the voltage, current and temperature boundaries of a technology can be circumvented by using distributed amplification [5, 6].

Unconventional technologies may ask for unconventional approaches. For example, in organic technologies, used for large-area, flexible-foil, and ultra-low cost electronics, hard faults (functional defects) and soft faults (variability in performance) completely dominate the design. This (still) leads to a preference for p-only technologies and circuits with a minimum number of transistors to reduce the hard faults. The severe p-only restriction leads to quite unconventional circuit architectures to provide an optimal match to the specific organic-technology properties, while reducing the vulnerability to the high technology spreads and the lack of spatial correlation (bad matching). Examples can be found in the references: in [7] the transistor output impedance is applied for filtering purposes, in [8] a specific "positive-feedback level shifter logic" is proposed, and in [9] a parametric way of amplification is used.

The p-only circuit limitation also makes discrete-time operation not realistic, which means that transformations are restricted to the two left quadrants in Figure 8. Complementary organic technologies (or hybrid technologies, with inorganic amorphous metal oxides), using evaporated or printed materials, face even more hard faults but can provide higher resilience to variability at circuit level, as all established complementary circuit options are available now to provide optimal resilience [10, 11]. Moreover, discrete-time operation becomes available now, enabling AD and DA, and more generally designs in the asd and staircase quadrants of AMS [12, 13].

Nonlinear transformations form a specific class of (unconventional) transformations. They can, for example, be used to exceed the frequency limitations of (already high-speed) technologies. Figure 9 shows how signals, generated at regular "electronics frequencies," matching the technology bandwidth, are frequency shifted in a transmitter with passive nonlinear transmission lines (NLTL), to the THz domain, so above the technology bandwidth. Subsequently, this THz signal is transmitted to and reflected by a device under test. In the receiver, another nonlinear transmission line (NLTL)

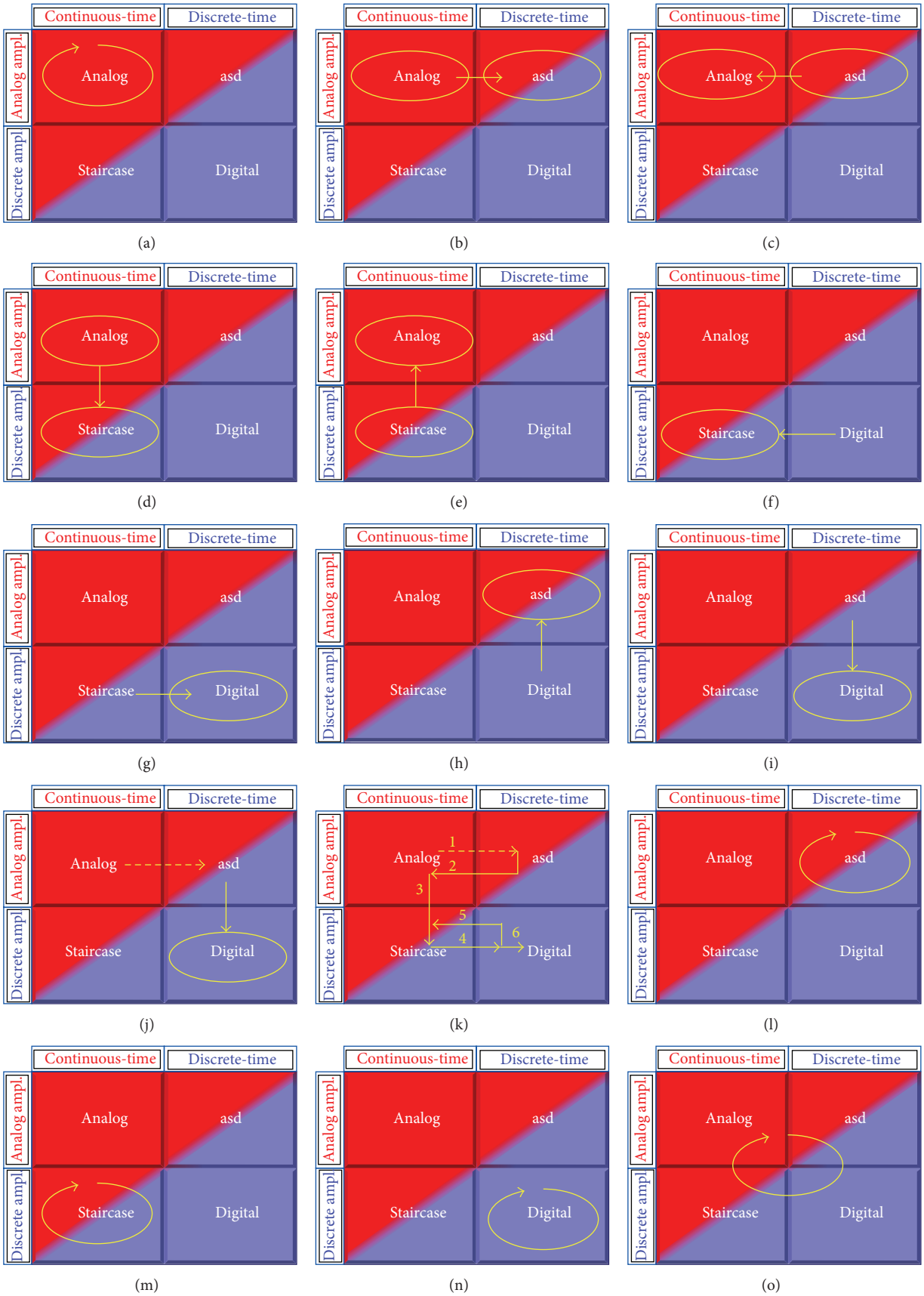

Figure 8: Intra- and interdomain transformations.

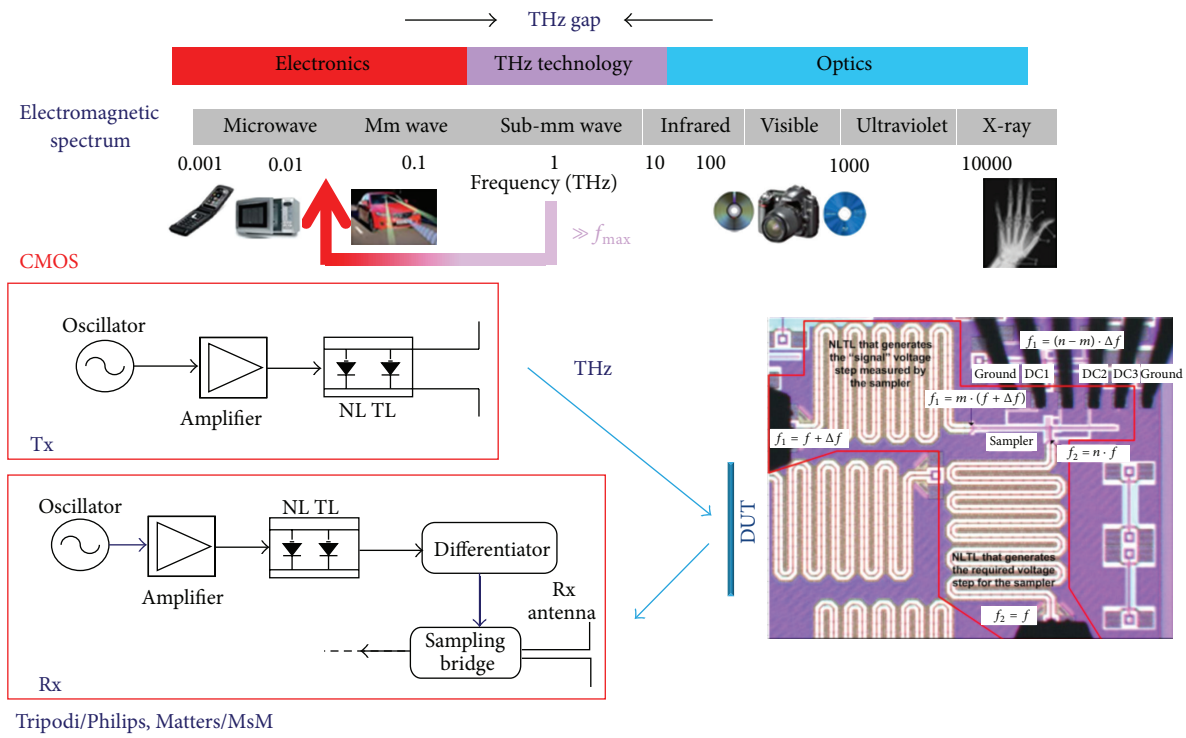

FIGURE 9: Passive nonlinear frequency shifting to match THz frequencies to IC technology frequencies.

mixes back these THz frequencies to "normal" frequencies that fit again in the bounded frequency domain of the technology. By this way we have created an on-chip THz spectrometer with frequencies far above the "boundary f_{max}" of the technology [14].

Another application of nonlinear transformations is shown in Figure 10. It shows how a strongly nonlinear low-noise input amplifier, here called "nonlinear interference suppressor" (NIS), is used, in a very unconventional and counterintuitive way in a transceiver like a smartphone. The deliberately introduced strong nonlinearity at the input of the receiver is very well controlled as a function of the known signal (transmitted by the same frontend) that forms a close-by interferer for the receiver. The nonlinearity is controlled in such a way that the fundamental component of the interferer is maximally suppressed (also called "compression"), and "replaced" by one or more if its harmonics outside the channel bandwidth [15, 16]. These harmonics are further away from the received signal and can therefore easily be suppressed by a filter.

Figure 8(b) refers to the well-known sampling, leaving only signal information at discrete-time moments, shifting a surplus of redundancy in the frequency domain (the surplus of bandwidth the hardware can handle) to the time domain without information loss. The redundant time in the physical carrier creates new freedoms for the designer. Examples are: time-multiplexing of the system functions, by clock-phase-controlled switches (time-variant operation); rescheduling of operations in time; positioning of the discrete-time samples of your signal in such a way that they are shifted in time with respect to the periodic glitches that are caused by clock generation or by digital blocks, so that the signal is not interfered by these glitches; making the signal processing insensitive to absolute errors (by making them only dependent on device ratios, like in switched-capacitor circuits); the use of scalar integration within a single domain (e.g., voltage to voltage, like in switched-capacitor integrators); the use of hardware sharing (time-multiplex use of hardware); and so forth. In fact, it enables within the analog domain a plurality of transformations that are already well known and heavily used in the digital domain; indeed, these properties are fundamentally related to discrete-time (and not to discrete amplitude) and as such not reserved for digital as most designers assume.

Figure 8(c) shows the well-known reconstruction to continuous-time signals, possibly done stepwise via oversampling and analog filtering. Information is then shifted from the amplitude to the time domain, resulting in less time-domain redundancy and more redundancy in frequency domain (less spectrum occupied) and amplitude domain.

Figure 8(d) shows a less conventional domain, here called the staircase domain. The amplitude domain is limited here to discrete levels, providing signal redundancy in the amplitude domain. An example is an asynchronous sigma-delta modulator that we designed to control a power amplifier with only discrete-amplitude levels, enabling efficient switched-mode (discrete-level) amplification; see Figure 11. With the number of quantization levels we can balance the redundancy in time and amplitude domain. The asynchronous "data-driven" sampling provides the time redundancy without introducing quantization errors: there is no loss of analog information; the information is only shifted partly from the amplitude domain

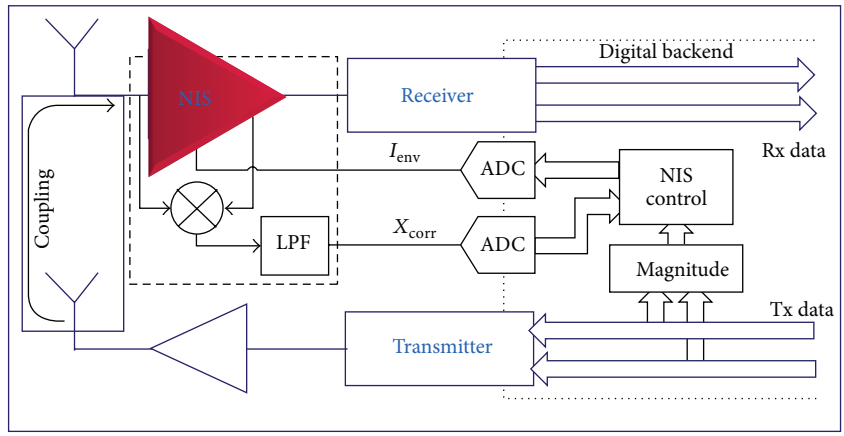

Figure 10: A nonlinear transform to shift a known close-by interferer away from the signal band.

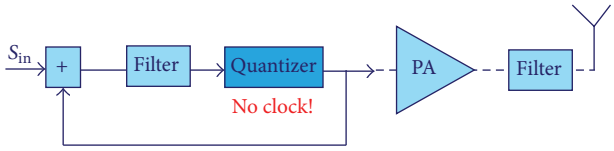

Figure 11: A staircase transformation to enable efficient switched mode power amplification.

to the time domain, where it is present in the position in time of the transitions in the square wave multilevel (possibly 2 level) signal, at the cost of a larger occupied bandwidth. More detailed information can be found in [17–21].

The so-called LINC amplifier uses an alternative staircase transformation to achieve efficient power amplification: a continuous-amplitude signal is split into 2 level signals, with different phases (information is thus now transferred to relative time domain). Both are subsequently efficiently amplified by two switched-mode amplifiers. Adding the outputs recreates the original continuous-amplitude signal but now amplified with respect to the original signal [22].

Yet another example for this class of transformations is the folding operation in an AD converter. The amplitude range is split into subranges and all of them are mapped to one and the same subrange [23].

Aside from hard splits in the amplitude domain, also smooth changeovers are possible, like in, for example, Doherty amplifiers, where for the larger amplitudes the amplification is gradually taken over from a main amplifier to a peak amplifier, via load pulling, an interaction between the amplifiers (with outputs connected via transmission lines) via their output impedances [24, 25].

In envelope-elimination-and-restoration (EER) amplifiers, a signal that originally has all its information in the amplitude domain is split into a signal in (again) continuous-amplitude domain (the envelope) and a two-level signal in the staircase domain (comprising the carrier phase information), such that a transistor (drain-modulated by the amplitude-continuous first signal) can be operated very efficiently in switched mode by switching it with the second (two-level) signal [26].

Yet another example is that of a VCO-based ADC. In that case, a signal with amplitude information is translated to a square wave signal of which the zero crossings contain the information. Subsequent translation to the digital domain is performed by counting the number of high-speed clock periods (of another clock) between the zero crossings. In [27] such an ADC is described for implementation in organic electronics, to provide robustness to the high spreads in such a technology. (Note that, in case of amplitude-to-phase transformation, the information is put on a continuous-time basis in the phase; in that case the transformation belongs to the situation described in Figure 8(a).)

In Figure 8(e), the way back is performed by spectral filtering; see, for example, the filter before the antenna in Figure 11. Such a filter reduces the bandwidth in this example to keep the transmitted signal within the boundaries of the allowed communication channel, without loss of information, as its output signal comprises more information in the amplitude domain than its input signal. This increases spectral redundancy (spectral purity) at the cost of amplitude redundancy.

In Figure 8(f), the transition from digital to staircase implies a transition from discrete-time to continuous-time and as such there is a reduction of the time-domain redundancy. This is used, for example, in asynchronous event-driven converters that exploit maximum technology speed: a next algorithmic step is done instantaneously after the hardware is ready with the previous step, instead of letting it wait till a next clock phase (in synchronous operation). See, for example, [28], where a "slope AD converter" (which is intrinsically slow) is geared to maximum speed: the slope automatically steps up at the maximum speed the hardware can provide (like a domino effect), until a comparator detects that it has reached the value of the analog input signal. The amount of steps is then the digital countervalue of the analog input.

In Figure 8(g), a transformation from staircase to digital implies (synchronous) sampling, or saying otherwise: a change from asynchronous to synchronous, but this sampling process experiences reduced constraints compared to the transition from purely analog (continuous both in amplitude and time) to discrete-time analog (analog sampled data),

Figure 8(b), as the amplitude is constant during the sampling process, thanks to the applied redundancy in the amplitude domain [18]. A quantization error is introduced (a loss of information, as both domains have now made discrete), and some hardware capacity lost (SNR deteriorated), but the robustness to timing errors has improved.

In Figure 8(h), from digital to asd means filtering with an infinite impulse response (IIR) filter, which translates the digital multilevel signal to a continuous-amplitude signal. Note that a finite impulse response (FIR) filter also increases the resolution in the amplitude domain (to more discrete levels), but the output remains multilevel, which implies a transformation within the digital domain (Note that binary is often mixed up with digital; however, binary is only a subset of digitals (multilevel).).

In Figure 8(i), the reverse direction reflects the well-known quantization, performed in all AD converters that start from the asd domain, introducing a quantization error with associated loss in used capacity in the amplitude domain. However, the gain in redundancy and robustness has formed the basis for many AD architectures [29, 30], thanks to the freedom that the increased redundancy provides in mapping over time and amplitude domains, like pipelining, time interleaving, recycling, sigma-delta modulation, and all kinds of combinations of them.

In Figure 8(j), introducing a sampling preceding the previously discussed quantization step reflects all conventional AD converters that have continuous-time input and perform the sampling before the quantization (which is not strictly necessary, as this paper shows).

In Figure 8(k), more complex AD conversion is possible, exploiting even more the various subdomains. A time-interleaved asynchronous SAR AD converter, for example, the one discussed in [31] and shown in Figure 12, first performs the sampling; see number "1" in both Figures 8(k) and 12. This sampling creates a redundancy in time which paves the way for time-multiplexing of the following iterative AD suboperations. A hold function translates the sampled signal back to a continuous-time hold signal (2), without losing the redundancy in time, enabling subsequent fast asynchronous operation of comparator and logic (3 + 4). Simultaneously, an approximating quantized signal is generated iteratively, each iteration with more accuracy, by the DA converter that translates the asynchronous digital words, in each iteration step, back to the staircase domain (5). After all asynchronous iteration slots, when the comparator output flips, meaning the analog input has been approached optimally, the final digital output is delivered. In a similar way, redundancy in time is created and used in [32–35].

In Figure 8(l), also within the asd domain, we can perform transformations. Sample-rate transformations with interpolating or decimating filters redistribute redundancy between amplitude and time domain. Many other asd functions are possible in this domain and are known from, for example, switched capacitor literature, like the ones discussed already above in the discussion of Figure 8(b).

In Figure 8(m), within the staircase domain, we find all kinds of period-modulation transformations, with information (partly) in continuous-time domain [19]. Any

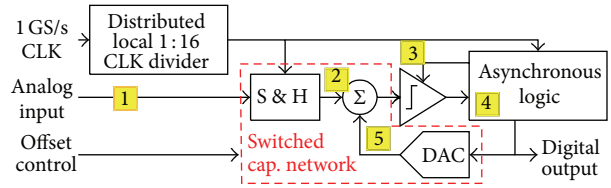

Figure 12: Example of time-multiplexed AD suboperations, enabled by first creating time redundancy by overall synchronous sampling, with transforms in all 4 subdomains of Figure 8.

transformation from purely analog to this domain needs ("data-driven" or asynchronous) sampling, to achieve the required time redundancy for time-domain operations; this asynchronous sampling was already discussed in Figure 8(d). The so-called time-domain AD converters first perform this transition from purely analog to staircase (two-level signals in this case, with the information now in the pulse duration) and subsequently use synchronous sampling to create the time redundancy required to do the suboperations of the AD algorithm in the "empty" (redundant) time periods. Synchronously counting the output periods introduces now the quantization, transferring the information to the digital domain [28].

In Figure 8(n), the digital transformations fall outside the AMS discussion; they reflect all processing in the digital backend of the IC.

In Figure 8(o), this figure emphasises that in any frontend with feedback loops we can have continuously transitions between domains. A continuous-time sigma-delta converter is an example.

(B) States-Driven Matching. On top of the above discussed technology-driven matching a states-driven matching is required to shift the boundaries; see Figure 7. As mentioned before, the actual situation, represented by the states, will differ from the system you wanted to design, as unwanted signals will "eat up" part of the capacity and because of uncertainties in the hardware capacity due to limited model accuracy at design time, technology variations at processing time, and environmental, system, application, and user variations at runtime. If we can do both the measurement and the correction at runtime, we can come far closer to the ideal situation [3, 4, 36, 37].

Figure 13 shows the generic situation for an AMS frontend [37]. First, the frontend must be made adaptive (reconfigurable architecture, adaptable parameters, test signals, etc.) which requires redundant hardware. For example, for a DA we can put redundancy in the decoder [38] or in the core, by using unary code,or even several sets of DAs, each with unary/binary cores [39–41].

Second, any information from outside or inside states, obtained if necessary with optional extra hardware (to detect, actuate, or generate test signals, to analyse the situation and to control feedback and learning algorithms), will help and should be used. Both core hardware and pre- and postprocessing can be adapted. Note that a states-driven approach also needs redundant hardware. Next, some examples will be shortly addressed to illustrate the states-driven matching.

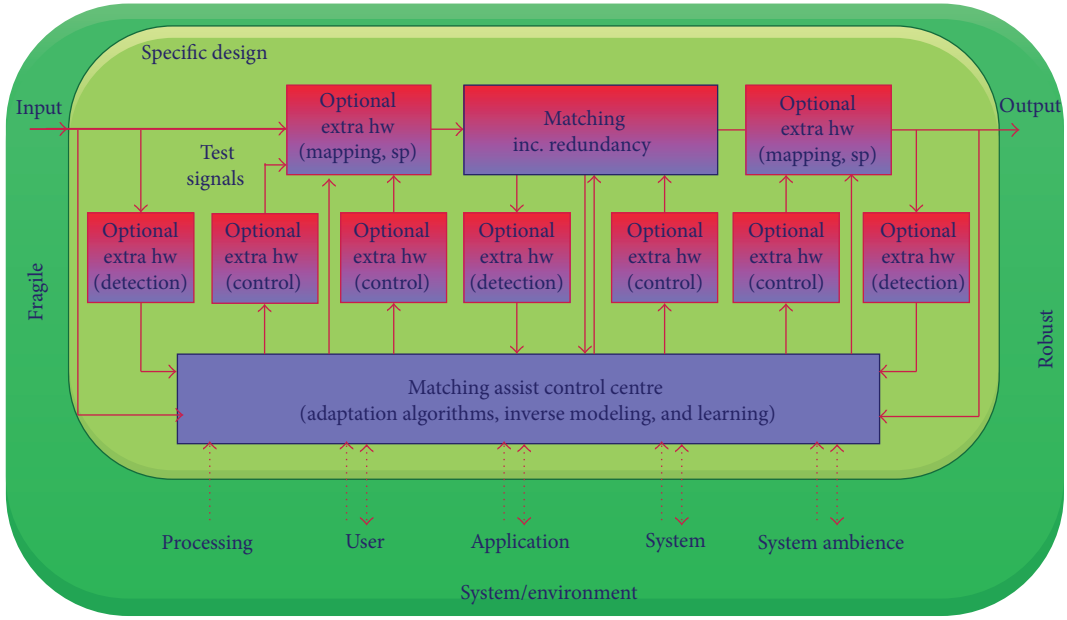

Figure 13: Generic diagram for a states-driven frontend system.

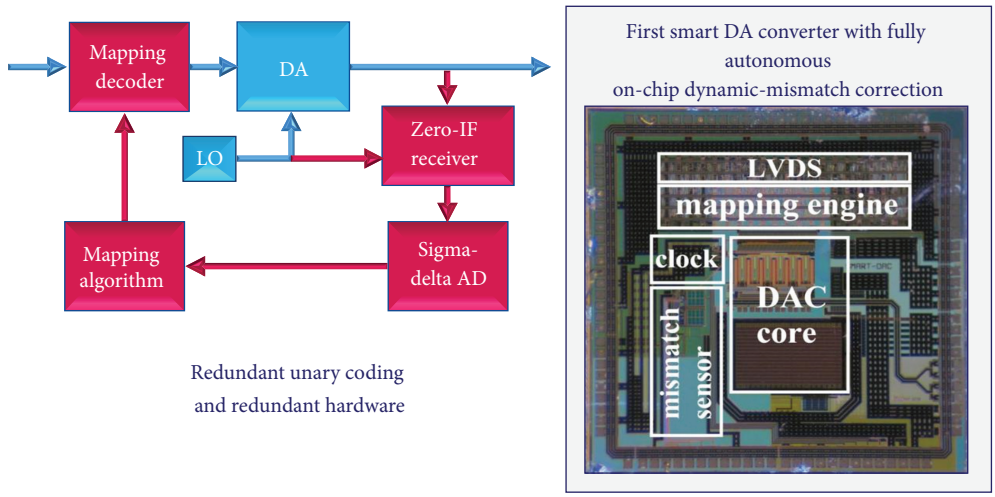

Figure 14: Dynamic-mismatch correction in a DA, based on code redundancy.

Figure 14 shows, as an example, how the algorithmic redundancy in the unary code of a DA converter in combination with an on-chip dynamic-error measurement and a feedback-controlled mapping decoder can be used to improve performance without excessive power consumption. The unary code provides many code options that, for an ideal DA, give the same output value. However, the errors in an actual DA lead to different results for these codes. The mapping algorithm that controls the decoder finds the best code options for the specific situation (with specific errors). The criterion for "best codes" is in this example the accuracy at high frequencies. This is detected by first downmixing that part of the spectrum in the "zero-IF receiver" and subsequently measuring the signal at baseband with a sigma-delta AD converter [42–44].

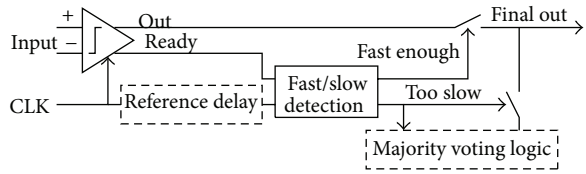

Figure 15: Improved SAR-ADC with comparator-state adaptive algorithm.

Another example is the "fast/slow detection circuit" in the SAR ADC in Figure 15 [33–35], which detects if the actual (processing and signal dependent) comparator is ready in time and adapts the SAR algorithm if necessary (more approximations in critical situations, followed by a

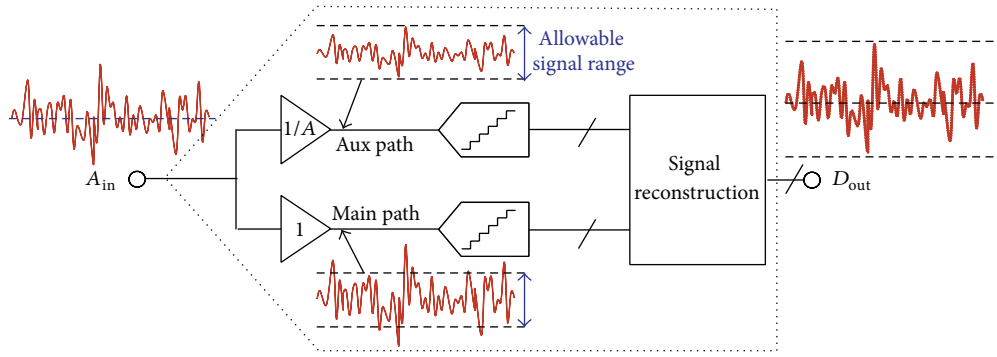

FIGURE 16: AD converter that uses amplitude multiplex based on signal statistics.

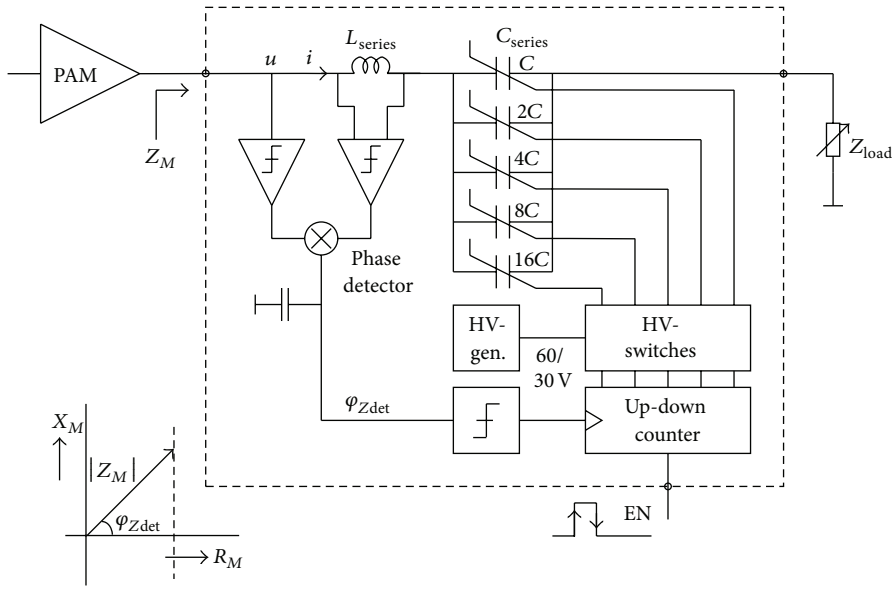

FIGURE 17: Adaptive antenna matching, dependent on reflection status.

majority voting). This is a favorable solution compared to overdesigning the power-consuming comparator such that it is fast enough for all potential situations.

Figure 16 shows an AD that splits the amplitude domain into subranges [45–47]. The performance of each AD is made proportional to the probability of the input signal in its subrange, which saves resources like power consumption. This is favorable for communication signals where the input signal shows a quite large probability for the lower amplitude range and a low probability for the higher amplitude range.

Figure 17 shows an example of a situation-dependent mismatch between the power amplifier and the transmit antenna (e.g., if a user holds his hand close to the antenna of his smart phone). This mismatch induces reflections, which can be measured and used to improve the antenna matching. This is a far more efficient solution than brute-force overdesigning for all potential situations [48–52].

Figure 18 shows a pregnancy monitoring system with smart sensing patches on the belly of the mother-to-be that can be made adaptive to the actual status of the mother and the baby, to the phase and to the history of the pregnancy, to interferers (by choosing the optimum set of patches), and so forth. Details can be found in [53, 54].

(C) Redundancy-Driven Matching. We have already discussed extensively the use of redundancy at the signal and hardware level to enable optimal matching transformations. We also discussed that redundancy is required to enable states-driven matching. This redundancy-driven matching approach can (and should) be extended to all higher levels of a system (algorithmic, circuit, and application level) and can as such relax considerably the requirements at the hardware (AMS) level. Many examples of this use of redundancy at the higher system levels can be found in literature, from error correction in AD, up to redundant parallel systems.

(D) Nature-Driven Matching. In the previous examples the hardware itself was calibrated based on redundancy and/or state information. Nature learns that redundancy is used abundantly, enabling very small and ultra-low-power primitive hardware cells. This leads to an efficiency in the use of hardware that exceeds the efficiency in our electronics with

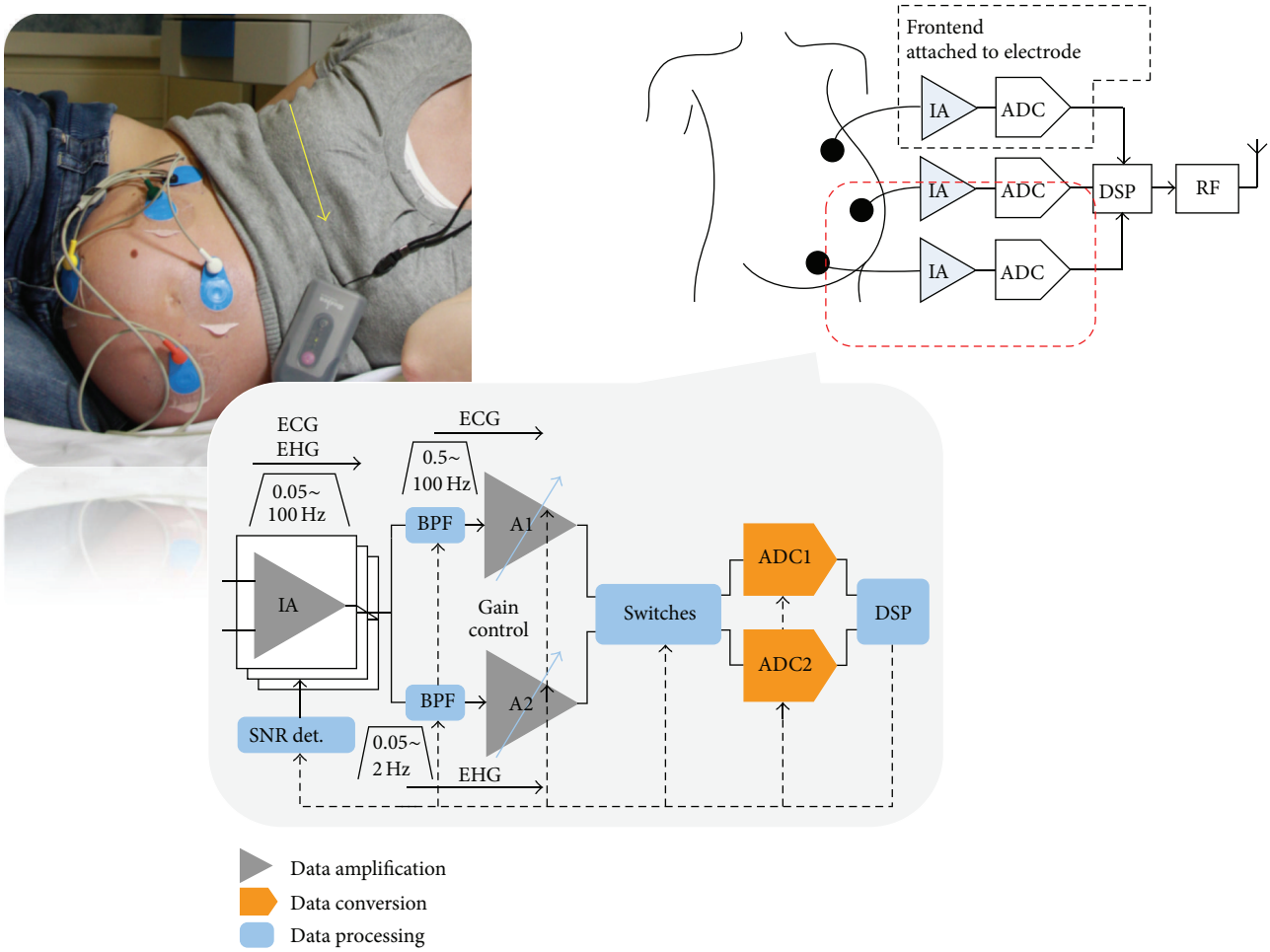

FIGURE 18: Pregnancy monitoring system based on status of baby and mother, pregnancy status, signal conditions, and history.

orders of magnitude. Indeed, these natural primitive cells are intrinsically very inaccurate, but that is corrected at the higher system levels, like ear and eye corrections in the brain. This correction is enabled by the abundant redundancy that is applied at the lower levels. Future IC-design should find an optimal balance also in that aspect. Further, nature relies on other paradigms, not yet used in IC design, as will be discussed next.

6. Future Prospects and Changing Paradigms

We are entering currently nanoscale electronics, clearly, but this is just a first step in a major transition that will be physics-driven and nature-inspired.

(i) Next to nanoelectronics come quantum electronics, with distinction between individual electron energy levels; with new, nanoscale, and quantum-scale devices at quantum-energy levels; with increased uncertainties in modelling and variability in processing; and with statistics-based design approaches.

(ii) A reduction in signal-handling capacity per device will be overcompensated by a capacity increase based on massively parallel hardware and signal processing and massive amounts of redundancy.

(iii) The digital paradigm, based on redundancy and correct primitive operation at the lowest level, might make place for analog mixed-signal processing (like in our brains!) in combination with redundancy at higher levels and learning mechanisms.

(iv) Alternative and hybrid technologies will arise, such as MEMS, organic and flexible electronics, optoelectronics, and molecular electronics.

(v) Alternative manufacturing technologies in terms of materials, processing, and lithography will be followed by self-organising and self-assembling hardware.

(vi) Self-organisation, self-learning, and self-assembling will enable autonomous short-term matching; self-growing, evolution, and inheritance will further lead to autonomous long-term matching.

7. Conclusions

Nowadays, system functionality is done digital, whereas AMS should perform a matching function between two media, while this AMS matching function itself is performed in an unmatched situation. This requires a shift in design approach, technology-driven, states-driven, redundancy-driven, and nature-driven matching, to enable crossing "boundaries" that are not fundamental boundaries but are consequences of a nonoptimal design approach. A high-level vision and accordingly a high-level design approach as discussed in this paper are necessary to be able to shift the frontiers in AMS design further.

We just face the very start of a new age of electronics. The changes we foresee will lead to an increased role for AMS in the future, even for system functionality implementation, combined with massive amounts of redundancy at various system levels, autonomous operation, self-organisation, and self-assembling. Like living cells.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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