CMOS Low-Noise Amplifier Design for Reconfigurable Mobile Terminals

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zur Verleihung des akademischen Grades

Doktor der Ingenieurwissenschaften
— Dr-Ing. —

genehmigte Dissertation

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Tag der wissenschaftlichen Aussprache: 03. Dez. 2004

Berlin 2004
D 83

Abstract

Communication standards developed in Europe, Japan and USA are not compatible with each other. This is a profound drawback particularly in the digital cellular telephony, where there is no common standard up to now.

The variety of wireless standards leads to some disadvantages, therefore the need for reconfigurability seems to be evident. A reconfigurable terminal should be able to support different standards.

Reasonable integration of different standards may include standards, which belong to the same family (e.g., GSM), but are developed in different continents. Such terminals have been already produced and a broad offer exists on the market.

A rather new approach of the standard integration is the combination of different families of standards, for example between wireless data and digital cellular telephony like UMTS with WLAN or HIPERLAN. In this case, nearly all parameters defining a standard are different.

In the scope of this work the multistandard, reconfigurable terminal is considered that supports the OFDM based WLAN standards (IEEE802.11 and Hiperlan/2) and the CDMA based UMTS FDD standard. Special consideration has been made for the receiver of this terminal.

A reconfigurable hybrid architecture has been developed, rather than an architecture using many parallel switchable transceivers. Additionally to the hybrid architecture, a study on RF impairments is given.

The second part of this work handles with transistor physics and low noise amplifier design for a reconfigurable receiver, defined earlier. Since the small FET sizes of state of the art sub-micron RF-MOS-technologies have low capacitance values, thus large inductors are needed for matching. Because of theirs large dimensions they are placed off-chip. For this reason, the pad capacitance can not be longer neglected in the design process. It is shown

that the noise figure of low-noise amplifiers can be improved considerably by a proper choice of passive components. A design methodology is introduced, which reduces the equivalent noise resistance, and thus very good noise performance can be achieved in spite of rather poor noise matching.

The measurements of the amplifier, in respect to the noise performance and power consumption, show very good results, one of the best ever reported. 0.76 dB noise figure and 12 dB gain were achieved at 2.14 GHz, 3.5 mA supply current and 1.2 V supply voltage.

Acknowledgments

I would like to thank my doctoral thesis supervisor Professor Georg Böck for his continuously support and many ideas that help me with work on this thesis.

I wish to acknowledge also Nokia Research Center Bochum, Germany. For the last three years, I have worked together with the Nokia Research Center, within the German funded BMBF-project "Software Defined Radio Based Architecture Studies for Reconfigurable Mobile Communication Systems" (RMS), No. 01 BU171. This thesis is partially based on the research carried out during this cooperation.

I also would like to thank my parents. Without their support in all aspect of my life, this thesis would never come true. I owe many very important things in my life to my parents, therefore I regret that my father had died before I have finished this thesis.

Finally I would like to thank my wife, Joanna for invaluable help and support. She has cheered me up during work on this thesis and during the long time of our separation, when every two weeks I travelled between Berlin and Warsaw back and forth. Actually, she has made almost all graphics in this thesis.

I can not forgot also my little daughter, Agata. Although unconscious of all the matter, she has also participated in writing this thesis. With his calmness, she let his father to go to sleep in the night. Therefore, I could finish faster this work. It is time now, to repay her for that.

This work is dedicated to her.

Contents

Chapter 1

Introduction

Decades of continuous development of wireless communication has brought many standards. This is an ongoing process focusing on 3G- and 4G- systems at the moment.

Although all existing wireless standards have their own particularities, they belong to one of the four following groups: digital cordless telephony, wireless data, analog cellular telephony and digital cellular telephony. They cover the frequency range from 800 to 5800 MHz.

Unfortunately, standards developed in Europe, Japan and USA are not compatible with each other. This is a profound drawback particularly in the digital cellular telephony, where there is no common standard up to now.

This problem exists also for new WCDMA systems, where the standards defined in Europe (e.g., UMTS) differ from the ones in USA and Japan. Reasons for this incompatibility are: different needs of mobile users, different frequency allocations for preceding standards, different interests of companies and political constraints.

The variety of wireless standards leads to some disadvantages: manufacturers have a high effort with respect to development of many different devices and systems for base stations and terminals. Providers and users have additional costs because of higher base station complexity and the need of more than one terminal (e.g., mobile phone) if international availability is needed. The well-known dual or tri-band GSM mobile phones are not really reconfigurable systems within meaning of this work, because they just support very similar standards in different or even adjacent frequency bands.

Therefore the need for reconfigurability seems to be evident. A reconfigurable terminal should be able to support different standards. The principle of reconfigurability presumes that only one standard will be used at a time, but does not exclude the advanced idea of multi-usability, where the terminal supports different standards in different networks at the same time.

Reasonable integration of different standards may also include standards, which belong to the same family (e.g., GSM) but are developed in different continents. Such terminals have been already produced and a broad offer exists on the market. These terminals support also a few frequency bands but use very similar procedures for signal and channel coding.

A rather new approach of the standard integration is the combination of different families of standards, for example between wireless data and digital cellular telephony like UMTS with WLAN or HIPERLAN. In this case, nearly all parameters defining a standard are different.

The development of such really reconfigurable systems is a challenging matter because very innovative ideas, concepts and technologies are needed to overcome the integration problems. Standardization-, system-, RF- and baseband engineers have to work very close together, to find the optimal system architecture. The optimization of the system performance can be no longer performed on the base of the single function blocks optimization, but a system simulation is needed. Only based on system simulations, the system optimizations with respect to technical performance, power consumption, dimensions, weight and cost will be possible.

This work copes with such demanding task, not only in high level system concept but also in LNA design.

1.1. Scope of This Work

The following chapters provide extensive information about reconfigurable systems and LNA design guidelines. To achieve these goals, this dissertation takes into consideration areas such as reconfigurability, transceiver system simulation, device physics, noise optimization and finally LNA design.

Chapter 2 shows the demand of reconfigurability for near future systems. For such reconfigurable systems the software defined radio and signal path optimization techniques shall be used. Therefore, the digital and analog part of the transceiver has to be optimized through system simulation. This chapter shows also the reconfigurable receiver radio frequency architecture that supports two standards. An impairments analysis based on system simulations is also given, for this architecture.

Chapter 3 discusses passive devices realized on chip, and Chapter 4 the submicron MOS transistor. In the latter chapter the short channel devices are emphasized since they play a major role for current circuit designs. Besides

of direct current (DC) characteristics, high frequency transistor behavior is shown, together with noise models. This chapter shows also the four noise parameters of the transistor as a function of its size. These results are extensively needed in subsequent chapters of this thesis.

Chapter 5 gives a background for two-port noise theory. Various two-port noise representations and their relationships are shown. The way of deriving the four noise parameters from noise correlation matrix is shown. Moreover, guidance for noise analysis of the circuit that consists of basic two-ports connected together is given.

Chapter 6 shows design guidelines for LNAs in which the pad capacitance is treated as a part of the amplifier. To the knowledge of the author, the extensive study presented in this chapter is novel. Based on the approach on two-port noise theory, It shows that pad capacitance have positive influence on the amplifier noise characteristic. The LNA using the described design methodology is designed, and the measured results are given in Chapter 7. Although some problems has been reported, measured and simulated noise performance is in good agreement. Finally, Chapter 8 concludes with a summary and suggestions for further improvements.

Several appendices provide more detailed explanation of certain subjects. Appendix A introduces some issues with layout and on-chip implementation of cascode amplifier. Appendix B gives an electrical chain matrix of a cascode amplifier. Finally, Appendix C shows the case when the power and noise matching in cascode amplifier leads to the same input matching network.

Chapter 2

Reconfigurable Systems

In the near future, communication systems will be required to perform an increasing number of functions within reduced size, power, and weight requirements and tight costs constraints. In a reconfigurable, software defined radio (SDR) system it is even more the case due to the necessity to support all the functionalities of two or more different systems within one hardware architecture [1].

Because of these requirements dynamic signal path optimization (SPO) becomes more and more important. SPO incorporates a variety of correction methods for radio frequency (RF)-related disturbances and mismatches, which should maintain a good system performance despite of nonlinearities and non-idealities of analog hardware elements. SPO is being carried out in the digital baseband (BB) but under conditions defined by the analog frontend (FE) configuration. By this way a higher precision is guaranteed than in case of a control loop in the FE.

Due to the existence of a great number of standards covering a variety of communication scenarios, reconfigurable multi-mode implementations for mobile terminals gain on popularity. The SDR approach [2] emerges as a potential answer to the trade-off between dynamic adaptation, reconfigurability and technical feasibility. Unlike many standard dependent operations (i.e. transmission techniques, modulation, coding), compensation of RF-related effects is primarily determined by the physical nature of the phenomena, and therefore predestinated for a joint implementation. In case of a transceiver supporting WLAN and UMTS, several SPO methods have been studied in order to achieve best possible performance of the complete system.

Orthogonal frequency division multiplex (OFDM) based IEEE 802.11a and code division multiply access (CDMA) based UTRA frequency division duplex (FDD) represent two different wireless systems using entirely different air interface technologies. Despite of the differences, it is highly desirable to

have an intelligent transceiver that can work seamlessly on both systems. It is also feasible to involve particularly IEEE 802.11a and UMTS because of their complementary character: wireless local area network (WLAN) can provide high data rate in a stationary hot-spot situation and UMTS will take over if high mobility is in demand.

Since the feasibility of an SDR supporting UMTS and WLAN is beyond controversy as far as market relevance and application areas of both systems are concerned, particular architectures and implementation solutions for the target system must be studied (compare [3]).

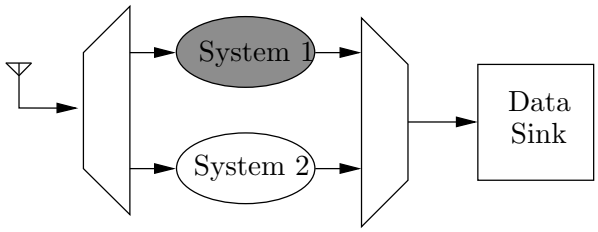
2.1. General Concepts in Multi-standard Radios

The variety of communication systems existing today, with their different applications, coverage areas, data rates, etc, raise the question about the possibility of having multi-standard transceivers that are capable to operate in any communication system, at any time. These super-transceivers would definitely give the users another reality of mobility and flexibility. In addition, from the network point of view, the operators would also win another perspective in the management of their links and services. However, the provisioning of such a multi-standard scenario is not a trivial task and is currently a diffused topic of research. It comprehends work on the necessary network procedures (inter-system handover, inter-connection between systems, etc) and the development of multi-standard transceivers.

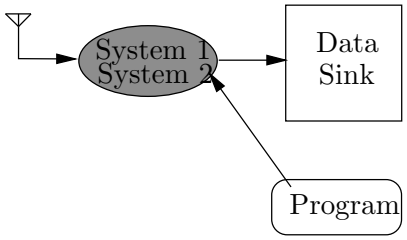
In the present chapter the multi-standard transceiver architectures are going to be discussed. The key-word when talking about multi-standard architectures is reconfigurability. The multistandard terminal must be able to be (re)configured according to the current application scenario. It should not be forgotten that to keep the implementation convenient the existing hardware resources must be as fast as possible [4]. In addition, the reconfiguration procedure (intersystem-handover) have to be as fast as possible. Basically, there are three types of reconfiguration architectures shown in Fig. 2.1.

2.1.1. One-Bit Reconfiguration

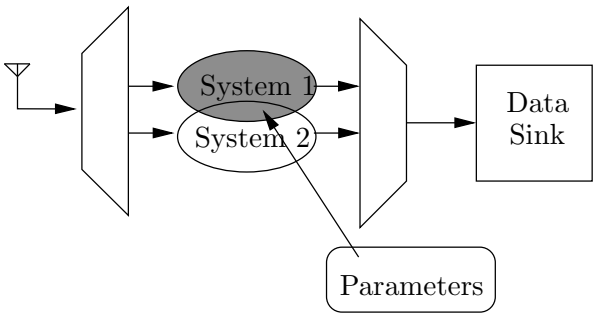
This reconfiguration scheme requires an independent baseband implementation for each standard. The incoming data stream is multiplexed to the dedicated baseband processing chain and the processed data is given back to the data sink. In this case, the amount of information needed for recon-



(a) One-Bit Reconfiguration



(b) Software Defined Radio



(c) Software Reconfigurable Radio

Fig. 2.1. Reconfigurable architectures

figuration is at the minimum of one single bit. However, this approach fails in sharing the existing hardware resources and for this reason is inadequate for mobile devices where the power consumption and area play an important role.

2.1.2. Software Defined Radio

This is the most flexible way to provide reconfigurability to the multi-standard transceiver. Here, (re)configuring the device has the meaning of (re)programming the device to the various standards. The target of this design-philosophy is to develop the transceiver architecture in such a way that its operations and functions can be represented by programs that run in a hardware platform [5]. This hardware platform must be able to cope with the different transmit and receive algorithms and thus has to provide sufficient processing power and communication bandwidth. Therefore, high-bandwidth communication systems such as 54 Mbit/s WLAN would require a massively parallel implementation of the up-to-date microprocessor and DSP resources in order to fulfill the performance requirements. This would lead to high power supply consumption and area overhead, making this approach uninteresting for mobile terminals. However, this is a long term tendency in wireless world.

2.1.3. Software Reconfigurable Radio

In this approach [6], the similarities and differences between the standards will be firstly identified and parameterized. Then, the basic algorithms underlying the systems are divided in classes according to their properties. Dedicated hardware will be now developed for the required classes of algorithms and the differences between the systems can be accommodated by reconfiguration based on the defined parameters.

The last two architectures are somewhat similar. The software reconfigurable radio is a simplified version of a software defined radio architecture. However, in recent publications the term software defined radio is used for both architectures.

2.2. RF Receiver Requirements

2.2.1. UMTS FDD

In this section four third generation partnership project (3GPP) front-end test cases are discussed briefly [7]. Based of these examples, it is demonstrated how RF key parameters can be derived from the 3GPP specification. The complete set of RF specific test cases for the 3GPP FDD mode can be found in [8], [9], [10] and is further discussed in [11].

In Tab. 2.1, common terms from the 3GPP specification used in the following section are described. Unless otherwise stated, all parameters are specified at the antenna connector of the receiver. They are defined using the 12.2-kb/s down link (DL) reference measurement channel [8]. The total received powe spectrum density (PSD) $\hat{I}_{or}$ for all test cases described in the following is composed of the actual data carrying signal (DPCH) to be detected and the so-called common downlink channels (pilot channel, synchronization channel, etc.), necessary for establishing and maintaining a link between the base station and terminal. Therefore, DPCH_E_c is usually several decibels below $\hat{I}_{or}$.

Tab. 2.1. Common 3GPP Parameters

DPCH_E_c	Average energy per chip of a dedicated physical channel (DPCH)
$\hat{I}_{or}$	Received (DL) power spectral density measured at the UE antenna connector
I_{or}	Total DL transmit power spectral density at the base station antenna connector
I_{oac}	Power spectral density of the adjacent channel measured at the EU antenna connector
I_{ouw}	Unwanted signal power level
OCNS	Orthogonal Channel Noise Simulator, a mechanism used to simulate users or control signals on the other orthogonal channels of a DL

Reference sensitivity level test case

In 3GPP, the reference sensitivity is the minimum receiver input power measured at the antenna port at which the bit error rate (BER) does not exceed a value of 10^{-3}. This test case determines the tolerable noise figure (NF) of the receiver front-end. $\hat{I}_{or}$ and DPCH_E_c are -106.7 dBm/3.84 MHz and -117 dBm/3.84 MHz, respectively. The 12.2-kb/s reference measurement channel used for this test case has a symbol rate of 30 ks/s and an spread factor (SF) of 128, i.e., a spreading gain (SG) of approximately 21 dB. Let us assume that the required bit energy to interference PSD ratio $E_{b,req}/I$ is 5 dB [12], then the insertion loss (IL) for the baseband implementation is 2 dB, and that the coding gain (CG) is 4 dB (CG estimation is difficult for

the used convolutional coder; 4 dB seems to be rather conservative). The acceptable interference signal level after despreading (P_I) then results in

$$P_I = DPCH\_E_c + SG + CG - \frac{E_{b,req}}{I} - IL. \tag{2.1}$$

Inserting the above given values, we have P_I=-99 dBm. This leaves a margin for the front-end NF of

$$NF = P_I - 10\log(kTB) = -99 \text{ dBm} + 108 \text{ dBm} = 9 \text{ dB} \tag{2.2}$$

with the Boltzmann constant k, the ambient temperature $T = 300$ K, and the bandwidth $B = 3.84$ MHz.

Adjacent channel selectivity test case

Adjacent channel selectivity (ACS) is a measure of a receiver's ability to receive a W-CDMA signal at its assigned channel frequency in the presence of an adjacent channel signal at a given frequency offset from the center frequency of the assigned channel. ACS is the ratio of the receive filter attenuation at the assigned channel frequency to the receive filter attenuation at the adjacent channel frequencies. The ACS has to be better than 33 dB. Simultaneously, the BER schould not exceed 10^{-3} for the following test parameters (see also Fig. 2.2): $\hat{I}_{or}$ and DPCH_E$_c$ are -92.7 dBm/3.84 MHz and -103 dBm/3.84 MHz, respectively. The same reference measurement channel with a symbol rate of 30ks/s and SG of 21 dB is used as in the reference sensitivity level test case. The PSD of the adjacent channel signal ±5 MHz away from the wanted channel is I_{oac}=-52 dBm/3.84 MHz. The signal levels for the ACS test case are summarized in Fig. 2.2.

$$P_I = DPCH\_E_c + SG + CG - \frac{E_{b,req}}{I} - IL = -85 \text{ dBm}. \tag{2.3}$$

If the adjacent channel interference signal is treated as Gaussian noise-like interference, the required ACS can be derived to be

$$ACS = I_{oac} - P_I = -52 \text{ dBm} + 85 \text{ dBm} = 33 \text{ dB}. \tag{2.4}$$

Intermodulation test case

For the intermodulation test case, two types of interferers are specified: a continuous wave (CW) interferer (I_{ouw1}) and a W-CDMA interference signal (I_{ouw2}). Both interferers have a power of 46 dBm, with the CW sig-

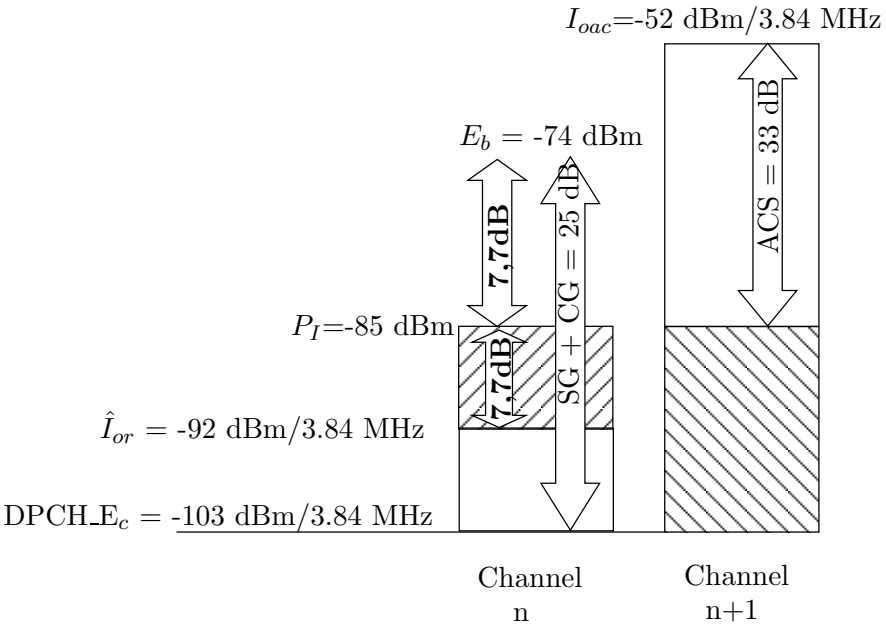


Fig. 2.2. Signal levels for the ACS test case

nal spaced 10 MHz away from the wanted signal and the modulated interferer having a spacing of 20 MHz. The power of the wanted channel is DPCH_E$_c$ =-114 dBm/3.84 MHz and $\hat{I}_{or}$ =-103.7 dBm/3.84 MHz. The modulated interference signal consists of the necessary common channels for any connection and 16 dedicated data channels with uncorrelated user data and the channelization codes for data channels are chosen to optimally reduce the peak-to-average ratio. These test-case conditions are illustrated in Fig. 2.3.

The sum of both interfering signals is transferred by means of a third-order nonlinearity into the desired channel. Therefore, this test case defines the required input intercept point of third order (IIP3) of the receiver. The acceptable noise-plus-interference level $P_{N,I}$ in the desired channel must not exceed -96 dBm/3.84 MHz if we assume a combined spreading gain of 25 dB. Before determining the required IIP3, we have to assign the total noise-plus-interference power $P_{N,I}$ to their sources. According to [13], we assume the following: 50% noise power (-3 dB), 15% intermodulation power (-8 dB), 15% blocking from CW interferer (-8 dB), 15% blocking from modulated interferer (-8 dB), and 5% power from oscillator noise (-13 dB). Furthermore, we neglect second-order products. From these assumptions, we derive a tolerable level for the third-order intermodulation power of

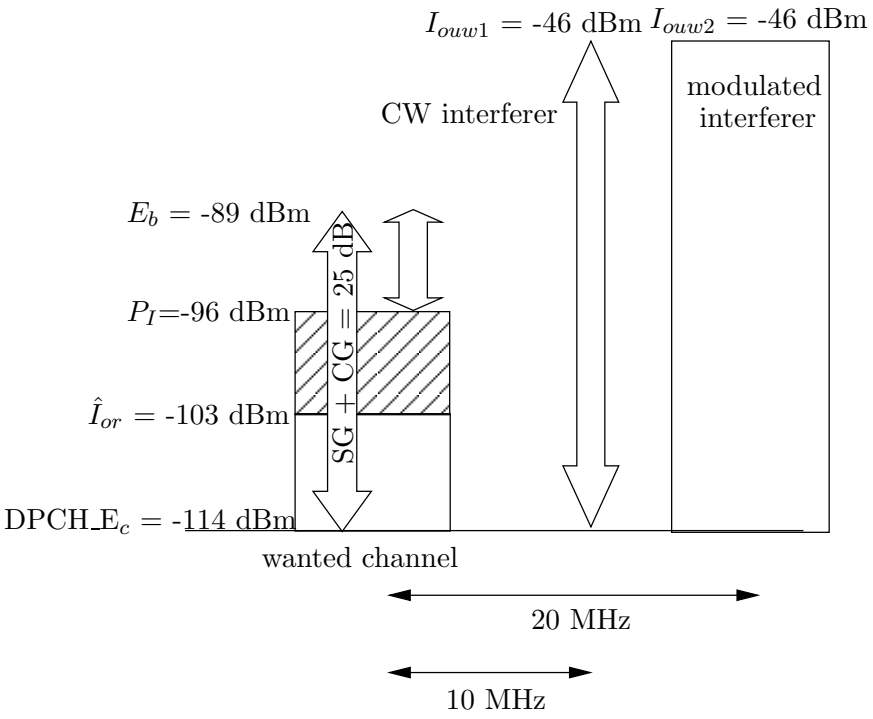


Fig. 2.3. Signal levels for the intermodulation test case

$P_{I,3} = -104.2$ dBm/3.84 MHz. The required IIP3 can be derived as

$$\text{IIP3} = \frac{2I_{ouw1} + I_{ouw2} - P_{I,3}}{2} = -16.9 \text{ dBm}. \tag{2.5}$$

The equations presented above exemplify how the signal levels are influenced by the despreading operation and by interference sources. Further estimations like the above-mentioned ones can be found in [13], [9]. However, one should keep in mind that these results can only serve as coarse estimates. What has been neglected in, e.g., the IIP3 calculation, is the fact that (2.5) is based on pure sinusoidal signals. However, the IIP3 of a nonlinear building block with respect to a W-CDMA signal is different from the IIP3 for sinusoidal signals [14]. A second point neglected in the above estimation is the fact that the modulated interference signal is a W-CDMA signal spread with other orthogonal variable spreading factor (OVSF) codes than the wanted signal. Depending on the preserved orthogonality between signals that are spread with different codes, this type of interference can behave strongly different to the Gaussian noise model, which is often used for CDMA signals. These simplifications make the above computation of the required IIP3 only to an estimation. Furthermore, the actual CG has to be

simulated to achieve realistic values. Altogether, this leads for certain test cases to the necessity of an accurate computer-aided system design using an appropriate combination of commercial baseband and microwave simulation tools like COSSAP, SystemC and ADS. These tools, in some cases, have to be backed up with self-written user-defined codes. The maximum input level test case is such an example.

Maximum input level test case

The maximum input level test case defines the maximum input power at the antenna port of the mobile station at which a coded BER of at least 10^{-3} must be achieved. According to the 3GPP specifications [8], the majority of the interference consists of a signal derived from a so-called orthogonal channel noise simulator (OCNS). This signal is used to simulate other user and control signals on the orthogonal channels in the downlink. $\hat{I}_{or}$ is specified to be -25 dBm/3.84 MHz with the wanted user signal level being 19 dB below. If we assume the interference coming only from the common channels and the OCNS and perform the same simplified estimations, as in the above-described test cases, we would require a combined spreading and CG of 26 dB to achieve the necessary E_b/I of 7 dB for a BER of 10^{-3}. However, the system simulations show different results [15].

It proves a fact that only with system simulation full and adequate receiver requirements can be obtained. In this case the 1-dB compression point (P_{1dB}) of the receiver has to be better than -20 dBm.

Other front-end specification

The font-end receiver specifications do not fully describe fully the receiver, because signal impairments play an important role, too. Impairments have their origin in hardware components. However, only system simulations that connect the hardware and software processing chain can define the maximum level of allowed signal impairments. Signal impairments are discussed later in this work. They are noticed here, to emphasize the need of system simulation in receiver design.

2.2.2. WLAN

The IEEE 802.11a standard [16] and Hiperlan/2 standard use the frequency bands shown in Fig. 2.4.

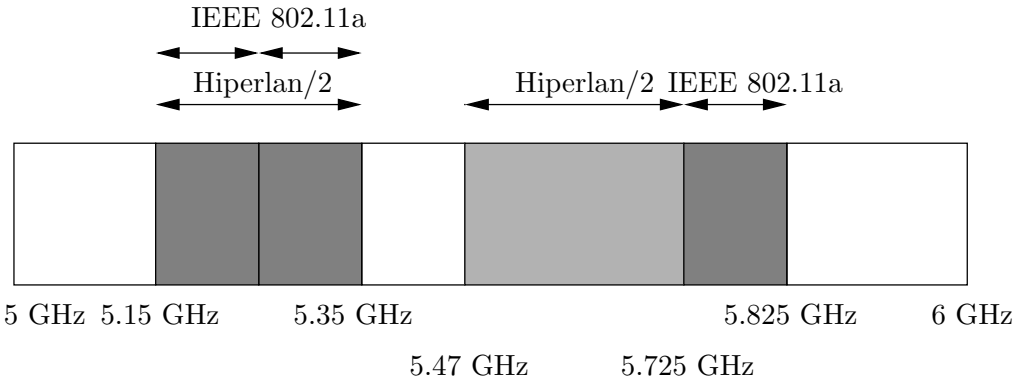


Fig. 2.4. Signal bandwidth for WLAN standards

Although the medium access control (MAC) layers for HiperLAN2 and 802.11a differ significantly, performance requirements for the RF signal processing blocks are quite similar [17], [18]. This commonality concerns similar frequency bands, data rates, and intended deployment scenarios. Consequently, it is possible for a single receiver design to comply with both sets of specifications. To determine the precise target values, we first compute the specifications for both HiperLAN and 802.11a separately, and select the more stringent of the two in every case. Here we reduce the specification set to frequency range, noise figure, maximum input signal level (or input-referred P_{1dB}), and limits of spurious emissions.

Wireless LAN systems require receiver architectures with wide dynamic range[19], [20], [21], [22]. When a transmitter and receiver are close to each other, the received signal strength can be as high as 20 dBm. A highly linear receiver is needed to accommodate such strong signals. On the other hand, the received signal can be quite weak due to fading. The receiver must be sensitive enough to detect signals as small as -148 dBm/Hz. (i.e., -74 dBm for a 24 MHz bandwidth signal [7]). To have a predetection signal-to-noise ratio (SNR) of at least 12 dB, the overall noise figure of the receiver must be better than

$$\mathrm{NF} = -148\ \mathrm{dBm/Hz} - 12\ \mathrm{dB} - (-174\ \mathrm{dBm/Hz}) = 14\ \mathrm{dB} \tag{2.6}$$

where 174 dBm/Hz is the available noise power of the source. This noise

figure is readily achievable in CMOS with a reasonably low power consumption.

Since the noise figure of the receiver is defined, other parameters can be derived. The P_{1dB} can be derived as maximum input power at the receiver antenna. This power is -20 dBm and -30 dBm for HIPERLAN/2 and IEEE802.11a, respectively. The receiver that can support both standards should have $P_{1dB} > -15$ dBm, with a small 5 dB margin.

Input intercept point of second order (IIP2) and third IIP3 can be derived from adjacent and non adjacent channel rejection specifications and blocking characteristics. The adjacent and non adjacent channels are shown in Fig. 2.5.

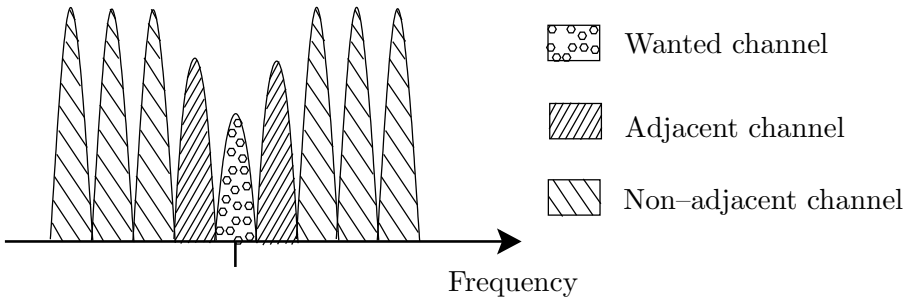


Fig. 2.5. Adjacent and non-adjacent channels

Since for both standards different blocking levels (BL) are defined as well as different channel rejection specification they have different requirements for the IIP2 and IIP3. It these parameters are defined as

$$\text{IIP2} = P_{in} + \text{SNR} + 2\text{BL} \tag{2.7}$$

and

$$\text{IIP3} = \frac{2P_{in} + \text{SNR} + 3\text{BL}}{2} \tag{2.8}$$

where P_{in} is the input power, 3 dB above sensitivity level, by definition. Taking the most restrictive values the receiver that supports both standards should have at least 6 dBm of the IIP2 and at least -7 dBm of the IIP3.

In both WLAN systems the phase noise of the oscillator is important, since the systems are wide band. This is because the phase noise of the receiver oscillator(s) is translated into the IF passband of the receiver by a strong accompanying signal. This phenomenon is called reciprocal mixing,

and is also described later in this work as an important source of signal impairment.

Typically, phase noise performances of the oscillators used in low cost WLAN equipments are in the order of -120 dBc/Hz at 1 MHz offset, with noise floors of around -140 to -150 dBc/Hz. In any system consideration, transmitter and receiver phase noise must be take into account, although for convenience in calculation, it is easier to assume a clean transmitter and degrade the receiver performance by 3 dB: this assumes equal phase noise performance between transmitter and receiver. However, the flexibility of WLAN systems means that precise calculations are impossible, but first order approximations are nevertheless useful in determining the magnitude of the effects of particular parameters.

From the view of a multiple signal environment, the dominant limiting parameter of receiver performance seems to be phase noise, rather than gain compression or intermodulation. Even where the phase noise performance of the receiver is adequate, the assumption that transmitters will be of equal performance is not necessarily valid when considering the multiplicity of offerings from various vendors.

The effects of phase noise in WLAN standards are devastating, insofar as these effects are bandwidth related. Considered WLAN systems will typically have a noise bandwidth in the order of 25 MHz, so that even a -140 dBc/Hz noise floor will produce noise at -66 dBc. Thus, a -20 dBm signal will lead to a noise floor some 12 to 15 dB above kTB level.

2.3. Reconfigurable RF Receiver Architecture

A high diversity of solutions regarding the analog processing of the RF signal is available on the market. The obvious trend is towards the reduction of the number of functional blocks needed and total integration of the analog part together with the baseband components on a single chip. This is the idea of the so-called system on a chip (SoC) approach.

The classical architecture used since decades is the heterodyne type presented in Fig. 2.6. The RF signal band is first down-converted to an intermediate frequency (IF) and in a second step down-converted to the baseband by the I/Q demodulator. On the one hand, due to the high requirements regarding particular components, especially an image reject filter, some components can hardly be integrated and have to be placed off chip. On the

other hand, heterodyne receivers offer advantages with respect to sensitivity, selectivity and intermodulation behavior over other solutions.

It is important, too, that such architectures can easily be implemented at very high RF frequencies. Therefore, the heterodyne architecture is often used for standards which work at relatively high frequencies like IEEE802.11a or HIPERLAN/2 ([23], [24]). Heterodyne architecture has also some limitations. However, they can be overcome. This architecture is not a good solution as far as reconfigurability is concerned, because external filters cannot be combined as bandwidth varies for the various modes. Fortunately, a lot of drawbacks can be limited, when the improved architecture [25] is used.

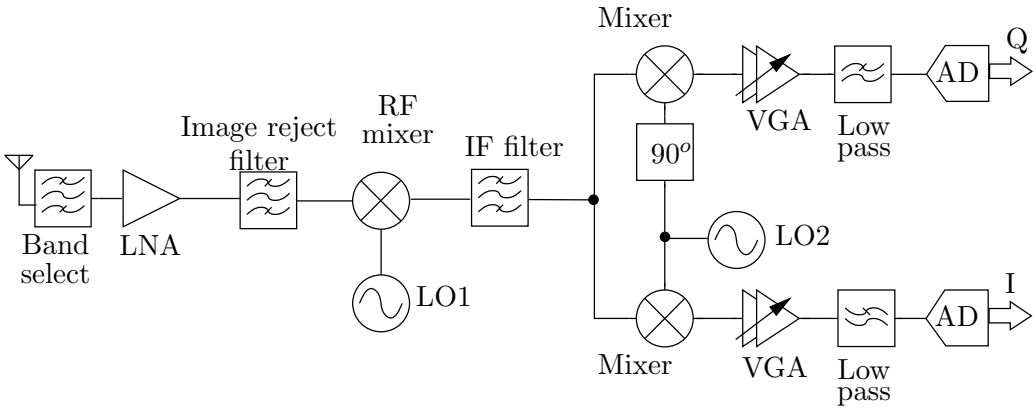


Fig. 2.6. Heterodyne receiver architecture

The homodyne receiver shown in Fig. 2.7 has gained in popularity in the recent years due to the overcoming of its principal challenges like the DC offset problem or the LO leakage [26], [27], [28]. In this receiver type, the RF signal channel is mixed with an LO frequency that is equal to the carrier frequency and thus, IF is equal to zero. For this reason this architecture is also called zero-IF (ZIF) or direct conversion receiver (DCR) [26]. The direct conversion architecture offers a number of advantages due to its simplicity, the possibility of a monolithic integration as well as the lack of image related problems [29]. Superior integration is given by the fact that no external IF filters are needed. It is also characterized by a smaller number of functional

blocks than the heterodyne receiver. Other resulting qualities are low power consumption, lower chip area and also lower production costs.

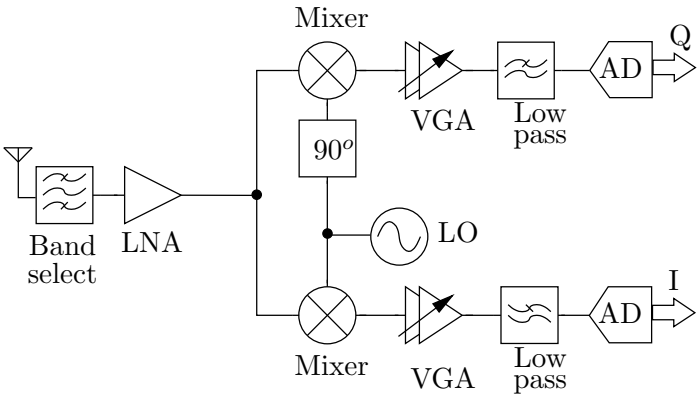


Fig. 2.7. Homodyne receiver architecture

Apart from the already mentioned advantages, the ZIF architecture has also some drawbacks. First of all, because of direct-conversion, the second order intermodulation (IP2) requirements for the receiver are high. Second, analog modules running at high frequencies suffer from I/Q imbalance. Moreover, low insertion loss passive filters are not available at baseband, and therefore active filters have to be used [30]. This leads to the fact that receiver noise can become a problem. These problems are rather uncritical for broadband baseband signals, so zero-IF is a very good candidate for UMTS or WLAN receivers (2 or 10 MHz bandwidth). All problems enumerated above are easier to overcome for lower RF frequencies, but the world tendency is to use DCR receivers even for high frequency [31], [32].

It is worth to mention that another receiver type, the low-IF architecture, gains more and more on significance. Although this architecture could also be regarded as a potential candidate for a multi-mode receiver, low-IF structures work well for rather narrowband baseband signals. As mentioned before, in our case, wide band signals are used in both standards.

Neither the homodyne nor the heterodyne architecture leads to the required reconfigurability with respect to integration level, power consumption, components design, etc., Therefore, after extensive studies of both architectures [33], we propose a reconfigurable solution shown in Fig. 2.8. A few months ago, similar solution has been published [24]. Although our solution was suggested almost three years ago, it shows advantages with respect to

component reuse. The objective drawback of our architecture is, that it has not been fully integrated, yet.

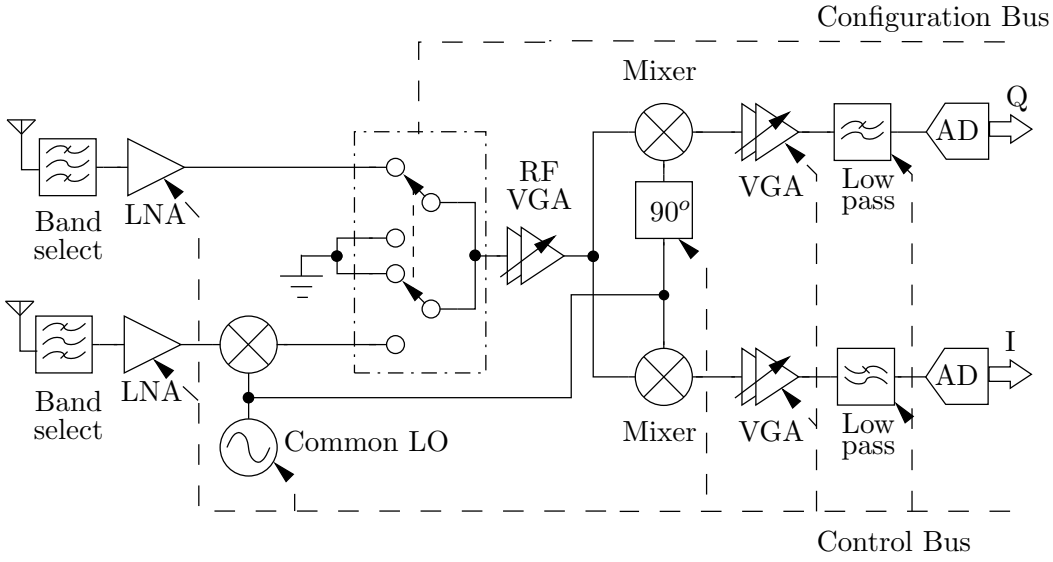


Fig. 2.8. Reconfigurable receiver architecture

The hybrid architectures combines both heterodyne and homodyne architectures [34]. The homodyne receiver is chosen for the UMTS and the heterodyne receiver for the WLAN standard. Such a hybrid solution does not support both standards at the same time, leading to a reconfiguration with downtime scenario. It means that to change the standard, power-off power-on sequence is needed.

In the above mentioned architecture, advantages of homodyne and heterodyne architectures are combined. Direct conversion receiver is used by the low frequency standard UMTS (2 GHz), therefore its well known drawback, I/Q imbalance, is decreased. On the other hand, high frequency standard WLAN (5 GHz) uses the heterodyne architecture, which gives good leakage rejection between RF and local oscillator (LO) port, and good selectivity.

This hybrid architecture provides the maximum number of reusable functional blocks by setting the IF band of the WLAN receiver very close to the RF band of the UMTS receiver. This way, the receiver chain behind the first WLAN mixer uses the same functional blocks for both standards. The active standard is chosen by the user through control and configuration buses. The configuration bus determines which signal path will be processed, whereas the control bus sets the functionality parameters for the implied functional blocks. The unused functional blocks, like the UMTS low noise amplifier

(LNA) in WLAN mode, are idled to save battery power. Both buses actually represent digital signals coming from higher layers of the BB part of the system.

Another advantage of this solution is the rational application of the LO frequencies. The heterodyne receiver uses the same LO frequency for both down-conversion stages, thus producing an IF at half of the RF input frequency [25]. That means a LO frequency in the range 2.5 – 2.9 GHz for WLAN. Moreover, in this solution the image band is centered around the zero frequency and is highly suppressed by the antenna, channel filter and LNA, therefore eliminating the need for external image reject filters. For the UMTS homodyne architecture, the LO frequency is, on the other side, in the range 2.1 – 2.2 GHz. This arrangement of LO frequencies offers the possibility of using a common reconfigurable LO, with a relatively narrow tuning range. To cover both standards, the voltage controlled oscillator (VCO) should work in the range from 2.1 GHz up to 2.91 GHz, giving a differential quadrature signal (90^o phase shift).

There are two commonly used ways for generating the quadrature signal. In the first method, the VCO is used, which works nominally at a frequency two times higher than needed [35], [36]. Then, the VCO output signal [37] is divided by two in a frequency divider which also introduces 90^o of the phase shift in the output signals. In our case, this method leads to the VCO operating in the frequency range from 4.2 GHz up to 5.82 GHz. Despite the two gaps in this range, the design of the such VCO can be challenging.

Therefore, a quadrature VCO (QVCO) is used [38]. This oscillator consists of two identical oscillators connected together in such way, that it generates the quadrature output signal. It is possible to cover the whole tuning range using only one reconfigurable QVCO [39].

The feasibility of a reconfigurable VCO is not the only argument for the half IF heterodyne receiver. Another advantage is given by the fact that the image band is centered around the zero frequency. This frequency band is highly suppressed by the antenna, channel filter and LNA, therefore eliminating the need for external image reject filters.

An advantage of the heterodyne WLAN receiver over the direct conversion solution is the fact that the LO – RF leakage can be rejected better by the LNA and antenna selectivity, avoiding the re-radiation problem that may occur in this way. There are, however, some problems that one must deal with in the heterodyne receiver. First, the flicker noise of the WLAN LNA is,

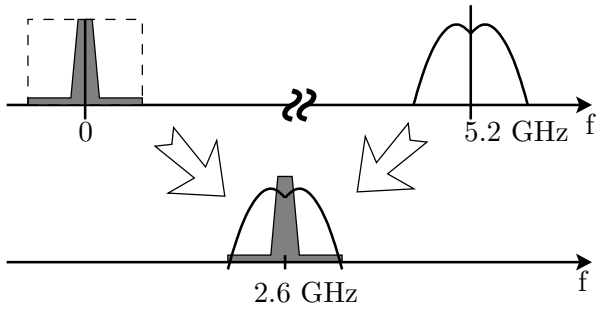


Fig. 2.9. Image band up-conversion for WLAN receiver

as depicted in Fig. 2.9, up-converted into the IF band and corrupts the signal. Depending on the transistor size, the flicker noise of the LNA may have a corner-frequency of several megahertz, so that the signal-to-noise (SNR) ratio of the WLAN signal despite its 20 MHz band may degrade considerably. In case of an active mixer topology, the mixer input stage will contribute along with the LNA to the flicker noise level. Therefore a resistive mixer should be the best solution in order to minimize the flicker noise level [40]. In this case a capacitive coupling between the LNA and the first WLAN mixer will solve the image problem. Another problem may appear in case of poor isolation between the LO and IF ports of the first WLAN mixer. In this case, the LO carrier may fall into the center of the IF band. As an effect, sensitivity problems may arise, making a double balanced mixer topology necessary to assure the best isolation values. Another problem which also concerns the I/Q demodulator mixer is the high linearity required for the mixer in absence of the channel select filter in the IF band. All these problems have to solved.

2.4. LNA Requirements

Having finished the studies on system simulations and system requirements, the system requirements have to be translated into specifications for each particular component [41]. It means, that all functional blocks shown in Fig. 2.8 has to be fully specified in respect to small signal, large signal and noise performance. Proposed reconfigurable architecture has two separate LNAs for UMTS and WLAN standards. The set of requirements for the UMTS LNA are collected in Tab. 2.2.

Tab. 2.2. Specification for UMTS low noise amplifier

Parameter	Value	Unit
Frequency	2110 – 2170	MHz
Input power level	-110 – -28	dBm
Input impedance	50	Ω
S_{11}	< -10	dB
Gain	13	dB
Noise Figure	< 3	dB
Input P_{1dB}	-17	dBm
IIP3	-7	dBm
Power dissipation	7	mW

2.5. RF Related Impairments

Despite of advanced sub-micron technologies and several particular solutions (c.f. [42]), the designer still has to struggle through trade-offs, technology constrains and increasing requirements. As an effect, the receiver components, even the best available, still show non-ideal behavior.

Since the receiver FE contains non-ideal components, the overall FE performance is affected [43]. Impairments appear at the receiver output signal, and handicap its decoding [44], [45].

This problem is ubiquitous and standard independent. However, the maximum level of impairments differs for various standards. In case of a reconfigurable receiver, the impairments should not exceed the limits defined for the more restrictive standard.

For further impairments analysis, it can be assumed that the hybrid receiver is a homodyne receiver, which receives a high frequency modulated signal $r(t)$. In this case, when the impairments of heterodyne architecture should be taken into account, the $r(t)$ signal has to be improved. Due to this assumption, impairments stem mainly from the common part of the hybrid receiver.

Once again, this part is followed by an appropriate down-converting stage in a heterodyne receiver, whereas it constitutes the only down-converting stage in a homodyne receiver. Since it can be found also in a Low-IF receiver architecture, this circuit depicts the common stage of every receiver used nowadays. Thus, next considerations are applicable to almost all receivers. The common part of the receiver depicted in Fig. 2.8 consists of the I/Q

demodulator (mixers, LO, phase shifter) and amplifiers with filters for each baseband analog branch. The LO produces a reference signal for the receiver and provides the channel select function. The phase shifter connected to the LO splits the LO signal into two signals with 90^o phase shift between them. The LO consist of a voltage controlled oscillator, which defines its frequency together with reference oscillator and a phase locked loop (PLL).

Since the power of the RF signal may vary in time, the gain of the variable gain amplifiers (VGA) depend on the RF input signal level. Therefore, the VGA delivers a constant power level at its output. Both filters restrict the frequency range of the baseband signal and filter adjacent, unwanted frequency bands and the interferers produced by nonlinearities in the receiver. These filters can also remove the DC component from the baseband signal.

Due to the non-deal components, the following impairments may occur: frequency offset, phase noise, direct current (DC) offset, I/Q imbalance and other imperfections.

Generally, the high frequency carrier modulated signal at receiver input can be expressed as [29]

$$r(t) = m_a(t)\cos[2\pi f_c + m_p(t)] \tag{2.9}$$

where f_c is the carrier frequency, $m_a(t)$ is the amplitude modulation and $m_p(t)$ is the phase modulation of the signal.

The signal

$$z(t) = m_a(t)e^{jm_p(t)} = z_I(t) + jz_Q(t) \tag{2.10}$$

contains all the information and it is called the complex envelope of the signal.

Due to quadrature demodulation, the received signal $r(t)$ is down-converted and divided into real and imaginary parts. The local LO signal $x_{LO}(t)$ can be simplified to:

$$x_{LO}(t) = \cos(\omega_{LO}t) - jg\sin(\omega_{LO}t + \phi), \tag{2.11}$$

where ϕ is the phase mismatch between I and Q signal and g the amplitude mismatch factor. $f_{LO} = \frac{\omega_{Lo}}{2\pi}$ denotes the LO frequency. Generally, the phase mismatch may have a considerable value, and g is bound to be very close to *one*.

In the following subsections, we focus on these impairments, show their sources and possible ways of avoiding them. We also search for implementation solutions which minimize these impairments. Unfortunately, not all

of them can be removed in the FE, thus the cooperation with the baseband (BB) in impairments cancellation is inevitable and necessary. This can be done if signal path optimization approach [46] is used.

2.5.1. Frequency Offset

In the UMTS and WLAN systems the information is transmitted using frequency channels. Each frequency channel is centered at a particular frequency (called carrier frequency) and occupies a predefined bandwidth. To retrieve the information placed in the channel, one has to shift down the carrier frequency to zero (2.9).

In order to receive information which is being transmitted through a channel with carrier frequency f_c at the antenna, the receive frequency has to be equal to f_c. Due to the non-ideal oscillators, obtaining these frequencies to be equal to each other is not a trivial task, and a sort of impairments called frequency offset occurs.

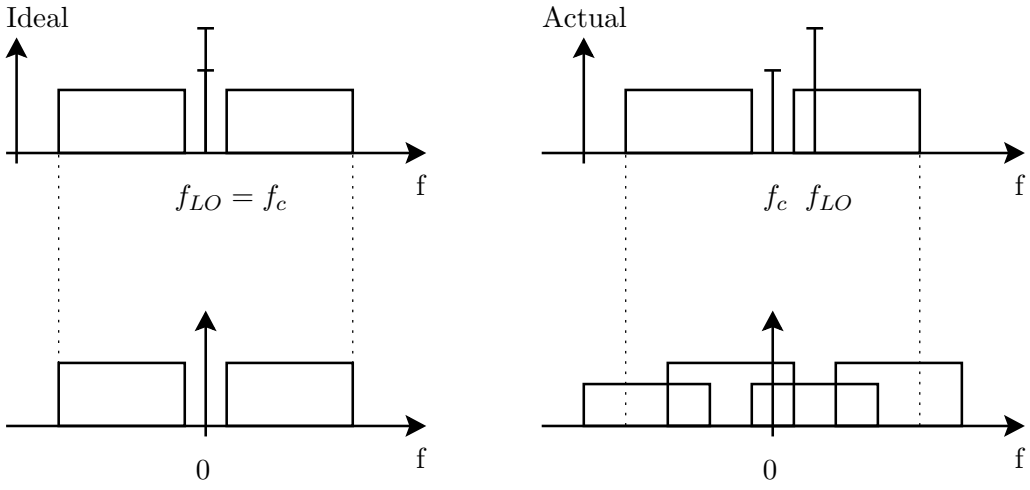


Fig. 2.10. Frequency offset phenomenon

According to that and (2.10), the BB equivalent signal at the FE output (BB input) can be expressed as

$$z_f(t) = z(t)e^{j(2\pi f_o t+\Theta)} + n(t)e^{j(2\pi f_o t+\Theta)} \tag{2.12}$$

where $f_o = |f_{LO} - f_c|$ for the homodyne case and $|2f_{LO} - f_c|$ for the heterodyne case. The $n(t)$ term denotes additive white Gaussian noise, and Θ stems from the phase difference between transmitted and received signal

and is responsible for twist of the constellation diagram. In other words, the constellation diagram rotates with angle velocity depending on the difference between the transmit and receive frequency.

In case of a WLAN system, the frequency offset disturbs the orthogonality between the subcarriers causing intercarier interference (ICI). The characteristics of the ICI are similar to white Gaussian noise and lead to degradation of the SNR.

Two frequency offset situations are depicted in Fig. 2.10. The first one shows an ideal case of $f_{LO} = f_c$, The other one shows he consequences of frequency offset in a pictographic, a bit exaggerated way.

The frequency offset is responsible for the rotation of the constellation diagram. When the frequency offset is constant, speed of rotation is also constant. This phenomenon can be also interpreted as an additional phase shift, which is added to the signal at each sampling time.

2.5.2. Phase Noise

In contrast to the frequency offset, which fluctuates rather slowly, quick changes of the LO frequency may also appear (variable f_o in (2.12)). Since the changes are random and result in unpredictable phase shifts, they are called phase noise. The LO generates also amplitude fluctuations, but the amplitude noise can be suppressed effectively by mixers as described before, so that in the end only the phase noise has a considerable influence on the quality of the FE signal path.

Two problems concerning LO phase noise should be taken into account. First, if any large blocking signal close to the wanted signal appears at the antenna receiver input, LO phase noise will appear at the IF due to a reciprocal mixing phenomenon. The signal to noise ratio will be automatically decreased by this way. Second, random changes of the LO frequency, even without the blocking signal, decrease the SNR, too. This case is also discussed in section 2.2.2

Phase noise induces reciprocal mixing at the receiver [47]. The receiver LO down-converts the RF carrier of the desired signal as well as the interferer, to a lower frequency. Ideally, the down-conversion should not spread the interference to the desired signal frequency. However, in the mixing process, phase noise in the LO modulates the interfering signal and can generate significant interference in the desired signal as shown in Fig. 2.11.

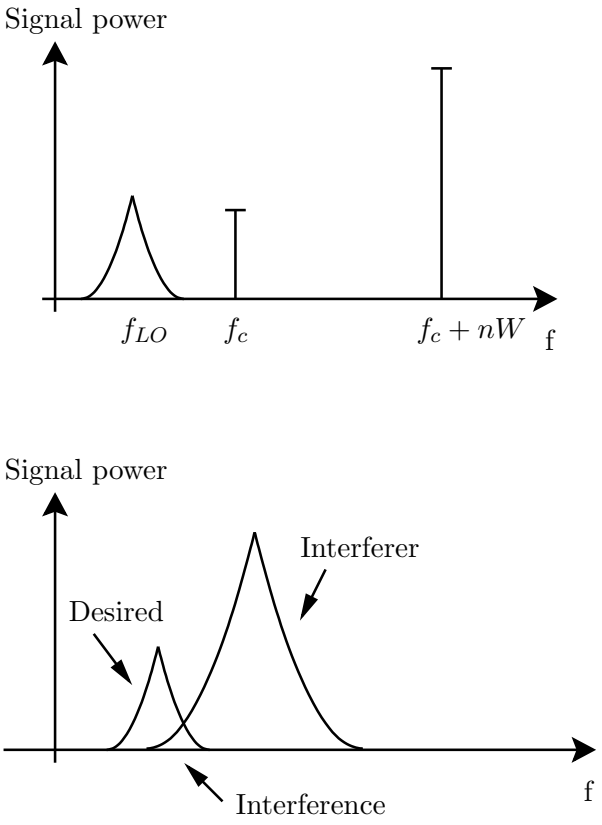


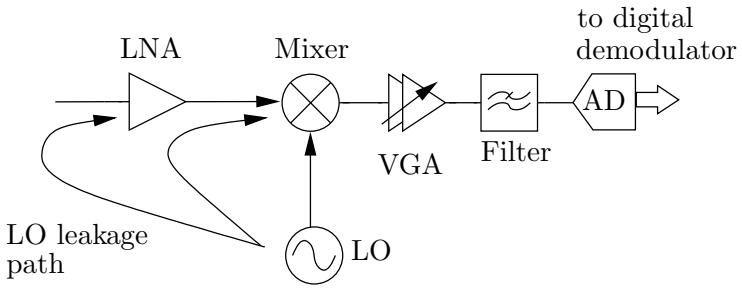
Fig. 2.11. Reciprocal mixing; the wanted signal suffers from significant noise due to the tail of the interference.

Deployment of a more precise LO is the only feasible way to limit phase noise in the FE. Actually, poor phase noise performance affects the FE functionality and triggers further problems.

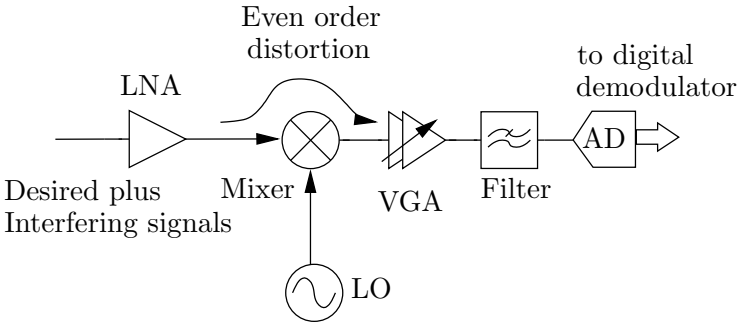
2.5.3. Direct Current Offset

The DC offset is an immediate consequence of the direct conversion process in zero-IF and near-zero-IF receivers [48]. It can be expressed mathematically, by adding a constant value to BB signal components (2.10). Basically, the DC offset can be classified into two types [49]:

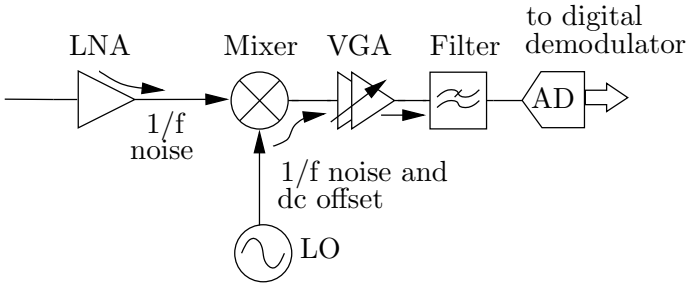
— Static type, caused by the LO leakage back into the antenna port of the transmitter or by circuit imbalances. This type is most common and varies only slowly. It is often considered fixed over a packet duration. Therefore, this type can be compensated simply by passing the signal through a running mean operation.



(a) LO leakage



(b) even order harmonic distortion



(c) 1/f noise leakage

Fig. 2.12. Sources of DC errors in homodyne receivers

— Dynamic type, resulting from the signal leakage from the RF input to the LO. Combined with the circuit imbalances and nonlinearity within the mixer, this type of DC offset causes second order intermodulation distortion within the mixer

Due to the substantial influence of the I/Q imbalance and the DC offset on the data transmission performance it is an important task to find an adequate solution to compensate the described mismatch. Fortunately that can be done in BB part of the receiver.

2.5.4. I/Q Imbalance

The main source of I/Q imbalance is the final stage of the receiver's analog part. Mixers, filters and amplifiers contribute to the I and Q mismatch, because of their non equal gains and group delays. Significant contributors may also be found in the digital part of the receiver. The main reason of phase imbalance is the phase shifter. Main amplitude imbalance contributor is a non equal gain in the I and Q signal paths. However, these impairments can also originate from the transmitter site, either a base-station or an access point in case of UMTS or WLAN, respectively.

An analytical description of the I/Q imbalance phenomenon may be obtained by processing (2.11) in a way described in [50]. It leads to the following form of the BB signal delivered by the receiver:

$$x(t) = z_I(t) + j\left(g\cos(\phi)z_Q(t) - g\sin(\phi)z_I(t)\right), \tag{2.13}$$

where $z(t) = z_I(t) + jz_Q(t)$ is the BB equivalent of the signal $r(t)$ received at the antenna.

Equation (2.13) describes I/Q impairments in a system with solely time domain signal processing. OFDM based systems must be considered separately.

Let $Z(f)$ and $X(f)$ denote the frequency domain representations of the original and filtered signal, respectively. The output signal $X(nf_s)$ may be expressed as a function of $Z(nf_s)$, where $f_s = \frac{1}{\Delta t_s}$ stands for the sampling frequency. After expressing $z(k\Delta t)$ as inverse fast fourier transformation (IFFT) of $Z(nf_s)$, inserting the result into (2.13) and computing fast fourier transformation (FFT), then splitting the exponential terms in their real and imaginary parts and taking advantage of the sum orthogonality, the following

equation appears:

$$\begin{aligned} X_n &= Z_n + \frac{1}{2}\left[(1 - g \cdot cos\phi)\left(Z_n - Z^*_{L-n+1}\right)\right. \\ &\quad \left. -jg \cdot sin\phi\left(Z_n + Z^*_{L-n+1}\right)\right], \end{aligned} \tag{2.14}$$

where $L - n + 1$ denotes a position symmetrical to n within the discrete fourier transformation (DFT) (or FFT) frame characterized by the length L. To simplify the equation, $X(nf_s)$ and $Z(nf_s)$ were referred to as X_n and Z_n, respectively.

Phase and amplitude impairments of an I/Q architecture are standard independent. However, OFDM based systems suffer more from imbalances than other communication systems due to a particular form of the distorted signal [51].

The differences between I/Q imbalance impact on a single carrier time division multiply access (TDMA)/frequency division multiply acces (FDMA) or CDMA system compared with an OFDM based one can be found in [51].

Equation (2.14) describes the influence of I/Q imbalance on multi carrier OFDM systems for $L > 1$ and single carrier systems for $L = 1$. Further observations may be derived from the analytical model for OFDM based systems:

— The FFT length has no relevance for I/Q imbalance,

— for each modulation symbol, the resulting constellation consists of the same number of points as the order of the modulation scheme because that is exactly the number of different Z^*_{L-n+1} signals that may exist,

— I/Q architecture is very sensitive to amplitude imbalance due to the $g \cdot cos\phi$ term,

— regular "chessboard-like" patterns appear for quadrature amplitude modulation (QAM) schemes due to their symmetry.

According to (2.14) the ranges of amplitude and phase imbalance values can be derived that do not lead to bit errors when no other influences are present. It can be seen that an error free range of phase imbalance values is larger than error free range of amplitude imbalance values. This important conclusion can be exploited by the SPO approach.

2.5.5. Nonlinearities

Nonlinearities are a general term for a whole class of impairments that affect the functionality of a receiver due to nonlinear characteristics of its components. The input power varies in time and in addition to the wanted

signal, unwanted signals like adjacent channels and sometimes also interferers appear at the antenna, too - producing a power level, which can cause nonlinear operation of the receiver. To avoid it, a high P_{1dB} of the receiver is needed, because small signal linearity measures (like IIP3) of the function block are in the linear relation. The IIP3 is around 10 dB and IIP2 is around 20 dB higher than P_{1dB} , without any linearization techniques. To define this receiver requirements some knowledge of the signal properties is necessary. Generally, each standard specifies maximum values of the signal at the receiver antenna, which shall be accepted without significant losses of the transmitted data. Additionally, the so-called back-off level defined as a minimum difference between maximum input power and P_{1dB} , has to be considered. Quite obviously, the larger the back-off, the more linear the receiver. In reality its value is limited, because high P_{1dB} requires more power and more chip area. Therefore, the back-off about 6-7 dB is very often used.

Another problem, which has to be considered, are third order nonlinearities. Since large adjacent channels accompany the received signal, nonlinearities of particular receiver stages (LNA, Mixers) become important. When large adjacent channels in the vicinity of the wanted signal appear at the antenna, the output signal, passing through the nonlinear functional block, contains also copies of the adjacent channels.

This phenomenon can negatively influence multiuser detection performed in the BB. Additionally, even without any strong interferer, when the input signal is larger than spurious free dynamic range (SFDR) of the receiver, the nonlinearity products will have values larger than the noise floor. It can be visible as the spectrum re-grow as depicted in Fig. 2.13. It can be seen that

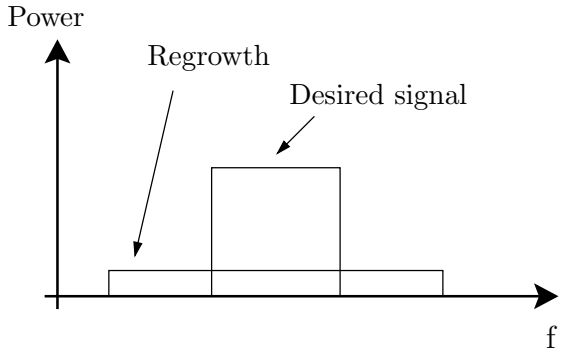


Fig. 2.13. Spectrum regrowth due to the third order nonlinearities

the original signal, which occupies only its own frequency band, regrows to adjacent frequency channels after passing through the nonlinear component. The same phenomenon occurs for the two adjacent channels. Therefore, if at least one of the adjacent channels is characterized by sufficient power, its copy will appear in the desired channel.

Chapter 3

Passive Devices

The performance of the RF integrated circuits is strongly connected with the quality of passive elements [52]. Good passive components are still a limitation of modern CMOS technologies. For example inductors of large values consume significant die area and have relatively poor quality factor Q.

Capacitors with high Q and low temperature coefficient are available, but their parasitics can not be neglected. Resistors with low parasitic capacitance and temperature coefficient are hard to come by. So design of RF integrated circuits is highly influenced by the passive devices.

In this section pads are also discussed. Obviously they are not basic devices, but they are passive and introduce significant contribution to the circuit.

3.1. Inductors

From the point of view of RF circuits the lack of good inductors is the shortcoming of the standard IC processes. Although active integrated circuits can sometimes synthesize the equivalent of an inductor, they always have higher noise, power consumption and distortion than real passive planar inductors.

3.1.1. Spiral Inductors

The widely used on-chip inductor is the planar spiral, which can be of different shapes, square, hexagonal, octagonal etc. The wiring of the spiral is implemented in the topmost available metal, sometimes are two or more metal layers strapped together and the connection to the center of the spiral is made with a cross-under of some lower level of metal. The inductance of such a spiral is a complicated function of geometry and accurate anylysis requires 3D-EM field solvers. However, using the libraries given in a Design

Kit from foundry, the designer has only to make choice of an appropriate kind of the inductor, and some parameters and the whole inductor parameters are self calculated by the design environment using the information provided by the model.

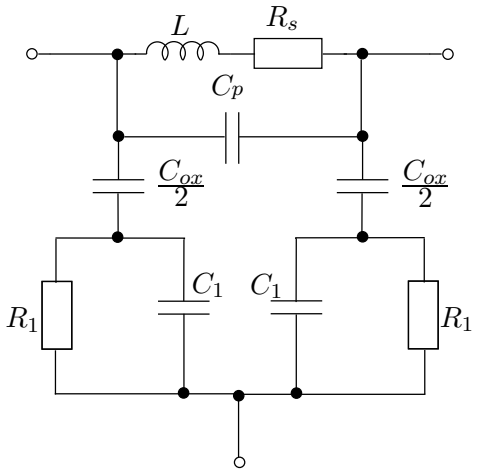


Fig. 3.1. Model for on-chip spiral inductor

To examine some important characteristic of the spiral on chip inductors simulation used an inductor taken from design kit has been performed. Simulation results are shown in Tab. 3.1. In the used design kit only the value of inductance L and number of turns n cab be specified by the designer. All other parameter are self calculated by the model.

Tab. 3.1. Simulated maximum Q and self resonant frequency f_{res} values for various inductors

Inductor		max Q	f_{res}
L [nH]	n		[GHz]
12	6.5	8.3 @ 1.5 GHz	2.6
10	6.5	8.7 @ 1.7 GHz	3.0
8	6.5	9.3 @ 2.0 GHz	4.0
6	6.5	10 @ 4.7 GHz	4.5
4	5.0	13 @ 3.3 GHz	6.2
2	4.25	15 @ 5.3 GHz	10.7
1	3.25	17 @ 8.5 GHz	18

In respect to the resonant frequency and maximum Q factor the best results shows the smallest inductor. Increasing the inductance leads to decreas-

ing the maximum Q, and resonant frequency, as well. For 2 GHz operation, maximum value of inductance used in the matching circuits is approximately equal 8 nH, and for 6 GHz 4 nH for this kind of inductor. For other purposes, like e.g., RF blocking larger values can be used.

The same value of inductance can be achieved by not only one combination of spiral diameter and number of turns. Tab. 3.2 shows maximum value of factor Q and resonant frequency f_{res} for an inductor with L=5 nH. Two values of n are extreme; smallest and largest realizable.

Tab. 3.2. Spiral inductors parameters with L=5 nH for different number of turns n

n	max Q	f_{res} [GHz]
3.25	14 @ 4 GHz	7.9
4.25	13 @ 4 GHz	7.8

From this investigation can be found, that increasing n lowers factor Q, but does not change the frequency at which maximum Q appears. Additionally, increasing n lowers the self resonant frequency of the inductor. Therefore, the conclusion is clear, one has to use inductors with as small number of turns as possible.

These on-chip spirals consume much area. Aside from large area another serious problem with the spiral inductors is their relatively large loss. The DC resistive losses together with the skin effect cause a nonuniform current distribution in a conductor at RF. The consequence is the reduction of the effective conductor cross-section, increasing the series resistance.

In addition to the series resistive loss, capacitance to the substrate is another problem of on-chip spirals. In silicon technology, there is a substrate near to the spiral and is fairly conductive, creating a parallel plate capacitor that resonates with the inductor. The resonance frequency of the LC combination represents the upper useful frequency of the inductor. The proximity of the substrate also degrades Q because of the energy coupled into the lossy substrate.

An additional parasitic capacitance is in shunt to the inductor that arises from the overlap of the cross-under from rest of the spiral. The model for on-chip spiral inductor is shown in Fig. 3.1. This model is symmetrical, even though actual spiral are not. The error introduced is in most instances negligible.

The series resistance R_s is proportional to the total length of winding and inverse proportional to the width of the interconnect and skin depth. The shunt capacitance C_p is proportional to number of turns, to the square of width of the interconnect and to the oxide capacitance. The capacitance C_{ox} is a parallel plate capacitor, with its capacitance between substrate and interconnection. The last element, C_1 denotes the substrate capacitance as well as other reactive effects associated with the inductor.

Q of the inductor can be optimized by removing the turns in the middle of the spiral as they contribute negligible to the total flux but contribute to the total loss. Furthermore, a pattern ground-shield [53] also helps to improve the Q of the inductor. A patterned ground shield prevents capacitive coupling to the lossy substrate while avoiding short-circuiting of the magnetic flux. Another advantage is that the shielding greatly reduces coupling of noise from the substrate to the inductor. The penalty is the reduction of the self resonant frequency of the inductor. In the layout of the final low noise amplifier shielded inductors are used.

3.1.2. Bond-wire Inductors

In addition to spirals, bond wires are frequently used to make inductors. Because standard bond wires are about 20 μm in diameter, they have much more surface area per length than the planar spirals and hence less resistive loss, and therefore higher Q values. The inductance of bond-wire can be approximately given by 1 nH/mm and resistance 0.1 Ω/mm.

The cross section o fa hypothetical bond wire between a chip and a test board shows Fig. 3.2. The length of the bond wire varies, thus the inductance varies also. It is the main problem of bond wires, lack of repeatability. Another problem associated with varying shape of the bond wire are additional parasitics. And last but not least, high values of inductance are rather not feasible, since the bond wire can act as an antenna.

3.2. MIM Capacitors

Metal insulator metal (MIM) type capacitors are illustrated in Fig. 3.3. They have lower parasitics than MOS capacitors. In the used technology,

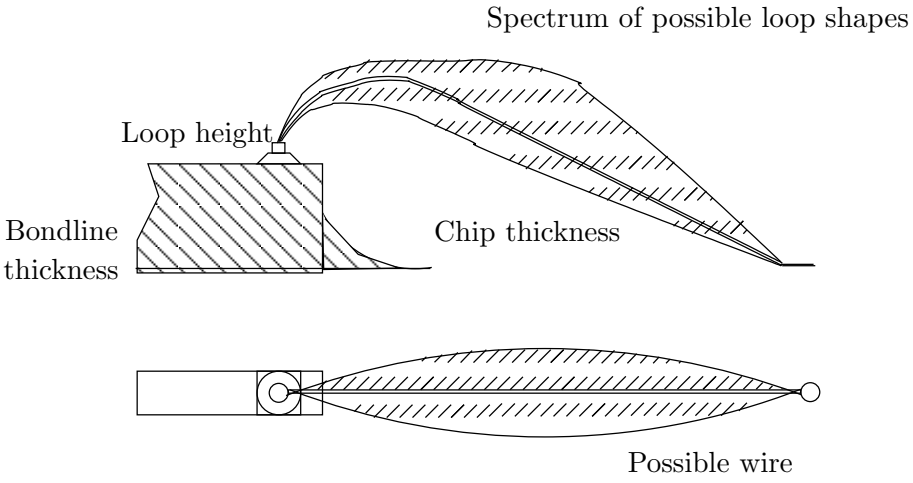


Fig. 3.2. Bonding wire

they are built using the additional dedicated metal layers. The capacitance is given by

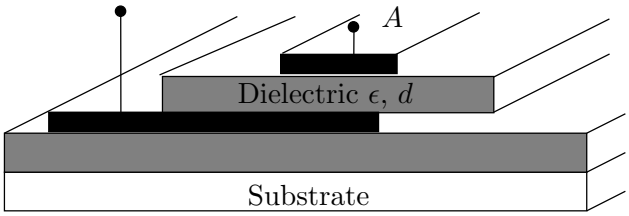
$$C = \frac{\epsilon_0 \epsilon_r A}{d} \tag{3.1}$$

where A is the plate area, ϵ_0 is the dielectric constant in the vacuum, ϵ_r is the relative dielectric material constant and d the distance between the metal plates. The capacitance per area is approximately 2 fF/μm^2.

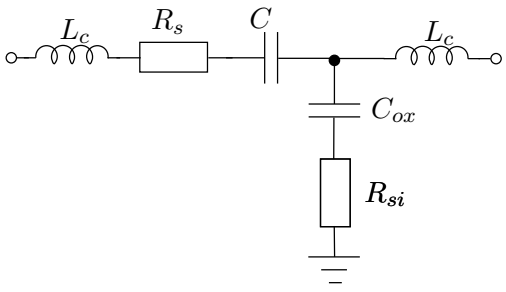
Good capacitors for RF application should have low voltage coefficients, good capacitor matching, precision control of capacitor values and small parasitic elements.

Traditionally parallel plate capacitance suffers from many such problems. One is the parasitic bottom plate capacitance which is frequently as large as 10-30 % or more of the main capacitance and often degrades the circuit performance.

Metal-insulator-metal (MIM) capacitors are very valuable in RF circuits. MIM capacitors can be used for coupling capacitances and bypass capacitances in RF circuits. They have good linearity and high dynamic range.In general, when MIM capacitors are used in RF circuits the dielectric loss must be extremely small and the series resistance of the wiring should be minimized.



(a) cross section



(b) electrical model

Fig. 3.3. MIM capacitor made on-chip

3.3. Resistors

There are relatively good resistor options in the standard CMOS (complementary metal-oxide silicon) processes. One possibility is to use polysilicon ("poly") interconnect material, since it is more resistive than metal. However, most poly these days have small resistivity. It stems form the fact, that poly material are used as a gate connection of the transistor, and decreasing its resistivity improves the noise performance of the transistor 4.3.2. The tolerance of the resistors is often poor and temperature coefficient depends on doping composition and is typically in order of 1000 ppm/°C. Unsilicided poly has higher resistivity, but higher tolerance, too. Poly resistors have a reasonably low parasitic capacitance per unit area and the lowest voltage coefficient of all the resistor material available in a standard CMOS technology. Resistors made from source-drain diffusion is also an option. The resistivities

and temperature coefficient are generally similar to those of silicided polysilicon with lower temperature coefficient associated with higher doping. There is also a significant parasitic capacitance and noticeably voltage coefficient. The former limits the useable frequency range of resistors while the latter limits the dynamic range of voltages that can be applied without introducing significant distortion.

3.4. Pads

In this work, grounded shielded (GS) pads shown in Fig. 3.4 are used for all signals, since only GS pads are available in used technology (HCMOS9, STM). The first metal acts as a shield connected to ground, and a top level metal layer acts as a pad connection [54]. For the GS structure, a grounded highly conducting plate is inserted underneath the pad metal plates to shield the upper bonding pad from the substrate. This technique has the advantages of excellent isolation [55] and lowered noise figure [55], [56], [57]. However, the insertion of the GS plate increases the pad capacitance. It results in a lower resonant frequency of the bond-wire-pad connection for a given inductance of the interface connection, especially for some technologies with a small number of metallization levels.

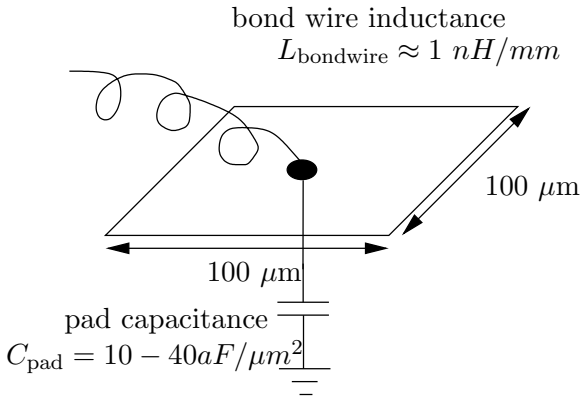


Fig. 3.4. Bonding pad together with connection

Typically, a GS bonding pad can have a pad capacitance as high as 0.35 pF for a typical pad size of 100 μm x 100 μm. Assuming a 2 mm long bond wire connected to the GS bonding pad, the inductance ($\approx$2 nH) of the bond wire will resonate with the pad capacitance at about 6 GHz as

$$f = \frac{1}{2\pi LC}. \tag{3.2}$$

The low resonant frequency can kill the high frequency connection of the bonding pad and the overall performance of the circuit. Hence, using these pads, the pad capacitance and bond wire inductance shall be kept low. However, as it is shown later in this work there are still more factors that should be taken into account especially in LNA design.

To overcome the mentioned issues with GS pads, depletion-insulation (DI) bonding pad structure can be used as shown in [58]. This kind of pads can be used for high frequencies [59].

Chapter 4

RF MOSFET Devices

4.1. Long-channel Regime

The physical structure of a MOSFET transistor is shown in Fig. 4.1. Electrically, the MOSFET has four contacts: a bulk, source, drain and gate contact [60], [61]. When the drain to source voltage V_{ds} is larger than zero, then the gate source voltage V_{gs} larger than the threshold voltage V_T forms a conducting channel between drain and source. Between the drain and source flows the current I_{ds}, which is dependent on the gate source voltage and the gate poly area (W, L).

MOSFETs exhibit three distinct regions of operation depending upon their bias condition. They are subthreshold, triode and saturation. In the first region, in simple MOSFET models, no current flows, and for RF design purposes it is not interesting.

The second mentioned region is triode or linear. A MOSFET operates in its triode when V_{gs} is large enough to guarantee the formation of an inversion layer the whole distance from source to drain [52]. It means that $V_{gs} \geqslant V_T$ and $V_{ds} \leqslant V_{gs} - V_T$, where V_{gs} is a threshold voltage. In this case the drain source current can be written as

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{4.1}$$

where W, L are device dimensions, C_{ox} is oxide capacitance and μ_n electron mobility.

Equation (4.1) shows, that in triode region drain source current is linear for small drain-to-source voltages. Thus, a MOSFET in this region behaves as a voltage controlled resistor.

In radio frequency applications, the MOSFET operates normally in its saturation region. In this case V_{ds} is high enough ($V_{ds} \geq V_{ds,sat} = V_{gs} - V_T$) so

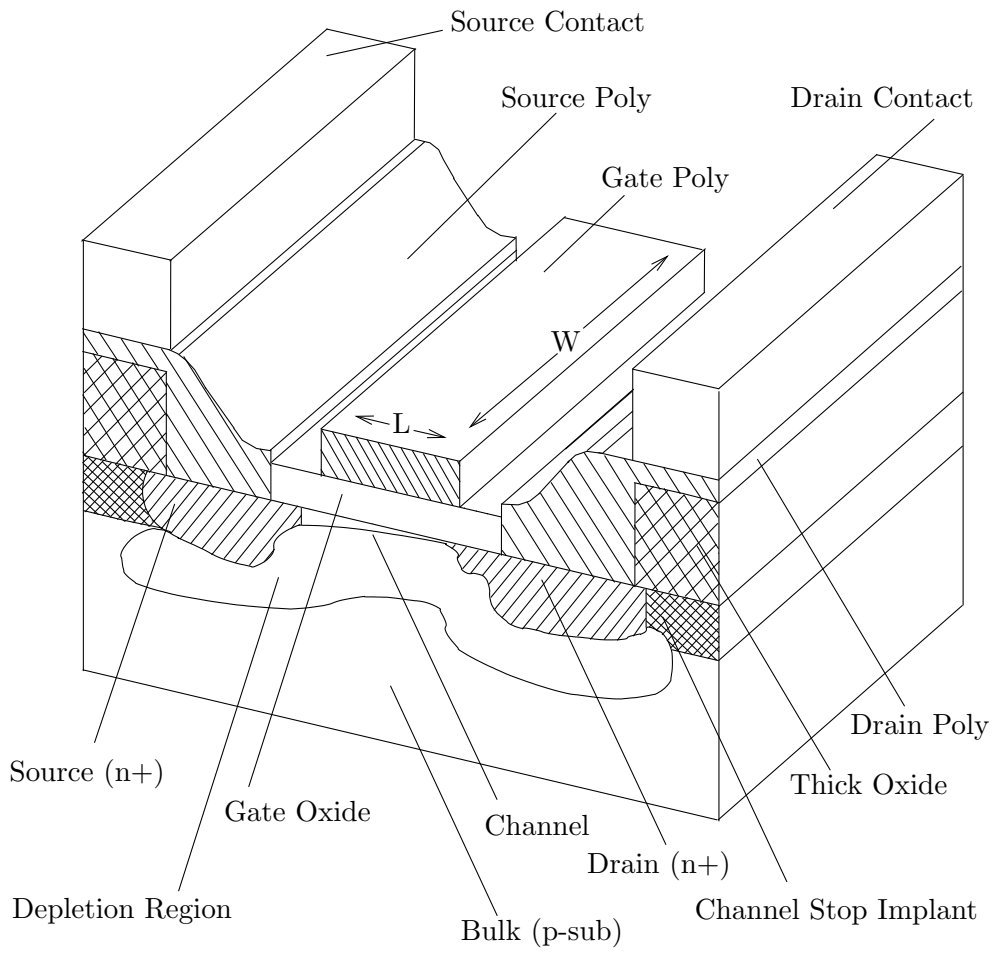


Fig. 4.1. Physical structure of a MOSFET

that the inversion layer does not extend the whole source to drain distance, the channel is said to be "pinched off", and any increase in V_{ds} increases the drain current only slightly. The reason that the drain current increases for increasing V_{ds} is because the depletion layer width increases for increasing V_{ds}.

This effect is called channel length modulation and is accounted for λ, the channel length modulation parameter. λ is in range from approximately 0.1 for short channel devices to 0.01 for long channel devices. Since MOSFETs designed for radio frequency operation normally use minimum channel lengths, channel length modulation is an important concern for radio frequency implementations in CMOS, especially for short channel devices commonly used in nowadays RF designs. When a MOSFET operates with a pinched off channel the drain source current can be written as

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\Big(V_{gs} - V_T\Big)^2\Big(1 + \lambda\Big(V_{ds} - V_{ds,sat}\Big)\Big) \tag{4.2}$$

Hence, in saturation, the drain current has a square-law dependence on the gate-source voltage and is independent of drain voltage if the channel length modulation is neglected.

The transconductance of such a device in saturation is easily found from differentiating the expression for the drain current with respect to V_{gs} (with neglecting the channel length modulation):

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_T) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}. \tag{4.3}$$

Transit frequency ω_T of a MOSFET transistor in terms of operating point, process parameters and device geometry can be written as [60]

$$\omega_T = \frac{3}{2} \frac{\mu_n (V_{gs} - V_T)}{L^2}. \tag{4.4}$$

Hence, ω_T depends on the inverse square of the length, and increases with increasing gate source voltage.

4.2. Short-channel Regime

As written above, channel lengths of state-of-the-art MOSFETs for radio frequency applications are very small. Therefore, various high-field effects become prominent at moderate voltages. These effects are: velocity saturation, threshold reduction, hot carriers. The primary high-field effect is that of velocity saturation.

4.2.1. Velocity Saturation

Note, that a short channel does not always refer to geometrical dimension. What really makes difference between long and short channel is the ratio $(V_{gs} - V_T)/L$ to E_{sat} – field strength at which the carrier velocity has dropped to one half of the value extrapolated from low-field mobility.

Velocity saturation has important practical consequences in terms of the current-voltage characteristics of a MOSFET acting in the saturation region. In particular, the drain current for a short channel device is given by [52]

$$I_D = \frac{\mu_n C_{ox}}{2} W \left(V_{gs} - V_T\right) E_{sat}. \tag{4.5}$$

It is visible, that in this case drain current is a linear function of V_{gs} and transconductance

$$g_m = \frac{\mu_n C_{ox}}{2} W E_{sat} \tag{4.6}$$

is constant over V_{gs} instead of linear, as it is for long-channel devices (4.3).

Moreover the transit frequency ω_T for the device in saturation region in short-channel regime can be written as

$$\omega_T = \frac{3}{4}\frac{\mu_n E_{sat}}{L}. \tag{4.7}$$

Equation (4.7) shows that the ω_T of a short-channel device depends on $1/L$, rather than on $1/L^2$ (4.4). Additionally, it does not depend on bias condition nor on oxide thickness.

4.2.2. Threshold Reduction

It is also called as drain-induced barrier lowering. A positive voltage applied to the drain terminal helps to attract electrons under the gate oxide region. This increases the surface potential and causes a threshold voltage reduction [62]. Since the threshold decreases with increasing V_{ds}, the result is an increase in drain current and therefore an effective decrease in the MOSFET's output resistance, beyond that associated with simple channel length modulation. Additionally, the drain-induced barrier lowering can cause dramatic increases in subthreshold current.

The effects of drain-induced barrier lowering are reduced in modern CMOS processes by using lightly doped drain (LDD) structures.

4.2.3. Hot Carriers

Velocity saturated charge carriers are often called hot carriers. Hot carriers can potentially tunnel through the gate oxide and cause a gate current, or they may become trapped in the gate oxide. Hot carriers that become trapped in the gate oxide change the device threshold voltage. Over time, if enough hot carriers accumulate in the gate oxide, the threshold voltage is adjusted to the point that analog circuitry performance is severely degraded.

The electric field near the drain can reach extraordinarily large values with moderate moderate voltage in short-channel devices. As a consequence, carriers can acquire enough energy between scattering events to cause impact ionization upon their next collision. Impact ionization by these hot carriers creates hole-electron pairs, and the holes are collected by the substrate while the electrons flow to the drain. The resulting substrate current is a function of the drain voltage, and this current represents an additional conductance term shunting the drain to ground.

Hot carriers effects degrade f_T and f_{max} of the transistor, third-order intercept point and the four noise parameters [63].

4.3. Radio Frequency Operation

MOSFET dimensions and physical layout are important determining factors for high frequency performance. As MOSFET operating frequencies approach several hundred MHz, the MOSFET can no longer be considered as a lumped device. The intrinsic and extrinsic capacitance, conductance, and resistance are all distributed according to the geometry and physical layout of the MOSFET. The distributed nature of the MOSFET operating at high frequencies is particularly important for the front-end circuitry in a receiver, such as in the low noise amplifier and first stage mixer input MOSFETs.

4.3.1. MOSFET Capacitances

Since the source and drain regions form reverse-biased junctions with the substrate, one expects the standard junction capacitance from each of those regions to the substrate. These capacitances are denoted C_{jsb} and C_{jdb}.

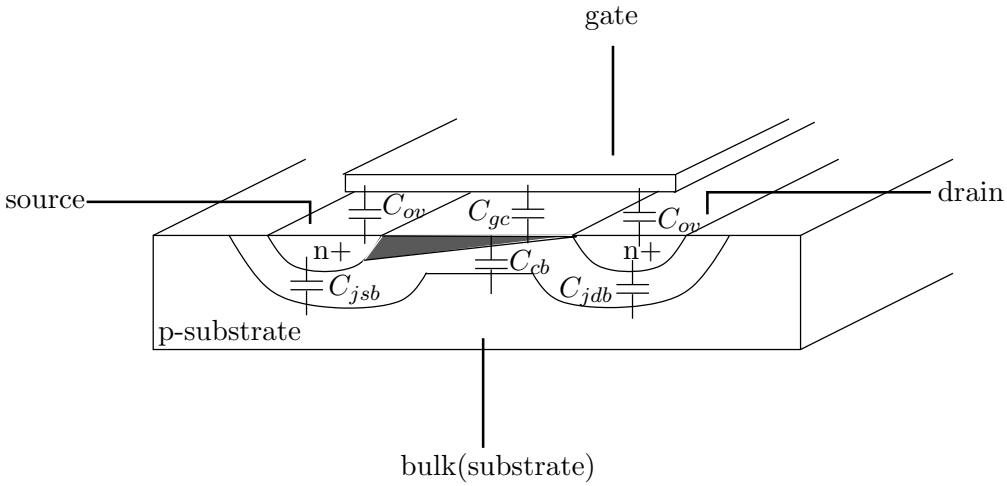


Fig. 4.2. MOSFET capacitances

There are also various parallel plate capacitances terms in addition to the junction capacitances shown in Fig. 4.2. The capacitor, called C_{ov}, represents

gate-source and gate-drain overlap capacitances. Another parallel plate capacitance is the gate-to-channel capacitance C_{gc}. There is also a capacitance between the channel and the bulk, C_{cb}, that behaves as a junction capacitance as well.

For compact modelling, the capacitances mentioned above (but also another ones) can be modelled as three capacitances [64]: C_{gs}, C_{gd} and C_{ds}. Capacitances C_{gs} and C_{gd} represent the spatial charge in the depletion region. In normal operation C_{gd} is much smaller than C_{gs}. Capacitance C_{ds} represents the capacitance between source and drain transistor areas.

4.3.2. Distributed Gate Resistance

In modern MOSFET technologies, the gate electrode is made of polysilicon [65]. Since its resistivity is relatively high its contribution to the transistor performance can not be neglected. Generally, the distributed gate resistance affects maximum frequency of oscillation (f_{max}), input referred thermal noise, and time response [66], but also input impedance and power gain.

Thermal noise contributions are discussed here. For an uniformly distributed MOS structure, it is possible to find an equivalent lumped resistance that can be placed in series with the gate terminal to represent the thermal noise of the polysilicon.

Consider the distributed model shown in Fig. 4.3, where the thermal noise of each resistor is modelled as a series voltage source. The drain noise current arises from both the gate resistance and the channel resistance. (The latter is described later in this chapter.) To calculate the equivalent lumped resistance, we determine the total drain noise current due to only the gate resistance and refer it back to the gate terminal of a lumped MOSFET as a voltage source (Fig. 4.3).

The drain current of M_1 resulting from the gate resistance is

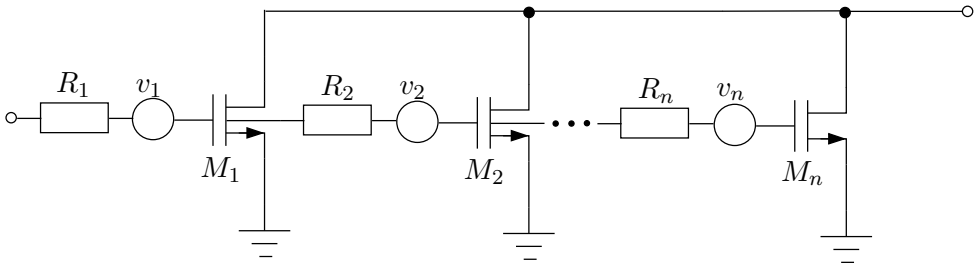
$$i_1 = g_{m1} v_1 \tag{4.8}$$

where v_1 is the noise voltage of R_1. Similarly,

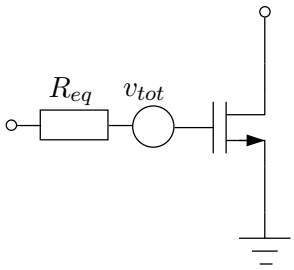
$$i_2 = g_{m2}(v_1 + v_2) \tag{4.9}$$

where v_2 is the noise voltage of R_2. Thus, for transitor M_j, we have

$$i_j = g_{mj}(v_1 + v_2 + \cdots + v_j) \tag{4.10}$$



(a) distributed model



(b) lumped model

Fig. 4.3. Circuit for calculating thermal noise generated by the gate resistance

and the total drain noise current is

$$i_{tot} = i_1 + i_2 + \cdots + i_n \tag{4.11}$$

$$= g_{m1}v_1 + g_{m2}(v_1 + v_2) + \cdots + g_{mn}(v_1 + v_2 + \cdots + v_n). \tag{4.12}$$

If $g_{m1} = g_{m2} = \cdots = g_m/n$, then

$$i_{tot} = \frac{g_m}{n}[nv_1 + (n-1)v_2 + \cdots + v_n)]. \tag{4.13}$$

Assuming $v_1, \ldots, v_n$ are uncorrelated, we can express the mean square noise current as

$$\overline{i_{tot}^2} = \frac{g_m^2}{n^2}[n^2\overline{v_1^2} + (n-1)^2\overline{v_2^2} + \cdots + \overline{v_n^2})]. \tag{4.14}$$

If $R_1 = R_2 = \cdots = R_g/n$, then $\overline{v_1^2} = \overline{v_2^2} = \cdots = \overline{v_n^2} = 4kTBR_g/n$, where k is Boltzmann constant, T absolute temperature, and B is the bandwidth. Equation (4.14) then reduces to

$$\overline{i_{tot}^2} = \frac{g_m^2}{n^2}\frac{4kTBR_g}{n}[n^2(n-1)^2 + \cdots + 1] \tag{4.15}$$

$$= g_m^2(4kTB)R_g\frac{n(n+1)(2n+1)}{6n^3}. \tag{4.16}$$

As $n \to \infty$,

$$\overline{i_{tot}^2} = g_m^2(4kTB)\frac{R_g}{3} \tag{4.17}$$

which can be referred to the input as

$$\overline{v_{tot}^2} = \frac{\overline{i_{tot}^2}}{g_m^2} \tag{4.18}$$

$$= 4kTB\frac{R_g}{3}. \tag{4.19}$$

This relation indicates that, for noise calculation purposes, the distributed structure of Fig. 4.3 can be replaced with a single MOS device of transconductance g_m and a lumped gate resistance of $R_g/3$. In addition to v_{tot} given in (4.18), channel resistance of the transistor also contributes to the overall thermal noise. Therefore, the relative significance of the gate resistance can be determined by comparing $R_g/3$ with $1/g_m$, and the minimum number of finger can be obtained.

The gate resistance can be decreased further [65], when the gate of the transistor is contacted at both ends, as it is shown in Fig. 4.4.

In such a case the equivalent resistance is given by:

$$R_g = \frac{1}{12}\left[\left(2n + 3 + \frac{1}{n}\right)r + \frac{1}{n}R\right] \tag{4.20}$$

where R is the resistance of a gate finger and r is the interconnect resistance. The interconnect resistance r can be neglected [65], since it is routed on a metal layer. However, interfinger capacitance of the gate strips affects the noise and RF performance of the device [67].

4.3.3. Channel Resistance and Transit Time Effects

At radio frequencies, due to the finite charging time of the carriers in the inversion layer, the gate impedance performs a remarkable phase shift from its purely capacitive value at lower frequency [68]. The channel charging resistance R_i (assumed to be noiseless) is used to account for this non-quasi-static

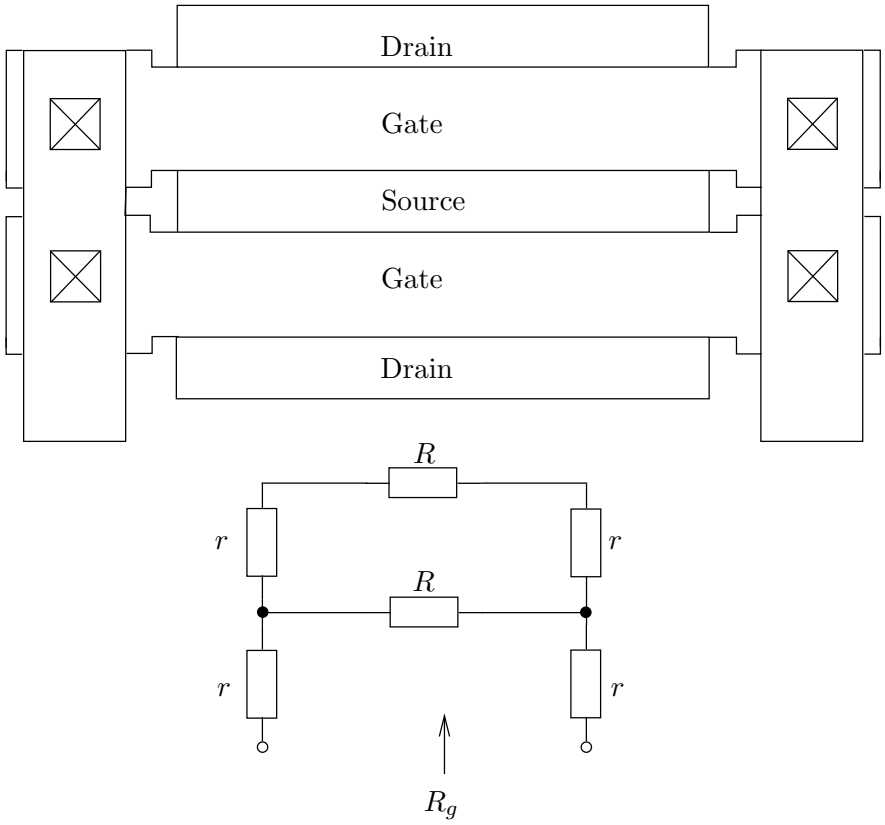


Fig. 4.4. Distributed gate resistance of a MOSFET, r-interconnect resistance, R-finger resistance [65].

behavior along the channel length. It can be shown [60] that the channel charging resistance is inversely proportional to the MOSFET drain conductance,

$$R_i \approx \frac{1}{k g_{d0}}, \tag{4.21}$$

where g_{d0} is is the value of g_{ds} evaluated at zero V_{ds}.

For long channel devices, with the distributed nature of the channel resistance between the source and drain taken into account, the constant of proportionality, k, was shown to be equal five. Measurements of short channel devices indicate that the proportionality constant can go down to one.

Unlike the noisy gate-poly parasitic resistance R_g, the channel resistance R_{ch} cannot be reduced using layout techniques [69]. The channel charging resistance of a MOSFET is important because it strongly influences the input conductance and the forward transconductance parameters of the device. Both the input conductance and the forward transconductance are monotonically decreasing functions of the channel charging resistance.

At high frequencies [70] the MOSFET must be considered as an RC distributed network, with the capacitive coupling to the gate representing the distributed capacitance and the channel itself representing the distributed resistance. This means that the high-frequency gate admittance Y_g of the device contains a conductive component g_g. This component is known as

$$g_g = \frac{\omega^2 C_{gs}^2}{k g_{d0}}, \tag{4.22}$$

where k has the same meaning as in (4.21).

4.3.4. Small-signal RF-model

A small-signal MOSFET transistor model is shown in Fig. 4.5. This model consist of either intrinsic or extrinsic components. The latter ones are L_g, R_g, L_d, R_d, L_s, R_s, and are connected with physical layout of a transistor. The designer has to minimize these elements, whenever the high RF performance is requested.

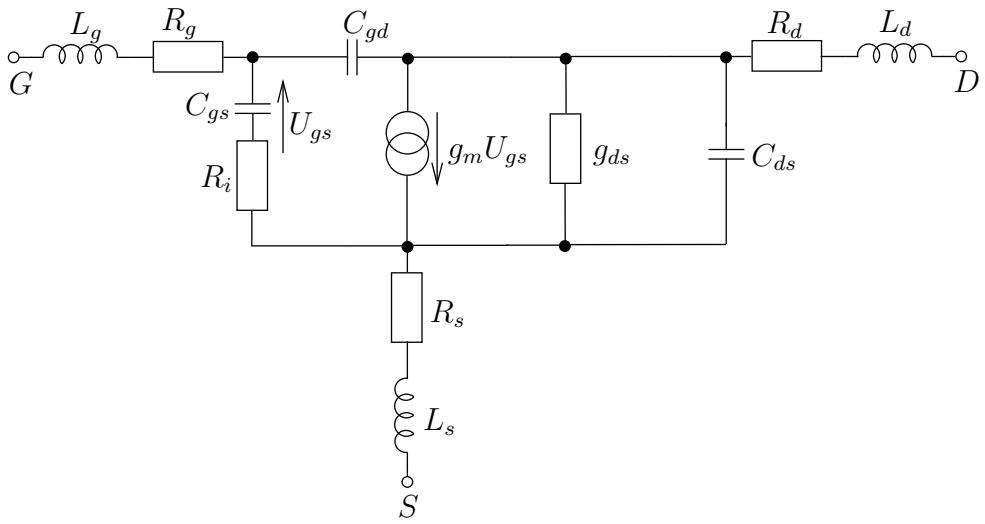


Fig. 4.5. Small-signal model of a MOSFET

4.3.5. Noise Model of a MOSFET

Noise characteristic of a MOSFET transistor plays an important role in the design of low noise circuits, particularly in low noise amplifier design.

Noise model of the MOSFET transistor is naturally connected with its small signal model. In RF community, the noise model presented in Fig. 4.5 is widely used, but with some simplifications described later in this text. In this case the capacitances C_{gd} and C_{ds} are neglected, since they do not affect noise performance significantly.

The noise of the intrinsic transistor can be described using two correlated noise sources, one in the gate circuit and one in the drain circuit.

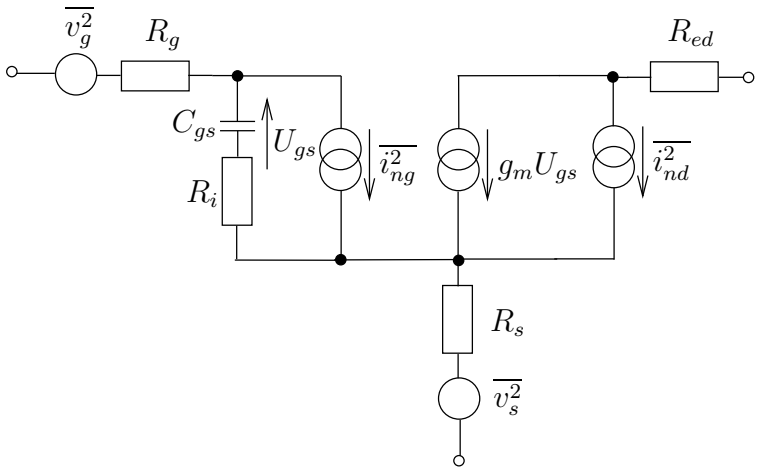


Fig. 4.6. Noise model of a MOSFET

The thermal channel noise is described as

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{4.23}$$

where γ is bias dependent parameter. The factor γ is an increasing function of V_{DS}, but a value of $\frac{2}{3}$ is often used for hand calculations and simple simulations. For short-channel devices γ is typically 2 - 3 times larger, but can be considerably larger [71]. Therefore, for low noise operation, the V_{DS} voltage shall be kept small. However, some research laboratories, e.g., Philips [72] prove, that γ is independent on the transistor length, and even for 0.18 μm transistors is still equal to $\frac{2}{3}$. For quasi-static MOSFET operation, $\overline{i_{nd}^2}$ is essentially independent on frequency.

The induced gate noise is described as [70]

$$\overline{i_{ng}^2} = 4kT\delta g_g\Delta f \tag{4.24}$$

where g_g is defined by (4.22) and δ is a bias dependent parameter typically greater than or equal to $\frac{4}{3}$ in long channel devices. Interestingly, the in-

duced gate noise is proportional to the square of the frequency. Clearly this expression cannot hold as the frequency becomes extremely large.

Although the spectral density of induced gate noise is not constant in frequency, it can be recast to the model in a form with a noise voltage source that possesses a constant spectral density. To derive this alternative model, transformation of the parallel network of C_{gs} and the g_g to the serial RC network shall be done, with the assumption of a large Q factor at the transistor input. In this case the serial resistance can be written as

$$r_{ge} = \frac{1}{g_g}\frac{1}{Q^2+1} \approx \frac{1}{g_g}\frac{1}{Q^2} = \frac{1}{kg_{d0}} \tag{4.25}$$

and the equivalent series noise voltage source as

$$\overline{V_{ge}^2} = 4kTr_{ge}\Delta f \tag{4.26}$$

The gate noise is correlated with the drain noise, and the correlation coefficient is defined by:

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{nd}^2} \cdot \overline{i_{ng}^2}}} \tag{4.27}$$

It can be explained, because thermal noise within the channel produces both drain channel noise and induced gate noise. Since both the channel drain noise and the induced gate noise are generated by the same physical noise sources, they exhibit a degree of correlation. Correlation coefficient c for long channel transistors is equal $j0.4$, and according [72] this values is still valid even for short channel transistors.

To recapitulate drain and induced gate noise we put some numbers in the noise equations to emphasize important facts. Factor γ in drain noise (4.23) is assumed to be $\frac{2}{3}$ and then

$$\overline{i_{nd}^2} = 4kT\frac{2}{3}g_{d0}\Delta f. \tag{4.28}$$

It can be shown [73] that induced gate noise with correlation neglected can be axpressed as

$$\overline{i_{ngcor}^2} = \frac{(\omega C_{gs})^2}{g_{d0}^2}\overline{i_{nd}^2}. \tag{4.29}$$

Taking the correlation into account

$$\overline{i_{ng}^2} = 4kT|c|\frac{2}{3}\frac{(\omega C_{gs})^2}{g_{d0}}\Delta f = 4kT\frac{4}{15}\frac{(\omega C_{gs})^2}{g_{d0}}\Delta f. \tag{4.30}$$

Substituting (4.22) and assuming further long channel approximation

$$g_g = \frac{(\omega C_{gs})^2}{5g_{d0}} \tag{4.31}$$

in (4.30) leads to

$$\overline{i_{ng}^2} = 4kT\frac{4}{3}g_g\Delta f. \tag{4.32}$$

that is identical with (4.24).

In Fig. 4.5 there are also depicted two additional thermal noise sources connected with parasitic resistance; the gate resistance R_g and the source resistance R_s. Thermal noise connected with the resistance is defined by the Nyquist theorem

$$\overline{v_n^2} = 4kTR\Delta f \tag{4.33}$$

Note, the resistance R_d has no thermal noise connected with it, since its contribution can be neglected.

4.3.6. Noise Matching

Classical noise matching analysis is applicable to the MOSFET shown in Fig. 4.7. These methods are directly applicable when all MOSFET internal sources are referred to the input. For the common source MOSFET configuration shown in Fig. 4.7, the input referred noise sources v_n and i_n are given by [60]

$$v_n = v_g - \frac{i_{nd}}{g_m} + (R_g + R_i)i_{ng} - j\frac{f}{f_T}(R_g + R_i)i_{nd} \tag{4.34}$$

and

$$i_n = i_{ng} - j\frac{f}{f_T}i_{nd} \tag{4.35}$$

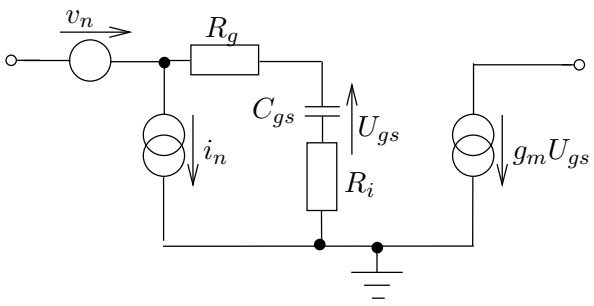


Fig. 4.7. Equivalent noise model of a MOSFET

The noise performance of a transistor with source impedance $Z_s = R_s + jX_s$ is fully described in terms of four noise parameters:
— the minimum noise figure F_{min},

— the equivalent noise conductance G_n,
— optimum driving resistance R_{opt},
— optimum driving reactance X_{opt}

Then, the noise parameters of the MOSFET can be found as

$$G_n \approx \left(\frac{f}{f_T}\right)^2 \gamma g_{d0} F_1 \tag{4.36}$$

$$R_{opt} \approx \sqrt{(R_g + R_i)^2 \left(\frac{f_t}{f}\right)^2 \frac{R_g F_4}{\gamma g_{d0}} + \left(\frac{f_t}{f}\right)^2 \frac{F_2^2 F_5}{\gamma g_{d0}^2 F_1}} \tag{4.37}$$

$$X_{opt} \approx \frac{F_2}{2\pi f C_{gs}} \approx -F_2 X_{in} \tag{4.38}$$

$$F_{min} \approx 1 + 2G_n(R_{opt} + R_g + R_i) \approx 1 + 2F_3 \frac{f}{f_T} \sqrt{\gamma g_{d0} R_g} \tag{4.39}$$

The factors $\{F_1, F_2, F_3, F_4, F_5\}$ result form algebraic manipulations of (4.34) and (4.35). If induced gate noise is ignored, then $\{F_1, F_2, F_3, F_4\}$ are qual one, otherwise they are less than one. Contrary, the fifth factor, F_5, is equal to zero if induced gate noise is ignored, and equal to one if induced gate noise is included. Two important facts stem from these considerations

— the minimum noise figure is proportional to $\sqrt{R_g}$. Therefore to realize a low noise figure the intrinsic gate resistance must be made as small as possible.
— the minimum noise figure is inversely proportional to $\sqrt{g_m}$, with assumption that g_{d0} is equal to g_m. Hence, increasing the g_m of devices decreases the minimum noise figure. Since both g_m and γ are functions of the transistor bias conditions, an optimum biasing point can be found that gives the lowest minimum noise figure.

The transistor noise factor is then

$$F = F_{min} + \frac{G_n}{R_s} |R_s - (R_{opt} + jX_{opt})|^2 \tag{4.40}$$

The noise performance of a two-port and is usually characterized by the noise factor (F) or noise figure ($NF = 10 \log F$). At one frequency, the noise factor of a linear circuit shows a parabolic dependence on the source impedance.

However, admittance transistor representation is more convenient, thus the four noise parameters are often defined in following way

— F_{min} – minimum noise factor,

— R_n – equivalent noise resistance,

— G_{opt} – optimum source conductance,

— B_{opt} – optimum source susceptance,

where the optimum source admittance is defined by $Y_{opt} = G_{opt} + jB_{opt}$.

When the two-port is driven by a single source with internal admittance $Y_S = G_s + jB_s$, its actual noise figure F can be written as

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2 \tag{4.41}$$

When the distributed effects are neglected, four noise parameters can be derived as follows [74]:

$$F_{min} \approx 1 + \frac{f}{f_T}\sqrt{\gamma\delta\zeta(1-|c|^2)} \tag{4.42}$$

$$R_n \approx \frac{\gamma g_{d0}}{g_m^2} \tag{4.43}$$

$$G_{opt} \approx \frac{g_m\omega C_{gs}}{g_{d0}}\sqrt{\frac{\delta\zeta(1-|c|^2)}{\gamma}} \tag{4.44}$$

$$B_{opt} \approx -\omega C_{gs}\left(1 - |c|\frac{g_m}{g_{d0}}\sqrt{\frac{\delta\zeta}{\gamma}}\right) \tag{4.45}$$

where $\zeta = 1/k$.

Note that in publications [65], [74] there is a small typographic error in (4.45), where c instead of $|c|$ is written.

Equations (4.39) and (4.42) suggest that devices with shorter channel length yield better noise figures, because the angular cutoff frequency f_T is proportional to $1/L_{eff}$ while $\sqrt{\gamma\delta\zeta(1-|c|^2)}$ becomes larger. Likewise, (4.36) (4.43) also suggest that shorter devices improve R_n. A more detailed study on this topic, however for silicon on insulator technology, can be found in [75].

In Tab. 4.1 scaling rules for MOSFET devices are collected. Various parameters are considered, and not only device dimensions are analyzed, but also two different ranges of the I_{DS} current. This table summarizes the consideration given in this chapter, and gives some first order approximations for choosing the transistor dimensions with the objective to decrease the noise and to increase the overall performance.

Tab. 4.1. MOSFET scaling rules

		Number of Fingers	Finger Width	Bias Current	
	Parameter	N	W	$I_{DS} < I_{\mathrm{DS,sat}}$	$I_{DS} > I_{\mathrm{DS,sat}}$
Performance	g_m	N	W	Increases with I_{DS}	∼constant
	f_T	Independent	Independent	Increases with I_{DS}	∼constant
	$f_{\max}$	Independent	∼1/W	Increases with I_{DS}	∼constant
Parasitics	C_{gs}, C_{gd}	N	W	∼constant	∼constant
	R_d, R_s, R_i	1/N	1/W	Independent	Independent
	R_g	1/N	W	Independent	Independent
Noise	$F_{\min}$	Independent	∼1/W	Decreases with I_{DS}	Decreases with I_{DS}
	R_n	1/N	1/W	Decreases with I_{DS}	∼constant
	G_{opt}	N	∼W	Increases with I_{DS}	∼constant
	B_{opt}	N	W	Independent	Independent

Chapter 5

Noisy two-ports

5.1. Noise Representation of Noisy Circuits

Due to the spectral representation of noise sources, noisy two-ports may be described by small signal equations, as is very well known, for example, for transistor equivalent circuits. The circuit theory of linear noisy networks shows that any noisy two-port can be replaced by a noise equivalent circuit which consists of the original two-port (assumed to be noiseless) and two additional noise sources [76],[77]. There are many equivalent representations for noisy two-ports, but only three of them are required for common applications.

The admittance form of the spectral representation of a noisy two-port is

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} I_{N_1} \\ I_{N_2} \end{bmatrix} \tag{5.1}$$

The equivalent circuit of the admittance representation is given in Fig. 5.1, where I_{N1}, I_{N2} represents the port noise currents with input and output short-circuited simultaneously. These two current sources do not actually exist in the positions marked in Fig. 5.1; they are merely concentrated equivalent representations of the effect of all noise-currents and noise-voltage sources inside the two-port.

These primary physical noise sources contribute to I_{N1}, I_{N2}. In general these two deduced quantities re not statistically independent. The arithmetic of noise quantities takes into account in the following way. Products $\overline{N_1 \cdot N_2^*}$ of two noise quantities N_1 and N_2 represent the Fourier transform of the cross-correlation functions $n_1(t)$ and $n_2(t)$. These products have o be taken as zero if $n_1(t)$ and $n_2(t)$ are not correlated at all or if there is no correlation at the particular frequency of interest. Otherwise,

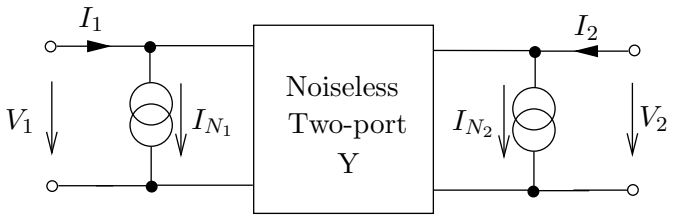


Fig. 5.1. Admittance representation of a noisy two-port

$$\overline{N_1 \cdot N_2^*} = c_{12}\sqrt{S_{n_1}(f) \cdot S_{n_2}(f)} \tag{5.2}$$

where $S_{n_1}(f)$ and $S_{n_2}(f)$ are spectral power densities of $n_1(t)$ and $n_2(t)$ and c_{12} is the so-called cross-correlation coefficient.

The noise parameters corresponding to the admittance matrix representation of a two port are

$$G_1 = \frac{\overline{|I_{N_1}|^2}}{4kT_0\mathrm{d}f} \quad , \quad G_2 = \frac{\overline{|I_{N_2}|^2}}{4kT_0\mathrm{d}f} \tag{5.3}$$

$$\rho_c = \frac{\overline{I_{N_1}^* I_{N_2}}}{\sqrt{|I_{N_1}|^2|I_{N_2}|^2}} \tag{5.4}$$

G_1 and G_2 are equivalent noise conductances, and ρ_c is the correlation coefficient ($\rho_c = |\rho_c|e^{\phi_c}$), $\mathrm{d}f$ is an increment frequency, T_0 is a standard temperature (290 K), and k the Boltzmann's constant.

The impedance representation of a noisy two port as given in Fig. 5.2 is

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + \begin{bmatrix} V_{N1} \\ V_{N2} \end{bmatrix} \tag{5.5}$$

Equation (5.5) expresses the fact that a noisy two-port generates noise voltages V_{N_1} and V_{N_2} across both of its ports if they are simultaneously open-circuited.

The representation in Fig. 5.2, natural for the impedance matrix representation, has the following noise parameters:

$$R_1 = \frac{\overline{|V_{N_1}|^2}}{4kT_0\mathrm{d}f} \quad , \quad R_2 = \frac{\overline{|V_{N_2}|^2}}{4kT_0\mathrm{d}f} \tag{5.6}$$

$$\rho_v = \frac{\overline{V_{N_1}^* V_{N_2}}}{\sqrt{|V_{N_1}|^2|V_{N_2}|^2}} \tag{5.7}$$

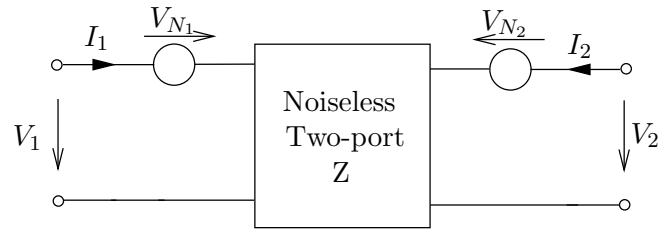


Fig. 5.2. Impedance representation of a noisy two-port

where R_1 and R_2 are equivalent noise resistances, and ρ_v is the correlation coefficient ($\rho_v = |\rho_v|e^{\phi_v}$).

A third, equivalent form of the two-port noise representation as shown in Fig. 5.3 formally uses two input sources V_N and I_N. This is the chain matrix

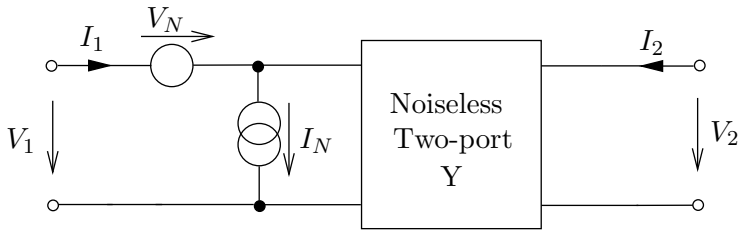


Fig. 5.3. Chain representation of a noisy two-port

representation. The equivalence of the admittance matrix and chain matrix representations require

$$I_N = I_{N_1} - \frac{Y_{11}}{Y_{21}} I_{N_2} \quad , \quad V_N = -\frac{I_{N_2}}{Y_{21}} \tag{5.8}$$

So, the chain representation of a noisy two-port is

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} + \begin{bmatrix} V_N \\ I_N \end{bmatrix} \tag{5.9}$$

Noise parameters for the chain matrix representation of a noisy two-port are R_N, g_N, and $|\gamma| = |\rho|e^{\phi}$, where

$$R_N = \frac{\overline{|V_N|^2}}{4kT_0 \mathrm{d}f} \quad , \quad g_N = \frac{\overline{|I_N|^2}}{4kT_0 \mathrm{d}f} \tag{5.10}$$

$$\rho = \frac{\overline{V_N^* I_N}}{\sqrt{|V_N|^2 |I_N|^2}} \tag{5.11}$$

where R_N is noise resistance, g_N is noise conductance and ρ is the correlation coefficient.

Another representation often used in simulators [78] is wave representation that makes use of noise waves theory, and scattering matrix of the two-port.

5.2. Correlation Matrices of Noisy Two-ports

A physically significant description of noise sources existing in the equivalent circuits of noisy two-ports is given by their self- and cross-power spectral densities, which are defined as Fourier transform of their auto- and cross-correlation matrices [77].

The so called normalized noise correlation matrix for admittance representation is

$$\mathbf{C_Y} = \frac{1}{4kT_0\mathrm{d}f}\overline{\begin{bmatrix} I_{N_1} \\ I_{N_2} \end{bmatrix}\begin{bmatrix} I_{N_1} \\ I_{N_2} \end{bmatrix}^+} = \frac{1}{4kT_0\mathrm{d}f}\begin{bmatrix} \overline{I_{N_1}I_{N_1}^*} & \overline{I_{N_1}I_{N_2}^*} \\ \overline{I_{N_2}I_{N_1}^*} & \overline{I_{N_2}I_{N_2}^*} \end{bmatrix} \tag{5.12}$$

where the overlines denote statistical average, and k Boltzmann's constant, T_0 reference absolute temperature (290 K), $\mathrm{d}f$ noise bandwidth, $^+$ conjugate transpose, * complex conjugate. Noise correlation matrices can be defined for other noise representations in the same way. They can be also normalized to thermal noise available power:

$$\mathbf{C_Y} = \frac{1}{4kT_0\mathrm{d}f}\mathcal{C}_\mathcal{Y} = \frac{1}{4kT_0\mathrm{d}f}\begin{bmatrix} \overline{I_{N_1}I_{N_1}^*} & \overline{I_{N_1}I_{N_2}^*} \\ \overline{I_{N_2}I_{N_1}^*} & \overline{I_{N_2}I_{N_2}^*} \end{bmatrix} \tag{5.13}$$

$$\mathbf{C_Z} = \frac{1}{4kT_0\mathrm{d}f}\mathcal{C}_\mathcal{Z} = \frac{1}{4kT_0\mathrm{d}f}\begin{bmatrix} \overline{V_{N_1}V_{N_1}^*} & \overline{V_{N_1}V_{N_2}^*} \\ \overline{V_{N_2}V_{N_1}^*} & \overline{V_{N_2}V_{N_2}^*} \end{bmatrix} \tag{5.14}$$

$$\mathbf{C_A} = \frac{1}{4kT_0\mathrm{d}f}\mathcal{C}_\mathcal{A} = \frac{1}{4kT_0\mathrm{d}f}\begin{bmatrix} \overline{V_NV_N^*} & \overline{V_NI_N^*} \\ \overline{I_NV_N^*} & \overline{I_NI_N^*} \end{bmatrix} \tag{5.15}$$

In general, elements of microwave circuits can be divided into two groups: passive and active multiports. Lossy multiports consist only of passive elements. Because of thermodynamical reasons, the correlation matrices in impedance and admittance representation are given by

$$\mathbf{C_Z} = 4kT\,\Re\{\mathbf{Z}\} \tag{5.16}$$

$$\mathbf{C_Y} = 4kT\,\Re\{\mathbf{Y}\}. \tag{5.17}$$

where $\mathbf{Z}$ and $\mathbf{Y}$ are electrical representation of a noiseless two-port, k is the Boltzmann constant and T absolute temperature.

Theoretical estimations of the correlation matrix are also obtained if noise equivalent circuits of the elements are used. For example if the currents I_{N_1} and I_{N_2} current of the two-port are known the correlation matrix can be found using (5.12).

In cases where the correlation matrix cannot be derived from theory, measurements of four noise parameters can be used. With these quantities, the chain representation of the correlation matrix is obtained as

$$\mathcal{C}_{\mathcal{A}} = 4kT\mathrm{d}f\mathbf{C_A} = 4kT\mathrm{d}f\begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_nY^*_{opt} \\ \frac{F_{min}-1}{2} - R_nY_{opt} & R_n|Y_{opt}|^2 \end{bmatrix} \tag{5.18}$$

using

$$\mathbf{C_A} = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \tag{5.19}$$

the four noise parameters are given by

$$\begin{aligned} R_n &= c_{11} && (5.20)\\ B_{opt} &= \frac{c_{12}-c_{21}}{2\cdot j\cdot c_{11}} && (5.21)\\ &= \Im\left(\frac{c_{12}}{c_{11}}\right) && (5.22)\\ &= -\Im\left(\frac{c_{21}}{c_{11}}\right) && (5.23)\\ G_{opt} &= \frac{\sqrt{4\cdot c_{11}\cdot c_{22}+(c_{12}-c_{21})^2}}{2\cdot c_{11}} && (5.24)\\ &= \sqrt{\frac{c_{22}}{c_{11}} - \left(\Im\left(\frac{c_{12}}{c_{11}}\right)\right)^2} && (5.25)\\ &= \sqrt{\frac{c_{22}}{c_{11}} - \left(\Im\left(\frac{c_{21}}{c_{11}}\right)\right)^2} && (5.26)\\ F_{min} &= 1 + c_{12} + c_{21} + \sqrt{4\cdot c_{11}\cdot c_{22}+(c_{12}-c_{21})^2} && (5.27) \end{aligned}$$

Noise correlation matrices are Hermitian matrices because

$$\Im(c_{11}) = \Im(c_{22}) = 0 \quad \text{and} \quad c_{12} = c^*_{21} \tag{5.28}$$

Because of this fact, noise properties of noisy linear two-ports are fully described by four numbers:

$$c_{11}, \quad c_{22}, \quad \Re(c_{12}), \quad \text{and} \quad \Im(c_{12}) \tag{5.29}$$

Another very important aspect of these matrices is that c_{11}, c_{22} and the determinant of these matrices are greater or equal to zero.

This formalism gives two matrices for each noisy two-port, namely the correlation matrix, which describes noisy components and the electrical matrix, which describes the noiseless part of the noise equivalent two-port. Obviously, each electrical matrix representation (impedance, admittance, chain) has its own corresponding correlation matrix.

5.3. Relations Between Different Noise Correlation Matrices

The noise correlation matrices can be transformed to different representations. The reason for changing the representations is given later in the text. The transformation can be made using the following general form:

$$\mathbf{C}' = \mathbf{P}\mathbf{C}\mathbf{P}^{+} \tag{5.30}$$

where $\mathbf{C}'$ and $\mathbf{C}$ denote the correlation matrices of the original and resulting representations, respectively, and the plus sign indicate conjugate transpose. Transformation matrix $\mathbf{P}$ can be obtained by establishing relations between the noise amplitudes of the original and resulting two-port and by expressing these relations in matrix form. The set of $\mathbf{P}$ matrices is shown in Tab. 5.1.

Tab. 5.1. Transformation matrices $\mathbf{P}$

Resulting Noise Representation	Original Noise Representation		
	Y	**Z**	**A**
Y	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$
Z	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$
A	$\begin{bmatrix} 0 & A12 \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

5.4. Relations Between Different Electrical Matrices

In circuit analysis as it is shown in the next chapter, one has to transform electrical matrix representation of two-ports. All transformations, which are important in this thesis are summarized in Tab. 5.2.

Tab. 5.2. Transformation relations for electrical chain, admittance and impedance matrix representation of two-ports

	A	**Y**	**Z**
A	$\begin{bmatrix} A & B \\ C & D \end{bmatrix}$	$\begin{bmatrix} \frac{-Y_{22}}{Y_{21}} & \frac{-1}{Y_{21}} \\ \frac{\Delta_Y}{Y_{21}} & \frac{-Y_{11}}{Y_{21}} \end{bmatrix}$	$\begin{bmatrix} \frac{-Z_{11}}{Z_{21}} & \frac{\Delta_Z}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix}$
Y	$\begin{bmatrix} \frac{D}{B} & \frac{-\Delta}{B} \\ \frac{-1}{B} & \frac{A}{B} \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} \frac{-Z_{22}}{\Delta_Z} & \frac{-Z_{12}}{\Delta_Z} \\ \frac{-Z_{21}}{\Delta_Z} & \frac{-Z_{11}}{\Delta_Z} \end{bmatrix}$
Z	$\begin{bmatrix} \frac{A}{C} & \frac{\Delta}{C} \\ \frac{1}{C} & \frac{D}{C} \end{bmatrix}$	$\begin{bmatrix} \frac{-Y_{22}}{\Delta_Y} & \frac{-Y_{12}}{\Delta_Y} \\ \frac{-Y_{21}}{\Delta_Y} & \frac{-Y_{11}}{\Delta_Y} \end{bmatrix}$	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$

where $\Delta = AD - BC$, $\Delta_Z = Z_{11}Z_{22} - Z_{12}Z_{21}$, $\Delta_Y = Y_{11}Y_{22} - Y_{12}Y_{21}$.

5.5. Interconnections of Noisy Two-ports

The correlation matrix of an interconnection of noisy two-ports is a linear transformation of their individual correlation matrices. A general form of this transformation is

$$\mathbf{C} = \mathbf{P_1}\mathbf{C^{(1)}}\mathbf{P_1}^{+} + \mathbf{P_2}\mathbf{C^{(2)}}\mathbf{P_2}^{+} \tag{5.31}$$

where $\mathbf{C^{(1)}}$ and $\mathbf{C^{(2)}}$ are correlation matrices of two-ports to be connected, $\mathbf{P_1}$ and $\mathbf{P_2}$ are transformation matrices, and $\mathbf{C}$ is the resulting correlation matrix of the interconnection. The transformation matrices corresponding to the various types of interconnections can be obtained by establishing matrix

relations between the noise amplitudes of the individual two-ports to be connected and the resulting two-port.

Of particular interest for the noise analysis of circuits composed of interconnected two-ports are series, parallel and cascaded connections. The following formulas can be used for these three connection types:
Parallel connection:

$$\mathbf{C_Y} = \mathbf{C_Y^{(1)}} + \mathbf{C_Y^{(2)}} \tag{5.32}$$

Series connection:

$$\mathbf{C_Z} = \mathbf{C_Z^{(1)}} + \mathbf{C_Z^{(2)}} \tag{5.33}$$

Cascade connection:

$$\mathbf{C_A} = \mathbf{A^{(1)}}\mathbf{C_A^{(2)}}\mathbf{A^{(1)+}} + \mathbf{C_A^{(2)}} \tag{5.34}$$

For series and parallel connection of two-ports the resulting correlation matrix is the sum of the correlation matrices in admittance or impedance representation of the original two-ports, respectively. In case of the cascade connection, the formula is more complicated (5.34).

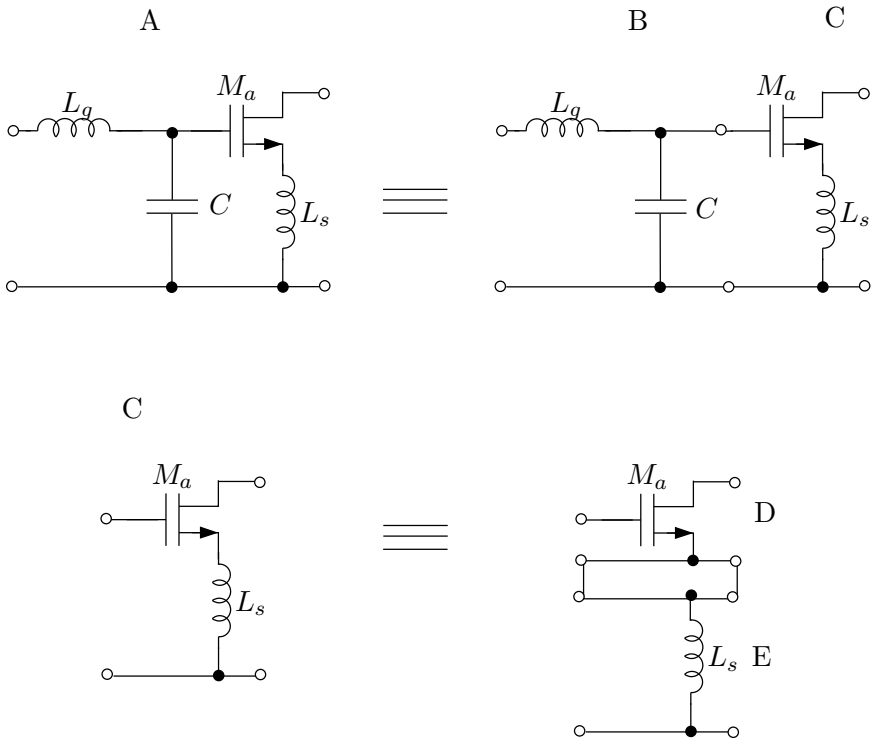


Fig. 5.4. Principle of noise analysis for the amplifier

Using the correlation and electrical matrices the noise analysis of circuits composed of interconnected two-ports can be easily performed. The principle of the analysis procedure is shown in Fig. 5.4.

The amplifier A, which has to be analyzed is decomposed into four basic two-ports B, C, D, E. The basic two-ports have to be specified by their electrical and correlation matrices. The electrical matrices are obtained by applying standard procedures, either calculations or measurements. Once all matrices are known the basic two ports are interconnected in a manner that finally the two-port A is obtained. The two-port A consist of two-ports B and C connected in cascade, and the two-port C consist of two-ports D and E connected in series. Depending of the kind of connection, noise correlation and electrical matrices are obtained using previous considerations.

Chapter 6

Low Noise Amplifier Design

The most critical point for the realization of a highly integrated receiver is the RF input. The first stage of a receiver is a low noise amplifier (LNA), which dominates the noise figure of the whole receiver. Besides of low noise, low power consumption, high linearity and small chip size are the other key requirements. Because of this situation the design of the LNA is really a challenge.

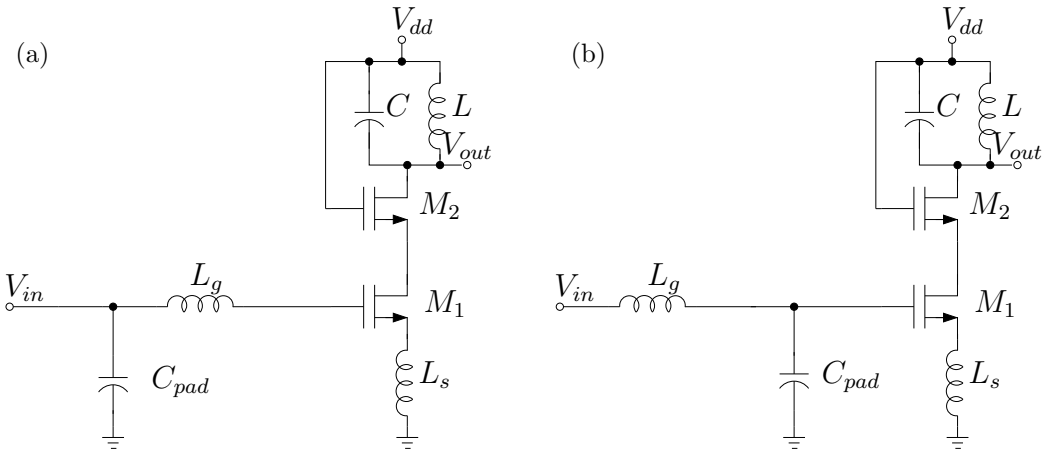


Fig. 6.1. Amplifiers with input matching circuits: (a) inductor L_g connected directly to the transistor, (b) pad capacitance C_{pad} connected directly to the transistor.

Among a few possible solutions for the LNA core, a cascode amplifier shown in Fig. 6.1 with inductive degeneration is often preferred. The transistor in common-gate (CG) configuration of the cascode amplifier reduces the Miller effect. It is well known, that the capacitance connected between output and input of an amplifier with inverting gain, is seen at its input and output multiplied by the gain. The gain of the common-source (CS) configuration is $-g_m R_L$ where R_L is the output impedance, and the input impedance of CG configuration is $1/g_m$. Therefore, if both transistors have

similar g_m the gain of the transistor in CS configuration decreases and the Miller capacitance is reduced [79]. At the output of the cascode amplifier, the overlap capacitance does no affect the Miller effect since the gate of the amplifier is grounded. Thus, the tuned capacitor of the LC tank only has to be large enough to make the tank insensitive to C_{gd2}. In addition, with a low impedance point at the output of the common source amplifier, the instability caused by the zero of the transfer function is highly reduced. Finally, with an AC ground at the gate of the cascode amplifier, the output is decoupled from the input, giving the cascode configuration a high reverse isolation. Although in Fig. 6.1 the LC tank is shown explicitly, in practical situations another configuration can be made, while for small signal circuits, it does not matter if the second node of the capacitor C is connected to V_{dd} or ground. However, in any case a serial output capacitor is needed to block the DC path. This capacitor, not shown in Fig. 6.1, can contribute to the output matching, so it has to be chosen very carefully. The output pad capacitance can be used for output matching additionally.

In order to connect the LNA to a measurement equipment, a package or an antenna bonding pads (C_{pad}) are needed. Fig. 6.1 shows two LNAs witch different input matching networks. In the networks from Fig. 6.1a all components are placed on the chip. This principle is very often used, therefore we start the LNA analysis from this point. The bonding pad is parallel to the input of the LNA, and as long as their impedance is much higher than the input impedance of the LNA, they do not introduce any significant effects to the input impedance of the whole circuit. In our case assuming practical value of 150 fF for C_{pad} and frequency of 2 GHz the impedance of the pad can be neglected in comparison with required 50 Ω. However, if the influence of C_{pad} can not be neglected only the imaginary part of Z_{in} is affected.

The use of inductive degeneration results in no additional noise generation since the real part of the input impedance does not correspond to a physical resistor [80]. The source inductor L_s generates a resistive term in the input impedance

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + j\left(\frac{\omega^2(L_g + L_s)C_{gs} - 1}{\omega C_{gs}}\right), \tag{6.1}$$

where L_s and L_g are source and gate inductors, respectively and g_m and C_{gs} denote small signal parameters of transistor M_1 (C_{gd}, g_{ds} and C_{pad} are neglected).

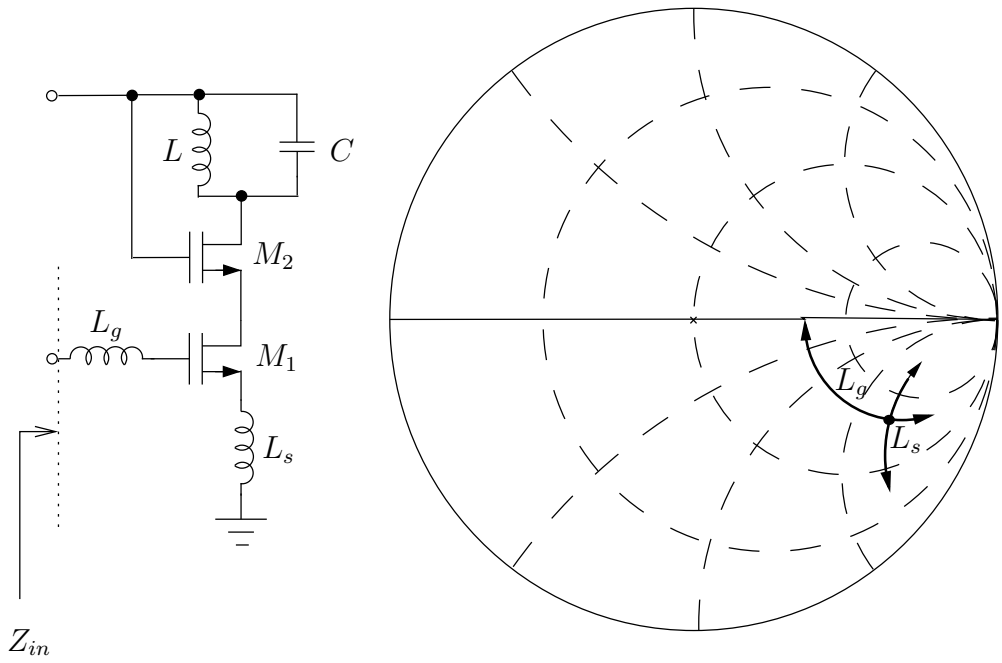


Fig. 6.2. Input matching on Z plane

The inductor L_g series connected with the gate cancels out the admittance due to the gate-source capacitor. Here, it is assumed that the tuned load (L, C) is in resonance at angular frequency ω_0 and therefore appears to be a pure resistive load R_L.

The input matching principle is shown in Fig. 6.2. To obtain a pure resistive term at the input, the capacitive part of input impedance introduced by the capacitance C_{gs} should be compensated by inductances. To achieve this cancellation and input matching, the source and gate inductances should be set to

$$L_s = \frac{R_s C_{gs}}{g_m} \quad , \qquad L_g = \frac{1 - \omega_0^2 L_s C_{gs}}{\omega_0^2 C_{gs}} \tag{6.2}$$

where R_s is the required input resistance, normally 50 Ω.

The noise figure of the whole amplifier with noise contribution of transistor M_2 neglected can be given as [81]

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega_0}{\omega_T}\right)\left[1 + \frac{\delta\alpha^2}{k\gamma}(1+Q^2) + 2|c|\sqrt{\frac{\delta\alpha^2}{k\gamma}}\right] \tag{6.3}$$

where

$$\alpha \equiv \frac{g_m}{g_{d0}}, \tag{6.4}$$

δ, γ, c, k are bias dependent transistor parameters and $Q = 1/(\omega_0 C_{gs} R_s)$ is the quality factor of the input circuit. It can be seen that noise figure is improved by the factor $(\omega_T/\omega_0)^2$ [81]. Note, that for currently used sub-micron MOS-technologies ω_T is in the order of 100 GHz. The noise figure of the LNA can be also expressed in simplified form with induced gate noise neglected, however, easier for first order analysis

$$F \approx 1 + \frac{\kappa g_m R_s}{(\omega_T/\omega_0)^2} \tag{6.5}$$

where κ is bias dependent constant and R_s is source resistance. Although on a first sight (6.5) suggests low transconductance g_m for low noise figure, taking into account that $\omega_T \approx g_m/C_{gs}$ one can see that it is not true. Increasing of g_m lowers the noise figure but at the cost of higher power consumption. Since C_{gs} contributes to the $(\omega_T/\omega_0)^2$ factor, lowering this capacitance leads to improved noise. The last possibility of noise reduction is reducing the signal source resistance R_s. However, this resistance is fixed, normally.

Decreasing the C_{gs} capacitance is done by reducing the size of the transistor. This has also impact on the linearity of the amplifier, and according to input matching requirements (6.2), very large inductors L_g should be used that can not be longer placed on chip. Because of this reason the inductor L_g is placed off-chip. Between the inductor and the amplifier the on chip pad capacitance C_{pad} is located as it is shown on Fig. 6.1b. It consists of the pad structure itself and the on chip capacitance of ESD structure and signal wiring. In this case pad capacitance and C_{gs} are in similar order. Therefore, the pad has to be treated as a part of an amplifier and then taken into account in the design process.

It should be noted, that particularly input pads (see section 3.4) need special consideration. It has been proven [55], [82] that shielded pads have ideally no resistive component, and so they neither consume signal power nor generate noise. They consist of two metal plates drawn on the top and bottom metals to reduce the pad capacitance value down to 50 fF. Unfortunately, it is not the whole capacitance, which should be taken into account. One has to realize that all connections to the pad increase this value.

The input matching circuit is very important for low noise performance of the LNA. In [83] low noise cascode amplifiers using different approaches for input impedance matching have been analyzed and compared in terms of noise figure performance for bipolar technology. The effect of noise filtering caused by the matching network has been pointed out. Furthermore, a

parallel-series matching network has been proposed, which allows dominant noise contributions to be reduced. A very low noise figure can be achieved by this way. This matching consists of series inductance and parallel capacitance connected between base and emitter of the common source transistor.

The input matching presented in Fig. 6.1b is quite similar to this presented in [83] for bipolar amplifier. Here, instead of base emitter capacitance pad capacitance is used. It can be expected, that taking pad capacitance as a part of input matching can lower the noise figure of a FET LNA. Indeed, as shown in recent publications e.g., [74], [82], [84], [85], [86], [87], [88] RF-CMOS LNAs have achieved lowest noise values if pad capacitance was taken into consideration. The reason for this behavior has not been discussed enough, so far.

In the amplifier from Fig. 6.1b C_{pad} is connected parallel to the C_{gs} of the transistor M_1. Since the small transistors are interesting for low noise low current amplifier, these two capacitances are in the similar order, as already written. Thus, C_{pad} can not be neglected in this case. The input impedance of such an amplifier can be expressed as

$$\begin{aligned} Z_{in} &= \frac{g_m L_s C_{gs}}{(C_{pad}+C_{gs})^2 + \omega^2 L_s C_{pad} C_{gs}^2(\omega^2 C_{pad} L_s - 2) + \omega^2 C_{pad}^2 L_s (g_m^2 L_s - 2)} \\ &+ j\frac{\omega^2(L_g+L_s)C_{gs}^2 - C_{gs} + C_{pad}(g_m^2 L_s \omega^2(\omega^2 L_g C_{pad} - 1) - (\omega^2 L_s C_{gs} - 1)^2)}{\omega((C_{pad}+C_{gs})^2 + \omega^2 L_s C_{pad} C_{gs}^2(\omega^2 C_{pad} L_s - 2) + \omega^2 C_{pad}^2 L_s (g_m^2 L_s - 2))} \\ &+ j\frac{C_{pad}(\omega^4 C_{gs}^2 L_s L_g(\omega^2 L_s C_{pad} - 2) + 2\omega^2 L_g C_{gs}(1 - \omega^2 L_s C_{pad}) + \omega^2 L_g C_{pad})}{\omega((C_{pad}+C_{gs})^2 + \omega^2 L_s C_{pad} C_{gs}^2(\omega^2 C_{pad} L_s - 2) + \omega^2 C_{pad}^2 L_s (g_m^2 L_s - 2))}. \end{aligned} \tag{6.6}$$

From (6.6), the real part of the input impedance can be approximated as

$$\Re(Z_{in}) \approx \frac{g_m L_s C_{gs}}{(C_{pad}+C_{gs})^2}, \tag{6.7}$$

and the imaginary part, if C_{gs} is at least 2 times larger than C_{pad}, can be approximated as

$$\Im(Z_{in}) \approx \frac{C_{gs}(\omega^2 L_s C_{gs} - 1 + \omega^2 L_g C_{gs})}{\omega(C_{pad}+C_{gs})^2}. \tag{6.8}$$

Contrary to the previous case either the real or imaginary part of input impedance is affected. The real part of input impedance decreases. This decrease requires higher values of inductance L_s. It is rather negative, first and foremost because of lowering the gain, but also because of introducing stability issues and generating noise.

The value of inductance L_g required for matching decreases. In turn, this is positive, since this inductor occupies a large area, particularly when the transistor M_1 (and C_{gs} value) is small. Besides of the area the noise contribution of L_g is limited, because smaller inductor has also lower resistance.

It can be concluded from (6.6), that for large FET sizes with large values of C_{gs} capacitance C_{pad} can be neglected. However, large transistors consume more power than small ones, even for small bias voltages. Moreover, later in this text it is shown that C_{pad} can have also positive influence on noise performance of the low noise amplifier.

6.1. Impact of Channel and Gate Resistance on LNA Performance

If in the circuit shown in Fig. 6.2 channel R_i and gate R_g resistance are taken into account, then the input impedance at the resonant frequency

$$\omega_0 = \frac{1}{\sqrt{C_{gs}L_sR_ig_m + (L_s + L_g)C_{gs}}} \tag{6.9}$$

is resistive:

$$R_{in} = R_g + R_i + \frac{g_mL_s}{C_{gs}}. \tag{6.10}$$

Neglecting the both resistances, particularly R_i introduces errors in input resistance and resonant frequency. Moreover, the channel resistance impacts also the noise figure. According to [68] an improved noise figure expression for the schematic shown in Fig. 6.2 can be derived as

$$F = 1 + \frac{R_g}{R_s} + \left(\frac{\omega_0}{\omega_T}\right)\gamma\frac{g_{d0}}{R_s}\left\{\left[R_s^2 + (L_g + L_s)^2\right]\frac{\delta\alpha^2}{5\gamma} + (R_s + R_i)^2 + \right.$$
$$\left. + 2R_s(R_s + R_i)c\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right\} \tag{6.11}$$

where parameters: α, δ, γ, c and Q have been already defined. Additional consideration on gate and channel resistance can be found in Chapter 4.

6.2. Choosing Transistor Width and Bias Conditions

One of the major problem during the design process is the selection of the proper widths of transistors M_1 and M_2. For this issue power-constrained

noise optimization [52] has been often used. After reformulating the expression for noise figure in terms of power consumption, and with some additional assumptions taken from long-channel theory the width of the optimum device (M_1) is given as:

$$W_{opt_{M_1}} \approx \frac{1}{3\omega_0 L_{eff} C_{ox} R_s} \tag{6.12}$$

where L_{eff} is the effective transistor length and C_{ox} is the oxide capacitance of the transistor. The (6.12) gives a definite width of the transistor, but for short channel devices like 0.13 μm CMOS leads to very large transistors.

With respect to the selection criterion of the gate width there are also other publications [89], [90], [91]. Unfortunately, they do not lead to best results, because not only the transistor has to be optimized.

As discussed earlier, the best results are achieved when pad capacitance is taken into account during design consideration. Currently best noise figures in 1 GHz range were reported in [74] and [84] and are in the order of 0.8 dB. Very good results for the 7 GHz band were reported in [82]. The achievements of this work and other recently reported achievements are shown in the next chapter.

For selection of the width of the cascode transistor M_2 two competing considerations should be made. The Miller capacitance of M_1 can reduce the gate and drain impedance of M_1 considerably, degrading both noise performance and input match. This behavior can be compensated by a large cascode device (CG device), which reduces the gain of the CS device. However, the parasitic source capacitance associated with a large CG device increases the amplification of the CG device. In recent publication, the ratio between CS and CG transistor widths varies from 0.5 [71] up to 3 [74], based on simulations. Note, the M_2 introduces noise in the amplifier, too, and the size of this transistor should be also constrained by the noise figure of the amplifier [92].

Another important issue is the current consumption. In [71], [82] the current consumption is about 5 - 6 mA for the single ended structure shown in Fig. 6.1. The current consumption is a key criterion for selecting the transistor width, since with known supply voltage and power budget a supply current can be derived.

The current consumption with given transistor size depends on gate to source voltage of the transistor M_1, and increases with increasing the overdrive voltage V_{od} defined as a difference between gate source voltage and

threshold voltage. It is well known, that increasing V_{od} improves the linearity of the amplifier, and V_{od} around 200 mV or even less is a reasonable value for a 130 nm MOS technology [93]. However, in the design considerations presented in this chapter such an assumption is not made, and the whole region of V_{od} voltage is analyzed.

Except low noise figure the LNA has to posses high gain and linearity. To find the best transistor size, bias condition and passive elements values simulations can be performed. During such simulations needed parameters can be swept. However, not all simulations are easy to done. For example the P_{1dB} or IIP3 simulations with transistor size and bias condition swept. In such a simulation, to obtain reasonable results the amplifier has to be always matched either on the input or in the output. It is easy to note, according to e.g., (6.6) that it is not an easy task, since transistor size and bias condition influence the input and output impedances.

A solution for that problem is the design flow that based on parameter simulation independent on additional elements. Such parameters are four noise parameters, DC current and its derivative.

Firstly, the impact of transistor fingers has to be found using the schematic shown in Fig. 6.1. For this reason the total width of the transistors are fixed and the number of fingers is swept. For simulations, both transistors have the same width, which is not an optimum, but shows some important issues. The gate bias voltage of the transistor M_1 is set to 0.6 V ($V_T \approx 0.45$ V), and the V_{dd} voltage is set to 1.2 V. The LC tank has a resonant frequency of 2.14 GHz (middle of the UMTS band), and both inductors L_s and L_g are shortened, so their inductances are equal to zero. Additionally, C_{pad} is also removed.

The results of such a simulation are shown in Fig. 6.3, Fig. 6.4 and Fig. 6.5. The supply current I_{dd}, the noise figure minimum and equivalent noise resistance against number of fingers are presented for two transistor widths, 50 and 100 μm, respectively. It can be seen in Fig. 6.3 that the current is not constant, although the the total width of the transistor is constant. However, for number of finger larger than 10 the current shows almost constant behavior.

It is shown in Fig. 6.4, that NF_{min} decreases when the number of fingers increases. These considerations lead on a first sight to the conclusion that more fingers lead to a better noise performance of the amplifier. Unfortunately this is not the fact, since a too short finger width with too many fingers,

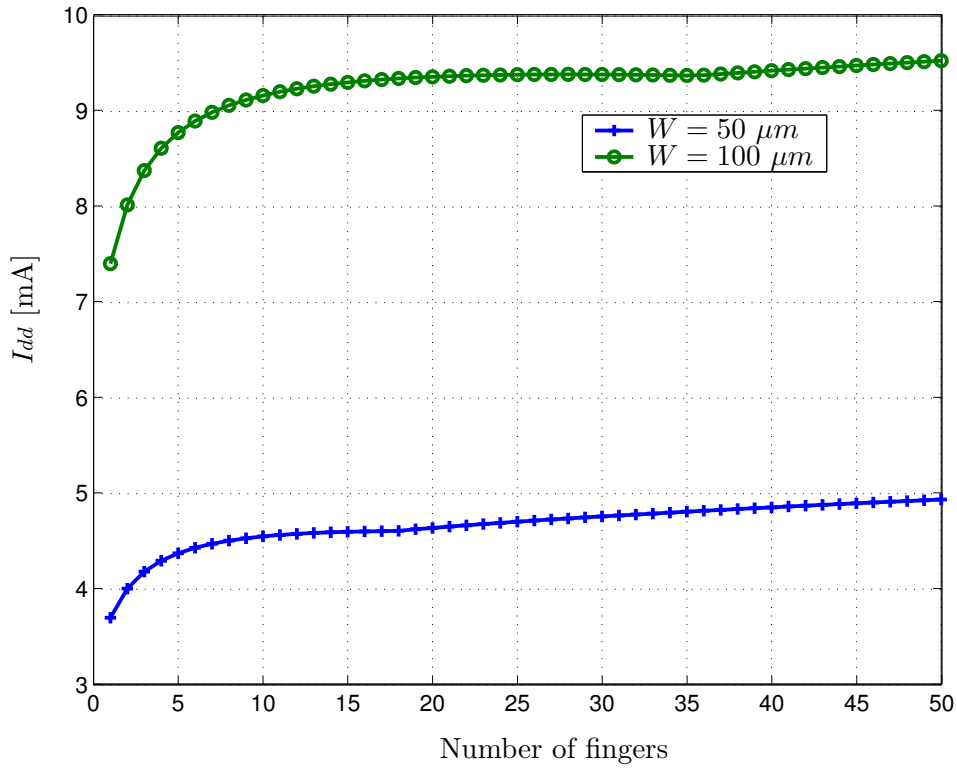


Fig. 6.3. I_{dd} current versus finger number for two different transistor widths with V_{gs} at M_1 set to 0.6 V.

although decreases the noise resistance (see section 4.3.2) increases the C_{gb} and reduces f_T of a transistor [94], [95]. The equivalent noise resistance show in Fig. 6.5 also decreases when the number of fingers increases, but finger numbers larger than 10 do not introduce significant improvements any more.

However, to find the most suitable transistor topology (number of fingers and width of each finger) for an assumed current another analysis can be performed. The conditions are the same as in the previous case except V_{gs} voltage that is varied to keep the supply current constant.

The minimum noise figure $\mathrm{NF}_{\mathrm{min}}$ and transconductance g_m is observed. To combine these both quantities the figure of merit (FoM) defined as a ratio between g_m and $\mathrm{NF}_{\mathrm{min}}$ is introduced.

Fig. 6.6 shows the best transistor topology (number of fingers and width of each finger) for 1 mA supply current. It is easy to see that for 1 mA current the best total transistor width for 20, 15 and 10 fingers is around 30 μm (the width of each finger 1.5, 2, and 3 μm, respectively). For only 5 fingers the optimum total transistor width is around 20 μm.

Fig. 6.7 shows the best transistor topology for 2 mA supply current. For this current the best total transistor width for 20, 15 and 10 fingers is around

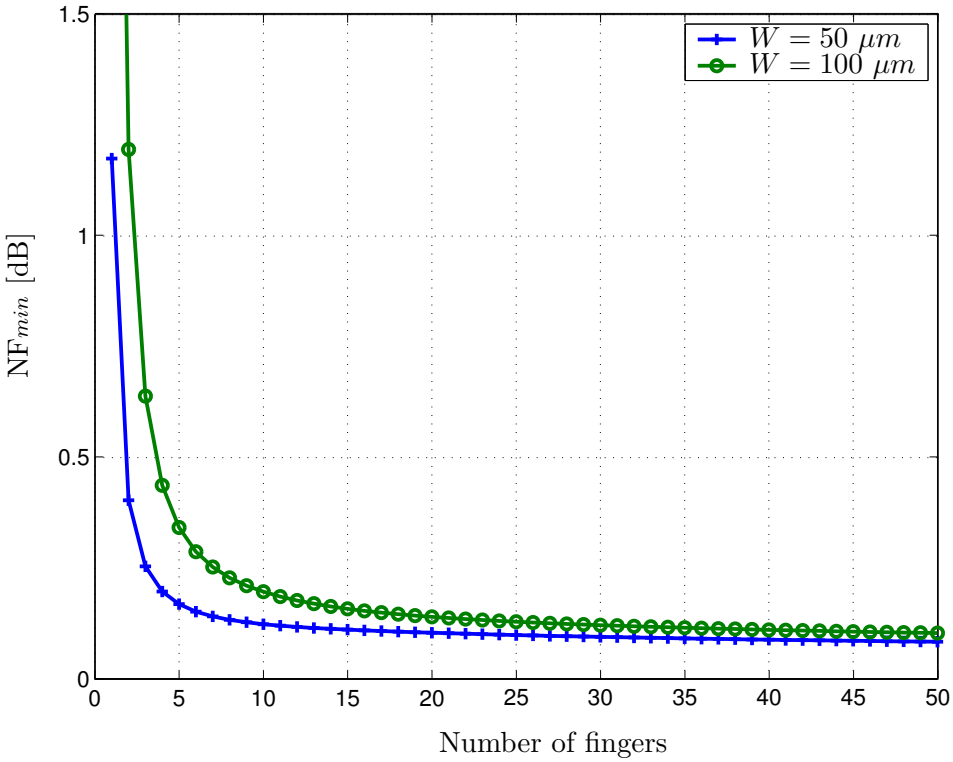


Fig. 6.4. Noise figure minimum at 2.14 GHz versus finger number for two different transistor widths with V_{gs} at M_1 set to 0.6 V

35 μm (the width of each finger 2, 2.5, and 3.5 μm, respectively). For only 5 fingers the optimum total transistor width is around 30 μm.

Fig. 6.8 shows the best transistor topology for 5 mA supply current. In this case the best total transistor width for 20, 15 and 10 fingers is around 60 μm (the width of each finger 3.5, 4, and 5 μm, respectively). For only 5 fingers the optimum total transistor width is around 40 μm.

Two important facts stem from this analysis. In each analysis the best performance in respect to FoM show topologies with maximum analyzed finger number. Secondly, lowering supply currents leads to decreasing the overall transistor width. The latter conclusion, in an agreement with previous statements, leads to conclusion, that the transistor width should be kept low, to achieve the best noise performance.

In the next analysis step the influence on transistor width and biasing is under consideration. This time, number of fingers is fixed to 20 and simulations show the dependencies of the four noise parameters at 2.14 GHz on supply current I_{dd}, transistor width W and gate source bias voltage of M_1 (see Fig. 6.1). The simulations have been performed using the same conditions as in the both previous cases.

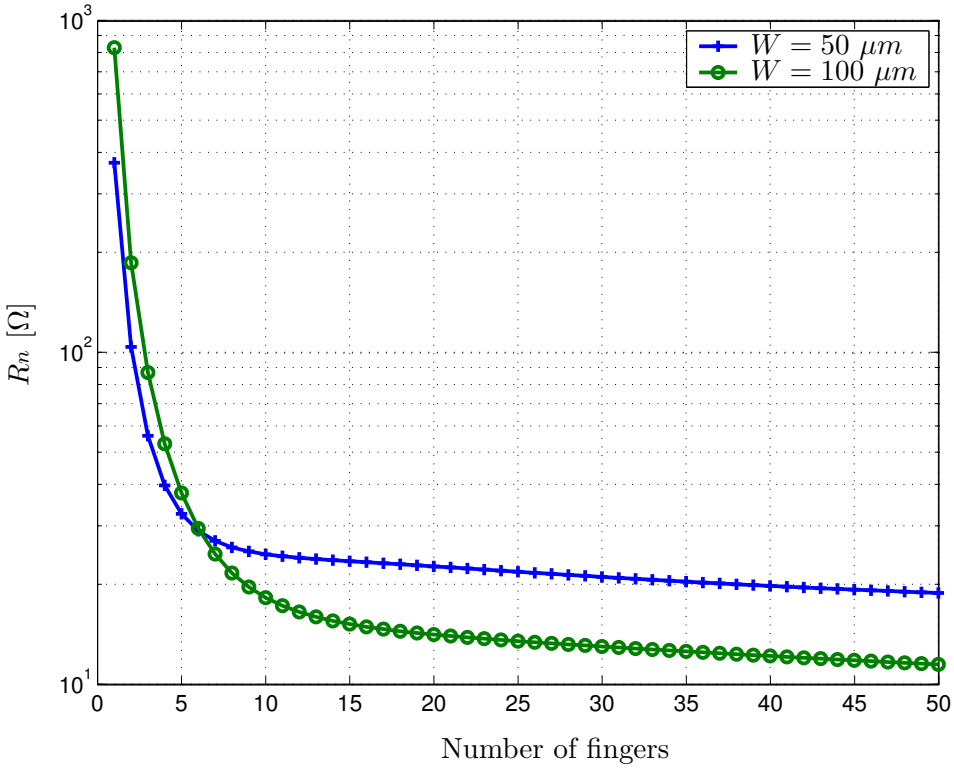


Fig. 6.5. Equivalent noise resistance at 2.14 GHz versus finger number for two different transistor widths with V_{gs} at M_1 set to 0.6 V

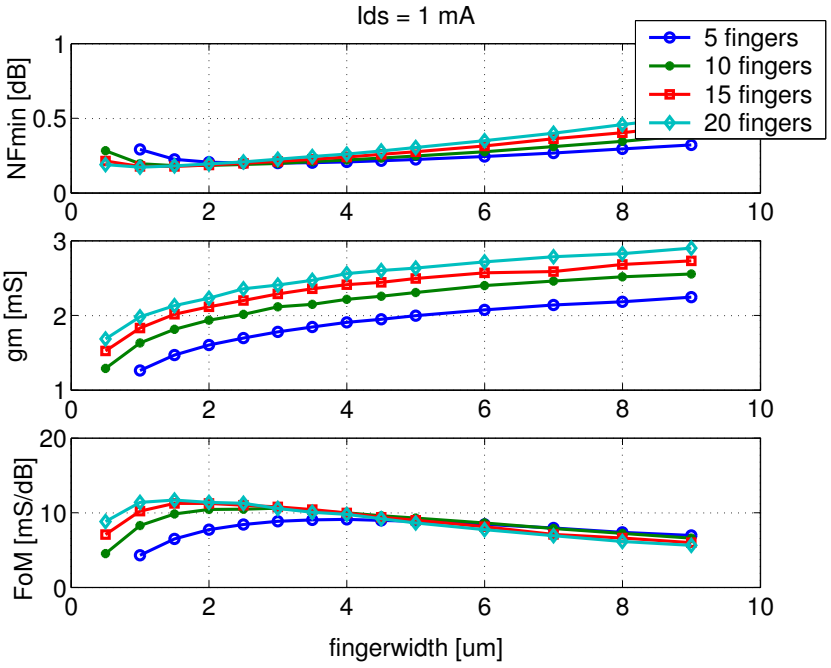


Fig. 6.6. $\mathrm{NF}_{\mathrm{min}}$, g_m and figure of merit FoM for various transistor topologies. Analysis frequency is 2.14 GHz and power consumption $I_{dd} = 1$ mA, $V_{dd} = 1.2$ V.

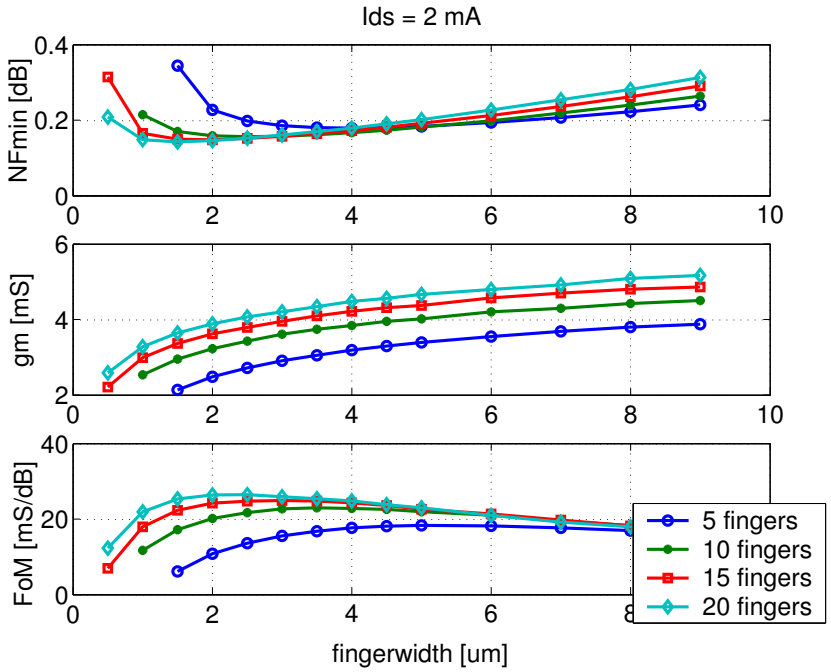


Fig. 6.7. $\mathrm{NF}_{\mathrm{min}}$, g_m and figure of merit FoM for various transistor topologies. Analysis frequency is 2.14 GHz and power consumption $I_{dd} = 2$ mA, $V_{dd} = 1.2$ V.

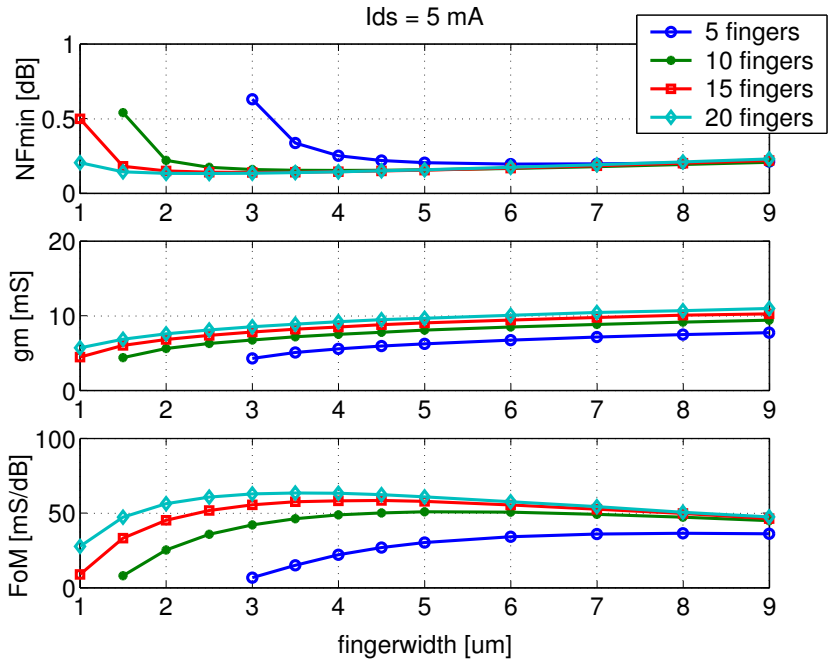


Fig. 6.8. $\mathrm{NF}_{\mathrm{min}}$, g_m and figure of merit FoM for various transistor topologies. Analysis frequency is 2.14 GHz and power consumption $I_{dd} = 5$ mA, $V_{dd} = 1.2$ V.

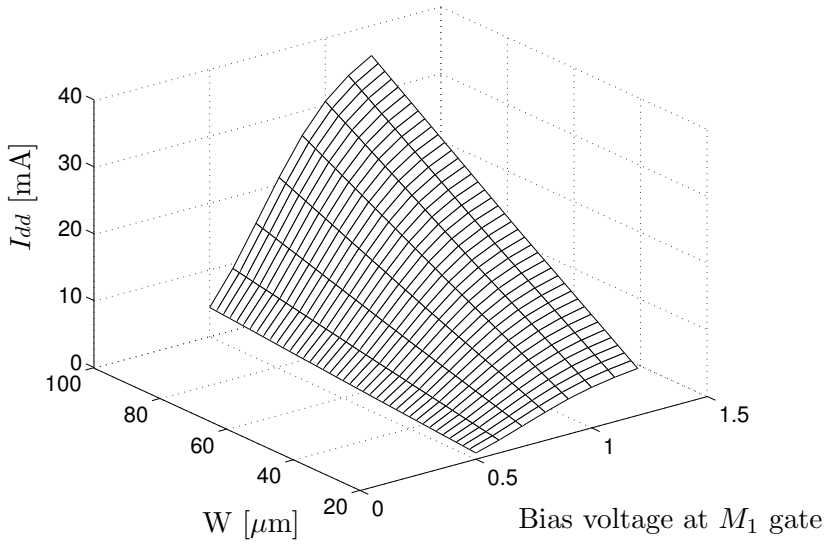


Fig. 6.9. Supply current versus transistor width W and bias voltage

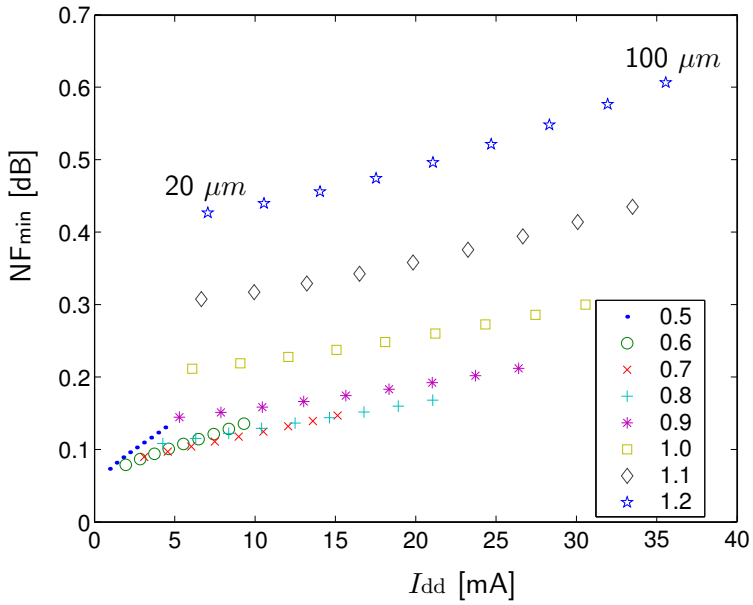


Fig. 6.10. Noise figure minimum versus supply current for various gate source voltages and transistor widths. Gate source voltages are in the range from 0.5 up to 1.2 V, and the transistor widths are between 20 and 100 μm with 10 μm step.

Simulation results shown in Fig. 6.10 – Fig. 6.13 are helpful for choosing the optimum transistor width and bias condition for low noise operation. A transistor width should be chosen that minimizes noise figure minimum and noise resistance. However, these simulation results do not show the optimum values for others amplifiers elements.

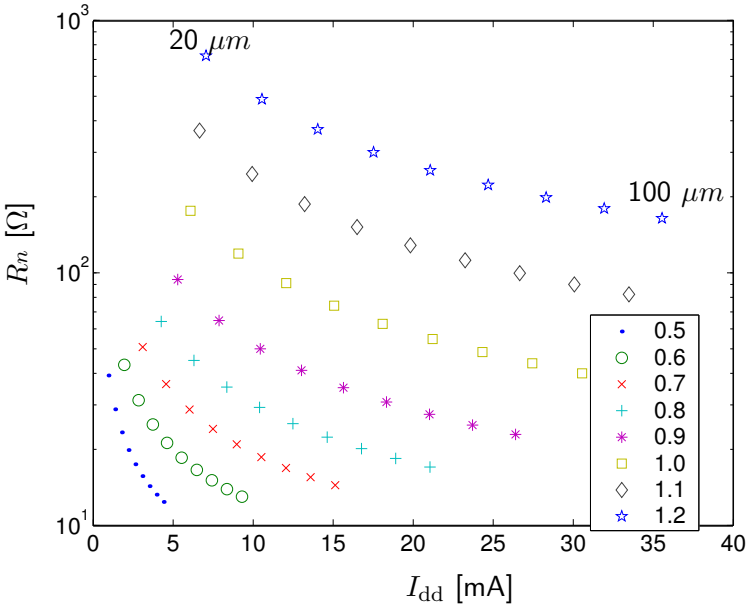


Fig. 6.11. Equivalent noise resistance versus supply current for various gate source voltages and transistor widths. Gate source voltages are in the range from 0.5 up to 1.2 V, and the transistor widths are between 20 and 100 μm with 10 μm step.

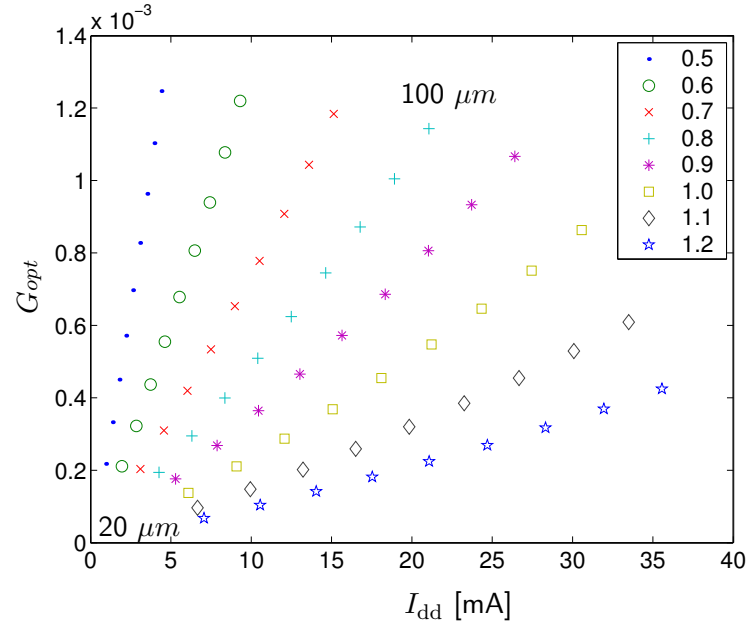


Fig. 6.12. Optimum source reactance versus supply current for various gate source voltages and transistor widths. Gate source voltages are in the range from 0.5 up to 1.2 V, and the transistor widths are between 20 and 100 μm with 10 μm step.

Therefore, in the following section the optimum choice of amplifiers components like L_s, L_g and C_{pad} is considered.

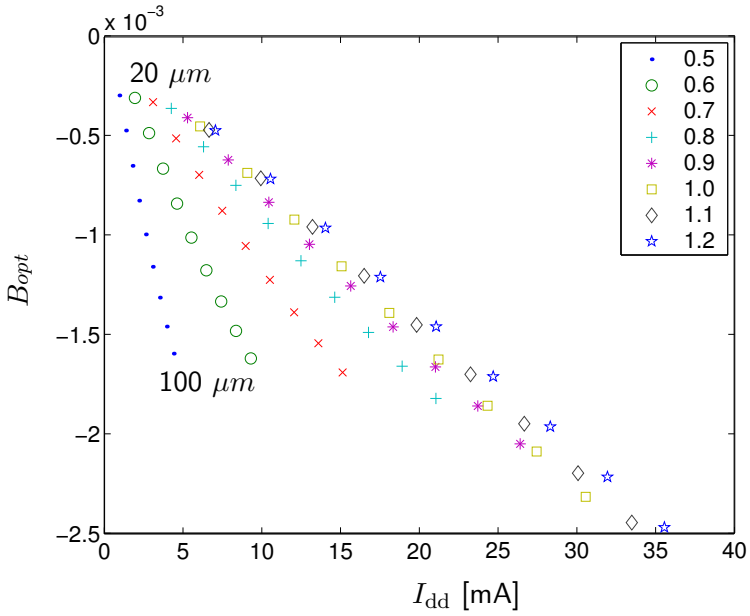


Fig. 6.13. Optimum source susceptance versus supply current for various gate source voltages and transistor widths. Gate source voltages are in the range from 0.5 up to 1.2 V, and the transistor widths are between 20 and 100 μm with 10 μm step.

6.3. Two-port Noise Theory in LNA Design

In this section it is shown, how the theory of noisy two-ports can be applied in design of the LNA. The analyzed amplifier consists always of two different two-ports: A and B. The noise parameters of two-port A are known, shown in Fig. 6.10 – Fig. 6.13 with some assumptions, however. The contribution of transistor M_2 to the overall noise figure is neglected. In case of cascode amplifiers, neglecting the noise contribution of M_2 leads to a small underestimate of the noise figure. However, having the optimum width of transistor M_1, the width of transistor M_2 can be found by further optimization.

In the following subsections influence of source degeneration and two different matching principles on overall noise performance is investigated.

6.3.1. Influence of source degeneration

Only in this case, according to section 5.5 an electrical matrix of cascode connection is needed. The electrical admittance representation matrix of transistor cascode connection is shown in (B.7) – (B.10) (B). According to

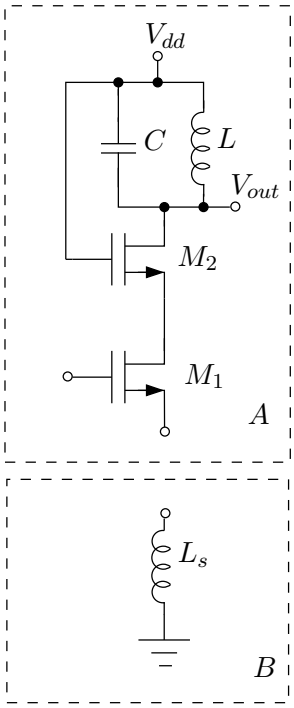


Fig. 6.14. Circuit diagram for source degeneration analysis

the assumptions made the electrical admittance representation of a cascode connection of FETs M_1 and M_2 is equal to

$$Y = \begin{bmatrix} j\omega C_{gs} & 0 \\ g_m & 0 \end{bmatrix}, \tag{6.13}$$

and the noise correlation matrix in chain representation is given by (5.15).

Firstly, the source degeneration is analyzed according to schematic shown in Fig. 6.14. Since the inductor L_s is in series with the transistor, the impedance representations of both matrices (correlation and electrical) have to be added [77], to obtain the resulting matrices. For this reason, the admittance matrix of the transistor has to be translated into impedance representation.

The impedance representation of the electrical matrix of the inductor L_s (two-port B) can be expressed as

$$\mathbf{Z_B} = \begin{bmatrix} j\omega L_s & -j\omega L_s \\ -j\omega L_s & j\omega L_s \end{bmatrix} \tag{6.14}$$

and the total electrical representation of the two series connected two-ports is given by

$$\mathbf{Z_{tot}} = \mathbf{Z_A} + \mathbf{Z_B} \tag{6.15}$$

where $\mathbf{Z_A}$ is the impedance matrix of the transistor transformed from $\mathbf{Y_A}$ given in (6.13).

Similar consideration has to be made for the correlation matrices. It is assumed that L_s is ideal and has no real terms in the impedance matrix (6.14), thus the correlation matrix of this inductor is a zero matrix, according to (5.16). In the case of the transistor, its correlation matrix should be converted from the chain to impedance representation. If the impedance electrical and correlation matrix are calculated, the latter can be transformed to the chain representation, because of easier analysis. Next, using (5.19)-(5.27) the noise parameters of the new two-port (two-port A with inductor L_s (B) shown in Fig. 6.14) can be expressed in terms of two-port A noise parameters and inductance L_s as follows:

$$R'_n = d\,R_n \tag{6.16}$$

$$B'_{opt} = \frac{B_{opt} + \omega L_s |Y_{opt}|^2}{d} \tag{6.17}$$

$$G'_{opt} = \frac{G_{opt}}{d} \tag{6.18}$$

$$F'_{min} = F_{min} \tag{6.19}$$

$$d = 1 + 2\omega L_s B_{opt} + \omega^2 L_s^2 |Y_{opt}|^2 \tag{6.20}$$

It is easy to see, that all noise parameters except F_{min} are dependent on L_s and Y_{opt} values and F_{min} is independent on the value of L_s.

However, in this analysis one important problem is omitted. In (6.13) C_{gd} and g_{ds} of the transistor M_1 and M_2 are neglected. For this reason, although (6.20) suggests that noise figure can be lowered by proper choice of L_s it is not always the truth. It is only valid for low operating frequency, or in other words only if C_{gd} can be neglected.

Simulations performed on 0.13 μm CMOS transistor show, that at 2 GHz, our lowest frequency of interest, neglecting C_{gd} and g_{ds} leads to erroneous results (F_{min} does depend on the value of L_s). However, some previous statements are still valid, foremost the value of L_s should be kept low to limit noise and stability issues and maximizes gain of the LNA.

6.3.2. Influence of Pad Capacitance with On-chip Inductance

This configuration is shown in Fig. 6.15. As written before, this architecture can be used for rather high frequency and large transistors, when inductor L_g has small values.

Let us assume, that the circuit consists of transistors together with inductor L_s, L and capacitor C (two-port A) can be characterized with four noise parameters R_n, B_{opt}, G_{opt}, F_{min} and they are known. Note $Y_{opt} = G_{opt} + jB_{opt}$, B_{opt} is negative and $|G_{opt}| < |B_{opt}|$ for CMOS transistors. We look for the new four noise parameters R'_n, B'_{opt}, G'_{opt}, F'_{min} of the circuits from Fig. 6.15 in relation with elements L_g and C_{pad}.

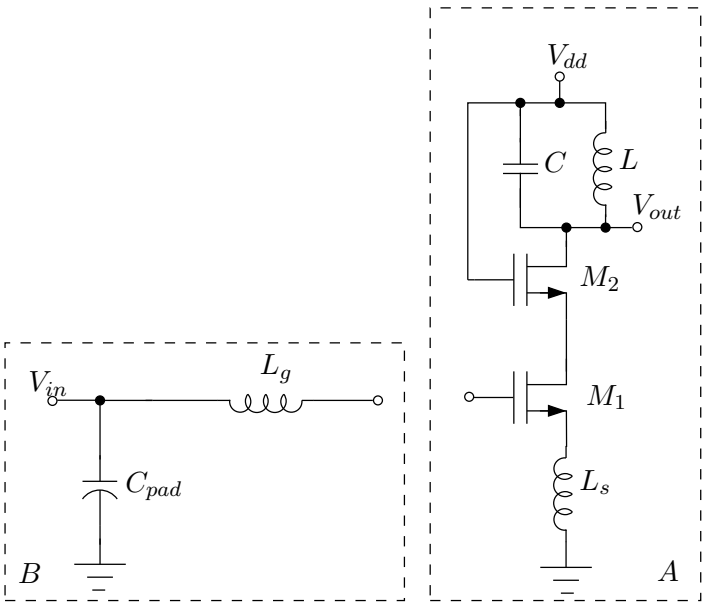


Fig. 6.15. Circuit for analysis pad capacitance with on-chip inductance

The inductor L_s is treated as an internal component of two-port A. In this case both two-ports A and B are connected in cascade and no information about the electrical matrix of two-port B is needed. The electrical matrix in chain representation of the two-port B, which consists of pad capacitance C_{pad} and on-chip inductance L_g can be expressed as

$$\mathbf{A_B} = \begin{bmatrix} 1 & j\omega L_g \\ j\omega C_{pad} & 1 - \omega^2 L_g C_{pad} \end{bmatrix} \tag{6.21}$$

The admittance representation of (6.21) has no real part, thus the noise correlation matrix $\mathbf{C_B}$ of this two-port is a zero matrix.

To obtain the chain representation of the noise correlation matrix of the new two-port, which consists of transistor two-ports A and B the formula

$$\mathbf{C_{A_{tot}}} = \mathbf{A_B} \cdot \mathbf{C_A} \cdot \mathbf{A_B}^{+} + \mathbf{C_B} \tag{6.22}$$

is used. $\mathbf{A_A}$ and $\mathbf{C_A}$ are the chain representations of electrical and noise matrices of two-port A, respectively, and $\mathbf{C_B}$ is the noise correlation matrix of two-port B.

Then, the noise parameters of the resulting two-port can be written as:

$$R'_n = d\,R_n \tag{6.23}$$

$$B'_{opt} = \frac{B_{opt}(1-2\omega^2 L_g C_{pad}) + \omega L_g |Y_{opt}|^2 - \omega C_{pad}(1-\omega^2 L_g^2 |Y_{opt}|^2)}{d} \tag{6.24}$$

$$G'_{opt} = \frac{G_{opt}}{d} \tag{6.25}$$

$$F'_{min} = F_{min} \tag{6.26}$$

$$d = (\omega L_g B_{opt})^2 + 2\omega L_g B_{opt} + (\omega L_g G_{opt})^2 + 1 \tag{6.27}$$

Solving (6.27) for L_g, the minimum achievable d factor is

$$d_{min} = \frac{G_{opt}^2}{G_{opt}^2 + B_{opt}^2} \tag{6.28}$$

It is easy to notice, that for d factor lower than *one* the equivalent noise resistance and thus the noise figure can be minimized. As shown in (6.27) and (6.28) the value of L_g has to be matched to the proper transistor dimensions and biasing since B_{opt} and G_{opt} according to (4.45) and (4.44) are the functions of transistor widths and bias conditions. In this case R_n and optimum source conductance G_{opt} are independent on the value of pad capacitance C_{pad}.

6.3.3. Influence of Pad Capacitance and Off-chip Inductance

The configuration for following analysis is shown in Fig. 6.16. Similar as in the previous case two-ports A and B are connected in cascade and inductor L_s is treated as an internal component of two-port A. The electrical matrix of the two-port B in chain representation, which consists of pad capacitance C_{pad} and off-chip inductance L_g can be expressed as

$$\mathbf{A_B} = \begin{bmatrix} 1-\omega^2 L_g C_{pad} & j\omega L_g \\ j\omega C_{pad} & 1 \end{bmatrix} \tag{6.29}$$

Since the admittance representation of (6.29) has no real part, the noise correlation matrix $\mathbf{C_A}$ of this two-port is a zero matrix. To obtain the noise correlation matrix in chain representation of a new two-port consisting of two-ports A and B, the formula (6.22) is used [96].

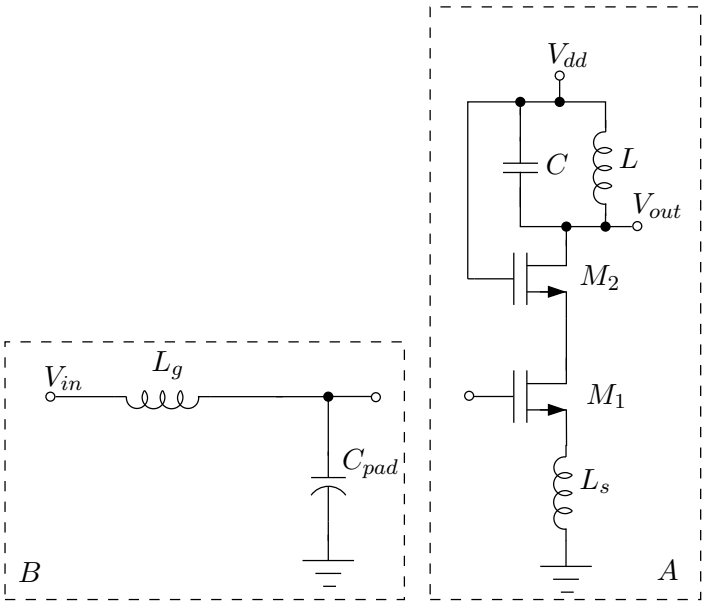


Fig. 6.16. Circuit for analysis of pad capacitance with off-chip inductance

Then, similarly to the previous case, the noise parameters of the new two-port can be expressed in terms of noise parameters of the already optimized two-port B as follows:

$$R'_n = d\,R_n \tag{6.30}$$

$$B'_{opt} = \frac{B_{opt}(1-2\omega^2 L_g C_{pad}) + \omega L_g |Y_{opt}|^2 - \omega C_{pad}(1-\omega^2 L_g C_{pad})}{d} \tag{6.31}$$

$$G'_{opt} = \frac{G_{opt}}{d} \tag{6.32}$$

$$F'_{min} = F_{min} \tag{6.33}$$

$$d = (\omega L_g B_{opt})^2 - 2(\omega^2 L_g C_{pad} - 1)\omega L_g B_{opt} + (\omega L_g G_{opt})^2 + (\omega^2 L_g C_{pad} - 1)^2 \tag{6.34}$$

Solving (6.34) for L_g yields to the minimum achievable factor d that can be written as

$$d_{min} = \frac{G_{opt}^2}{G_{opt}^2 + B_{opt}^2 + \omega C_{pad}(\omega C_{pad} - 2B_{opt})} \tag{6.35}$$

All noise parameters except F_{min} are dependent on L_g, C_{pad} and Y_{opt} values. Additionally, decreasing the d value improves the noise figure, as well.

In practice, the pad capacitance is given and designer has no freedom to change it. For this reason, the optimum values of L_g can be expressed as

$$L_{g_{opt}} = \frac{-B_{opt} + \omega C_{pad}}{\omega(\omega^2 C_{pad}^2 - 2\omega B_{opt} C_{pad} + G_{opt}^2 + B_{opt}^2)} \tag{6.36}$$

Analysis of optimum value of L_g leads to the conclusion, that optimum L_g value is lower for large transistor sizes than for small ones. Generally, the optimum value of L_g is independent on the supply current.

It can be also observed, that increasing C_{pad} lowers the values of $L_{g_{opt}}$. For small transistor sizes, it is even easier to notice. These considerations are very significant, since they prove that shielded pads not only do not deteriorate noise performance [97], but can be used to improve the noise performance.

6.3.4. Comparison of two input matching principle

In previous analysis has been shown that pad capacitance improve the noise performance. Comparison of (6.28) and (6.35) leads to a conclusion that pad capacitance C_{pad} in the amplifier shown in Fig. 6.1b reduce the factor d. Thus, this amplifier shows better noise performance because of reduced R_n'. Interestingly, C_{pad} is mostly treated as a parasitic component that has negative influence on the performance of the amplifier, especially on the noise performance [98].

To prove the mathematical investigations simulation have been performed [99]. Noise parameters for three different cases have been calculated:

1. cascode circuit without C_{pad}, L_g and L_s (two-port B in previous analysis).
2. cascode circuit with C_{pad}, L_g on-chip, 50 Ω matched (the LNA from Fig. 6.1a)
3. cascode circuit with C_{pad}, L_g off-chip, 50 Ω matched (the LNA from Fig. 6.1b).

The results for these three cases for 2 mA supply current are summarized in Tab. 6.1. Capacitance C_{pad} is 70 fF and the transistor widths are 48 and 96 μm for M_1 and M_2, respectively. The inductors L_s and L_g are ideal and are chosen according to (6.7) and (6.8) to fulfill input matching condition.

The off-chip solution for L_g (case 3) shows the following advantages:

1. The 50 Ω noise figure (NF_{50}) is about 0.6 dB lower as in the case of on-chip L_g.
2. L_g is much lower as in the on-chip case. This means less chip area and less losses.

Tab. 6.1. Summary of noise analysis

Case	R_n [Ω]	NF_{min} [dB]	B_{opt} [mS]	G_{opt} [mS]	NF_{50} [dB]	L_s [nH]	L_g [nH]
1	63.5	0.22	-0.86	0.4	3.6	—	—
2	12.4	0.25	-0.85	2.0	1.0	0.3	75
3	3.53	0.33	-0.12	9.0	0.4	1.2	39

3. The equivalent noise resistance R_n achieves the lowest value. This means a very flat noise paraboloid and insensitivity against noise mismatch.
4. The real part of G_{opt} is closest to 50 Ω matching (G_{opt} = 9 mS).

To show how the width of the transistors impacts the noise behaviour another analysis has been performed. Both transistors M_1 and M_2 have the same widths, supply current is constant and equal 2 mA and analysis frequency is 2.14 GHz. Transistors length is 0.13 μm and C_{pad} value is set to 70 fF. Simulation results are summarized in Tab. 6.2.

Tab. 6.2. Simulation results of amplifiers from Fig. 6.1a and Fig. 6.1b at 2.14 GHz for 2 mA supply current and different transistor sizes.

transistor width	24 μm		48 μm		96 μm	
L_g	on chip	off-chip	on chip	off-chip	on chip	off-chip
NF [dB]	1.04	0.25	0.92	0.34	0.54	0.35
Gain [dB]	25.42	15.71	23.08	16.67	19.39	15.69
M (noise measure)	0.27	0.06	0.24	0.08	0.13	0.09

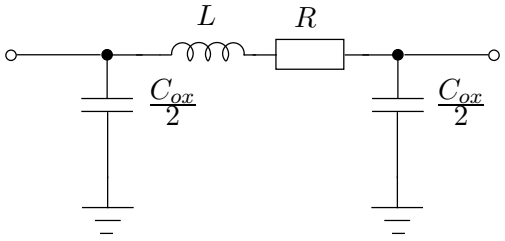
The amplifier with capacitance near the transistor's gate shows better results (noise measure M) in all cases. But for 96 μm the difference is not so significant. However, a supply current of 2 mA is too low for such a large transistors and this amplifier exhibit linearity issues.

Similar investigations with comparable results have been performed also for 1 and 5 mA supply current. Although absolute values of parameters are different, the trend observed for 2 mA is still valid. Since the analysis show that the LNA from Fig. 6.1b shown better performance, such an amplifier is designed and described later in this chapter.

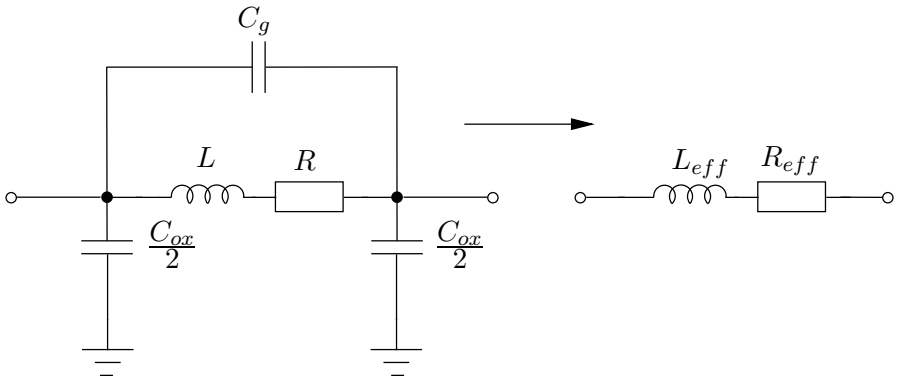
6.3.5. Influence of On-chip Enhanced Inductance

Large inductor L_g in the LNA shown in Fig. 6.1a can be avoided. A small capacitor can be placed in parallel with an on-chip inductor to achieve

a larger inductance [100]. A simplified inductor model (see section 3.1) is used for analysis, shown in Fig. 6.17(a): R is the total series resistance, C_{ox} is the total capacitance to the substrate and L is the inductance. As shown in Fig. 6.17(b), the equivalent inductor is obtained after placing a capacitor C_g in parallel.



(a) Simplified inductor model



(b) equivalent circuit with a parallel capacitor

Fig. 6.17. Increasing the equivalent inductance by parallel connection of a small capacitance C_g

The equivalent output impedance of this LC tank Z_{eff} is

$$Z_{eff} = \frac{(j\omega L + R)\frac{1}{j\omega(C_g + C_{ox})}}{j\omega L + R + \frac{1}{j\omega(C_g + C_{ox})}} = R_{eff} + j\omega L_{eff}, \tag{6.37}$$

where

$$R_{eff} = \frac{R}{1 - 2\omega^2 L(C_g + C_{ox}) + \omega^2(\omega^2 L^2 + R^2)(C_g + C_{ox})^2}, \tag{6.38}$$

$$L_{eff} = \frac{L - (\omega^2 L^2 + R^2)(C_g + C_{ox})}{1 - 2\omega^2 L(C_g + C_{ox}) + \omega^2(\omega^2 L^2 + R^2)(C_g + C_{ox})^2} \tag{6.39}$$

$$Q_{eff} = \frac{\omega(L - (\omega^2 L^2 + R^2)(C_g + C_{ox}))}{R} \tag{6.40}$$

Here R_{eff}, L_{eff} and Q_{eff} are the effective series resistance, effective inductance and quality factor, respectively. As one can expected for small C_g values, R_{eff} and L_{eff} increase while Q_{eff} decreases.

If the gate inductor L_g is implemented by this way, more than doubling of L_g value is possible. However, such an inductor has a lower Q [100]. Another problem that has to be taken into consideration is, that the equivalent series resistance of the gate inductor can not longer be neglected. This means, that R_{eff} contributes to the input impedance as well as the source inductor L_s, but in contrast to the L_s, introduces noise into the circuit.

6.4. Design Flow

Very briefly, the design starts with optimum transistor width, finger number and operating point, which have to be defined based on simulations for given power consumption. Noise parameter dependencies on transistor width and supply current result from these investigations. Next, a transistor is needed, whose impedance data at the gate together with the pad capacitance lead to the required real part of the input impedance. Finally, the external inductor at the gate together with the bonding-wire should be chosen so, that the imaginary part of the input impedance is cancelled. Linearity considerations finish the design.

Below the design procedure is explained in a more detailed way.

1. Design LC tank for wanted frequency.
2. Calculate the pad capacitance, take into account ESD structure and wiring.
3. Make transistor M_2 and M_1 equal to each other, as a first approximation.
4. Additionally choose the proper number of fingers in transistors.
5. Knowing pad capacitance find such a transistor size W that together with L_s give the wanted real impedance part. Choose the proper V_{od} value and check current consumption.
6. Design the L_g inductor to make full input matching, take the bonding wire into account.

7. Make the output matching, a properly chosen series blocking capacitor, together with a pad and a bonding wire are enough.
8. Check the gain of the amplifier and bandwidth, change the LC tank values if needed, (higher L means higher gain, but lowers the bandwidth). Change L_s if needed and go to point 3.
9. Simulate nonlinearities. P_{1dB} is improved by larger transistor, while larger V_{od} improves small signal nonlinearity (IIP3).
10. Change the size of the second transistor, taking into account gain, noise and linearity. The size of M_2 is negligible for input and output matching.
11. The design is finished.

Of course, like in all engineering problems an experience is needed for a fast and successful design.

The design flow presented here has been used for the design of an UMTS LNA. The layout of the amplifier is shown in Fig. 6.18. The presented structure consists of two independent amplifiers. However, they can be used together as a differential amplifier.

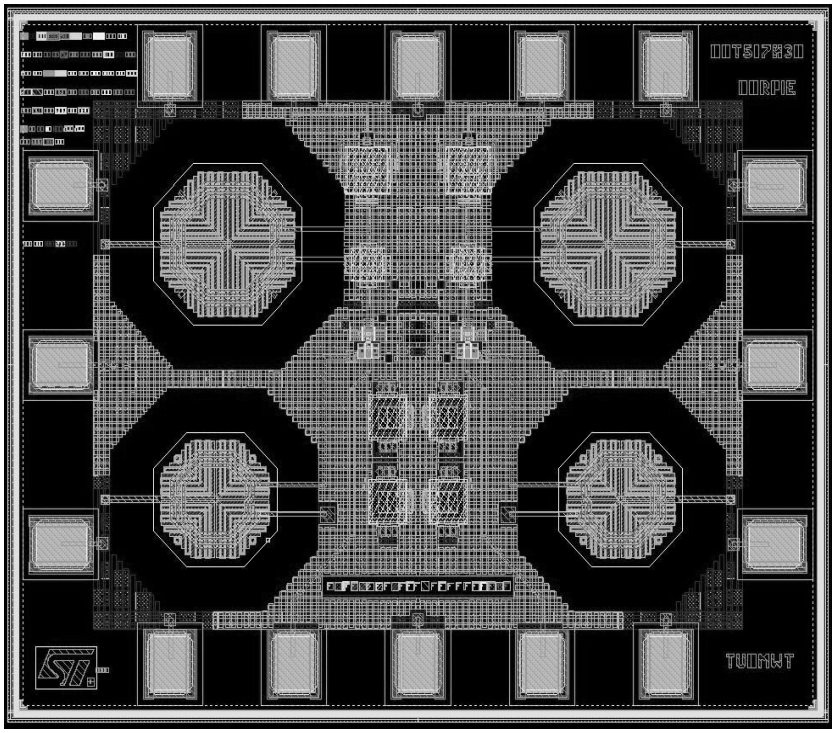


Fig. 6.18. Layout of the designed LNA

A balanced UMTS LNA has been designed by doubling the circuit shown in Fig. 6.1 and using the methodology of reducing the noise equivalent re-

sistance described in this chapter. The amplifier is designed for the 0.13 μm HCMOS process from STMicroelectronics.

The width of the transistors is 36 and 72 μm for M_1 and M_2, respectively. Both transistors are segmented into 4 μm-long gate fingers, and both ends of each finger are connected.

During the design process, there were two sources of information concerning the pad capacitance: a model of a pad and parasitic extraction process. Information taken from these sources was inconsistent. Therefore an assumption about C_{pad} was made, based on the parasitic extraction process. Furthermore, special design consideration was made using the parasitic extraction process, since the C_{pad} stands not only for the pad capacitance alone, but includes also wiring.

The both inductors L_s, and L has been taken from the library and have values of 1.6 and 3.8 nH, respectively. The L_g inductor, about 30 nH is placed off-chip. Post layout simulations of the single ended structure with all parasitic extracted show, that the simulated noise figure of the amplifier is only 0.1 dB larger then $\mathrm{NF}_{\mathrm{min}}$, while the gain is around 15 dB for 3.1 mA of the I_{ds} current.

The chip has no fixed gate bias voltage because of two well known facts: Even small changes of V_{gs} and V_{th} voltage change the I_{dd} current considerably. Furthermore the amplifier was designed for demonstrator reasons. For this purpose, external voltage supplies offers more experimental flexibility, too.

Chapter 7

LNA Measurements

In the first step, fabricated chips were pre-characterized on-wafer. Although they are differential structures they can be measured as single ended structures, since they do not posses any common current source. This was done because of much less expense compared to the differential case.

When the S-parameter of the chip were known, the test board with input and output matching circuits was designed and fabricated. In the last step the wire bonding between amplifier pads and the test board was performed.

Unfortunately, the total pad capacitance of the chip is larger than expected. Moreover, the transistor models used in simulation were not in good agreement with the measured behavior. To compensate the larger pad capacitance a more complicated input matching circuit, having more than one series inductance, is needed. This complicated input matching circuit, makes the comparison between simulated and measured results difficult. Therefore, only a series inductance was used for the input matching. Its value was chosen in this way, that the imaginary part of the input impedance is cancelled. As was already mentioned, because of larger pad capacitance the real part of input impedance is lower than 50 Ω. Although, it increases with rising the supply current of the amplifier, S_{11} values in the order of around 7 dB were achieved.

For this reason the measured gain is lower than the simulated one, and measured P_{1dB} is higher than simulated. Noise figure measurements and simulation are in good agreement.

In the following subsections the measurements are described in detail.

7.1. Measurement Test Bench

As already mentioned, all simulations and measurements presented in this thesis has been done for a single ended structure. Such measurements can be

easily transformed to differential measurements. For the same noise figure value the current has to be two times higher and the input referred P_{1dB} is 3 dB higher, too. Others parameters of the amplifier are unchanged.

The schematic of the test board is shown in Fig. 7.1. Elements TL1 – TL4 denote transmission lines, L_1, L_2 are inductors and bond is a bonding wire. The depicted test board contains input and output matching circuits.

Input matching circuits consists of a bonding wire modelled as an inductor, very narrow transmission line (TL2), the inductor L_1=12 nH from Coilcraft and a 50 Ω microstrip line (TL1), which is only for mechanical purposes. In the simulations, the S-parameter model from Coilcraft has been used for the inductor rather than pure, ideal inductor. Because the gate bias is applied the input matching circuit is DC coupled. Similarly to the input matching circuits the bonding wire was also taken into account in the output matching circuit and the S-parameter model for L_2 from Coilcraft has been used, too.

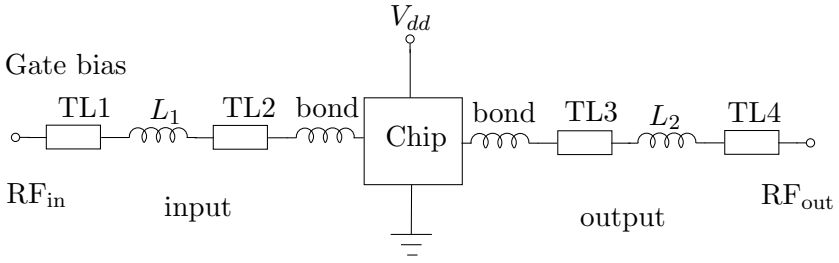


Fig. 7.1. Schematic of the test board used for the chip characterization

The layout of the test board is shown in Fig. 7.2. It consists of a chip structure facilitating bonding, input and output matching circuits and power supply structure. The board is fabricated using Rogers 4003 material (ϵ_r=3.4 and thickness equals to 0.51 mm). Board dimensions are 40 x 100 mm. The board was prepared for characterization by using a microstrip test fixture.

Similarly to the simulations presented in the previous chapter V_{dd} voltage is constant and set to 1.2 V for all measurements. The gate bias voltage V_{gs} is varied during the characterization.

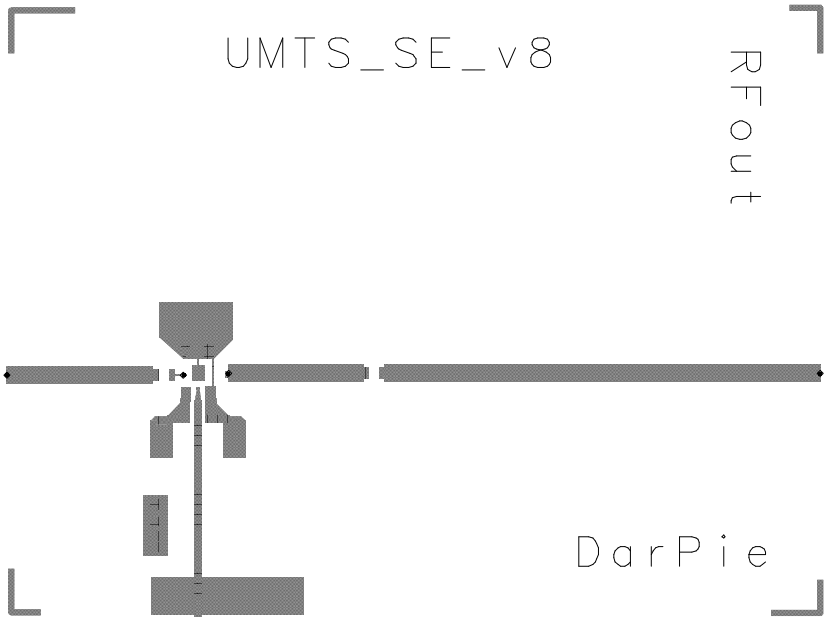


Fig. 7.2. The test board used for chip measurements

7.2. DC Measurements

Results of DC measurements are shown in Fig. 7.3 and Fig. 7.4. Fig. 7.3 shows the I_{dd} current versus gate bias voltage V_{gs}. A V_{gs} shift of around 30 mV between simulation and measurements can be noticed in linear region.

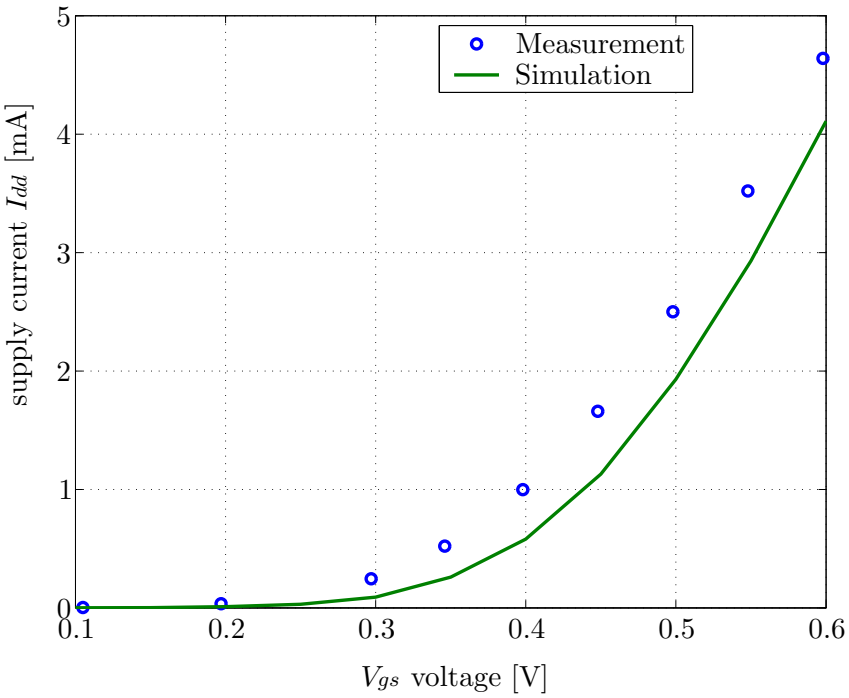


Fig. 7.3. Supply current I_{dd} versus V_{gs} voltage

This leads to a considerable transconductance difference at small V_{gs} bias voltage. This discrepancy vanishes with increasing V_{gs} more and more.

For small signal nonlinearity (IIP2, IIP3) of the amplifier the derivatives of the transconductance are important. Unfortunately, a reliable experimental determination of I_{dd} current was impossible because of too strong current fluctuations introduced by the oxidation of the pad contacts.

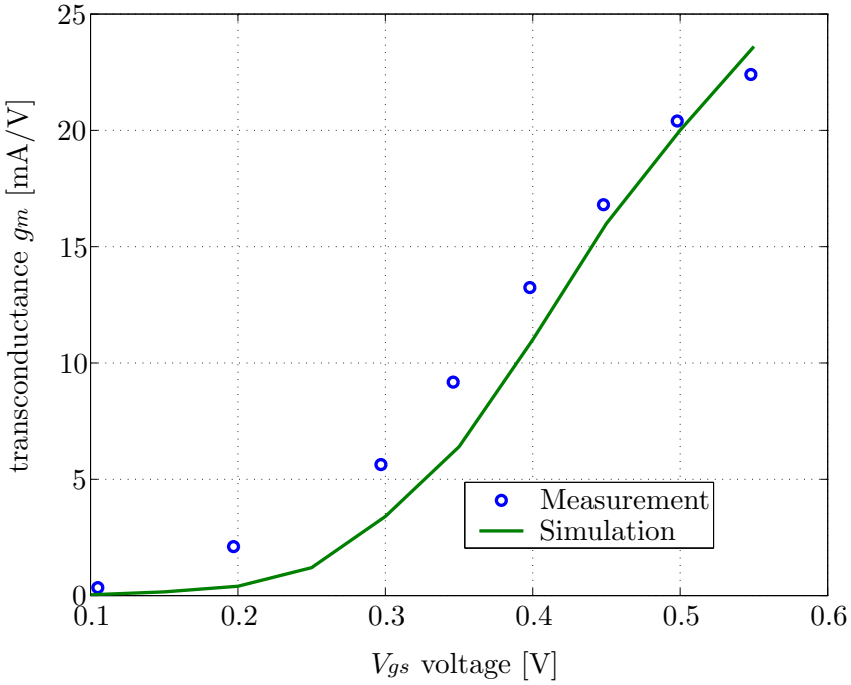


Fig. 7.4. Measured and simulated transconductance versus V_{gs} voltage

7.3. S-parameter Measurements

Results of S-parameter measurements for different drain source currents are shown in Fig. 7.5 – Fig. 7.8. In Tab. 7.1 results of S-parameters simulation

Tab. 7.1. Simulated S-parameters at 2.14 GHz

Current [mA]	S_{11} [dB]	S_{12} [dB]	S_{21} [dB]	S_{22} [dB]
1	-17	-43	14.0	-36
1.7	-23	-43	15.7	-33
2.5	-32	-43	16.7	-31
3.5	-33	-43	17.2	-29
4.6	-29	-43	17.4	-28

at 2.14 GHz are collected. Particularly measured S_{11} differs from simulated one. As written, it is the reason of too large pad capacitance.

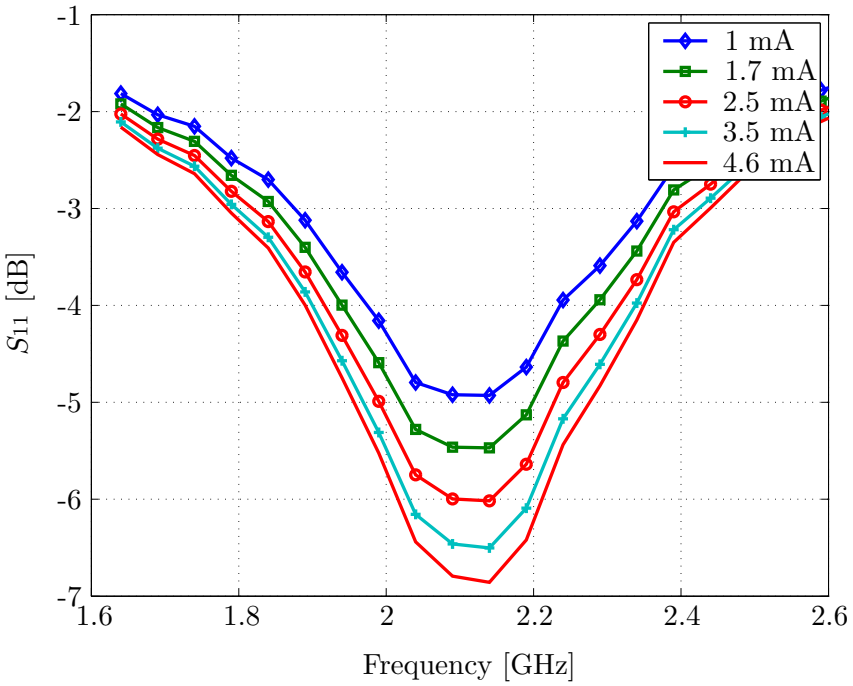


Fig. 7.5. Measured S_{11} versus frequency for various currents I_{dd}

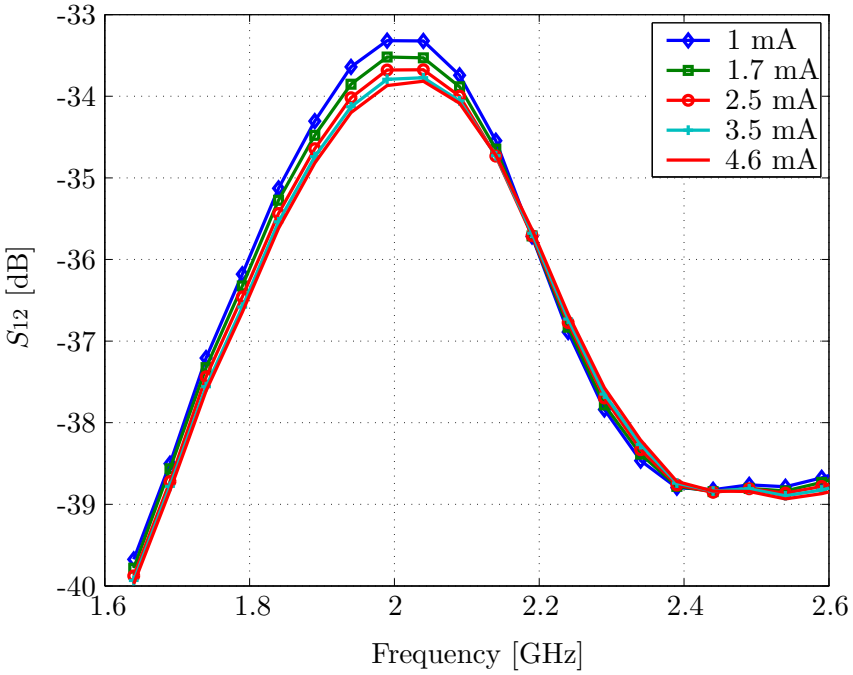


Fig. 7.6. Measured S_{12} versus frequency for various currents I_{dd}

Output matching (Fig. 7.8) and reverse transmission (Fig. 7.6) show rather small dependence on the drain source current. This is because these

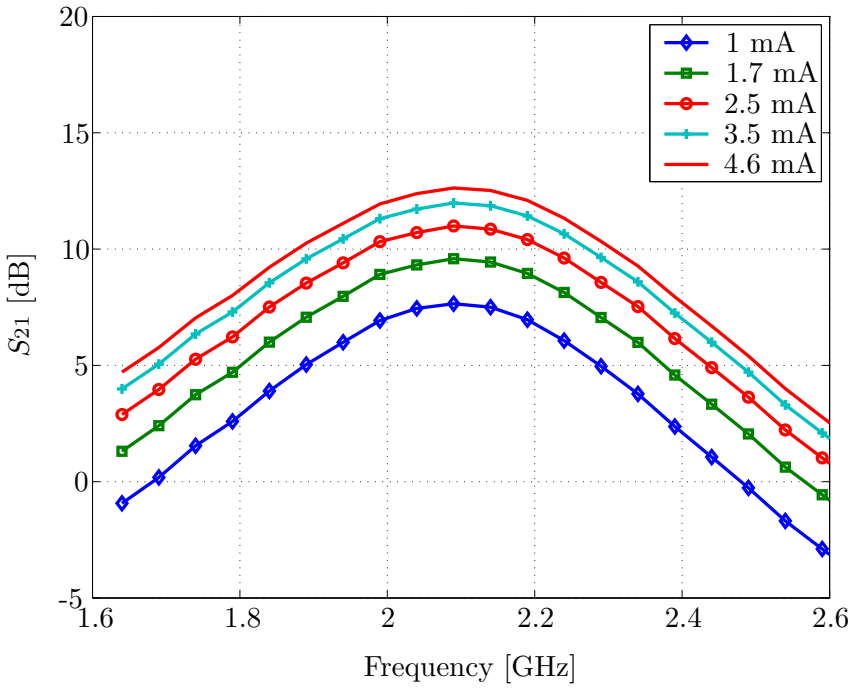


Fig. 7.7. Measured S_{21} versus frequency for various currents I_{dd}

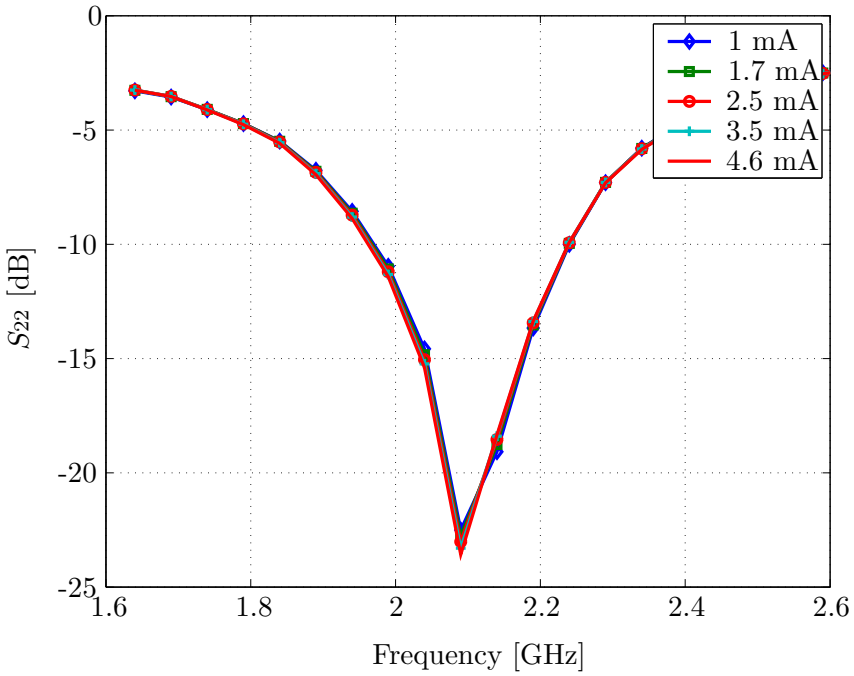


Fig. 7.8. Measured S_{22} versus frequency for various currents I_{dd}

parameters dependent only on the passive components of the amplifier. Excellent performance has been achieved for the output matching, too. Input return loss and gain are bias dependent. Higher currents increase the gain and improve the input matching. This is because the transconductance is higher and the input impedance is closer to 50 Ω.

7.4. Noise Figure Measurements

The results of the amplifier noise measurements are shown in Fig. 7.9 – Fig. 7.13. The measured and simulated noise figure of the amplifier is compared for five different drain supply currents I_{dd}. The measured characteristics differ considerably from measured ones. For this behaviour some reasons can be enumerate.

Firstly, working DECT telephony introduces peaks visible in all measurements in the frequency band of around 1.8 GHz. Such disturbing peaks are also visible in the UMTS frequency range (2.11 – 2.17 GHz), since the UMTS base stations works near the laboratory.

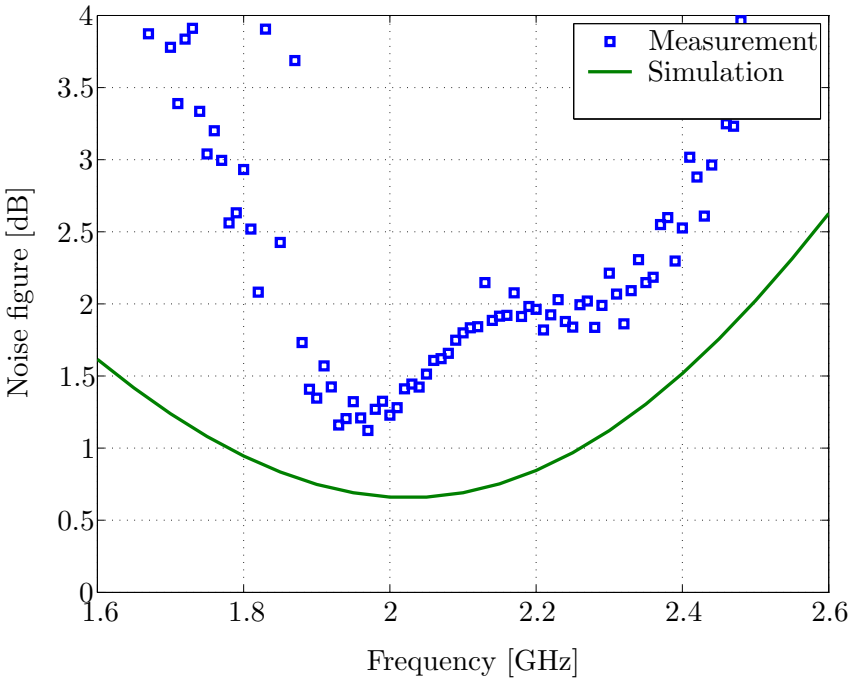


Fig. 7.9. Measured and simulated noise figure versus frequency for supply current $I_{dd} = 1$ mA

Except the peaks, in the band of interest there is also a bump of noise figure values. One of the possible explanation of this behaviour is the working

UMTS standard, which introduce errors (in the shape of this bump) in measurements. The LNA is designed to work in the UMTS frequency range by its input and output matching and a narrow bandwidth of gain characteristics. Additionally, it can be assumed, that the UMTS signal present in laboratory has a constant power in the whole frequency range, except the peaks mentioned above. For these reasons the shape of the gain characteristic appears in the noise figure measurements. To avoid this effect, the measurements in electromagnetic chamber could be helpful.

However, the suboptimum design can both deepened or even caused this problem. As written, pad capacitance affects both input power match and noise performance of the LNA. Since the pad capacitance is larger than assumed, it could be also the reason of the hill in the measured noise characteristic. At last but not least, a similar hill in the band of interest can bee seen in other publications e.g., [84], [101].

The minimum value of the noise figure as a dependency of the supply current is shown in Fig. 7.14. This figure shows, that with increasing current I_{dd} the noise figure drops. This lead to a trade-off situation between current consumption and noise figure [102].

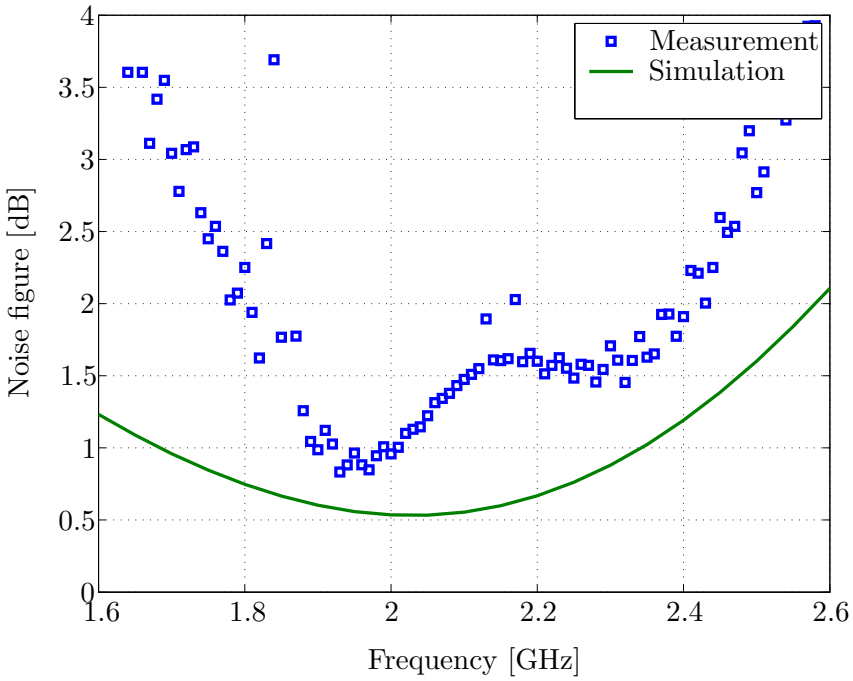


Fig. 7.10. Measured and simulated noise figure versus frequency for supply current $I_{dd} = 1.7$ mA

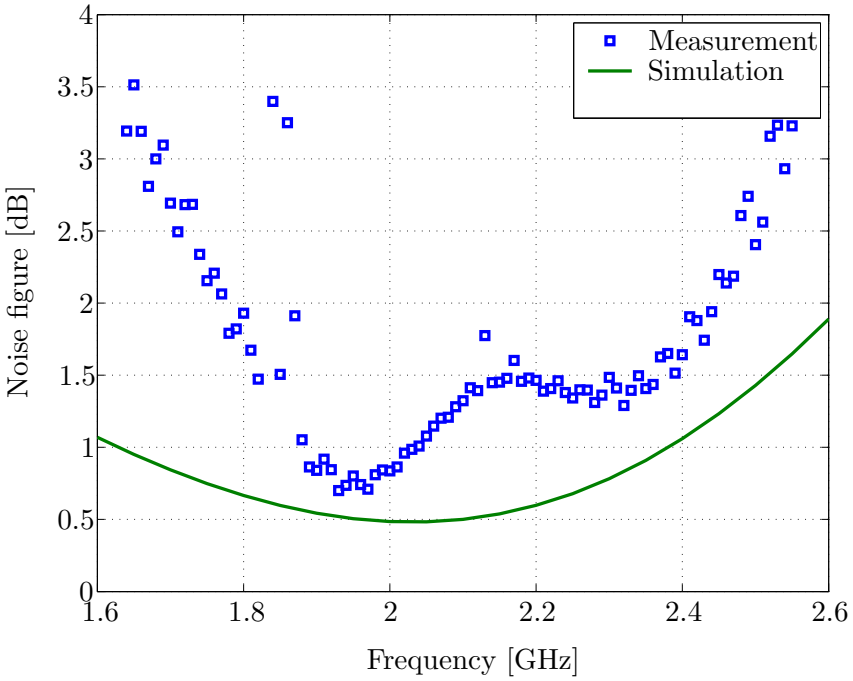


Fig. 7.11. Measured and simulated noise figure versus frequency for supply current $I_{dd} = 2.5$ mA

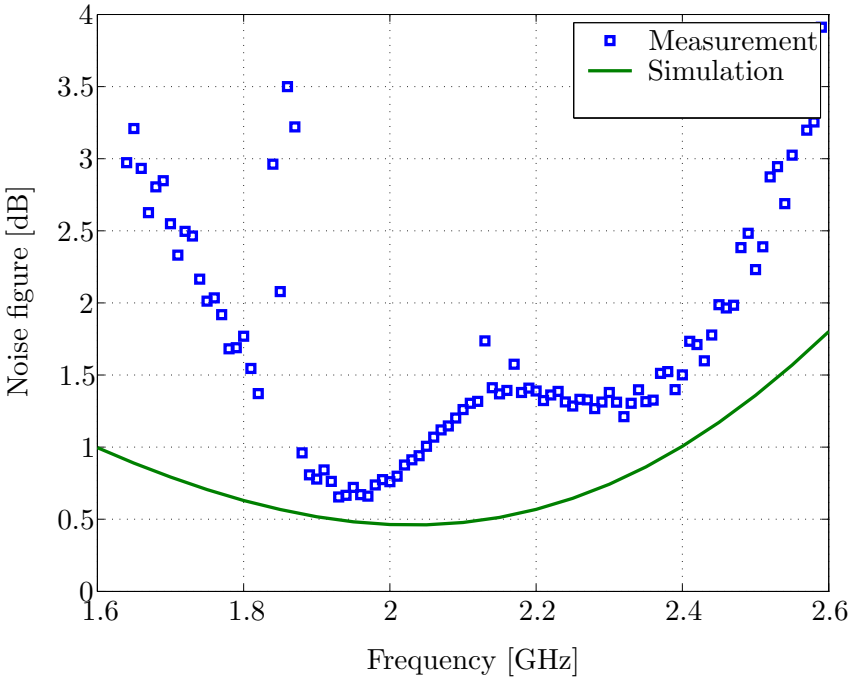


Fig. 7.12. Measured and simulated noise figure versus frequency for supply current $I_{dd} = 3.5$ mA

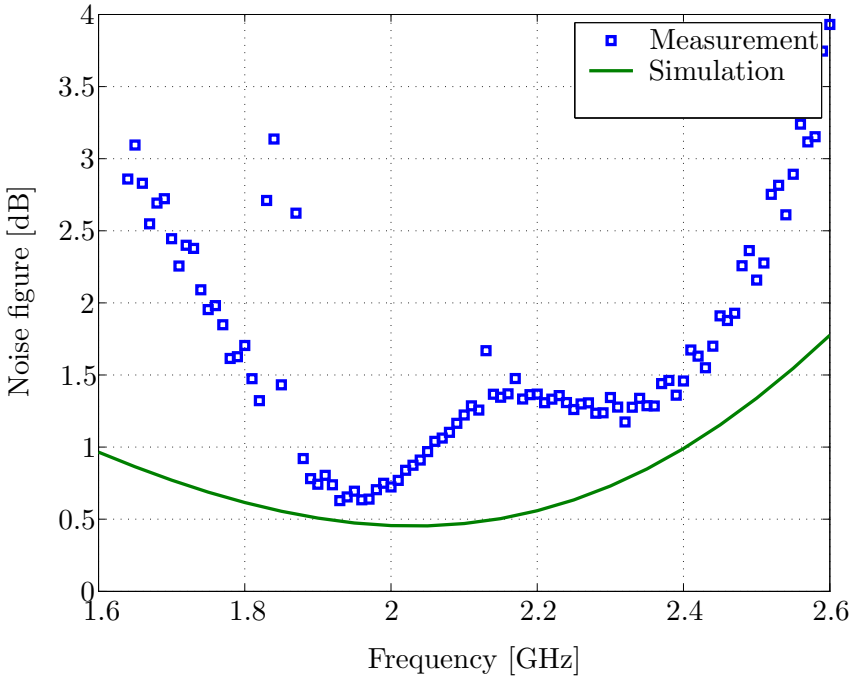


Fig. 7.13. Measured and simulated noise figure versus frequency for supply current $I_{dd} = 4.6$ mA

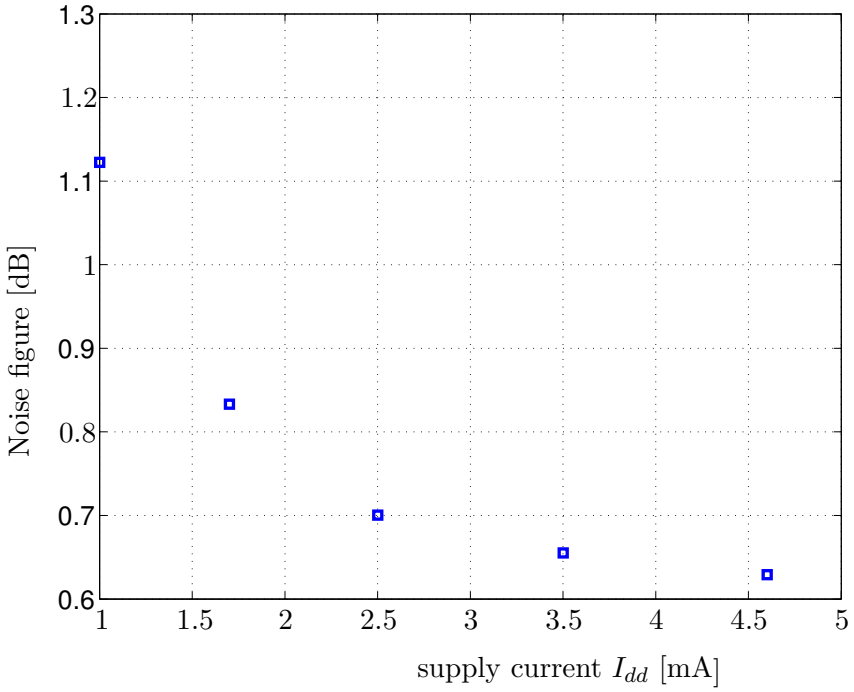


Fig. 7.14. Minimum value of the measured noise figure versus supply current I_{dd}

7.5. Compression Measurements

The gain compression behavior of the amplifier is shown in Fig. 7.15. The amplifier gain versus input power for different supply currents I_{dd} is presented. The compression points P_{1dB} are shown as small circles. As already mentioned measured values are higher than simulated ones. However, the differences between them vary.

Compression measurement for 1 mA supply current needs an explanation. Although largest value of P_{1dB} has been achieved, the amplifier work in nonlinear range, because its gain versus input power is not constant, and even increases with increasing input power.

Additionally small signal nonlinearities IIP3 has been measured. The results are shown in Tab. 7.2 in the next subsection.

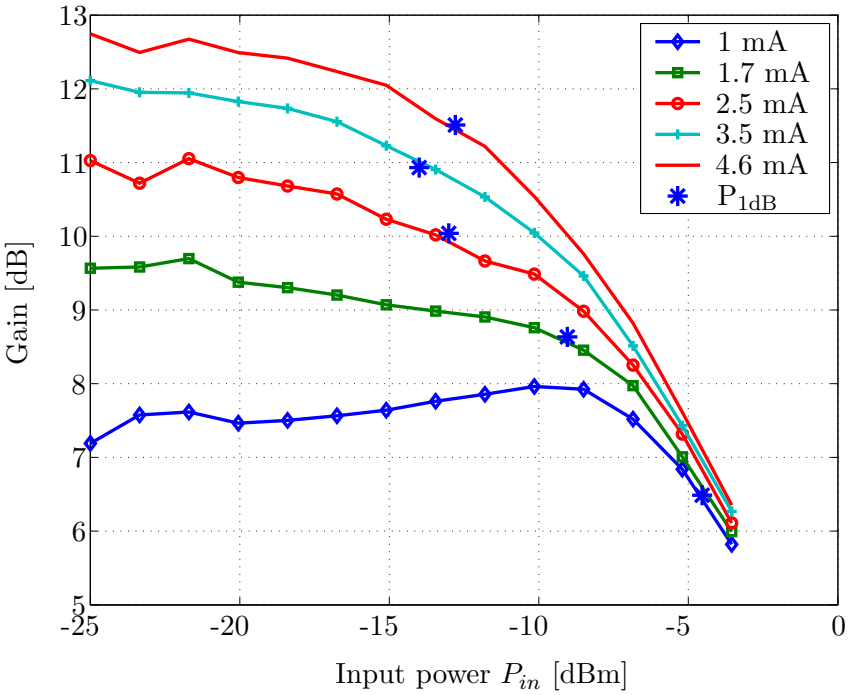


Fig. 7.15. Measured input referred P_{1dB}

7.6. Comparison with State-of-the-art Amplifiers

The measured results of the designed LNA are collected in Tab. 7.2. The most important amplifier characteristics like the input and output matching, noise figure and gain are shown for various supply currents.

This table can be used for choosing the best operating point of this amplifier with respect to all parameters collected in this table. For further

Tab. 7.2. Summary of measurements

Current [mA]	S_{11} [dB]	Gain [dB]	S_{22} [dB]	NF [dB]	Input P_{1dB} [dBm]	IIP3 [dBm]
1	-5	7.5	-23	1.1	-4.5	-1.9
1.7	-5.5	9.5	-23	0.85	-9	-3.7
2.5	-6	11	-23	0.8	-13	-3.5
3.5	-6.5	12	-24	0.76	-14	-2.5
4.6	-6.8	12.5	-24	0.72	-13	-1.7

comparison with state-of-the-art amplifiers supply current equals to 3.5 mA is chosen.

In [83], [103], [104], [84] there are also very good results achieved concerning the noise figure and current consumptions. All these designs have the pad or ESD structure capacitance connected between gate and source or ground (base and emitter in bipolar technology), as it is analyzed in section 6.3.3. Although in publications mentioned above other types of analysis are performed the conclusions are similar to these addressed in this thesis.

Tab. 7.3. Comparison with other publications

Freq. [GHz]	P_{dc} [mW]	S_{11} [dB]	Gain [dB]	S_{22} [dB]	NF [dB]	Input P_{1dB} [dBm]	IIP3 [dBm]	Ref.
1.22	9	-11	20	-11	0.8	n.a	-11	[84]
5.75	16	n.a.	14.2	-8	0.9	-17	0.9	[101]
0.9	17.6	-10	15	-27	0.85	n.a.	1	[104]
2	10.8	-12	15	-22	0.7	-9.5	6	[105]
1.5	30	-7	22	n.a	3.5	-22	-10	[90]
2.1	50	-8	14	n.a	2.1	-13	n.a.	[106]
2.45	10	-25	14	n.a.	2.3	-8.5	0	[107]
1.9	9	n.a.	17.5	n.a	1.6	n.a.	-6.8	[71]
5.8	n.a.	n.a.	12	n.a.	4	n.a.	n.a.	[87]
2.1	**4.2**	**-6.5**	**12**	**-24**	**0.76**	**-14**	**-2.5**	**This work**

The technology comparison presented in [105] shows that achieved results concerning the noise figure, gain and current consumption are in the best of achievable values. In Tab. 7.3 some recently published LNAs are presented. This comparison proves also, that designed amplifier belongs to the best reported.

Chapter 8

Conclusion

The focus of this thesis is CMOS low noise amplifier design for a reconfigurable mobile system. The LNA is not reconfigurable itself. However, designed amplifier can be use improved with on-off function by connecting the gate of the transistor M_2 through a switch to the V_{dd} or ground. The thesis addresses also issues in range from high level system simulation down to the circuit physics.

In scope of this work the multistandard, reconfigurable terminal is considered that supports, however not simultaneously, the OFDM based WLAN standards (IEEE802.11 and Hiperlan/2) and CDMA based UMTS FDD standard. Special investigation has been made on the receiver of this terminal.

After defining the obvious need of reconfigurability, general information on reconfigurable transceivers is given. Further the inspection of the supported standards is shown and receiver requirements for each standard are derived.

Reconfigurable RF receiver architecture is also one of the main topic in this work. In the ideal case, in the software defined radio approach only the antenna and a wide band low noise amplifier is needed. Many obstacles, however, make this approach impossible at least at the time being. There is a tendency to reduce the number of conversion stages in the transceiver, thus the direct conversion principle is applied more and more. On the other hand, there is also a tendency to reuse the functional blocks in multistandard transceivers, rather than using many parallel switchable transceivers. Based on this consideration, a reconfigurable hybrid architecture has been developed. Although, not fully integrated on chip, this architecture is a good solution for multistandard systems, which operates at different frequency bands.

Additionally to the investigation of hybrid architectures, the study on RF impairments is given. Most important RF impairments are described in

detail, very often accomplished with baseband signal model for use in high level system simulations. The RF impairments can be divided into three groups. The first group of impairments (e.g., nonlinearity) can be reduced only in the baseband. The impairments belonging to the second group can be reduced only in the frontend, just at that place where they come from. The last group of impairments (e.g., DC offset, I/Q imbalance), can be reduced by using signal path optimization techniques in the frontend and baseband, as well. In signal path optimization approach, RF impairments are evaluated in the baseband and on this base the correction signals are generated, which control various frontend blocks.

The second part of this work describes RF-MOS devices and low noise amplifier design for reconfigurable receivers. Firstly, the noise performance of a transistor is under consideration, e.g., transistor parasitic elements that lowers the available noise figure.

Small FET devices of state of the art sub-micron RF-MOS-technologies have low capacitance values, thus large inductors are needed for matching. Because of their large dimensions they have to be placed off-chip. For this reason, the pad capacitance can not be longer neglected in the design process. Based on the two-port noise theory it is shown, that the pad capacitance, although very often treated as a parasitic capacitance, is very important for noise performance. This fact has been already reported so far, but the extensive study presented in this thesis is novel. It is shown for a cascode amplifier, that the consideration of the pad capacitance into the optimization process can lead to a decreased noise figure because of a reduced equivalent noise resistance. In other words, the noise figure of low-noise amplifiers can be improved considerably by taking into consideration all passive components very carefully. The design methodology is introduced, which reduces the equivalent noise resistance and thus excellent noise performance can be achieved in spite of rather poor noise matching.

The characterization of the amplifier, with respect to the noise performance and power consumption, confirms the simulations with good agreement. The designed amplifier shows 0.76 dB noise figure and 12 dB gain at 2.14 GHz for 3.5 mA supply current and 1.2 V supply voltage. This results belong to the knowledge of the author to the best ever reported.

Appendix A

Cascode Amplifier

The schematic of a cascode LNA is typically quite different from its real structure. Because of the physical properties of the transistor layout, wiring and physical process constrain parasitic elements like inductors, resistors, capacitors and even transistors and diodes appear in the circuit.

The designer can decrease the parasitic elements by proper layout techniques as discussed in 4.3.2, but parasitics (even very small) are unavoidable. Thus, additional elements are needed that can compensate parasitic elements.

The schematic of a layouted cascode LNA, which includes the most important parasitics and compensation components is presented in Fig. A.1. The parasitic elements are: L_{bond}, L_p, C_{sb} and C_p. Cascode amplifiers, while having good isolation S_{21}, are prone to oscillate if some precautions are not taken.

First, the gate of the cascode transistor (M_2) has to be connected to V_{dd} by a resistor R. Actually, the gate-drain capacitance of the cascode transistor in series with the equivalent inductor L_p of the V_{dd} connection and the bondwire L_{bond} create an LC resonator, which can create a low impedance path to ground (from the drain of M_2). The inductor at the gate of a common gate transistor can implement an oscillator (inductive feedback).

Secondly, the transistor M_1 presents a capacity to the source of the cascode transistor. This is together with its own gate-source capacitance a capacitive degeneration of M_2. A capacitive degeneration can create a negative input impedance at the gate of M_2, which degrades the stability. The gate should be tied to ground trough a capacitor that acts as an AC short for high frequencies. Moreover, a resistor of 2k - 5k parallel to C_b may be added between gate of M_2 and ground.

Besides of this issues other problems exist that are related to source degeneration itself. In scope of this work, we assume that source degeneration is solely inductive. Actually, the parasitic capacitance C_{sb} is physically present

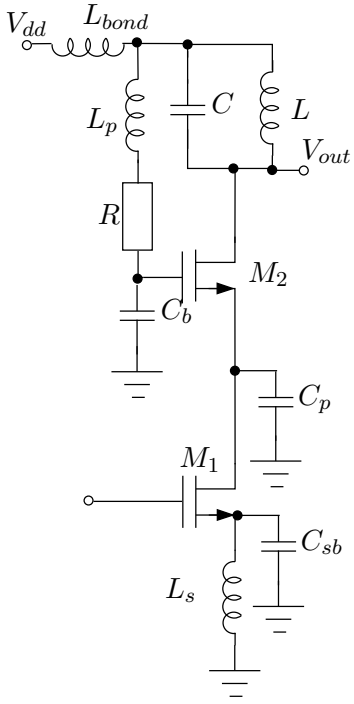


Fig. A.1. Parasitic components in the cascode amplifier

and impedance of the source degeneration $Z_s = j\omega L_s$ becomes more complicated

$$Z_s = \frac{j\omega L_s}{1 - \omega^2 L_s C_{sb}}. \tag{A.1}$$

Note, for $\omega^2 L_s C_{sb} > 1$ the effective inductance becomes negative. Since the real part of input impedance $((g_m L_s)/C_{gs})$ is proportional to L_s, the real part of input impedance becomes negative and the circuit oscillates.

Appendix B

Electrical Chain Matrix of Cascode Amplifier

In a cascode amplifier there is a cascade connection of the common source and common gate amplifier. For the noise analysis the electrical matrix of this connection is needed.

The electrical admittance matrix of the MOSFET in common-source configuration is

$$Y_{cs} = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ g_m - j\omega C_{gd} & g_{ds} + j\omega C_{gd} \end{bmatrix} \tag{B.1}$$

In turn, the electrical admittance matrix of a MOSFET in common-gate configuration is

$$Y_{cg} = \begin{bmatrix} -j\omega C_{gs} - g_m - g_{ds} & -g_{ds} \\ g_m - g_{ds} & g_{ds} + j\omega C_{gd} \end{bmatrix} \tag{B.2}$$

To calculate resulting Y matrix of the cascode amplifier, both Y_{cs} and Y_{cg} should be converted to the chain representation and then multiplied. Assumed that both transistors have the same small signal parameters, after back conversion from chain to admittance matrix, the resulting admittance parameters of the cascode stage is:

$$Y_{11} = -\frac{\omega(-2jC_{gs}g_{ds} + 2\omega C_{gs}C_{gd} - 2jC_{gd}g_{ds} + \omega C_{gs}^2 + jC_{gs}g_m)}{j\omega(C_{gd} + C_{gs}) + 2g_{ds} - g_m} \tag{B.3}$$

$$Y_{12} = \frac{j\omega g_{ds}C_{gd}}{j\omega(C_{gd} + C_{gs}) + 2g_{ds} - g_m} \tag{B.4}$$

$$Y_{21} = \frac{(-g_m + j\omega C_{gd})(g_m - g_{ds})}{j\omega(C_{gd} + C_{gs}) + 2g_{ds} - g_m} \tag{B.5}$$

$$Y_{22} = \frac{-g_{ds}^2 - 3j\omega C_{gd}g_{ds} + \omega^2 C_{gd}^2 - j\omega C_{gs}g_{ds} + \omega^2 C_{gs}C_{gd} + j\omega C_{gd}g_m}{j\omega(C_{gd} + C_{gs}) + 2g_{ds} - g_m}. \tag{B.6}$$

It can bee seen, that even with the assumption of identity of the small signal parameters of both transistor the equations (B.3)-(B.6) are complicated and their use for noise analysis is difficult. However, further assumptions can

be done concerning the C_{gd} capacitance and g_{ds} value. With the C_{gd} equals to zero and $g_m >> g_{ds}$ the admittance parameters of cascode transistor connection can be simplified to:

$$Y_{11} = j\omega C_{gs} \tag{B.7}$$

$$Y_{12} = 0 \tag{B.8}$$

$$Y_{21} = -\frac{g_m(g_m - g_{ds})}{2g_{ds} + j\omega C_{gs} - g_m} \approx -\frac{g_m^2}{j\omega C_{gs} - g_m} \tag{B.9}$$

$$Y_{22} = \frac{g_{ds}(g_{ds} + j\omega C_{gs})}{2g_{ds} + j\omega C_{gs} - g_m} \approx \frac{g_{ds}(g_{ds} + j\omega C_{gs})}{j\omega C_{gs} - g_m}. \tag{B.10}$$

Appendix C

Simultaneously Power and Noise Matching in LNA

For the sake of simplicity, induced gate noise is very often neglected in LNA design. In this chapter, based on two-port theory it is shown, that such an assumption leads to errors, particularly for low frequencies.

According to (4.44) and (4.45) the optimum source conductance and reactance can be written as:

$$B_{opt} \approx -\alpha\omega C_{gs} \tag{C.1}$$

$$G_{opt} \approx \beta\omega C_{gs} \tag{C.2}$$

where α and β are bias and technology dependent constants.

If we connect the source inductance L_s the optimum source conductance and reactance according to (6.16) - (6.20) can be written as:

$$B_{opt} = \frac{\omega C_{gs}(\omega^2 L_s C_{gs}(\alpha^2+\beta^2) - \alpha)}{d_{Ls}} \tag{C.3}$$

$$G_{opt} = \frac{\beta\omega C_{gs}}{d_{Ls}} \tag{C.4}$$

where

$$d_{Ls} = 1 - 2\alpha\omega^2 L_s C_{gs} + \omega^4 L_s^2 C_{gs}^2(\alpha^2+\beta^2) \tag{C.5}$$

After connecting the inductance L_g to the two-port and by neglecting the pad capacitance C_{pad} according to (6.34), the d term can be found as follows:

$$\begin{aligned} d_{Lg} =& \frac{\omega^4 L_s^2 C_{gs}^2(\alpha^2+\beta^2) + \omega^4 L_g^2 C_{gs}^2(\alpha^2+\beta^2)}{1 - 2\alpha\omega^2 L_s C_{gs} + \omega^4 L_s^2 C_{gs}^2(\alpha^2+\beta^2)} \\ &+ \frac{2\omega^4 L_g L_s C_{gs}^2(\alpha^2+\beta^2) - 2\alpha\omega^2 C_{gs}(L_s+L_g)}{1 - 2\alpha\omega^2 L_s C_{gs} + \omega^4 L_s^2 C_{gs}^2(\alpha^2+\beta^2)} \end{aligned} \tag{C.6}$$

It can be found that the minimum value of d_{Lg} depends on the inductances L_s and L_g. However, although an optimum value of L_s exists, this does not lead to the useful practical results, since neither g_m nor source resistance

R_s are taken into account. For this reason only the optimum value of the inductance L_g can be found.

It is easy to verify, that the inductance L_g, which minimizes the factor d_{Lg} is

$$L_g = \frac{\alpha - \omega^2 L_s C_{gs}(\alpha^2 + \beta^2)}{\omega^2 C_{gs}(\alpha^2 + \beta^2)} \tag{C.7}$$

The L_g value, that is needed for input matching at angular frequency ω_0 according to (6.2) is

$$L_g = \frac{1 - \omega_0^2 L_s C_{gs}}{\omega_0^2 C_{gs}} \tag{C.8}$$

A comparison of equations (C.8) and (C.7) shows that they do not lead to the same result.

Some assumption for the bias dependent parameters α and β are made now. If the long channel theory is taken into account, $g_m = g_{d0}$, $\delta = 4/3$, $\gamma = 2/3$, $\zeta = 1/5$ and thus $\alpha \approx 0.75$ and $\beta \approx 0.58$. With this numbers the difference between L_g values calculated from (C.7) and (C.8) is around 17%. Since the inductor L_g is rather large (about 25 nH or even more for 2 GHz) noise and power matching can not be obtained simultaneously. Because the needed value of inductor L_g decreases with frequency, noise and power matching is easier to obtain at higher frequencies, However, with increasing frequency the noise performance automatically worsens.

The induced gate noise is very often neglected in LNA design (e.g. [107]). With this assumption ($\alpha = 1$ and $\beta = 0$) L_g values calculated from (C.7) and (C.8) are the same. It proves the fact the power and noise matching can be achieved simultaneously only with the induced gate noise neglected. This conclusion can be also found in [108].

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Nomenclature

λ	Channel length modulation parameter
μ_n	The electron mobility
ω_0	resonant angular frequency
ω_T	Transit frequency
C_{ox}	The oxide capacitance
g_m	Transconductance of the MOS transistor
g_{d0}	The value of g_{ds} evaluated at zero V_{ds}
Q	Quality factor
R_s	source resistance
V_{gs}	Gate source voltage
V_T	Threshold voltage
W, L	Device dimensions
3GPP	Third generation partnership project
$\mathrm{P_{1dB}}$	1-dB compression point
ACS	Adjacent channel selectivity
AD	Analog to digital converter
BB	Baseband
BER	Bit error rate
CDMA	Code division multiply access
CG	Coding gain
CMOS	complementary metal-oxide silicon
DC	Direct current
DCR	Direct conversion
DL	Down link
DSP	Digital signal processor
FDD	Frequency division duplex
FE	Front-end
IF	intermediate frequency

IIP2	Input intercept point of second order
IIP3	input intercept point of third order
LNA	Low noise amplifier
LO	Local oscillator
OCNS	Orthogonal channel noise simulator
OFDM	Orthogonal frequency modulation
PSD	Power spectrum density
RF	Radio frequency
RFVGA	Radio frequency variable gain amplifier
SDR	Software defined radio
SG	Spreading gain
SNR	Signal to noise ratio
SPO	Signal path optimization
UL	Up link
UMTS	Universal mobile telecommunication system
UTRA	Universal terrestrial radio acces
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier
WLAN	Wireless local area network
ZIF	Zero intermediate frequency

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