Wide-band mixing DACs with high spectral purity

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Elbert Bechthum

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PROEFSCHRIFT

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Want de wijsheid van deze wereld is dwaasheid bij God, ...
1 Korinthe 3 : 19

Contents

1 Introduction

Humans are social creatures by nature and hence they strive for communication. Communication can be defined as 'The imparting or exchanging of information by speaking, writing, or using some other medium' [1]. The way we communicate over large distances has changed drastically throughout history. In the past, people used for instance drums, fire beacons, or written forms. More recently, electronic forms of communication gained popularity. The invention of wireless signals enabled an evolution of hand-held devices which changed the way people connect to each other. Although these electronic devices offer a wide range of possibilities, it is said that extensive use will alter our ability for normal face-to-face communication. Nowadays, people are continuously on-line and they expect to be able to access information and interact with people at any time and place. To achieve this, wireless connectivity is massively used.

To maximize the amount of information in wireless signals, high signal bandwidth and high spectral efficiency of the signal is required. High spectral efficiency is required to maximize the information rate in the available bandwidth. An overview of a hypothetical signal spectrum is shown in Figure 1.1. The indicated spectral purity is in this work defined as the ratio between the desired signal and the undesired signal components. These undesired signal components include noise, harmonic distortion and disturbances. Fundamentally there are two domains, which define the spectral efficiency: time and amplitude. Since the spectrum is strictly regulated and partitioned, the bandwidth of the available band is limited. It can be seen in Figure 1.1 that spectral impurities cause the effective signal bandwidth to be less than the bandwidth of the available band. A lower level of spectral impurities results in less unused bandwidth, see Figure 1.1. Hence, to efficiently use the available band and thus maximize the information in the time domain, a transmitter with high spectral purity is required. To maximize the use of the amplitude domain within the signal bandwidth, advanced modulation methods are used, e.g. QAM, OFDM etc. For accurately

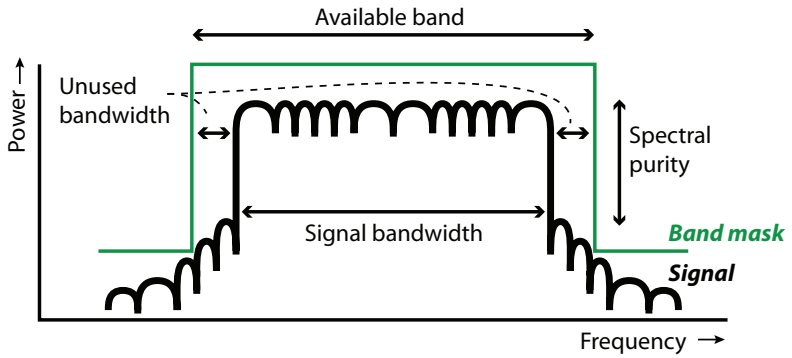


Figure 1.1: Maximum signal bandwidth depends on the bandwidth of the available band and on the spectral purity

reproducing these high-resolution signals, a transmitter with high spectral purity is required too.

Various wireless standards exist, which all have their own specific requirements. Some standards have narrow-band signals but require a high spectral purity, e.g. GSM. Especially for basestations which transmit multicarrier signals, the required spectral purity is high. For multicarrier GSM, a spectral purity of more than 80dBc is required [2], see also Chapter 2. Other standards require a lower spectral purity but have a large signal bandwidth, e.g. LTE. Therefore, a universal transmitter that covers all standards, should have both high linearity *and* large bandwidth. Various high spectral purity applications and wide-band applications operate at multi-GHz frequencies, e.g. multicarrier GSM at 0.5-2GHz. These performance figures and the exemplary application of multicarrier GSM are further discussed in Chapter 2.

Two core functions of a transmitter are the digital-to-analog conversion and the mixing to the RF frequency. This research shows that it is advantageous to implement both functions together using a Mixing-DAC. A Mixing-DAC is defined in this work as a *single integrated design* which implements both a mixing function and a digital-to-analog-conversion function. As such, various implementation options are categorized as Mixing-DAC. Examples of architectures, which are classified as Mixing-DACs, are: a high speed Nyquist DAC with integrated mixing in the digital domain or a low speed Nyquist DAC with integrated analog mixer.

For the aforementioned wide-band transmitter with high spectral purity, a Mixing-DAC with wide-band high spectral purity is required.

1.1 Aims and scope

The research question of this work is:

Can a Mixing-DAC be used to generate wide-band signals with high spectral purity, what are the dominant spectral-purity limitations and what can be achieved with current process technologies?

The overall aim of this work is to explore the possibilities of using a Mixing-DAC in a wide-band transmitter with high spectral purity. The first subgoal is to analyze the limitations and strong points of Mixing-DACs. The second subgoal is to design a chip implementation of a Mixing-DAC with high spectral purity, to validate the analysis and explore what is the maximum achievable linearity and spectral purity for Mixing-DACs, in view of the constraints of the given technology. This research is not aimed at designing a Mixing-DAC for a specific wireless standard. Instead, the intention is to find fundamental and practical limitations on spectral purity.

The scope of this work is on the Mixing-DAC function within a transmitter. Other transmitter blocks, e.g. filters or power amplifier, are not considered. Also other concerns, such as the interfacing to the digital domain with different sampling rates, the removal of signal images, or the power control of the output signal are not considered. The focus is on the spectral purity of a Mixing-DAC. Other characteristics of the Mixing-DAC are of minor importance, e.g. power consumption or cost. The scope is limited to multi-GHz Mixing-DACs up to 4GHz, as discussed in Chapter 2. As implementing process technology, only 65nm CMOS is considered. However, the conclusions of this work can easily be extended to other process technologies.

1.2 Scientific approach

The approach followed in this work is to first systematically explore the limitations of Mixing-DACs, then synthesize the most optimal solution and finally validate the approach by measurement of a test chip. Therefore, the following steps are taken:

- analyze the state-of-the-art architectures;
- classify all aspects of a Mixing-DAC architecture;
- systematically analyze the impact of all architectural aspects on the wide-band spectral purity;
- synthesize the concept of the most optimal architecture by combining the most optimal choices for each architectural aspect;

- design and measure a proof of concept to validate the effectiveness of the classification.

This project was supported by the high-speed data converter group of IDT. This industry partner provided IP blocks of a baseline DAC [3]. These IP blocks, which provide functions that are not in the core of this research but have supportive functions, are used for the design of the chip implementation. Some blocks are used as-is, others are modified to match the Mixing-DAC function.

1.3 Thesis outline

The outline of this work is given in Table 1.1.

Table 1.1: Thesis outline

Chapter	**Purpose**
Chapter 2	To establish a common background and framework for the research discussed in this thesis, the technical background of the research, together with an analysis of the state-of-the-art Mixing-DACs is discussed.
Chapter 3	To facilitate a structured synthesis of an optimal architecture, a classification of various aspects of the Mixing-DAC architecture and analysis of their impact on the spectral purity is discussed in this chapter.
Chapter 4	To show that the classification leads to three promising architectures, that need further investigation.
Chapter 5 to 9	To analyze the process-technology dependent aspects of the trade-off between the three promising architectures.
Chapter 10	To summarize the conclusions of the previous chapters regarding the process-technology dependent aspects, and to conclude which architecture is the most optimal.
Chapter 11 and 12	To validate the conclusions of the classification, an implementation of the most optimal architecture is designed and measured.
Chapter 13 and 14	To answer the research question, general conclusions are drawn and recommendations for further research are proposed.

1.4 Original contributions

The original contributions of this work are:

- the classification of Mixing-DAC architectures based on architectural aspects;
- the analysis of the impact of architectural aspects on spectral purity;
- architectures that are synthesized based on the classification, especially the architecture which is implemented as a test chip;
- a new DAC segmentation trade-off which includes dynamic characteristics;
- analysis of the impact of an output transformer on the Mixing-DAC performance with the focus on linearity;
- a novel calibration method to improve the static linearity of (Mixing-)DACs;
- validation of the theory using a chip implementation ;
- a measured design with an IMD of <-82dBc and an $SFDR_{RB}$ of >75dBc up to 1.9GHz, which is more than respectively 10dB and 5dB better than all known state-of-the-art publications.

2 | Background

The technical background of the research is described in this chapter. The main differences between a transmitter with Mixing-DAC and a traditional transmitter with separate DAC and Mixer are discussed. Typical spectra of these two types of transmitters are shown and explained. The exemplary application, multicarrier GSM, is discussed along with the importance of a high spectral purity. The current-steering principle is chosen for implementing a Mixing-DAC with high spectral purity. The most important non-linearity figure is shown to be the IMD. Various performance metrics are discussed in this chapter, which are used to quantify the performance of the Mixing-DAC in the remaining part of the thesis. The state-of-the-art Mixing-DACs are discussed and their performance analyzed.

2.1 Introduction

Transmitters are important parts of the wireless systems. The performance of transmitters depends on the application. Especially for multicarrier transmitters in basestations, the required spectral purity is high.

The traditional transmitter and the Mixing-DAC transmitter are discussed in Section 2.2 and Section 2.3 respectively. The specifications of a target application are discussed in Section 2.4. Section 2.5 proposes a Mixing-DAC definition and applies the current steering approach to Mixing-DACs. Performance figures of the Mixing-DAC are discussed in Section 2.6. Section 2.7 gives an overview of the performance of state-of-the-art Mixing-DAC publications.

2.2 Traditional transmitter

A popular transmitter architecture is the zero/low-IF transmitter. Like most transmitters, the zero-/low IF transmitter exhibits a separation between

low-frequency baseband functions, i.e. the Digital to Analog Converter (DAC), and the high-frequency RF functions, i.e. mixer and Power Amplifier (PA). A functional overview of such a transmitter is shown in Figure 2.1. This particular example is based on I/Q signaling. Alternatives for I/Q signaling are discussed in Section 3.3.2.

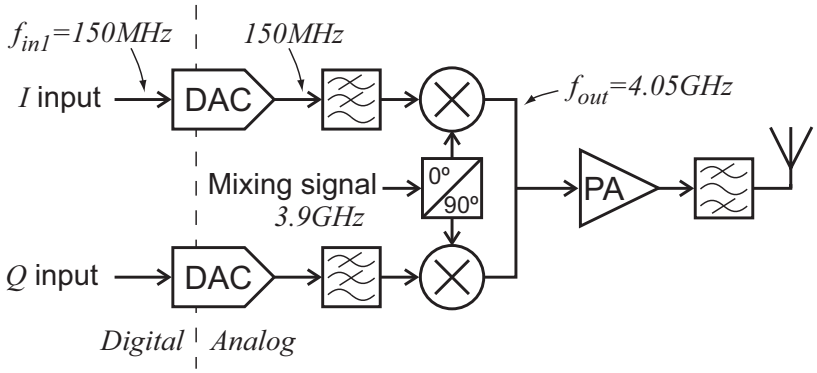


Figure 2.1: Signal chain of a traditional I/Q transmitter, with exemplary signal frequency values

The transmitter elements are meant to be linear. Due to non-idealities in the transmitter elements, the transfer function of the transmitter is non-linear which introduces harmonic distortion and reduces the spectral purity of the transmitter. The most non-linear elements in a typical transmitter implementation are the PA and the mixer. Using non-CMOS implementation technologies, e.g. GaAs, usually results in a higher linearity than standard CMOS technology but also increases cost. The amplitude of the non-linear distortion in the mixer and PA depends on the output power. Therefore, using output power back-off also improves linearity, but degrades the efficiency.

Another method for improving the linearity is Digital PreDistortion (DPD). The DPD adds a signal (counter-distortion) to the digital input signal, which cancels the spurious components generated by the transmitter non-linearity[4]. The characteristics of the additional counter-distortion can be determined a-priori or using a feedback loop during operation. A-priori characterization requires either a very elaborate characterization for various signal conditions (e.g. signal power, signal frequency) and environment conditions (e.g. temperature, supply voltage), and can also be limited in the usability (e.g. limited bandwidth, sensitive to aging). Using a feedback loop for characterization during normal operation requires a linear feedback path and an algorithm to calculate the required DPD compensation. The implementation of DPD results in a higher power consumption and increases

the number of transmitter components, which increases cost. DPD also introduces additional signal delay.

2.3 Mixing-DAC transmitter

Thanks to the continuous reduction of CMOS transistor size, integration density increases and errors due to parasitic capacitance and coupling become smaller, which can result in higher linearity. This enables the integration of the mixing and DAC function at high speed and high linearity at reasonable cost, and recently resulted in the introduction of the Mixing-DAC [5]. A transmitter signal chain with this novel Mixing-DAC is shown in Figure 2.2. A Mixing-DAC functionally features two signal inputs: the baseband (BB)

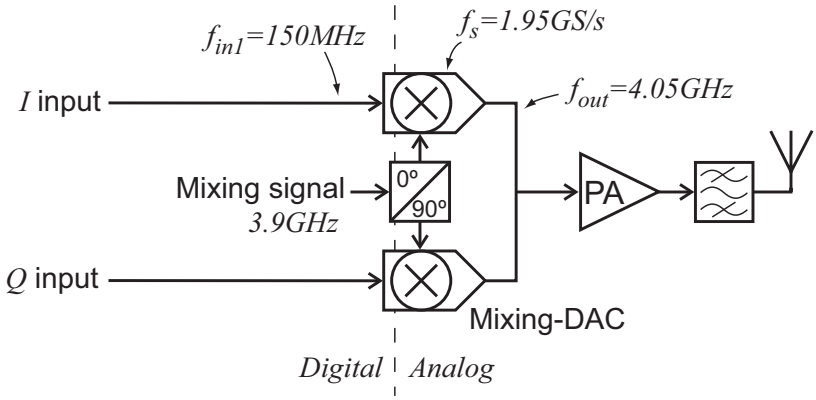


Figure 2.2: Signal chain of I/Q transmitter with Mixing-DAC, with exemplary signal frequency values

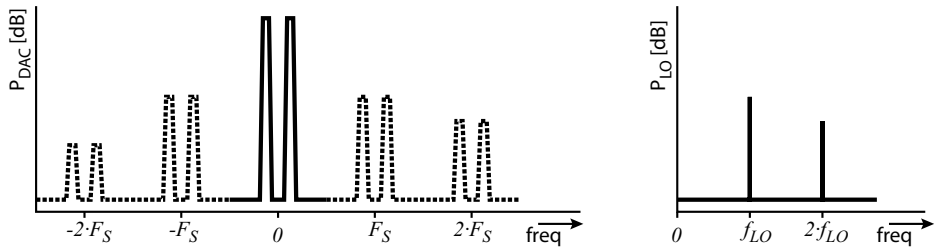
data input (i.e. '*I* input' and '*Q* input' in Figure 2.2), which contains the sampled low frequency information signal; and a mixing signal, alternatively called Local Oscillator (LO) signal.

As a single unit, the Mixing-DAC features much more architectural choices, compared to just combining a DAC and a mixer. Potential advantages of these new architectural choices include: lower power consumption, higher linearity, higher signal frequency and lower noise power[6]. Moreover, by combining the DAC and mixer in one package, the number of components of a transmitter is reduced, which reduces the total footprint and reduces cost.

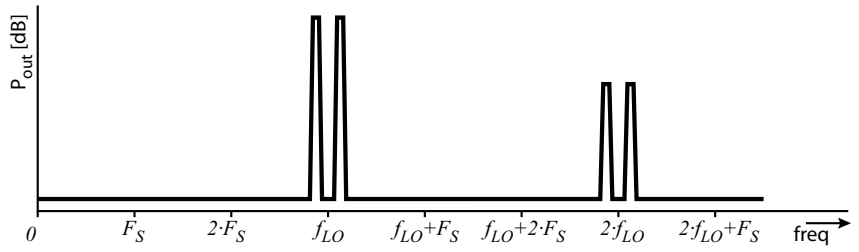
One of the most obvious differences between the traditional transmitter and the Mixing-DAC transmitter, is the absence of a reconstruction filter between the DAC and mixer function in the latter. This poses additional requirements on the RF output filter, which now also has to filter out the signal

images in the higher Nyquist bands. Figure 2.3 graphically shows the output spectrum difference between a separate DAC and mixer with and without reconstruction filter for the given input spectra. The former case represents the signal at the output of the mixer in a traditional transmitter while the latter case represents the output signal of a Mixing-DAC in the novel Mixing-DAC transmitter.

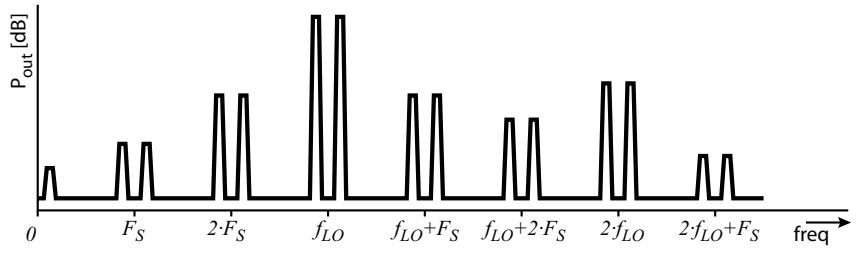
Another disadvantage of the absence of a reconstruction filter is that the Mixing-DAC sampling rate and the mixing frequency cannot be chosen freely, but must be interdependent. This relationship is further discussed in Section 3.4.2.3. In the traditional transmitter with reconstruction filter, the



(a) Spectra of input signals: DAC digital input (P_{DAC}) and *LO* input (P_{LO})



(b) Spectrum of mixer output signal with reconstruction filter



(c) Spectrum of mixer output signal without reconstruction filter

Figure 2.3: Spectral content of the transmitter signals: DAC digital input and *LO* input (a), mixer output signal with reconstruction filter (b) and without reconstruction filter with $f_{LO} = 3 \cdot F_S$ (c)

mixing frequency is independent of the DAC sampling rate.

Although the Mixing-DAC changes the filtering requirements, it is expected to offer architectural choices which enable high linearity at high frequency. An application which can profit from these advantages is discussed in the next section.

2.4 Multicarrier GSM

Different communication standards have different requirements on the linearity and bandwidth of the transmitter. GSM is the most demanding communication standard with respect to linearity. Advantages of using a Mixing-DAC for GSM transmitters are similar to the general advantages of Mixing-DAC transmitters: lower power consumption, higher linearity, higher signal frequency and lower noise power (see Section 2.3).

The spectral purity of the GSM-transmitter output signal is defined by a spectral mask in the GSM standard[2]. An exemplary mask is shown in Figure 2.4. Since the lowest level of the spectral mask is 80dB below the signal power, the required spectral purity of a GSM transmitter is: $SFDR_{RB}$>80dBc (Spurious Free Dynamic Range in a Reduced Bandwidth, see Section 2.6.2). To account for the non-linear distortion of elements further in the signal chain, e.g. the PA, ideally the $SFDR_{RB}$ should be above 85dBc, typically in a RB of 300MHz.

A single carrier transmitter can achieve these specifications by tight filtering. For multicarrier transmitters, filtering is not applicable since multiple carriers are present in the output signal, which would be attenuated if one carrier is filtered with a tight bandpass filter. Specific filtering is also not practical since it would need to be adjusted for each specific frequency configuration. For multicarrier transmitters, wide-band noise, intermodulation of various carriers and other spurious components can cause violations of the spectral mask. Therefore, the satisfaction of the spectral mask is much more challenging for multicarrier transmitters.

As intermodulation of the carriers should not produce violations of the spectral mask, the required IMD (InterModulation Distortion, see Section 2.6.2) is between -80dBc and -85dBc, while accounting for the other transmitter elements. The required NSD (Noise Spectral Density, see Section 2.6.2) can be calculated from the lowest mask level of -80dBc in a measurement bandwidth of 100kHz, see Figure 2.4. The reference power of the spectral mask (0dB in Figure 2.4) is measured in a 30kHz bandwidth while the total power of one GSM carrier is spread over its signal bandwidth of approximately 200kHz. Therefore, the reference power is approximately

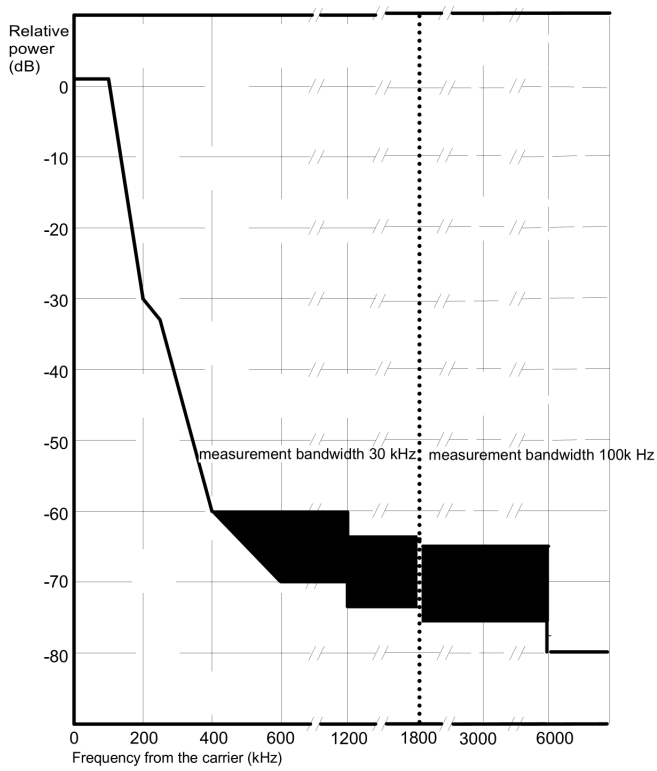


Figure 2.4: An examplary GSM mask [2]

6dB lower than the total power of the GSM carrier. The required NSD is: NSD=-6-80-10$\cdot \log_{10}$(100kHz)=-136dBc/Hz. Since most multicarrier GSM transmitter operate in a back-off of typically -16dB$_{\mathrm{FS}}$ and to account for other spurious components and other transmitter elements with 10dB margin, the required NSD of the Mixing-DAC is NSD=-162dB$_{\mathrm{FS}}$/Hz.

Some relaxing terms are present in the GSM specifications for multicarrier basestation transmitters. Examples are: higher spurious components are allowed in a limited number of bands, exceptions are specified for intermodulation components, and wide-band noise specifications are relaxed for the transmit band. However, it is beyond the scope of this work to evaluate all these exceptions. Therefore, the specifications of single carrier GSM are used, which is the most stringent reference point.

For multicarrier GSM transmitters in basestations, the required bandwidth is large with respect to one carrier. This downstream bandwidth (i.e. from the basestation to a mobile device) of a GSM basestation can be as high as 75 MHz (i.e. for DCS1800 [2]). The use of predistortion for the

mixer and the PA increases the bandwidth of the Mixing-DAC output signal even more. Therefore, the bandwidth in which the high linearity should be achieved (reduced bandwidth (RB)) is chosen to be 300MHz. The linearity and bandwidth target are visualized in Figure 2.5. This figure clearly shows the high required linearity and bandwidth of multicarrier GSM transmitters.

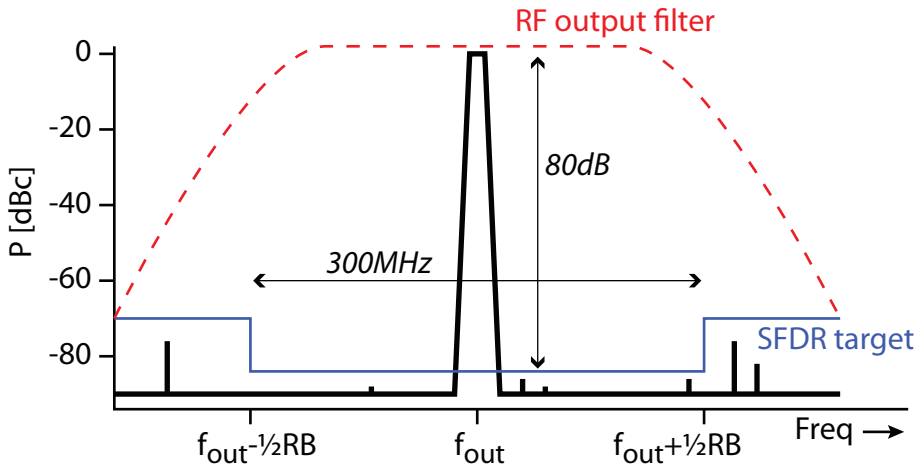


Figure 2.5: Exemplary target performance figures of Mixing-DAC output spectrum for this work

Current GSM standards are defined between 450MHz and 1990MHz[2]. To account for future GSM definitions at higher frequencies, and other communication standards, in this work the target output frequency range is between 0.4GHz and 4GHz.

2.5 (Current steering) Mixing-DAC

Since the Nyquist DAC architectures are closely related to Mixing-DACs, Nyquist DAC principles are investigated as a starting point for the research. All state-of-the-art high speed DACs are implemented using the current-steering (CS) approach. A CS (Mixing-)DAC is based on an array of current sources, which are switched on and off depending on the digital input data. An overview of the CS DAC principle is shown in Figure 2.6.

The popularity of the CS approach is mainly because of how a CS DAC produces the output power. CS DACs generate a continuous current that creates signal power in a simple resistive load. This signal power is continuously available to drive the load and output capacitance. Hence, there is no necessity for an output buffer which can limit the performance.

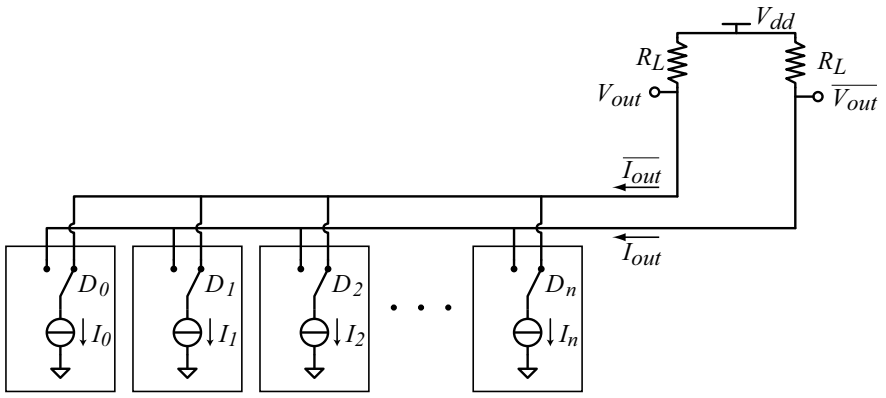


Figure 2.6: Principle of a current steering DAC

A CS DAC can achieve high accuracy thanks to the well-known matching of current sources. Well-matched current sources require a large area, which result in large parasitic capacitances, limiting the sampling rate. However, in a CS DAC, these large current sources only generate a DC current and don't need to be switched at high speed. Furthermore, the large current sources can be decoupled from the fast switching action by cascodes. This is not possible if switched resistors or capacitances are used as reference components.

2.6 Performance figures

The performance of a Mixing-DAC is evaluated using the spectral purity of the output spectrum. A distinction between the desired and undesired components of the output spectrum is discussed in the next section. Thereafter, performance metrics are defined and discussed.

2.6.1 Spectral contents

An exemplary signal spectrum at the output of the Mixing-DAC is shown in Figure 2.7. Ideally, the target output spectrum only contains signal power at the intended output frequency (signal inside the dashed box in Figure 2.7):

$$f_{out} = f_{LO} + f_{in}, \tag{2.1}$$

where f_{out}, f_{LO} and f_{in} correspond to the output, LO and input signal frequencies. However, due to the sampling nature of a DAC and harmonic components in the mixing signal, the output spectrum also contains signal energy at (see Figure 2.7):

$$f_{out} = M \cdot f_{LO} + K \cdot F_S \pm f_{in}, \tag{2.2}$$

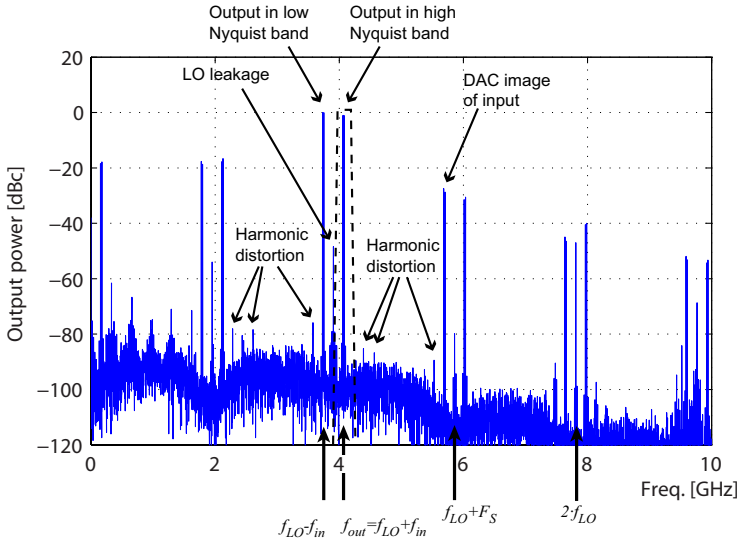


Figure 2.7: Exemplary simulated Mixing-DAC output spectrum ($f_{LO} = 2 \cdot F_S$)

where M, $K \in \mathbb{Z}$, and F_S is the sampling rate of the D/A conversion. The power of these images depends on a number of variables, such as the shape of the mixing waveform (e.g. sine or square, see Section 3.4.1.1) and the shape of the Mixing-DAC impulse response.

In practice, Mixing-DAC implementations suffer from non-linear distortion. For an input signal consisting of two tones at f_{in1} and f_{in2}, the output spectrum also contains undesired harmonic distortion components:

$$f_{out} = M \cdot f_{LO} + K \cdot F_S + N_1 \cdot f_{in1} + N_2 \cdot f_{in2}, \tag{2.3}$$

where N_1, $N_2 \in \mathbb{Z}$. This harmonic distortion depends on for instance the sequence (i.e. order) of Mixing and DAC operation (see Section 3.5.2) or the mixing locality (see Section 3.4.2.1).

The energy at $M = 1$, $K = 0$, and $N_1 = 1$ or $N_2 = 1$ is desired. For high spectral purity, the other components should be minimized. A bandpass filter (dashed line in Figure 2.7) can filter undesired output signals far from the desired output signal frequency. However, Intermodulation Distortion (IMD, see Section 2.6.2) is close to the desired output signal, which can be seen in a zoom-in around the output frequency of the output spectrum in Figure 2.8, where the dashed filter characteristic cannot filter the IMD tones. Therefore, IMD is the most critical type of non-linear distortion.

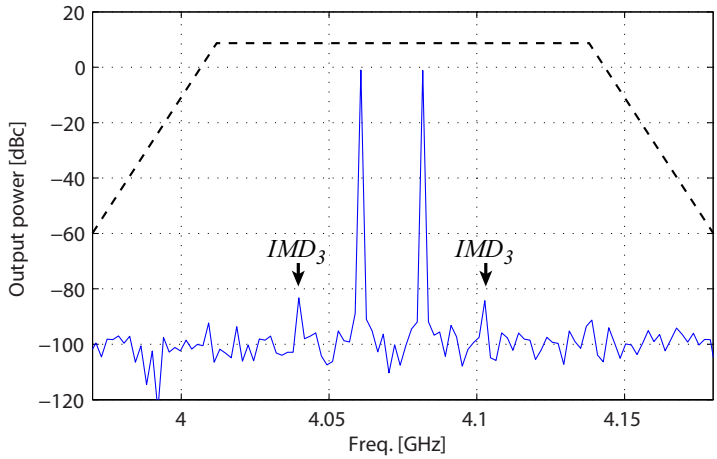


Figure 2.8: Zoom-in of simulated exemplary Mixing-DAC output spectrum ($f_{LO} = 2 \cdot F_S$)

2.6.2 Definitions of performance metrics

This section discusses the performance metrics which are used in this work to quantify the performance of the Mixing-DAC.

2.6.2.1 Static specifications

Power consumption [mW]: sum of the power consumed from all static power sources. Hence, dynamic sources such as the LO or clock input are not taken into account in the power consumption figure. The power consumption depends among others on the sample rate and the input signal.

Integral NonLinearity (INL) & Differential NonLinearity (DNL) [LSB]: INL is the difference between the Mixing-DAC transfer characteristic and the expected straight line, and DNL is the error in a DAC code transition, see [7]. A good INL is crucial for achieving a high linearity. In this work, the static linearity is not limiting the performance at high frequencies. The measurement of INL is not trivial when using the used output configuration, which is tailored for the measurement of the RF characteristics, see Section 12.2.2. However, the order of magnitude of the INL can be estimated from the low frequency harmonic distortion.

2.6.2.2 Dynamic specifications with sinusoidal signal

Output power [dBm]: The output power is measured per tone, unless indicated otherwise. For example, for a dual-tone signal, the output power

per tone is 6dB lower than a single tone with the same amplitude.

Spurious Free Dynamic Range (SFDR) [dBc]: The ratio between the power of the desired signal and the power of the highest tone of the undesired spurious components (spurs). For an input signal with multiple tones, the power of the tone with the highest power is used as the signal power. In this work, the input signal is a full-scale[1] single tone signal, unless otherwise specified. The bandwidth in which the spurs are measured, is one Nyquist band. Hence, LO leakage and signal images are not taken into account.

SFDR in a Reduced BandWidth ($SFDR_{RB}$) [dBc]: SFDR measurement within a predefined frequency band (the reduced bandwidth RB), which is smaller than the Nyquist band. In this work, the position of the RB in the frequency domain is relative to the output signal. The RB is from f_{out}−RB/2 to f_{out}+RB/2. When the input frequency f_{in} is low, the LO frequency falls in the RB ($|f_{out}-f_{LO}|$<RB/2). In that case the SFDR_{RB} could be equal to the LO leakage, since that spur is mostly higher than all other spurs around the output signal in this work. Therefore, for low input frequency values, the RB is chosen such that the LO leakage does not fall in the RB: the RB is then from f_{LO} to f_{LO}+RB for the high Nyquist band and from f_{LO} to f_{LO}-RB for the low Nyquist band.

InterModulation Distortion (IMD) [dBc]: The ratio between the power of the IMD tone and the desired output signal power per tone. The two signal tones have equal power per tone. The power of both signal tones is equal. Theoretically, for a two-tone output signal with frequencies f_1 and f_2, the IMD spectral components are situated at $n_1 \cdot f_1 + n_2 \cdot f_2$, with $n_1, n_2 \in \mathbb{Z}$. In a Mixing-DAC, IMD is generated in two different frequency domains: the baseband domain and the RF domain. If the IMD is generated in the baseband part of the Mixing-DAC, these spurs are generated due to the frequencies f_{in1} and f_{in2}, and then mixed with f_{LO}. Hence, baseband IMD is present in the output spectrum at $f_{LO}+(n_1 \cdot f_{in1}+n_2 \cdot f_{in2})$. If the IMD is generated in the RF domain, the IMD is generated due to $f_{out1}=f_{LO}\pm f_{in1}$ and $f_{out2}=f_{LO}\pm f_{in2}$, and hence occurs at $n_1 \cdot f_{out1}+n_2 \cdot f_{out2}$. Since spurs close to the output signal are the most important spurs, in this work only the IMD components close to the output signal are considered when discussing IMD, hence the odd orders which satisfy: $|n_1 + n_2| = 1$. The order of the IMD component is defined as $|n_1| + |n_2|$. For example, the two IMD3 components are shown in Figure 2.8. In this work, the IMD3 value is calculated using the highest of the two IMD3 tones. When a IMD value is given without reference to the order of the IMD tone, the highest tone of all odd IMD orders is used.

[1] In measurements, limitations in the software used for generating the digital input signal, forces the maximum input amplitude to be -0.1dB_{FS}

Harmonic distortion (HD) [dBc]: The harmonic distortion components, which are measured using a single-tone output signal, are situated at frequency multiples of the fundamental frequency. For a given frequency f_{ex}, the HD components are at $(n+1) \cdot f_{ex}$, with $n \in \mathbb{N}$. For Mixing-DAC harmonics that are generated in the baseband domain, the HD frequencies are $f_{LO}+(n+1)\cdot f_{in}$. When a HD component falls outside the Nyquist band, the power of the folded back component is used as the corresponding HD value. HD components which are generated in the RF domain, are situated at $(n+1)\cdot f_{out}$. The frequency of the HD components in the RF domain is far from the fundamental output frequency, and hence only the HD components from the baseband domain are taken into account.

LO leakage [dBm]: Power in the output signal at the frequency of the LO signal. The absolute power is used for the LO leakage, since it is shown to be independent of the output signal power.

Image leakage [dBc]: The output of a single Mixing-DAC contains two input signal components, one at $f_{LO}+f_{in}$ and one at f_{LO}-f_{in}. When using I/Q signaling and two LO signals with 90° phase difference, one of those two images can be canceled in the combined output. However, this suppression is never perfect. The amplitude of the undesired suppressed signal image with respect to the desired output component is the image leakage.

Phase noise [dBc/Hz]: Phase noise is uncertainty in the phase of the output signal. Phase noise can distort narrowband output signals. A phase noise measurement uses a single tone output signal. The phase noise is measured in the frequency domain at various frequency distances from the output tone.

Noise Spectral Density (NSD) [dB_{FS}/Hz]: Wide-band noise can also cause violations of the spectral mask of the target application. A wide-band noise measurement uses a small input signal to prevent harmonic distortion which can obscure the noise measurement. The NSD is measured in the frequency domain and as far from the carrier as necessary to not measure the phase noise.

Efficiency [%]: The efficiency is the output power divided by the total power consumption. The output power is measured using a sinusoidal single tone input signal with full scale amplitude.

2.6.2.3 Dynamic specifications with modulated signal

Error vector magnitude (EVM) [dB]: Error in the accuracy of the modulated signal. For high linearity Mixing-DACs, the EVM is usually orders of magnitude smaller than specified by the standard. Measurement of the EVM requires specialized hardware to demodulate of the signal. Therefore,

it is not taken into account in this work.

Spectral mask: The GSM application defines a spectral mask, which is the maximum power of the output signal at each frequency, see Figure 2.4. This spectral mask is drawn over the spectrum of the output signal to reveal any violation.

Adjacent Channel Leakage Ratio (ACLR) [dBc]: The ACLR is defined for wireless standards which have predefined signal bands, which are adjacent. The ACLR is the ratio between the signal power in the desired signal band and the power in the adjacent channel with the highest power. The signal power is integrated over the complete signal band. The ACLR is a measure of the linearity and noise performance of the Mixing-DAC. In this work, the ACLR figures of WCDMA and LTE signals are measured.

2.7 State of the art Mixing-DAC performance

The first appearance of an RFDAC or Mixing-DAC at RF frequency [5] uses the traditional CS DAC topology, where the current-source transistor

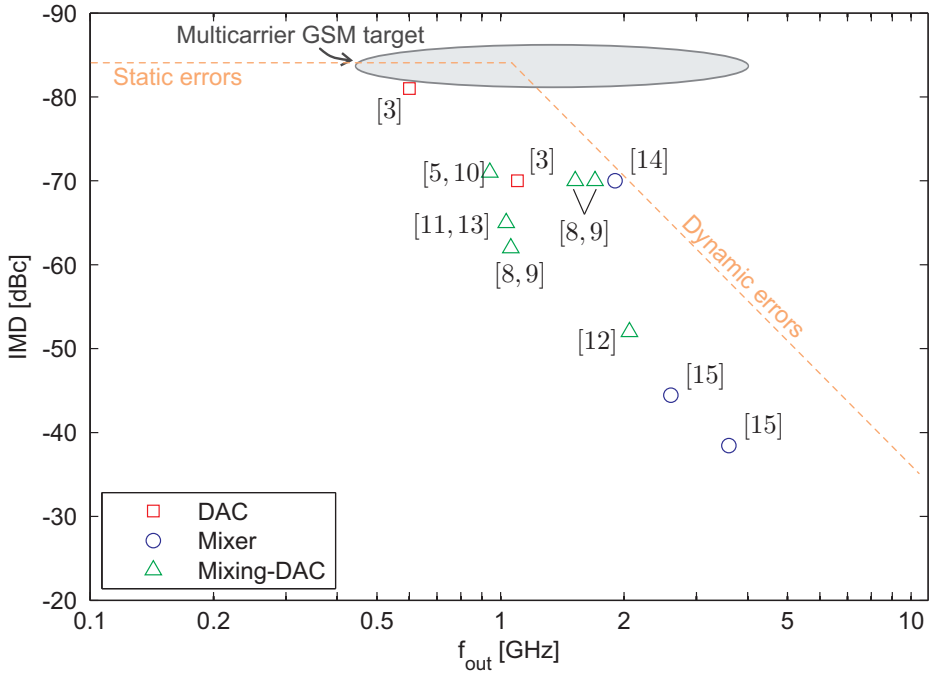


Figure 2.9: Overview of the IMD of state-of-the-art Mixing-DAC publications, DACs and mixers (at $1V_{pp}$ output signal amplitude)

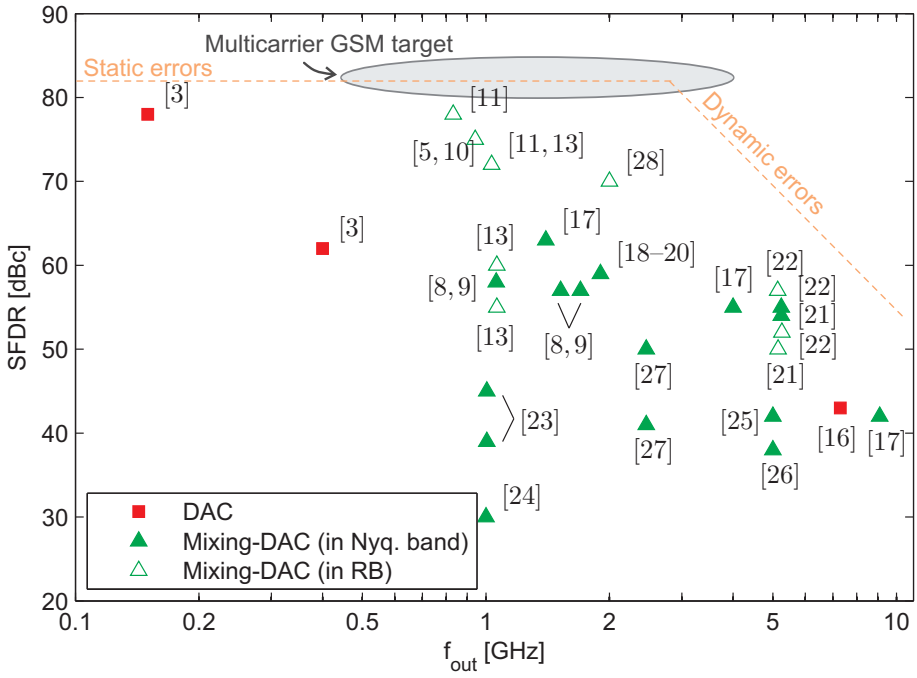


Figure 2.10: Overview of the SFDR of state-of-the-art Mixing-DAC publications and DACs

acts as the amplitude reference and as a mixer. Other publications use the same architecture [10, 11, 13]. However, there is a trend toward topologies based on a (fully balanced) Gilbert-cell mixer [8, 9, 12, 17–23, 25–27, 29–32]. Compared to a CS DAC output stage, these topologies have an additional layer of transistors which implement the mixing function. This strategy can enable separate optimization of the three functions in the Mixing-DAC output stage (i.e. reference generation, data switching, and mixing). The additional layer of transistors sacrifices voltage headroom which otherwise could have been used for cascoding the current source or the entire output stage. Therefore, only few publications combine Gilbert-cell mixing with an output cascode [21, 22, 33] and none combine it with a current source cascode.

Topologies focusing on high efficiency and high output power use a minimal stack of just one or two transistors [28, 34–37]. This low number of stacked transistors requires a low operating voltage and enables a large output voltage swing and hence can result in a high energy efficiency.

To achieve a high frequency, some publications use a low resolution, which results in a small area and hence achieves high frequency [10–13, 21–23, 29, 30]. In these low resolution Mixing-DACs, the quantization noise is shaped

using ΔΣ-modulation. However, ΔΣ-modulation results in high noise power at frequencies farther away from the output frequency (out-of-band) and hence limit the bandwidth. Some solutions use a bandpass filter to remove the high out-of-band noise [21, 22].

For a high performance Mixing-DAC, both the static and dynamic errors should be sufficiently low. Most publications are unable to sufficiently isolate those two types of errors. They achieve either high performance at low frequency or low performance at high frequency. This can be seen in the overview of the IMD and SFDR performance of relevant DACs, mixers and Mixing-DACs, which is given in Figure 2.9 and Figure 2.10 respectively. For mixers, the 3^{rd} order interception point at $1V_{pp}$ output voltage is chosen as a measure of the linearity.

These figures clearly show that the intrinsic linearity of both the Mixing-DAC and the traditional DAC and mixer combination is not sufficient for the exemplary application. Above f_{out}=600MHz, the IMD values are worse than necessary for the multicarrier GSM target. Mixing-DAC SFDR values close to the target are only achieved in a narrow reduced bandwidth, e.g. [5, 13], using expensive non-CMOS technologies, e.g. GaAs [8], or at low output power, e.g. [22].

Using an architecture which isolates the static errors from the dynamic errors, enables separate optimization and can offer high performance at high frequency.

2.8 Conclusion

A Mixing-DAC can be used to replace the DAC and Mixer of a traditional transmitter. Using a Mixing-DAC instead of a separate DAC and mixer reduces the number of components in a transmitter, which can decrease the cost and increase robustness. Novel architectures of Mixing-DACs can offer higher linearity and higher signal to noise ratio and lower power consumption.

The current-steering principle is the main approach for the implementation. The exemplary application, i.e. multicarrier GSM, requires a high linearity and large bandwidth, which cannot be achieved by state-of-the-art Mixing-DACs. The most important non-linear distortion component is the IMD because it cannot be filtered out.

3 Architecture classification and synthesis

To achieve high spectral purity, a novel architecture is needed. However, there are numerous possible architectures. This chapter proposes a classification of Mixing-DAC architectures. Each architecture is characterized based on its architectural aspects. This chapter proposes a set of thirteen architectural aspects and subdivides them into three different groups: system level, signals level and implementation level.

The structured synthesis of an architecture consists of a set of choices for all architectural aspects. The optimal choices for all architectural aspects lead to three proposed candidate architectures.

This chapter is based on a paper submitted to the Springer journal Analog Integrated Circuits and Signal Processing [82].

3.1 Introduction

The design space of Mixing-DACs is highly complex. Numerous interdependent architectural choices exist. In open literature, a high number of exemplary Mixing-DAC implementations can be found, as illustrated in Section 2.7. However, the choice for a given architecture is not well substantiated, since a comparison between Mixing-DAC architectures is not available.

To achieve high spectral purity, a novel architecture needs to be synthesized. Only a structured synthesis lead to the most optimal architecture. Therefore, this chapter proposes a classification to clarify and structure the impact of high level architectural choices on the Mixing-DAC performance. The scope of this comparison is high spectral purity. The

classification incorporates the Mixing-DAC definition of Section 2.5. The focus is on architectural choices which are specific for Mixing-DACs and are differentiating between various architectures. Subjects like Data drivers, LO driver, segmentation or RF packaging are not discussed since these are not differentiating between the various architectures. Using the classification, a candidate Mixing-DAC architecture is proposed, which is expected to provide sufficient intrinsic performance for multicarrier GSM.

The classification of Mixing-DAC architectures is proposed in Section 3.2. Three levels of abstraction are discussed: system level, signal level and implementation level in Section 3.3, Section 3.4 and Section 3.5 respectively.

3.2 Mixing-DAC architecture classification

For high spectral purity at high output frequency, the Current Steering (CS) principle is almost solely used. The reasons for that are explained in Section 2.5 and Section 3.3.1. In this classification, the class of CS Mixing-DACs is mainly considered. In CS (Mixing-)DACs, the output wide-band noise power is predominantly caused by the thermal noise of the current sources. Therefore, it is not differentiating between architectures and is not discussed into detail. Simulations of exemplary circuits are done using an implementation in 1.2V/3.3V 65nm CMOS. For the simulations, each Mixing-DAC output stage (array of parallel current cells which generate the output signal, e.g. Figure 3.4 or Figure 3.8) are modeled at transistor level, unless stated otherwise. To focus on the differences between various output-stage architectures, the common signals (e.g. the *LO* and *Data* signal, and the biasing signals) are assumed to be ideal. Realistic signal levels and transition times assure realistic simulation results and an accurate comparison between architectures.

An overview of the proposed classification is shown in Figure 3.1. The three levels of abstraction in the classification are discussed separately in the next three sections.

3.3 System level classification

The three system level classes are: Power class, data representation and smart methods.

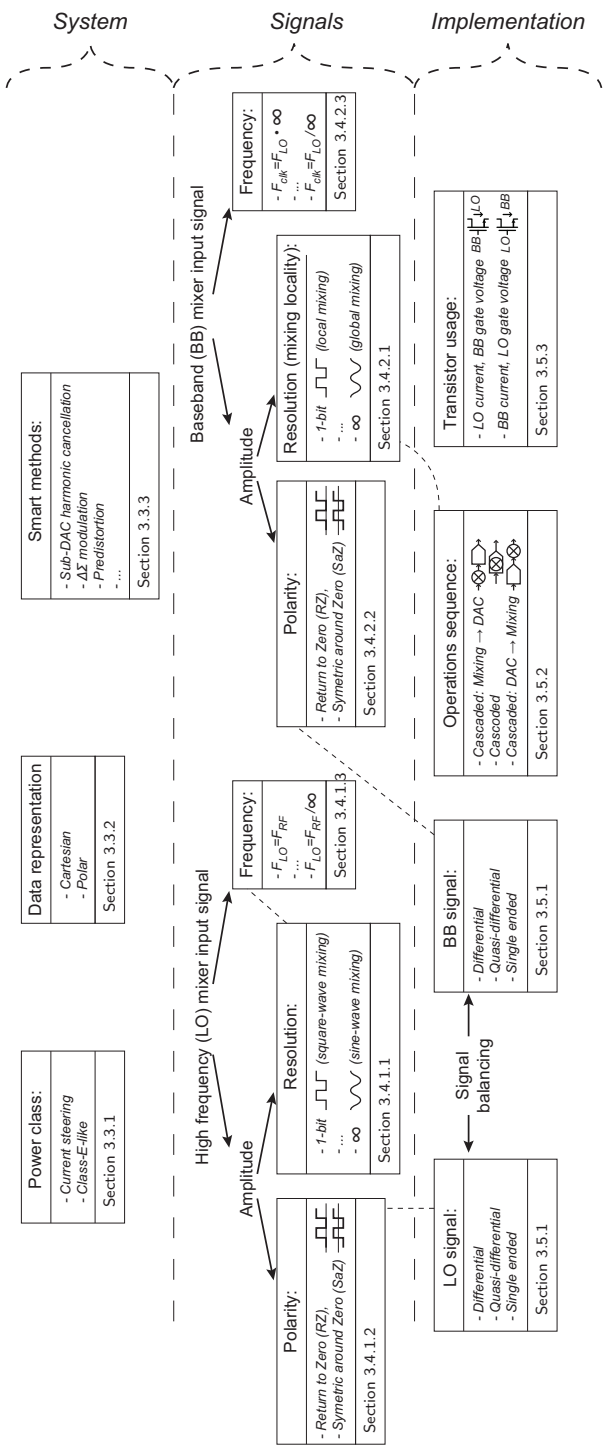


Figure 3.1: Overview of the proposed classification of Mixing-DAC architectures

3.3.1 Power class

Two main principles are in use for generating the output power: current steering and class-E-like[28].

The current-steering approach is well known from high performance DACs, and offers high linearity and high sample rate at reasonable output frequency. For example, the DAC of [38] produces IMD3<-85dBc at 1.5GSps and 152MHz input frequency. However, the efficiency of a current-steering DAC is not very high, typically well below 1% [3, 38].

Class-E type Mixing-DACs are based on the class-E power amplifier (PA), which is a switching type PA and offers high output power and a high efficiency. The class-E Mixing-DAC basically consists of a number of class-E amplifiers in parallel, which are enabled depending on the digital input data. Just like class-E PAs, high output power and efficiency are achieved (e.g. 20% at 2GHz in [28]), compared to current-steering Mixing-DACs. Since this type of Mixing-DAC basically uses a transistor in the linear region as reference-resistor, the linearity of this Mixing-DAC principle is low compared to CS Mixing-DACs.

The current-steering principle is the best option for achieving the high linearity which is required for a Multicarrier-GSM transmitter. Hence, in the following parts of the classification, it is assumed that the current-steering principle is used.

3.3.2 Data representation

Most traditional transmitters use the Cartesian data representation and processing, i.e. I-Q signaling. Another option for the signal representation is polar signaling. In polar signaling, a signal is defined by its phase and amplitude(i.e. envelope). Examples of transmitters using polar signaling are the Kahn Envelope Elimination and Restoration (EER) [39] or Direct Digital RF (DDRF) polar transmitters [33, 35, 36]. The general advantages and disadvantages of Cartesian and polar Mixing-DACs are summarized in Table 3.1. The advantages and disadvantages of a complete polar transmitter are elaborately discussed in literature [41–43].

3.3.2.1 Efficiency

The efficiency of Cartesian and polar Mixing-DACs partly depends on the balancing of the signals, which is discussed in Section 3.5.1.

The main advantage of a transmitter based on a single-ended polar Mixing-DAC is the high power efficiency, especially at low output power. Since the phase is coded in the LO signal, the envelope signal will always have a positive

Table 3.1: Comparison between signal representations

Signal repres.	**Example**	**Characteristics**
Cartesian	Sine-wave RZ current source mixing [5,10,11, 13] Gilbert current cell mixing [8,9,18–20,30,31,40] and many others	**Advantages:** baseband signal does not need conversion, LO-clock phase can be optimized. **Disadvantages:** usually poor power efficiency at low signal level.
Polar	Kahn envelope elimination and restoration [39] Differential direct digital to RF [33,35] Single ended direct digital to RF [36]	**Advantages:** good power efficiency at low signal level. **Disadvantages:** signals need larger bandwidth; disables RZ masking of BB timing errors.

sign, and hence can directly control the number of enabled current sources in the Mixing-DAC output stage. At a low signal level, only few current sources are enabled, and hence the power efficiency can be high.

In a single-ended Cartesian Mixing-DAC, on average half of the current sources are always enabled, since even a signal with small amplitude resides around mid-scale. Quasi-differential signaling can improve the power efficiency of I/Q Mixing-DACs[28], see Section 3.5.1.

Since baseband signals are usually in Cartesian format, a polar transmitter may require a conversion step from Cartesian signaling to polar signaling, which results in a higher power consumption and higher delay.

3.3.2.2 Bandwidth

A disadvantage of polar transmitters is the required bandwidth of the envelope and phase signal, which is required to be much larger than the bandwidth of the corresponding Cartesian signals to satisfy EVM[42,43] and harmonic distortion requirements[41].

3.3.2.3 Synchronization

Another advantage of a polar Mixing-DAC is that only one Mixing-DAC core is required for single sideband transmission. For Cartesian transmitters,

two Mixing-DACs are required (for the I and Q path), or a steep filter is required to filter out the undesired image in the output spectrum. The shape of such a filter is shown as a dashed line in Figure 2.7.

In I/Q Mixing-DACs, the I and Q paths can be combined to remove one of the two signal images at the left or right of the LO frequency. The I and Q paths need to be matched in order to achieve good image rejection. This problem has been extensively investigated for traditional I/Q transmitters. Since both paths are of the same type, their behavior is intrinsically matched, and only random mismatch causes an unbalance in the two signal paths. To improve the matching, digital predistortion [44] can be used. Interesting I/Q combining techniques exist for Mixing-DACs[28].

In polar Mixing-DACs, the hybrid matching of the phase path and amplitude path poses a challenge[41]. These signals are different in type and processing hardware, and do not offer intrinsic matching, as in I/Q matching. Timing mismatch between the two paths worsens EVM, causes spectral mask violations [42, 43], and causes harmonic distortion [41].

For polar Mixing-DACs, the transitions in the LO signal and the amplitude signal are not aligned. Section 3.4.1.2 discusses that RZ signaling for the LO signal can be used to mask the timing errors in the transitions of the BB signal if these transitions are aligned with the 'zero' phase of the LO signal. Therefore, in polar Mixing-DACs the RZ signaling cannot be used to mask the timing errors, which can be a disadvantage.

Section 12.4.4 shows that the phase between the sample clock and the LO signal influences the harmonic distortion components. For I/Q transmitters, this phase can be chosen freely, and hence optimized for performance. For polar transmitters, this phase is dictated by the input data and cannot be chosen freely.

3.3.2.4 Conclusion

Because of the disadvantage of polar transmitters regarding the signal bandwidth, they are almost solely used for narrowband signals, e.g. single carrier GSM[42]. Polar transmitters are not suitable for the transmission of multicarrier GSM because of the high signal bandwidth combined with high spectral purity of the signal, especially in combination with predistortion, which is discussed in Section 2.2. However, polar transmitters are suitable for narrowband, high efficiency and low spectral purity transmitters. Cartesian transmitters can achieve large bandwidth and high linearity. Therefore, Cartesian signaling is the best option for the highly linear multicarrier GSM transmitter.

3.3.3 Smart methods

Smart methods can be used to improve the intrinsic performance of a CS Mixing-DAC architecture. Examples of smart methods are: amplitude calibration [45, 46][87], see also Chapter 8, timing error calibration [47][88], Sub-DAC harmonic cancellation[48], $\Sigma\Delta$ modulation[5, 11, 22], RF FIR filtering [11–13, 49] or predistortion [50]. More examples of smart methods are summarized in [7]. Although these smart methods can improve specific non-idealities, the correction mechanisms can introduce or worsen other non-idealities, e.g. increase the noise power, increase the power consumption or decrease the maximum output frequency.

This chapter is aimed at synthesizing a Mixing-DAC architecture with the highest intrinsic spectral purity. In general, smart methods can be applied with almost equal effect on every architecture. Hence, it is assumed that the Mixing-DAC architecture with the highest intrinsic performance also provides the highest spectral purity when smart methods are taken into account. However, smart methods will be mentioned when they influence the trade-off between architectural choices.

3.4 Signal level classification

The mixer function in the Mixing-DAC has two input signals. One input is the high frequency mixing signal (LO), usually only containing a discrete number of frequencies. The other is the low frequency input containing the baseband data (BB). These two signals are considered in the signal level of the classification.

3.4.1 High frequency signal (LO)

One of the inputs of the mixer function is the high frequency mixing signal. The characteristics of the LO mixing signal can be divided in two subsets: amplitude and frequency characteristics. The amplitude characteristics are subdivided into resolution and polarity characteristics.

3.4.1.1 Amplitude - resolution

Two common shapes of mixing waveforms are: sine-wave and square wave, which corresponds with ∞-bit and 1-bit resolution. A third option is quantized sine-wave mixing, which corresponds with n-bit resolution, where n depends on the number of quantization levels. Examples of the aforementioned options and a summary of the advantages and disadvantages are shown in Table 3.2.

Table 3.2: Classification of Mixing-DAC architectures based on the amplitude resolution of the LO signal

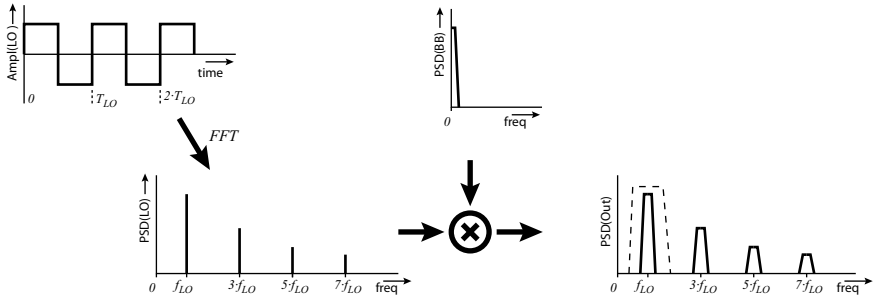
Shape	**Example**	**Characteristics**
Sine-wave	Sine-wave RZ current source mixing [5, 10, 11, 13] Gilbert current cell sine-wave mixing [21, 22, 51] Conventional two step conversion	**Advantages:** low control signal feedthrough, low data timing error sensitivity, no additional input signal images in output signal. **Disadvantages:** sensitive to mixing transistor non-linearity.
Quantized sine-wave	Quantized sine-wave two step conversion[52] Quantized sine-wave Mixing-DAC[53]	**Advantages:** controllable number of additional input signal images in output signal, low data timing error sensitivity, compatible with modern CMOS process technologies. **Disadvantages:** high chip area, limited output frequency.
Square-wave	Single-ended square-wave mixing [54–56] Semi-differential square-wave current source mixing [57] Direct conversion [48] Gilbert current cell mixing [8, 9, 18–20, 30, 31, 40] Combined output mixing [12, 58] Conventional two step conversion [59]	**Advantages:** very well compatible with modern CMOS process technologies, low sensitivity to mixing transistor linearity, high output signal energy. **Disadvantages:** additional number of input signal images in output signal.

Spurious components

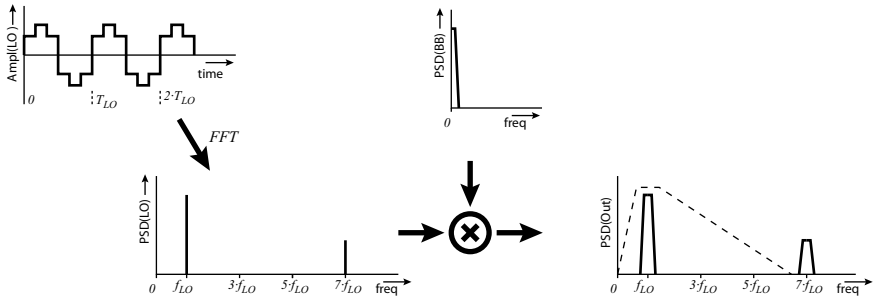
The amplitude behavior of the LO mixer input determines the repetition of the BB input spectrum in the RF output spectrum, i.e. $|M| > 1$ in (3.1) (see also (2.2)):

$$f_{out} = M \cdot f_{LO} + K \cdot F_S \pm f_{in}, \tag{3.1}$$

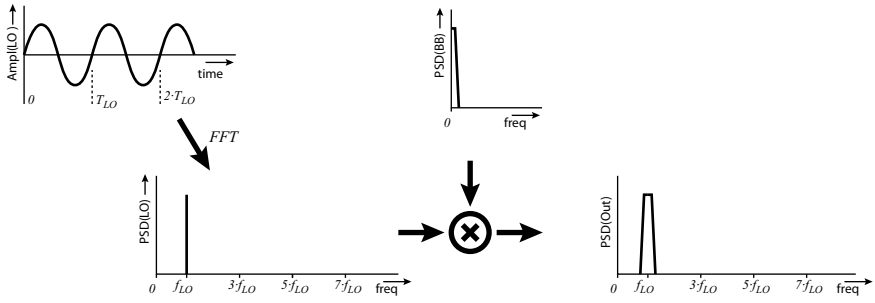
where f_{out}, f_{LO} and f_{in} are the output, LO and input signal frequencies respectively, and F_S is the D/A-conversion sampling rate, and M, $K \in \mathbb{Z}$. Figure 3.2 shows the difference between the output spectra of sine-wave mixing, quantized sine-wave mixing and square-wave mixing. When the resolution is 1-bit, the LO mixer input is a square-wave. A square wave with 50% duty cycle results in repetition of the BB input spectrum at each odd multiple of the fundamental LO frequency[30], i.e. $|M| \in \{1, 3, 5, ...\}$



(a) Square-wave mixing



(b) Quantized sine-wave mixing[52]



(c) Sine-wave mixing

Figure 3.2: Spectral consequence of sine-wave mixing, square-wave mixing and quantized sine-wave mixing[52]

in (3.1). An exemplary output spectrum of square-wave mixing is shown in Figure 3.2(a). The undesired spurious components at higher frequencies can be filtered out, which is illustrated by the dashed filter characteristic in Figure 3.2(a).

When the resolution of the LO input is infinite, the mixing signal can be a sine-wave, ideally resulting in just one repetition of the BB input spectrum in the RF output spectrum[21], i.e. $|M| \in \{1\}$ in (3.1). An exemplary output spectrum of sine-wave mixing is shown in Figure 3.2(c). Sine-wave mixing reduces the necessity of applying output filtering. However, repetitions of the BB spectrum are also present in the output spectrum due to the sampled nature of the BB input signal in combination with the zero-order-hold impulse response of the Mixing-DAC, corresponding to $|K| > 0$ in (3.1). Hence, choosing sine-wave mixing only reduces the spectral repetitions of the BB spectrum, but it does not completely remove them.

With quantized sine-wave mixing, the number of input spectrum repetitions in the output spectrum is controlled by the number of quantization levels: $|M| \in \{1, 7, 13, ...\}$ for the example of Figure 3.2(b) [52]. Output filtering can be relaxed with respect to square-wave mixing since the closest mixing spur is at a higher frequency.

Linearity

The linearity of the mixing transistors is important when using sine-wave mixing. Only sine-wave mixing with a linearly mixing transistor results in no input signal images in the output signal due to the mixing operation. Newer CMOS processes exhibit lower linearity and faster switching[60]. Therefore, square-wave mixing and quantized sine-wave mixing are more attractive than sine-wave mixing when implemented in CMOS. However, square wave mixing allows for a higher LO frequency than quantized sine-wave mixing, since the latter requires more LO signal transitions for the same fundamental frequency.

Complexity

Another disadvantage of quantized sine-wave mixing compared to the other two options, is the implementation complexity. Typically, multiple synchronized control signals and DAC cores are necessary to generate the quantized sine-wave mixing. This increases chip area and power consumption.

Feedthrough

Since both the square-wave mixing and the quantized-sine-wave mixing use switching signals with steep transitions, coupling between the control signals and the output of the Mixing-DAC can easily lead to spurs in the output spectrum at harmonics of the control signal frequency. However, the

frequency of this control signal feedthrough is $n \cdot f_{LO}$, which is much higher than the frequency of the primary output signal, and hence can be filtered out.

When using sine-wave mixing, the control signals do not contain sharp edges and hence sine-wave mixing is less sensitive to mixing-signal feedthrough to the output of the Mixing-DAC.

BB transition masking

Around the zero crossing of the sine-wave mixing signal, the mixer masks the Mixing-DAC input from the output[10]. Therefore, if the input data changes at that specific moment, the switching non-idealities of the transition from one input code to the next are masked by the mixing signal. Since timing errors in the transition between input codes introduces harmonic distortion in the DAC output signal[61, 62][88], this masking behavior improves the dynamic performance of the Mixing-DAC. The masking behavior is to a smaller degree also present in a quantized sine-wave Mixing-DAC. The square-wave mixing signal does not possess the aforementioned masking behavior, unless RZ signaling is used for the LO waveform.

Output power

The output spectrum amplitude in the first Nyquist band, i.e. the primary output signal, is dependent on the mixing signal shape. Assuming equal peak-to-peak amplitude for both the square-wave and the sine-wave, the power of the fundamental frequency in the square-wave spectrum is $\frac{\pi}{4} \approx 2.1$dB times the power of the fundamental frequency in the sine-wave spectrum. This assumes the square-wave contains infinitely fast transitions, which is not true in practice. Therefore, the output power of a square-wave Mixing-DAC can be up to 2.1dB higher than a sine-wave Mixing-DAC. The output power of quantized sine-wave mixing is comparable with sine-wave mixing.

Conclusion

Sine wave mixing is suitable for transmitters which have no output filter or a simple output filter. Square wave mixing is suitable for transmitters where the far-off spurious components are not important because of the presence of an output filter, and where no masking of the BB timing errors is required, unless RZ signaling is used. Hence, square-wave mixing is the most suitable mixing-signal shape for the demanding multicarrier GSM transmitter.

3.4.1.2 Amplitude - polarity

The mixing signal can alternate between +1 and -1, i.e. Symmetric around Zero (SaZ) signaling, or alternate between +1 and 0, i.e. Return to Zero

(RZ) signaling. Examples of Mixing-DAC implementations are categorized in Table 3.3, based on their LO signal shape and polarity behavior.

Table 3.3: Classification of exemplary Mixing-DAC architectures based on LO signal polarity and shape

Shape	**SaZ**	**RZ**
Sine-wave	Gilbert current cell sine-wave mixing [21, 22, 51] Conventional two step conversion with sine-wave mixing	Sine-wave RZ current source mixing [5, 10, 11, 13] Direct conversion [48]
Quantized sine-wave	Quantized sine-wave two step conversion[52]	
Square-wave	Single-ended square-wave mixing [54–56] Semi-differential square-wave current source mixing [57] Gilbert current cell square-wave mixing [18–20, 30, 31, 40] Global square-wave mixing [12] Conventional two step conversion with square-wave mixing [59]	Gilbert current cell RZ mixing [8, 9] Combined output RZ mixing [58] Gilbert current cell Multi-RZ mixing [17]
	Advantage: higher output power.	**Advantage:** lower sensitivity to data signal timing errors.

The reason for deliberately choosing RZ signaling is usually to mask the transitions of the BB signal. Timing errors in these transitions cause harmonic distortion. This masking is enabled by switching the BB signal during the 'Zero' phase of the LO signal[5, 17]. The effect of BB timing errors can also be alleviated by other techniques[47].

A downside of RZ mixing is that a portion of the output power is lost, typically 50%. Moreover, RZ mixing results in a large common mode signal at the output, which makes interfacing with other RF components troublesome. The lower output power and large common mode output signal can be alleviated by time-interleaving of two Mixing-DACs with RZ mixing.

However, the power efficiency of RZ mixing remains two times lower than SaZ mixing. RZ mixing is inherent to single-ended mixing[5, 12, 54], which is discussed in Section 3.5.1.

When data timing errors are a concern, and no other technique is employed to reduce the consequence of these timing errors, RZ signaling results in the highest linearity. When data timing errors are not relevant, SaZ mixing is the best option because of the output power advantage and RF interfacing advantage.

3.4.1.3 Frequency

Usually, the first Nyquist band at the fundamental LO frequency of the output spectrum is used as the primary output signal, i.e. $M = 1$ and $K = 0$ in (3.1). Higher Nyquist bands also contain signal energy which can be used as output signal [17, 63], i.e. $|K| > 0$ in (3.1). When the LO signal also contains energy at multiples (harmonics) of the fundamental LO frequency, also the signal energy around these LO harmonics can be used as primary output signal, i.e. $|M| > 1$ in (3.1). The signal energy in higher LO harmonic bands can be maximized by choosing square-wave mixing, and by choosing a specific duty-cycle for the LO waveform [58]. Figure 3.3 shows an exemplary Mixing-DAC output spectrum, where both the higher Nyquist zones and the LO harmonic bands are indicated. In this case, the LO frequency is twice the BB sample rate, i.e. $f_{LO} = 2 \cdot F_S$.

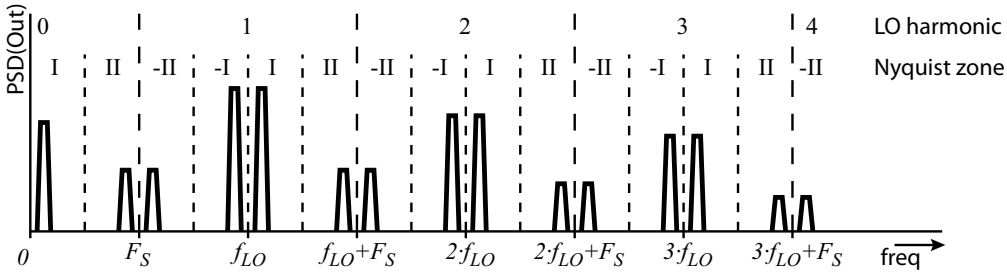


Figure 3.3: Multiple Nyquist zones and LO harmonic bands in a Mixing-DAC output spectrum contain signal energy and can be used as primary output zone. In this case, $f_{LO} = 2 \cdot F_S$

Using $|K| > 0$ or $|M| > 1$ does not result in better linearity while the signal power and Signal to Noise Ratio (SNR) is worse [17, 63]. Therefore, for high spectral purity, the output signal in the 1st Nyquist band and primary LO output band should be used as the output of the Mixing-DAC.

3.4.2 Low frequency mixer input signal (BB)

The other input of the mixer function is the baseband signal. The characteristics of the baseband (BB) mixer input signal can be divided in two subsets: amplitude and frequency characteristics. The amplitude characteristics are subdivided into resolution and polarity characteristics.

3.4.2.1 Amplitude - resolution

When the resolution of the BB signal is high, mixing is applied to the combined DAC output, i.e. 'global mixing'. When the resolution of the BB signal is 1 bit, mixing is applied locally to each DAC unit cell separately, i.e. 'local mixing'. Examples of global and local mixing are shown in Figure 3.4 and Figure 3.5 respectively. An option in between global mixing and local mixing is 'subset mixing', where a subset of the outputs of the DAC 1-bit cells are combined before the mixing operation takes place. An example of subset mixing is shown in Figure 3.6.

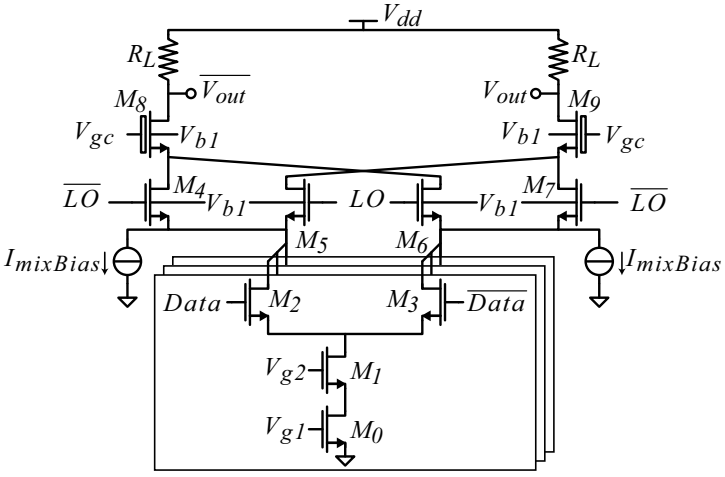


Figure 3.4: Global mixing and simultaneous operations; the architecture is synthesized based on the classification

Advantages and disadvantages of the various mixing locality options, and literature examples are given in Table 3.4. Subset mixing does not appear in open literature.

For global mixing, a very linear mixer is required since the current through the mixer in Figure 3.4 is data dependent. However, a current commuting CMOS transistor is not very linear. When increasing the bias current through the mixer ($I_{mixBias}$ in Figure 3.4), the ratio between data-dependent current

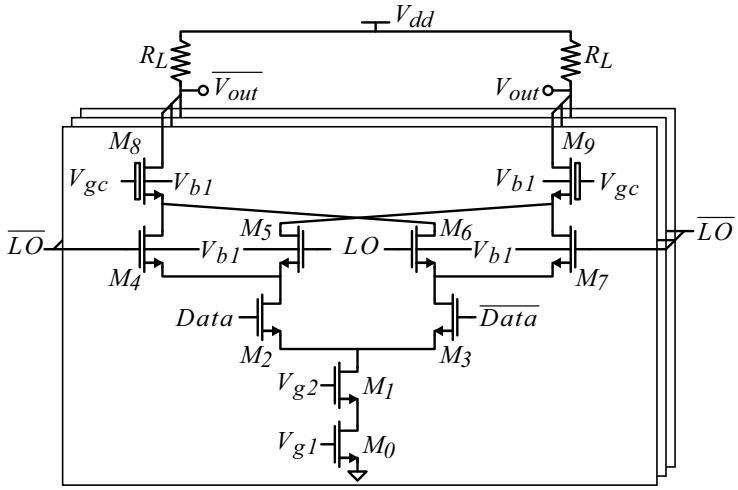


Figure 3.5: Local mixing and simultaneous operations; the architecture is synthesized based on the classification

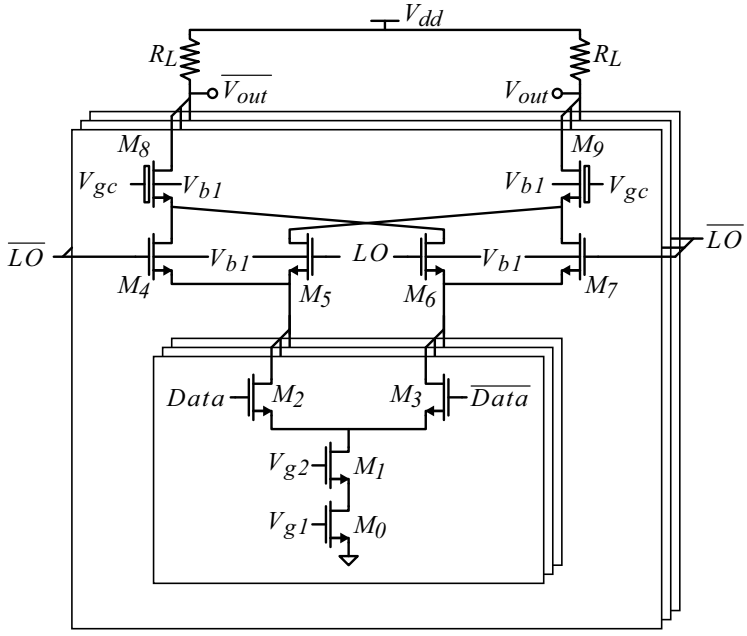


Figure 3.6: Subset mixing and simultaneous operations; the architecture is synthesized based on the classification

and data-independent current decreases, which increases the linearity at the expense of power consumption.

For local mixing, the current through the mixer only contains binary information, hence the linearity of the mixer is not important. However, mismatch between the numerous local mixers, i.e. mismatch in the LO signal timing or mismatch of the mix transistors (M_4-M_7 in Figure 3.4), can degrade the linearity of the Mixing-DAC. This effect is similar to timing errors in traditional baseband DACs, discussed in [64].

The chip layout of a Mixing-DAC with local mixing is expected to be more complex than with global mixing, since local mixing requires mixing transistors for each current cell and the routing of the LO signal to each current cell. A more complex layout can result in more undesired coupling between signals.

The advantages and disadvantages of subset mixing largely depend on the specific implementation. Subset mixing has a better mismatch sensitivity than local mixing. However, mixer linearity is a concern in subset mixing, since the current through the mixer is signal dependent. Subset mixing will add layout complexity since the layout does not have the regularity of local or global mixing.

The qualitative analysis of the differences between global mixing and local mixing does not give a clear view on which option is better for high spectral purity. Therefore, Chapter 5 and Chapter 6 discuss a quantitative analysis of the differences between these two options.

3.4.2.2 Amplitude - polarity

Almost all Mixing-DAC's employ Symetric around Zero (SaZ) signaling for the BB mixer input since there is no advantage in using Return to Zero (RZ) signaling. This RZ signaling is not to be mistaken for the RZ mixing of the LO signal, the advantages and disadvantages or which are discussed in Section 3.4.1.2. The difference between the polarity of the LO signal and the polarity of the BB signal are visualized in Figure 3.7.

RZ is only used when the architecture does not allow SaZ signaling because the chosen architecture is completely single ended[54]. Section 3.5.1 discusses the signal balancing.

3.4.2.3 Frequency

The sample rate of the BB mixer input influences the spectral content related to the term $K \cdot F_S$ in (3.1). These spectral components are usually undesired and can be filtered out. When these spectral components are filtered

Table 3.4: Examples of Mixing-DAC architectures for all three classes of mixing locality

Mixing locality	**Example**	**Characteristics**
Local mixing	Current source mixing [5, 10, 11, 13] Gilbert current cell mixing [8,9,18–22,30,31,40,51] Single-ended square-wave mixing [54–56] Semi-differential square-wave current source mixing [57] Direct conversion [48]	**Advantage:** insensitive to mixing transistor non-linearity. **Disadvantages:** sensitive to mixing transistor mismatch, larger chip area.
Subset mixing		Characteristics between local mixing and global mixing.
Global mixing	Two step conversion[52, 59] Combined output mixing [12, 58]	**Advantages:** insensitive to mixing transistor mismatch, smaller chip area **Disadvantage:** sensitive to mixing transistor non-linearity.

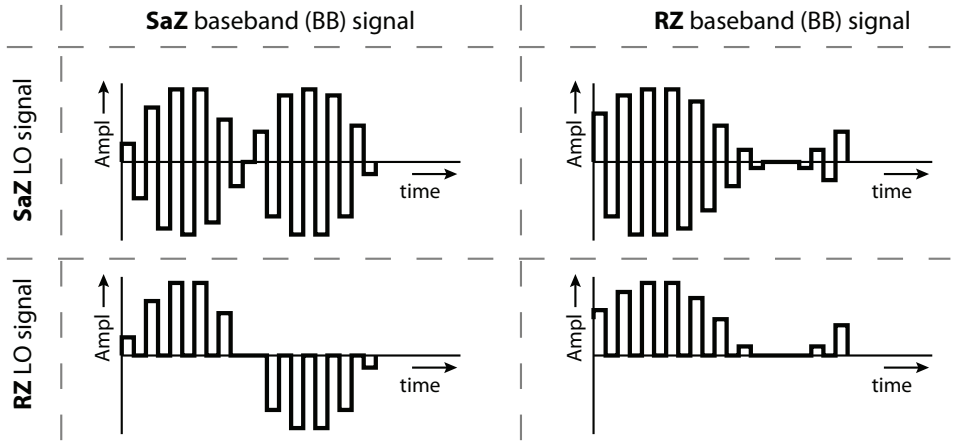


Figure 3.7: Mixing-DAC output signal, indicating the difference between BB polarity and LO polarity, with BB signal in analog domain (global mixing)

out between the D/A conversion and the mixing operation, the sample rate F_S of the BB signal can be chosen freely. However, when no intermediate filtering is present, or when this filtering is not possible (e.g. cascoded mixing, see Section 3.5.2), F_S should be an integer value of the LO signal frequency f_{LO}:

$$F_{LO} = n \cdot F_S, \qquad n \in \mathbb{Z}. \tag{3.2}$$

This synchronization is necessary to align the LO and BB transitions, and to align the BB spectrum repetitions, related to $|M| > 1$ and $|K| > 0$ in (3.1), in the output spectrum.

The advantage of a low sample rate is the low distortion due to timing errors [64]. The advantages of high sample rate include: low noise floor due to clock jitter[64], low quantization noise floor, large Nyquist bandwidth, and large separation between the main output signal and the image in the second Nyquist band. The choice for a certain sample rate is also influenced by the positioning of the harmonic distortion components.

3.5 Implementation level classification

At the implementation level, four different aspects are distinguished: balancing of the signals, sequence of the DAC and mixing operation, locality of mixing, and the usage of the mixing transistors.

3.5.1 Signal balancing

The two main signals in the Mixing-DAC (BB and LO) can both be implemented with single ended signaling, differential signaling or quasi-differential signaling[28]. Table 3.5 gives examples of Mixing-DAC architectures with different combinations of signal balancing. The various combinations are: both signals differential ('Fully differential'), one signal differential and one signal single ended ('Partially single-ended'), both signals single ended ('Single ended'), and combining two single ended Mixing-DACs to generate a differential-like signal ('Quasi-differential').

3.5.1.1 Reference current

Fully differential CS Mixing-DACs can use a reference current source which is always on. This enables the use of a large area which results in a high accuracy. In single-ended Mixing-DACs, the reference is switched on and off,

Table 3.5: Examples of Mixing-DAC architectures classified according to balancing of signals

Signal balancing	**Example**	**Characteristics**
Fully differential	Gilbert current cell mixing [8,9,18–22,30,31,40,51] Two step conversion [52, 59] Direct conversion [48] Combined output mixing [12, 58]	**Advantages:** insensitivity to common mode disturbances, low control signal feedthrough, suppression of even order harmonic distortion, undisturbed power supply current. **Disadvantage:** possibly larger chip area, low energy efficiency
Partially single-ended	Sine-wave RZ current source mixing [5, 10, 11, 13] Semi-differential square-wave current source mixing [57]	**Advantages:** moderate energy efficiency, partially insensitive to common mode disturbances, partial suppression of even order harmonic distortion **Disadvantage:** output signal contains large common-mode part
Single-ended	Single-ended square-wave mixing [54–56]	**Advantages:** high energy efficiency **Disadvantage:** interface mismatch with differential circuits later in the signal chain
Quasi-differential	Quasi-differential mixing [28]	**Advantages:** high energy efficiency, partially insensitive to common mode disturbances, partial suppression of even order harmonic distortion **Disadvantage:** output signal contains large common mode part

and hence must occupy a small area to enable fast switching. This small area results in a low accuracy, which degrades the linearity. Also quasi-differential signaling uses a switched references, which needs to have a small area which results in a low accuracy.

3.5.1.2 Disturbance

When a certain signal is implemented with differential signaling, and both wires are close together in layout, most disturbances equally couple to both signals. This common disturbance is attenuated by the following block in the signal chain, provided it has a high Common Mode Rejection Ratio (CMRR). With a single ended signal, disturbances are directly added to the signal.

Applying this to the Mixing-DAC, it can be argued that when both input signals are implemented with differential signaling (fully differential signaling), disturbances at the Mixing-DAC output are minimized. When one of the two signals is single ended, or when the Mixing-DAC is completely single-ended, the Mixing-DAC is most sensitive to disturbances, since each disturbance directly couples to the output signal. With quasi-differential signaling, both signals partially receive the same disturbance, depending on the spatial separation. However, the disturbance sensitivity is higher than for differential signaling since the two signals are usually not as close as differential signaling, and there is no common reference.

3.5.1.3 Even-order harmonics

Another advantage of differential signaling is the suppression of even order harmonic distortion. For the LO signal, even order harmonics only influence signal frequencies far outside the band of interest. However, for the BB signal, the frequency of the second order harmonic is close to the signal band and hence must be as low as possible. The actual suppression of even order harmonic distortion depends on the matching of the two paths of the differential signals. Partial single ended signaling and quasi-differential signaling exhibit partial second-order distortion cancellation, depending on the specific implementation.

3.5.1.4 Signal feedthrough

For some fully differential circuits with differential control signals, the feedthrough of the input signals to the output partially cancel. For instance, a fully differential Gilbert cell mixer significantly reduces the coupling between the LO signal and the output with respect to a single-ended mixer. For full cancellation, matching of the differential signal paths is required.

(Partially) single ended signaling and quasi-differential signaling do not offer input signal feedthrough cancellation.

3.5.1.5 Data-dependent power consumption

The power consumption of (partially) single ended signaling and quasi-differential signaling is dependent on the input signals. This causes input-dependent voltage drop (i.e. IR-drop) over the power supply connections, which can couple back to output stage and causes harmonic distortion in the Mixing-DAC output signal.

Fully differential signaling results in a constant power consumption, and hence the aforementioned coupling path does not cause harmonic distortion.

3.5.1.6 Chip area

Single ended circuits require less active components than differential structures, hence the active chip area of a single ended Mixing-DAC can be less. However, single ended signaling will require more decoupling capacitance than differential signaling on the supply nodes to filter the aforementioned input-dependent disturbance, which increases the chip area. The actual amount of required chip area depends on a number of factors and is specific for each architecture and implementation. Quasi-differential signaling requires approximately the same chip area as differential signaling, due to the double signal paths.

The larger active area of the active circuits and the double wiring of a differential solution usually results in higher parasitic capacitances. An example of this is the double output capacitance of a double balanced Gilbert cell mixer in comparison with a single balanced Gilbert cell mixer. This results in a higher power consumption or lower maximum frequency of differential circuits.

3.5.1.7 Output signal

Almost all RF circuits require differential input signals, hence the Mixing-DAC should produce such a signal. A fully single ended circuit cannot produce a differential output signal without additional circuitry, e.g. a balun. A partial single ended or quasi-differential Mixing-DAC has a positive and negative output terminal, but does not produce a true differential output signal. Instead, the common mode of the output signal is equal to half the magnitude of the differential output signal[13]. This output signal behavior is not always acceptable for RF applications. Only fully differential signaling produces a true differential output signal without a large common-mode component.

3.5.1.8 Efficiency

An advantage of single ended structures is that the power consumption of the Mixing-DAC output stage scales with the power of the signal, when polar signaling is used, see Section 3.3.2. For I/Q signaling, the power consumption of a single-ended Mixing-DAC is half of the power consumption of a differential Mixing-DAC, due to the DC level which is present in the BB input signal. The power consumption of quasi-differential signaling is similar to the power consumption of single-ended signaling.

3.5.1.9 Conclusion

For high spectral purity, the sensitivity of the Mixing-DAC to disturbances must be minimized, while power consumption is a secondary consideration. Therefore, fully differential signaling should be used for high spectral purity.

3.5.2 Sequence of operations

The sequence of the two operations in the Mixing-DAC (i.e. mixing and digital to analog conversion) can be chosen freely. The two operations can be done cascaded (mixing before the D/A conversion, or mixing after the D/A conversion), or cascoded. Cascoded mixing and D/A conversion can be done in the same current path (e.g. traditional Gilbert current-cell mixing of for instance Figure 3.5) or using a folded cascode structure (e.g. folded Gilbert-cell Mixing-DAC, proposed in Figure 3.8).

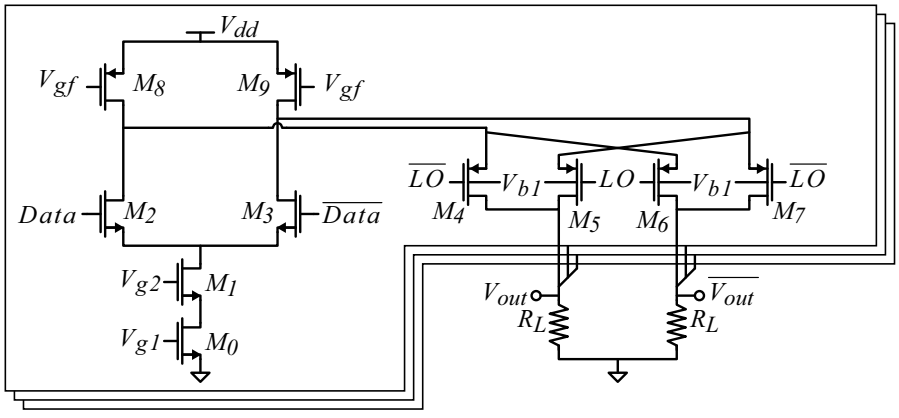


Figure 3.8: Mixing-DAC architecture with local mixing, simultaneous mixing and DA conversion with folded structure; the architecture is synthesized based on the classification

The choice for the sequence of D/A conversion and mixing operation, and the previously discussed choice for BB mixer input resolution (i.e. mixing locality, see Section 3.4.2.1) are interdependent. Figure 3.9 graphically shows this interdependence. For example: global mixing is not available with the cascaded 'mixing -> D/A conversion' sequence.

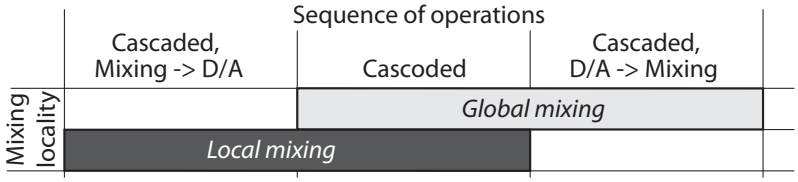


Figure 3.9: Choices for mixing locality and sequence of operations are interdependent

Examples for the classification based on the sequence of mixing and DAC operation in the Mixing-DAC are given in Table 3.6.

The main difference between the various operations sequences is the presence or absence of an analog voltage-to-current (V-I) and a current-to-voltage (I-V) conversion.

3.5.2.1 Cascaded: DAC before mixing

An I-V conversion using a MOST is a non-linear operation. 1-bit signals remain undistorted by definition when passing a non-linear operation while analog signals are distorted. Therefore, the linearity of analog mixers is limited and hence 'D/A -> mixing' sequence results in a non-linear mixing operation [6].

Applying mixing after the D/A conversion enables the use of an analog reconstruction filter between the DAC and mixer. This filter can remove the undesired signal images associated with $K \neq 0$ in (3.1) and reduces the requirements of the RF filter after the Mixing-DAC.

3.5.2.2 Cascaded: mixing before DAC

In cascaded 'Mixing -> D/A', mixing is done on 1-bit signals, hence a high linearity can be achieved. This digital mixing requires a DAC core which is capable of producing at least 8GSps for a 4GHz RF output, which is a very high speed for the required linearity. Known problems with high linearity DACs at high frequency are the data-dependent output impedance[65], random timing errors due to mismatch [64] and inter-symbol-interference.

Table 3.6: Classification of Mixing-DAC architectures based on sequence of the operations mixing and DAC

Sequence	Example	Characteristics
Cascaded: mixing before DAC	Single-ended square-wave mixing [54–56] Semi-differential square-wave current source mixing [57] Direct conversion [48]	**Advantages:** no mixing signal feedthrough to output because of mixing in digital domain, compatible with modern CMOS process technologies because of mixing in digital domain, possibility of intermediate filtering. **Disadvantages:** higher power consumption because of two-stage conversion, digital mixing reduces possibility of high output frequency
Cascaded: DAC before Mixing	Quantized sine-wave two step conversion[52] Conventional two step conversion [59]	**Advantages:** possibility of intermediate filtering. **Disadvantages:** higher power consumption because of two-stage conversion.
Cascoded	Sine-wave RZ current source mixing [5,10,11, 13] Gilbert current cell mixing [8,9,18–22,30,31,40,51] Combined output mixing [12, 58]	**Advantages:** no linearity degradation due to multiple stages in signal path, low power consumption. **Disadvantages:** no possibility of intermediate filtering, reduced current cell voltage headroom.

Timing errors are an important consideration in digital mixing. Mixing to the RF frequency can be done anywhere in the digital signal chain, ranging from the Mixing-DAC data input signal to the Mixing-DAC driver stage. Implementing the latter option results in a novel architecture which is proposed in Figure 3.10. The potentially large mismatch in the RC time constant of the *Mixed* nodes causes timing errors. These timing errors will introduce non-linear distortion and limit the spectral purity. The magnitude of the non-linearity due to the timing errors requires quantitative analysis, which is discussed in Chapter 6.

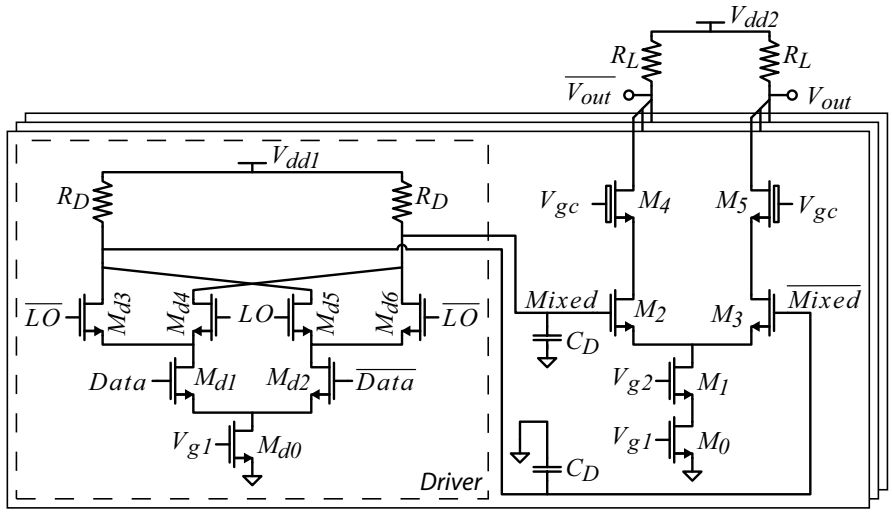


Figure 3.10: Digital mixing in the driver with fully differential, current steering DAC structure; the architecture is synthesized based on the classification

Applying digital mixing early in the signal chain enables digital filtering and digital I/Q combining, as opposed to mixing in the driver or later in the signal chain. Filtering in the digital domain reduces the requirements on analog RF filtering. However, digital filtering of the upconverted RF signal requires additional digital hardware. Digital filtering at the RF frequency can be very costly in terms of power when the RF output frequency is high. However, with newer CMOS process technologies, digital operations are becoming cheaper in terms of power consumption and chip area. I/Q combining (see Section 3.3.2) in the digital domain is accurate and does not suffer from the mismatch in I/Q combining or LO leakage of analog I/Q combining.

3.5.2.3 Cascoded

Cascoded mixing and DAC offers a choice in mixing locality. Section 3.4.2.1 shows that both global and local mixing have advantages and disadvantages. This is further discussed in Chapter 5.

Cascoded operations with the traditional Gilbert-cell mixing has the disadvantage that it requires additional voltage headroom with respect to a CS DAC, due to the transistors which implement the additional mixing function. Two exceptions are the use of the current source transistor as the mixer [5], or using a folded structure. Mixing using the current source is limited in speed

or accuracy, depending on the size of the current source transistor. Cascoded operations with the folded Gilbert-cell mixing has the disadvantage that it has a higher current consumption due to the additional current path through the folded mixer path, with respect to the CS DAC.

3.5.2.4 Conclusion

The three options for the sequence of mixing and D/A conversion are discussed in the previous sections. Cascaded operations with mixing after D/A conversion has an analog I/V and V/I conversion which results in severe non-linear distortion.

Cascaded operations with D/A conversion after mixing is sensitive to timing errors, but determining its magnitude requires further quantitative analysis, which is discussed in Chapter 4 and Chapter 6. Cascoded mixing and D/A conversion is sensitive to non-linear mixing or timing errors, depending on the mixing locality. Determining the actual magnitude of the resulting non-linear distortion also requires further quantitative analysis, which is discussed in Chapter 4 and Chapter 5.

3.5.3 Transistor usage

When using a current commutating transistor as a mixer, two different usage scenarios are available with respect to the LO and BB signals, see Figure 3.11.

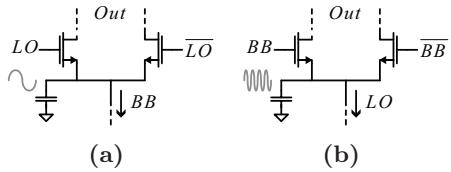


Figure 3.11: Difference between options of transistor usage: BB current through transistor(a) and LO current through transistor(b)

One option is to supply the gate of the mix transistor with the LO signal and put the BB signal in the current through the mixer, see Figure 3.11(a). An example of this mixing configuration is proposed in Figure 3.5.

The other option is to supply the gate of the mix transistor with the BB signal and put the LO signal in the current through the mixer, see Figure 3.11(b). This option is available for two architectures types. The first architecture is digital mixing, imagine Figure 3.10 but with swapped *LO* and *Data* connections. The second architecture group is when mixing and

DAC conversion are executed cascoded in the output stage and local mixing is applied, imagine Figure 3.5 but with swapped *Data* and *LO* signals, or mixing in the current sources [5].

Figure 3.11(b) shows that when the current through the mixer is at a high frequency, the source node of the mixer transistor contains high frequency voltage swing. For charging and discharging the parasitic capacitance at that node, signal current is used. Simulations have shown that the power loss can be as large as 1.5dB compared to the other transistor usage option.

Simulations of the Gilbert cell Mixing-DAC based on Figure 3.5 do not show a linearity difference between the two transistor usage scenarios, but output power difference is present. Therefore, the LO gate option is chosen although there is no advantage in spectral purity.

An overview of the classification based on transistor usage is given in Table 3.7.

Table 3.7: Classification of Mixing-DAC architectures based on transistor usage

Usage	**Example**	**Characteristics**
BB gate	Sine-wave RZ current source mixing [5,10,11, 13] Combined output mixing [12,58] Gilbert cell mixing [18–22,40]	**Disadvantage:** lower output power.
LO gate	Gilbert cell mixing [8, 9,30,31,51]	**Advantage:** higher output power.

3.6 Conclusion

The proposed systematic analysis and classification of Mixing-DAC architectures reveals the most crucial architecture choices, when high frequency high spectral purity is considered. The sequence of mixing and D/A operation and the resolution of mixing signals are important architectural choices that strongly determine the linearity of a Mixing-DAC architecture.

For high spectral purity at GHz frequencies, the following characteristics are optimal: current-steering principle, Cartesian signaling, square-wave mixing, symmetric around zero signaling for the LO and data signal, fully differential and LO-gate transistor usage. The best mixing-locality option depends on the magnitude of the mixer non-linearity and the timing errors

for global mixing and local mixing respectively. The best sequence of mixing and D/A conversion operations also depends on the impact of timing errors. However, mixing after the D/A conversion is expected to result in a poor linearity. These uncertainties require additional quantitative analysis, which will be discussed in the next chapter.

With the presented analysis of Mixing-DAC architectures, designers and researchers now have a clear insight on the impact of architectural choices on the spectral purity of the Mixing-DAC output signal.

4 Promising architectures

The preceding classification of Mixing-DAC architectures identifies a number of characteristics of a Mixing-DAC which are expected to enable the best spectral purity. This leads to three promising architectures, which require additional quantitative analysis. In the classification, the trade-off between various architectures was virtually technology-independent. But for the analysis of timing errors and mixer linearity, 65nm CMOS is assumed to be the implementing process technology. However, the analysis can be extended to other process technologies.

4.1 Introduction

The top level view of the synthesis of the most optimal architecture is shown in Figure 4.1. All possible architectures are considered. First, the classification is used to analyze which choices for all architectural aspects result in an architecture which is suitable for wide-band signals and is expected to lead to high spectral purity. These architectural choices are: current-steering principle, Cartesian signaling, square-wave mixing, symmetric around zero signaling for the LO and data signal, fully differential and LO-gate transistor usage. However, there are also architectural aspects which require further analysis. These architectural aspects are further analyzed using process information, which leads to a most optimal architecture.

4.2 Classification uncertainties

The previous chapter identifies two architectural choices which need further analysis: mixing locality and sequence of operations.

Mixing locality defines if mixing is done locally in each current cell or globally on the combined output of the current cells, see Section 3.4.2.1. Both local mixing and global mixing could result in a high linearity. For global

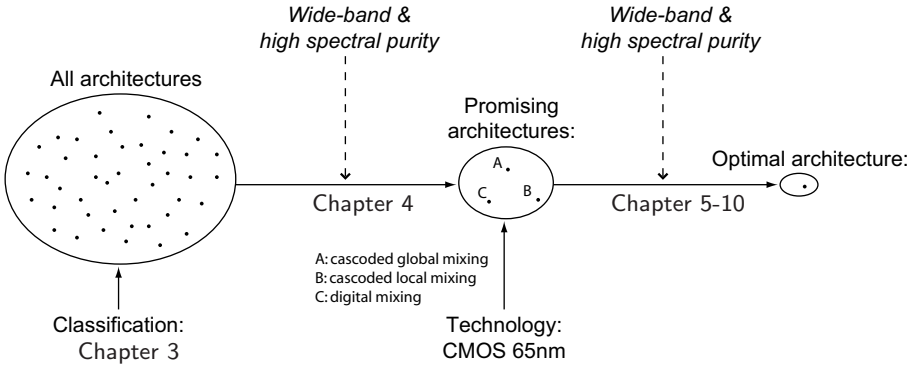


Figure 4.1: Process to synthesize a promising Mixing-DAC architecture

mixing, the linearity of the mixer is crucial. For local mixing, mismatch between the local mixers introduces non-linearity. The magnitude of both effects depends on the implementation and on the sequence of the mixing and D/A conversion, and requires quantitative analysis.

The sequence of the two Mixing-DAC operations (D/A conversion and mixing) determines the order in which these two operations take place. Three options can be distinguished: cascaded DAC before mixing, cascaded mixing before DAC and cascoded operations, see Section 3.5.2. Main difference between these two options is the presence or absence of V-I and I-V conversions. Cascaded DAC before mixing is expected to produce large non-linearities due to an analog V-I and I-V conversion. Hence, only cascoded operations and cascaded mixing before DAC can result in a high linearity.

4.3 Architecture synthesis

Combining the two options for the two architectural choices of the previous section, three promising architectures can be synthesized. These architectures are:

- cascoded global mixing, see Figure 3.4,
- cascoded local mixing, see Figure 3.5,
- digital mixing, see Figure 3.10.

The trade-off in the mixing locality between cascoded global mixing and cascoded local mixing is discussed in Chapter 5. The trade-off in the sequence of mixing and D/A conversion between cascoded local mixing and digital mixing is discussed in Chapter 6.

4.4 Other architecture considerations

Other important aspects of a CS Mixing-DAC architecture are: amplitude errors and segmentation. Amplitude errors between the current source of the current cells result in non-linearity in the transfer characteristics [7]. Chapter 8 presents a calibration method which is especially aimed at (Mixing-)DACs at high frequencies and with high robustness.

The trade-off for the segmentation of the Mixing-DAC is a complex problem. A theoretical framework for the segmentation of Nyquist DACs is published in [66]. However, that work is focused at low-frequency characteristics, i.e. INL and DNL. For Mixing-DACs, dynamic characteristics are much more important, e.g. IMD and SFDR. Therefore, a segmentation trade-off for high frequency Mixing-DACs is discussed in Chapter 9.

4.5 Conclusion

The classification identifies two architectural choices which need further analysis: mixing locality and sequence of operations. Combining these architectural choices results in three promising Mixing-DAC architectures: cascoded global mixing, cascoded local mixing and digital mixing. These architectures require quantitative analysis, which is discussed in the following chapters. The analysis of amplitude errors and segmentation is important, which is also discussed in the next chapters.

5 | Mixing locality

The previous chapter discussed that the mixing locality is an important trade-off in the architecture synthesis of a Mixing-DAC with high spectral purity. Local mixing is sensitive to mismatch between the local mixer in each current cell. Global mixing requires a linear mixer. Based on an estimation of parasitic capacitances on the most sensitive nodes, global mixing is shown to offer a lower linearity than local mixing. It is also shown that local mixing requires an output cascode in each current cell to sufficiently isolate the internal nodes from the large output voltage swing. An alternative to the output cascode is an output transformer, which is discussed in Chapter 7

This chapter is based on a paper published in the proceedings of the IEEE ISCAS 2012 conference [85].

5.1 Introduction

Numerous error sources that limit the Mixing-DAC linearity exist. Simulations show that the mixing locality has a major impact on the linearity. This mixing locality is also discussed in Section 3.4.2.1. Two main options for mixing locality are distinguished: global mixing and local mixing, see Figure 5.1.

In global mixing, the output signals of the unit DAC functions are first combined before being mixed. When implementing global mixing with transistors, the non-linearity of the transistor results in a non-linear mixing function.

When local mixing is used, the mixing is executed inside the DAC unit cells before the signals are combined. These unit cells contain only 1-bit signals, hence the mixing operation is inherently linear even if real transistors are used. However, mismatch between the mixing operation in the unit cells can deteriorate the linearity of the Mixing-DAC.

A third option for mixing locality is subset mixing. With subset mixing, a subset of the DAC unit element output signal is combined before the mixing

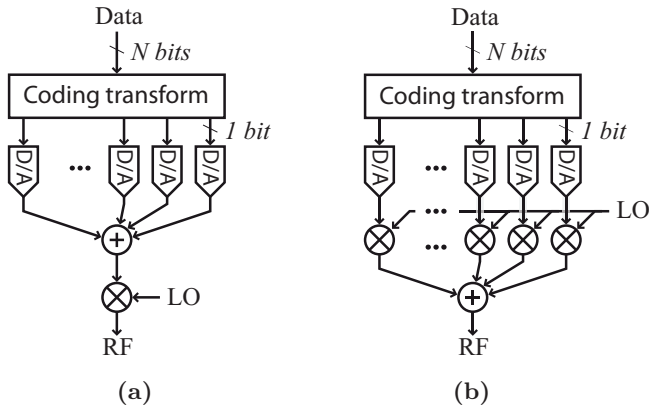


Figure 5.1: General model of global mixing (a) and local mixing (b)

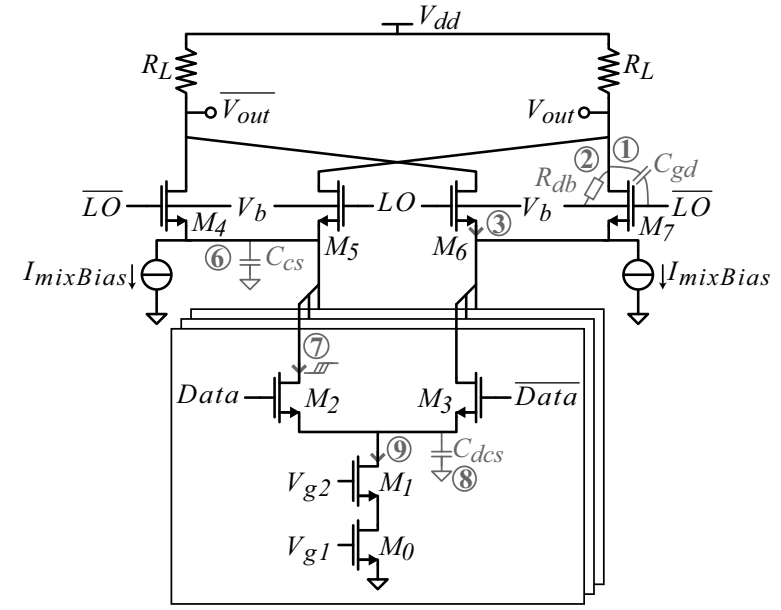
operation is applied, see Figure 3.6 in Section 3.4.2.1. The linearity of subset mixing largely depends on the implementation and the error sources are a combination of the error sources of local mixing and global mixing. Therefore, this third option is not discussed separately.

5.2 Analysis and simulations

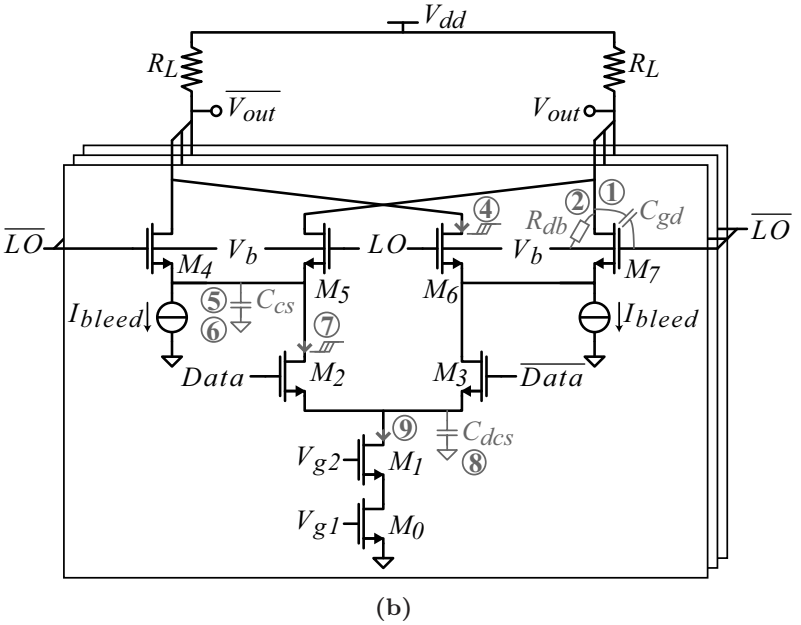
For the analysis of the two mixing locality options, a specific implementation is assumed: a 65nm 1.2V/3.3V CMOS process with thin-oxide and thick-oxide transistors. However, the analysis can be extended to other process technologies.

Since high linearity DACs are usually implemented as Current Steering(CS) DACs, the Mixing-DAC under investigation is chosen to be a CS Mixing-DAC. The simplified schematics of a CS Mixing-DAC with global mixing and local mixing are shown in Figure 5.2(a) and Figure 5.2(b) respectively

Table 5.1 summarizes the most important error sources of the CS Mixing-DAC which lead to non-linearity. The following subsections systematically analyze each error source separately, using the corresponding identification number in Table 5.1 and Figure 5.2. Unless otherwise indicated, simulations use the following simulation setup. The load resistors (R_L) are 25Ω (50Ω double terminated) each and the maximum output current is 20mA, generating a differential output-signal amplitude of $1V_{PP}$. The input signal is a two-tone full scale signal at f_{in1}=150MHz and f_{in2}=165MHz. Together with a mixing signal frequency (f_{LO}) of 4.02GHz, the resulting output signal



(a)



(b)

Figure 5.2: Transistor model of two options for mixing locality: global mixing (a) and local mixing (b)

Table 5.1: Mixing-DAC error sources leading to non-linearity

	#	**Description**
Output effects	1	Non-linear C_{gd} combined with output voltage swing
	2	Non-linear R_{db} combined with output voltage swing
Global mixing	3	Mixer input-current dependent mixing
Local mixing	4	Mixer data-dependent timing errors
	5	C_{cs} combined with the output-voltage dependent settling of the mixer common source nodes after data switching
Common	6	Common-source node disturbance due to LO transition combined with C_{cs}, dependent on output voltage swing
DAC effects	7	Data timing errors
	8	Disturbance due to data switching combined with C_{dcs}
	9	Mismatch between output current of current sources

frequencies (f_{out}) are 4.17GHz and 4.19GHz. In the simulations, the IMD3 of the output signal is used as a measure for the linearity.

5.2.1 Output effects

For isolating the Mixing-DAC non-linear output effects in simulation, the simulation setup of Figure 5.3(a) is used. An ideal Mixing-DAC output signal is generated by I_{out} and R_L, while M_1 and M_2 model the output non-linearity of a Mixing-DAC. A sweep over the output common mode voltage (V_{out_dc}) for various values of the output signal frequency (f_{out}) is used to show the effect of the output non-linearities, see Figure 5.3. This simulation clearly shows that an IMD3 of -85dBc at 4GHz is achievable with CMOS output transistors.

The most limiting output effects are: gate-drain capacitance and drain-bulk leakage (error sources 1 and 2 in Table 5.1 and Figure 5.2). These two effects mainly depend on V_{out_dc}, f_{out} and output signal voltage swing.

5.2.2 Specific global mixing non-linearities

In the global mixing simulation model, only transistors M_4 to M_7 of Figure 5.2(a) are real transistors. The other parts of the Mixing-DAC are implemented in Verilog-A.

Global mixing suffers from non-linearity errors due to the data-dependent current through the mixing transistors (error source 3). Global mixing can

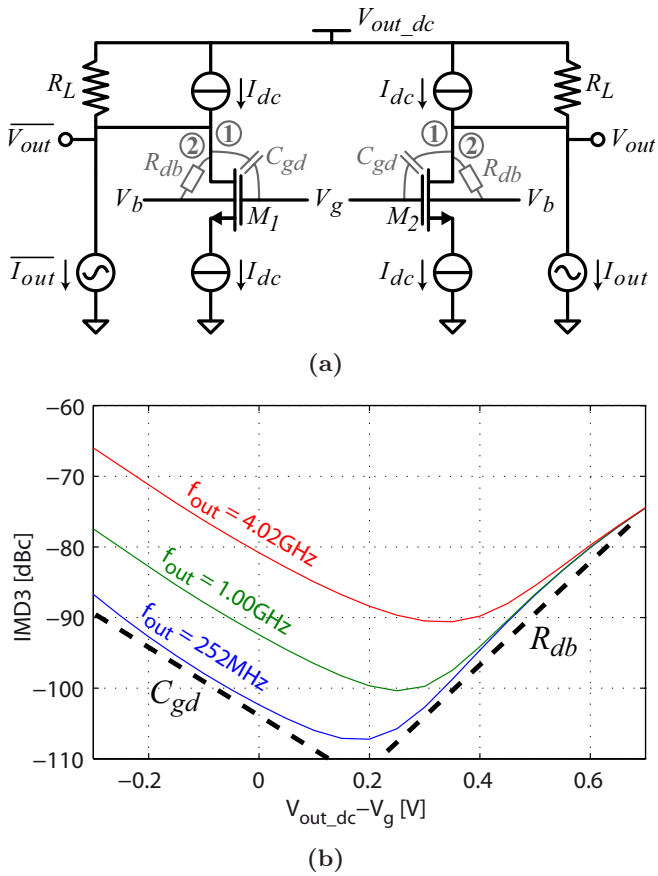


Figure 5.3: Output effect simulation: circuit (a) and simulation results (b)

be linearized by optimizing the ratio between signal current and bias current, hence by adding bias current through the mixer ($I_{mixBias}$ in Figure 5.2(a))

Figure 5.4 shows the IMD3 dependence on $I_{mixBias}$. For equal bias voltage levels at each node, increasing $I_{mixBias}$ also means increases the size of the mixing transistors, which increases the output-related non-linearity. Therefore, there is a maximum achievable IMD3 for global mixing which is -82dBc (see Figure 5.4). This is worse than the required -85dBc.

5.2.3 Specific local mixing non-linearities

In the simulation model of the local Mixing-DAC, only transistors M_4 to M_7 of Figure 5.2(b) are real transistors, the other Mixing-DAC parts are

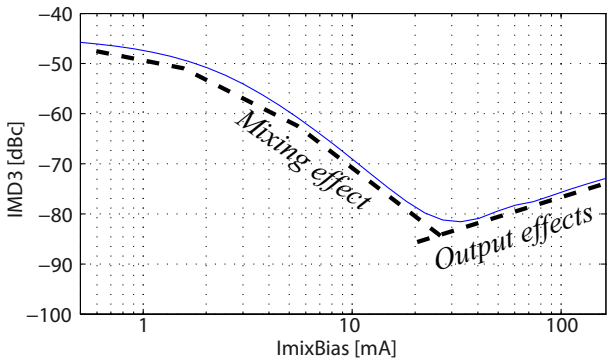


Figure 5.4: With global mixing, the mixing operation linearity depends on the added bias current

implemented using Verilog-A.

The current through a mixer transistor pair (e.g. M_4-M_5) exhibits a large step if the input code of the corresponding data transistor (e.g. M_2) changes. This generates a large voltage step at the mixer common source node V_{cs}. The settling behavior of the V_{cs} step depends on the output voltage (error source 5), which introduces a error charge on the parasitic capacitance C_{cs}. By optimizing I_{bleed}, this error source can be minimized.

Threshold voltage mismatch of the mixing transistors causes timing errors in the mixing operation between current cells, generating non-linearity (error source 4). A more elaborate discussion of the nature of the timing errors in a local Mixing-DAC is given in Chapter 6.

The results of a Monte Carlo (MC) mismatch simulation are shown in Figure 5.5. In this simulation the transition time of the LO waveform is 50ps and R_L is chosen very small (0.25Ω) to isolate the mismatch non-linearity. The simulated standard deviation of the timing errors is approximately 0.8ps. In the corresponding IMD3 distribution, 99% of all IMD3 results is better than -93dBc. Therefore, it is concluded that the LO timing errors do not degrade the dynamic linearity of the CS Mixing-DAC below the required IMD3=-85dBc. The timing errors due to imperfect signal routing are assumed to be negligible and hence are not taken into account.

5.2.4 Common mixing non-linearities

Both local and global mixing are very sensitive to capacitance C_{cs} at the common source node of the mixer (error source 6). During an LO transition a disturbance occurs at the common source node of the mixer transistors. The size of this disturbance is dependent on the Mixing-DAC input signal,

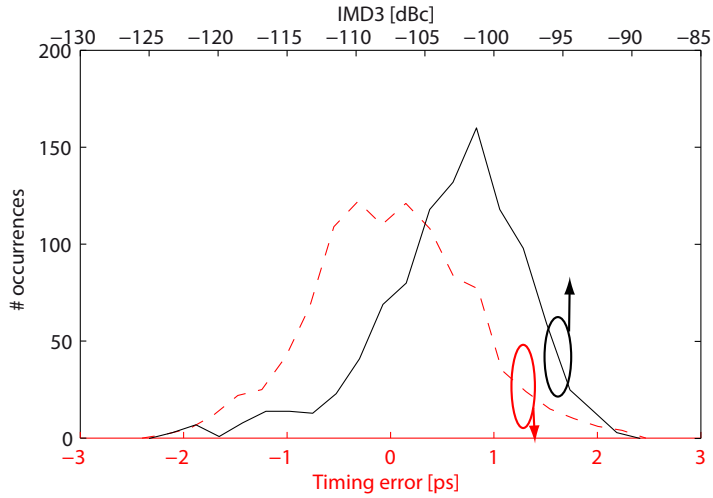


Figure 5.5: Monte Carlo mismatch simulation: distribution of timing errors between two current cells and resulting IMD3 distribution

generating non-linear distortion. For local mixing, this data dependence originates from the finite isolation between the output voltage swing and the mixer common-source node. For global mixing, the signal current through the mixer causes the above mentioned data-dependence.

Figure 5.6 shows the IMD3 dependence on the value of C_{cs}. In this simulation, the same models as given in Section 5.2.2 and 5.2.3 are used. Realistic values for C_{cs} are 10-20fF for local mixing and 1-2pF for global mixing. In those regions, the linearity of the Mixing-DAC is reduced to IMD3=-72dBc, which is much worse than the required -85dBc.

5.2.5 DAC non-idealities

Non-linearities specifically related to the DAC function (e.g. error sources 7-9) are not discussed in this chapter. Other authors have extensively discussed these effects [61, 64][87, 88]. Moreover, the DAC-function non-linearities are common to global mixing and local mixing.

5.2.6 Output cascode

For local mixing, the isolation between the output signal and the mixer common source node can be increased by adding a local output cascode to each cell. Figure 5.7 shows the schematic of a local Mixing-DAC with output cascode. Careful biasing ensures all transistors do not exceed their maximum

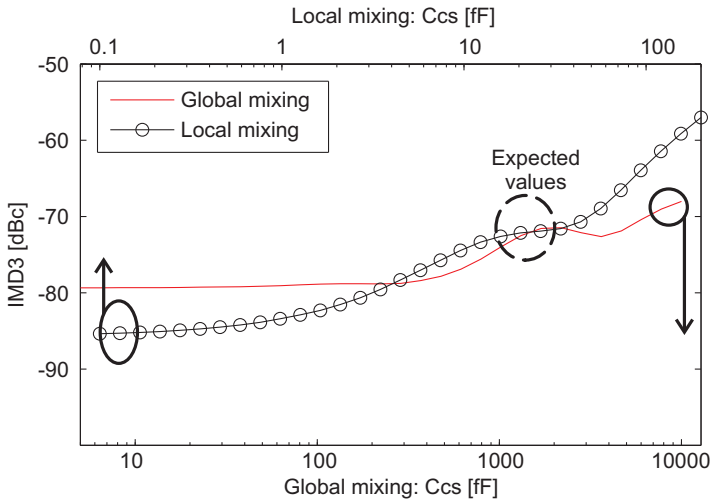


Figure 5.6: Sensitivity of mixing linearity to capacitance at the mixer common-source node, without output cascode

operating conditions. The new IMD3 dependence on mixer common source node capacitance is simulated using a simulation model where only M_4-M_9 are real transistors. The results are shown in Figure 5.8. It can be seen that the simulated performance is improved to IMD3=-92dBc. The isolation between the output and internal nodes can also be implemented using an output transformer, which is further discussed in Chapter 7.

Using a simulation model where all Mixing-DAC current cell transistors (M_0-M_9) are real transistors and assuming realistic wiring capacitances, the IMD3 is -88dBc, achieving the desired linearity.

For global mixing, adding additional isolation between the output and the mixer common-source node does not improve the linearity, since the C_{cs} dependent non-linearity in global mixing is due to the data dependent current through the mixer. Figure 5.8 confirms this claim, where the expected IMD3 value is -75dBc.

5.3 Conclusion

For high linearity Mixing-DACs, mixing locality is a major concern. For a current steering Mixing-DAC, the impact of the capacitance at the mixer common-source node (C_{cs}) dominates the Intermodulation Distortion (IMD) performance. For global mixing, this error source cannot be prevented. For local mixing, the IMD degradation due to C_{cs} originates from coupling

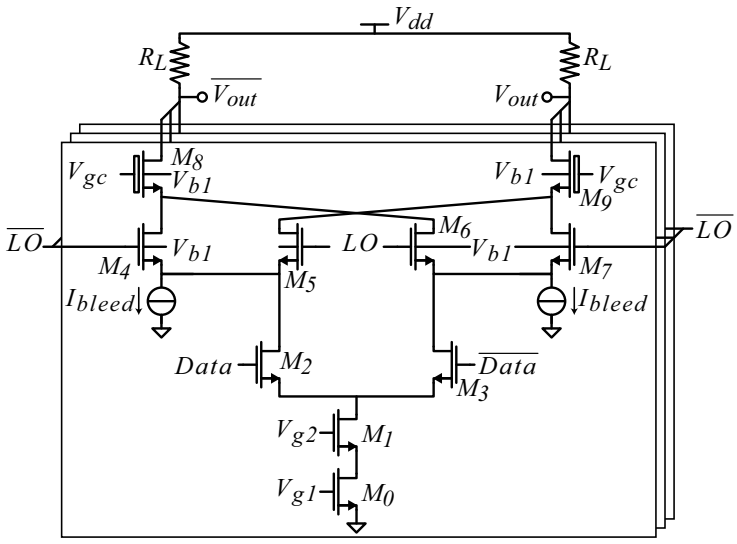


Figure 5.7: Local CS Mixing-DAC with local output cascode

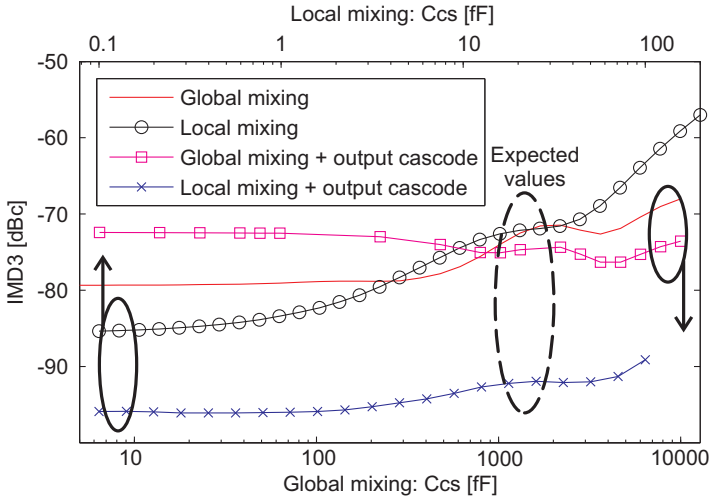


Figure 5.8: Sensitivity of mixing linearity to capacitance at the mixer common-source node, with and without output cascode.

from the mixer common-source node to the output voltage. Implementing a local output cascode reduces the sensitivity to C_{cs}. The expected IMD3 performance of the exemplary local mixing CS Mixing-DAC is <-88dBc at f_{out}>4GHz output frequency, enabling the use of a Mixing-DAC for multicarrier GSM applications.

6 | Timing errors

The architecture classification in Chapter 3 identified mixing locality and the sequence of mixing and D/A conversion are important trade-offs. Chapter 5 demonstrates that local mixing is the most promising mixing locality. In this chapter, the sequence of operations is investigated by comparing two architectures with local mixing: cascoded local mixing and cascaded mixing before DAC (digital mixing). It is shown, that the impact of timing errors is different for the two architectures. Cascoded local mixing has advantageous characteristics with respect to its timing errors, but timing errors in digital mixing do cause a non-linear distortion that is much worse than in the case of cascoded local mixing.

This chapter is based on part of a paper published at the IEEE ISCAS 2014 conference[83].

6.1 Introduction

A Current Steering (CS) Mixing-DAC with local mixing (see Chapter 5) can be very linear if the responses of all 1-bit switched current sources (current cells) are uncorrelated and identical, or ideally scaled for binary current cells. For high linearity at high frequency, both timing and amplitude of the 1-bit cells should be considered. The amplitude matching in CS (Mixing-)DACs has been thoroughly researched, and many intrinsic and correction methods exist[67], for example the calibration method proposed in Chapter 8. However, the synthesis of a Mixing-DAC architecture with the focus on timing errors is not discussed in open literature, while this is critical for achieving high linearity at high frequency.

This chapter focuses on local mixing, since this architecture can suffer from timing errors, see Chapter 5. With local mixing, the timing synchronization between the current cells is important, since timing errors degrade the linearity.

Current steering Mixing-DACs predominantly use a segmented implementation, with a unary scaled MSB part and a binary scaled LSB part. Without loss of generality, the analysis in this chapter assumes a 16 bit Mixing-DAC with a segmentation of 6bit unary MSB and 10 bit binary LSB, implemented in 65nm CMOS. The presented analysis is also applicable to other segmentations. The used signal frequencies are: input frequency f_{in}=150MHz, sample rate F_S=1.95GSps and LO mixing frequency f_{LO}=3.9GHz.

Section 6.2 discusses the characteristics of timing errors in a CS Mixing-DAC. Various architecture options are proposed in Section 6.3. The timing errors on the three most important signals in the Mixing-DAC are analyzed in Section 6.4, Section 6.5 and Section 6.6. A comparison between the proposed architectures is discussed in Chapter 6.7.

6.2 Timing errors characteristics

In CS Mixing-DACs, a segmented approach results in the most optimal performance. For a full-scale signal, the performance of the unary (MSB) part is most critical. Timing errors in the unary part are only randomly distributed. No systematic timing errors are present since each cell is identical.

Random timing errors predominantly can occur in three signals in the Mixing-DAC unit cells: *Data* input, *LO* input and the *Mixed* signal (see Figure 6.2 for *Data* and *LO*, and Figure 6.4 for *Mixed*). Only timing error *differences* between the current cells are relevant since they lead to non-linear distortion. The timing errors are assumed to be Gaussion distributed with zero mean.

Two types of timing errors are considered: delay timing errors and duty-cycle timing errors. An ideal periodic square waveform and the same waveform with timing errors are shown at the left of Figure 6.1. The difference between

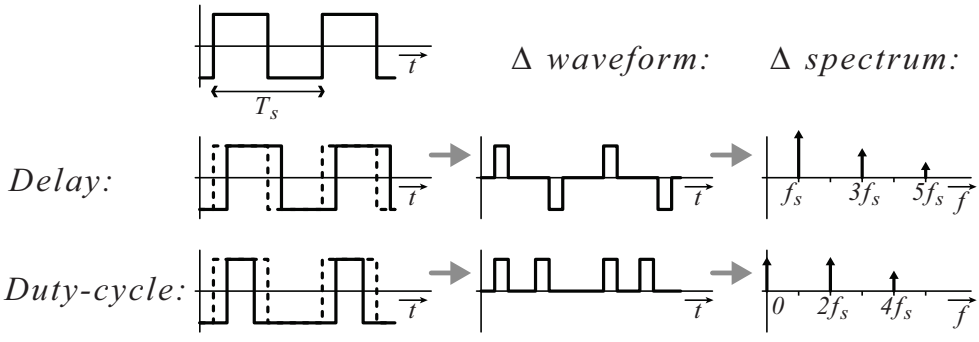


Figure 6.1: Time domain and spectral characteristics of timing errors

the base waveform and the waveforms with timing errors, and the spectra of these differences, are also shown. For all practical values of the timing errors, the error spectrum of the Δ-waveform with a delay timing error only contains odd harmonics of the base frequency, and the duty-cycle error spectrum only contains even harmonics of the base waveform. This spectral difference is important for the Mixing-DAC architecture analysis.

For all practical segmentations and for a full-scale signal, the response of the MSB unary current cells determines the performance. In this section the binary current cells are thus assumed to be ideal. The next subsections discuss possible Mixing-DAC architectures and the impact of timing errors at three nodes in a Mixing-DAC: *LO*, *Data* and *Mixed* signal. The value of the $\mathrm{SFDR_{RB}}$ in a a 200MHz band around f_{out}=f_{LO}+f_{in} is used as a measure of the spectral purity.

6.3 Architecture options

Two main Mixing-DAC architectures with local mixing, but with different choices for the sequence of operations, are: cascoded local mixing and cascaded mixing before DAC (digital mixing). Another degree of freedom is the locality of the LO driver, which can be either global or local. Hence, in this chapter three Mixing-DAC architectures are compared: cascoded local mixing with global LO driver, cascoded local mixing with local LO driver, and digital mixing. For digital mixing, the choice of a local or global driver does not influence the results of the timing error analysis.

Mixing-DAC architectures with cascoded local mixing with a global and local LO driver, are shown in Figure 6.2 and Figure 6.3 respectively. For digital mixing, the mixing can be done in the driver using a mixing-driver (see Figure 6.4) or earlier in the digital signal path.

In this chapter, intrinsic timing error sensitivity of the three proposed architectures is mutually compared. Numerous timing error calibration techniques for CS DACs exist [47, 61][88] but they are not considered since it is assumed that they are equally applicable to all proposed architectures.

6.4 Timing of *Data* signal

Timing errors in the *Data* input signal are extensively discussed in publications regarding CS DAC timing errors[47, 61, 64, 68][88]. The same conclusions and calibration techniques apply to all proposed Mixing-DAC architectures, which is verified with simulations. Therefore, *Data* timing errors have no influence on the architecture comparison.

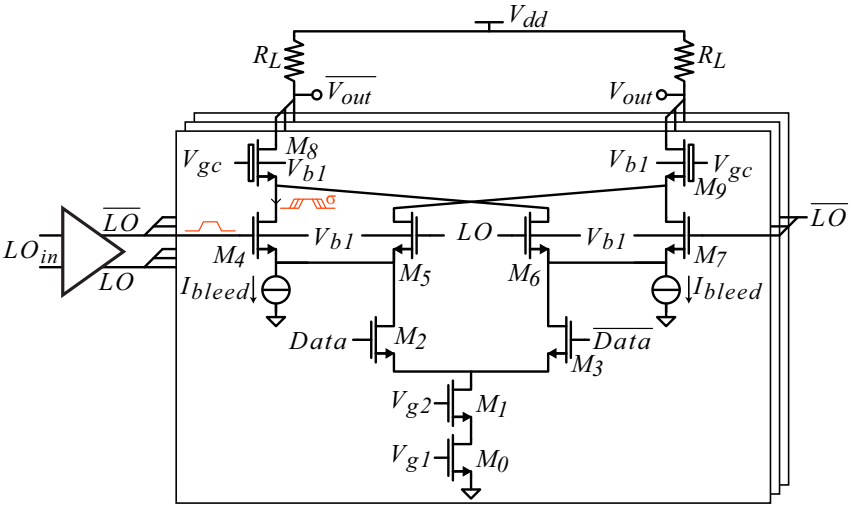


Figure 6.2: Local Mixing-DAC architecture with annotated timing errors: output stage mixing with a single global LO driver

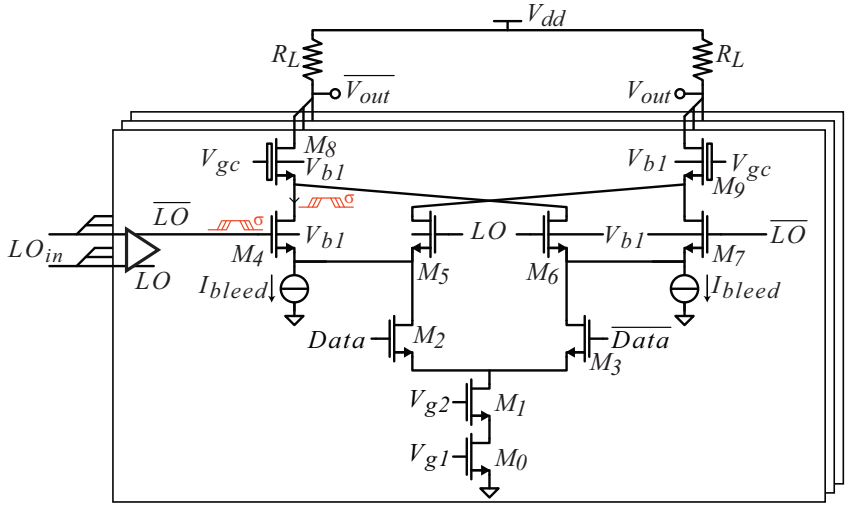


Figure 6.3: Local Mixing-DAC architecture with annotated timing errors: output stage mixing with local LO drivers

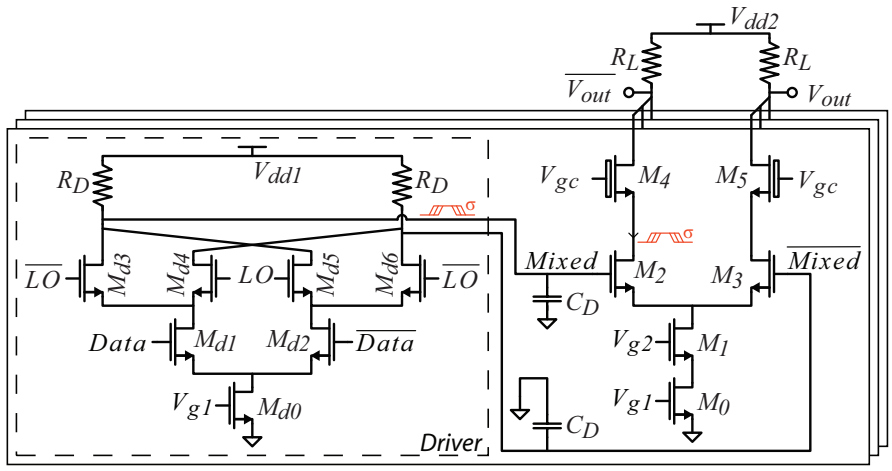


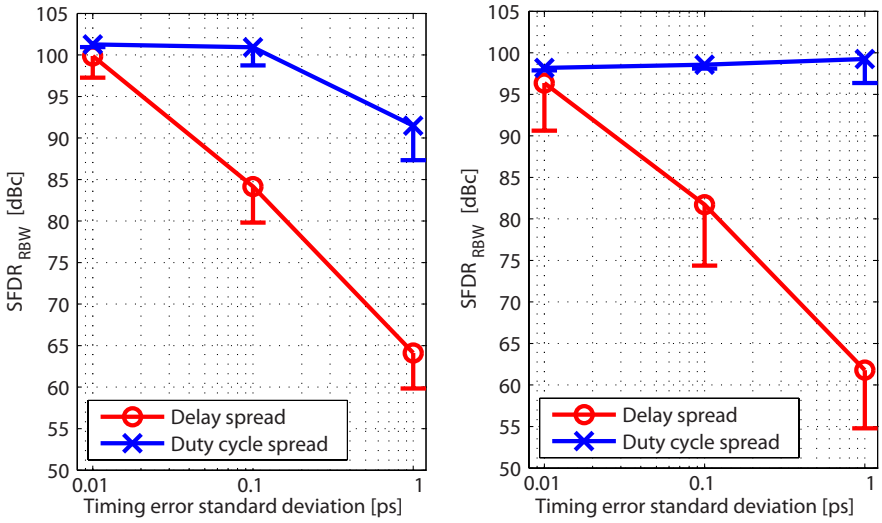
Figure 6.4: Local Mixing-DAC architecture with annotated timing errors: proposed example of mixing in the digital domain with mixing-driver

6.5 Timing of *LO* signal

Sensitivity to LO timing errors is specific for Mixing-DACs. Figure 6.5(a) shows the results of transistor level simulations of the circuit of Figure 6.2 at f_{LO}=3.9GHz, where the two types of timing errors are deliberately introduced in the LO input. Each current cell has its own independent random timing error, which is fixed for one trial of the Monte Carlo simulation. To isolate the nonlinear distortion due to timing errors, other error sources are eliminated: $R_L \approx 0$ (to reduce output related effects [85]), the drivers and current sources are modeled with ideal components with realistic drive strength and transition times.

A 90% yield SFDR_{RB} of 85dBc at f_{LO}=3.9GHz requires $\sigma(delay)$<55fs and $\sigma(duty\text{-}cycle)$<1.3ps. Hence, the Mixing-DAC is very sensitive to delay errors, but at least 20 times less sensitive to duty-cycle errors. The cause for the difference in sensitivity to the two types of timing errors can be seen in Figure 6.6, where two output spectra with added delay and duty-cycle timing errors in the LO signal are shown. The delay timing errors cause spurs around f_{LO} (which is close to the output band) while the duty-cycle timing errors create spurs around $2{\cdot}f_{LO}$. This can be expected, see Figure 6.1, since the delay error spectrum contains energy at the fundamental frequency (i.e. f_{LO}), while the duty-cycle error spectrum contains energy at double this frequency (i.e. $2{\cdot}f_{LO}$).

With a single common LO signal (i.e. a single global LO driver, see



(a) *LO* timing errors in Figure 6.2 **(b)** *Mixed* timing errors in Figure 6.4

Figure 6.5: Resulting $\mathrm{SFDR_{RBo}f}$ timing errors (error bar=90%, #trials=20)

Figure 6.2) and output stage mixing, predominantly duty-cycle timing errors occur. The duty-cycle timing errors mainly originate from threshold mismatch and gain mismatch in the mixing transistors, M_4-M_7 in Figure 6.2. This can be verified in the results of Monte Carlo mismatch simulations for the architecture of Figure 6.2, which is shown in Figure 6.7, where only the mixing transistors have mismatch. The mismatch-induced timing errors are almost exclusively duty-cycle timing errors. The standard deviation of each type of timing error are: $\sigma(delay)$ =35fs and $\sigma(duty\text{-}cycle)$ =0.92ps. These values are very close to the required values. The resulting 90% yield $\mathrm{SFDR_{RB}}$ is approximately 85dBc.

A significant delay error can only originate from imperfect layout of the *LO* distribution or output recombination structure. Careful layout of the corresponding tree structures can reduce the expected delay error to less than ±5fs.

A local *LO* driver, as proposed in Figure 6.3, introduces additional duty-cycle timing errors *and* delay timing errors, which can easily exceed 200fs, while <55fs is required.

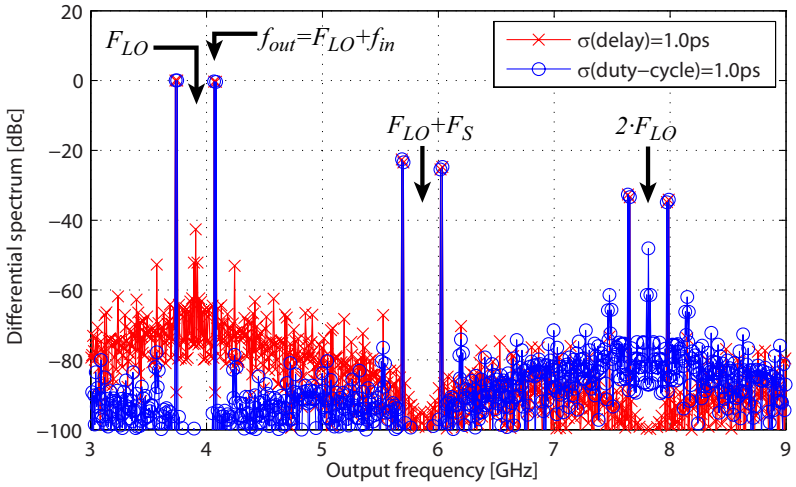


Figure 6.6: Schematic level simulation, comparing the spectral impact of delay and duty cycle timing errors

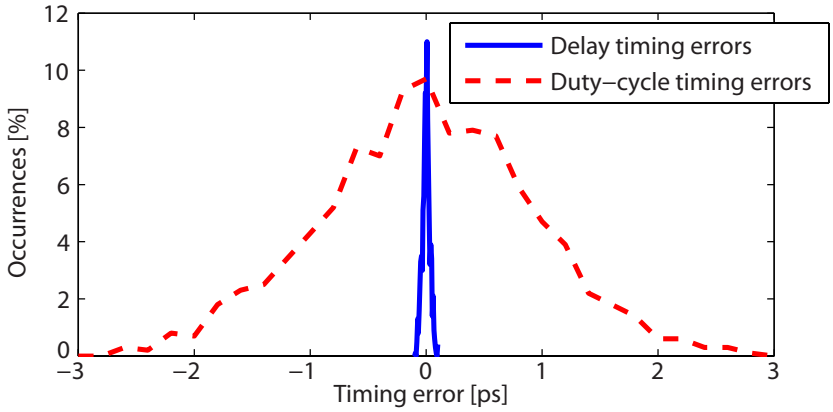


Figure 6.7: Simulated *LO* timing errors due to mixer mismatch

6.6 Timing of *Mixed* signal

Figure 6.5(b) shows the results of a Monte Carlo transistor level simulation of the Mixing-DAC architecture with mixing-driver of Figure 6.4, where $R_L \approx 0$, and with ideal current sources, and ideal *Data* and *LO* drivers. In each current cell with mixing-driver, a random timing error is deliberately introduced in the *Mixed* signal (i.e. output of mixing-driver). Again, the performance is very sensitive to delay timing errors: $\sigma(delay)$<31fs for 90% yield SFDR_{RB}>85dBc.

Mismatch in the mixing-driver, e.g. in the current source (M_{d0} in Figure 6.4), load resistor value (R_D) or (parasitic) load capacitance C_D of the CML driver, can generate large timing errors. Note that C_D is not an intentional capacitor, but consists of the parasitic capacitance of the driver transistors (M_{3d}-M_{6d}), wiring and the switches in the output stage (M_2 and M_3). The exemplary implementation of the aforementioned Mixing-DAC with digital mixing is simulated with mismatch in the value of R_D and C_D. The simulation results are presented in Table 6.1. The frequencies of the signals are: 3.9GHz LO signal and 160MHz and 175MHz dual-tone input data at 1.95GS/s sample rate.

Table 6.1: Simulated digital Mixing-DAC non-linearity due to mismatch in the driver RC-constant

	$\sigma_{RC} = 1\%$	$\sigma_{RC} = 3\%$	$\sigma_{RC} = 10\%$
σ(delay)	87fs	0.26ps	0.87ps
SFDR_{RB}(90%)	76dBc	66dBc	56dBc

The relationship between the 90% yield SFDR_{RB} value and the spread in C_D and R_D is:

$$SFDR_{RB}(90\%) \propto 1/\sigma_{RC}^2 \tag{6.1}$$

The physical positions of the R_D's and C_D's are spread over a large area, i.e. the complete output stage width which can be as wide as 1mm. Therefore, 3% mismatch estimation is realistic. A mismatch of 3% in R_DC_D results in a delay timing error of $\sigma(delay)$=0.26ps, while $\sigma(delay)$<31fs is required. The corresponding 90% yield SFDR_{RB} value of is -66dBc. Hence, mismatch in the local mixing-driver already causes enough timing errors to severely limit the spectral purity.

6.7 Architecture comparison

A summary of the performance of cascoded local mixing and mixing in the driver is given in Table 6.2.

Digital mixing with a mixing-driver requires $\sigma(delay)$<31fs for a 90% yield SFDR_{RB} of85dBc, while the expected timing errors are much larger, leading to a inferior spectral purity. Cascoded local mixing (Figure 6.2) requires: $\sigma(delay)$<31fs and $\sigma(duty - cycle)$<1.3ps. Simulations show that these requirements can be achieved when a single global LO driver is used. Hence, the architecture with cascoded local mixing achieves the highest performance and is expected to achieve the target SFDR_{RB} of 85dBc.

Table 6.2: Comparison of the two Mixing-DAC architectures

Architecture	**Figure**	**$SFDR_{RB}$**	
		Nominal	90% yield
Cascoded local mixing	6.2	88dBc	85dBc
Cascaded mixing in the driver	6.4	84dBc	66dBc

6.8 Conclusion

Timing errors are a main concern in high speed highly linear Mixing-DAC architectures. The random timing errors of the unary part influence the choice of the most optimal architecture. The linearity of a Mixing-DAC architecture is very sensitive to delay timing errors in the *LO* and *Mixed* signal. Hence, the architecture with cascoded local mixing achieves the highest performance. The simulated performance of this architecture is: 90% yield $SFDR_{RB}$=85dBc at f_{out}=4GHz.

7 | Output transformer

Chapter 5 shows that the isolation between the large output voltage swing and internal nodes is important for achieving high linearity. A traditional solution is the use of a local output cascode. Another solution, discussed in this chapter, is an output transformer. It is shown that using a high turn ratio results in a high attenuation of the output voltage swing from the secondary to the primary side. But it is also shown that a high turn-ratio also results in a high power consumption.

This chapter is based on a paper published in the proceedings of the IEEE ECCTD 2013 conference [84].

7.1 Introduction

An RF-DAC based on the Current Steering DAC approach can be very linear when the 1-bit switched current sources are independent and identical. However, among the main causes of harmonic distortion are the output related error mechanisms, which are discussed in Chapter 5. The large signal swing at the output (typically $1V_{pp}$) modulates the non-linear output capacitance and couples to internal nodes due to the finite output impedance. When the output signal swing is reduced, the linearity of the converter improves.

For a simple simulation, Figure 7.1 shows the IMD3 (i.e. linearity) versus the load resistance at $I_{out,pp}$=20mA and f_{out}=4GHz. At the typical load resistance of 50Ω, the IMD3 is -71dBc, which is not sufficient for a highly demanding application such as multicarrier GSM. Since the output related non-linearity mainly originates from the switching output transistors, only those transistors are realistically modeled in the simulation of Figure 7.1.

In Chapter 5, local output cascode transistors are used to shield the internal switching transistors from the output, and hence improve the linearity. This chapter proposes another solution: the use of an output transformer, which is shown in Figure 7.2. When the turn ratio of the

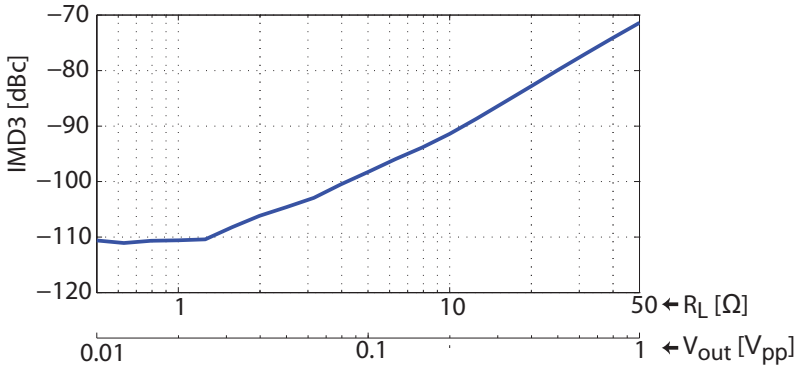


Figure 7.1: Current Steering Mixing-DAC output linearity dependence on the load resistor (i.e. output voltage swing)

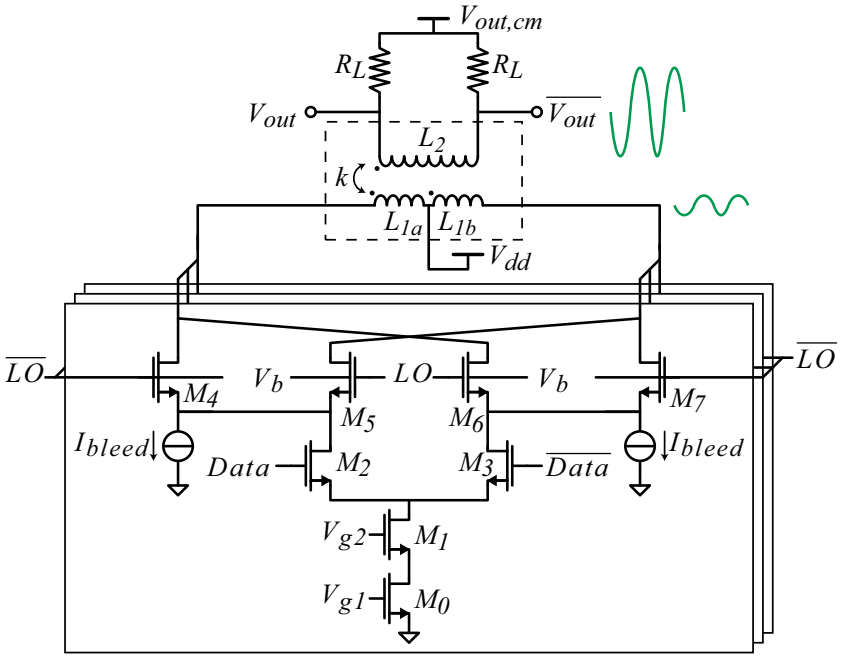


Figure 7.2: Current Steering Mixing-DAC with output transformer

transformer n is larger than one, the load impedance seen from the Mixing-DAC current cells is roughly R_L/n^2. Therefore the voltage swing at the output of the Mixing-DAC current cells is lower than at the load, which reduces the output related non-linearities. An RF-DAC with output transformer has been

presented before [28], but it has never been proposed for linearity reasons.

The next section compares these two linearity enhancement methods. In Section 7.3, implementation options for the output transformer are discussed. Section 7.4 presents calculations of the specific transformer setup. Section 7.5 presents simulation results of the transformer and Mixing-DAC with transformer.

7.2 Cascode vs. transformer

Two methods for RF-DAC linearization, discussed in this section, are: local output cascode and output transformer. Note that the two methods are not mutually exclusive, but can be combined. Table 7.1 gives an overview of the comparison.

Table 7.1: Comparison of cascode and transformer for RF-DAC

	Cascode	**Transformer**
Area	++	--
Power consumption / efficiency	++	--
Common mode isolation	--	++
Voltage headroom	--	++
High frequency output filtering	-	+
DC output filtering	o	o
Added non-linear elements	-	+
High frequency capability	-	+
Noise	-	+

Main disadvantages of the output transformer method include power consumption and chip area usage. For the transformer, a turn ratio $n > 1$ is required to decrease the output related non-linear distortion. However, the Mixing-DAC output current needs to be increased by n to maintain equal signal power at the load, increasing the power consumption and area of the Mixing-DAC core. In addition, inductors usually consume significant chip area and create power losses.

Main advantages of the transformer are as follows. The output transformer introduces common mode isolation between the Mixing-DAC and the load, resulting in a completely independent common mode level at the load. Moreover, the required voltage headroom is lower than for the output cascode. Especially in advanced process technology nodes, the voltage headroom is severely limited. The output transformer also filters the low frequency offset and higher frequency undesired output components. Low frequency filtering

can be a disadvantage of the transformer when DC-coupling to a next stage is required. A core-less transformer (i.e. passive element) is highly suitable for high frequencies and does not introduce significant additional non-linear distortion. An output cascode on the contrary consists of transistors (i.e. active element), which are inherently non-linear and introduce additional parasitic capacitances, limiting the maximum signal frequency. The wide-band output noise of the Mixing-DAC is mainly generated by the current source transistors. Since the output current is increased in the transformer method, the SNR will also improve for equal current density.

7.3 Implementation options

Three different transformer implementation options are considered: on-chip (i.e. on-die), on-laminate and on-PCB; see Figure 7.3. In principle, multiple cascaded transformers with different implementation can also be used. For simplicity, in this chapter only a single transformer is considered.

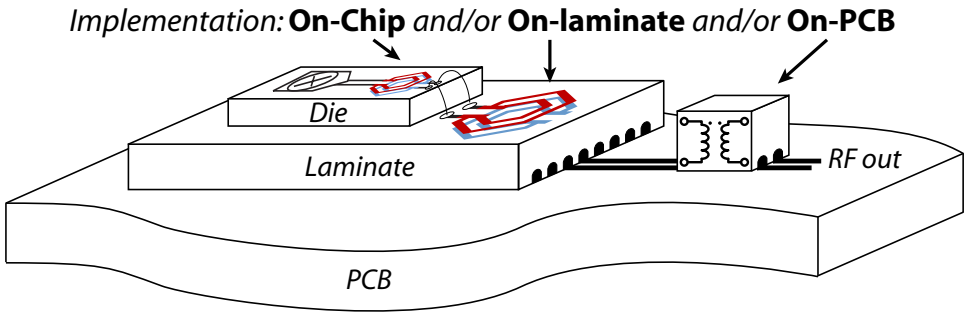


Figure 7.3: Three implementation options for the Mixing-DAC output transformer

On-chip transformers are very popular in literature [69–71], but not yet proposed for linearity enhancement of RF-DACs. For the design and simulation of a fully customized transformer, numerous tools are available. The interface between the Mixing-DAC and the transformer is very good, since both reside on the same substrate. However, the transformer coils can be bulky for the low target frequencies, which can make the on-chip transformer expensive.

A discrete on-PCB transformer is the most inexpensive and flexible option, but is only available in a limited number of configurations. The interface between the transformer and the Mixing-DAC contains one or multiple bondwires, which can degrade the transformer performance.

With on-laminate transformers, large inductors are possible due to the low cost of laminate area compared to standard CMOS chip area, and custom transformer design is possible. However, a bondwire interface is present between the Mixing-DAC and the transformer. Flip-chip assembly can minimize the inductance and resistance of the chip-to-laminate interface.

Simulations of the transformer model including bondwires reveal the most suitable implementation, see Section 7.5.2.

7.4 Theoretical framework

The transfer of a Mixing-DAC with a transformer as output buffer can be calculated. Two models of a Mixing-DAC with transformer are discussed in this section. Calculation results and simulation results provide the optimal parameter values.

7.4.1 Transformer model

For calculations and simulations, the *Direct form model* of [69] is used. Figure 7.4 shows this transformer model with the source and load configuration, where k is the transformer coupling factor ($k < 1$), and n is the turn ratio $n = \sqrt{L_2/L_1}$.

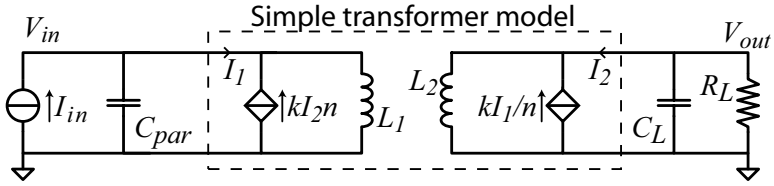


Figure 7.4: Simple transformer model for calculations

The signal source is the Mixing-DAC, which can be modeled as a current source (I_{in}) with finite output impedance. In practice, the output resistance is much larger than the load resistance, hence it is not modeled. The output capacitance C_{par} is typically 1pF. The load impedance is ideally only a resistor (R_L), but typically also contains some capacitance (C_L).

In reality, transformers also contain parasitic capacitances and resistances. Bondwires are usually not taken into account in transformer analysis, but can severely limit the transformer performance. Therefore, also an extended model of the transformer with the aforementioned elements is used in the simulations, see Figure 7.5.

Calculations on transformer characteristics in open literature usually discuss the transformer performance in the case of matched source and

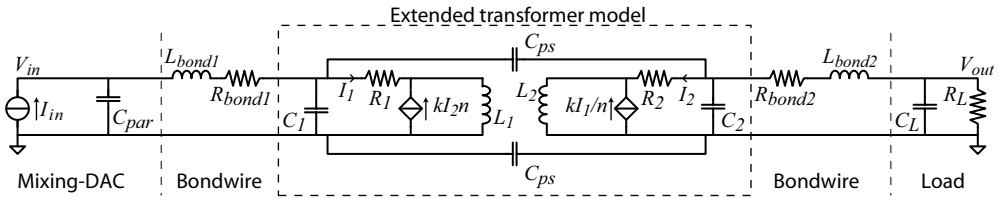


Figure 7.5: Extended model of a transformer in a Mixing-DAC

load impedances and only dicuss S-parameters. In the Mixing-DAC output transformer, the source impedance is not matched and the S-parameters do not give the desired information. Instead, the voltage attenuation between input and output, $H_{VV}(\omega)$, is of main importance. The power transfer is analyzed using the input current to output voltage transfer of the transformer $H_{VI}(\omega)$. Both performance metrics are discussed in the next subsections. For the first order approximation, the simple model of Figure 7.4 is used.

7.4.2 Current-to-voltage transfer $H_{VI}(\omega)$

It is assumed that the output current of the Mixing-DAC current cells is scaled with n, such that the output power at the load is constant. The output impedance of the Mixing-DAC current cells also changes accordingly: $I_{in} = I_{in,0} \cdot n$, $C_{par} = C_{par,0} \cdot n$. The calculated transfer characteristic is:

$$H_{VI}(\omega) = \frac{V_{out}(\omega)}{I_{in}(\omega)} = H_0 \cdot \left(\frac{1}{1 - \left(\frac{\omega}{\omega_{res}}\right)^2} \right) \cdot \left(\frac{1}{1 + j\frac{\omega}{\omega_H} + \frac{1}{j\frac{\omega}{\omega_L}} + \frac{1}{j\frac{\omega}{\omega_A} + \frac{1}{j\frac{\omega}{\omega_B}}}} \right), \tag{7.1}$$

where:

$$H_0 = R_L \cdot k \cdot \frac{1}{n}, \qquad \omega_{res} = \sqrt{\frac{1}{(1-k^2)\,\frac{L_2}{n} C_{par,0}}}, \tag{7.2}$$

$$\omega_L = \frac{R_L}{L_2}, \qquad \omega_A = \frac{R_L k^2}{L_2(1-k^2)}, \tag{7.3}$$

$$\omega_H = \frac{1}{R_L C_L}, \qquad \omega_B = \frac{n}{k^2 R_L C_{par,0}}. \tag{7.4}$$

An approximation of the bode plot of the $H_{VI}(\omega)$ amplitude is shown in Figure 7.6. The passband amplitude H_0 is determined by R_L, converted by the

transformer with ratio k/n. The lower frequency corner ω_L is mainly due to the R_L/L_2 time constant. A resonance peak and second order low-pass filter corner is present at ω_{res}. This resonance is caused by an LC tank, formed by the leakage inductance $(1-k^2)L_2$ and the Mixing-DAC output capacitance seen at the transformer output $C_{par,0}/n$. The other high frequency pole ω_H is mainly due to the $R_L C_L$ time constant. The other two roots at ω_A and ω_B only slightly influence the H_{VI} transfer characteristic around the resonance frequency.

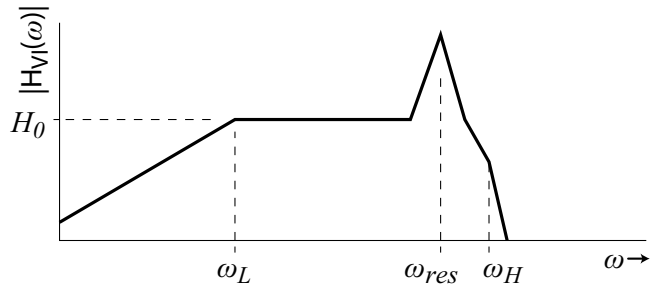


Figure 7.6: Amplitude of the $H_{VI}(\omega)$ of the simplified transformer model

7.4.3 Voltage gain $H_{VV}(\omega)$

The voltage gain $H_{VV}(\omega)$ of the transformer is a measure for the linearity improvement which can be attained when adding the transformer to the output of the Mixing-DAC:

$$\begin{aligned} H_{VV}(\omega) =& \frac{V_{out}(\omega)}{V_{in}(\omega)} \\ =& k \cdot n \cdot \frac{1}{1+(1-k^2)j\omega\frac{L_2}{R_L} - (1-k^2)\omega^2 C_L L_2} \end{aligned} \tag{7.5}$$

As expected, the low frequency value of $H_{VV}(\omega)$ is determined by $k \cdot n$. The bandwidth is determined by the leakage inductance due to imperfect transformer coupling $L_2(1-k^2)$ together with R_L and C_L.

7.5 Simulation results

In this section, simulation results of the separate transformer and simulations of the Mixing-DAC with output transformer are presented.

7.5.1 Transformer

The configuration of the simulation setup is: $R_L = 50\Omega$, $C_L = 500fF$ and $C_{par,0} = 1pF$. Simulations have shown that an optimal transformer configuration for the exemplary application (0.7-4.0GHz) is: $L_2 = 8nH$, $k = 0.85$ and $n = 4$ (hence, $C_{par} = 4pF$ and $L_1 = 0.5nH$), where k and n are limited by what is practically achievable. The resulting simulated transfer characteristic $H_{VI}(\omega)$ and voltage gain $H_{VV}(\omega)$ are shown in Figure 7.7.

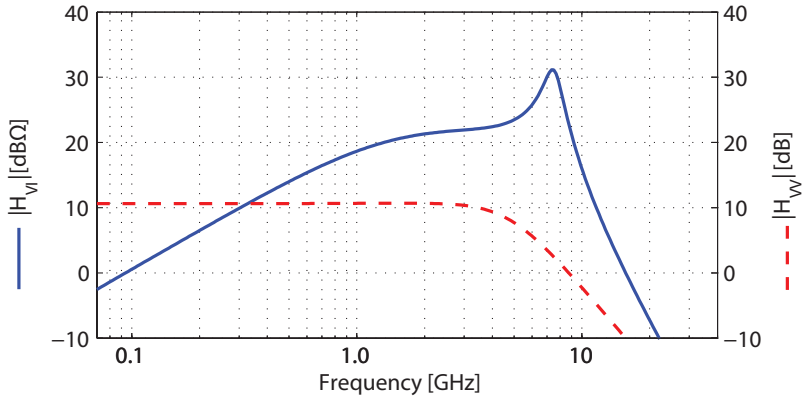


Figure 7.7: Simulation results of simple transformer model

The shapes of the simulated $|H_{VI}(\omega)|$ and $|H_{VV}(\omega)|$ closely match the calculated shapes. The passband amplitude of $|H_{VI}(\omega)|$ is 22dBΩ, resulting in approximately $1V_{pp}$ signal at R_L for I_{in}=n·20mA=80mA. The passband flatness is 6dB. At low frequencies $|H_{VV}(\omega)|$ is 10.7dB, lowering to 9.4dB at 4.0GHz. The $|H_{VI}(\omega)|$ in-band flatness of 6dB can be improved by improving k or C_{par}, which are both practically limited. However, simple digital preprocessing can easily counteract the non-flatness of the power transfer. The 4GHz $|H_{VV}(\omega)|$ value can only be increased by decreasing the L_2 inductance, increasing the turn ratio n, or improving the coupling factor k, which are all impractical or undesirable.

7.5.2 Extended transformer model

One of the important extensions to the simple transformer model is bondwire inductance and resistance. The bondwire inductances act in the same way as imperfect transformer coupling k, lowering the resonance frequency in $|H_{VI}(\omega)|$ and lowering the bandwidth of $|H_{VV}(\omega)|$.

The transformer input inductance value L_1 is very low ($L_1 = L_2/n^2$), hence the transformer input is sensitive to additional bondwire inductance.

Figure 7.8 shows the $|H_{VI}(\omega)|$ flatness and the values of $|H_{VV}(\omega)|$ at the extremes of the band of interest, as a function of L_{bond1}. For higher L_{bond1} values, the $|H_{VV}(\omega)|$ bandwidth and amplitude degrades, and the resonance peak in $|H_{VI}(\omega)|$ shifts in the band of interest, causing a poor $|H_{VI}(\omega)|$ flatness. Therefore, L_{bond1} should be less than 0.15nH, which is not practical. Hence, transformers for high frequency and with high turn ratios (i.e. small inductance at the transformer input) can only be implemented on-chip, resulting in $L_{bond1} \approx 0$.

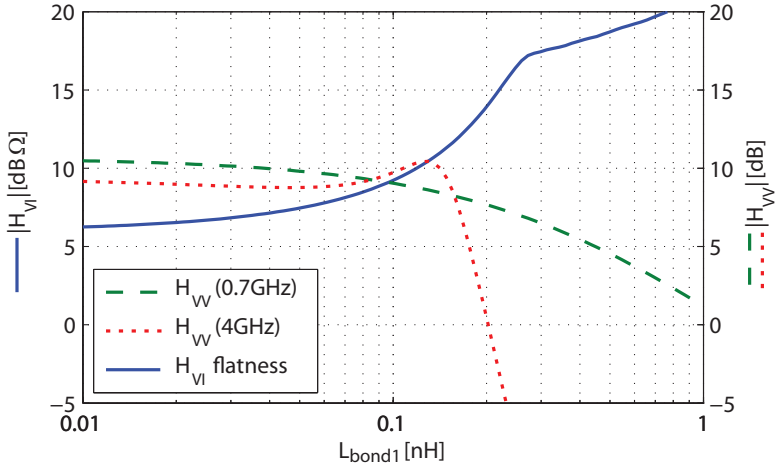


Figure 7.8: Transformer performance degradation due to L_{bond1}

A bondwire at the transformer output with achievable values for the inductance and resistance (L_{bond2}=0.5nH, R_{bond2}=1Ω) does not degrade the transformer performance significantly.

The required parasitic coil resistance and capacitance for performance preservation are not critical. The following values are assumed: C_1=100f, C_2=200fF, C_{ps}=200fF, R_1=1Ω, R_2=4Ω.

7.5.3 Transformer and Mixing-DAC

The Mixing-DAC model, mentioned in Section 7.1, together with the simple and extended transformer model of Section 7.5.1 and Section 7.5.2 is used to verify the linearity improvement when using the output transformer on a Mixing-DAC. The IMD3 dependence on n of the Mixing-DAC for the most critical output frequency (4GHz) is shown in Figure 7.9.

The signal voltage swing at the load is approximately $1V_{pp}$ for all simulations. For an almost ideal transformer 'Simple, k=0.95', the IMD3 at n=4 is -89dBc, 18dB better than the conventional Mixing-DAC. However,

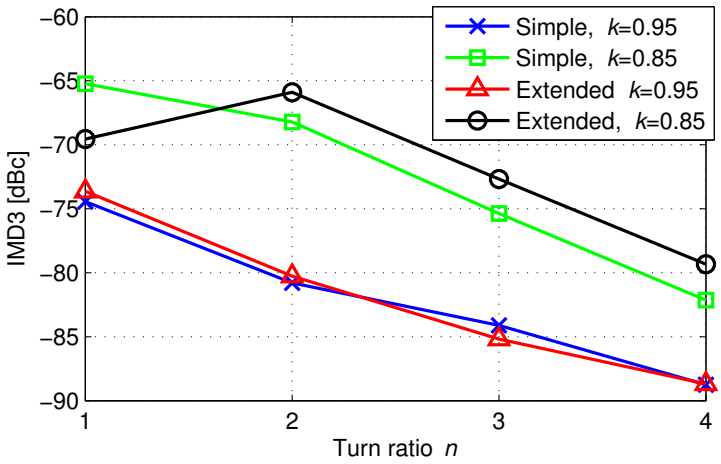


Figure 7.9: Simulated IMD3 for Mixing-DAC with output transformer

the linearity degrades when the non-idealities of the transformer are added, specifically at lower values of k. Also k itself strongly influences the linearity. For the simulation setup with insufficent linearity improvement, it can be observed that signal power at the transformer input at multiples of the LO frequency is not attenuated by the transformer because of the limited transformer bandwidth. This unattenuated high frequency signal power causes non-linear distortion in the Mixing-DAC. A higher k increases the bandwidth of the transformer and hence improves the linearity. Using the extended transformer model at n=4 and assuming k=0.9 is achievable, the resulting IMD3 is -85dBc, 14dB better than the conventional Mixing-DAC.

7.6 Conclusion

Output related non-linearity is a major concern for highly linear current steering RF-DACs. This chapter proposes a novel approach for RF-DAC linearization based on a wide-band impedance transformation. Simulations of the presented transformer model clearly indicate that for the implementation of an output transformer for high-frequency wide-band RF-DACs, on-chip transformer implementation is the only viable approach.

Higher turn ratios result in a larger voltage gain, and hence a higher linearity improvement. However, higher turn ratios also increase the power consumption of the DAC output stage, thus decreasing the efficiency of the Mixing-DAC. Simulations of a specific RF-DAC model with an output

transformer show that the IMD3 improves by about 14dB. The proposed novel output-transformer based RF-DAC architecture is expected to enable the design of highly linear wide-band transmitters.

8 | Calibration

One of the sources of non-linearity in Current Steering (CS) DACs and Mixing-DACs is mismatch of the current sources in the switched current cells. Some traditional calibration methods compensate this mismatch by means of a calibrating DAC in each current cell. However, this method tries to calibrate a mismatch value with a nominal value. These two values respond differently to changes in the environment, e.g. temperature changes. Hence, the calibration is only valid for the same environment as the calibration environment.

A novel calibration method is discussed in this chapter, that compensates the mismatch of the main current source with the mismatch of another current source. This ensures equal response to environment variations. Simulations demonstrate the effectiveness of the calibration method.

This chapter is based on a paper published in the proceedings of the IEEE ISCAS 2011 conference [87] and in the proceedings of the annual STW ProRISC 2011 conference [86].

8.1 Introduction

The static DAC linearity, e.g. INL (Integral Non Linearity), is mainly limited by the finite matching of the DAC current source transistors. The mismatch between identically sized and biased transistors is given in (8.1) [72].

$$\left(\frac{\sigma_I}{\bar{I}}\right)^2 = \left(A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2}\right) \cdot \frac{1}{2WL} \tag{8.1}$$

Using large devices ($W \cdot L$) reduces the random mismatch, but increases occupied area and hence increases the systematic mismatch and degrades high-frequency performance. The dynamic linearity, e.g. SFDR (Spurious Free Dynamic Range), is usually limited by the achieved static linearity, and further reduced at high speeds by the parasitic capacitances and resistances

of the current source transistors. Therefore, to achieve high linearity at high speed, both small and accurate current source transistors are necessary.

To improve the DAC static linearity and to reduce the size of the DAC current source transistors, calibration of the mismatch errors of the DAC current sources can be used. An example of calibration in a Current Steering DAC (CSDAC) is shown in Figure 8.1 [46]. For an analysis of different correction methods, see [73].

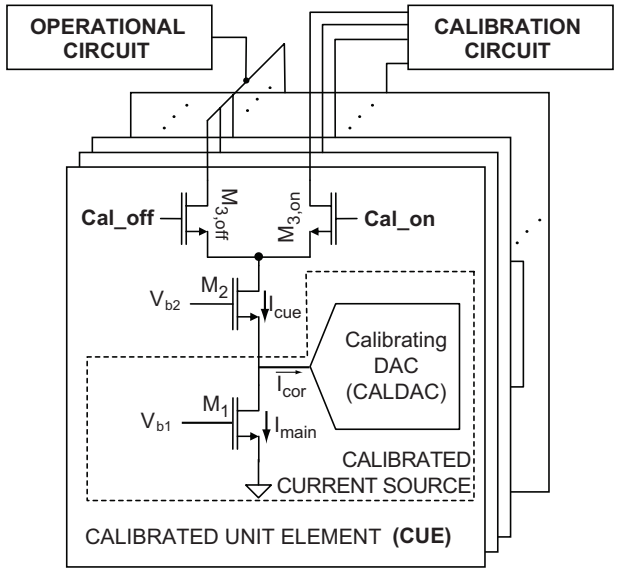


Figure 8.1: Implementation of CalDAC calibration principle in a current cell[46]

Two types of calibration strategies can be distinguished: foreground and background calibration. Background calibration is continuously running while the DAC is actively used [74]. It suffers from increased power consumption during operation and the output signal may be polluted by spurious components of the calibration activities. Foreground calibration is only active when the DAC is idle, e.g. at startup, and hence avoids the aforementioned disadvantages. However, discrepancies in the environment between calibration and use, e.g. temperature or supply voltage, can reduce the advantages of the calibration. In addition, the advantages of the existing calibration methods also reduce at high speeds [74].

The proposed foreground calibration method uses identical unit transistors in both the current source and the CalDAC to guarantee matched responses to disturbances and temperature variations. The current cell is calibrated by combining unit transistors with opposite mismatch within one current cell

such that their combined mismatch is minimized.

The next section explains the temperature and disturbance sensitivity of the conventional calibration. In Section 8.3, a new CalDAC implementation and calibration algorithm is proposed which is insensitive to temperature variations and disturbances. Section 8.4 shows simulation results.[1]

8.2 Temperature and disturbance dependence

An exemplary schematic of a CSDAC using CalDAC calibration is shown in Figure 8.1, which is used in [75] and [76]. In the current cell, named *Calibrated Unit Element* (CUE), transistor M_1 is the main current source with output current I_{main}. Due to process spreading and systematic mismatches, the value of I_{main} deviates from the nominal designed value $\bar{I}_{main}$, i.e. for the n-th current source $I_{main,n} = \bar{I}_{main} + I_{error,n}$. The CalDAC generates a correction current such that the output of the CUE $I_{cue,n}$ equals the value of $\bar{I}_{cue}$.

In the example of Figure 8.1, the state of transistors $M_{3,off}$ and $M_{3,on}$ decides if the CUE output current is either used for the normal operation of the DAC or connected to the *Calibration circuit* and measured for calibration.

An exemplary implementation of a conventional CalDAC is shown in Figure 8.2 [76, 77]. The main current source M_1 consists of M transistors. The CalDAC, consisting of transistors $M_{cal,1}$ to $M_{cal,N}$, adds the required correction current.

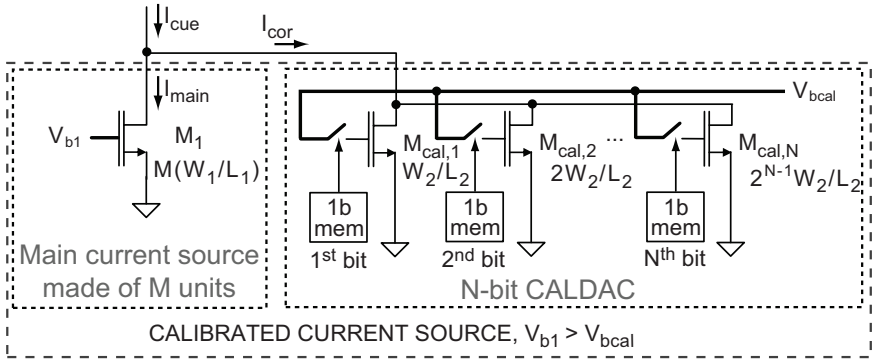


Figure 8.2: Conventional implementation of the CalDAC

[1] The presented calibration method is not used in the Mixing-DAC design of Chapter 11. Instead, the calibration method which is available in the baseline DAC from the industry partner (see Section 11.1) is used, which can calibrate both the static and dynamic errors of a DAC [3].

To achieve high post-calibration static linearity, the LSB of the CalDAC should be much smaller than the LSB of the DAC [7]. Therefore, the transistors of the CalDAC have a smaller overdrive voltage ($V_{GS} - V_T$) and usually also different width (W) and length (L) with respect to the main current source transistors. With the exemplary DAC of [76], measurements show that a relative correction step of $\frac{I_{LSB,cor}}{I_{LSB,main}} < 0.2$ results in a 12 bits linearity and a relative correction step of $\frac{I_{LSB,cor}}{I_{LSB,main}} < 0.1$ results in a 13 bits linearity [73].

8.2.1 Temperature response

In CMOS processes, the mismatch between the output current of identically biased transistors is given by (8.1). For high performance DACs, the main current source transistor is usually much larger than the feature size of modern CMOS processes. Thus, the current mismatch is dominated by the threshold voltage mismatch. This assumption is confirmed by measurements of an existing DAC implementation [7]. Figure 8.3 shows the standard deviation of the output current of the 15 unary current cells. The mismatch clearly exhibits a square root dependence on the drain current, which is in conformance with (8.1) in combination with the drain current relationship of a MOS transistor in saturation, as shown by (8.2).

$$I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 \tag{8.2}$$

At high temperatures, the mobility of the carriers (μ) decreases. Usually, a temperature independent current controls the output current of the DAC current source transistors. Therefore, at high temperatures, $V_{GS} - V_T$ increases to compensate for the decreasing μ. Together with the matching equation of (8.1), it is clear that when the temperature increases, i.e. $V_{GS} - V_T$ increases, the relative threshold mismatch decreases. Mismatch measurements of the existing DAC at high temperature confirm this analysis, see Figure 8.3.

In the discussed conventional CUE, the mismatch of a main current source is compensated by the nominal value of the CalDAC output current, i.e. $I_{cue,n} = \bar{I}_{main} + I_{error,n} + I_{cor,n}$. $\bar{I}_{main}$ and $I_{cor,n}$ are set by temperature independent references, while $I_{error,n}$ is temperature dependent. Therefore, the temperature coefficient of $I_{cue,n}$ depends on the ratio between $I_{cue,n}$ and $I_{error,n}$. Figure 8.4 shows the buildup of the output current of two exemplary CUEs. The CUEs are calibrated at $T = 25°\text{C}$, but for $T \neq 25°\text{C}$, the CalDAC calibration is not valid.

To quantify the temperature dependence, a simple transistor level simulation based on [76] is performed. Two calibrated CUEs with threshold

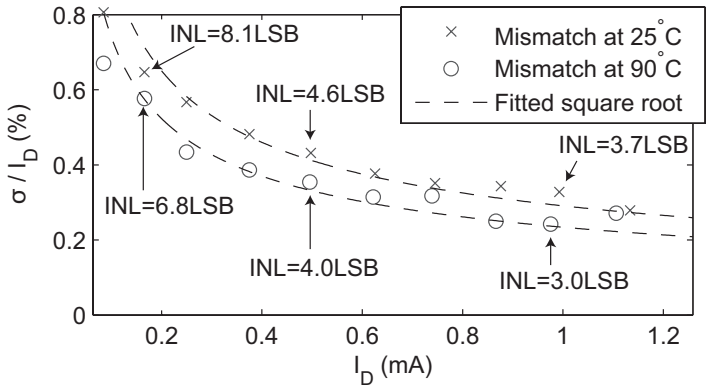


Figure 8.3: For an existing DAC current cell array, increasing the bias current and hence the output current improves the output current standard deviation. More importantly, the output current matching improves for higher temperature.

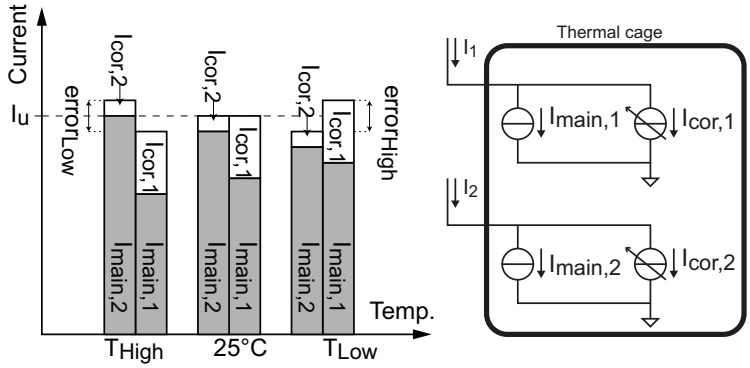


Figure 8.4: Output current temperature dependence of two CUEs

voltage mismatch between each other are simulated over a temperature range of $-50°C$ to $125°C$. The temperature dependence of the CUEs output current difference, i.e. $error_{Low} - error_{High}$, can be as large as 8 CalDAC LSBs, which is 1.3% of the CUE output current.

Thus, for foreground calibration, the INL degrades and also the SFDR worsens when temperature changes. This phenomenon is confirmed by INL and SFDR measurements of an existing DAC [7].

8.2.2 Disturbance response

Next to the temperature dependence of the calibration, the CUEs exhibit a calibration dependent disturbance response. It can easily be argued that two

CUEs with different ratios between main current and CalDAC current have different responses to a disturbance on the gate node of the CalDAC current sources. This also holds for disturbances on other nodes of the CUEs. For an exemplary DAC, implemented in a CMOS 65nm process, with two current cells with different correction currents and a disturbance at V_{bcal} of Figure 8.2, the difference in the output current response of the two current cells is shown by the top waveform of Figure 8.5. The cell dependent response difference of more than 50% will certainly introduce input code dependent behavior, which results in spurious components, significantly reducing the SFDR.

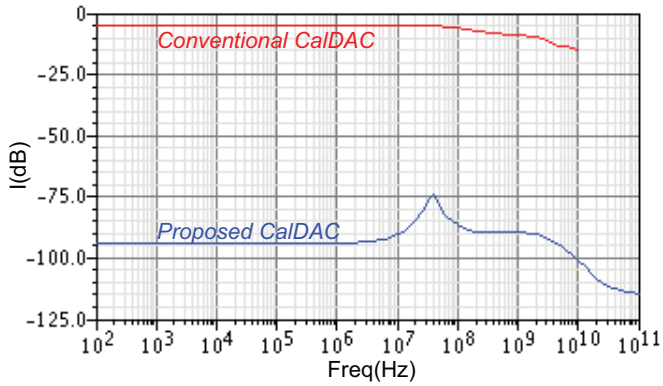


Figure 8.5: Difference in response of two current cells with different calibrated mismatch for both the conventional CalDAC and the new proposed CalDAC

8.3 Proposed new calibration method

To match the response of the correction hardware to temperature and on-chip disturbances, and hence extend the advantages of the foreground calibration, a new calibration method is proposed [86, 87]. A chip implementation of this method is later published in [78].

In the proposed CUE, the same number of unit transistors (M) is used in every CUE. These M transistors are divided in two groups, $M - K$ unit transistors in the fixed group and K unit transistors in the configurable group. The K unit transistors in the configurable group can be interchanged with X additional redundant unit transistors, such that the mismatch of the configurable group transistors compensates the mismatch of the fixed group. The two groups together generate the desired output current.

A novel principle is the use of identical unit transistors for both the fixed group and the configurable group, sharing a common bias voltage, providing

a matched response for every CUE in the DAC. Another novel concept is to compensate the mismatch of the fixed group of transistors in the current cell with the mismatch of the configurable group transistors, generating a temperature stable calibration.

8.3.1 Hardware

A schematic overview of the new CalDAC implementation is shown in Figure 8.6. The $M - K$ main current source transistors provide the fixed current I_{main}. K units in the group of P unit transistors in the CalDAC are switched on to generate the correction current I_{cor}. The value of X defines the added amount of redundant current sources with respect to the M-transistor intrinsic current cell. The value of P is an indication of the added layout complexity, since every transistor in the CalDAC is controlled separately.

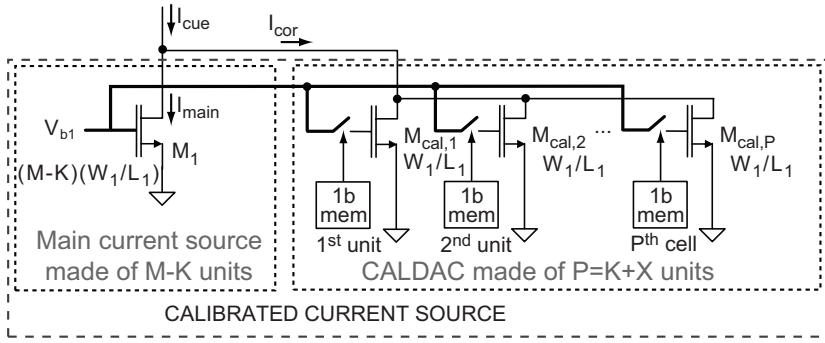


Figure 8.6: Proposed Caldac with common transistor dimensions and biasing

8.3.2 Algorithm

The algorithm to find the optimal correction for a current source is explained using a segmented DAC architecture, of which the Least Significant Bits (LSBs) are implemented using binary current cells and the Most Significant Bits (MSBs) are implemented with unary coded current cells. Note that the described method can also be applied to a fully unary or binary coded DAC. Two different calibration methods are used for the unary current cells and the binary current cells, which are described separately.

8.3.2.1 Unary current cells

The principle of the calibrating algorithm of one CUE is to select which transistors of the CalDAC should be switched on such that I_{cue} is properly corrected. The first step in the algorithm is to sort the transistors in the CalDAC according to their output amplitude and then switch on K of the highest amplitude transistors. Figure 8.7 gives an example, where $M = 8$, $K = 3$ and $X = 3$. The top figure shows the output amplitude of the unit transistors (which are named a-k), and gives the first step.

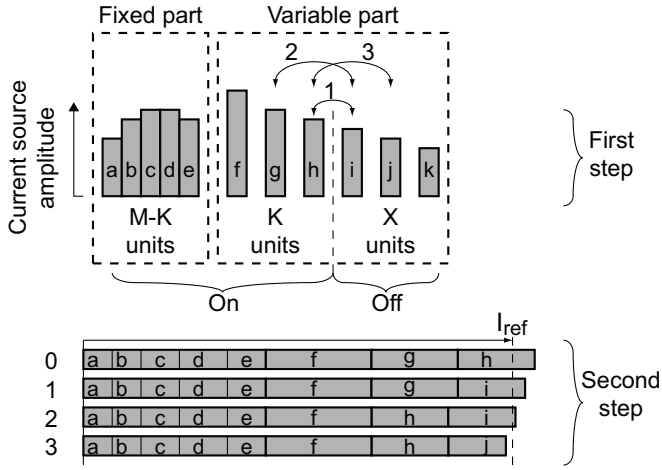


Figure 8.7: Example of the calibration algorithm

The second step in the algorithm is to swap transistors between the on-group and the off-group until the total output current becomes less than the reference. The top diagram of Figure 8.7 indicates the first three swap actions (named 1-3). The bottom diagram gives the resulting total output current of the CUE for the initial state (named 0) and after each swap action. The algorithm will stop after swap step 3, because the total output current is less than the reference I_{ref}.

For the calibration of the unary current cells, the reference consists of the sum of all binary current cells and one LSB current source as in [77]. Therefore, the binary current cells should be calibrated before the unary current cell calibration. The main hardware component necessary to implement the algorithm for the unary current cells is a comparator to sort the transistors and compare the reference and the CUE total output current. The algorithm can be realized as a simple Finite State Machine (FSM).

8.3.2.2 Binary current cells

The algorithm to calibrate the binary current cells is largely identical to the algorithm for the unary current cells. For the calibration of N_{lsb} binary current cells in one DAC, N_{lsb} reference currents are required, with a ratio of 2 between two successive references. Since exact current ratios are difficult to implement in the analog domain, the complete binary calibration algorithm is implemented in the digital domain. Therefore, all unit transistor currents are measured using an Analog to Digital Converter (ADC), and all transistor sorting, swapping and output current calculation can be done digitally. To be insensitive to gain and offset errors of the ADC, the main current source of the binary current cells is omitted ($M - K = 0$). Instead, the current cell output current is constructed using the separately measured unit transistors of the CalDAC. The algorithm is insensitive to the ADC offset and gain error since all unit transistors share the same ADC errors with equal relative importance.

For the binary calibration, the simple comparator check in the unary current cell calibration is replaced by a check if the difference between the reference and the total output current is minimal. The reference for the binary calibration is generated by separately measuring all CalDAC transistors of the complete DAC with the ADC, computing the average and multiplying by the corresponding power of two.

The necessary hardware to implement the binary current cell calibration is the ADC and a FSM. The ADC does not need to be fast or accurate and is implemented as a Successive Approximation (SAR) ADC [76, 77] with 5 bits linearity. The additional area for the ADC and the FSM is negligible compared to the area of the current source array.

8.4 Simulation results

The effectiveness of the proposed calibration method is validated with simulations of the INL improvement, temperature response and disturbance response.

8.4.1 Algorithm

The presented new calibration algorithm is validated using a Matlab model of a 6+6 (unary + binary) bits segmented DAC. All current cells are based on the same unit transistor. The LSB current cell consists of 1 transistor, the next current cell of 2 transistors, etc. Thus, the unary current cell has a weight of 2^{Nlsb} LSB, and hence consists of $M = 64$ transistors.

There is a trade-off between the additional hardware and hardware complexity in the choice for K and X. The achieved improvement between the intrinsic INL and the calibrated INL depends on K and X. Monte Carlo simulations of 1200 DACs per one simulation point are executed to investigate the effects of using different values for K and X on the 99% yield INL.

First, these simulation show that with a fixed number of CalDAC transistors (P), the highest improvement of INL is achieved when $K = X$, since then the number of possible combinations is maximized. For different values of K, X and unit transistor matching, the 99% yield INL values, with respect to 12 bits accuracy, are shown in Figure 8.8. It is clear that using more transistors in the CalDAC results in more possibilities for the algorithm and hence higher improvement when applying the calibration method. It is also observed that the improvement between the intrinsic INL and the calibrated INL is constant when the values of K and X are fixed.

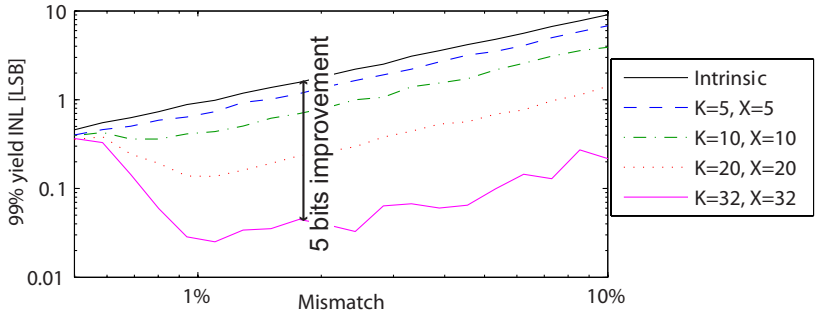


Figure 8.8: Matlab simulations showing the matching- and configuration-dependent 99% yield INL of the new calibration method

When for the exemplary 6+6bits DAC, 12 bit linearity is required and 99% yield for the INL specification, the combination of 3% unit transistor matching and a CalDAC with $K = X = 20$ results in an improvement of static linearity from 9.4 bits to 12.2 bits, while only increasing the current source area with approximately 30%.

8.4.2 Temperature response

To investigate the temperature coefficient of the proposed calibration method, the same transistor level simulation of Section 8.2 has been performed. After calibration, the temperature dependence of the difference between the two currents is less than 0.001% of the total output current

over the complete temperature range, which is 1000 times lower than the conventional CalDAC calibration. Thus, the proposed calibration principle results in a temperature stable calibration.

8.4.3 Disturbance response

The same number of transistors is switched on in every CUE. Therefore, every CUE has approximately the same response to disturbances, independent of the correction current. This indicates that the calibration advantages are also present at high speeds. For a disturbance at the gate node of the current source transistors (V_{b1} in Figure 8.6), the difference in output response of the two exemplary CUEs is shown as the bottom waveform in Figure 8.5. Over the complete frequency band, the difference in response between the two CUEs is less than -70dB. Since the response difference is magnitudes lower than the conventional CalDAC, it is expected that the spurious components due to on-chip disturbances are significantly reduced.

8.5 Conclusion

The proposed novel calibration method overcomes the problems with the cell-dependent temperature coefficients of the Calibrated Unit Elements. Also the cell-dependent response to disturbances is reduced. Due to the reduction of these two cell-dependent responses, the spectral purity of the DAC output signal is expected to improve.

The new calibration algorithm provides opportunities to improve the post calibration INL of a DAC. For an exemplary 6+6bits segmented current steering DAC, the expected 99% yield INL improves with almost 3 bits when using only 30% additional current cell area. The proposed new calibration method will obliviate the need for background calibration, while also providing calibration advantages to high DAC speeds.

9 | Segmentation

The segmentation trade-off of many current-steering DACs is based on the segmentation approach of [66]. This trade-off is based on the INL/DNL characteristics of the converter. However, for high speed DACs and Mixing-DACs, also the dynamic characteristics of the converter influence the segmentation trade-off. This chapter discusses these dynamic characteristics and proposes a new approach to the segmentation trade-off.

This chapter is based on part of a paper published at the IEEE ISCAS 2014 conference[83].

9.1 Introduction

Current Steering (CS) Mixing-DACs predominantly use a segmented implementation, with a unary scaled MSB part and a binary scaled LSB part. A CS Mixing-DAC with local mixing[85] can be very linear if the responses of all 1-bit switched current sources (current cells) are uncorrelated and identical, or ideally scaled for binary current cells.

For multicarrier transmitters, the power of a single carrier is much lower than the total full scale output power. This significantly increases the importance of the responses of the binary (LSB) current cells and alters the segmentation trade-off. As discussed before, amplitude errors are extensively discussed in open literature. In this chapter, the timing error of the binary part and its impact on the performance are discussed. In the binary part, systematic timing errors are dominant over random timing errors. The systematic binary timing errors are discussed in this chapter.

Section 9.2 introduces the concept of output power back-off and its impact on the spectral purity. In Section 9.3, the importance of matching of the binary LSB part of a Mixing-DAC is discussed. The consequences of these two subjects for the segmentation trade-off are discussed in Section 9.4.

9.2 Output power back-off

One of the characteristics of a multicarrier transmitter is that the power of each single carrier is lower than the full scale signal, which is called back-off (typically around -16dB$_{FS}$/tone). In such a transmitter, the signal of one tone only uses a small subset of the unary current cells, effectively changing the segmentation of the Mixing-DAC. Hence, the binary part of a segmented Mixing-DAC becomes increasingly important. Figure 9.1 shows the spectra of a full-scale dual-tone signal at -6dB$_{FS}$/tone, and a signal at -16dB$_{FS}$/tone (10dB back-off). While the difference in signal power is 10dB, the spur-floor is at the same absolute level, reducing the SFDR. The cause of this high spur-floor is systematic timing errors between the binary current cells.

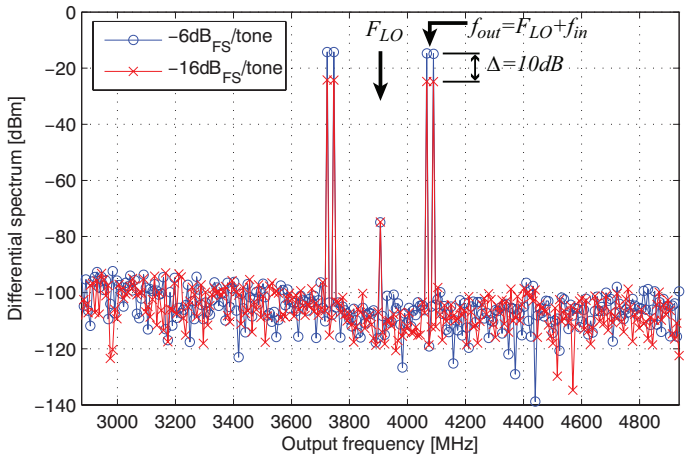


Figure 9.1: Spectral compariston between full-scale output and back-off

9.3 Binary matching

In a traditional DAC output stage, only one critical high-speed node should be rigorously optimized for binary scalability: the source of the output cascodes. In the chosen Mixing-DAC architecture of Figure 9.2, two sets of high-speed nodes need precise optimization: the source of the output cascodes (nodes A and A') and the source of the mixer (nodes B and B'). The response of these nodes should be exactly scaled with respect to the unary current cell. To guarantee this binary matching, the capacitance values and the gain of the transistors at these nodes should scale exactly with the binary current cell scaling.

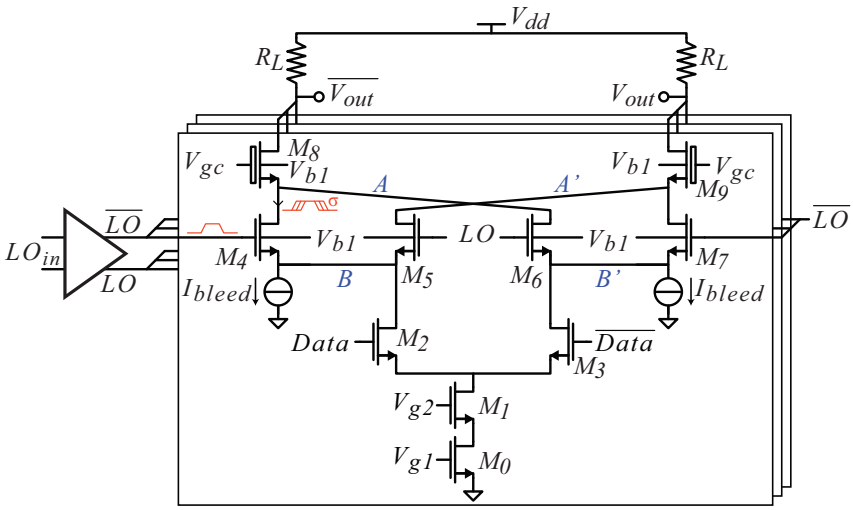


Figure 9.2: Chosen Mixing-DAC architecture with annotated timing errors: output stage mixing with a single global LO driver

To illustrate the sensitivity of the performance to capacitance deviations in the binary current cells, Figure 9.3 shows the SFDR_{RB} as a function of the parasitic capacitance at the source of the output cascodes (A and A') of the three most significant binary cells (B9, B8 and B7) in the LSB part of the exemplary Mixing-DAC. The pre-annotated capacitance in the schematic model of the current cells is altered. The x-axis is in % deviation of the ideally scaled value to ease the comparison between the various binary cells. The ideal value at 0% is the exactly binary scaled capacitance: the 6fF in the unary cell results in 3fF for B9, 1.5fF for B8, etc.

Figure 9.3 clearly demonstrates the low robustness of the spectral purity to the capacitance value. A change of 4% in the capacitance value in B9 results is a SFDR_{RB} degradation of 9dB to 83dBc, which is worse than the required 85dBc.

Figure 9.3 also shows a relationship between the capacitance robustness and the binary cell index. The B9 cell has the lowest robustness: ±3% for 85dBc. The subsequent binary cells have a doubled robustness for each index decrement: B8=±6%, B7=±12%. Even though the actual robustness numbers may only be valid for the exemplary Mixing-DAC implementation, the robustness trend is valid for all CS (Mixing-)DACs. The robustness of an implementation is limited, which also limits the maximum SFDR_{RBw}hen the segmentation is fixed.

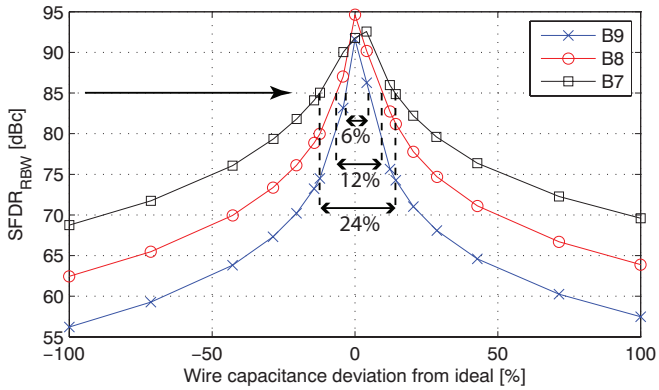


Figure 9.3: SFDR dependence on the parasitic capacitance at the output cascode source node of B9, B8 and B7

9.4 Segmentation

A novel, back-off aware segmentation trade-off is proposed in Figure 9.4(a), in analogy to the segmentation trade-off figures in [66]. A larger unary MSB part improves the $SFDR_{RB}$, but a lower output power reduces the $SFDR_{RB}$. The segmentation trade-off of the exemplary Mixing-DAC is shown in Figure 9.4(b). The proposed segmentation (6b unary, 10b binary) is design point α, where $SFDR_{RB}$=86dBc at -16dB_{FS}/tone. If the back-off requirement increases to -22dB_{FS}/tone, the $SFDR_{RB}$=80dBc (design point β). If the $SFDR_{RB}$ of 86dBc value should be maintained at -22dB_{FS}/tone back-off, the segmentation should be changed to one more unary bit, which is design point γ. This illustrates the trade-off between $SFDR_{RB}$, segmentation and output power back-off. Naturally, changing the segmentation has numerous other implications, e.g. on layout area or maximum signal frequency.

The simulated performance of the exemplary Mixing-DAC segmentation at -16dB_{FS}/tone (10dB back-off) of $SFDR_{RB}$=86dBc is sufficient for the required 85dBc, hence the chosen segmentation is optimal.

9.5 Conclusion

Timing errors are an important consideration in high speed highly linear Mixing-DAC architectures. For multicarrier transmitters, output power back-off is often used. With back-off, the matching of parasitic capacitances at the high-speed nodes in the binary current cells is crucial for achieving a high $SFDR_{RB}$. The proposed segmentation trade-off shows that for every 6dB of additionally required back-off, one extra unary bit is needed.

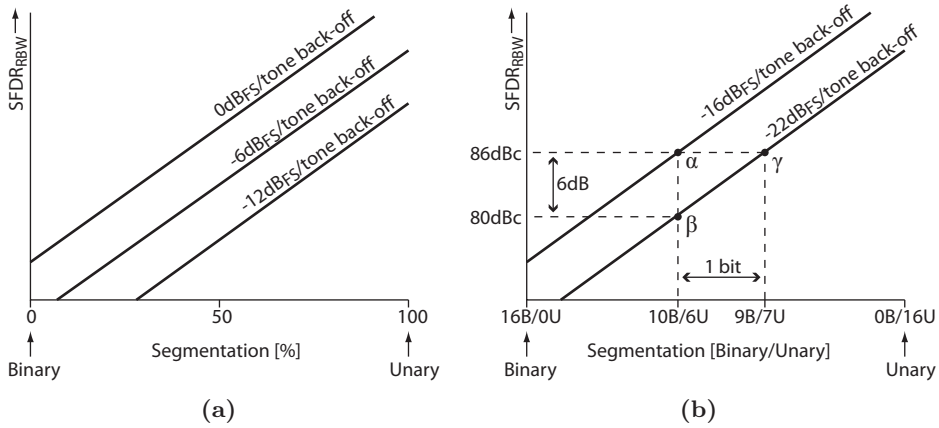


Figure 9.4: Segmentation trade-off based on $SFDR_{RB}$ and back-off, showing both the trend (a) and quantitative results for an exemplary Mixing-DAC (b)

The proposed method leads to an optimal segmentation for the chosen Mixing-DAC architecture tailored toward the high spectral purity and high frequency requirements of multicarrier GSM transmitters. The simulated performance of this architecture is $SFDR_{RB}$=86dBc at f_{out}=4GHz and -16dB_{FS}/tone output power (10dB back-off).

10 | Optimal architecture

Chapter 4 discusses three promising architectures. Chapter 5-9 addresses the differences between those architectures. This chapter summarizes the conclusions of that analysis and proposes the most optimal architecture. Based on the linearity of the three architectures, both in the nominal case and with mismatch, it is concluded that cascoded local mixing is the most optimal architecture. The implementation of this architecture as a test chip is discussed in Chapter 11.

10.1 Classification

The classification (see Chapter 3) identifies the most optimal characteristics for a high spectral purity GHz frequencies Mixing-DAC: current-steering principle, Cartesian signaling, square-wave mixing, symmetric around zero signaling for the LO and data signal, fully differential and LO-gate transistor usage. The classification identifies two architectural choices which need quantitative analysis: Mixing locality and sequence of operations. Combining these architectural choices results in three promising Mixing-DAC architectures: cascoded global mixing, cascoded local mixing and digital mixing.

10.2 Quantitative architecture analysis

Chapter 5 shows that cascoded local mixing achieves a higher linearity than global mixing with the use of a local output cascode. Chapter 6 shows that cascoded local mixing exhibits much lower timing-error sensitivity than digital mixing. These conclusions are summarized in Table 10.1 by comparing the $\mathrm{SFDR_{RB}}$ values of all three promising architectures. For these simulations, the frequency values are: f_{LO}=3.92GHz, F_S=1.96GHz, f_{in}=150MHz & 165MHz. For the mismatch simulations, only the relevant

components have mismatch. Mismatch that is corrected with calibration is not taken into account.

Table 10.1: Comparison of a selection of Mixing-DAC architectures

Sequence	**Locality**	**Figure**	**$SFDR_{RB}$**	
			Nominal	90% yield
Cascoded	Global	3.4	75dBc	75dBc
	Local	3.5	88dBc	85dBc
Mixing → DAC		3.10	84dBc	66dBc

It can seen that cascoded operations together with local mixing achieves the best spectral purity, both in the nominal case and the mismatch case.

Chapter 7 shows that using an output transformer instead of a local output cascode is feasible. However, the resulting power consumption is much higher than when using an output cascode. Since the output cascode also achieves the desired linearity, no output transformer is used.

Based on the classification of Mixing-DAC architectures and the aforementioned quantitative analysis, a strong candidate Mixing-DAC architecture for high spectral purity can be synthesized. The basic characteristics of the architecture are as follows: Cartesian signaling, 1-bit SaZ LO mixer input (square-wave LO signal), 1-bit SaZ BB mixer input (local mixing), fully differential signaling, cascoded mixing and D/A conversion, LO mixing signal at transistor gate.

The choice for SaZ LO mixer input over RZ LO mixer input is influenced by the features of the baseline DAC of the industry partners, see Section 11.1. This DAC core contains a method to reduce the effect of BB timing errors, which eliminates the advantage of using RZ LO signal, see Section 3.4.1.2. Since this calibration method also calibrates the amplitude mismatch of the current source, the calibration method of Chapter 8 is not used.

10.3 Segmentation

The segmentation of the baseline DAC of the industry partner is used for the implementation of the proposed Mixing-DAC architecture. The resolution is 16 bit, segmented in 6 MSB unary bits and 10 LSB binary bits. This segmentation results on the one hand in a nominal SFDR which is just over the required 85dBc. On the other hand, the capacitance of the output tree is such that the output power at the target maximum frequency of 4GHz

is reduced with approximately 5dB, which is significant. However, changing the segmentation to less MSB bits will result in a worse SFDR which is not desired.

10.4 Expected performance of final architecture

A mixing-DAC architecture incorporating all above mentioned characteristics is shown in Figure 3.5. A typical output spectrum of the implementation of this architecture is shown in Figure 10.1 and Figure 10.2. For this simulation, the frequency values are: f_{LO}=3.92GHz, F_S=1.96GHz, f_{in}=150 & 165MHz. In this random mismatched simulation, the IMD3 is -86dBc and the SFDR_{RB} in a reduced bandwidth of 300MHz is -85dBc.

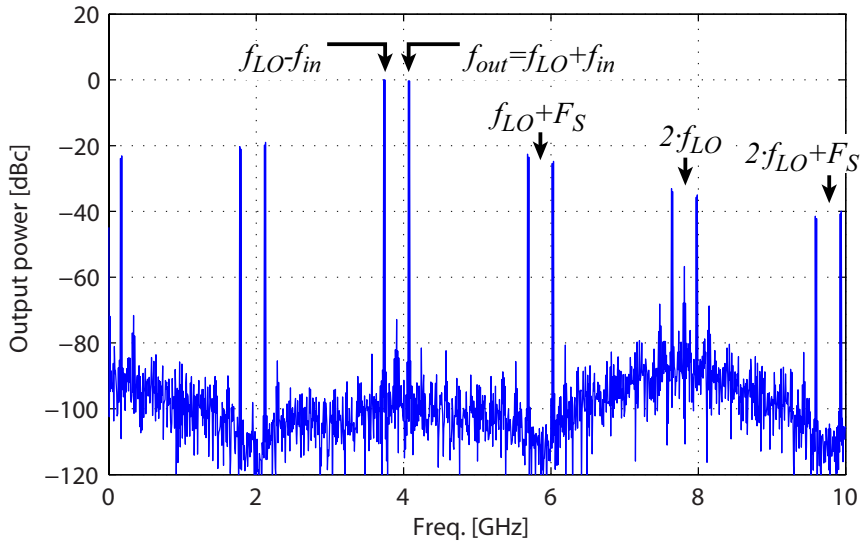


Figure 10.1: Exemplary Mixing-DAC output spectrum

10.5 Conclusion

The classification leads to a number of promising Mixing-DAC architectures for high spectral purity at GHz frequencies. Quantitative analysis of these promising architectures leads to the synthesis of the most optimal architecture. The characteristics of this architecture are: Cartesian signaling, 1-bit SaZ LO mixer input (square-wave LO signal), 1-bit SaZ BB mixer input (local mixing), fully differential signaling, cascoded mixing and D/A conversion, LO mixing signal at transistor gate.

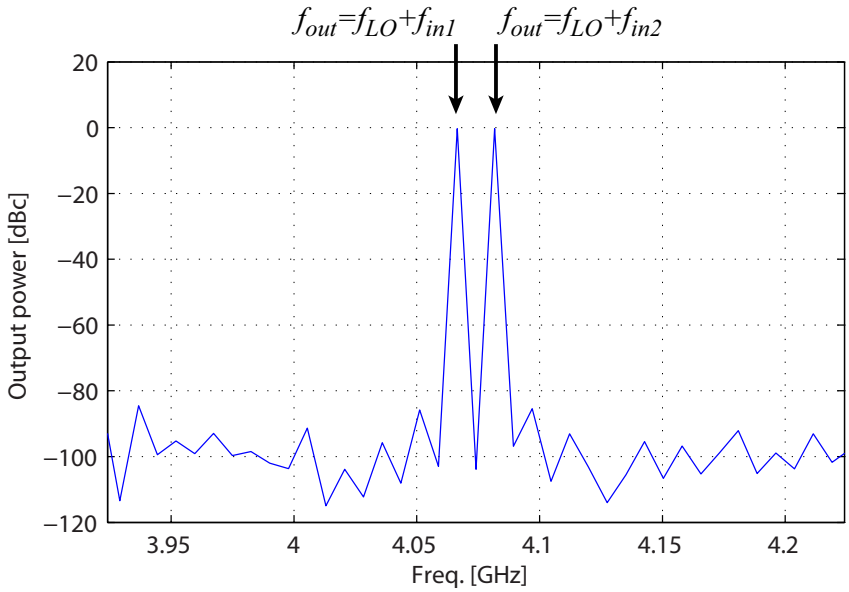


Figure 10.2: Exemplary Mixing-DAC output spectrum

11 | Design of a highly linear wide-band Mixing-DAC

In the previous chapter the most optimal Mixing-DAC architecture for high spectral purity is proposed. To validate this architecture, it is implemented in 65nm CMOS. Various aspects of the design are discussed in this chapter, together with main performance limitations. The discussed circuits are: output stage, LO driver, data path and elevated bulk generation. This chapter also presents the simulation results of this architecture. Measurement results of this design are presented in Chapter 12.

This chapter contains parts of a paper submitted to the IEEE ISSCC conference [81].

11.1 Introduction

To validate the proposed architecture, a 16 bit 2GSps 4GHz Mixing-DAC is designed. The used process technology is a triple-well 65nm CMOS with 1.2V and 3.3V supplies. IP blocks of a baseline DAC are provided by the industry partner. These IP blocks include: the digital signal processing, the data path including the data drivers, the chip outline including IO ring and ESD devices, the biasing, the current source array, and the calibration circuitry. Large amount of alterations needed to be made to add the circuitry for changing the function to a Mixing-DAC.

One of the most important features which are used, is the sort-and-combine calibration algorithm to calibrate the timing errors of the data path and the amplitude errors of the current source array, see Section 11.2 and Section 12.2.3. The maximum sample rate of the baseline DAC is more than 2GSps, hence this is also the target of the Mixing-DAC. For generating an

output signal up to 4GHz, a maximum LO frequency of 4GHz is chosen. Since the case of F_S=2GSps and f_{LO}=4GHz is the most challenging case, this configuration is used in most of the simulations. The frequency of the baseband input signal is around 150 MHz since in that case any LO leakage falls outside the RB with a bandwidth of 300MHz. The typical full-scale output current is 20mA, terminated in 50Ω differential load.

In Section 11.2, the various elements of the architecture are introduced. The main elements are: output stage, LO driver, elevated bulk generation and data path. These elements are discussed in Section 11.3 to Section 11.6 respectively. Section 11.7 presents the high level simulation results of the Mixing-DAC.

11.2 Architecture

An overview of the architecture is shown in Figure 11.1. The chip consists of two independent Mixing-DACs which can also be used in an I/Q configuration. These two Mixing-DACs are designated Mixing-DAC A and Mixing-DAC B. The schematics of the two Mixing-DACs are identical and there are no significant differences between the layouts. Unless stated otherwise, Mixing-DAC A is discussed.

The 16 bit converter is segmented into a 6 bit unary part and a 10 bit binary part. The data decoding for the 63 unary current cells is done by a programmable decoder, which is also used for calibration similar to [3]. The sort-and-combine algorithm calibrates the static mismatch of the current sources and timing mismatch of the data switching in the switched current cells of the output stage. Besides the minimum required 63 unary current cells, there are a number of redundant current cells. These redundant current cells are used for outlier elimination in the calibration algorithm. The current cells with the most deviating behavior are disabled during normal operation.

The performance of the Mixing-DAC is mainly determined by the output stage. The output stage generates the output current, and is discussed in Section 11.3. The LO signal is generated by the LO driver from the external LO_{in} signal. This driver is required to have a low output impedance since it needs to drive the LO distribution tree and the gate capacitance of the mixer transistors. The LO driver is discussed in Section 11.4.

The triple-well process technology enables using a separate bulk voltage if desired. An elevated bulk voltage is used for a number of transistors in the output stage, in order to raise the absolute operating voltages of these transistors. The generation of this elevated bulk voltage is discussed in Section 11.5.

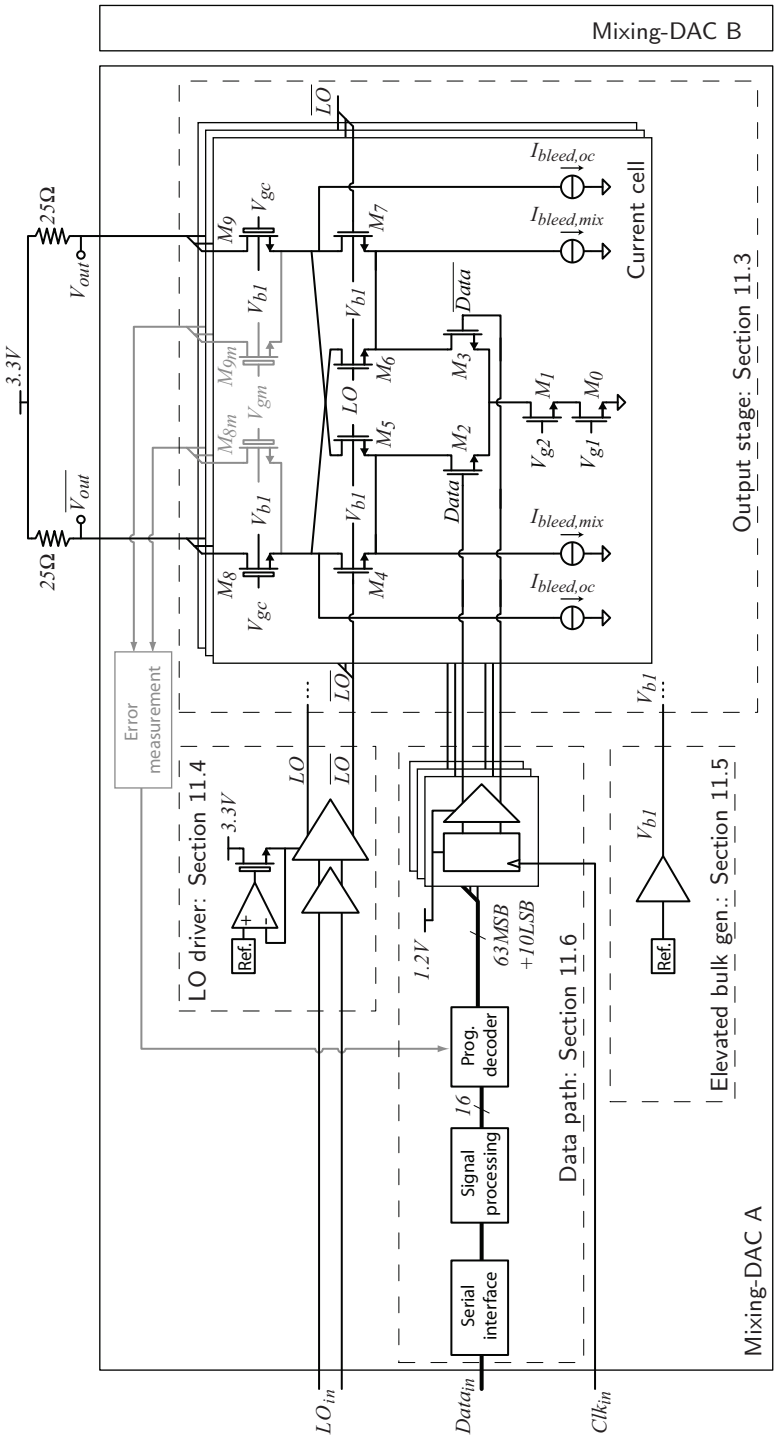


Figure 11.1: Overview of Mixing-DAC system

The baseband data is provided externally by the $Data_{in}$ signal. After processing, the signal is decoded to the segmented coding of the output stage. Latches and drivers synchronize the signal and amplify it to the desired amplitude. This data path is discussed in Section 11.6.

11.3 Output stage

An overview of the output stage is shown in Figure 11.2. Both the schematic (see Section 11.3.1) and layout (see Section 11.3.2) of the output stage are important for achieving high performance.

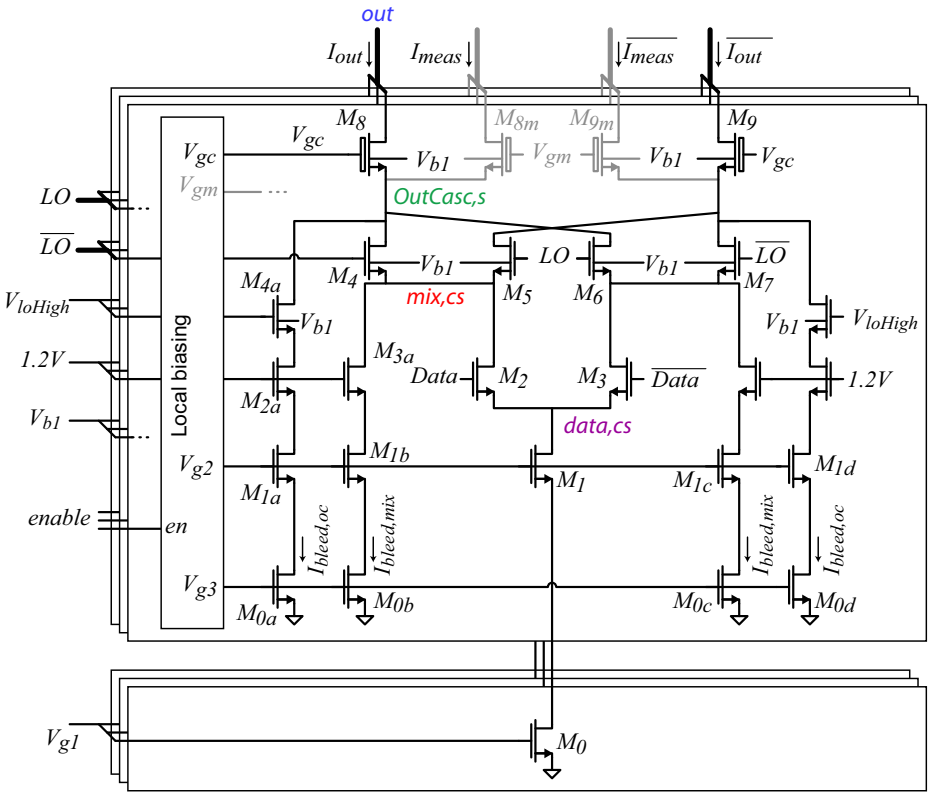


Figure 11.2: Schematic of output stage

11.3.1 Schematic

A current cell contains a cascoded current source (M_0, M_1), baseband data switches (M_2, M_3), mixer switches (M_4-M_7) and output cascodes (M_8, M_9).

The array of current sources is drawn separately from the other part of the current cell to indicate that there is a relatively large spacing between those two parts in layout while the current sources themselves are close together. The measurement probes (M_{8m}, M_{9m}) for the error measurement of the calibration can individually connect each current cell to the measurement circuit during calibration. The bleed currents have cascoding at the same levels as the path of the main signal current. This is to ensure a maximum output impedance, to protect the thin-oxide devices and to minimize parasitic capacitances at the sensitive nodes $OutCasc, s$ and mix, cs.

Besides the cascode transistors M_1,M_8-M_9, the switching transistors (data switches M_2-M_3 and mixing transistors M_4-M_7) also act as cascodes. This multi-level cascoding strategy ensures that each function of the current cell is isolated from the other functions. Some state-of-the-art Mixing-DACs combine multiple functions in one transistor, which hampers the separate optimization of each function. Examples of combining functions are: use the current source transistor also as mixer[5, 10, 11, 13, 13], use the current source also as Data switch [29], or combine the function of the Data and LO switch [79]. The separate transistor level per function of the proposed architecture enables the precise optimization of the implementation of each function. Additional cascoding (M_1,M_8,M_9) and bleed currents are used to protect the most sensitive nodes and increase the output impedance.

11.3.1.1 Output cascode

The output cascode (M_8,M_9 in Figure 11.2) isolates the sensitive internal nodes of the output stage from the large output voltage swing. At the output cascode, three error-sources introduce non-linear distortion:

- non-linear drain impedance,
- switching of the drain impedance,
- settling of the source node.

The non-linear drain-impedance mainly comes from the gate-source and gate-drain capacitance (C_{gs} and C_{gd}), which both originate from the channel of the output cascode. The magnitude of this non-linear distortion depends on the size of the capacitances and on the non-linearity of the capacitance.

The non-linearity of these two capacitances strongly depends on the output common-mode voltage, given a fixed gate voltage V_{gc}. This dependence is illustrated in Figure 11.3, where V_{out_cm} is the common-mode output voltage. The shape of the waveform is different than discussed in Section 5.2.1, since that section discusses a thin-oxide transistor while the final output cascode, discussed in this section, is implemented using a thick-oxide transistor. The

drain voltage, which is the Mixing-DAC output voltage, determines the shape of the channel in the output cascode, and thereby the non-linearity introduced by the channel modulation. For low V_{out_cm}, the output cascode is in the linear region where C_{gs} and C_{gd} are both connected to the output through a low resistance. Hence, they both fully contribute to the non-linearity. When V_{out_cm} is increased, the output cascode transistor is more in saturation, C_{gs} counts less and the non-linearity is less. The optimum (at 2.8V for the example of Figure 11.3) is due to partial cancellation of the non-linearity of the two capacitances. This cancellation effect is very stable and is present in all simulations. Hence, V_{gc} is chosen such that the output voltage is in this optimal region.

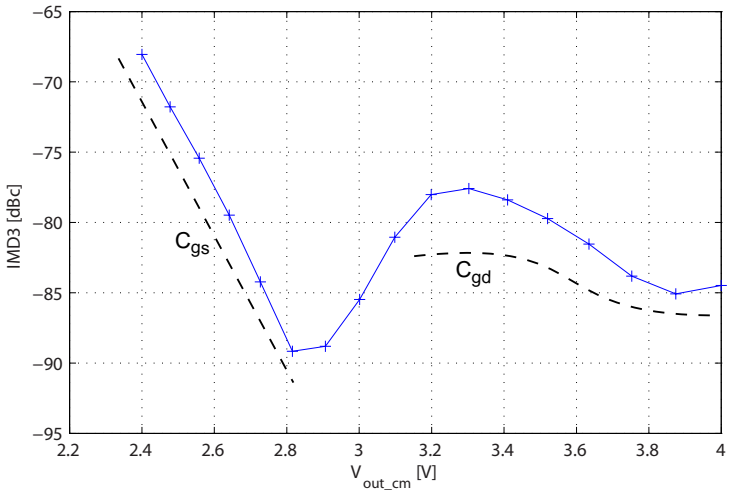


Figure 11.3: Linearity dependence on the output common-mode voltage

The size of the capacitance is minimized by reducing the area of the transistor. The width/length ratio of the output cascode (W_{oc}/L_{oc}) is minimized while respecting the mixer voltage headroom required for saturation. At a given W_{oc}/L_{oc} ratio, the area is minimized by minimizing L_{oc}. However, reducing L_{oc} increases the non-linearity of the C_{gs} and C_{gd} capacitance values. Hence, there is an optimal value of L_{oc}, which is demonstrated in Figure 11.4.

The second non-linearity is generated due to the switching of the output cascode, which generates a data-dependent output capacitance [65]. This capacitance again depends on the C_{gs} and C_{gd} capacitances. The difference of the capacitance values between the on- and off-state can be reduced by

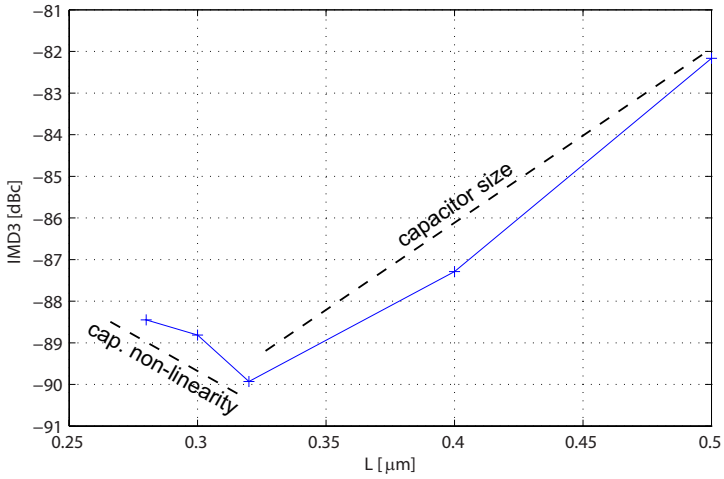


Figure 11.4: Linearity dependence on the length of output cascode

adding bleed currents. The total bleed current through the output cascode is the sum of the bleed current through the mixer ($I_{bleed,mix}$) and the additional bleed current ($I_{bleed,oc}$):

$$I_{cascBias} = I_{bleed,mix} + I_{bleed,oc}. \tag{11.1}$$

The third error source which generates non-linear distortion is the settling of the source nodes of the output cascode ($OutCasc, s$ node in Figure 11.2). Incomplete settling causes inter-symbol-interference (ISI) for transitions of the *Data* signal, which causes non-linear distortion. Incomplete settling after *LO* signal transitions do not cause ISI since the *LO* signal switches in each current cell, and hence there is no cell-dependent behavior which can cause non-linear distortion. The ISI due to incomplete settling at the *Data* transitions can also be reduced by increasing $I_{cascBias}$. The dependence of the IMD3 value on $I_{cascBias}$ is shown in Figure 11.5. In this simulation, the width of the output cascode transistors linearly depends on the maximum current through the output cascode to keep the occupied voltage headroom constant. For low values of $I_{cascBias}$, increasing $I_{cascBias}$ improves the IMD3 value since the ISI effect is reduced. However, when $I_{cascBias}$ is too high, the transistor size of the output cascode has to increase significantly, increasing the impact of the non-linear drain impedance and thereby increasing the non-linear distortion. The optimum depends on the value of the parasitic capacitance of the output cascode source node $C_{OutCasc,s}$. For this design, the optimal $I_{cascBias}$ is between 10µA and 100µA for $C_{OutCasc,s}$=5fF.

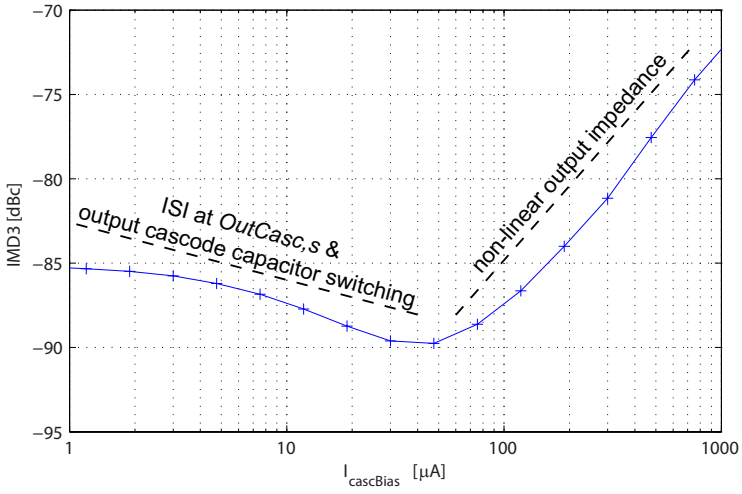


Figure 11.5: Linearity dependence on the total bleed current through the output cascode

The output cascode also acts as a selection switch. Together with another set of transistors (M_{8m},M_{9m}), the output cascode selects the output tree or the measurement tree as the output network for the current cell.

11.3.1.2 Mixer

The mixer operates at the LO frequency and hence its parasitic capacitances are critical. Therefore, ideally the mixer should be implemented using thin-oxide devices. This would result in a challenge to fit 4 cascoded transistors in a voltage headroom of only 1.2V, which is the maximum voltage for thin-oxide devices without reducing the reliability. Decreasing the voltage headroom for each level of transistors requires the W/L ratio of the transistors to be larger which increases the size of the parasitic capacitances. Larger parasitic capacitances result in lower switching speed for the switches and larger non-linearity. The lower voltage headroom also results in more mismatch for the current-source transistor which also reduces the linearity.

The state-of-the-art Mixing-DAC architectures solve the voltage-headroom problem by reducing the number of stacked transistors. This is done by combining multiple functions in one transistor level, which hampers the separate optimization of the implementation of each function leading to a reduction in the performance, as discussed in Section 11.3.1. Another solution is to omit cascoding of the current source [18–20, 22], which results in a decrease in the performance. A third solution is to apply a negate bulk voltage

to the current source and its cascode [79], which requires a negative supply voltage. Using a thick-oxide transistor as mixer is also a solution, but this results in a lower switching frequency or a higher power consumption. Hence, these solutions are not practical or result in inferior performance.

The proposed architecture uses a solution which does not have the aforementioned disadvantages. Utilizing the triple-well technology, the operating voltages of the mixer are shifted. The bulk voltage of the mixer transistor is elevated by approximately 0.6V. If the absolute voltages of the terminals of the mixer transistor are between 0.6V and 1.8V, the relative voltages between the mixer terminals are lower than 1.2V and the reliability is not compromised. The total available voltage headroom for the thin-oxide transistors is increased to 1.8V, supplying sufficient additional voltage headroom for the thin-oxide mixer transistors. Since all functions are implemented using a separate level of transistors, and a current-source cascode is applied to protect the sensitive current-source drain node, maximum performance is achieved. No impractical negative supply voltage is necessary.

There are three mechanisms which generate non-linear distortion related to the local mixer. One error mechanism is mismatch in the mixer which generates timing errors. This is discussed in Chapter 5 and Chapter 6. Another error mechanism is related to the *LO* signal transitions which generate a disturbance on the voltage of the common-source node of the mixer ($V_{mix,cs}$ in Figure 11.2), see error mechanism 6 in Section 5.2.4. The waveforms are shown in Figure 11.6, which shows the output waveform and the disturbance on $V_{mix,cs}$. The size of the disturbance, induced by a *LO* transition, depends on the settling value of $V_{mix,cs}$. Due to a limited output impedance, the settled $V_{mix,cs}$ value depends on the output voltage. Since there is parasitic capacitance on this node, the output-dependent disturbance consumes signal charge and hence introduces non-linear distortion.

The third error-source is the settling of $V_{mix,cs}$ when the *Data* signal switches. The mixer common-source node settles slowly. When the data switches again before $V_{mix,cs}$ is settled, ISI occurs, which generates non-linear distortion. This settling behavior is shown in Figure 11.7.

The non-linear distortion due to the latter error-source can be reduced by increasing the bleed current $I_{bleed,mix}$. Increasing $I_{bleed,mix}$ decreases the settling time and hence reduces the ISI. The required bleed current also depends on the input signal frequency, since a higher frequency results in the *Data* signal switching more frequent and thus the ISI occurring more often. This relationship is demonstrated in Figure 11.8 and Figure 11.9. To isolate this specific error source f_{LO} and F_S are chosen to be a low value (1GHz), which eliminates the other non-linearities. In this simulation, the

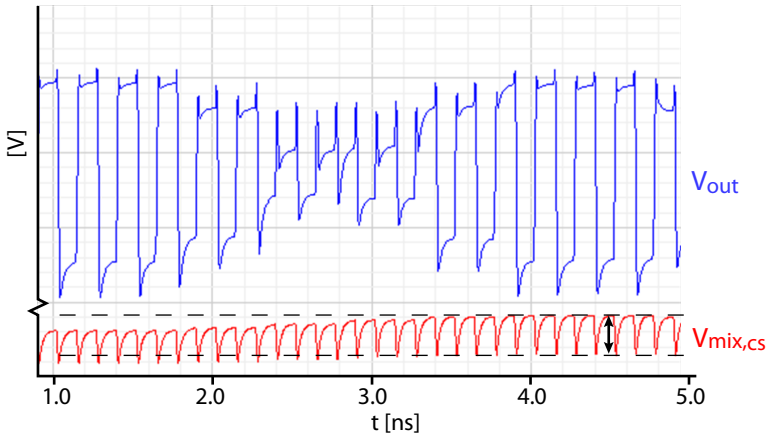


Figure 11.6: Mixer transitions cause disturbance on $V_{mix,cs}$ which introduces non-linear distortion

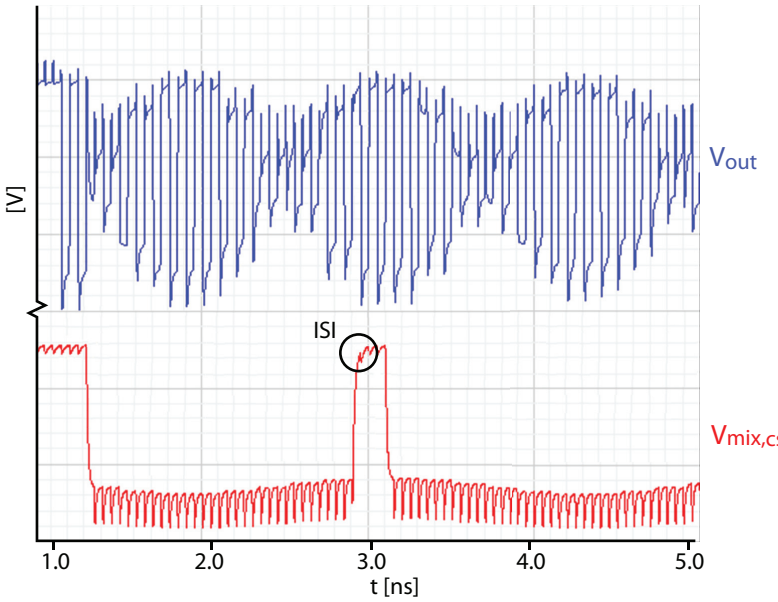


Figure 11.7: Incomplete settling of $V_{mix,cs}$ after *Data* transitions can cause Inter-Symbol-Interference (ISI) which causes non-linear distortion

width of the mixer transistors linearly depends on the maximum current through the transistor. The total bleed current through the output cascode is kept constant. The figures clearly shows the impact of the *Data* related ISI, which is present at higher input frequencies. Increasing $I_{bleed,mix}$

decreases this distortion. However, for very high $I_{bleed,mix}$, the transistor sizes become significantly larger, which increases $C_{OutCasc,s}$, increasing other non-linearities. A high bleed current also results in a high power consumption and large area. The chosen bleed current is 30µA, which is a trade-off between performance, power consumption and area.

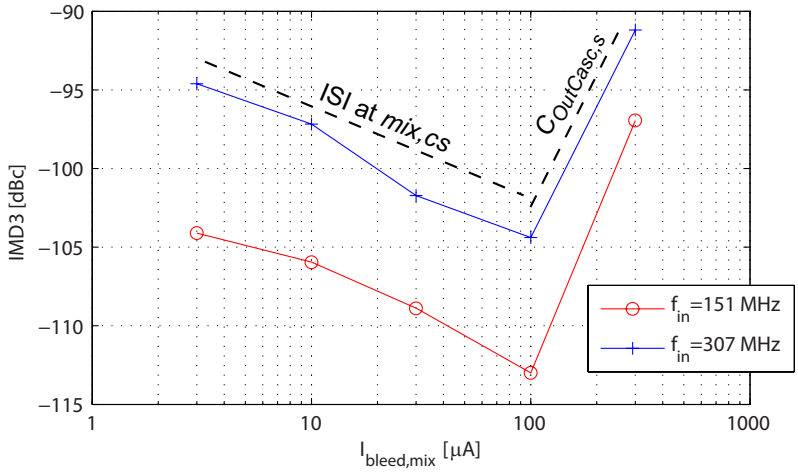


Figure 11.8: IMD3 dependence on bleed current and input frequency

The capacitive load for the LO driver should be as small as possible. Therefore, the area of the mixer is minimized. The length of the mixer (L_{mix}) is chosen 80nm, which is almost the lowest value. Choosing a lower value does not result in a significant lower capacitance but increases the mismatch significantly which worsens the timing errors.

The width of the mixer transistor (W_{mix}) is minimized for two reasons. The first reason is minimizing the capacitive load on the *LO* signal. The second reason is to minimize the parasitic capacitances at the source and drain of the mixer in the output stage. The capacitance at these nodes degrade the linearity. However, minimizing W_{mix} is limited by the available voltage headroom. Moreover, for scaling of the binary cells, a mixer transistor consists of 8 unit elements, which limits the minimum total W_{mix}. Choosing less unit elements will hamper the matching of the binary cells and degrade the SFDR, see Section 11.3.1.5.

The ISI due to the $C_{mix,cs}$ introduces IMD3 and single-ended HD2. Increasing W_{mix} increases this parasitic capacitance. Since the external balun has a limited common-mode rejection ration (CMRR), also the differential HD2 of the output signal is affected. The HD2 dependence on W_{mix} is shown

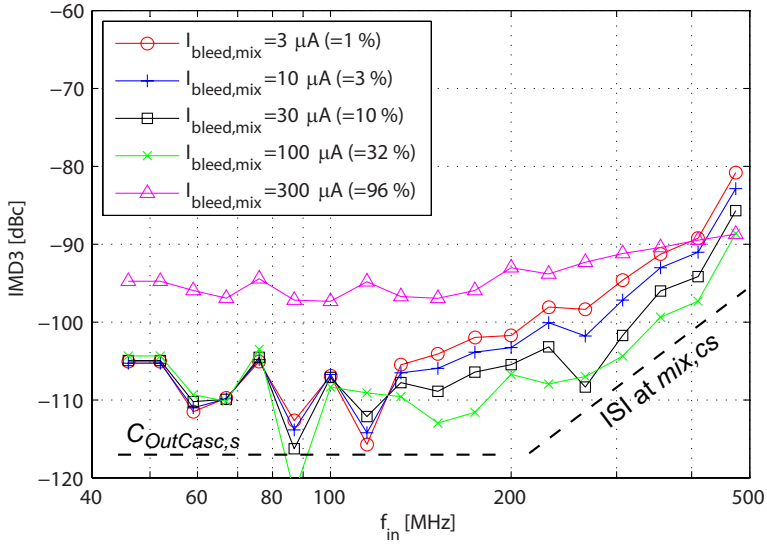


Figure 11.9: IMD3 dependence on input frequency and bleed current

in Figure 11.10.

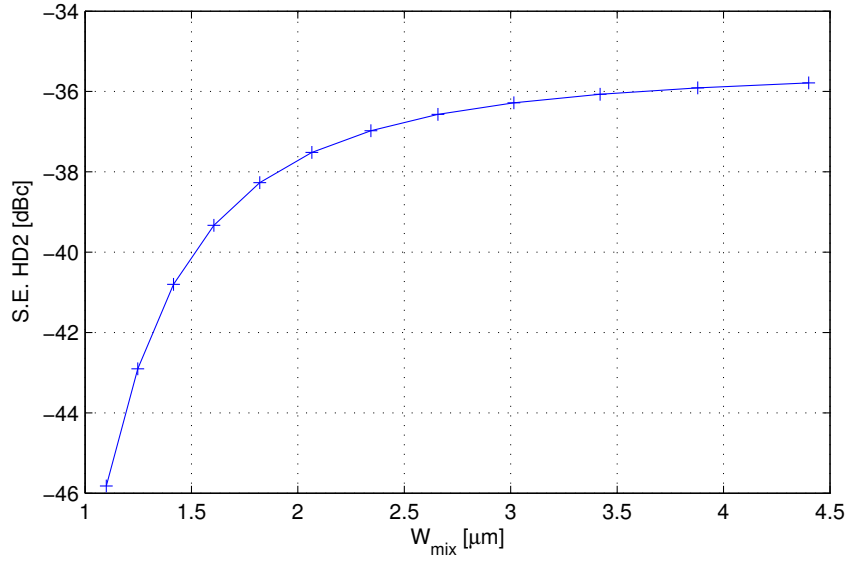


Figure 11.10: Single ended HD2 depends on the mixer width

11.3.1.3 Data switches & cascoded current sources

The data switches and cascoded current source are identical to the implementation of the baseline DAC. The sizing of the Data switches and current source cascode are optimized for voltage headroom for the current source and for minimizing the parasitic capacitances $C_{mix,cs}$ and $C_{data,cs}$. These transistors consist of a number of unit elements to offer good scalability for the binary current cells.

11.3.1.4 Local biasing and decoupling

To prevent crosstalk between the various unary current cells, local biasing and decoupling is used. A global gate-source voltage is distributed to generate a local bias current in each current cell. This bias current is used to locally generate the gate voltage of the current-source cascode (V_{g2}) and output cascode (V_{gc} and V_{gm}). Local decoupling of the sensitive voltages ensures that disturbances are filtered out. All static voltages of transistors higher than the current source cascode (Data switch, mixer, output cascode and bleed-current cascodes) are decoupled to the 1.2V supply. In this way, almost all voltages in the current cell are relative to the 1.2V supply. Using a one common reference prevents disturbances between multiple references, which could generate spurious components in the output.

11.3.1.5 Binary cells

The response of the binary current cells should be an exactly scaled version of the response of the unary cell. An example of the difference between the output spectrum of sub-optimal scaling and optimized scaling is shown in Figure 11.11. The scaling of the binary part is also discussed in Chapter 9. Three techniques are employed to achieve optimal scaling.

The first technique is that each transistor in the unary current cell consists of 2^u unit elements, where u is an integer number. In this way, binary scaling is as easy as disconnecting a number of the transistor unit elements. Each binary cell has half the unit elements enabled compared to the previous binary cell. In the unary current cell, the mixer transistors consist of 8 unit elements each. This means that unit-element scaling is possible up to the third binary cell (B9, B8 and B7). For the other binary cells the width of the transistor needs to be scaled to approach the accurate scaling. The output cascode transistors consist of 4 unit elements, hence unit-element scaling is possible for B9 and B8. However, the width of the unit element transistors is such that width-scaling is possible and acceptable results are achieved.

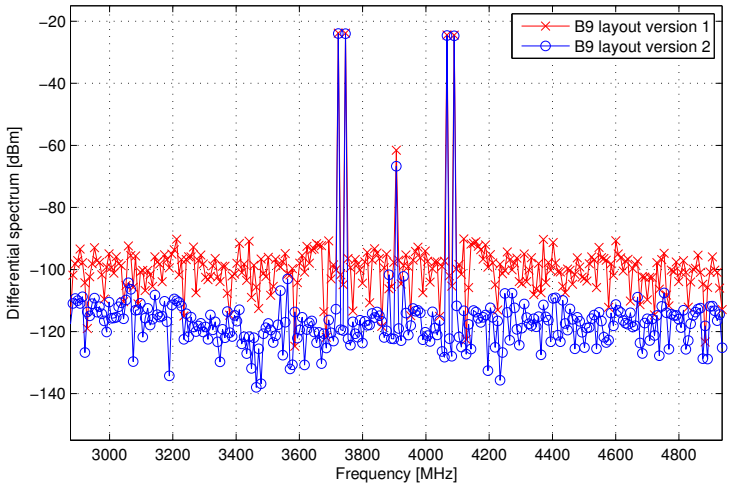


Figure 11.11: Spectrum of the simulated back-off output signal with sub-optimal and optimized B9 layout

The second technique is the scaling of the parasitic capacitances. When the parasitic capacitances are not accurately scaled, the time-constant of the nodes are not identical and hence the response is different. The scaling of the parasitic capacitances requires a scalable layout, which is discussed in Section 11.3.2.

The third technique is to make the unary and binary cells identical for the driving signals. In that way, the Data driver and the LO distribution tree do not need to be altered for the binary cells and can be identical for all current cells. The Data driver and the LO distribution tree need to sense the same input impedance for each unary and binary current cell. However, only a subset of the Data and LO unit transistors are used in the main output branch for the binary cells. The remaining unit transistors are also connected to the driving *Data* and *LO* signals, but their drain-source current is used in a replica branch. This replica branch has approximately the same behavior as the output branch such that the total impedance for the driving signals is identical to the unary current cells. A schematic representation of the replica branch is shown in Figure 11.12, where the biasing and the bleed currents are omitted for clarity.

The use of a replica branch also aids the scaling of the parasitic capacitances. Since the replica branch has identical behavior with respect to the output branch, parasitic capacitances between corresponding nodes of the replica branch and main branch do not conduct error charge and hence

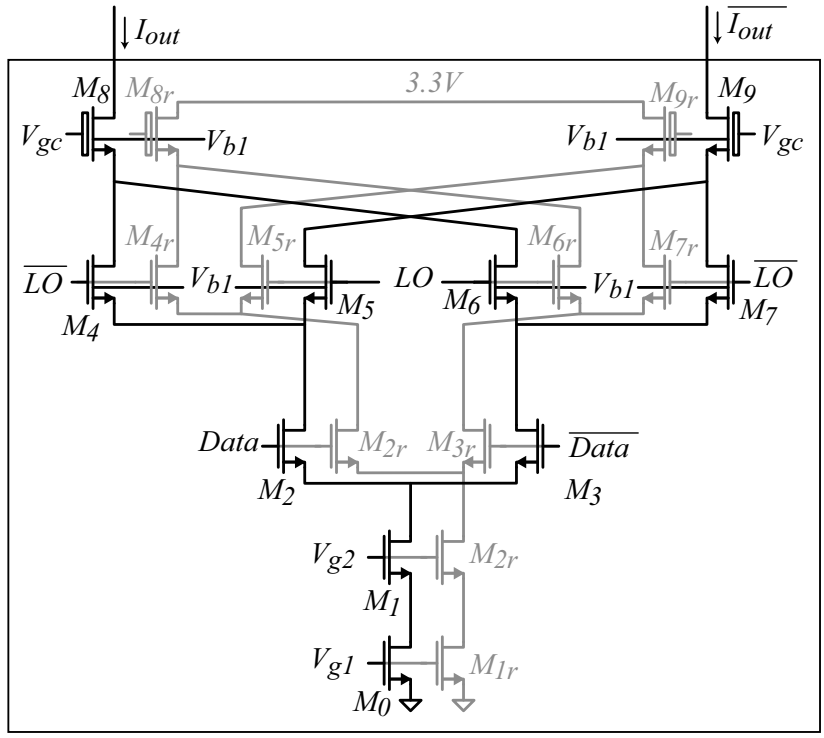


Figure 11.12: Binary current cell with ultimate replica branch

are not important.

11.3.2 Layout

The layout of the output stage is key to achieving a high spectral purity. Reducing parasitic capacitance values at crucial nodes prevents crosstalk, ISI and other error sources which cause non-linear distortion.

11.3.2.1 Floorplan output stage

The floorplan of the complete output stage is shown in Figure 11.13. In this floorplan, the length of the RF signal path is minimized. Therefore, the LO distribution tree, mixer, output cascode and output tree are close together. The track of the *Data* signal connects the Data drivers to the Data switches. The sample rate of the *Data* signal is lower than the LO frequency, and the *Data* signal switches only at the input frequency. Hence, the distance of the *Data* track is less important than the distance of the tracks of the RF signals. Also less important is the distance between the biasing and current source

array on the one hand and the other parts of the output stage on the other hand.

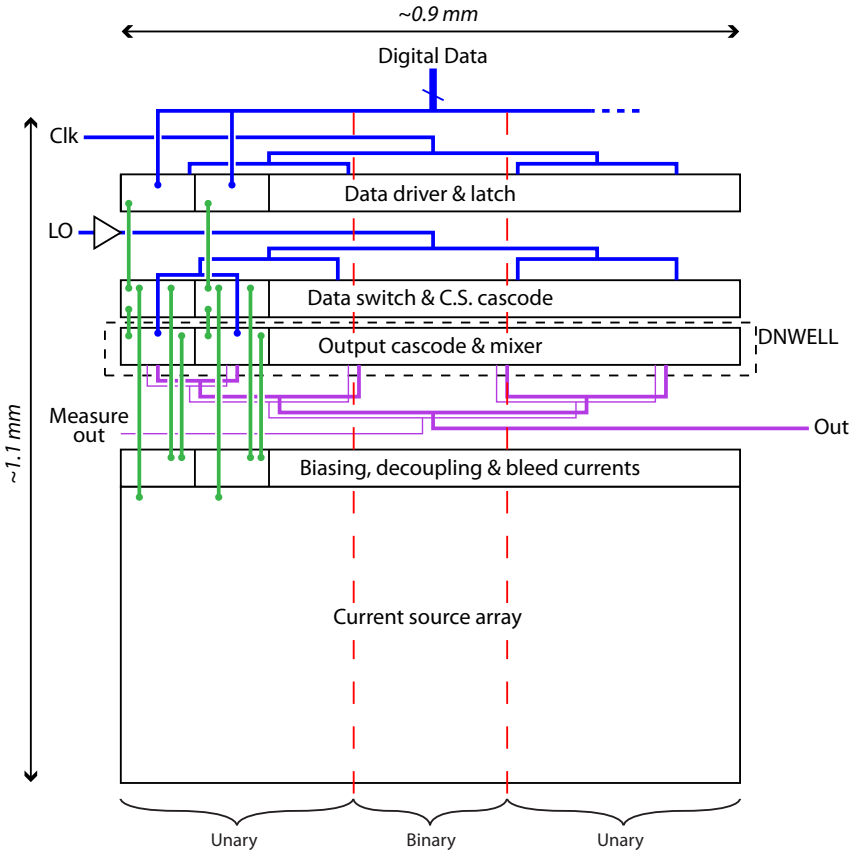


Figure 11.13: Floorplan of the output stage with Data drivers and latches

The current cells are positioned in vertical slices, where shielding between the slices prevents crosstalk. The binary cells are positioned at the center of the current-cell array, while the unary current cells are positioned on either side of the array.

The layout of a current cell influences the impact of processing imperfections, e.g. due to shading effects in the processing. In the proposed layout, half of the current cells have inversely polarized *Data* and *LO* connections. Hence, layout unbalances due to the processing are compensated when two neighboring cells are both enabled. This is true for most cases, since the current-cell array is controlled in a thermometer fashion.

11.3.2.2 Floorplan current cell

The floorplan of one slice is shown in Figure 11.14, which is a more elaborate version of the floorplan of Figure 11.13. The parasitic capacitance of the internal nodes of the current cell needs to be minimized, hence the current-source cascode, data switch, mixer and output cascode are grouped close together. Tracks with high frequency signals are short while lower-frequency tracks and biasing connections are allowed to be longer. The decoupling of the locally generated voltages and the distributed voltages is split in two parts: one part close to the signal path for high frequency decoupling and a part further away for the lower frequency decoupling. The biasing block contains the generation of the bleed currents and the local voltages for the gates of the current-source cascode and output cascodes.

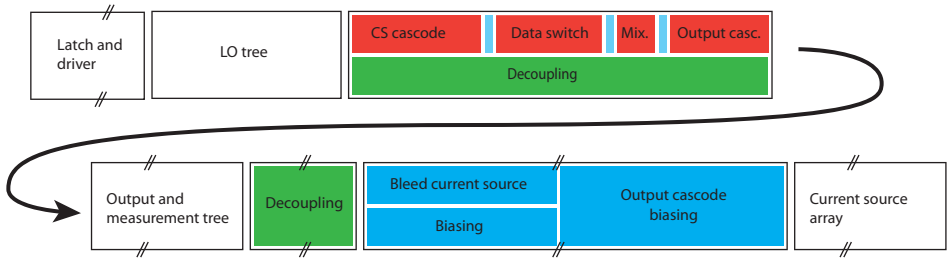


Figure 11.14: Floorplan of one slice of the output stage, 90° rotated

11.3.2.3 Output cascode layout

The most important parasitic capacitance is at the source of the output cascode ($OutCasc, s$ in Figure 11.2), since it experiences the largest coupling to the large output voltage swing. This capacitance should be minimized and should be made maximally scalable for the binary cells. The layout strategy for these requirements is illustrated in Figure 11.15. In this figure, the measurement cascodes and the replica branches are omitted. The blue blocks are the transistors. The sources of those transistors are connected to the $OutCasc, s$ node, while the drains are connected to the *out* node which is the output of the Mixing-DAC. The black lines represent layout connections. The length of the $OutCasc, s$ connection is partly scalable and partly fixed. The scaling of the parasitic capacitance can be perfected by tuning the width of the track. Tuning of the track width is also required for the output cascode of binary current cells B7 to B0.

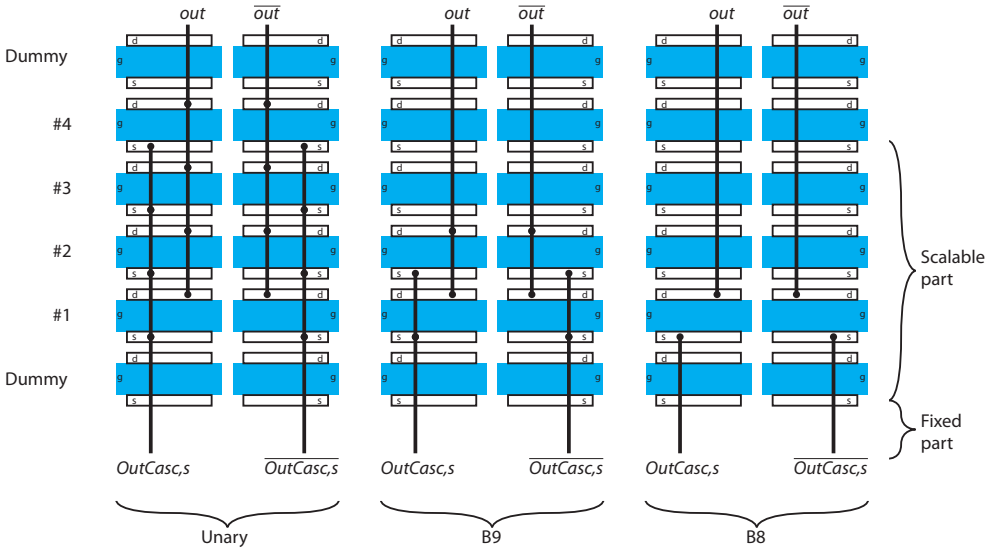


Figure 11.15: Layout strategy for the output cascode

11.3.2.4 Mixer layout

The mixer layout is specifically challenging because of the cross connections of the mixer. The layout strategy of the mixer is similar to that of the output cascode and is illustrated in Figure 11.16. In this illustration, the dummy transistors and the replica branches are omitted. This layout strategy is focused at a scalable $OutCasc, s$ node, minimal parasitic capacitance at the $OutCasc, s$ node, and differential matching.

Minimal parasitic capacitance of the $OutCasc, s$ node and scalability of the $OutCasc, s$ node are both achieved by connecting this node without horizontal connecting wires, as is the case for the LO and mix, cs nodes. However, there still is a part of the $OutCasc, s$ track which has a fixed length. Tuning of the width of this track perfects the binary scaling of the parasitic capacitance of this node.

For differential matching, all corresponding nodes (LO and $\overline{LO}$, $OutCasc, s$ and $\overline{OutCasc, s}$, mix, cs and $\overline{mix, cs}$) have the same length of wiring. However, some tracks see different environments and hence have different parasitic capacitances to different nodes. Therefore, single ended HD2 is converted to differential HD2 due to non-ideal matching of these parasitic capacitances.

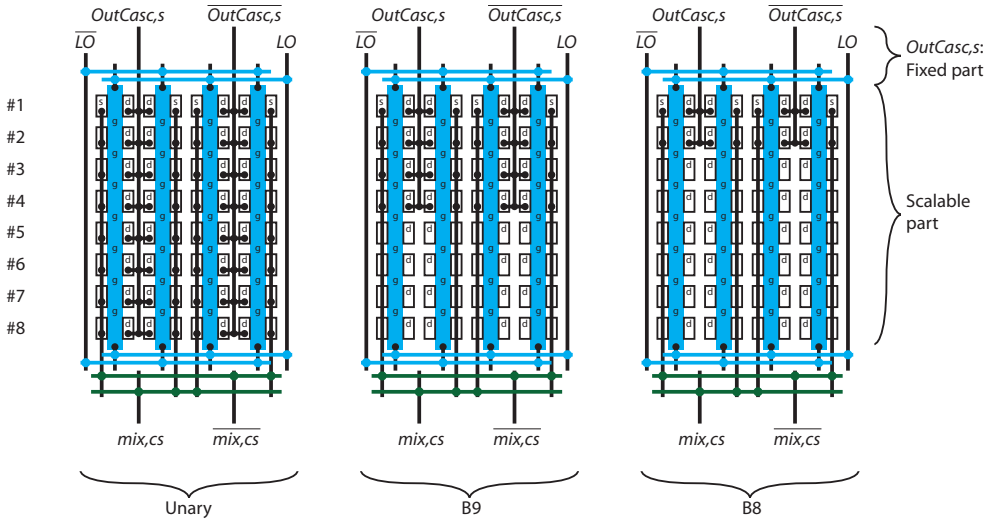


Figure 11.16: Layout strategy for mixer

11.3.2.5 Layout of cascoded current source, data switches and biasing

The layout of the current source, current source cascode, data switches and biasing is adopted from the layout of the baseline DAC. The same approach as for the mixer and the output cascode is employed: unit elements for scaling, layout of the connection tracks for scaling, and minimization of parasitic capacitances at sensitive nodes.

11.3.2.6 *LO* and output tree layout

For high spectral purity, the delay timing errors should be minimized, see Chapter 6. Unbalance in the distribution of the *LO* signal or output recombination can cause delay timing errors. Hence, a balanced tree structure is used to implement these two functions.

For the LO distribution tree, the load of all unary and all binary cells is equal. For the binary cells, this is achieved by utilizing the replica approach which is discussed in Section 11.3.1.5. The tree structure is based on a binary tree. The principle of the tree, which is adopted from the tree design of the baseline DAC, is illustrated in Figure 11.17. The various metal layers in the chip can be used to exchange lateral area occupation with the number of occupied metal layers.

The tree is characterized by the delay between the root and the leafs. The goal of the tree structure is do minimize the delay difference between the leafs.

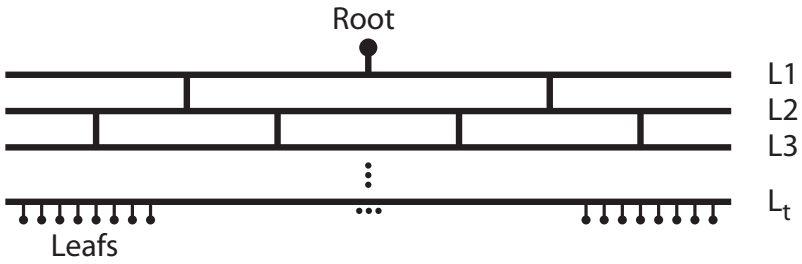


Figure 11.17: Principle of the binary tree for the *LO* and output signal

Each level of the tree (L1, L2, ..., Lt) smooths this delay difference. All levels consist of 2^L connections to the next level, where L is the number of the level. Since the number of cells is 80, which is not a power of two, the last level L_t does not contain 2^t levels, but 80 levels. The higher t, the lower the delay differences between the leafs.

The relative delay for the LO tree is shown in Figure 11.18. The x-axis is the spatial position of the current cell in the array of current cells, while the y-axis is the delay error with respect to the average delay. As can be seen in the plot, the binary cells are positioned at the center of the current-cell array, while the unary current cells are positioned on either side of the array. These simulation results are obtained using RC extractions. For higher frequencies or higher accuracy, an EM simulation would be more appropriate. The original configuration is a tree with 7 levels and with the position of each connection between levels at the theoretical position. However, even with this tree structure the delays of the 80 leafs are not identical. Due to edge effects the delay distribution is inclined toward the middle. And due to non-identical capacitive load at the binary cells, the delay for the binary cells is different than the delay of the unary cells.

One optimization technique that is applied, is to shift the connections between the various levels away from the center of the tree. This compensates for the rotated delay distribution.

It can be observed that the delay spread of the binary cells is larger than that of the unary cells. However, since the influence of the binary cells is much smaller than the influence of the unary cells, the delay spread of the binary cells is allowed to be orders of magnitude larger than for the unary cells. Therefore, the larger delay spread of the binary cells is acceptable and no compensation is required.

The same approach is used to design the output recombination tree, which is shown in Figure 11.19. For the optimization of the output tree, the

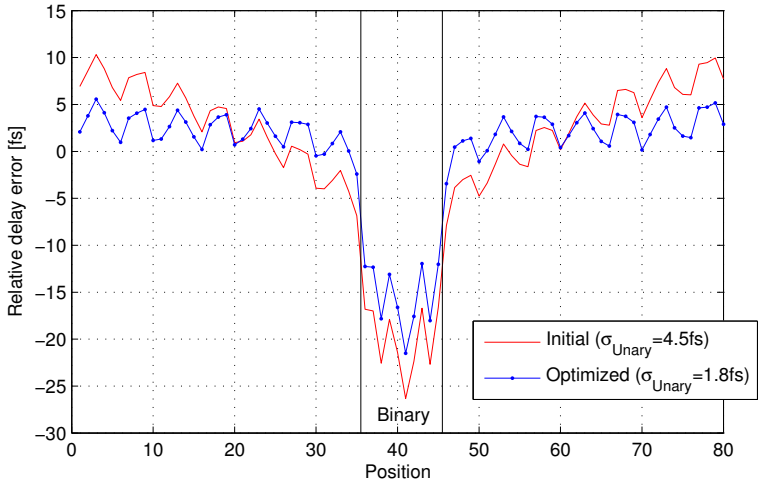


Figure 11.18: Relative delay error of each endpoint of the LO tree to the root, both for initial and optimized layout

following methods are used: shifting of connections between levels, widening of the last level, tuning of the leaf wiring of the binary current cells. The output capacitance of the binary cells is not similar to that of the unary cells. Therefore, the width of the wiring between the output of the binary current cells and the last level of the tree is optimized to equalize the RC time constants and remove any excessive delay timing errors.

The standard deviation of the delay errors of the unary part of the LO tree and the output tree are 1.8fs and 7.2fs respectively, which are both smaller than the required 55fs of Section 6.5.

11.4 LO driver

The LO driver is required to drive the LO switching transistors, which are connected by the LO tree. The LO tree and the LO transistors cause a large parasitic load at the output of the LO driver. The timing errors between the *LO* signals at the gates of the LO transistors is required to be minimal. Therefore, the LO driver is a global driver and connected to the LO transistors via a balanced tree.

The LO drive chain consists of two cascaded CML drivers, a regulator for the local supply voltage and a reference voltage generator for the regulator. The schematic of the LO drive chain is given in Figure 11.20.

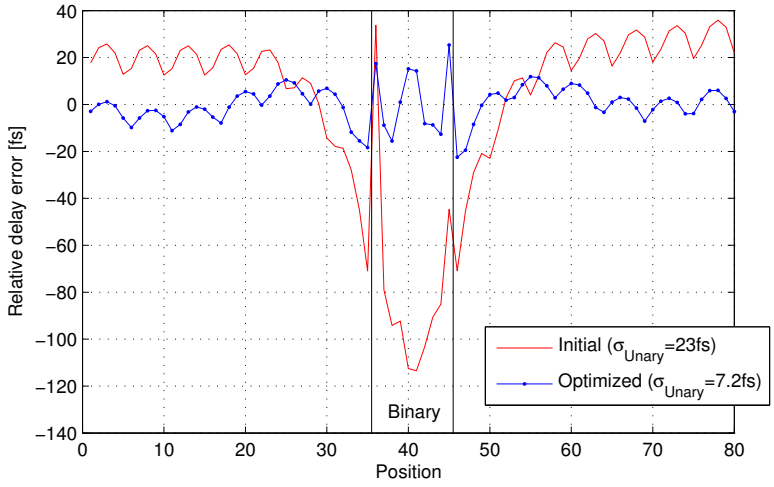


Figure 11.19: Relative delay error of each current-cell output to the root of the output tree, both for initial and optimized layout

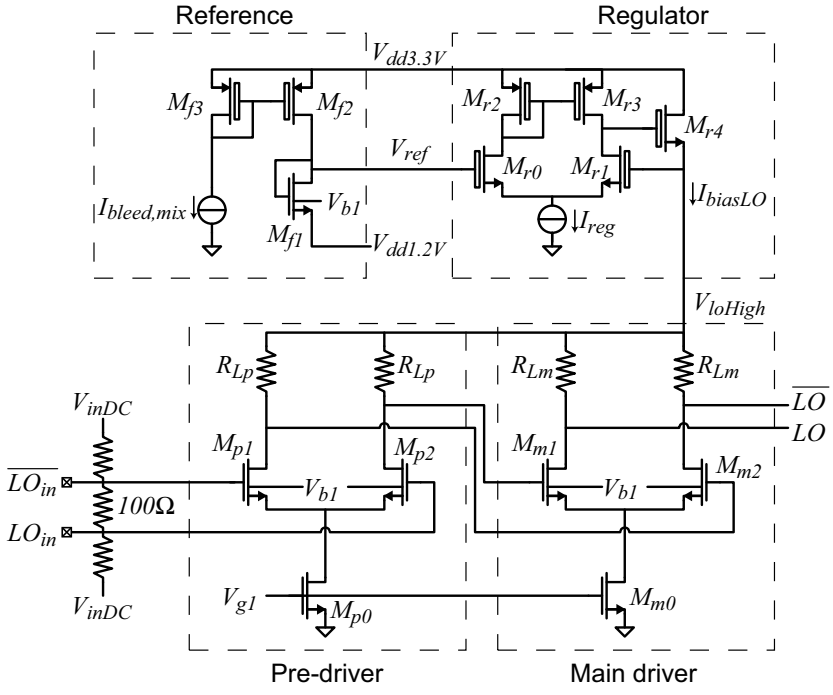


Figure 11.20: Schematic *LO* drive chain

11.4.1 Drivers

Both the main LO driver and the pre-driver are implemented using a CML buffer to prevent signal-dependency in the supply current. It also enables easy control over the signal levels and the cross-over point. The drivers use thin-oxide transistors as switches (M_{p1}, M_{p2}, M_{m1} and M_{m2}) to minimize the parasitic capacitances and thus enable high-speed operation. The *LO* signal voltage levels are above 1.2V, hence the bulk voltage of the switching transistors is the same elevated bulk voltage as the mixer switches in the output stage.

The LO frequency of 4GHz requires a low RC time constant for the LO driver. The large LO tree parasitic capacitance, i.e. approximately 1pF, forces a low load resistance for the CML driver. The load resistor (R_{Lm}) is chosen to be 20Ω. Since the W/L of the mixer is low, the swing of the *LO* signal should be large, i.e. 800mV. This requires a tail current of 40mA through M_{m0}.

The pre-driver only requires I_{tail}=10mA (through M_{p0}) and R_{Lp}=80Ω for fast operation. The input of the pre-driver contains a 100Ω differential resistor for termination of the transmission line of the external LO_{in} signal. The input of the pre-driver also contains resistors for the biasing of the input transistor pair, hence external capacitive coupling is preferred.

The LO driver has a number of digital inputs. The digital input can configure the *LO* signal to be static. In that case, the mixer transistors in the output stage become normal cascodes and the Mixing-DAC becomes a Nyquist DAC. For calibration purposes, the polarity of the static *LO* signal can also be controlled. For clarity reasons, the implementing circuits of both functions are not shown in the schematic of Figure 11.20.

Disturbances at the supply of the LO drivers (V_{loHigh}) couple to the output of the Mixing-DAC through two coupling paths. One coupling path is that low frequency disturbances (at f_{dist}) first mix with the *LO* frequency, and then appear at the *LO* signal. Hence, the output of the Mixing-DAC has disturbances at $f_{in}+f_{LO}+f_{dist}$. The second disturbance path is that a high frequency disturbance at f_{dist} directly couples to the Mixing-DAC output at f_{dist}. This coupling path mainly causes single-ended distortion at the output. For achieving the desired spectral purity, these disturbances need to be smaller than approximately 10mV. Therefore, the regulator of the local supply voltage is optimized for rejection of disturbances from the 3.3V supply. When expecting a disturbance in the order of 50mV on the 3.3V power supply, the regulator should have a power supply rejection ration (PSRR) of approximately 14dB.

11.4.2 Local supply voltage

The internal regulator generates the local power supply V_{loHigh} for the LO drivers from the 3.3V supply voltage. The regulator also ensures that the local supply voltage of the LO driver remains clean and undistorted.

A low output impedance is necessary to prevent modulation of the V_{loHigh} due to variations in the current through the LO drivers. The feedback configuration provides a low output impedance for low frequencies. The second stage of the regulator is a source follower, which supplies 50mA to the LO drivers and hence has a very large area and large parasitic capacitances. Therefore, the bandwidth of the feedback loop is only 8MHz. The source follower configuration provides a low output impedance for frequencies above 8MHz. For very high frequencies, decoupling of V_{loHigh} results in a low output impedance. The decoupling capacitors are not shown in the schematic. Combining these three features, the worst case output impedance is 5Ω.

The PSRR of the regulator is 15dB at the worst corner-case. This is better than the required 14dB, hence disturbances below 50mV on the 3.3V power supply will not cause the spectral purity to be worse than the target.

11.4.3 Reference generator

The reference V_{ref} for the regulator is generated from the 1.2V supply and a diode-connected transistor. This transistor has the same sizing and layout as a mixer transistor in the output stage. The current through the transistor is equal to the bleed current $I_{bleed,mix}$. Hence, the reference voltage is: $V_{ref} = 1.2V + V_{gs}(I_{bleed,mix})$. In this way, the voltage at the source of the mixer never exceeds 1.2V, and the data switches are protected against an excessive voltage.

The ratio of the current mirror in the reference can be programmed through a digital interface. By controlling the current through the reference diode, V_{ref} can be programmed for optimal performance.

11.5 Driver for elevated bulk voltage

The schematic of the circuit which generates the elevated bulk voltage is shown in Figure 11.21. It is a simple two-stage amplifier. The elevated bulk voltage is approximately 0.6V and is referenced to the 1.2V supply and decoupled to the same power supply. This referencing to the 1.2V power supply is because all transistors in the output stage which are connected to the elevated bulk voltage are also referred to the 1.2V supply. Thanks to the

large decoupling capacitor, the output pole is dominant and the amplifier is very stable. The reference current through the resistor is programmable.

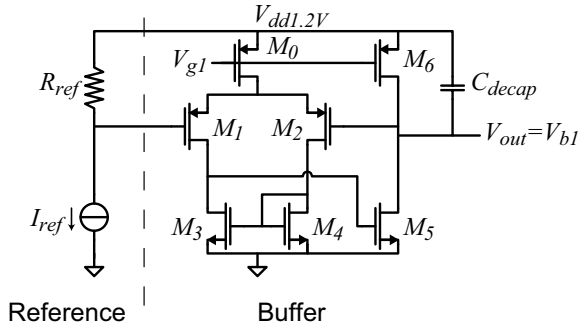


Figure 11.21: Schematic for generating the elevated bulk voltage

11.6 Data path

The data path consist of a serial interface, digital signal processing, a programmable decoder, latches and drivers. The implementation of these functions are identical to the implementation in the baseline DAC.

The digital signal processing can be used to apply simple operations, such as: upsampling, filtering, mixing with a sine-wave. These operations can be applied in the complex signal domain and hence the two Mixing-DAC cores can operate with I/Q signaling. The digital signal processing also contains controllable compensation for mismatch in the analog part of the I/Q paths.

The ESD devices of the LO inputs and the digital power supply are connected to the same power-supply rail. This causes coupling between the LO signal and the digital supply voltage. Some of the digital operations are executed at $1/8^{\text{th}}$ of the sample rate, which causes harmonics in the supply voltage at $n{\cdot}F_S/8$. Due to the coupling of the ESD devices, in measurements spurious components at those frequencies can appear in the *LO* signal and also in the Mixing-DAC output. Due to time limitations, the ESD domains could not be separated to prevent this coupling.

For the latches and drivers, CML logic is used. This prevents data-dependent current drawn from the power supply and enables control of the crossover point of the *Data* signal.

11.7 Full system simulations

The total area of the implementation of one Mixing-DAC core (Mixing-DAC without digital signal processing) is 1.6mm^2. System level simulations are performed on the complete chip excluding digital signal processing and with package model. The most important circuits are modeled with C-extracted models.

A wide view of the resulting spectrum with full-scale signal is shown in Figure 11.22, where both the single ended and the differential output signal are shown. The main output components are around f_{LO}=3.9GHz. A zoom-in of the output Nyquist band above f_{LO} is given in Figure 11.23. The main performance specifications are: IMD3=-82dBc and SFDR_{RB}=78dBc. The SFDR_{RB} is limited by an IMD2 component at the edge of the RB, close to the LO frequency. When omitting the IMD2, the highest spur is the IMD3 component at -82dBc.

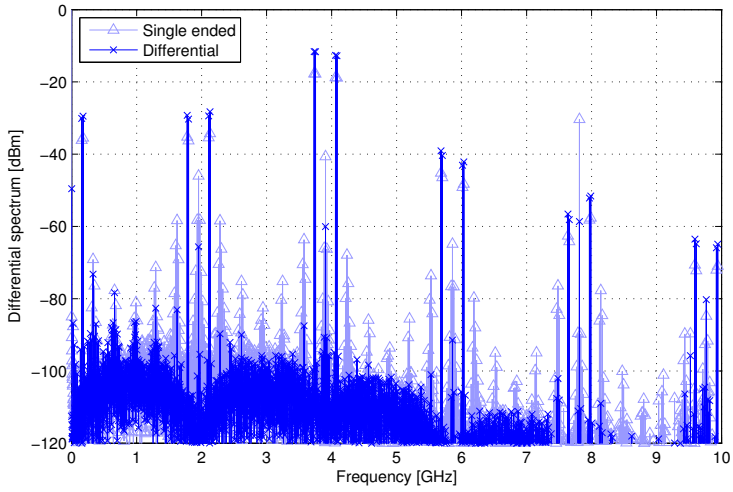


Figure 11.22: Wide spectrum of the simulated full-scale output signal of Mixing-DAC A

Fundamental limits of the IMD are the output coupling to internal nodes and the mismatch of the mixer. The coupling of the output to internal nodes is related to the output cascode. Increasing the cascode size improves the cascode function, but also increases the non-linear capacitance values. Mismatch in the mixer causes timing errors. The mismatch can be reduced by increasing the size of the mixer. This will increase the parasitic capacitances in the mixer which will increase the non-linearity due to coupling of the output

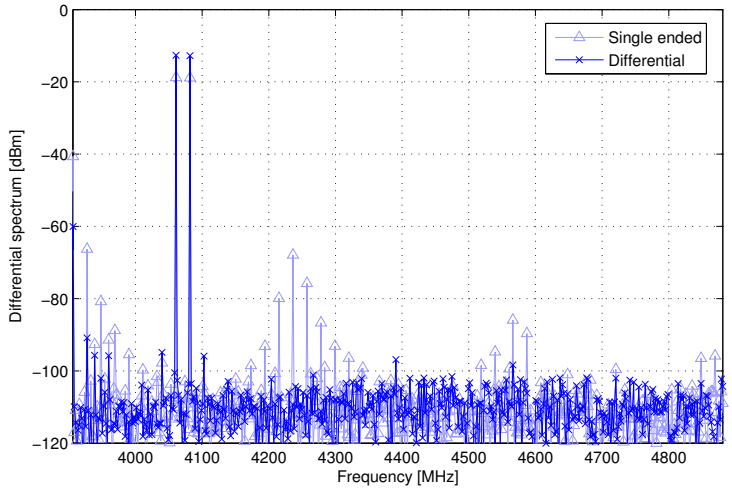


Figure 11.23: Nyquist spectrum of the simulated full-scale output signal of Mixing-DAC A

voltage to the internal nodes.

Practical error-sources also limit the performance. The IMD2 can be caused by imperfect balancing of the layout of the current cells, ISI at the source of the mixer and coupling between bond wires and wiring on the chip. Practical limitations on the achieved IMD3 can be due to capacitive coupling of on-chip signals.

For -16dB$_{FS}$/tone output power, the simulated spectrum is shown in Figure 11.24. The main performance specifications are: IMD3=-93dBc and SFDR$_{RB}$=80dBc. The SFDR in back-off is limited by the matching of the binary cells.

Corner simulations show only small degradation of the performance metrics. The simulation results are close enough to the formulated targets to justify fabrication of this design for verification.

11.8 Conclusion

To validate the proposed architecture, a 16 bit 2GSps 4GHz Mixing-DAC is designed. The design of the output stage is crucial for achieving the desired spectral purity. Using the correct techniques, the desired performance can be achieved. Crucial techniques are:

- giving each current cell an identical environment,

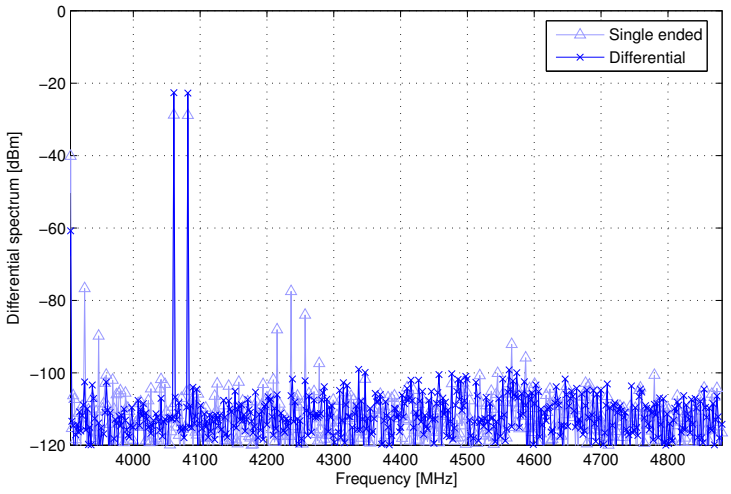


Figure 11.24: Nyquist spectrum of the simulated output signal of Mixing-DAC A in back-off

- isolating the current cells from one another,
- isolating the internal nodes of the current cells from the output signal,
- implementing each function of the output stage with a separate level of transistors,
- using an elevated bulk voltage for improving voltage headroom.

The verification simulations show that the expected performance is close to the target specifications.

The expected and simulated performance is limited by the coupling of the output to internal nodes, output-cascode capacitances, mismatch-induced timing errors of the mixer, coupling between signals due to the bondwires and on-chip wiring, and matching of the binary cells.

12 | Experimental results

The design proposed in the previous chapter has been fabricated and measured. This chapter presents the measurement results and compares these results with the simulated performance and with the state-of-the-art performance. The performance limitations are analyzed and suggestions for improvements are given. The measurement results show that the proposed architecture can achieve high linearity and large bandwidth at GHz frequencies.

This chapter is based on a paper submitted to the IEEE ISSCC 2015 conference [81].

12.1 Introduction

The design presented in Chapter 11 has been fabricated. A photo of the dual-Mixing-DAC die with two Mixing-DAC cores and the digital front-end is shown in Figure 12.1. This chapter presents the measurement results of that chip. The measurement setup is discussed in Section 12.2. The baseband performance (LO driver in static state) is discussed in Section 12.3. The performance of the Mixing-DAC with the mixer enabled, is discussed in Section 12.4 and Section 12.5 for sinusoidal signals and radio signals respectively.

12.2 Measurement setup

The setup for measuring the Mixing-DAC performance is shown in Figure 12.2. The two main parts of the measurement setup are the equipment and the measurement board.

12.2.1 Measurement equipment

The 16-bit digital data for the Mixing-DAC is generated by the data generation board. The output of the Mixing-DAC is observed by a spectrum

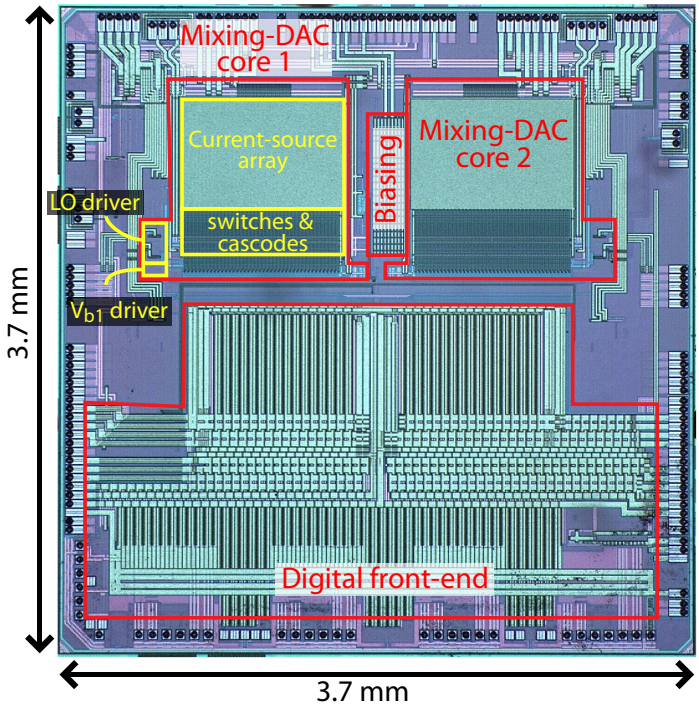


Figure 12.1: Photo of the fabricated chip

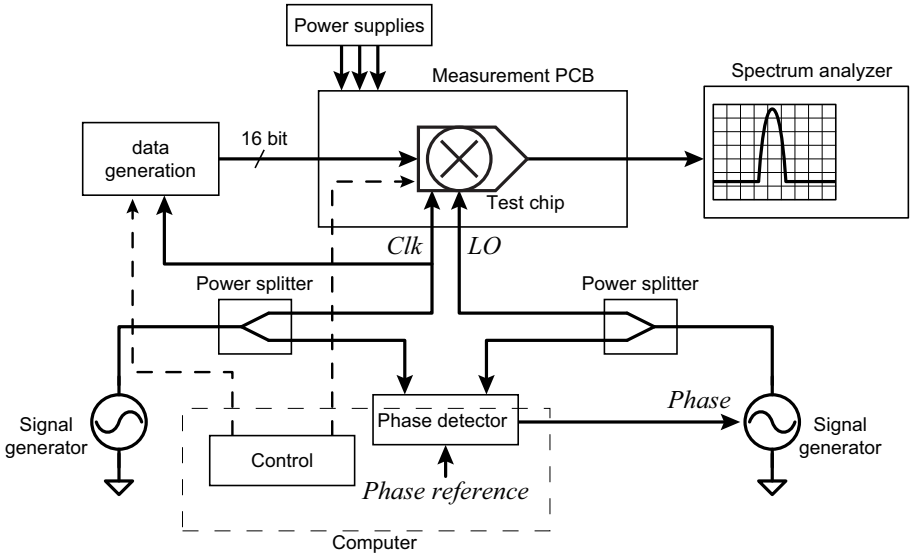


Figure 12.2: Measurement setup

analyzer.

The sample clock and LO signal are sine-wave signals, generated by signal generators. As discussed in Section 12.4.4, the phase between these two signals is important for linearity. Therefore, the sample clock and LO signal are both split using power splitters. One side is connected to the Mixing-DAC and the other side is connected to a phase detector. The phase detector is actually an oscilloscope which measures the time difference between the zero-crossings of the two signals. This time difference is transferred to the computer, which compares it to the phase reference set by the user. The computer calculates the phase error between the actual clock-LO phase and the desired phase. The user can initiate the phase correction of the LO signal generator, so the computer does not execute phase corrections autonomously during sensitive measurements.

The settings of the data generation board and the Mixing-DAC are configured using the computer. Power supplies provide power to the Mixing-DAC.

12.2.2 Measurement board

The Mixing-DAC measurement board is used to interface between the measurement equipment and the Mixing-DAC chip. An overview of the schematic of the measurement board is shown in Figure 12.3.

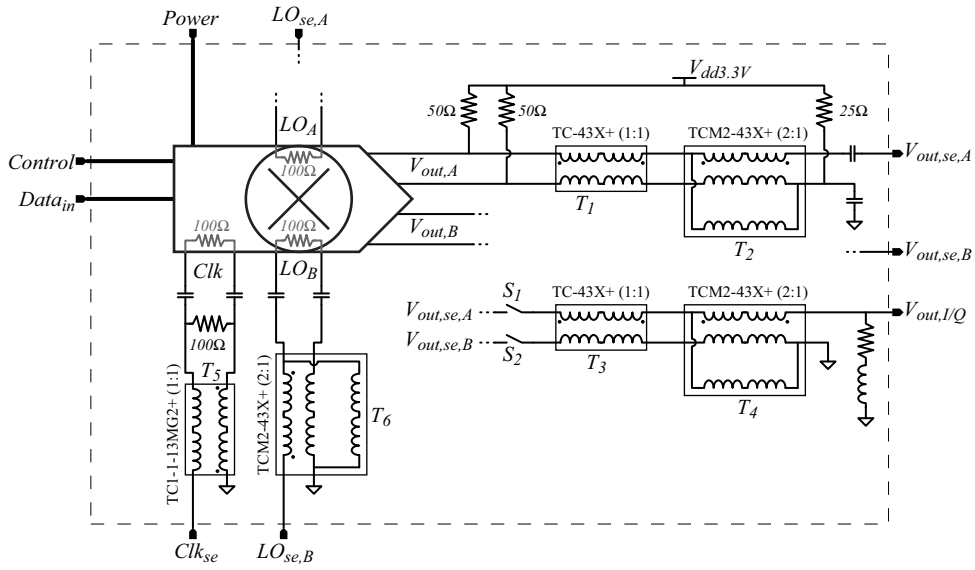


Figure 12.3: Measurement board

The input and output signals of the Mixing-DAC are all differential, while the inputs and outputs of the measurement equipment are all single ended. Therefore, transformer baluns (T_2, T_5, T_6) are used to convert the signals between differential and single ended. For additional common-mode rejection at the Mixing-DAC outputs, an additional (1:1) common-mode transformer (T_1) is used. For measurements with I/Q signaling, a branch which combines the single-ended outputs of the two Mixing-DAC cores is implemented with transformers (T_3, T_4). This additional circuitry can be connected by closing switches S_1 and S_2, but is normally disconnected to not influence the single-Mixing-DAC measurements.

All transmission lines are terminated with effective 50Ω. The Clk input of the Mixing-DAC contains an internal 100Ω termination. Together with the external 100Ω termination and the 1:1 transformer T_5, the input impedance of the Clk_{in} input is 50Ω. The LO_A and LO_B inputs are internally terminated with 100Ω. Together with the 2:1 transformer T_6, the input impedance is 50Ω. The Mixing-DAC outputs are not internally terminated. The external termination of 100Ω differentially and the 2:1 transformer T_2 result in an output impedance of 50Ω.

Since the output connection contains the most sensitive signal, the output circuit of a single Mixing-DAC on the measurement board is characterized. The output return loss (S22) of the output of the measurement board with chip and connecting cable is shown in Figure 12.4. The S22 should be below -10dB for good suppression of the reflections. A possible cause for the two violations at 1GHz and 2GHz can be that the output of the Mixing-DAC is not

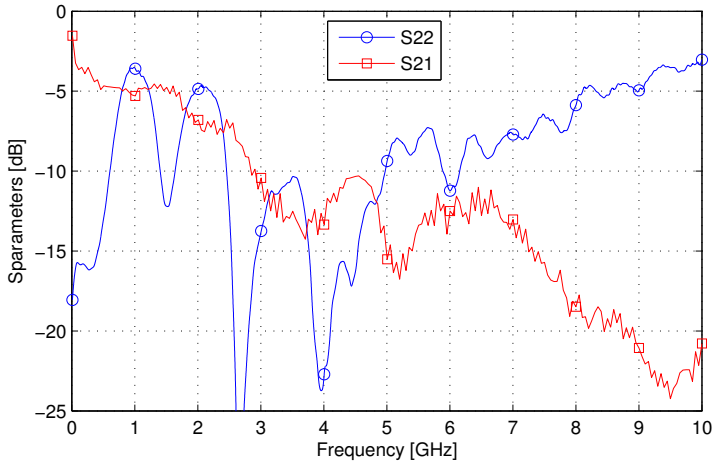


Figure 12.4: Scattering parameters of the measurement board

a proper transmission line up to the 2x50Ω resistors, but is more capacitive and inductive due to the Mixing-DAC output capacitance and bondwires. The reflections caused by suboptimal termination can cause frequency dependent fluctuations in the signal power and may cause degradation of the measured linearity. The insertion loss (S21) of the measurement board and cable, from the pins of the Mixing-DAC chip to the output of the cable is also shown in Figure 12.4. The high frequency dependent loss is due to the loss of the transformers, the tracks on the measurement board and the connecting cable.

A photo of the measurement setup is shown in Figure 12.5.

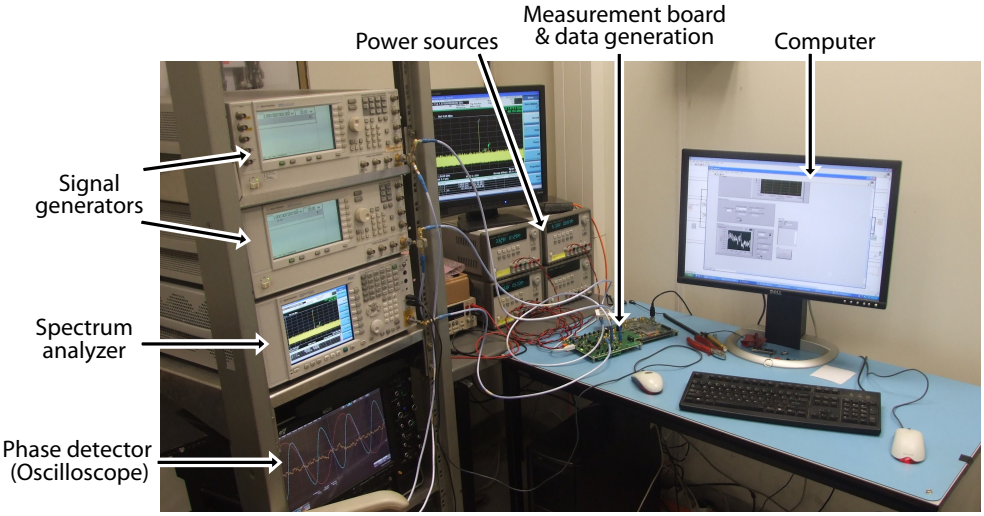


Figure 12.5: Photo of measurement setup

12.2.3 Calibration

The Mixing-DAC contains a sort-and-combine calibration method [3]. This calibration compensates for the static mismatch of the current sources and timing errors of the Data switching. The principle of the sort-and-combine calibration is to combine unary current cells with opposite errors. In the combined current cell, the errors cancel one another. Hence the combined error is much smaller than the individual errors. Due to the combining of the unary current cells, the effective segmentation of the converter is not the aforementioned 6MSB + 10LSB, but less MSB unary bits. The combing is done twice, hence the effective segmentation is: 4 calibrated MSB unary bits, 2 calibrated binary bits, 10 uncalibrated LSB binary bits. A programmable decoder for the binary-to-unary decoding for the unary current cells executes

the calibration map, which contains the information about which current cells should be used together.

The error sources are measured using an on-chip measurement circuit. The measured values are transferred to a computer, which calculates the most optimal combination of unary current cells, the calibration map. This map is programmed once in the chip, and is active for the remaining lifetime of the chip.

12.3 Baseband performance

First the performance of the Mixing-DAC in baseband mode is measured. For this measurement, the LO driver is configured in static state, hence the mixer transistors only acts as a cascode and do not mix.

The baseband mode of the Mixing-DAC is not the main operating mode and the design is not optimized for this operating mode. Therefore, the performance measurements at baseband are only informative. All measurements are done using a dual-tone signal, no separate single-tone signal is generated for SFDR measurements.

The sample rate is 1.5GSps and the input signal is a dual-tone signal at 155.0MHz and 155.1MHz. The output spectrum of the full Nyquist band is shown in Figure 12.6. The dual-tone SFDR is 68.1dBc with the HD2 being the highest spurious component. The spectrum of the reduced bandwidth is shown in Figure 12.7, where the dual-tone $\mathrm{SFDR_{RB}}$ in a 300MHz RB bandwidth, excluding the IMD tones, is 87.1dBc. Further zooming in, the spectrum around the signal tones in Figure 12.8 shows that the worst case IMD is the IMD3 at -86.8dBc. The increase of the noise toward the two signal tones is due to phase noise of the spectrum analyzer.

A sweep over the input frequency shows that the performance is best at low frequencies and worsens for higher frequencies. The results of the input-frequency sweep is shown in Figure 12.9. For these simulations, a dual-tone input signal is used.

The results for the IMD is as expected by simulations. At low frequencies, the IMD is constant and is limited by the matching of the current sources. For higher frequencies, timing errors limit the performance, which results in a degrading IMD for increasing frequency.

The harmonic distortion strongly depends on the input frequency. The increase for the near-Nyquist frequency suggests that the error-source is in the baseband part of the converter. Measurements in the mix mode determine if that is the case, or if the error-source is output-frequency dependent, see Section 12.4.5.2 and Section 12.4.5.3.

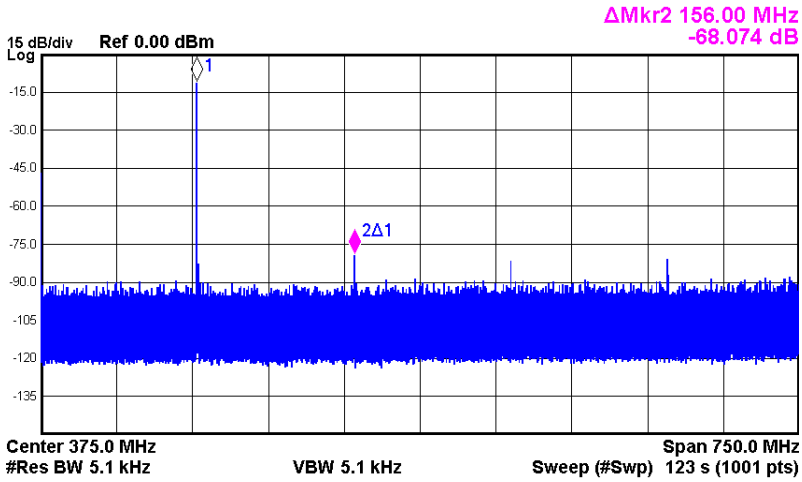


Figure 12.6: Spectrum of the full Nyquist band for a dual-tone input signal in baseband mode (no mixing)

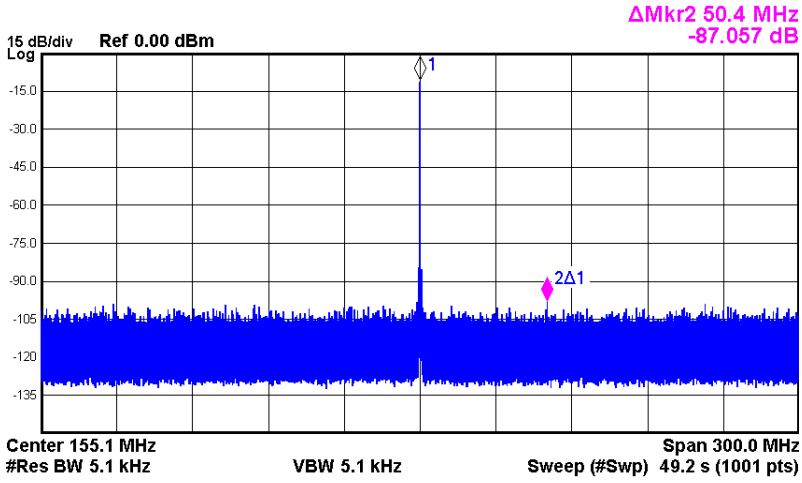


Figure 12.7: Spectrum of the 300MHz RB for a dual-tone input signal in baseband mode (no mixing)

The SFDR is mostly limited by the HD2. Only for frequencies below 100MHz other spurs limit the SFDR. The SFDR_{RB} for frequencies below RB/2 (=150MHz) are limited by the HD components. For higher frequencies, the degradation for increasing frequencies suggest that timing errors cause these spurious components.

The total current consumption is approximately 620mA from the 1.2V power supply and 130mA from the 3.3V power supply. Hence, the total power

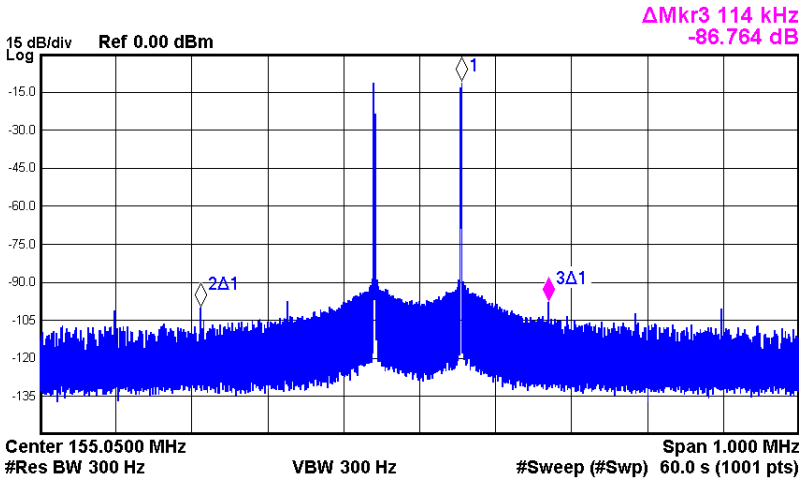


Figure 12.8: Spectrum of the dual-tone output signal in baseband mode (no mixing)

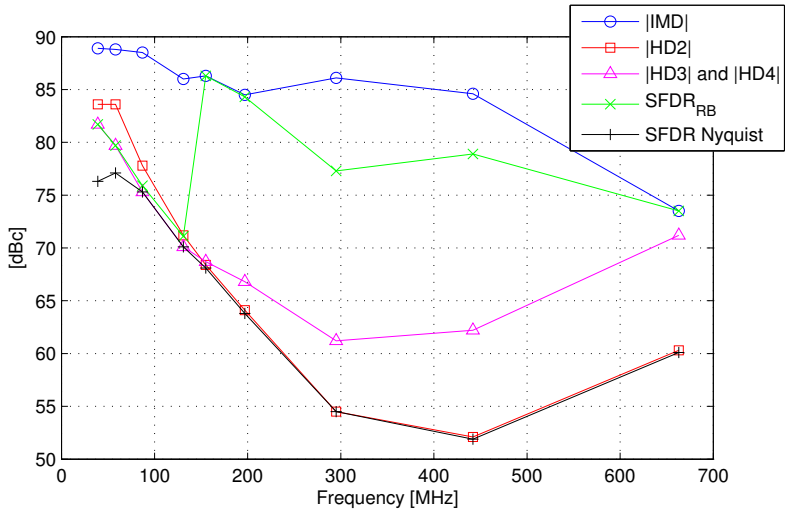


Figure 12.9: Dual-tone output spectrum in baseband mode (no mixing), F_S=1.5GHz, dual-tone SFDR&HD

consumption of the test chip is approximately 1.2W. This includes two Mixing-DAC cores and the digital signal processing. The power consumption of the analog circuitry is 710mW with two Mixing-DAC cores enabled and 380mW with only one Mixing-DAC core enabled. Since all circuitry in the Mixing-DAC cores is implemented with CML circuits, the current consumption is frequency independent. The same circuits are enabled for the baseband mode

and the mix mode, hence the power consumption in the mix mode is identical to the power consumption in baseband mode. An overview of the power consumption is given in Table 12.1.

Table 12.1: Power consumption of the dual-Mixing-DAC test chip

Part	**1.2V**	**3.3V**	**Power**
Digital circuits	415mA	0mA	498mW
Mixing-DAC cores	2x80mA	2x70mA	2x327mW
Auxiliary analog circuits	43mA	0mA	52mW
Total			**1.2W**

12.4 Mixing dynamic performance

When the mixer is enabled, the digital baseband signal is upconverted to the LO frequency. The spectrum of the output for F_S=1.5GSps, f_{LO}=3GHz and a single-tone input signal at f_{in}=155MHz is shown in Figure 12.10. These results coincide with the simulation results of Figure 11.22, although with different frequencies. Hence the test chip implements the function of a Mixing-DAC. However, there are number of small differences in the spectra. The LO leakage in the measurements is higher than the simulation results. This can be due to coupling in the measurement setup or coupling on-chip at a level which is not extracted for capacitive coupling. The output power is lower than the simulated value, which is further discussed in Section 12.4.2.

Measurements at RF frequencies are sensitive to external disturbances, see Section 12.4.1. The output power is discussed in Section 12.4.2. Optimization of the Mixing-DAC settings and measurement setup results in improved performance, see Section 12.4.3 and Section 12.4.4 respectively. The resulting performance is discussed in Section 12.4.5.

12.4.1 External disturbances

When measuring at RF frequencies, signals from RF transmitters couple to the measurement setup and can cause spurious signals in the measured signal. For example, when measuring around 1.85GHz, GSM transmitters close to that frequency directly couple to the measured output voltage. Figure 12.11 shows a measurement at 1.845GHz, with external disturbances at 1.855GHz and 1.875GHz.

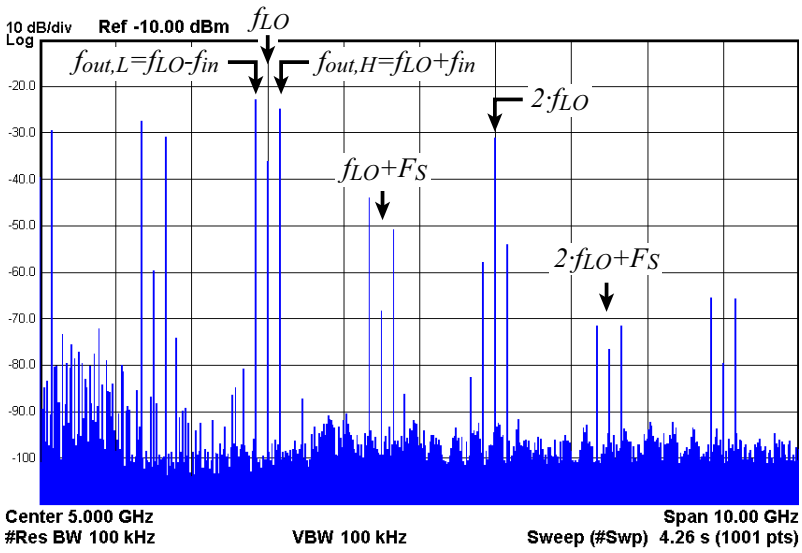


Figure 12.10: Output spectrum in mix-mode

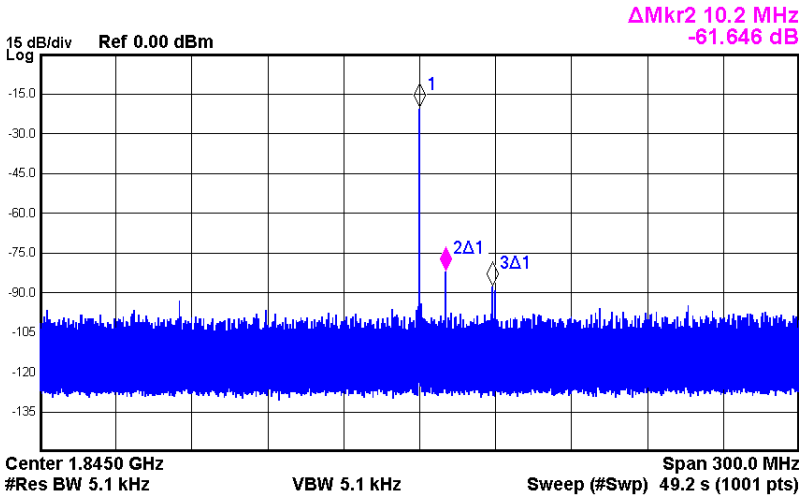


Figure 12.11: External interference due to GSM transmitter

Due to these external disturbances, a Faraday cage is used for the measurements at frequencies where other transmitters are active. Around 1.5GHz, no strong transmitters are active. Therefore, some of the measurements are executed around this frequency.

12.4.2 Output power

The output power of the measured Mixing-DAC is lower than the simulated values. The dependence of the measured output power on the output frequency is shown in Figure 12.12 for output frequencies of 0.3GHz to 5.8GHz. The value of the Mixing-DAC sample rate is limited. Therefore, to generate a wide-band signal at this wide range of output frequencies, multiple ratios between the sample rate F_S and the LO frequency f_{LO} are used: $f_{LO}= r{\cdot}F_S$, where $r \in \{0.5, 1, 2, 3, 4\}$. In other words, Figure 12.12 combines measurements with multiple ratios, as indicated at the top of the figure. For each region with a fixed r, the LO frequency is swept to generate multiple output frequencies, which consequently also sweeps the sample rate. The input frequency is fixed at f_{in}=155MHz.

The measured power is shown as P_{meas}. Both the output power of the low Nyquist band (at f_{LO}-f_{in}) and the high Nyquist band (at f_{LO}+f_{in}) are shown, i.e. P_{meas} *Low* and P_{meas} *High* respectively.

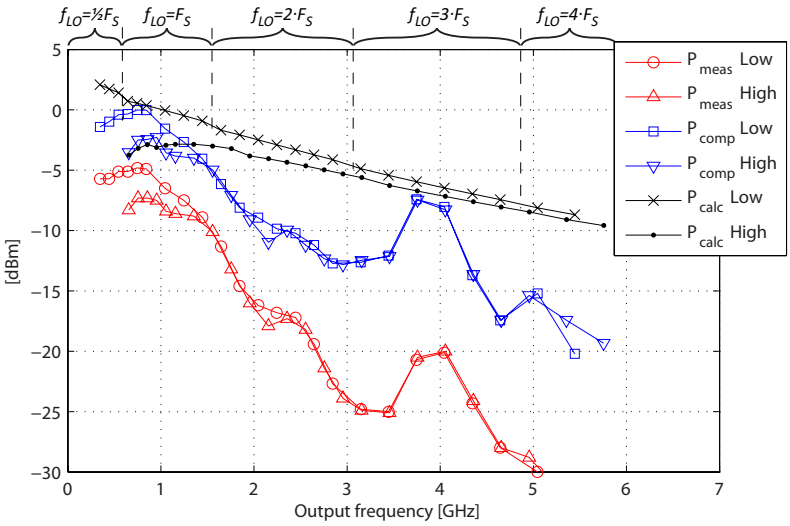


Figure 12.12: Dependence of the output power on the output frequency

Between the output of the Mixing-DAC and the spectrum analyzer, a number of components cause losses: capacitance of the tracks on the measurement board, transformers on the measurement board and the cable between the measurement board and the spectrum analyzer. The loss of these components is measured using a network analyzer. In Figure 12.12, the compensated output power is shown as P_{comp} for both the low and high Nyquist band.

The expected output power is shown in Figure 12.12 as P_{calc}. The expected output power is calculated using the known output current (20mA), the 50Ω differential effective load resistance, an estimated load capacitance of 1.5pF and the response of the zero-order-hold and mixing. Due to the zero-order-hold transfer characteristic of the DAC and mixing function, a sinc-shaped frequency-response is present in the expected output power. The relative frequency-response due to this sync-shape also causes the signal power in the Low and High Nyquist bands to be different. This effect is shown in Figure 12.13, where the frequency-response of the zero-order-hold and mixing function is shown for various ratios between F_S and f_{LO}. The asymmetry of the response is due to the mixing operation being a mixing operation with f_{LO} and -f_{LO}. Multiplying the sinc-shape of the DAC zero order hold with f_{LO} and -f_{LO} results in the asymmetric response.

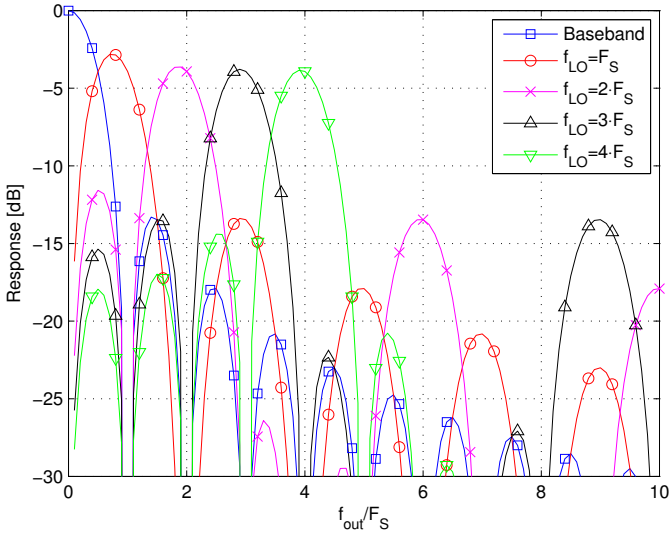


Figure 12.13: Mixing-DAC response due to zero-order-hold function

The compensated output power is close to the calculated output power for low frequencies and around 4 GHz. The difference at other frequencies is expected to be caused by frequency-dependent reflections on the PCB and in the measurement setup due to imperfect impedance matching. The output power can be improved in a redesign of the Mixing-DAC, where extra attention is paid to the output impedance. An option for a redesign is to position some of the termination resistances on-chip, thereby eliminating some of the negative effects of the bondwires.

12.4.3 Biasing optimization

The performance of the Mixing-DAC depends on the settings of the bias currents and voltages. The biasing setting which are optimized, are:

- LO driver tail current I_{LO}
- Data driver tail current I_{data}
- LO driver supply voltage V_{loHigh}
- Elevated bulk voltage $V_{bulkHigh}$
- Mixer bleed current $I_{bleed,mix}$
- Output-cascode bleed current $I_{bleed,oc}$

Main optimization targets are IMD, SFDR_{RB} and SFDR. Optimizing for these different optimization targets often results in different optimal bias settings. For instance, for a good IMD, the I_{data} should remain at the nominal value, while the SFDR improves when I_{data} is decreased. The final biasing value is a trade-off between the optimal IMD, SFDR_{RB} and SFDR.

12.4.4 Clock - LO phase optimization

The phase between the DAC sample clock and the *LO* signal influences the spectral purity. Figure 12.14 shows a simulation result for changing the phase of the *LO* signal at f_{LO}=4GHz, F_S=2GSps and f_{in}=155MHz.

In these simulations, the HD3 limits the SFDR. It can be seen that both the IMD3 and the dual-tone SFDR can vary 10dB depending on the phase. There is a repetition with 180° since the alignment of transitions is determining the performance, and the actual direction of the transition is less important due to the differential structure of the Mixing-DAC. The phases for the optimal IMD3 of the high Nyquist band and the low Nyquist band are 90° apart. Also the phases of the optimal SFDR in both Nyquist bands are 90° apart. The phases for the optimal SFDR and IMD3 in the high Nyquist band coincide. However, the phases for the optimal SFDR and IMD are in anti phase for the low Nyquist band.

The measured performance also shows a dependence on the phase between the clock and LO signal. The dependence of the IMD and the HD on the clock-LO phase for f_{LO}=1.5GHz F_S=1.5GSps and f_{in}=155MHz is shown in Figure 12.15. The repetition with 180° is also present in these measurements. The main difference between the simulation results and these measurement results is that the phases of the optimal IMD and HD in the low Nyuist band are identical in the measurements, while they are in anti-phase in the simulations. The causes for this difference are unknown.

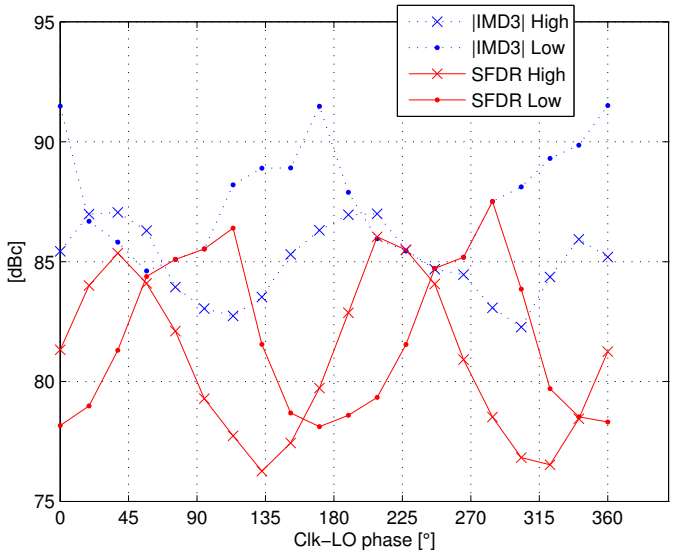


Figure 12.14: Simulated dependence of the spectral purity on the phase between the clock and the *LO* signal

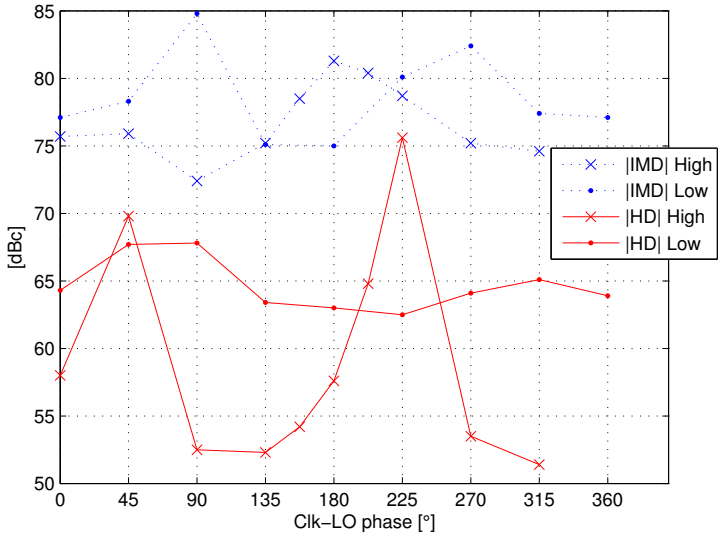


Figure 12.15: Measured dependence of the spectral purity on the phase between the clock and the *LO* signal

These measurements clearly show a strong dependence of the performance on the clock-LO phase. However, due to the different phase behavior of the equipment, cables, PCB tracks and transformers, externally controlling this phase is challenging. Therefore, in a redesign of the chip, an on-chip synchronization method would improve the stability of the measurement results. Since the frequencies of the sample clock and the LO signal have a well-defined ratio, an on-chip frequency divider or PLL is also an option worth investigating.

12.4.5 Dynamic performance

The linearity of the Mixing-DAC is assessed using sinusoidal signals. This section discusses the linearity at the typical configuration and for various values of the input frequency, sample rate and LO frequency.

12.4.5.1 Typical frequency

There are numerous wireless standards which use frequencies around 1.9GHz, e.g. GSM, 3G, 4G. Therefore, the linearity of the Mixing-DAC around that frequency is important. For an output frequency of 1.905GHz, the Mixing-DAC uses f_{LO}=1.75GHz, F_S=1.75GSps and f_{in}=155MHz. The output in the high Nyquist band is used.

The spectrum of the full Nyquist band is shown in Figure 12.16, where the input signal is a single-tone signal. The power of the single-tone signal is -14.9dBm at the input of the spectrum analyzer. Correcting for the losses of the measurement setup, the signal power is calculated to be -8.0dBm at the output of the Mixing-DAC. The SFDR is 66.3dBc, limited by the HD2 component. The HD2 is expected to be caused by imperfect symmetry of the mixer layout in the output stage. The second largest spurious component is the HD3 at -69.7dBc.

The spectrum of the RB of 300MHz is shown in Figure 12.17, where the input signal is a single-tone signal. Since the HD2 component falls outside this RB, the SFDR_{RB} value of 75.1dBc is much better than the SFDR value. The SFDR_{RB} is limited by a spurious component at f_{LO}+F_S/8-f_{in}=1813.75MHz. Some of the digital circuits operate at F_S/8. Its disturbance on the power supply couples via the ESD circuits to the LO input, which causes this mixing product, see Section 11.6. Other spurious components are: f_{LO}+F_S/4-f_{in}=2032.5MHz (-78dBc), and HD12 at 1860MHz (-80dBc). When omitting the spurious components associated with the digital signal processing, the SFDR_{RB} is 80dBc.

The spectrum of a two-tone signal is shown in Figure 12.18. The IMD5 is

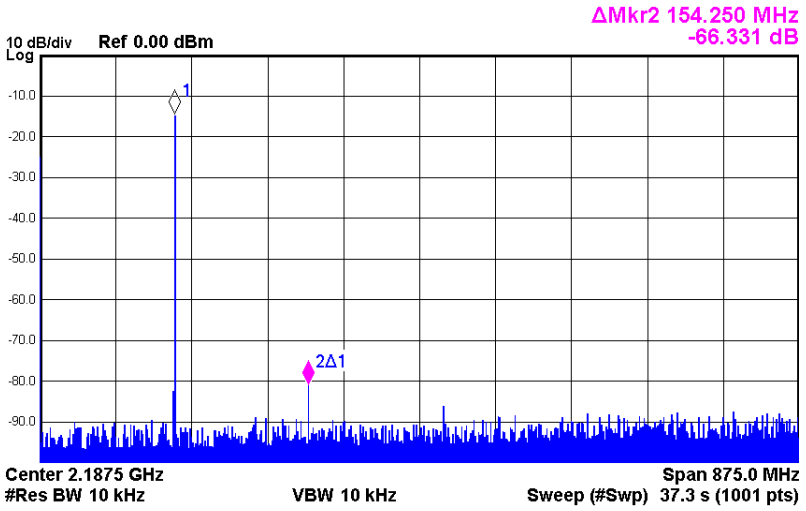


Figure 12.16: Spectrum of the full Nyquist band at f_{LO}=1.75GHz, F_S=1.75GSps and a single-tone signal at f_{in}=155MHz

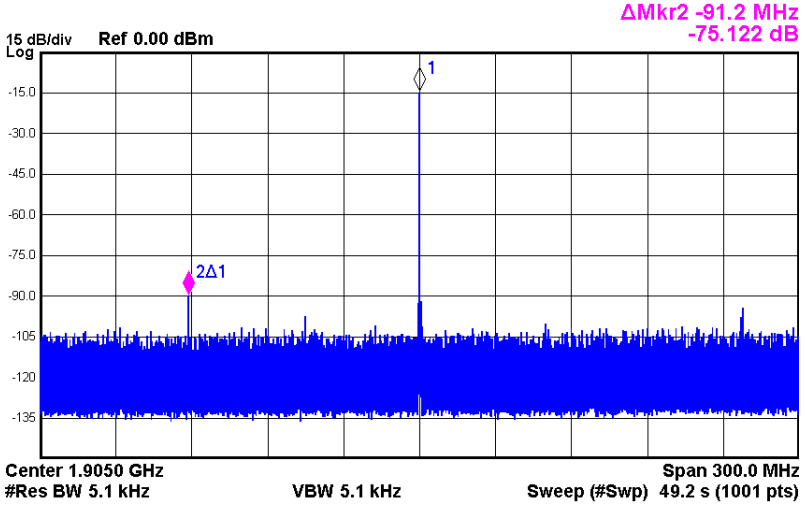


Figure 12.17: Spectrum of the 300MHz RB at f_{LO}=1.75GHz, F_S=1.75GSps and a single-tone signal at f_{in}=155MHz

the most dominant odd-order IMD at -83.9dBc. The dominance of the IMD5 over IMD3 suggests that mismatch errors cause these non-linear distortion. Also the relatively high HD12 in the SFDR_{RB} with respect to the simulation implies the dominance of mismatch errors. This is further discussed in

Section 12.4.5.3. The thermal noise power is -168dBm/Hz at 10MHz from the output frequency.

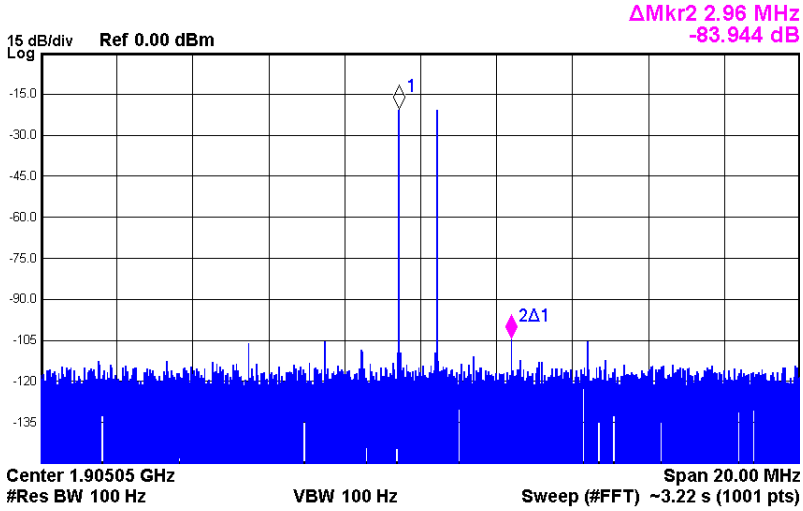


Figure 12.18: Spectrum around the output signal at f_{LO}=1.75GHz, F_S=1.75GSps and a dual-tone signal around f_{in}=155MHz

12.4.5.2 Input frequency dependence

Measuring at various input frequency values shows which part of the Mixing-DAC is limiting the performance. The measurement results for F_S=1.5GSps and f_{LO}=1.5GHz are shown in Figure 12.19. For low f_{in} values, the IMD is below -80dBc, the HD3 and HD4 are below -75dBc. For increasing f_{in}, the HD values degrade. This applies to both the high and low Nyquist band. Hence, the cause of the HD is in the baseband part of the Mixing-DAC, e.g. the Data switches or the capacitance at the drain of the Data switches. The IMD for f_{in}<150MHz depends more on the output frequency than on the f_{in} value. Hence, the cause for this non-linear distortion is in the RF part of the Mixing-DAC, e.g. the mismatch of the mixer switches or the parasitic capacitance at the source of the output cascode.

For the exemplary application of multicarrier GSM, the linearity at f_{LO}=1.5GHz is near the target -85dBc. However, to maintain this linearity, the input frequency should be limited to approximately 150MHz. These results clearly show that the proposed architecture achieves high linearity in a large bandwidth.

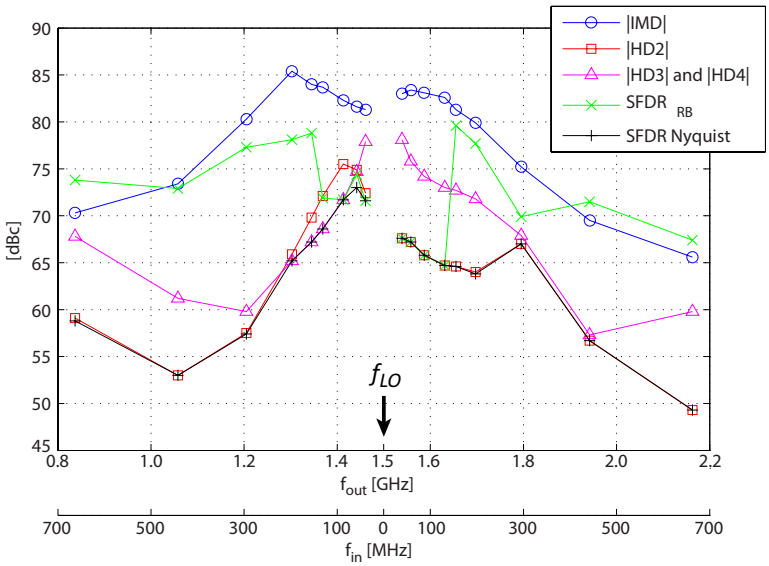


Figure 12.19: Sweep over the input frequency in mix mode, F_S=1.5GSps, f_{LO}=1.5GHz

12.4.5.3 Output frequency dependence

The flexibility of the Mixing-DAC architecture enables the generation of an RF output signal from baseband to multi-GHz frequencies. To demonstrate this capability, Figure 12.20 shows the performance for output frequencies of 1.1-5.3GHz. To cover this range, the ratio between F_S and f_{LO} should be between 1 and 4. The F_S is between 1.1GSps and 1.75GSps while the f_{LO} is 1.3-5.1GHz. The input frequency is always 155MHz. For each value of f_{LO}, the configuration of the data driver bias current and the LO driver bias current are altered in a range of 6% and 12% respectively for the best performance. For each data point, also the clock-LO phase is optimized.

The IMD and the SFDR_{RB} does not strongly depend on the output frequency for frequencies below 1.9GHz and 1.7GHz respectively. Hence, the error sources in the baseband part of the Mixing-DAC limit the linearity. For higher frequencies, the IMD and SFDR_{RB} depend on the output frequency. For these frequencies, the non-linearity is caused by error sources in the RF part of the Mixing-DAC. The SFDR is almost constant for f_{out}<4GHz, limited by the HD2, HD3 or HD4. These HD components are caused by effects in the baseband part of the Mixing-DAC. Above 4 GHz, both the HD spurs and the SFDR worsen, limited by error sources in the RF part of the converter. The peak in the HD2 value around 3.2GHz suggests that there are two HD2-

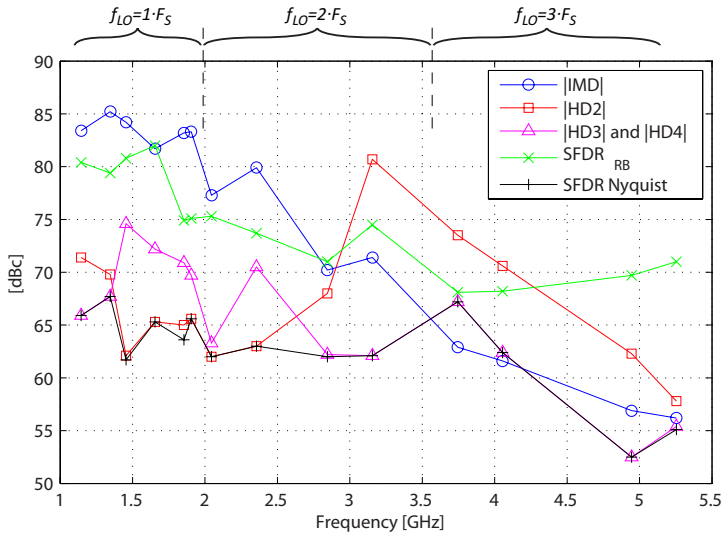


Figure 12.20: Sweep over the output frequency, F_S=1.1-1.75GSps, f_{LO}=1.3-5.1GHz, f_{in}=155MHz

generating effects, which can cancel one another.

To analyze which error-source causes the IMD to degrade for frequencies above 1.9GHz, a dither signal is added to the input data. A dither signal is a random signal, which has no correlation with the desired input signal. The goal of adding a dither signal is to randomize which current cells are used for a specific value of the desired dual-tone input signal. When there are cell-dependent error sources which cause non-linear distortion, the distortion is converted to noise. The amplitude of the dual-tone input signal is decreased by 6dB to allow for the dither signal with a total amplitude of -6dB$_{FS}$. The resulting IMD is shown in Figure 12.21. For a discussion on the relationship between the input-signal power and the linearity, see Chapter 9 and Section 12.4.5.4.

These measurement results show that the IMD can be better than -80dBc for frequencies between 1.9GHz and 3.5GHz when using dither. Note that the input signal effectively experiences a 15 bit converter due to the amplitude reduction of 6dB of the input signal. The IMD performance up to 3.0GHz is independent of the output frequency. From 2.5GHz up to the maximum measured frequency of 5.3Ghz, the dither IMD is more than 10dB better than the IMD without dither. These measurement results clearly demonstrate that the most dominant error source above 1.9GHz is a cell-dependent error source. Examples of this type of error source are:

- timing errors in the mixer;

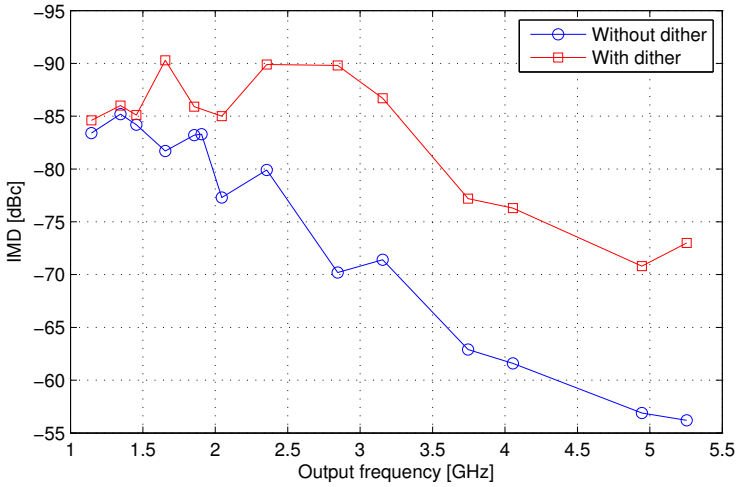


Figure 12.21: IMD with and without dither for various output frequencies

- timing errors in the LO distribution tree;
- timing errors in the output recombination tree.

It is unknown which of these error sources is the most dominant. These error-sources can be due to imperfect design or due to process variations. For errors due to imperfect design, e.g. timing errors in the distribution tree, a redesign can enable a solution. For errors due to process variation, e.g. timing errors due to mixer mismatch, a calibration method can be used to measure and correct the timing errors of the mixer. However, this requires the measurement accuracy of the timing-error measurement circuit to be in the order of 55fs, see Section 6.5. An exemplary applicable calibration method is the sort-and-combine calibration already present in the Mixing-DAC implementation.

For the exemplary application of multicarrier GSM, the IMD value is near the required -85dBc for output-frequency values up to 1.9GHz. However, if the cell-dependent error-source would be compensated, the IMD performance up to approximately 3.5GHz is satisfactory. The high IMD up to almost 4GHz closely matches the simulation results. The cell-dependent error-sources can be compensated by adding a dither signal to the input data or in a new implementation, e.g. by timing-error calibration of the RF part of the Mixing-DAC. However, measurements show that the absolute value of the Noise Spectral Density (NSD) (in dBm/Hz) degrades with roughly 6dB when adding dither. This additional noise is caused by the HD and IMD components which have been randomized and appear as noise.

The measured thermal NSD (without dither) for various output-frequency values is shown in Figure 12.22. For these measurements, an LNA is used between the output of the measurement board and the spectrum analyzer to reduce the impact of the spectrum-analyzer noise. Due to the low noise power and the large attenuation of the measurement setup, the noise of the measurement setup limits the measured noise above f_{out}=1.7GHz. The NSD up to 1.7GHz is -157dB$_{FS}$/Hz and it is expected that the NSD of the Mixing-DAC is identical for all other output frequency values. This NSD value is close to the required -162dB$_{FS}$/Hz for the exemplary application of multicarrier GSM.

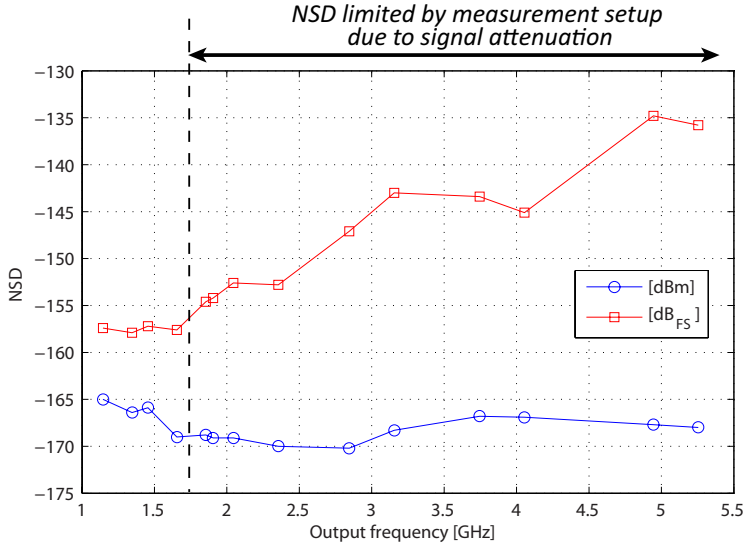


Figure 12.22: Thermal noise spectral density for various output-frequency values

12.4.5.4 Input-power dependence

Since multicarrier transmitters typically operate in back-off, the performance with a reduced input-signal power is important (see Chapter 9). There are two types of responses of the non-linearity to the value of the input-signal power. Decreasing the input-signal power improves the IMD if the dominant distortion is caused by a non-linear element, such as for instance a single transistor. The IMD degrades for decreasing input-signal power if the distortion is caused by cell-dependent effects.

The spectral purity for various values of the input-signal power is shown in Figure 12.23. In this measurement, F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$155MHz

and the high Nyquist band is used.

A lower input power means that less unary current cells are used, that the effective segmentation changes to less unary bits, and that the relative importance of the cell-dependent error sources increases. At f_{LO}=1.5GHz, the IMD and $SFDR_{RB}$ almost linearly depend on the input power, hence the dominant error source at this frequency is cell-dependent, as suggested in the previous section. The error-source which generates the HD is not the most dominant error-source at f_{LO}=1.5GHz. However, the degradation of the HD above $10dB_{FS}$ back-off shows that there are cell-dependent error sources which can influence the HD at the right conditions. This coincides with the conclusions in the previous section, where the HD degrades for high output frequency values, and with the discussion of the segmentation in Chapter 9.

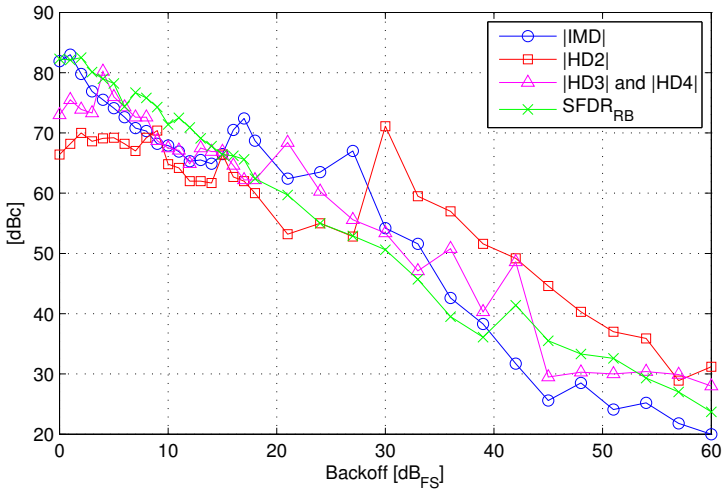


Figure 12.23: Dynamic performance for various values of the digital input power (F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$155MHz, high Nyquist band)

12.4.5.5 Temperature dependence

The measurement board including the data generation board was placed in an controlled-temperature environment to evaluate the performance over temperature. The results of an ambient temperature sweep from -35°C to 125°C are shown in Figure 12.24. In this measurement, F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$155MHz and the high Nyquist band is used.

There are no IMD results for temperatures above 95°C because the data-generation board failed to operate above these frequencies. However, because

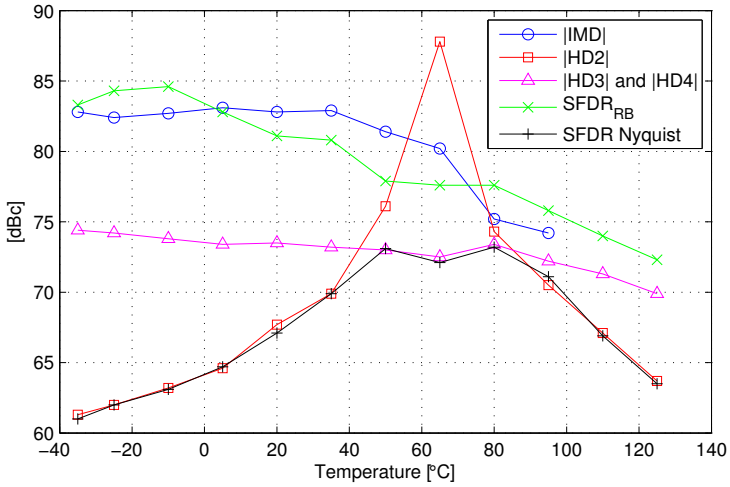


Figure 12.24: Dynamic performance for various values of the temperature (F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$155MHz, high Nyquist band)

the Mixing-DAC chip can independently generate single-tone signals, there are HD and SFDR results for the complete temperature range.

The IMD degradation above 40°C is due to the IMD3; the other IMD components slightly improve from -83dBc at -35°C to -88dBc at 80°C. The cause of the IMD other than the IMD3 is mismatch induced timing errors. Mismatch becomes smaller for higher temperatures, hence timing errors are smaller for higher temperature improving the IMD. The cause of the IMD3 degradation is expected to be transistors in the output stage of the Mixing-DAC leaving their saturation region. When the LO high voltage (V_{loHigh}) and the Data driver bias current are slightly increased, the IMD3 at 95°C improves from -74dBc to beyond -90dBc. The $\mathrm{SFDR_{RB}}$ is expected to also suffer from this transistor not being in saturation.

The shape of the HD2 curve suggest that there are two HD2 effects which cancel one another, which is also observed in Section 12.4.5.3. The other HD components only weakly depend on the temperature.

The power consumption is almost independent of the temperature. The total current consumption varies less than 4% for the temperature range of -35°C to 80°C.

12.4.5.6 Multiple samples

For analyzing the robustness of the Mixing-DAC performance, 15 samples are measured. All measurements use identical clock-LO phase and identical biasing configuration. The histogram of the IMD and the $\mathrm{SFDR_{RB}}$ is shown in Figure 12.25. In this measurement, F_S=1.5GSps, f_{LO}=1.5GHz, f_{in}=155MHz and the high Nyquist band is used.

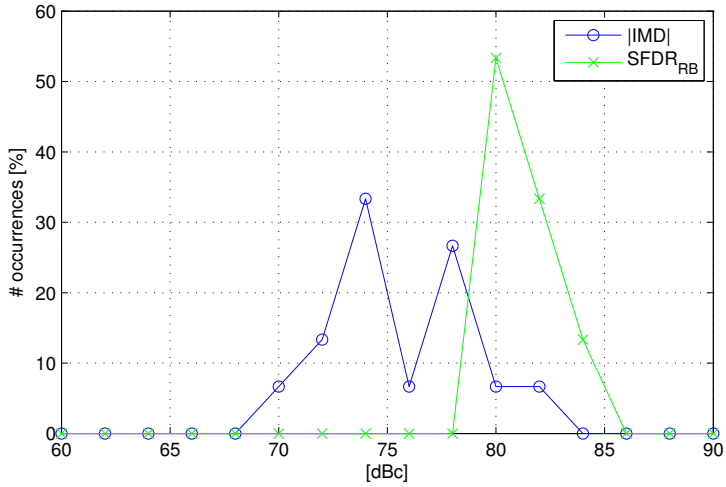


Figure 12.25: Histogram of |IMD| and $\mathrm{SFDR_{RB}}$ for 15 samples with identical configuration (F_S=1.5GSps, f_{LO}=1.5GHz, f_{in}=155MHz, high Nyquist band)

The performance of the elaborately discussed sample (#5) is: IMD=-82dBc and $\mathrm{SFDR_{RB}}$=82dBc. The median of the 15 samples are IMD=-75dBc and $\mathrm{SFDR_{RB}}$=81dBc. Sample #5 has an average $\mathrm{SFDR_{RB}}$, but it is the best sample with respect to its IMD. A possible cause of this single good IMD for sample #5 is that the clock-LO phase and the biasing configuration is optimized for this specific sample. However, when applying the same optimization method to another sample (#12), the IMD3 only improves slightly, from -74dBc to -76dBc, which is worse than the original sample #5. But the IMD5, HD2, HD3 and HD4 of sample #12 are similar or better than sample #5. Timing errors due to mismatch do not cause this worse IMD3 because then also the IMD5 would be worse, which is not the case. However, the determination of the reason for the worse IMD3 requires further investigation.

The histogram of the LO leakage is shown in Figure 12.26. It can be observed that the chips have two discrete values of the LO leakage: -22dBm

or around -51dBm. There is a large correlation between the LO leakage value and the value of the HD2 and HD4 in each sample. Hence, one of the causes for the LO leakage is an unbalance in the differential signals. The other cause for a high LO leakage is expected to be the calibration algorithm. The Mixing-DAC contains a number of redundant current cells such that the calibration algorithm can select the current cells with the best behavior, as discussed in Section 11.2 and Section 12.2.3. The floorplan of the output stage incorporates inversely polarization of half of the current cells, as discussed in Section 11.3.2.1. This inversion of the polarization is done by connecting the LO tree with inverse polarity to the mixer in the mirrored current cells. When the calibration algorithm selects an equal number of inversely polarized and straight current cells, the LO leakage of those two types of current cells cancel one another. This results in a low LO leakage. When the number of the two types of current cells are not equal, the LO leakage is not canceled and a high LO leakage is observed.

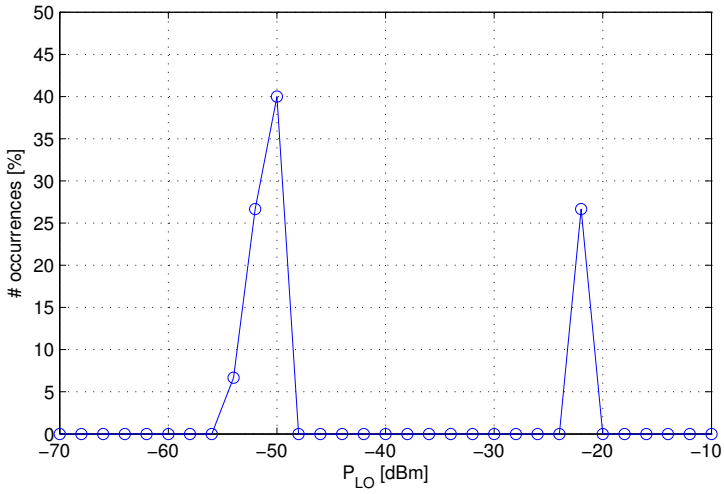


Figure 12.26: Histogram of LO leakage for 15 samples with identical configuration (F_S=1.5GSps, f_{LO}=1.5GHz, f_{in}=155MHz, high Nyquist band)

12.5 Radio signals

The measurement of real radio signals shows the usability of the Mixing-DAC for transmitters. GSM signals have a relatively small bandwidth, but require a high spectral purity. WCDMA and LTE are standards which require

more signal bandwidth, especially in a multicarrier setup. However, the required spectral purity is lower than that of GSM. For all radio standards, the required spurious-component free bandwidth is large.

The typical full-scale output current of the Mixing-DAC is 20mA, but it is programmable up to 51mA. For the single-carrier radio signals, the noise of the Mixing-DAC and the measurement setup limits the performance. Therefore, configuring the Mixing-DAC for a higher output power at the expense of linearity results in a better ACLR (Adjacent Channel Leakage Ratio). For multi-carrier radio signals, intermodulation products can limit the ACLR and hence the linearity is more important.

12.5.1 Multicarrier intermodulation

To demonstrate the excellent intermodulation performance of the Mixing-DAC, a 13-tone signal is measured at 2.0GHz output. The measured spectrum is shown in Figure 12.27. The reason for the low level of the intermodulation spurs is due to the 13 tones acting as a sort of dithering signal for the other tones, thereby spreading the energy of the distortion spurs (see Section 12.4.5.3). In this figure, there is a spur at $f_{LO}+F_S/8$ (=1.97GHz) present, which is masked by one of the signal tones. Since the clock-related spurs are not caused by an error in the Mixing-DAC core but are caused by the digital circuits, these clock-related spurs are not relevant. The $\mathrm{SFDR}_{\mathrm{RBi}}$n a 300MHz bandwidth, excluding the clock spur, is 81dBc. This shows that the linearity of the Mixing-DAC is sufficient to accommodate multicarrier signals without being limited by intermodulation of the carriers.

12.5.2 GSM

A single-carrier GSM signal is shown in Figure 12.28, together with a part of the GSM spectral mask. Figure 12.29 shows the same GSM signal with the remaining part of the GSM mask. The validation of conformance to the GSM mask is split in these two parts since the spectrum analyzer can only handle a limited number of different levels in the spectral mask. These measurements use an LNA to lower the impact of the spectrum-analyzer noise. The GSM signal satisfies the spectral mask up to ±20MHz from the carrier. This validates the excellent phase noise and thermal noise, which are sufficiently low to satisfy the single-carrier GSM requirements. At more than 20MHz from the carrier, various spurious components violate the spectral mask. However, most of these spurs are also present when the Mixing-DAC is idle, and hence are expected to be external disturbances coupling to the measurement setup.

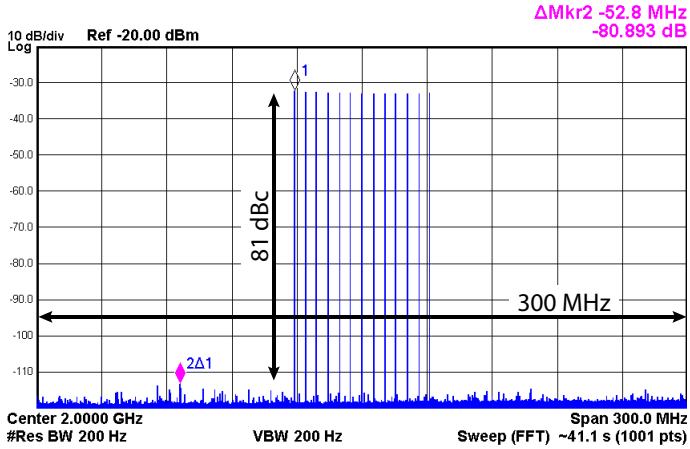
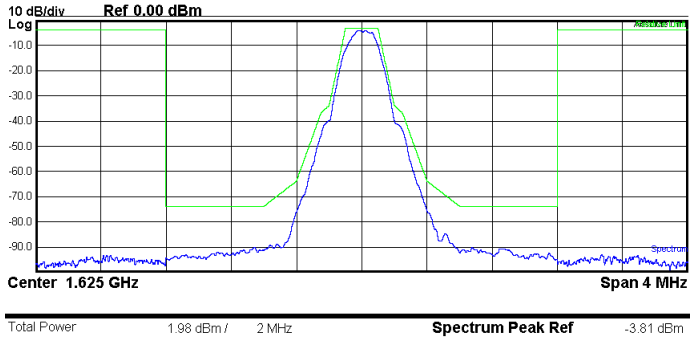


Figure 12.27: 13-tone output signal demonstrates low intermodulation (f_{LO}=1.75GHz, F_S=1.75GSps, and a 13-tone signal around f_{in}=250MHz, high Nyquist band)



Start Freq	Stop Freq	Integ BW	dB	Lower ΔLim(dB)	Freq (Hz)	<- Peak -> dB	Upper ΔLim(dB)	Freq (Hz)
0.0 Hz	100.0 kHz	30.00 kHz	-0.18	(-0.68)	-20.00 k	-0.37	(-0.87)	24.00 k
100.0 kHz	200.0 kHz	30.00 kHz	-16.04	(-5.56)	-136.0 k	-18.07	(-3.93)	148.0 k
200.0 kHz	250.0 kHz	30.00 kHz	-36.23	(-5.87)	-206.0 k	-35.91	(-5.91)	200.0 k
250.0 kHz	400.0 kHz	30.00 kHz	-41.75	(-8.75)	-250.0 k	-40.42	(-6.70)	254.0 k
400.0 kHz	600.0 kHz	30.00 kHz	-72.33	(-12.33)	-400.0 k	-71.84	(-11.84)	400.0 k
600.0 kHz	1.200 MHz	30.00 kHz	-86.35	(-16.35)	-658.0 k	-86.36	(-16.36)	678.0 k

Figure 12.28: GSM signal at 1.625GHz and GSM mask close to the signal (F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$125MHz, high Nyquist band)

The equivalent NSD at 20MHz from the GSM carrier in Figure 12.29 is calculated to be -141dB$_{FS}$. This does not correspond with the measured NSD of -157dB$_{FS}$ of Section 12.4.5.3. Possible reasons for this difference are in the spectrum analyzer. The attenuation of the spectrum analyzer is 14dB to prevent non-linear distortion of the spectrum analyzer to limit the GSM measurement. This increases the relative weight of the noise of the spectrum

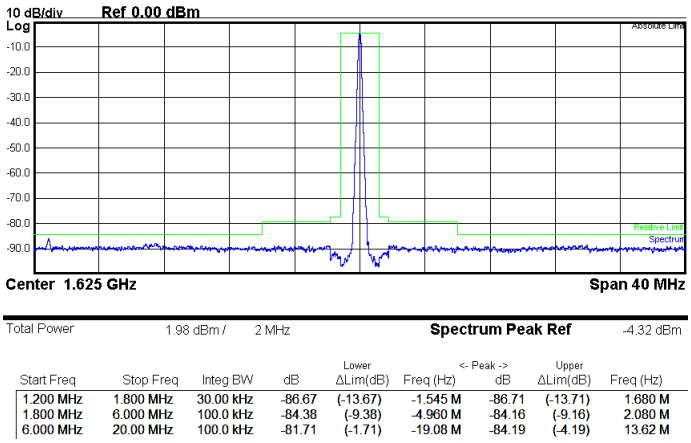


Figure 12.29: GSM signal at 1.625GHz and GSM mask far away from the signal (F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$125MHz, high Nyquist band)

analyzer. Furthermore, the settings of the spectrum analyzer when measuring the GSM signal are optimized for dynamic range and linearity and not for low noise. Finally, the phase noise of the spectrum analyzer is -145dBc at 10MHz, which is close to the calculated -141dB$_{\mathrm{FS}}$ noise floor.

A 3-carrier GSM signal is shown in Figure 12.30. Since the noise floor is much higher than expected from the earlier measured NSD of Section 12.4.5.3, the noise violates the spectral mask. At the frequencies of the IMD3 of the GSM carriers, slight increase in noise can be observed due to the limited IMD3 of the Mixing-DAC.

12.5.3 ACLR of WCDMA and LTE

The measurement of the ACLR of WCDMA and LTE signals is limited by the noise of the measurement setup. Therefore, for most ACLR measurements the output current is increased typically to 38mA. This improves the ratio between the output-signal power and the noise floor, thereby increasing the ACLR. Although increasing the output current reduces the linearity, it usually does not degrade the ACLR since the ACLR is limited by noise and not by non-linearity.

The spectrum of a 1-channel LTE signal is shown in Figure 12.31. The peak-to-average ratio of the LTE signal is 11dB. Therefore the output power is 11dB lower than the maximum single-tone output power to prevent clipping. The measured ACLR is -69dBc for f_{out}=2GHz. Since the output power increases for lower frequencies, the ACLR for lower frequencies is better.

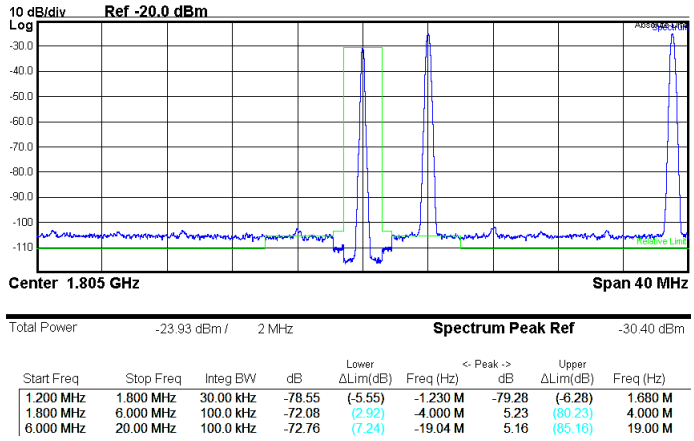


Figure 12.30: Multicarrier GSM signal at 1.805GHz to 1.824GHz (F_S=1.0GSps, f_{LO}=2.0GHz, $f_{in=}$176-195MHz, low Nyquist band)

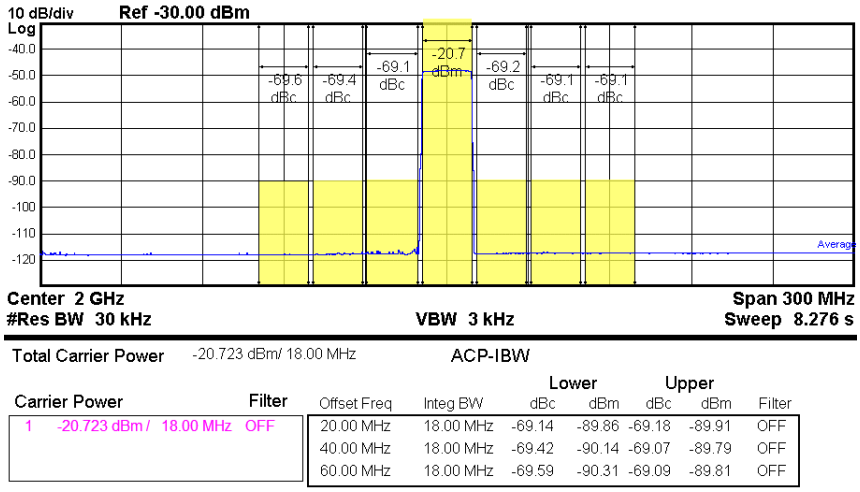


Figure 12.31: Single-channel ACLR of a LTE signal at 2.0GHz (F_S=1.75GSps, f_{LO}=1.75GHz, f_{in}=250MHz, high Nyquist band)

A 4-channel LTE signal is shown in Figure 12.32. Since the carriers add up in amplitude, the output power is 12dB lower than the power of the 1-channel signal. To maximize the signal to noise ratio, an LNA is used in the measurement setup to amplify the input signal of the spectrum analyzer. Since the ACLR is limited by the noise, the 4-channel ACLR of -58dBc is approximately 12dB lower than the 1-channel LTE signal.

The LTE ACLR at 4.1GHz is -73dBc, see Figure 12.33. This ACLR similar

to the ACLR at 2GHz since the output power at 4GHz is similar to the 2GHz output power, see Section 12.2.2.

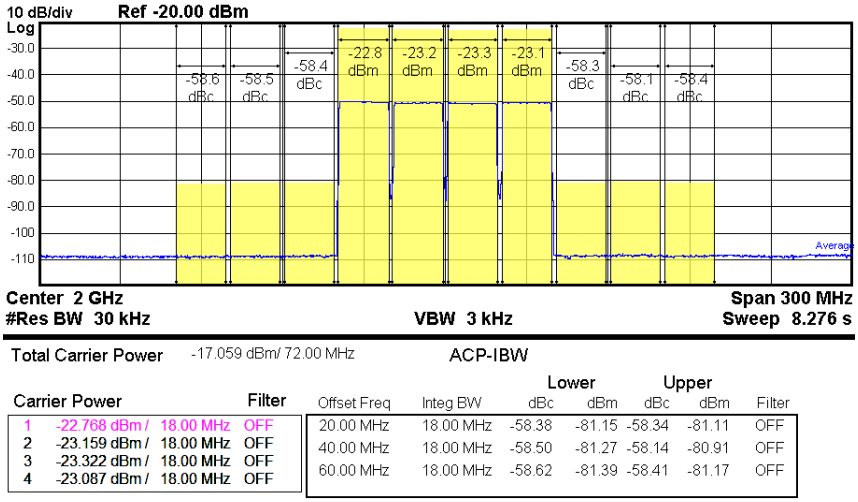


Figure 12.32: 4-channel ACLR of a LTE signal at 2.0GHz, measured with LNA (F_S=1.75GSps, f_{LO}=1.75GHz, f_{in}=250MHz, high Nyquist band)

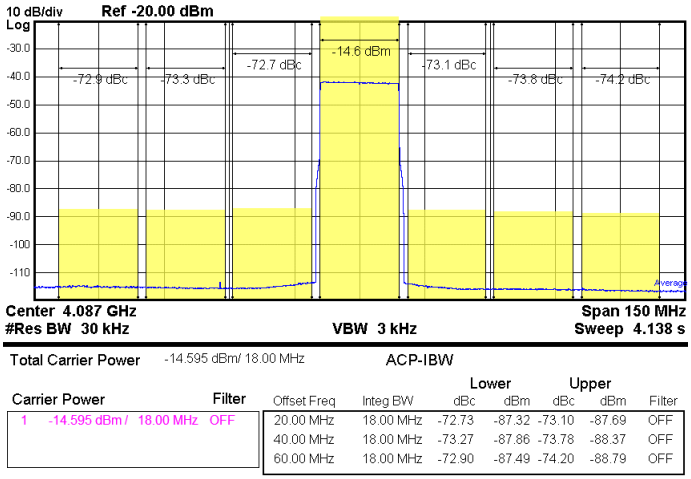


Figure 12.33: Single-channel ACLR of a LTE signal at 4.1GHz (F_S=0.983GSps, f_{LO}=3.932GHz, f_{in}=155MHz, high Nyquist band)

The ACLR dependence on the input frequency is shown in Figure 12.34. By choosing a high f_{in}, the distance of the output frequency to the LO leakage

or signal images is increased. This allows for a wider or less-steep output filter.

The LTE ACLR is limited by the noise floor. Since the output power decreases for increasing f_{in}, the ACLR also decreases slightly. The higher ACLR at 2.35GHz is due to the HD2 falling inside the measurement band.

The ACLR of the WCDMA signal is better than that of LTE since the bandwidth of the ACLR channel is lower, integrating less noise in one channel. The WCDMA ACLR in the first neighboring channel is the highest, since it also contains intermodulation of the signal channel. The linearity of the converter is limited due to the increased output current.

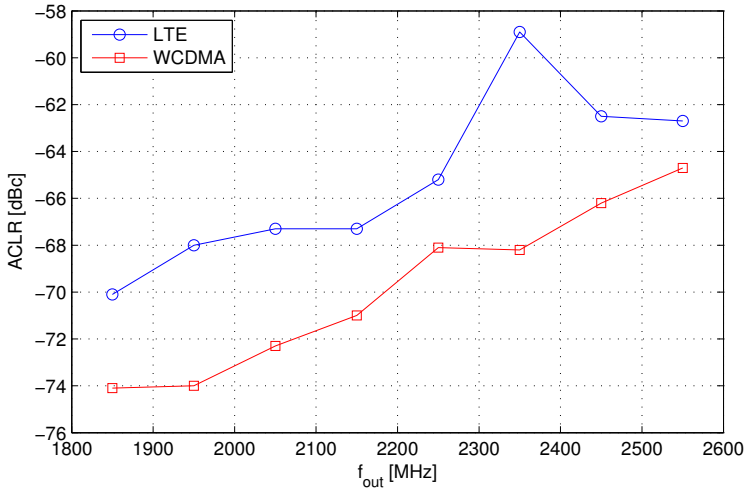


Figure 12.34: Single-channel ACLR of a WCDMA signal and aLTE signal for various values of the output frequency(F_S=1.75GSps, f_{LO}=1.75GHz, high Nyquist band)

12.6 I/Q signaling

The measurement board also contains an option to combine the outputs of the two Mixing-DAC cores. When these two Mixing-DAC cores are used in an I/Q configuration, cancellation of the output signal in one of the Nyquist bands can be achieved. Without compensation of the mismatch between the two Mixing-DACs, the combined output spectrum contains image leakage, see Figure 12.35. The output signal also contains LO leakage. In this measurement, F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$155MHz.

The image leakage is approximately -27dBc, which is much worse than the image leakage of a typical I/Q mixer. This high image leakage is mainly

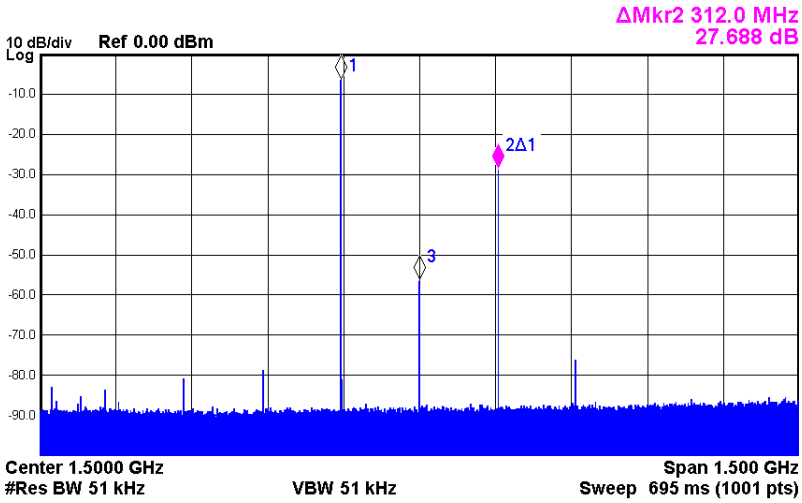


Figure 12.35: I/Q configuration (F_S=1.5GSps, f_{LO}=1.5GHz, $f_{in=}$155MHz)

caused by the I/Q combination transformer, which has amplitude and phase unbalance. A transformer amplitude unbalance of 0.4dB already causes an image leakage of more than -27dBc. However, the DSP in the digital part of the chip contains gain correction for the I/Q channels. Phase correction can be applied by changing the phase of the LO input signals. Tuning these parameters, the image rejection can be optimized. Also the LO leakage can be compensated by adding DC offset to the digital input data, which is also enabled by the on-chip DSP. The results of manual tuning is shown in Figure 12.36. The image leakage is -83dBc, 56dB better than the original value. The LO leakage is -91dBm=-84dBc, 35dB better than the original value. The tuning can be automatized, as is done in typical high performance transmitters.

The high Nyquist band can also be selected by changing the phase of the LO signal. The optimized image rejection is 69dB while the optimized LO leakage is -85dBm (=-73dBc).

The sensitivity of the image leakage to the phase of the LO signal is high. When the LO phase changes 0.5ps, which is 0.27° at 1.5GHz, the image leakage of the low Nyquist band increases with 10dB, from -83dBc to -73dBc. However, a more balanced recombination method than the transformer will give a better initial image rejection and will consequently result in a lower sensitivity to an LO-phase error.

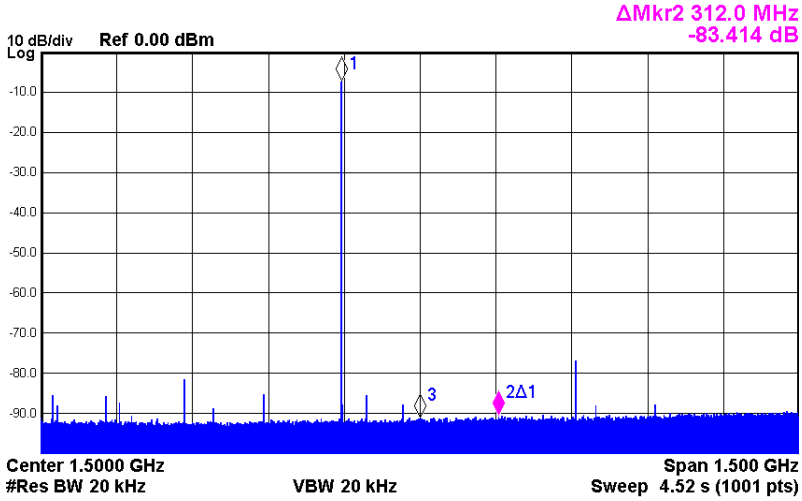


Figure 12.36: I/Q configuration with gain/phase mismatch compensation and LO leakage compensation (F_S=1.75GSps, f_{LO}=1.75GHz, $f_{in=}$155MHz)

12.7 Comparison with the state-of-the-art

An overview of the performance of the state-of-the-art DACs, mixers and Mixing-DACs is discussed in Section 2.7. A comparison of the performance of this work with the performance of the state-of-the-art solutions is given in Figure 12.37 and Figure 12.38 for the IMD and SFDR respectively. The references of the state-of-the-art data points are given in Section 2.7.

The IMD, SFDR and SFDR_{RB} of this work are better than or similar to that of the referenced publications for all measured frequencies, see also Section 2.7. The IMD is at least 10dB better and the SFDR_{RB} is at least 5dB better, while measuring in a larger RB.

The proposed Mixing-DAC is specifically aimed at achieving high linearity. Other publications make architecture choices which degrade the performance. The closest IMD is achieved by [8,9]. This is a GaAs implementation without an output cascode (mixer modulation due to large output voltage swing), without current source cascode (disturbance at switching of *Data* signal) and it suffers from mismatch in the current sources. Other publications either do not use an output cascode [5,10–13], do not use a current source cascode [5,10], use global mixing (low linearity) [12] or use mixing in the current source (no possibility for separate optimization of the 'reference' and 'mixing' function) [5, 10, 11, 13].

For the SFDR and SFDR_{RB}, the same limitations apply. Architectures

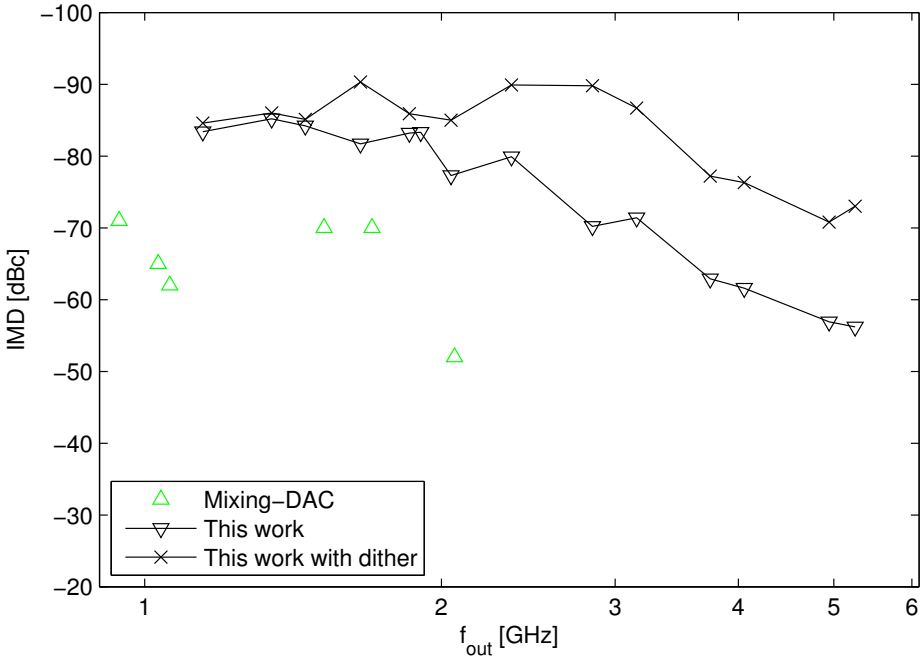


Figure 12.37: Overview of the IMD of state-of-the-art Mixing-DAC publications and this work

which come close to the measured SFDR [17–22] use separate transistors for the main functions of the output stage (see Section 11.3.1), although an output cascode or current source cascode is usually omitted, which reduces the linearity. The $\mathrm{SFDR_{RB}}$ of the referenced publications is generally achieved in a very small RB of less than 20MHz. Only [21, 22] measures in a larger RB of 200MHz, but achieves good SFDR and $\mathrm{SFDR_{RB}}$ by using a output bandpass filter to eliminate harmonic distortion.

A comparison of the performance of the Mixing-DAC test chip with the best competitors is given in Table 12.2. The performance of this work is given for the frequency range, $f_{out} \leqslant 1.9\mathrm{GHz}$ and for the output frequency of 4.1GHz since the performance at those frequencies is typical.

The comparison of the Mixing-DAC with the traditional DAC-mixer combination is crucial in assessing the usability of the Mixing-DAC as a replacement of the separate DAC and mixer in transmitters. There are two main comparison points: linearity and power consumption. The presented Mixing-DAC is compared with a state-of-the-art highly linear mixer which is commercially available, the LT5579 [15]

Table 12.2: Summary and comparison

	This work	[9]	[10]	[20]	[22]
Technology	**65nm CMOS**	80GHz f_T GaAs	180nm CMOS	130nm CMOS	130nm CMOS
Core area	1.6mm^2	3.2mm^2	-	1mm^2	**0.7mm^2**
Resolution	**16bit**	12bit	3bit ($\Delta\Sigma$)	10bit	3bit ($\Delta\Sigma$)
Max. sample rate	1.75GSps	1.6GSps	0.51GSps	0.15GSps	**2.63GSps**
Max. effective signal bandwidth	**875MHz**	800MHz	30MHz	75MHz	300MHz
Max. LO frequency	5.1GHz	1.6GHz	1.03GHz	1.9GHz	**5.25GHz**
Max. outputt frequency	**5.26GHz**	2.4GHz	0.94GHz	1.92GHz	**5.26GHz**
f_{out}	$\leqslant$1.9GHz	4.1GHz	1.7GHz	0.94GHz	1.92GHz	5.26GHz
Core power consumption	380mW	380mW	1200mW	-	**92mW**	187mW
IMD	< **-82dBc**	-62dBc	-70dBc	-71dBc	-	-
SFDR Nyquist	> 62dBc	**63dBc**	57dBc	-	50dBc	52dBc
$SFDR_{RB}$ @ RB	> **75dBc**	68dBc	-	75dBc	-	52dBc
	300MHz	300MHz	-	17.5MHz	-	200MHz
NSD	< -165dBm/Hz	**-167dBm/Hz**	-	-	-146dBm/Hz	-
1-ch. ACLR: LTE	< -69dBc	**-73dBc**	-	-	-	-
1-ch. ACLR WCDMA	< -74dBc	**-77dBc**	-	-	-58dBc	-

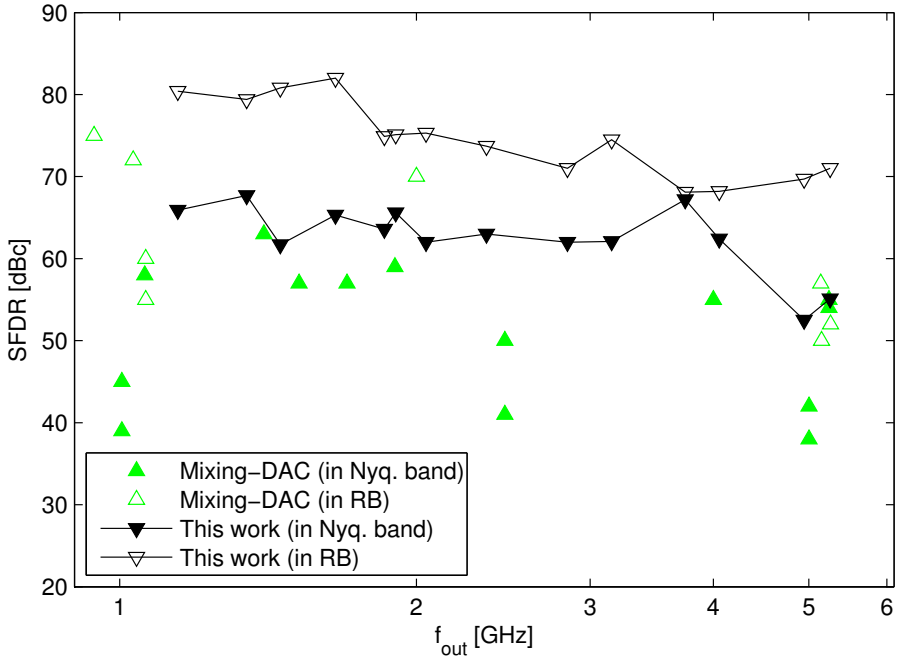


Figure 12.38: Overview of the SFDR of state-of-the-art Mixing-DAC publications and this work

The output power of the Mixing-DAC at 1.75GHz and 2.14GHz is -7dBm and -10dBm and achieves -83dBc and -77dBc respectively. The OIP3 (third order output interception point) of the mixer at those frequencies is +29dBm and +27dBm respectively, leading to an IMD3 value of -84dBc and -86dBc respectively. This is less than 9dB better than the Mixing-DAC. However, when using dither, the IMD3 of the Mixing-DAC improves to -86dBc and -85dBc which is similar to the highly linear mixer. Hence, when counteracting the cell-dependent error sources, the Mixing-DAC achieves similar linearity to the highly linear mixer. If the output impedance of the Mixing-DAC would be less capacitive and thus the bandwidth of the output RC filter larger, it is expected that the IMD would be not degrade, which would improve the comparison with the traditional mixer.

For extending the baseband DAC with a mixing-function, the Mixing-DAC only requires 50mA more from the 3.3V power supply than the baseband DAC. The separate mixer requires 225mA from the 3.3V supply, which is more than 4 times more than the Mixing-DAC. Hence, the Mixing-DAC is a more power-efficient solution for highly linear transmitters than a separate mixer.

12.8 Conclusion

The chip implementation of the proposed Mixing-DAC architecture has been successfully measured. The performance depends on the biasing configuration and the clock-LO phase. The output power is attenuated by RC filtering at the output of the Mixing-DAC and by losses in the measurement setup.

Both in baseband mode and in mix mode, the target linearity of IMD<-80dBc is achieved. The IMD is approximately better than -80dBc up to 3.5GHz using a dithering signal in the input data. Without dithering, the IMD is better than -82dBc up to 1.9GHz. This shows that the linearity is limited by cell-dependent error sources. Clock-mixing spurs usually limit the $SFDR_{RB}$. At 1.9GHz, the clock-mixing spur is at -75dBc while the highest non-linearity spur is at -80dBc. The SFDR in the full Nyquist band is mostly limited by the HD2, which is expected to be generated by imbalance in the layout in the baseband part of the converter. The noise power of -168dBm/Hz at 1.9GHz is low enough to satisfy the challenging GSM spectral mask for a singe-carrier signal.

The IMD, SFDR and $SFDR_{RB}$ of the presented chip is similar or better than all state-of-the-art Mixing-DACs at the measured frequencies. The measurement results of the test chip demonstrates that the proposed Mixing-DAC architecture achieves both high linearity and large bandwidth at GHz carrier frequencies.

13 | General conclusions

In this chapter, general conclusions are drawn. For detailed conclusions, the reader is referred to the conclusions of the separate chapters.

A Mixing-DAC can be used to replace the DAC and Mixer of a traditional transmitter. Using a Mixing-DAC results in different architecture trade-offs than the ones that are available when just combining a DAC and mixer. These new architecture trade-offs enable a reduction of the cost and power consumption, while improving the linearity at high frequencies. One of the most challenging applications is a multicarrier transmitter, which requires high spectral purity in a wide band.

For the Mixing-DAC with high spectral purity in a wide band, an optimal architecture should be used. In this work, a systematic analysis and classification of various aspects of Mixing-DAC architectures are presented. The classification is a powerful tool to synthesize the best architecture in a structured way. The classification is used to synthesize a Mixing-DAC architecture with high spectral purity. This architecture can indeed achieve the desired high spectral purity. Characteristics of this architecture are: current-steering principle, Cartesian signaling, local mixing with local output cascodes, square-wave mixing, symmetric around zero signaling for the LO and data signal, fully differential, cascoded operations, and LO-gate transistor usage. Furthermore, it is also shown that using local output cascodes is more power efficient than using an output transformer.

The implementation of the architecture is challenging. The current cells in the output stage feature multiple cascoded functions, which are all implemented using thin-oxide devices. This leads to multiple cascoded thin-oxide devices in a limited supply voltage. The low supply voltage becomes increasingly limiting for process technologies with smaller feature size. It is shown that increasing the bulk voltage of some of the transistors enables raising the supply voltage without compromising the reliability. Finally, a DAC core is used which is calibrated for static and dynamic errors.

The measured linearity up to 1.9GHz is IMD<-82dBc, which is better than

the target IMD of -80dBc. The $SFDR_{RB}$ up to 1.9GHz is >75dBc. Above this frequency, the linearity decreases due to cell-dependent timing errors. Circumventing these error sources, e.g. by means of dithering, the linearity up to 3.5GHz is better than the target. This proves that cell-dependent timing errors are the most dominant error sources. The thermal noise power of -165dBm/Hz up to 1.9GHz is low enough to satisfy the challenging GSM spectral mask for a singe-carrier signal. The measured linearity, expressed in IMD and $SFDR_{RB,}$ is respectively 10dB and 5dB better than any published state-of-the-art implementation known to the author.

The answer to the research question is summarized as follows. A Mixing-DAC can indeed be used to generate wide-band signals with high spectral purity. This is argued and demonstrated with the chosen architecture and chip implementation. The most dominant spectral-purity limitations are: timing errors between current cells, coupling of the large output voltage swing to internal nodes and the non-linear output capacitance. The linearity that can be achieved with current process technologies, is: IMD<-82dBc and $SFDR_{RB}$>75dBc up to 1.9GHz with 65nm CMOS.

The presented architecture enables the advantages of Mixing-DACs to multicarrier transmitters.

14 | Recommendations

The presented research shows a Mixing-DAC architecture and implementation for high spectral purity and wide bandwidth. The results reveal new possibilities for further research.

- The dependence of the linearity on the phase relationship between clock and LO signal can be further analyzed. This can reveal if there is a universal optimal phase for all configurations. The controllability of the phase between the clock and LO signal would improve if both signals were to be derived on-chip from one single clock signal.
- The output power of the chip implementation decreases with increasing output frequency. This hampers the measured signal to noise ratio. Further research is needed to reduce the impact of the capacitive output impedance and thereby improve the output power for high frequencies.
- For higher frequencies, the cell-dependent timing errors limit the performance. Possible sources of these errors are: mixer mismatch between the current cells, or imperfect LO and output tree. Simulation of the tree structures with an EM simulator can reveal if the tree structures are indeed a source of timing errors. Improved design or a sensitive calibration loop can reduce the timing errors or their impact.
- In a typical application, I/Q combination of two Mixing-DACs will be used to eliminate one of the signal images. This I/Q combining is an excellent candidate for on-chip integration. This integration can be combined with an automatic calibration algorithm to improve the image rejection and LO leakage.
- The Mixing-DAC architecture can also be used to generate signals at much higher RF frequencies where the available bandwidth is very high; e.g., at 60GHz roughly 7GHz of bandwidth is available [80]. At higher frequencies, other considerations are important. The higher bandwidth requires a higher sample rate and the higher RF frequency can increase the importance of jitter.

Bibliography

[1] "Oxford dictionaries," Nov 2014. [Online]. Available: http://www.oxforddictionaries.com/

[2] *Digital cellular telecommunications system (Phase 2+); Radio transmission and reception (GSM 05.05 version 8.5.1 rel. 1999)*, ETSI.

[3] H. Van de Vel, J. Briaire, C. Bastiaansen, P. van Beek, G. Geelen, H. Gunnink, Y. Jin, M. Kaba, K. Luo, E. Paulus, B. Pham, W. Relyveld, and P. Zijlstra, "A 240mW 16b 3.2GS/s DAC in 65nm CMOS with <-80dBc IM3 up to 600MHz," in *Solid-State Circuits Conference, 2014 (ISSCC). Digest of Technical Papers. IEEE International*, Feb 2014.

[4] What can wideband RF bring for GSM? Huawei. Visited: 23-04-2014. [Online]. Available: http://www.huawei.com/ru/static/hw-081711.pdf

[5] S. Luschas, R. Schreier, and H. Lee, "A 942 MHz output, 17.5 MHz bandwidth, -70dBc IMD3 ΣΔ DAC," in *Custom Integrated Circuits Conference (CICC), 2003 IEEE*, Sept. 2003.

[6] S. Balasubramanian, S. Boumaiza, H. Sarbishaei, T. Quach, P. Orlando, J. Volakis, G. Creech, J. Wilson, and W. Khalil, "Ultimate transmission," *Microwave Magazine, IEEE*, 2012.

[7] G. Radulov, "Flexible and self-calibrating current-steering digital-to-analog converters," Ph.D. dissertation, Eindhoven University of Technology, 2010.

[8] M.J. Choe, K.H. Baek, and M. Teshome, "A 1.6-GS/s 12-bit return-to-zero GaAs RF DAC for multiple nyquist operation," *Solid-State Circuits, IEEE Journal of*, Dec. 2005.

[9] M.J. Choe, K.H. Baek, and M. Teshome, "A 1.6GS/s 12b return-to-zero GaAs RF DAC for multiple nyquist operation," in *Solid-State*

Circuits Conference, 2005 (ISSCC). Digest of Technical Papers. IEEE International, Feb. 2005.

[10] S. Luschas, R. Schreier, and H.S. Lee, "Radio frequency digital-to-analog converter," *Solid-State Circuits, IEEE Journal of*, Sept. 2004.

[11] S. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A bandpass ΔΣ RF-DAC with embedded FIR reconstruction filter," in *Solid-State Circuits Conference, 2006 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2006.

[12] S. Taleie, Y. Han, T. Copani, B. Bakkaloglu, and S. Kiaei, "A 0.18μm CMOS fully integrated RFDAC and VGA for WCDMA transmitters," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2008 IEEE*, June 2008.

[13] S. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A linear ΣΔ digital IF to RF DAC transmitter with embedded mixer," *Microwave Theory and Techniques, IEEE Transactions on*, May 2008.

[14] Datasheet ADL5365. Analog Devices. Visited: 23-8-2011. [Online]. Available: http://www.analog.com/static/imported-files/data_sheets/ADL5365.pdf

[15] Datasheet LT5579. Linear Technology. Visited: 24-8-2011. [Online]. Available: http://cds.linear.com/docs/Datasheet/5579fa.pdf

[16] Y.M. Greshishchev, D. Pollex, S.C. Wang, M. Besson, P. Flemeke, S. Szilagyi, J. Aguirre, C. Falt, N. Ben-Hamida, R. Gibbins, and P. Schvan, "a 56GS/s 6b DAC in 65nm CMOS with 256×6b memory," in *Solid-State Circuits Conference, 2011 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2011.

[17] M.J. Choe, K.J. Lee, M. Seo, and M. Teshome, "DC - 10GHz RF digital to analog converter," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011 IEEE*, 2011.

[18] P. Eloranta and P. Seppinen, "Direct-digital RF modulator IC in 0.13 μm CMOS for wide-band multi-radio applications," in *Solid-State Circuits Conference, 2005 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2005.

[19] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A multimode transmitter in 0.13 μm CMOS using direct-digital RF modulator," *Solid-State Circuits, IEEE Journal of*, Dec. 2007.

[20] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A WCDMA transmitter in 0.13μm CMOS using direct-digital RF modulator," in *Solid-State Circuits Conference, 2007 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2007.

[21] A. Jerng and C. Sodini, "A wideband ΔΣ digital-rf modulator with self-tuned RF bandpass reconstruction filter," in *Custom Integrated Circuits Conference (CICC), 2006 IEEE*, Sept. 2006.

[22] A. Jerng and C. Sodini, "A wideband ΔΣ digital-RF modulator for high data rate transmitters," *Solid-State Circuits, IEEE Journal of*, Aug. 2007.

[23] N. Zimmermann, "Design and implementation of a broadband RF-DAC transmitter for wireless communications," Ph.D. dissertation, Rheinisch-Westflischen Technischen Hochschule Aachen, 2011.

[24] B. Mohr, N. Zimmermann, B. Thiel, J. Mueller, Y. Wang, Y. Zhang, F. Lemke, R. Leys, S. Schenk, U. Bruening, R. Negra, and S. Heinen, "An RFDAC based reconfigurable multistandard transmitter in 65 nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*, June 2012.

[25] O. Wada, T.T. Ta, S. Tanifuji, S. Kameda, N. Suematsu, T. Takagi, and K. Tsubouchi, "5 GHz-band CMOS direct digital RF modulator using current-mode DAC with idle current," in *Wireless Symposium (IWS), 2013 IEEE International*, Apr. 2013.

[26] O. Wada, T.T. Ta, S. Tanifuji, S. Kameda, N. Suematsu, T. Takagi, and K. Tsubouchi, "5 GHz-band CMOS direct digital RF modulator using current-mode DAC," in *Microwave Conference Proceedings (APMC), 2012 Asia-Pacific*, Dec 2012.

[27] M. Park, "Time-based circuits for communication systems in advanced CMOS technology," Ph.D. dissertation, Massachusetts institute of technology, 2009.

[28] M. Alavi, R. Staszewski, L. de Vreede, A. Visweswaran, and J. Long, "All-digital RF I/Q modulator," *Microwave Theory and Techniques, IEEE Transactions on*, Nov. 2012.

[29] N. Zimmermann, B. Thiel, R. Negra, and S. Heinen, "System architecture of an RF-DAC based multistandard transmitter," in *Circuits and Systems, 2009. MWSCAS '09. 52nd IEEE International Midwest Symposium on*, Aug. 2009.

[30] N. Zimmermann, R. Negra, and S. Heinen, "Design of an RF-DAC in 65nm CMOS for multistandard, multimode transmitters," in *Radio-Frequency Integration Technology (RFIT) 2009, IEEE International Symposium on*, Apr. 2009.

[31] M. Park and M. Perrott, "A multiphase PWM RF modulator using a VCO-based opamp in 45nm CMOS," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2010 IEEE*, May 2010.

[32] P. Eloranta, "A 14-bit D/A-converter with digital calibration," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, May 2006.

[33] Z. Boos, A. Menkhoff, F. Kuttner, M. Schimper, J. Moreira, H. Geltinger, T. Gossmann, P. Pfann, A. Belitzer, and T. Bauernfeind, "A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode," in *Solid-State Circuits Conference, 2011 (ISSCC). Digest of Technical Papers. IEEE International*, 2011.

[34] V. Chironi, B. Debaillie, A. Baschirotto, J. Craninckx, and M. Ingels, "A compact digital amplitude modulator in 90nm CMOS," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2010*, March 2010.

[35] C. Presti, F. Carrara, A. Scuderi, P. Asbeck, and G. Palmisano, "A 25 dbm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *Solid-State Circuits, IEEE Journal of*, 2009.

[36] V. Chironi, B. Debaillie, A. Baschirotto, J. Craninckx, and M. Ingels, "An area efficient digital amplitude modulator in 90nm CMOS," in *Circuits and Systems 2010 (ISCAS), IEEE International Symposium on*, 2010.

[37] M. Alavi, A. Visweswaran, R. Staszewski, L.C.N. De Vreede, J. Long, and A. Akhnoukh, "A 2-GHz digital I/Q modulator in 65-nm CMOS," in *Solid State Circuits Conference (A-SSCC), 2011 IEEE Asian*, Nov. 2011.

[38] Product leaflet DAC1658D. IDT. Visited: 28-02-2014. [Online]. Available: http://www.idt.com/document/dst/dac1653d-dac1658d-datasheet

[39] L. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proceedings of the IRE*, July 1952.

[40] A. Maxim, R. Poorfard, M. Reid, J. Kao, C. Thompson, and R. Johnson, "A DDFS driven mixing-DAC with image and harmonic rejection capabilities," in *Solid-State Circuits Conference, 2008 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2008.

[41] F. Raab, "Intermodulation distortion in Kahn-technique transmitters," *Microwave Theory and Techniques, IEEE Transactions on*, Dec. 1996.

[42] P. Reynaert and M. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *Solid-State Circuits, IEEE Journal of*, Dec. 2005.

[43] M. Talonen and S. Lindfors, "System requirements for OFDM polar transmitter," in *Circuit Theory and Design (ECCTD), 2005 17st European Conference on*, 2005.

[44] M. Valkama, M. Renfors, and V. Koivunen, "Advanced methods for I/Q imbalance compensation in communication receivers," *IEEE Transactions on Signal Processing*, 2001.

[45] W. Groeneveld, H. Schouwenaars, and H. Termeer, "A self calibration technique for monolithic high-resolution D/A converters," in *Solid-State Circuits Conference, 2089 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 1989.

[46] G. Radulov, P. Quinn, J. Hegt, and A. van Roermund, "A start-up calibration method for generic current-steering D/A converters with optimal area solution," in *Circuits and Systems 2005 (ISCAS), IEEE International Symposium on*, May 2005.

[47] Y. Tang, J. Briaire, K. Doris, R. van Veldhoven, P. van Beek, H. Hegt, and A. van Roermund, "A 14b 200MS/s DAC with SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist band enabled by dynamic-mismatch mapping," in *VLSI Circuits (VLSIC), 2010 IEEE Symposium on*, June 2010.

[48] S. Balasubramanian and W. Khalil, "Direct digital-to-RF digital-to-analogue converter using image replica and nonlinearity cancelling architecture," *Electronics Letters*, July 2010.

[49] W. Gaber, P. Wambacq, J. Craninckx, and M. Ingels, "A CMOS IQ direct digital RF modulator with embedded RF FIR-based quantization noise filter," in *Solid-State Circuits Conference, 2011 (ESSCIRC). Proceedings of the 37st European*, 2011.

[50] H.H. Chen, C.H. Lin, P.C. Huang, and J.T. Chen, "Joint polynomial and look-up-table predistortion power amplifier linearization," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, Aug. 2006.

[51] H. Danneels, M. Verhelst, P. Palmers, W. Vereecken, B. Boury, W. Dehaene, M. Steyaert, and G. Gielen, "A low-power mixing DAC IR-UWB-receiver," in *Circuits and Systems 2008 (ISCAS), IEEE International Symposium on*, May 2008.

[52] J. Weldon, R. Narayanaswami, J. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.C. Tsai, C.W. Lee, and P. Gray, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *Solid-State Circuits, IEEE Journal of*, Dec. 2001.

[53] M. Sadeghifar and J. Wikner, "A higher Nyquist-range DAC employing sinusoidal interpolation," in *NORCHIP, 2010*, Nov. 2010.

[54] P. Cruise, C.M. Hung, R. Staszewski, O. Eliezer, S. Rezeq, K. Maggio, and D. Leipold, "A digital-to-RF-amplitude converter for GSM/GPRS/EDGE in 90-nm digital CMOS," in *Radio Frequency integrated Circuits (RFIC) Symposium, 2005 IEEE*, June 2005.

[55] R. Staszewski, J. Wallberg, S. Rezeq, C.M. Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phones," *Solid-State Circuits, IEEE Journal of*, Dec. 2005.

[56] M. Park, M.H. Perrott, and R.B. Staszewski, "A time-domain resolution improvement of an RF-DAC," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, July 2010.

[57] A. Pozsgay, T. Zounes, R. Hossain, M. Boulemnakher, V. Knopik, and S. Grange, "A fully digital 65nm CMOS transmitter for the 2.4-to-2.7GHz WiFi/WiMAX bands using 5.4GHz $\Delta\Sigma$ RF DACs," in *Solid-State Circuits Conference, 2008 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2008.

[58] S.S. Chen, N.S. Kim, and J. Rabaey, "Multi-mode sub-Nyquist rate digital-to-analog conversion for direct waveform synthesis," in *Signal Processing Systems, 2008. SiPS 2008. IEEE Workshop on*, Oct. 2008.

[59] G. Brenna, D. Tschopp, J. Rogin, I. Kouchev, and Q. Huang, "A 2-GHz carrier leakage calibrated direct-conversion WCDMA transmitter in 0.13-µm CMOS," *Solid-State Circuits, IEEE Journal of*, Aug. 2004.

[60] A.J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *Solid-State Circuits, IEEE Journal of*, Jan. 2005.

[61] K. Doris, "High-speed D/A converters: from analysis and synthesis concepts to IC implementation," Ph.D. dissertation, Eindhoven University of Technology, 2004.

[62] Y. Tang, H. Hegt, A. van Roermund, K. Doris, and J. Briaire, "Statistical analysis of mapping technique for timing error correction in current-steering DACs," in *Circuits and Systems 2007 (ISCAS), IEEE International Symposium on*, May 2007.

[63] T. Nakabayashi, M. Shinozawa, and H. Arai, "Transmitting system using alias harmonic components of output signal of DAC," in *Microwave Conference, 2006. 36th European*, Sept. 2006.

[64] K. Doris, A. van Roermund, and D. Leenaerts, "Mismatch-based timing errors in current steering DACs," in *Circuits and Systems 2003 (ISCAS), IEEE International Symposium on*, May 2003.

[65] C.H. Lin, F. van der Goes, J. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, "A 12 bit 2.9 GS/s DAC with IM3 < - 60 dBc beyond 1 GHz in 65 nm CMOS," *Solid-State Circuits, IEEE Journal of*, Dec. 2009.

[66] C.H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *Solid-State Circuits, IEEE Journal of*, no. 12, 1998.

[67] G. Radulov, P. Quinn, J. Hegt, and A. van Roermund, *Smart and flexible digital-to-analog converters*. Springer, 2011.

[68] T. Chen and G. Gielen, "The analysis and improvement of a current-steering DACs dynamic SFDR-I: the cell-dependent delay differences," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, Jan. 2006.

[69] J. Long, "Monolithic transformers for silicon RF IC design," *Solid-State Circuits, IEEE Journal of*, Sept. 2000.

[70] P. Sakian, E. Janssen, A. van Roermund, and R. Mahmoudi, "Analysis and design of a 60 GHz wideband voltage-voltage transformer feedback lna," *Microwave Theory and Techniques, IEEE Transactions on*, March 2012.

[71] H. Cheema, R. Mahmoudi, and A. van Roermund, "On the importance of chip-level EM-simulations for 60-GHz CMOS circuits," in *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, Sept. 2010.

[72] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *Solid-State Circuits, IEEE Journal of*, Oct. 1989.

[73] G. Radulov, P. Quinn, H. Hegt, and A. van Roermund, "DAC correction and flexibility, classification, new methods and designs," in *Analog Circuit Design*, 2010.

[74] M. Clara et al., "A 1.5V 13bit 130-300MS/s self-calibrated DAC with active output stage and 50MHz signal bandwidth in 0.13µm CMOS," in *Solid-State Circuits Conference, 2008 (ESSCIRC). Proceedings of the 34st European*, Sep. 2008.

[75] W. Schofield, D. Mercer, and L. Onge, "A 16b 400MS/s dac with <-80dBc IMD to 300MHz and <-160dBm/Hz noise power spectral density," in *Solid-State Circuits Conference, 2003 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2003.

[76] G. Radulov, P. Quinn, H. Hegt, and A. van Roermund, "A flexible 12-bit self-calibrated quad-core current-steering DAC," in *Circuits and Systems, 2008. (APCCAS). IEEE Asia Pacific Conference on*, Nov. 2008.

[77] G. Radulov, P. Quinn, H. Hegt, and A. van Roermund, "An on-chip self-calibration method for current mismatch in D/A converters," in *Solid-State Circuits Conference, 2005 (ESSCIRC). Proceedings of the 31st European*, Sep. 2005.

[78] J. Kim, S. Modjtahedi, and C.K. Yang, "A redundancy-based calibration technique for high-speed digital-to-analog converters," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, Dec. 2014.

[79] G. Engel, S. Kuo, and S. Rose, "A 14b 3/6GHz current-steering RF DAC in 0.18 µm CMOS with 66dB ACLR at 2.9GHz," Feb. 2012.

[80] T. Kürner and S. Priebe, "Towards thz communications - status in research, standardization and regulation," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 35, no. 1, pp. 53–62, 2014.

List of Publications

[81] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "A 5.3GHz 16bit 1.75GSps wideband RF Mixing-DAC achieving IMD<-82dBc up to 1.9GHz," in *Solid-State Circuits Conference, 2015 (ISSCC). Digest of Technical Papers. IEEE International*, Feb. 2015, accepted.

[82] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "Classification for synthesis of high spectral purity current steering Mixing-DAC architectures," *Analog Integrated Circuits and Signal Processing*, 2014, submitted.

[83] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "A novel timing-error based approach for high speed highly linear Mixing-DAC architectures," in *Circuits and Systems 2014 (ISCAS), IEEE International Symposium on*, 2014.

[84] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "A novel output transformer based highly linear RF-DAC architecture," in *Circuit Theory and Design (ECCTD), 2013 21st European Conference on*, 2013.

[85] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "Systematic analysis of the impact of mixing locality on Mixing-DAC linearity for multicarrier GSM," in *Circuits and Systems 2012 (ISCAS), IEEE International Symposium on*, May 2012.

[86] E. Bechthum, G. Radulov, and A. van Roermund, "A temperature and disturbance insensitive calibration method for high speed digital to analog converters," in *Proceedings of the Annual workshop on circuits, systems and signal processing (ProRISC)*, 2011.

[87] E. Bechthum, G. Radulov, and A. van Roermund, "A novel temperature and disturbance insensitive DAC calibration method," in *Circuits and Systems 2011 (ISCAS), IEEE International Symposium on*, May 2011.

[88] E. Bechthum, Y. Tang, H. Hegt, and A. van Roermund, "Timing error measurement for highly linear wideband digital to analog converters," in *Circuits and Systems 2011 (ISCAS), IEEE International Symposium on*, May 2011.

[89] E. Bechthum, Y. Tang, H. Hegt, and A. van Roermund, "Calibration method for timing errors in current steering digital to analog converters," in *Proceedings of the Annual workshop on circuits, systems and signal processing (ProRISC)*, 2010.

Summary

Wide-band Mixing-DACs with high spectral purity

Cellular multicarrier transmitters for communication infrastructure require both high linearity and large bandwidth at GHz frequencies. The combination of multicarrier GSM, WCDMA and LTE typically requires IMD<-80dBc and $SFDR_{RB}$>80dBc in a large transmit bandwidth (RB) of 300MHz and at an output frequency of up to 3.5GHz and beyond.

Using a Mixing-DAC, which integrates the function of the mixer and DAC together, can result in different architecture trade-offs than just combining a DAC and mixer, and potentially enables an overall reduction of the cost and power consumption, while improving the linearity at high frequencies. The state-of-the-art Mixing-DAC publications do not report a high linearity, especially not in combination with large bandwidth. This thesis explores the linearity limitations of Mixing-DACs and the challenges of designing a Mixing-DAC with high spectral purity and large bandwidth.

To attain high spectral purity, a novel architecture is needed. The synthesis of such an architecture requires optimal choices for many aspects. This thesis classifies the possible choices for each aspect and evaluates their impact on the Mixing-DAC performance. Based on this classification, three promising architectures are selected for further analysis: cascoded global mixing, cascoded local mixing and cascaded local mixing (digital mixing).

An important trade-off between these architectures is the mixing locality. Global mixing at the output is sensitive to the non-linearity of the mixing transistors. Local mixing per current cell is sensitive to the mismatch between the local mixers. Cascoded local mixing can result in a higher linearity than

cascoded global mixing.

The difference between cascoded local mixing and digital mixing is the sensitivity to timing errors. There are two types of timing errors: delay errors and duty-cycle errors. Both architectures are more sensitive to delay errors than to duty-cycle errors. The delay errors in cascoded local mixing are much smaller than in digital mixing, hence cascoded local mixing is the most linear architecture.

A method to reduce the non-linearity due to the large output voltage swing is to use an output transformer. Although the optimal transformer configuration improves the linearity significantly, it also results in a four times increase of the power consumption.

For achieving high spectral purity, the static mismatch between the current sources should be minimized. This thesis proposes a calibration method which combines multiple unit elements of the current source such that the mismatch of these unit elements cancels one another. This results in an improved static linearity which is robust against temperature variations and external disturbances.

Furthermore, the segmentation aspects are considered. The traditional segmentation trade-off in literature so far is based on static performance. However, for high speed Mixing-DACs with high spectral purity, the segmentation trade-off should be based on the dynamic matching of the binary current cells which can be achieved.

Thus, this thesis concludes that the most optimal architecture is cascoded local mixing, which has been implemented using a 65nm CMOS triple-well technology with 1.2V and 3.3V power supplies. The key properties of this architecture are: local mixing per current cell, multi-level cascoding with double bleeding currents and elevated bulk voltage, supply-isolated LO driver, and sort-and-combine calibration.

The measurement results up to 1.9GHz are: IMD<-82dBc, $SFDR_{RB300MHz}$ >75dBc, NSD<-165dBm/Hz. The linearity up to 1.5GHz is almost constant and is actually limited by the baseband-frequency part of the converter. Above 1.5GHz, cell-dependent timing errors in the mixer cause the linearity to degrade for increasing output frequency. Nevertheless, the presented proof-of-concept outperforms all known state-of-the-art Mixing-DAC publications in terms of IMD and $SFDR_{RB}$, while measuring in the largest RB and up to an output frequency of 5.3GHz.

The reported classification, the analysis and the verification of a full design validate that Mixing-DACs can simultaneously provide high spectral purity and large bandwidth.

Samenvatting

Multicarrier zenders voor de communicatie infrastructuur vereisen zowel hoge lineariteit als een grote bandbreedte op GHz frequenties. De combinatie van multicarrier GSM, WCDMA en LTE vereist typisch IMD<-80dBc en $SFDR_{RB}$>80dBc in een grote zendbandbreedte van 300MHz en op frequenties tot 3.5GHz en hoger.

Het gebruik van een Mixing-DAC, die de functie van een mixer en een DAC integreert, kan leiden tot andere architectuurafwegingen dan het combineren van een DAC en een mixer. Nieuwe architecturen zouden een reductie van kosten en vermogensdissipatie mogelijk kunnen maken, terwijl de lineariteit op hoge frequenties wordt verbeterd. De state-of-the-art Mixing-DAC publicaties vermelden geen hoge lineariteit, en vooral niet in combinatie met een grote bandbreedte. Dit proefschrift verkent de lineariteitsbeperkingen van Mixing-DACs en de uitdagingen van het ontwerp van een Mixing-DAC met hoge spectrale zuiverheid en grote bandbreedte.

Om een hoge spectrale zuiverheid te bereiken is een nieuwe architectuur nodig. De synthese van de nieuwe architectuur vereist optimale keuzes voor alle aspecten van de architectuur. Dit proefschrift classificeert alle mogelijke keuzes voor de architectuuraspecten en evalueert hun invloed op de prestaties van de Mixing-DAC. Gebaseerd op deze classificatie zijn drie veelbelovende architecturen geselecteerd voor verdere analyse: gecascodeerd globaal mixen, gecascodeerd lokaal mixen en cascadegeschakeld lokaal mixen (digitaal mixen).

Een belangrijke afweging tussen deze architecturen is de lokaliteit van het mixen. Globaal mixen bij de uitgang van de Mixing-DAC is gevoelig voor de niet-lineariteit van de mixer transistors. Lokaal mixer per stroomcel is gevoelig voor de mismatch tussen de lokale mixers. Simulaties laten zien dat gecascodeerd lokaal mixen tot een hogere lineariteit leidt dan gecascodeerd globaal mixen.

Het verschil tussen gecascodeerd lokaal mixen en digitaal mixen is de gevoeligheid voor tijdfouten. Er zijn twee soorten tijdfouten: gelijke vertraging van de steigende en dalende flank (delay), en tegenovergestelde

vertraging van de steigende en dalende flank (duty-cycle). Beide architecturen zijn veel gevoeliger voor delay-fouten dan voor duty-cycle-fouten. De delay-fouten in digitaal mixen zijn veel groter dan in gecascodeerd lokaal mixen, en dus is de laatstgenoemde de meest lineaire architectuur.

Een methode om de niet-lineariteit ten gevolge van een grote signaalamplitude aan de uitgang van de Mixing-DAC te verminderen, is het gebruik van een uitgangstransformator. Het gebruik van een uitgangstransformator met een optimale configuratie zorgt inderdaad voor een verbetering van de lineariteit, maar dit leidt wel tot een vier keer hogere vermogensdissipatie.

Voor het bereiken van een hoge spectrale zuiverheid moet de statische mismatch tussen de stroombronnen ook worden geminimaliseerd. Dit proefschrift stelt een kalibratiemethode voor, die meerdere unit-elementen van de stroombron op een zodanig manier combineert dat de mismatch van de verschillende unit-elementen elkaar compenseren. Dit resulteert in een verbetering van de statische lineariteit die robuust is voor temperatuurvariaties en externe verstoringen.

Ook de segmentatieaspecten zijn overwogen. De traditionele segmentatieafwegingen in literatuur zijn gebaseerd op de statische eigenschappen. Maar voor Mixing-DACs met hoge snelheid en hoge spectrale zuiverheid zou de segmentatieafwegingen ook gebaseerd moeten zijn op de dynamische mismatch van de binaire stroomcellen welke bereikt kan worden.

In dit proefschrift wordt dus geconcludeerd dat de meest optimale architectuur is gecascodeerd lokaal mixen. Deze architectuur is geïmplementeerd in 65nm CMOS tripple-well technologie met 1.2V en 3.3V voedingsspanningen. De cruciale eigenschappen van deze architectuur zijn: lokaal mixen per stroomcel, multi-level cascoderen met dubbele bleedstromen en verhoogde bulkspanning, voedingsspanning-gesoleerde LO-driver, en sorteer-en-combineer kalibratie.

De meetresultaten bij 1.9GHz uitgangsfrequentie zijn: IMD<-82dBc, $SFDR_{RB300MHz}$ >75dBc, NSD<-165dBm/Hz. De lineariteit tot 1.5GHz is zo goed als constant en is afhankelijk van het basisbandfrequentiegedeelte van de Mixing-DAC. Boven 1.5GHz degradeert de lineariteit voor toenemende uitgangsfrequentie door cel-afhankelijke tijdfouten in de mixer. Toch heeft het gepresenteerde ontwerp een betere IMD en $SFDR_{RB}$ dan alle state-of-the-art Mixing-DACs tot aan de maximaal gemeten uitgangsfrequentie van 5.3GHz.

De gepresenteerde classificatie, analyse en verificatie van een volledig ontwerp, valideren dat Mixing-DACs tegelijkertijd hoge spectrale zuiverheid en grote bandbreedte kunnen leveren.

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Biography

Elbert Bechthum was born on 30th of May 1984 in Kapelle. He studied electrical engineering at the Eindhoven University of Technology where he achieved his bachelor and master degree. He graduated in 2008 at the Mixed-signal-microelectronics group on measurement of timing errors in high speed digital to analog converters. After graduation, he worked for SystematIC design in Delft as analog design engineer on low-power receivers and navigation hardware for satellites. In 2009 he married Lisanne Ravensbergen. In 2010 he rejoined the Eindhoven University of Technology for pursuing a PhD degree.

His research interest include high performance data converters, digital-assisted analog and smart calibration techniques.

List of symbols and abbreviations

ACLR	Adjacent channel leakage ratio
ADC	Analog to digital converter
BB	Baseband
CalDAC	Calibrating DAC
Clk	Clock
CML	Current mode logic
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
CS	Current steering
CUE	Calibrated unit element
DAC	Digital to analog converter
dBc	dB with respect to a carrier
dB_{FS}	dB with respect to full scale
DCS1800	Digital cellular system at 1800 MHz
DDRF	Direct digital RF
DNL	Differential non-linearity
DPD	Digital predistortion
EER	Envelope elimination and restoration
EVM	Error vector magnitude
f_{in1}	Input frequency
FIR	Finite impulse response
f_{LO}	LO (mixing) frequency
f_{out}	Output frequency
F_S	Sample frequency
FSM	Finite state machine
GaAs	Gallium arsenide
GS/s	Gigasample per second
GSps	Gigasample per second

GSM	Global System for Mobile Communications
HD	Harmonic distortion
HD2	Second-order harmonic distortion
I/V	Current to voltage
I/Q	In-phase / quadrature
IDT	Integrated Device Technology
IMD	Intermodulation distortion
IMD3	Third-order intermodulation distortion
INL	Integral nonlinearity
IP	Intellectual property
ISI	Inter symbol interference
L	Length of transistor
LO	Local oscillator
LSB	Least significant bit
LTE	Long term evolution
MC	Monte carlo
MSB	Most significant bit
NSD	Noise spectral density
OFDM	Orthogonal frequency-devision multiplexing
PA	Power amplifier
PLL	Phase-locked loop
PSRR	Power supply rejection ratio
QAM	Quadrature amplitude modulation
RB	Reduced bandwidth
RF	Radio frequency
RZ	Return to zero
SAR ADC	Successive approximation ADC
SaZ	Symmetric around zero
SFDR	Spurious-free dynamic range
$\mathrm{SFDR_{RB}}$	Spurious-free dynamic range in a reduced bandwidth
$\mathrm{SFDR_{RB300MHz}}$	Spurious-free dynamic range in a reduced bandwidth of 300MHz
V/I	Voltage to current
V_{out}	Output voltage
$\mathrm{V_{pp}}$	Volt peak-to-peak
W	Width of transistor
WCDMA	Wideband code division multiple access
$\mathbb{Z}$	Set of all integers
$\Delta\Sigma$	Delta-sigma