# ULTRA WIDEBAND 5 W HYBRID POWER AMPLIFIER DESIGN USING SILICON CARBIDE MESFETs

von
Master of Engineering
Ahmed Sedek Mahmoud Sayed

von der Fakultät IV – Elektrotechnik und Informatik
der Technischen Universität Berlin
zur Erlangung des akademischen Grades
Doktor der Ingenieurwissenschaften
– Dr.-Ing. –

genehmigte Dissertation

Promotionsausschuss:

Vorsitzender: Prof. Dr.-Ing. H. Klar
Gutachter: Prof. Dr.-Ing. G. Böck
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Tag der wissenschaftlichen Aussprache: 31. Mai 2005

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*To my Parents and my Wife*

# ACKNOWLEDGMENTS

All praise is due to our God (ALLAH) who has been bestowing me with his great bounties and enabled me to complete my dissertation.

I'm deeply indebted to my graduate advisor, Professor Georg Boeck, who is extremely hard working and dedicated to his work, for his guidance and encouragement during the past four years. His work ethics, pragmatic methodology have greatly influenced my approach to the professional world and surely will be with me for the years to come.

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My deep gratitude is due to my parents for their continuous guidance, encouragement, support, and prayers during my life. Thanks are due to my wife for her patience, help, and being away from her family for several years during my study.

Finally, to my Sons Alaa and Mohamed, when you smile, I see my live with colors. Thanks for Allah to be in my life.

# ZUSAMMENFASSUNG

Aufgrund des hohen Bandabstandes von SiC besitzen SiC-MESFETs ein hohe Duruchbruchspannung und können folglich bei hohen Versorgungsspannungen betrieben werden. Darüber hinaus besitzen sie eine hohe Elektronensättigungsgeschwindigkeit und Wärmeleitfähigkeit. Aufgrund dieser Eigenschaften eignen sich diese Bauelemente hervorragend für die Entwiklung von breitbandigen Leistungsverstärkern bis in den unteren GHz-Bereich. In dieser Arbeit wird ein neues empirisches Modell für SiC MESFET vorgeschlagen. Ein kommerziell erhältlicher, gehäuster MESFET Typ (CREE CRF24010) wird für die Entwicklung des Modelles verwendet. Messungen wurden sowohl in Arbeitspunkten mit als auch ohne Vorspannung durchgeführt um die Gleichungen und Parameter abzuleiten. Die “Cold FET“ Technik wurde verwendet um die parasitären extrinsischen Elemente zu bestimmen, während die arbeitspunktabhängigen Elemente des Modelles analytisch bei mehreren Arbeitspunkten bestimmt wurden. Nichtlineare Gleichungen für die arbeitspunktabhängigen Elemente wurden ebenfalls abgeleitet. Das so entwickelte Modell für den SiC MESFET wurde sowohl hinsichtlich des Kleinsignal als auch des Großsignalverhaltens überprüft. Fünf verschiedene Generationen von Breitband-Leistungsverstärkern wurden auf Grundlage des entwickelten Modelles implementiert. Dabei wurde keinerlei Impedanztransformator eingesetzt. Eine neuartige breitbandige Biasstruktur wurde entwickelt, um gute Isolation und geringe Verluste über die angestrebte Bandbreite zu erreichen. Die Anpassungsnetzwerke an Eingang, Ausgang und zwischen den Stufen sowie die Parallel-Rückkopplung wurden mit Hilfe von Mikrostreifenleitungstechnik realisiert um die Bandbreite zu erhöhen und die Stabilität zu verbessern. Als erste Generation wird ein einstufiger 5 Watt Leistungsverstärker mit einem SiC MESFET entworfen und aufgebaut, der den Frequenzbereich von 10 MHz bis 2,4 GHz abdeckt. Eine Leistungsverstärkung von 6 dB, 37 dBm Ausgangsleistung, 33% PAE und 52 dBm OIP3 wurden erreicht. Ein zweistufiger Leistungsverstärker mit hoher Verstärkung für die selbe Bandbreite, der einen GaAs und einen SiC MESFET in Kaskade verwendet, wurde ebenfalls aufgebaut. Typische Werte von 23 dB Leistungsverstärkung, 37 dBm

Ausgangsleistung, 28 % PAE und 47 dBm OIP3 wurden erreicht. Der Einfluss der Treiberstufe auf die Leistungs- und Linearitätseigenschaften der zweiten Generation wurde untersucht. Basierend auf SiC Chips wurden die dritte und vierte Generation in Form von einstufigen und zweistufigen ultra-breitband Leistungsverstärkern implementiert, die das Frequenzband von 1 MHz bis 5 GHz abdecken. Der Einfluss des GaAs FET Treibers in der vierten Kategorie auf die Gesamteigenschaften wurde ebenfalls diskutiert. Unter Einsatz der Rückkopplungs-Kompensationstechnik wurde ein schmalbandiger 10 W Leistungsverstärkerentwurf mit hoher Verstärkung, basierend auf einem SiC Chip, als fünftes Beispiel vorgestellt. Alle Leistungs- und Linearitäts-Ergebnisse wurden über das gesamte Frequenzband ermittelt. Die Entwurfsprozedur wird detailliert beschrieben und die Ergebnisse werden diskutiert und ausführlich mit den Simulationen verglichen.

# ABSTRACT

SiC MESFETs have an enormous potential for realizing high-power amplifiers at microwave frequencies due to their wide band-gap features of high breakdown field, high electron saturation velocity and high operating temperature. In this thesis, a new empirical model for SiC MESFET is proposed. A commercially packaged high power MESFET device (CREE CRF24010) is adopted for the model development. Both hot and cold bias condition measurements are performed to derive equations and parameters. Cold FET technique is used to extract the parasitic extrinsic elements whereas the bias-dependent model elements are extracted analytically from multiple bias points. Nonlinear equations for the bias dependent elements are derived, too. The derived model for the SiC MESFET has been verified in small signal as well as large signal performances. Five different generations of broadband power amplifiers based on the developed model have been implemented. No impedance transformer was used at all. A novel broadband choke structure has been developed to obtain good isolation and low loss over the desired bandwidth. Input, interstage and output matching networks and shunt feedback topology have been designed based on microstip technique to increase the bandwidth and improve the stability. In the first generation, a single stage 5-watt power amplifier using a SiC MESFET covering the frequency range from 10 MHz to 2.4 GHz is designed and fabricated. A power gain of 6 dB, 37 dBm output power, 33 % PAE and 52 dBm OIP3 have been achieved. A high gain two stage power amplifier covering the same bandwidth using a GaAs- and a SiC-MESFET in cascade also has been fabricated. Typical values of 23 dB power gain, 37 dBm output power, 28 % PAE and 47 dBm OIP3 have been obtained. The impact of the driver stage on power and linearity performances of the second generation has been discussed. Based on SiC Chip, the third and the fourth generation represent ultra wideband single stage and two stage power amplifiers, covering the frequency band from 1 MHz to 5 GHz have been simulated. Small signal and harmonic balance simulations based on ADS have been introduced. The impact of the GaAs FET driver in the fourth category on the overall performances also has been discussed. Using feedback compensation technique, a 10-W narrow band high gain power amplifier

design based on SiC Chip has been presented as a fifth example. All power and linearity results were obtained over the whole frequency band. The design procedure is given in detail and the results are being discussed and compared with simulations extensively.

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# CHAPTER ONE

# INTRODUCTION

The demand for power amplifiers has been continually increasing over the last decade. The requirements include aspects of high power level, high efficiency, high linearity and high operating frequency and the relative importance of each of these features is application specific [1 - 3]. One major trend is the continuous demand for more power over a very wide bandwidth. Unfortunately, the existing technologies have struggled to satisfy the higher demand. GaAs-based power devices have been very reliable workhorses at high frequencies especially in the microwave spectrum. However, their power performances have already been pushed close to the theoretical limit [4].

Under such circumstance, wide band-gap semiconductors with an order of magnitude or so higher breakdown voltage along with excellent thermal properties began to emerge. High breakdown voltage makes low operating current and high internal impedance possible. High internal impedance in turn can simplify impedance matching and result in efficient power coupling and broad bandwidth. Further, the performance of these transistors does not degrade drastically under elevated temperatures (unlike conventional GaAs and silicon devices). Therefore, we expect RF power amplifiers made of these transistors to have uniform performance characteristics over both a wide bandwidth and a wide temperature range. Such amplifiers are very desirable for applications in measurement equipment, aerospace and military systems that involve frequency hopping or spread spectrum operation under a fluctuating ambient temperature [5 - 7].

The interest in power amplifier design based on SiC MESFETs necessitates the development of accurate large signal models that can predict the maximum output power level, achievable power added efficiency (PAE) and other nonlinear phenomena over the whole operating frequency range, using harmonic balance (HB) simulation. Empirical table-based models of MESFET are the most widely used models in nonlinear circuit simulators today which have the important advantage of

flexibility and high computation efficiency. A lot of empirical models suitable for the simulation of MESFET in nonlinear circuits have been developed. In this approach, the tabulated data that represent the extracted nonlinear elements of the small signal model are mathematically transformed into spline functions which should be differentiable to a high order of derivatives in order to ensure a correct description of harmonics and convergence with harmonic balance simulations.

In order to achieve a higher output power level, a large periphery device would be required. The lowered impedance levels of the devices would represent more difficulty in the design of the matching networks. Generally speaking, the ratio for each matching circuit should be less than 1.5 in order to achieve larger than 3:1 bandwidth. Multisection matching networks would be necessary to achieve the desired bandwidth, resulting in more complex and lossy matching networks [8], [9]. In this work, impedance transformation is demonstrated based on multisections of microstrip elements. The output matching network is implemented based on the simulated load pull data for maximum output power. Input, and interstage matching networks are designed for maximum gain. Feedback technique is used to flatten the gain ripple and improve the stability of the device. A novel DC biasing network is developed with very low loss to meet the wide frequency band. [11], [70].

With the power density advantage of the SiC MESFETs technology and the novel approaches to the challenges of the broadband power amplifier design, we have successfully designed five categories of SiC power amplifiers; two of them have been fabricated and measured. All simulations in this work have been accomplished based on ADS2003A from Agilent while the design fabrication has been done based on microstrip materials R4003 from Rogers.

This thesis includes seven chapters. First chapter is the introduction of the thesis; it describes the background of the research and defines the objective of the thesis. Chapter 2 reviews the fundamentals of the power amplifier, design considerations, distortion in amplifiers and how to measure it and some of power amplifier classes have been also described.

Chapter 3 introduces an accurate small signal parameter extraction procedure. Extrinsic parameters in both pinch-off and forward bias modes are extracted using cold FET technique whereas the intrinsic parameters are being extracted analytically at various bias points.

Chapter 4 presents the model incorporating empirical expressions for DC, capacitance and frequency dispersion modeling. Accuracy of the new model will also be verified. A model developed by Cree for the packaged transistor CRF24010 is compared in its performance to the proposed model.

Chapter 5 introduces the design procedure in 3 steps. First, the selection process leading to the power transistor, which fulfils the design requirements, is described. The development of the DC biasing networks that meet the desired bandwidth is considered in the next step while the third one deals with input, output and interstage matching networks as well as shunt feedback circuit design resulting in the required broadband characteristic.

In chapter 6, simulations and measurements of the implemented amplifiers are given and discussed. Small-signal gain, stability factor and matching over the frequency band are introduced, and power performances (PAE, output power and power gain) are presented. Two-tone measurements at frequency spacing of 200 kHz have been performed, too. AM−AM and AM−PM conversion data are introduced and discussed at the end of the chapter.

Chapter 7 concludes the thesis with the achievements summary and suggestions for the future work.

Appendix A introduces a brief analysis for intermodulation distortion in power amplifiers. Appendix B presents the two-port intrinsic Y-parameters extraction in terms of the measured S-parameters. Small signal gain determination based on the value of the feedback resistance is presented in appendix C.

# CHAPTER TWO

# POWER AMPLIFIER FUNDAMNENTALS

The RF power amplifier (PA), a critical element in transmitter units of communication systems, is expected to provide a suitable output power at a very good gain with high efficiency and linearity. The output power from a PA must be sufficient for reliable transmission. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. High efficiency improves thermal management, battery lifetime and operational costs. Good linearity is necessary for bandwidth efficient modulation. However, these are contradicting requirements and a typical power amplifier design will require a certain level of compromise. There are several types of power amplifiers, which differ from each other in terms of linearity, output power or efficiency. In this chapter, we present an overview on power amplifiers; design considerations, distortions in power amplifiers and how to measure them. The last section introduces a number of PA classes that meet either high efficiency or linearity.

## 2.1 Power Amplifier Design Considerations

The beneficial method is to characterize the properties of MESFETs through its two-port scattering parameters matrix (S-parameters), which is widely used in RF/microwave theory. This approach works very well under steady state and small-signal approximation. As it is known when dealing with power amplifiers this approximation is not valid because the amplifier operates over a nonlinear region. Therefore, some other techniques have to be presented to conduct the appropriate design. Harmonic balance (HB) analysis is utilized as a method to characterize PA. Anyhow, small signal S-parameters may still be used when designing a class A amplifier with sufficient precision. Here the signal amplification is largely restricted

to the linear region of the transistor. However, the small-signal S-parameters become progressively unsuitable for class AB, B, or C amplifiers, due to changes in the transfer characteristic of the device (it is not possible to assume anymore that transconductance is constant) [12]. In other words, when the power of the input signal reaches a certain level, the amplifier saturates and starts clipping the output signal. The consequence is the generation of spurious frequencies that invokes distortion of the fundamental signal and power losses. As a result, the specific properties for evaluation of PAs as well as typical properties must be considered.

### 2.1.1 Output Power

There are two concepts of power for RF/microwave circuits: available and dissipated power. Available or transferable is the maximum power, which is accessible from a source. The maximum available power is obtained from the source if the input impedance of the device equals the conjugate of the source impedance ($Z_{in} = Z_s^*$) [13]. Therefore, the maximum available power as a function of frequency can be expressed as:

$$P_{av}(\omega) = \frac{1}{8}\frac{|V_S(\omega)|^2}{\mathrm{Re}\{Z_S(\omega)\}}, \tag{2.1}$$

where $V_S(\omega)$ is the peak value of a sinusoidal voltage applied to the input. $\mathrm{Re}\{Z_S(\omega)\}$ is the real part of the source impedance. The dissipated or transferred power is the power dissipated in a load [14]. It can be expressed as:

$$P_d(\omega) = \frac{1}{2}\frac{|V_L(\omega)|^2}{\mathrm{Re}\{Z_L(\omega)\}}, \tag{2.2}$$

where $V_L(\omega)$ is the peak value of the sinusoidal output voltage. $\mathrm{Re}\{Z_L(\omega)\}$ is the real part of the load impedance. The more practical representation for output power in terms of class A PA is;

$$P_{out} = \frac{1}{2}V_D I_D = \frac{1}{8}V_{\max} I_{\max}, \tag{2.3}$$

where $I_{max} = 2\ I_D$, $V_{max} = 2\ V_{DS}$ are maximum drain current and voltage.

### 2.1.2 Power Gain and Stability

Power gain is the ratio of the power delivered to an arbitrary load ($P_L$) to the power delivered to the network by the source ($P_S$). It is a function of the load

reflection coefficient ($\Gamma_L$) and the S-parameters of the network and it is independent of source reflection coefficient. This can be expressed as shown in the following formula:

$$G_P = \frac{P_L}{P_S} \tag{2.4}$$

The stability of a small-signal RF amplifier is ensured by deriving a set of S-parameters from measured data or a linear model, and then establishing the value of the K factor stability parameter. If the K factor is greater than unity, at the frequency and bias level in question, then expressions for matching impedances at input and output can be evaluated to give a perfect conjugate match for the device. Amplifier design in this context is mainly a matter of designing matching networks, which present the prescribed impedances over the necessary specified bandwidth. If the K factor is less than unity, negative feedback or lossy matching must be employed in order to maintain an unconditionally stable design (as will be discussed later in chapter 5).

There are cases where a device has a very high K factor value, but very low gain in conjugate matched condition. The physical cause of this can be traced to a device, which has gain roll-off due to carrier-mobility effects, rather than parasitics. In such cases, introduction of some positive feedback reduces the K factor and increases the gain in conjugately matched conditions, while maintaining unconditional stability.

### 2.1.3 Efficiency

Efficiency is a critical factor in PA design. Three definitions of efficiency are commonly used. Drain efficiency is defined as the ratio of RF output power to DC input power:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.5}$$

Power-added efficiency (PAE) incorporates the RF drive power by subtracting it from the output power, i.e.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.6}$$

PAE gives a reasonable indication of PA performance when gain is high. An overall efficiency such as $P_{out} / (P_{dc} + P_{in})$ is useable in all situations. This definition can be varied to include driver DC input power, the power consumed by supporting circuits, and anything else of interest.

### 2.1.4 Linearity

The need for linearity is one of the principal drivers in the design of modern power amplifiers. Nonlinearities cause imperfect reproduction of the amplified signal, resulting in distortion and splatter. In the next section, a variety of distortion in PAs will be discussed. Measures of distortion include 1 dB compression point representing the amplitude distortion, intercept point representing the intermodulation distortion, and amplitude to phase (AM−PM) conversion representing the phase distortion will also be presented.

## 2.2 Distortion in Power Amplifiers

This section presents the various forms of RF amplifier distortion: single-tone (harmonic distortion), two-tone (intermodulation distortion), phase distortion and other spurious distortions.

### 2.2.1 Harmonic distortion

An ideal amplifier will have a linear transfer characteristic, where the output voltage would be a scalar multiple of the input voltage, that is,

$$V_{out}(t) = K_1 V_{in}(t) \tag{2.7}$$

where $K_1$ is the voltage gain of the amplifier. The output spectrum from such an amplifier will be identical to that of the input and no new (extra) frequency components will be introduced neither within nor outside the amplifier bandwidth as shown in figure 2.1.

However, practical amplifiers are nonlinear devices. A simple form of amplifier nonlinearity may be illustrated (for example) by the addition of a second order term to the transfer characteristic given by (2.7) as

$$V_{out} = K_1 V_{in}(t) + K_2 V_{in}^2(t) \tag{2.8}$$

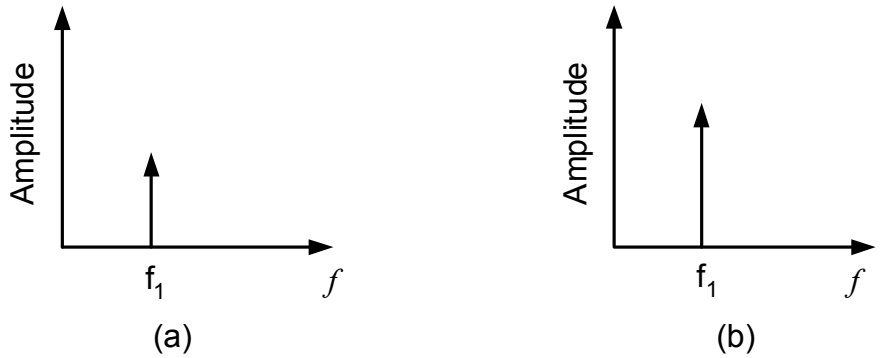


Figure 2.1. Frequency response of an ideal amplifier: a) at the input, b) at the output.

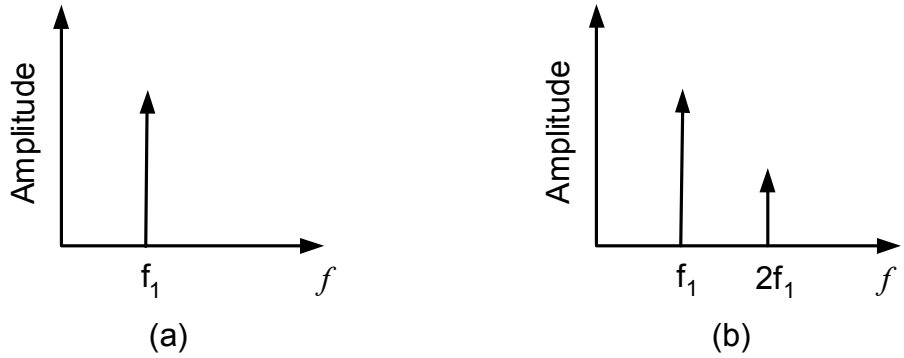


Figure 2.2. A frequency spectrum for the input and output of a nonideal amplifier.

This nonlinear amplifier will introduce extra frequency components, which will appear at two times the original frequency. This gives rise to the term *second harmonic distortion* used to describe the form of nonlinear distortion introduced by the second-order term in the transfer characteristic, as shown in figure 2.2. Examination of the amplitude of the second harmonic component indicates that it will increase in proportion to the square of the input signal (and also in proportion to the constant, $K_2$). The amplitude of the fundamental frequency component, however, will only increase in proportion to the voltage gain, $K_1$. As a result, the amplitude of the second harmonic will increase at a greater rate than that of the fundamental component with increasing input level and at some input level both the fundamental and the second order harmonic will have the same output level, which is referred to as *second harmonic intercept point*. Note that a second order characteristic produces harmonic distortion but it does not produce in-band intermodulation distortion (see below). This is an important difference between even-order and odd-order nonlinearities, even-order nonlinearities do not generate in-band intermodulation distortion.

### 2.2.2 Intermodulation Distortion

Intermodulation distortion is a nonlinear distortion characterized by the appearance in the output of a device, of frequencies that are linear combinations of the fundamental frequencies and all harmonics present in the input signals (see appendix A for details) [15]. A very common procedure to measure the intermodulation distortion is by means of a two-tone test. In a two-tone test a nonlinear circuit is excited by two closely spaced input sinusoids. This would result in an output spectrum consisting of various intermodulation products in addition to the amplified version of the two fundamental tones and their harmonics as shown in figure 2.3. If $f_1$ and $f_2$ are the fundamental frequencies then the intermodulation products are seen at frequencies given by

$$f_{IMD} = \pm m f_1 \pm n f_2 \tag{2.9}$$

The ratio of power in the intermodulation product to the power in one of the fundamental tones is used to quantify intermodulation. Of all the possible intermodulation products usually the third order intermodulation products (at frequencies $2f_1$-$f_2$ and $2f_2$-$f_1$) are typically the most critical as they have the greatest power. Furthermore they often fall into the receiver pass band making it difficult to filter them out.

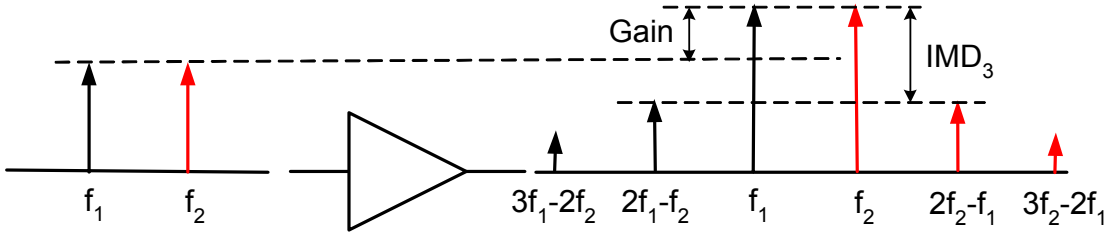


Figure 2.3. Graphical concept of intermodulation distortion.

### 2.2.3 Phase Distortion

Most practical amplifier circuits exhibit memory effects because of storage elements such as capacitors and inductors. In this case, phase distortion can arise from capacitive or inductive nonlinearities. This is commonly referred to as amplitude-modulation-to-phase modulation (AM−PM) conversion. By applying a single-tone signal at the input of a nonlinear amplifier, the fundamental component at the output can be given by the form [16]:

$$(A + Be^{j\theta})\cos(\omega t) \tag{2.10}$$

The amplitude of equation (2.10) consists of a first order component, $A$, and a third order component, $Be^{j\theta}$, where θ is the phase difference (due to nonlinear capacitances) between the two components.

Addition of the two phasors, linear and third order, leads to a phasor with a new angle. This new angle is dependent on variations of the input signal amplitude. As a result, changes in input amplitude give rise to changes in angle of the linear component of the output signal. This mechanism is called AM−PM conversion. Since the third order component rises three times faster than the first order output component on a logarithmic scale, AM−PM conversion will be most serious as the circuit is driven into saturation. Figure 2.4 illustrates AM−AM and AM−PM conversions on a sinusoidal signal in three cases: only amplitude conversion (Figure 2.4 (a)), only phase conversion as in case (b), and the superposition of two conversions as in figure 2.4(c).

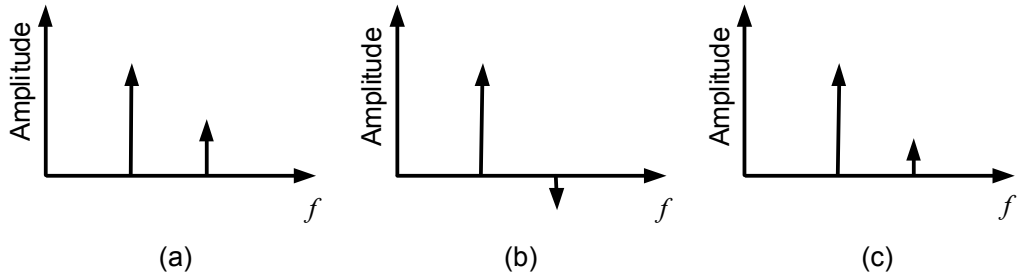


Figure 2.4. (a) AM−AM conversion, (b) AM−PM conversion, (c) combination of AM−AM and AM−PM conversion.

### 2.2.4 Spurious Distortion

Some signals appear at the output of an amplifier and they have no obvious relationship to the input signals being amplified. They may appear and disappear randomly and may change frequency and level. Such signals are referred to as spurious products and consist of parasitic and sub-harmonic oscillations together with unwanted external interference.

## 2.3 Measures of Distortion

In order to get a better understanding of the level of nonlinear distortion of a circuit, measures are defined which characterize nonlinear behaviour of the circuits.

Two commonly used measures to describe nonlinearities of a circuit are 1 dB compression point and third order intercept point (IP3). Simple test signals such as those described in the previous section are commonly used to test the device for linearity and find these measures. First, the 1 dB compression point as a measure for gain (output power) compression will be discussed.

### 2.3.1 1 dB Compression Point

The 1 dB compression point is defined as the power gain where the saturation of the device (caused by nonlinearities) reduces the power gain by 1 dB over the small signal linear power gain [17]. This is the point where the gain is no longer in the linear area, and the component/system is starting to compress. It is useful to know the 1 dB compression point of any component or system, since this parameter determines the maximum input power which can be supplied to the amplifier and still have a gain that can be considered constant with respect to power level. As discussed in section 2.2, harmonic and intermodulation distortion (when multiple input frequencies are present) occur when the DUT starts to saturate. Figure 2.5 shows two different ways of displaying the same compression behaviour. Referring to the plot of $P_{out}$ versus $P_{in}$, the compression can be seen to begin at the point where the data deviates from a linear 1:1 slope line. The second display method is to plot the gain versus input power. Compression can be seen to begin where the data drops below a constant valued gain, and the 1 dB compression point can be deduced as the point where the gain has dropped 1 dB, compared to the reference level.

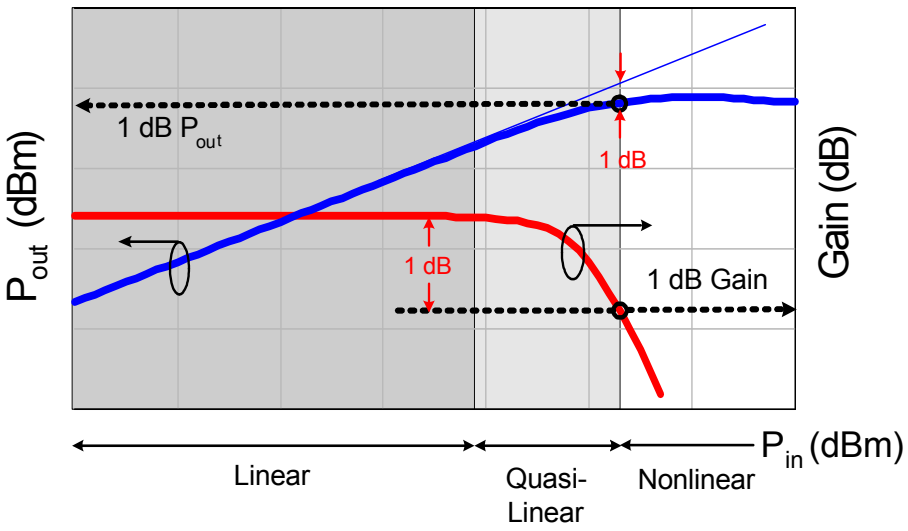


Figure 2.5. 1 dB compression point.

### 2.3.2 Intercept Point

The intercept point is the point where the slope of the fundamental linear component meets the slope of the intermodulation products on a logarithmic chart of output power versus input power. The intercept point can be input or output referred. Input intercept point represents the input power level for which the fundamental and the intermodulation products have equal amplitude at the output of a nonlinear circuit. In most practical circuits, intermodulation (IM) products will never be equal to the fundamental linear term because both amplitudes will compress before reaching this point. In those cases intercept point is measured by a linear extrapolation of the output characteristics for small input amplitudes. Since the third order intermodulation products, among the IM products, are of greatest concern in power amplifier design, the corresponding intercept point called the third order intercept point (IP3) is an important tool to analyze the effects of third order nonlinearities. In fact, intercept point serves as a better measure of linearity in comparison to intermodulation products as it can be specified independent of the input power level [18].

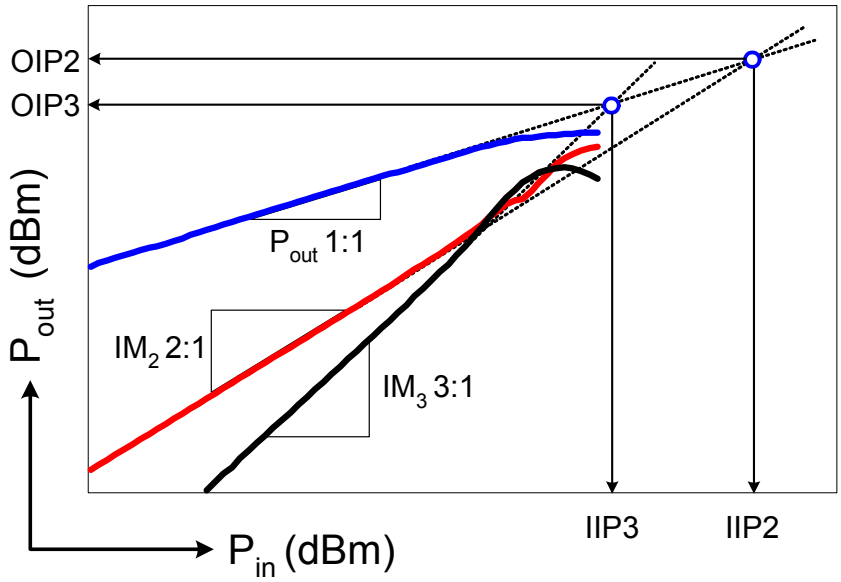


Figure 2.6. Graphical intercept point concept.

## 2.4 Power Amplifier Classes

RF power amplifiers are commonly designated as classes A, B, C, D, E, and F [19]. All but class A employ various nonlinear, switching, and wave-shaping

techniques. Classes of operation differ not only in the method of operation and efficiency, but also in their power-output capability.

### 2.4.1 Class A

Class A is the simplest power amplifier type in terms of design and construction. The Class A amplifier has a conduction angle of 2π radians or 360°. Conduction angle refers to the time period for which a device is conducting. Thus a conduction angle of 360º tells us that in Class A operation the device conducts current for the entire input cycle. Class A amplifiers are considered to be the most linear since the transistor is biased in the center of the load line to allow for maximum voltage and current swings without cut-off or saturation (Figure 2.7). However the problem with Class A amplifiers is their poor efficiency. This is because the device is draining current at all times which translates to higher power loss. In fact it can be shown that the maximum efficiency achievable from a Class A power amplifier is only 50% [19]. However, this is a theoretical number and the actual efficiency is typically much less. In fact commercial Class A amplifiers have efficiencies as low as (20 - 30 %). Hence Class A amplifiers are usually only used in places where linearity is a stringent requirement and where efficiency can be compromised as in the initial stages of a multi-stage power amplifier.

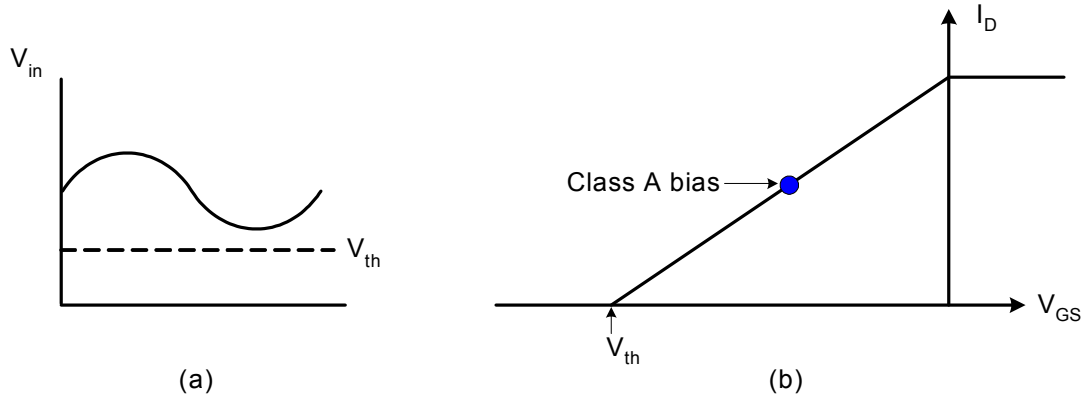


Figure 2.7. Class A PA: (a) input waveform, (b) bias point.

### 2.4.2 Class B

The transistor is biased at the threshold voltage point of the transistor for Class B operation (Figure 2.8). Hence there is a current flowing at the output of the device only when there is a signal at the input. Moreover the device would conduct current

only when the input signal level is greater than the threshold voltage. This occurs for the positive half cycle of the input signal and during the negative half cycle the device remains turned off. Hence the conduction angle for Class B operation is 180º or π radians. Due to this behaviour, there is a large saving in the power loss. It can be shown that the maximum theoretical efficiency achievable with Class B operation is about 78.5% [19]. Commercial Class B amplifiers typically have an efficiency of 50-60%. However, the increased efficiency comes at the cost of reduced linearity. The reduction in the output power occurs because the output current flows for only one half cycle of the input signal. The poor linearity is primarily attributed to an effect called the crossover distortion [19]. Whenever the transistor is turned on (at the start of positive half cycle) and turned off (at the start of negative half cycle) the transistor does not change abruptly from one state to the other. Instead the transition is gradual and nonlinear, and results in an offset voltage. This voltage alters the output waveform (crossover distortion) thereby reducing the linearity. Sometimes a class B amplifier is realized in "push-pull" configuration. In this configuration the two transistors are driven 180° out-of-phase so that each transistor is conducting for one half cycle of the input signal and turned off for the other half cycle.

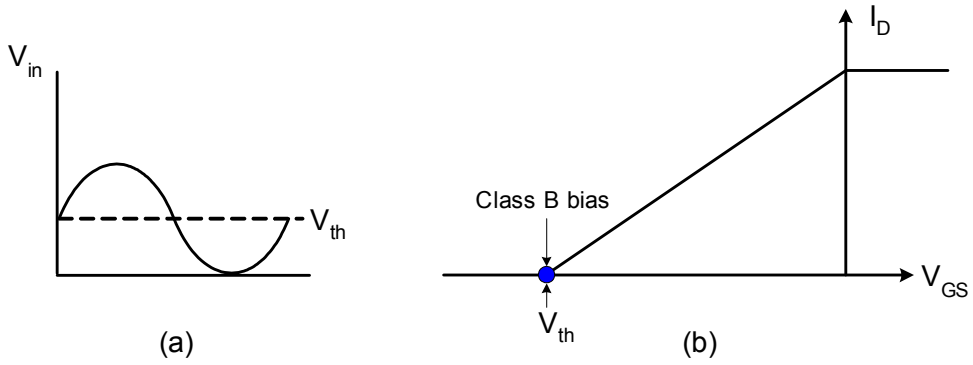


Figure 2.8. Class B PA: (a) input waveform, (b) bias point.

### 2.4.3 Class AB

The crossover distortion effect in Class B amplifiers can be minimized by biasing the gate in a way to produce a small quiescent drain current. This leads to the type of amplifiers called Class AB, where the transistor is biased above the threshold voltage but below the center of the load line (Figure 2.9). Class AB amplifier operation, as the name suggests, can be considered to be a compromise between Class A and Class B

operation. The conduction angle of a Class AB amplifier lies between 180º and 360º. By varying the conduction angle the amplifier can be made to behave more like a Class A or Class B amplifier. Hence the theoretical maximum efficiency of a Class AB amplifier is between 50% and 78.5%. Commercial Class AB amplifiers typically have much lower efficiencies in the order of 40-55%. A trade-off between linearity and efficiency can be achieved by simply changing the gate bias. Class AB amplifiers can also be realized in push-pull configurations even though single transistor configuration is preferred for high frequency linear operation.

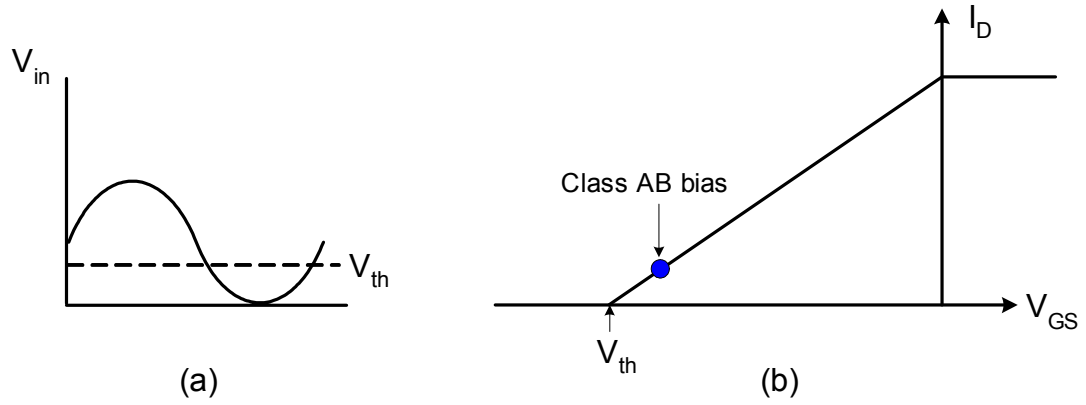


Figure 2.9. Class AB PA: (a) input waveform, (b) bias point.

### 2.4.4 Class C

A Class C power amplifier is a nonlinear power amplifier used in places where linearity is not a requirement and high efficiency is highly desired. Class C amplifiers are widely used in constant envelope modulation systems where linearity is not required. The transistor is biased below threshold for Class C operation and hence the device conduction angle varies from 0º to 180º (see figure 2.10). When a voltage signal is applied to the input, the transistor conducts only for the period of time when the input signal is greater than the threshold voltage. The transistor remains switched off at all other times. Since only a portion of the positive input voltage swing takes the device into the amplifying region the output current is a pulsed representation of the input. Due to this pulsed output current the input and output voltages are not linearly related. Thus the amplitude of the power amplifier output is highly distorted. The efficiency of a Class C amplifier depends on the conduction angle. The efficiency increases for decreasing conduction angle. The maximum theoretical efficiency of a Class C power amplifier is 100%. However this is obtainable only for a conduction

angle of 0º, which means that no signal is applied and this condition is of no interest. Commercially Class C amplifiers typically show an efficiency of 60% or more.

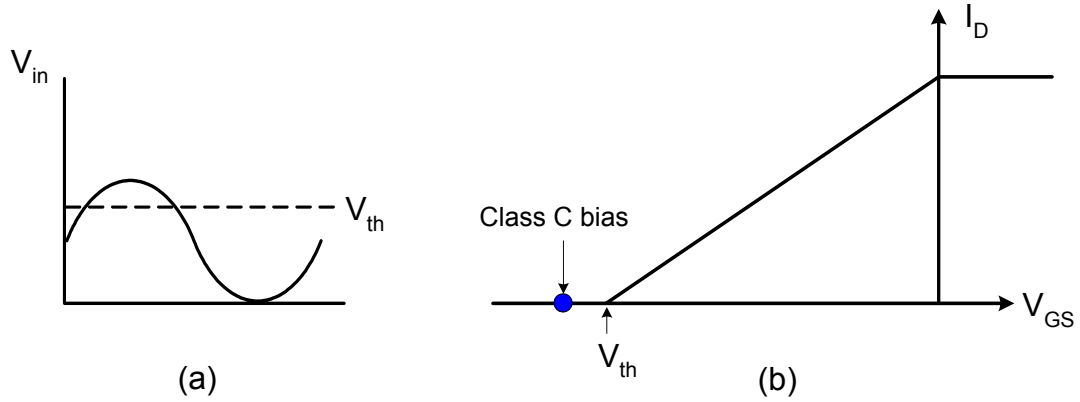


Figure 2.10. Class C PA: (a) input waveform, (b) bias point.

### 2.4.5 Class D

Class D PAs use two or more transistors as switches to generate a square drain-voltage waveform. Referring to the schematic diagram shown in figure 2.11, a series-tuned output filter passes only the fundamental-frequency component to the load, resulting in power outputs of $(8/\pi^2)V_{DD}^2/R_L$ for the transformer-coupled configuration. Current is drawn only through the transistor that is on, resulting in a 100-percent efficiency for an ideal PA. A unique aspect of class D (with infinitely fast switching) is that efficiency is not degraded by the presence of reactance in the load. Practical Class D PAs suffer from losses due to saturation, switching speed, and drain capacitance. Finite switching speed causes the transistors to be in their active regions while conducting current. Drain capacitances must be charged and discharged once per RF cycle. The associated power loss is proportional to $V_{DD}^3/2$ and increases directly with frequency [20]. Class-D PAs with power outputs of 100 W to 1 kW are readily implemented at RF, but are seldom used above lower VHF because of losses associated with the drain capacitance. Recently, however, experimental Class-D PAs have been tested with frequencies of operation as high as 1 GHz [21].

### 2.4.6 Class E

Class E employs a single transistor operated as a switch (Figure 2.12). The drain voltage waveform is the result of the sum of the DC and RF currents charging the drain-shunt capacitance. In optimum class E, the drain voltage drops to zero and has

zero slope just as the transistor turns on. Figure 2.13 shows the corresponding input and output waveforms in this case. The result is an ideal efficiency of 100 percent, elimination of the losses associated with charging the drain capacitance in Class D, reduction of switching losses, and good tolerance of component variation.

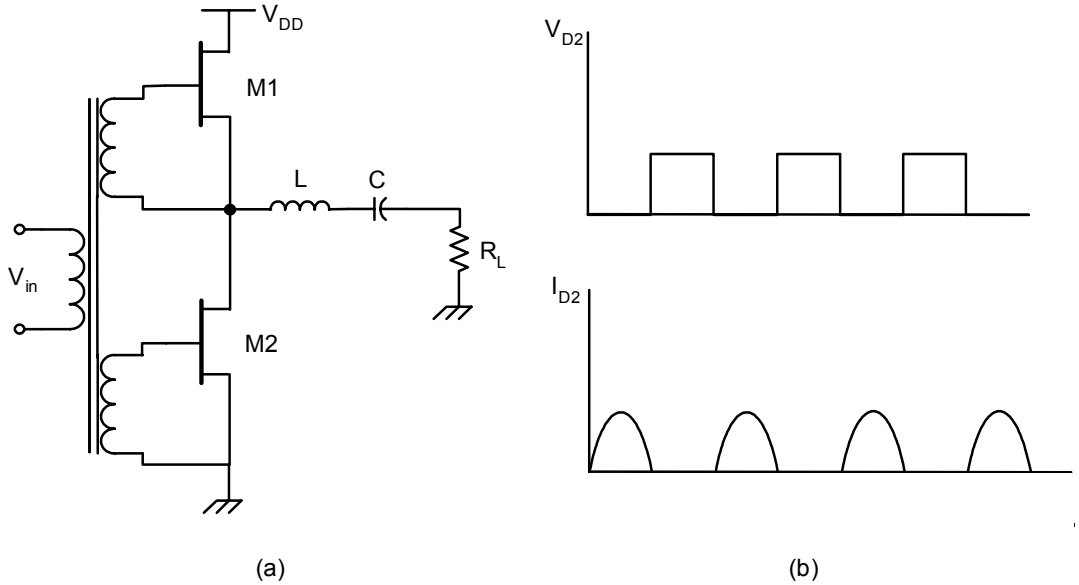


Figure 2.11. Class D PA: (a) circuit implementation, (b) ideal drain voltage and current waveforms.

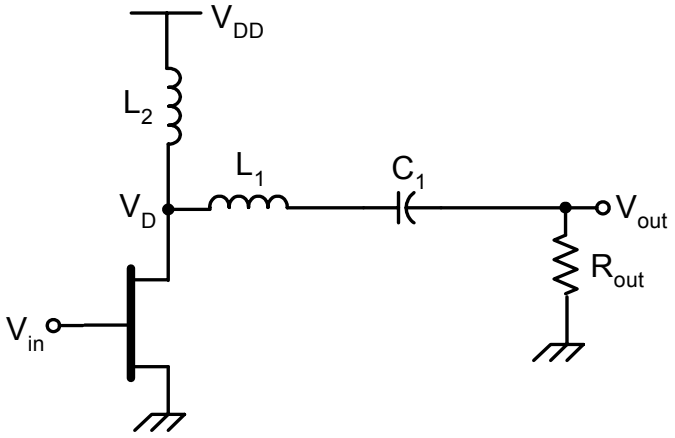


Figure 2.12. Class E PA implementation.

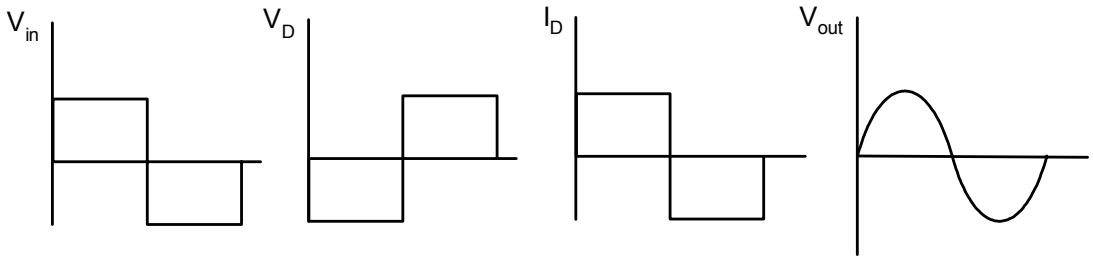


Figure 2.13. Class E PA waveforms.

However, variations in load impedance and shunt susceptance cause the PA to deviate from optimum operation [22, 23], but the degradations in performance are generally no worse than those for class A and B.

### 2.4.7 Class F

Class F amplifiers are usually considered as very high efficiency (80% or more power-added efficiency) amplifiers where the high efficiency is obtained through the use of harmonic traps (L-C filters or quarter-wavelength transmission lines), which provide suitable terminations (either open or short) for the generated harmonics (see figure 2.14). By doing this, a distorted wave drain voltage is produced (Figure 2.15). Since only a drain voltage or a drain current exists at any given time, the power dissipation is ideally zero resulting in 100% theoretical efficiency. These very high efficiency values are usually associated with poor linearity. However the linearity can be improved to meet the design standards but compromising on efficiency.

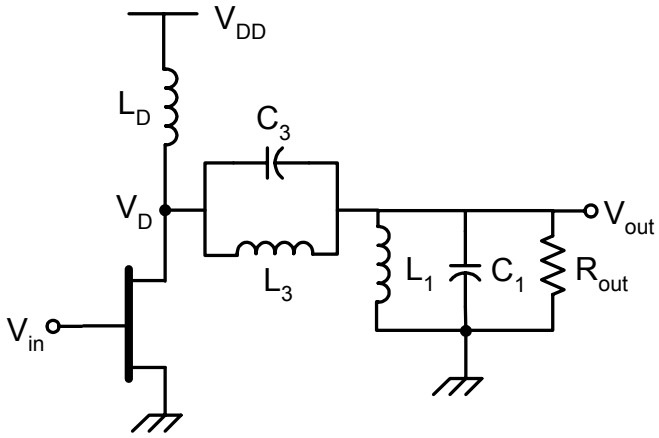


Figure 2.14. Class F PA implementation.

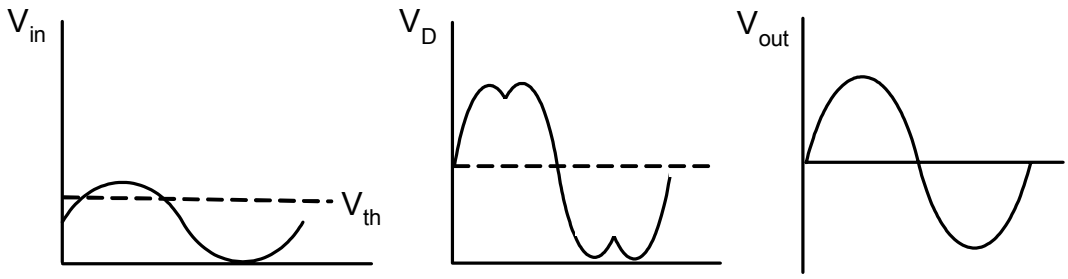


Figure 2.15. Class F waveforms.

# CHAPTER THREE

# SMALL SIGNAL MODELING OF SILICON-CARBIDE MESFETS

The strong interest in silicon carbide (SiC) MESFETs for RF and power applications necessitates an accurate model that is able to predict the device performance. Towards large signal modeling, this chapter introduces an accurate small signal parameter extraction procedure. Extrinsic parameters in both pinch-off and forward bias modes are extracted using cold FET technique whereas the intrinsic parameters are being extracted analytically at multiple bias points.

## 3.1 Why SiC MESFETs

Silicon carbide (SiC) has received remarkable attention during the last decade as a promising device material for high temperature, high frequency, and high power device applications due to its high thermal conductivity and high critical field for breakdown. The wide bandgap energy and low intrinsic carrier concentration of SiC allow it to maintain semiconductor behavior at much higher temperatures than silicon and GaAs technologies. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device doping. Depending upon specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300 °C. SiC's much smaller intrinsic carrier concentration theoretically permits device operation at junction temperatures exceeding 800 °C [4].

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized in SiC devices. Since power is a product of

voltage and current, it follows that high operating voltage can result in low current and high internal impedance. High internal impedance in turn can simplify impedance matching and result in efficient power coupling and broad bandwidth. The most beneficial inherent material superiorities of wide bandgap materials (SiC, GaN and Diamond) over silicon and GaAs as listed in table 3.1 are its high breakdown electric field, wide bandgap energy, high thermal conductivity, and high carrier saturation velocity.

The schematic structure of the MESFETs is shown in figure 3.1 [4]. It consists of a semi-insulating substrate, a p-type buffer layer, an n-type channel layer and an n+ contact layer. The current flow from the drain to the source is controlled by applying a negative voltage at the gate, which depletes the n-channel [24]. Principles of MESFET operation will be given in the next section in some detail.

| Property | Si | GaAs | SiC | GaN | Diamond |
|---|---|---|---|---|---|
| Bandgap, $E_g$ (eV) | 1.12 | 1.43 | 3.26 | 3.45 | 5.45 |
| Dielectric const. $\varepsilon_r$ | 11.9 | 13.1 | 10.1 | 9 | 5.5 |
| Electric Breakdown field, $E_c$ (kV/cm) | 300 | 400 | 2,200 | 2,000 | 10,000 |
| Electron mobility $\mu_n$ ($cm^2$/V.s) | 1,500 | 8,500 | 1,000 | 1,250 | 2,200 |
| Thermal conductivity, $\lambda$ (W/cm.K) | 1.5 | 0.46 | 4.9 | 1.3 | 22 |
| Saturated velocity, $v_{sat}$ (*$10^7$ cm/s) | 1 | 1 | 2 | 2.2 | 2.7 |

Table 3.1. Inherent material superiorities of wide bandgap materials over silicon and GaAs.

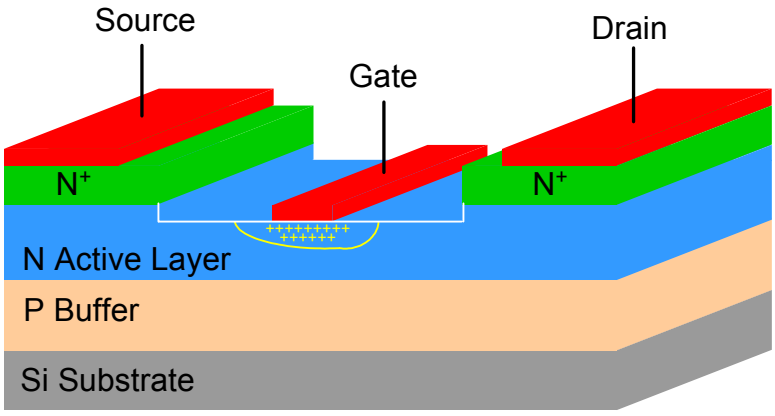


Figure 3.1. Perspective of SiC MESFET Structure.

## 3.2 Principles of the MESFET Operation

A MESFET device is a three-terminal device like any transistor [25], [26]. Since it is a FET, it has three electrodes drain, source, and gate as shown in figure 3.1. A MESFET device is biased by applying two voltages: $V_{GS}$ between gate and source and $V_{DS}$ between drain and source [18]. These voltages control the channel current between the drain and source by varying the height of the gate-depletion region and the longitudinal electric field. The operation can be explained qualitatively without going into deep physical analysis. If $V_{GS}$ is larger than the pinch-off voltage, three cases can be recognized for the $I_{DS}$-$V_{DS}$ characteristic curve of the MESFET, low $V_{DS}$ voltage where $I_{DS}$ is linearly proportional to $V_{DS}$, high $V_{DS}$ where the current is almost constant, and moderate $V_{DS}$ where $I_{DS}$ has nonlinear relationship of $V_{DS}$. Let first assume that $V_{GS} = 0$ and $V_{DS}$ is raised from zero to some low value as shown in figure 3.2 (a) [25]. When $V_{GS} = 0$, the depletion region under the Schottky-barrier gate is relatively narrow, and as $V_{DS}$ is raised, longitudinal electric field and current are established in the channel. Because of $V_{DS}$, the voltage across the depletion region at the drain end is greater than at the source end, so the depletion region becomes wider at the drain end. The narrowing of the channel and the increased $V_{DS}$ increase the electric field near the drain, causing the electrons to move faster. Although the channel depth, and in turn the channel's conductive cross section is reduced, the net effect is increased current. When $V_{DS}$ is low, the current is approximately proportional to $V_{DS}$. However, if the gate reverse bias is increased while the drain bias is held constant, the depletion region widens and the conductive channel becomes narrower, reducing the current. When $V_{GS} = V_p$, the pinch-off voltage, the channel is fully depleted and the drain current is zero, regardless of the value of $V_{DS}$. Thus, both $V_{GS}$ and $V_{DS}$ can be used to control the drain current. When the MESFET is operated under such bias voltages, where both $V_{GS}$ and $V_{DS}$ have a strong effect on the drain current, it is said to be in its linear or voltage controlled resistive region. If $V_{DS}$ is raised further, as shown in Figure 3.2 (b), while $V_{GS}$ is greater than the pinch-off voltage, the channel current increases, the depletion region becomes deeper at the drain end, and the conductive channel becomes narrower. The current clearly must be constant throughout the channel. As a result, and as long as the conductive channel near the drain becomes narrower, the electrons must move faster. However, the

electron velocity cannot increase indefinitely; the average velocity of the electrons in SiC cannot exceed the saturated drift velocity ($2x10^7$ cm/s). If $V_{DS}$ is increased beyond the value that causes velocity saturation (usually only a few tenths of a volt), the electron concentration rather than velocity must increase in order to maintain current continuity. Accordingly, a region of electron accumulation forms near the end of the gate. Conversely, after the electrons transit the channel and move at saturated velocity into the wide area between the gate and drain, an electron depletion region is formed. The depletion region is positively charged because of the positive donor ions remaining in the crystal. As $V_{DS}$ is increased further, as shown in figure 3.2 (c), progressively more of the voltage increase is dropped across this region to enforce the electrons to cross it and less is dropped across the unsaturated part of the channel. This region is called a dipole layer or charge domain.

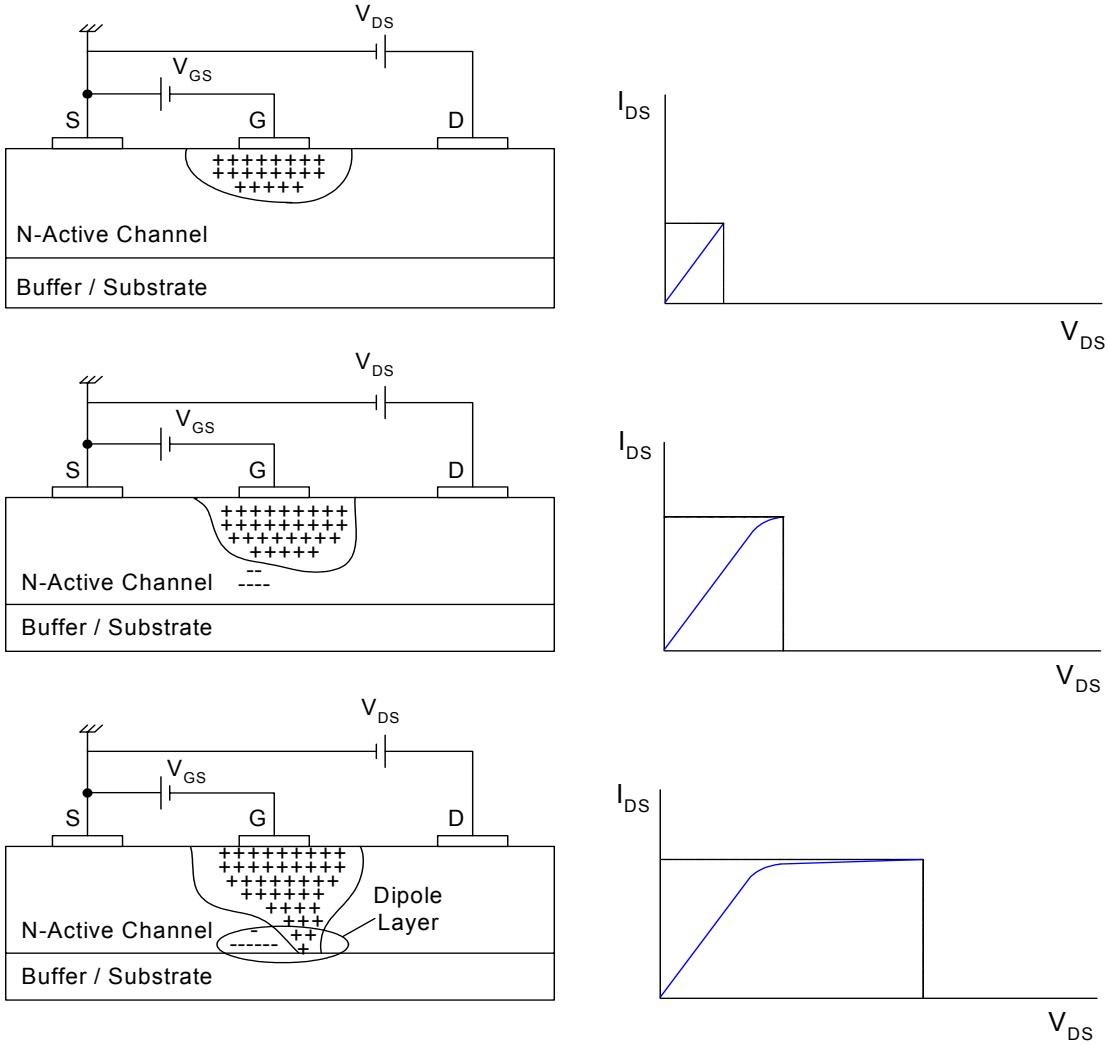


Figure 3.2. SiC MESFET operation under different $V_{DS}$ biasing with $V_{GS} < 0$: (a) Linear region ($V_{DS}$ is very low), (b) $V_{DS}$ at the onset of saturation, (c) $V_{DS}$ is high.

Eventually, a point is reached where further increase in $V_{DS}$ is dropped entirely across the charge domain and does not substantially increase the drain current. At this point, the electrons move at saturated drift velocity over a large part of the channel length. When the MESFET is operated in this manner, which is the normal mode of operation for small-signal devices, it is said to be in its saturated region. Accurate models may include the effect of the charge domain in some way. Therefore, some models include a capacitor between the drain and the gate-source equivalent circuit to account for the charge domain.

The small-signal model can be proposed based on the physical structure of the MESFET device. Most of the suggested models are based on the model shown in figure 3.3. This model is a lumped-element model, which is valid over a frequency range of several tens of GHz.

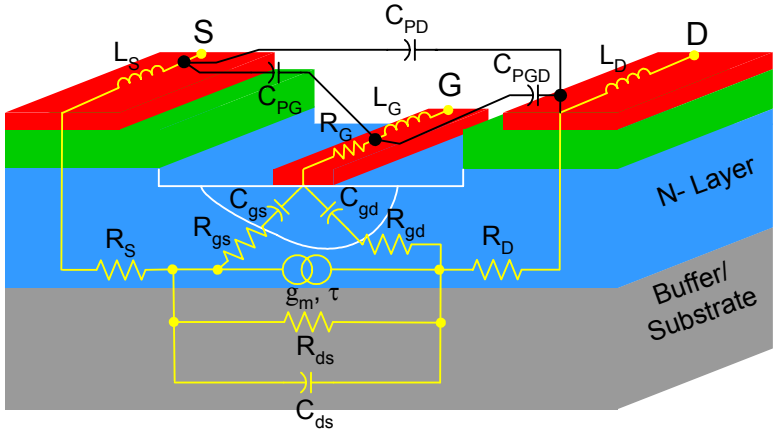


Figure 3.3. MESFET model showing physical origin of elements and the corresponding small-signal model.

The physical meaning of each element is clearly interpreted. $R_G$ is the ohmic resistance of the gate while $R_S$ and $R_D$ are the source and drain ohmic resistances, respectively. $L_G$ is the inductance of the gate while $L_S$ and $L_D$ are the inductances of the source and the drain metallization, respectively. $R_{gs}$ is the resistance of the semiconductor region under the gate, between the source and the channel. $C_{ds}$ the drain-source capacitance, which is dominated by geometric capacitance and is often treated as a constant. $C_{gs}$ and $C_{gd}$ are the channel capacitances, which in general are nonlinear. $I_{ds}$ is the controlled drain-source current from which the transconductane $g_m$, transit time delay $\tau$, and output resistance $R_{ds}$ can be calculated. $C_{PG}$, $C_{PD}$ and $C_{PGD}$ are the pad capacitances of gate, drain and gate-drain respectively.

If voltages are expected to be large enough to forward–bias or reverse avalanche breakdown the gate junction, one can include diodes in parallel with $C_{gs}$ and $C_{gd}$. Because operation with gate-channel avalanche breakdown or high values of rectified gate current usually destroys the device, some of the model elements are nonlinearly dependent on the internal voltages $V_{gs}$ and $V_{ds}$. Others are linear, or can be approximated as linear elements. $I_{ds}$, $C_{gs}$, and $C_{gd}$ are usually nonlinear elements for their strong dependence on $V_{gs}$ and $V_{ds}$. On the other hand, the circuit model can be divided into two parts: the extrinsic parameters and the intrinsic parameters. The intrinsic parameters characterize the active region under the gate and are functions of biasing conditions, whereas the extrinsic parameters depend, at least to a first order approximation, only on the technological parameters. The intrinsic parameters include $C_{gs}$, $R_{gs}$, $C_{gd}$, $g_m$, $\tau$, $R_{ds}$, and $C_{ds}$ whereas the extrinsic parameters include all other elements in the model $C_{PG}$, $C_{PD}$, $C_{PGD}$, $R_G$, $R_D$, $R_S$, $L_G$, $L_D$, and $L_S$. Some of the intrinsic elements can be assumed linear for their weak dependence on the internal voltages, those elements are $R_{gs}$, $\tau$, and $C_{ds}$. In contrast, some of the intrinsic elements may be nonlinear if their dependence on the internal voltages is significant. We will discuss the significance of each element of the small-signal model in the following subsections.

### 3.2.1 Parasitic Inductances

The parasitic inductances are the inductances of the extrinsic part of the circuit model, which include $L_G$, $L_D$, and $L_S$. Those inductances arise primarily from metal contact pads deposited on the device surface. For short gate length devices, the gate inductance is usually the largest of the three, although this is a function of the particular layout employed. The source inductance is often small. Note that these inductances exist for the bare Die device, so, any other inductances such as parasitic bond wire inductances or parasitic package inductances must also be accounted for in the complete circuit model of the packaged device.

### 3.2.2 Parasitic Resistances

The parasitic resistances $R_G$, $R_D$, and $R_S$ are also included in the extrinsic part of the circuit model. The resistances $R_S$ and $R_D$ are included to account for the contact resistance of the ohmic contacts between the metal electrodes and the N+ SiC as well

as any bulk resistance leading up to the active channel. The gate resistance $R_G$ results from the metallization resistance of the gate Schottky contact. All three resistances are on the order of a few ohms. Although measurements of $R_S$ and $R_D$ indicate a slight bias dependence in these values, they are held constant in the large-signal models commonly available in the commercial simulators nowadays. However, accurate models should take into consideration their bias dependence, especially if their values depend significantly on the bias voltages. All parasitic resistance values can be estimated either from forward DC conduction measurements or directly from S-parameters using Cold-FET technique. However, the latter technique is preferable for more accurate results because it calculates the resistance values from typical high frequency data at the bias point of concern.

### 3.2.3 Pad Capacitances

These capacitances are also included in the extrinsic part of the circuit model. The pad capacitances come from the stray capacitance between the metal pads. The pad capacitance consists of crossover capacitance of the metal lines and the capacitance between the pad and the back face of the semi-insulating substrate, which is usually connected to the source terminal. However, the crossover capacitance is usually much smaller than the substrate capacitance [27]. Three pad capacitances are often included in the circuit model: the gate pad capacitance $C_{PG}$, the drain pad capacitance $C_{PD}$ and the capacitance between the gate and drain pads $C_{PGD}$. On the other side, pad capacitances may be placed in two different positions in the model, either on the most outer terminals of the model or between the corresponding parasitic inductances and resistances as shown in figure 3.3. Pad capacitance values depend on the utilized layout. Pad capacitances can be estimated either from special structures without the active device or directly from S-parameter measurements using an optimization technique.

### 3.2.4 Intrinsic Capacitances

Intrinsic capacitances are indicated in the model by $C_{gs}$, $C_{gd}$, and $C_{ds}$. $C_{gs}$ and $C_{gd}$ model the change in the depletion charge with respect to the gate-source and gate-drain voltages, respectively. Figure 3.4 shows the depletion region beneath the gate for a symmetric structure where the gate is located directly in the middle of the gap

between the source and the drain terminals. Figure 3.4(a) represents the symmetric bias case in which $V_{gs} = V_{gd}$. Figure 3.4(b) represents the case in which the gate-drain reverse bias is greater than the gate-source reverse bias. This case represents the normal MESFET bias conditions in most applications. Figure 3.4 is used to clarify the physics of both $C_{gs}$ and $C_{gd}$. However, the discussion is also valid for any geometrical structure and bias conditions. The distribution of the depletion charge is symmetric with respect to the drain and source in Figure 3.4(a). On the other hand, the depletion charge extends deeper at the drain end of the gate than at the source end of the gate, and it also extends closer to the drain than to the source. This charge redistribution in the depletion region with the bias voltage variation identifies the two depletion capacitances $C_{gs}$ and $C_{gd}$. The charge of the depletion region is shared between $C_{gs}$ and $C_{gd}$. Thus, they should be defined carefully as:

$$C_{gs} = \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{V_{gd}=constant} \tag{3.1-a}$$

$$C_{gd} = \left.\frac{\partial Q_g}{\partial V_{gd}}\right|_{V_{gs}=constant} \tag{3.1-b}$$

Under normal operating conditions, $V_{gs}$ and $V_{ds}$ are the DC controlling bias voltages. For this reason, the gate to source capacitance is often defined as:

$$C_{gs} = \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{V_{ds}=constant} \tag{3.2}$$

Equations (3.1-a) and (3.2) are not equivalent, but slightly different quantities. The distinction is usually minor, but can be significant if calculations are based on a physically based model in which the depletion charge is defined by a mathematical expression. When capacitance is determined by measurements or derived from empirical models, the capacitance definition given by equations (3.1-a) and (3.2) are not applied. Instead, the capacitance values are defined in terms of an equivalent circuit, and so, the values are determined to accurately predict the device behavior. Thus, it does not matter in this thesis which definition of $C_{gs}$ should be taken because $C_{gs}$ is calculated from S-parameter measurements. One might also have noticed that the voltages indicated in the capacitance definitions are the internal voltages, not the external terminal voltages.

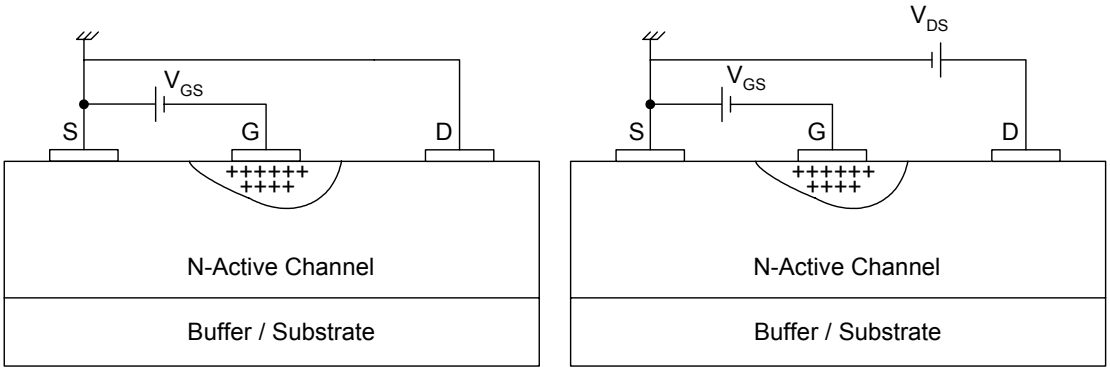


Figure 3.4. Depletion region shapes for different applied bias voltages: (a) gate-source voltage is equal to gate-drain voltage, (b) gate-drain reverse bias is greater than gate source reverse bias.

It is well known from depletion capacitance analysis that the depletion capacitance decreases as the reverse junction voltage increases. For this reason and under normal bias conditions, the gate-drain capacitance $C_{gd}$ is considerably smaller in magnitude than $C_{gs}$; nevertheless, $C_{gd}$ is critical for obtaining accurate S-parameter predictions. The drain-source capacitance $C_{ds}$ is included in the equivalent circuit to account for geometric capacitance effects between the source and drain electrodes. It is usually not considered to be bias dependent for the purposes of device modeling.

### 3.2.5 Charging Resistance $R_{gs}$

Although the charging resistance $R_{gs}$ represents the intrinsic resistance under the gate between the source and the channel, it is included primarily to improve the match to $S_{11}$. For many devices, however, the presence of $R_G$ is sufficient to match the real part of $S_{11}$. So, for power devices $R_{gs}$ is difficult to extract and is of questionable physical significance. The difficult discrimination between $R_{gs}$ and $R_G$ in the extraction process will be discussed in section 3.4.

### 3.2.6 Transconductance

The intrinsic gain mechanism of the MESFET is provided by the transconductance. The transconductance $g_m$ is a measure of the incremental change in the output current $I_{ds}$ for a given change in the internal input voltage $V_{gs}$. The internal input voltage is the voltage across the gate source junction. In other words, the device transconductance is defined as the slope of the $I_{ds}$-$V_{gs}$ characteristics with the drain-

source voltage held constant. The mathematical statement of this definition can be expressed as:

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=cons\tan t} \tag{3.3}$$

The transconductance of the device is one of the most important indicators of the device quality for microwave and millimeter wave applications. When all other characteristics are equal, a device with high transconductance will provide greater gain and superior high frequency performance. The transconductance suffers from what is called low frequency dispersion. The low frequency dispersion is the phenomenon of a parameter variation at low frequencies. The low frequency dispersion takes place as a result of the deep levels in the device structure. So, it significantly depends on the semiconductor material quality and fabrication processes. Therefore, the transconductance varies with frequency below a frequency of about 1 MHz. RF values of transconductance are typically 5 to 25% lower than DC values for a SiC MESFET. Transconductance values vary directly with gate width and inversely with gate length.

### 3.2.7 Transit Time

The transconductance cannot respond instantaneously to changes in the gate-source voltage. The delay inherent to this process is described by the transit time (transconductance delay) $\tau$. Physically, the transconductance delay represents the time it takes for the charge to redistribute itself after a fluctuation of the gate voltage. Typical values of $\tau$ are on the order of 1 psec. From physical considerations, transit time is expected to decrease with decreasing gate length.

### 3.2.8 Output Resistance

The output resistance $R_{ds}$ is the incremental resistance between drain and source, and it is more convenient to be explained in terms of its reciprocal, the output conductance $g_{ds}$. The output conductance is a measure of the incremental change in output current $I_{ds}$ with the output voltage $V_{ds}$. So, it can be defined as the slope of the $I_{ds}$-$V_{ds}$ characteristics with the gate-source voltage held constant. Mathematically, the output conductance and resistance can be defined by

$$g_{ds} = \frac{1}{R_{ds}} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=cons\tan t} \tag{3.4}$$

The output conductance of the device is an important characteristic in analog applications. It plays a significant role in determining the maximum voltage gain attainable from a device and is extremely important for determining optimum output matching properties. In general, it is desirable to have a device with extremely high output resistance, or equivalently, low output conductance. The low frequency dispersion is more significant in output conductance than in the transconductance. The RF output conductance can be more than 100% higher than the DC output conductance. The RF values for both transconductance and output conductance are of primary concern for small-signal modeling applications while both RF and DC values are important for accurate large-signal modeling.

## 3.3 Small Signal Modeling and Parameter Extraction

Figure 3.5 shows the most common MESFET model at normal bias conditions, i.e. the device is biased in the saturation region. Some of those elements can be neglected in the analysis later on. The model can be divided into two sections: the extrinsic element section and the intrinsic element section. The extrinsic section includes all extrinsic elements: $C_{PG}$, $C_{PD}$, $C_{PGD}$, $R_G$, $R_D$, $R_S$, $L_G$, $L_D$, and $L_S$. The intrinsic section includes all the intrinsic elements: $C_{gs}$, $R_{gs}$, $C_{gd}$, $R_{gd}$, $g_m$, $\tau$ , $R_{ds}$, and $C_{ds}$. The resistance $R_{gd}$ has been added to ensure smooth transition from the symmetric cold model ($V_{ds} = 0$) to operating points in the saturation region [27]. Although this element has little effect on the performance of the model and many authors neglect it, it was included here to present full analytical expressions.

The main concept of the extraction process, which is employed by many researchers, is to remove the extrinsic element section from the measurements to end up with Y-parameters of the intrinsic section. The Y-parameters are the most convenient parameters since the intrinsic section exhibits PI topology. The simple analytical expressions of the Y-parameters can be used to calculate the intrinsic elements.

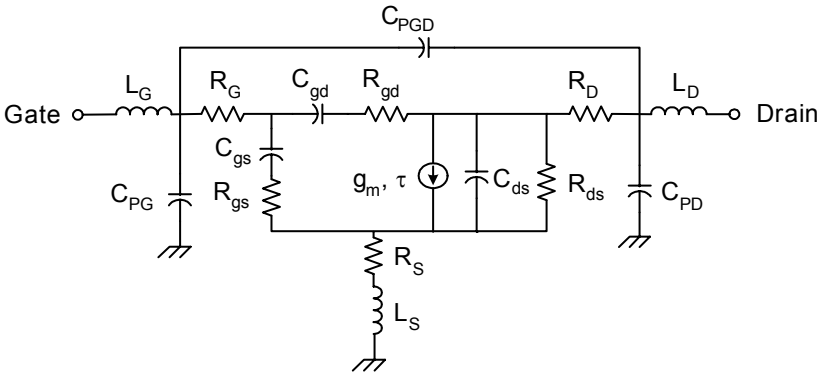


Figure 3.5. Small signal equivalent circuit of SiC MESFET.

### 3.3.1 Determination of the Intrinsic Y-Parameters

The process is depicted in figures (3.6- 3.9) [29]. We always start with the measured S-parameters ($S_{meas}$) of the device. S-parameters at the angular frequency (ω) are stored in the S-matrix. The S-matrix $S_{meas}$ is converted to the Z-parameters matrix $Z_{i3}$, the parasitic inductances $L_G$ and $L_D$ are subtracted as in figure 3.6.

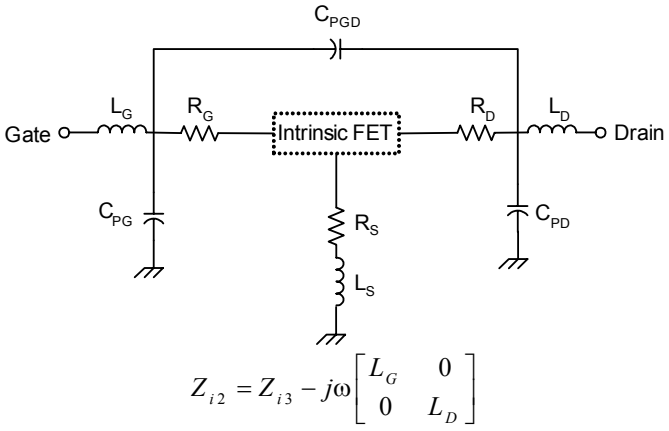


Figure 3.6. De-embedding of inductances $L_G$ and $L_S$: $S_{meas}$ ⇨ $Z_{i3}$.

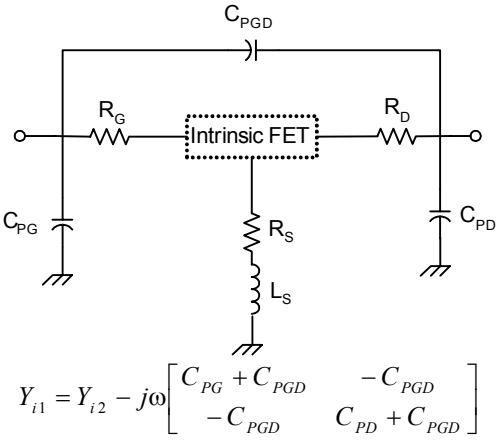


Figure 3.7. De-embedding of the parasitic capacitances $C_{PG}$, $C_{PGD}$ and $C_{PD}$: $Z_{i2}$ ⇨ $Y_{i2}$.

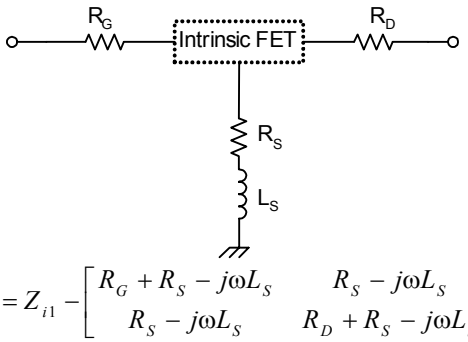


Figure 3.8. De-embedding of the resistances $R_G$, $R_D$ and $R_S$: $Y_{i1} \Rightarrow Z_{i1}$.

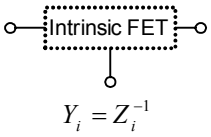


Figure 3.9. Converting of the intrinsic MESFET Z-parameters into Y-parameters: $Z_i \Rightarrow Y_i$.

In figure 3.7 Z-parameters $Z_{i2}$ are converted into Y-parameters $Y_{i2}$ and the pad capacitances $C_{PG}$, $C_{PGD}$ and $C_{PD}$ are then subtracted. The resulting Y-parameters $Y_{i1}$ are converted into $Z_{i1}$ to subtract the series resistances $R_G$, $R_D$ and $R_S$. This is shown in figure 3.8. The last step in calculating Y-parameters of the intrinsic device $Y_i$ is to convert $Z_i$ to $Y_i$ as shown in figure 3.9:

$$y_{11,i} = \frac{1}{R_{gs} + \frac{1}{j\omega C_{gs}}} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \tag{3.5-a}$$

$$y_{12,i} = -\frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \tag{3.5-b}$$

$$y_{21,i} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega C_{gs} R_{gs}} - \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \tag{3.5-c}$$

$$y_{22,i} = \frac{1}{R_{ds}} + j\omega C_{ds} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \tag{3.5-d}$$

In the mentioned process, we assumed that all the parasitic elements and pad capacitances are known either from other mathematical processes at different bias points or as optimized parameters.

### 3.3.2 Intrinsic Parameters in Terms of Intrinsic Y-Parameters

All intrinsic parameters can be extracted at each frequency point in terms of $Y_i$ data mentioned in equation (3.6). Solving for the MESFET intrinsic parameters, refer to Appendix B for more details, the intrinsic parameters can be stated as [29]:

$$R_{gs} = \mathrm{Re}\left(\frac{1}{y_{11,i} + y_{12,i}}\right) \tag{3.6}$$

$$C_{gs} = -\frac{1}{\omega\,\mathrm{Im}\left(\frac{1}{y_{11,i} + y_{12,i}}\right)} \tag{3.7}$$

$$R_{gd} = \mathrm{Re}\left(\frac{1}{-y_{12,i}}\right) \tag{3.8}$$

$$C_{gd} = \frac{1}{\omega\,\mathrm{Im}\left(\frac{1}{y_{12,i}}\right)} \tag{3.9}$$

$$R_{ds} = \frac{1}{\mathrm{Re}\left(y_{22,i} + y_{12,i}\right)} \tag{3.10}$$

$$C_{ds} = \frac{\mathrm{Im}\left(y_{22,i} + y_{12,i}\right)}{\omega} \tag{3.11}$$

$$g_m = \left|\left(y_{21,i} - y_{12,i}\right)\left(1 + j\omega C_{gs} R_{gs}\right)\right| \tag{3.12}$$

$$\tau = -\frac{1}{\omega}\arctan\left\{\frac{\mathrm{Im}\left\{\left(y_{21,i} - y_{12,i}\right)\left(1 + j\omega C_{gs} R_{gs}\right)\right\}}{\mathrm{Re}\left\{\left(y_{21,i} - y_{12,i}\right)\left(1 + j\omega C_{gs} R_{gs}\right)\right\}}\right\} \tag{3.13}$$

## 3.4 A Simplified Model of the MESFET at Pinch-off Mode

In this section, we will provide a much simpler analysis of a SiC MESFET model at a gate-source bias voltage less than or equal to the pinch-off voltage of the device, $V_p$, with zero drain-source bias voltage. The model itself is much simpler and seems to be highly symmetric; consequently, the associated analysis is much easier. At pinch-off voltages, the channel is closed and therefore it exhibits high resistance between the drain and the source. As a result, the dominant component between the drain and the source is $C_{ds}$.

There is no current flowing from drain to source and $g_m$ should be equal to zero. At pinch-off voltages, both the gate-source and the gate-drain junctions are deeply reverse biased; in turn $C_{gs}$ and $C_{gd}$ would be too small. Therefore, both $R_{gs}$ and $R_{gd}$

can be neglected. Figure 3.10 shows the simplified model of a SiC MESFET at pinch-off voltage with $V_{ds} = 0$ and $V_{gs} < V_p$.

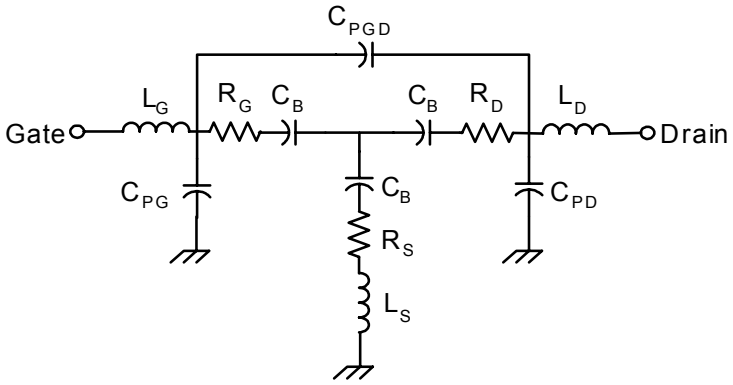


Figure 3.10. Simplified equivalent circuit at pinch-off mode.

Moreover, as $V_{ds} = 0$, the device structure is symmetric and therefore $C_{gs}$ should be equal to $C_{gd}$. This assumption will be used later on to calculate some extrinsic elements. This simple model of the MESFET device at pinch-off voltage is usually used to calculate the pad capacitances $C_{PG}$, $C_{PGD}$ and $C_{PD}$.

### 3.4.1 Determination of Pad Capacitances

At zero drain-source bias, and for a gate voltage lower than the pinch-off voltage, the intrinsic capacitance under the gate cancels out. Hence, the gate-source and gate-drain capacitances are dominated by the fringing capacitances $C_B$ attributed to the extension of the depleted layer at each side of the gate [32].

Moreover, all parasitic resistances and inductances have no influence on the imaginary part of the Y-parameters up to a few gigahertz (e.g. 5 GHz) since all the capacitances of the model are too small. As a result, one can remove the parasitic resistances and inductances from the model as a rational approximation. The reduced model in this case is shown in figure 3.11.

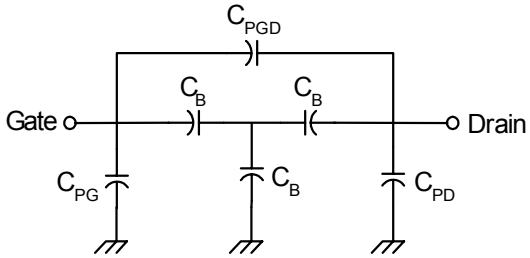


Figure 3.11. Simplified equivalent circuit in the pinch-off mode at low frequencies.

The analytical equations of the Y-parameters are very easy to determine from the equivalent circuit in figure 3.11:

$$\mathrm{Im}(Y_{11}) = \omega (C_{PG} + 2C_B / 3 + C_{PGD}) \tag{3.14}$$

$$\mathrm{Im}(Y_{12}) = \omega (-C_B / 3 - C_{PGD}) \tag{3.15}$$

$$\mathrm{Im}(Y_{22}) = \omega (C_{PD} + 2 C_B / 3 + C_{PGD}) \tag{3.16}$$

It is obvious that all imaginary parts of the Y-parameters are linearly proportional to the frequency. One may notice that we have three independent equations with four unknowns: $C_{PG}$, $C_{PGD}$, $C_{PD}$ and $C_B$. Unfortunately, this approach is not able to extract the parasitic capacitances directly from the measured Y-parameters. A simple and accurate approach to determine the parasitic capacitances in two steps is introduced:

1. Neglecting the effect of the parasitic capacitance $C_{PGD}$ for a moment, during which other parasitic capacitances $C_{PG}$ and $C_{PD}$ and the fringing capacitance $C_B$ can be simply extracted as follows:

$$C_B = -3\ \mathrm{Im}(Y_{12})/\omega \tag{3.17}$$

$$C_{PG} = \mathrm{Im}(Y_{11})/\omega - 2\ \mathrm{Im}(Y_{12})/\omega \tag{3.18}$$

$$C_{PD} = \mathrm{Im}(Y_{22})/\omega - 2\ \mathrm{Im}(Y_{12})/\omega \tag{3.19}$$

2. Using the two-point technique, at two different frequencies the extracted parasitic capacitance values are used in an optimization process based on assuming a start value for the capacitance $C_{PGD}$ minimizing the error between the measured and simulated imaginary part of the Y-parameters. The objective function (the error function) should be estimated to find its minimum. The objective function can be written in the following form:

$$\varepsilon = \sum_{ij=1}^{2} \left( \frac{\left| \mathrm{Im}\left(Y_{meas_{ij}}\right) - \mathrm{Im}\left(Y_{sim_{ij}}\right) \right|^2}{\left| \mathrm{Im}\left(Y_{meas_{ij}}\right) \right|^2} \right) \tag{3.20}$$

where $\mathrm{Im}(Y_{meas_{ij}})$ is the imaginary part of the measured Y-parameters, while $\mathrm{Im}(Y_{sim_{ij}})$ refers to the imaginary part of the simulated Y-parameters. If the value of $C_{PGD}$ does not result in the minimum of the objective function, the value of $C_{PGD}$ should be updated using an optimization algorithm and step 2 should be repeated. Otherwise, the value of $C_{PGD}$ can be considered as the optimum value. Figure 3.12 shows good agreement between the simulated and measured imaginary part of Y-

parameters at low frequencies. As a result, the optimization variable $C_{PGD}$ can then be extracted. Figure 3.13 depicts the extracted parasitic capacitances versus frequency according to equations (3.17-3.19). From this figure, the values seem to be constant along frequency (up to few gigahertz), the average values of these capacitances are then considered in the model [31].

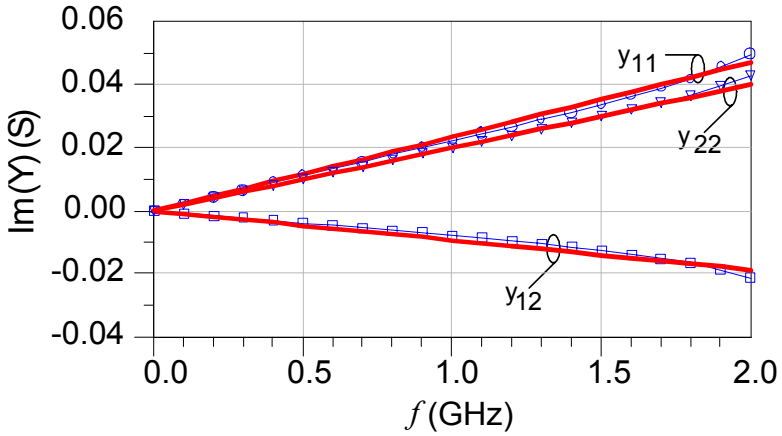


Figure 3.12. Simulated (solid lines) and measured imaginary part of Y-parameters after optimization process.

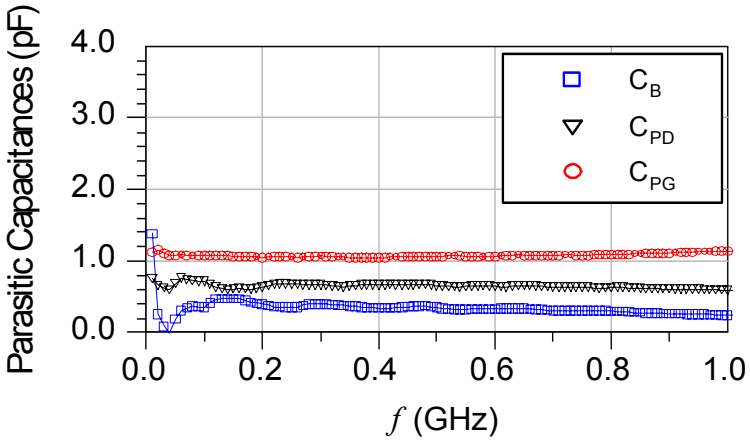


Figure 3.13. Extracted parasitic capacitances versus frequency.

## 3.4.2 Cold FET Measurements at Forward Bias

This case occurs when $V_{DS} = 0$ and $I_g >> 0$. Under this bias condition, the transistor is a nonlinear symmetric device. The intrinsic FET model is replaced by an appropriate diode model that depends on external gate voltage. Figure 3.14 shows the simplified circuit diagram in this mode.

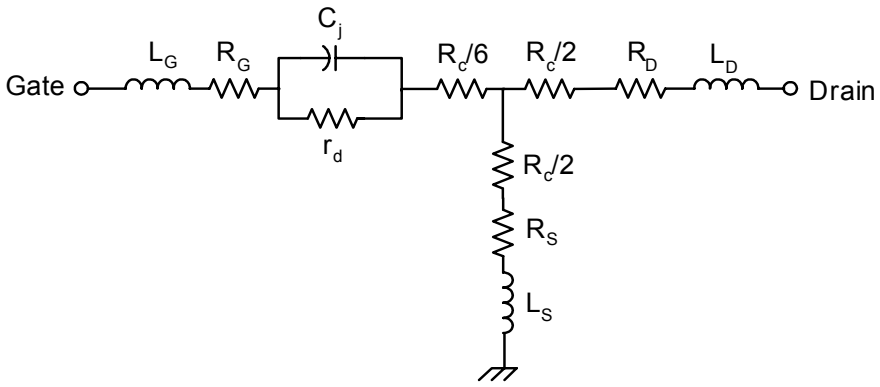


Figure 3.14. Simplified equivalent circuit at forward bias.

The parasitic inductances $L_G$, $L_D$ and $L_S$ as well as the parasitic resistances $R_G$, $R_S$ and $R_D$ can be determined. At this bias point, the following simplified equations given by [28], are valid:

$$Z_{11} = R_G + R_S + \frac{R_C}{3} + \frac{r_d}{1+\left(\omega\, r_d\, c_j\right)^2} + j\omega\left(L_G + L_S - \frac{c_j\, r_d^2}{1+\left(\omega\, r_d\, c_j\right)^2}\right) \tag{3.21}$$

$$Z_{12} = Z_{21} = R_S + \frac{R_C}{2} + j\omega\, L_S \tag{3.22}$$

$$Z_{22} = R_D + R_C + R_S + j\omega\left(L_S + L_D\right) \tag{3.23}$$

As the gate current increases, $r_d$ decreases and $c_j$ increases but the exponential behavior of $r_d$ versus $V_{gs}$ is the dominant factor; consequently the term $(r_d.c_j.\omega)$ tends to zero. In this case, we have

$$r_d = \frac{nkT}{q}\frac{1}{I_g} \tag{3.24}$$

For such a gate current, the capacitive effect of the gate disappears:

$$\mathrm{Re}\left(Z_{11}\right) = f\left(\frac{1}{I_g}\right) = R_G + R_S + \frac{R_C}{3} + r_d = R_G + R_S + \frac{R_C}{3} + \frac{nkT}{q}\frac{1}{I_g} \tag{3.25}$$

$$\mathrm{Im}\left(Z_{11}\right) = f\left(\frac{1}{I_g^{\,2}}\right) = \omega\left(L_G + L_S - c_j r_d^{\,2}\right) = \omega\left(L_G + L_S - c_j\left(\frac{nkT}{q}\right)^2\frac{1}{I_g^{\,2}}\right) \tag{3.26}$$

### 3.4.2.1 Determination of Parasitic Inductances

The source inductance $L_S$ can be determined easily from the imaginary part of $Z_{12}$ or $Z_{21}$. The drain inductance $L_D$ can then be obtained from the following equation:

$$L_D = \frac{1}{\omega}\left(Z_{22} - Z_{12}\right) \tag{3.27}$$

Now, in order to extract the parasitic gate inductance $L_G$, Eq. (3.26) can be reformed here as $Y = m\,X + C$, where

$$m = -c_j \left( \frac{nkT}{q} \right)^2 \text{ and } C = L_G + L_S \tag{3.28}$$

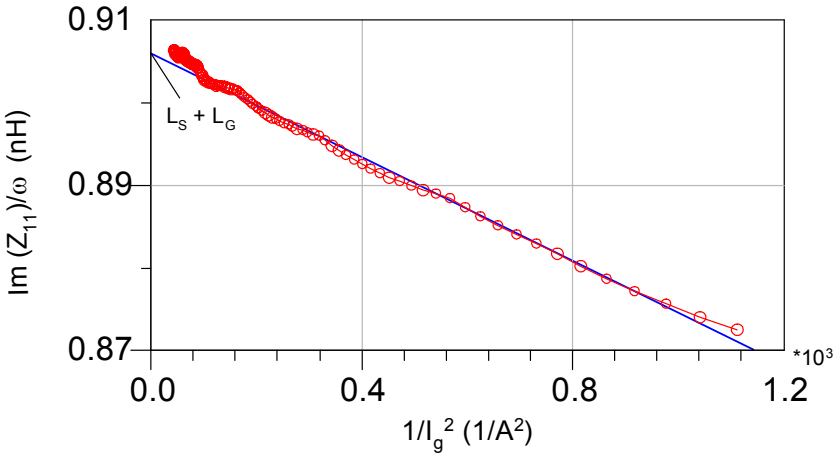


Figure 3.15. Dependency of $\mathrm{Im}(Z_{11})$ on gate current $(1/Ig^2)$.

This relation can be plotted at different gate currents. Using linear regression technique, the extrapolation of the linear relation results in sum of $L_S$ and $L_G$ at the intercept point of the ordinary axis as shown in figure 3.15. At this point, $I_g^2$ tends to infinity.

### 3.4.2.2 Determination of Parasitic Resistances

Extraction of the parasitic resistances may be considered difficult to obtain directly as in the parasitic capacitances extraction where there are four unknowns ($R_G$, $R_S$, $R_D$ and $R_C$) in three equations. Equation (3.25) can also be considered as linear equation. At various gate currents, the real part of $Z_{11}$ is plotted versus $(1/I_g)$. Using the linear regression technique, one can extrapolate the measurements along $(1/I_g)$ to get the intercept point with the ordinary axis at $R_G + R_S + R_C/3$. Figure 3.16 depicts the dependency of Re $(Z_{11})$ on the gate current $(1/I_g)$ (in circles) and the linear regression relation resulting in an extrapolated summation of the extrinsic resistances $R_G$, $R_S$ and the channel resistance $R_C$ as $I_g$ tends to infinity.

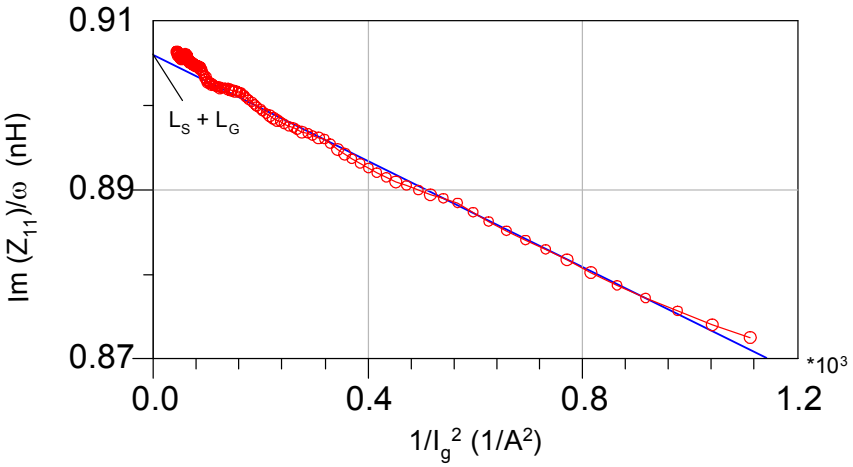


Figure 3.16. Dependency of Re ($Z_{11}$) on gate current ($1/I_g$).

Dependency of channel resistance $R_C$ on gate-source voltage ($V_{GS}$) has been studied. Hower and Bechtel [30] have estimated the sum of $R_D + R_S$ at $V_{DS} = 0$. Equation (3.23) is first modified as:

$$\mathrm{Re}(Z_{22}) = R_S + R_D + \frac{R_{C0}}{1 - \sqrt{\frac{V_{GS} - V_{bi}}{V_p}}} \tag{3.29}$$

where $R_{C0}$ is the independent voltage channel resistance, $V_{bi}$ is the built-in voltage that can be extracted from Schottky diode forward bias ($I_g$ vs $V_{GS}$) at $V_{DS} = 0$. At different positive gate-source voltages, the measured gate current ($I_g$) at $V_{DS} = 0$ is shown in figure (3.17). The intercept point of its slope to the X-axis ($V_{GS}$) is referred to $V_{bi}$.

The procedure of Hower and Bechtel is accomplished as follows:

1. The measured S-parameters (converted into Z-parameters) are given at different at $V_{GS}$ values between $V_p$ and $V_{bi}$.

2. The real parts of $Z_{22}$ are then plotted versus frequency; average values along different $V_{GS}$ values were extracted. These values are plotted versus $V_{GS}$.

A nonlinear equation in the form:

$$f(V_{GS}) = A + \frac{B}{1 - \sqrt{\frac{V_{GS} - V_{bi}}{C}}} \tag{3.30}$$

can be fitted to the measured Z-parameters Re ($Z_{22}$) along $V_{GS}$, the constants A, B and C of the fitted equation that refer to $R_S + R_D$, $R_{C0}$ and $V_p$, respectively can then be

extracted. Figure (3.18) illustrates the measured (in circles) and the fitted equation versus $V_{GS}$.

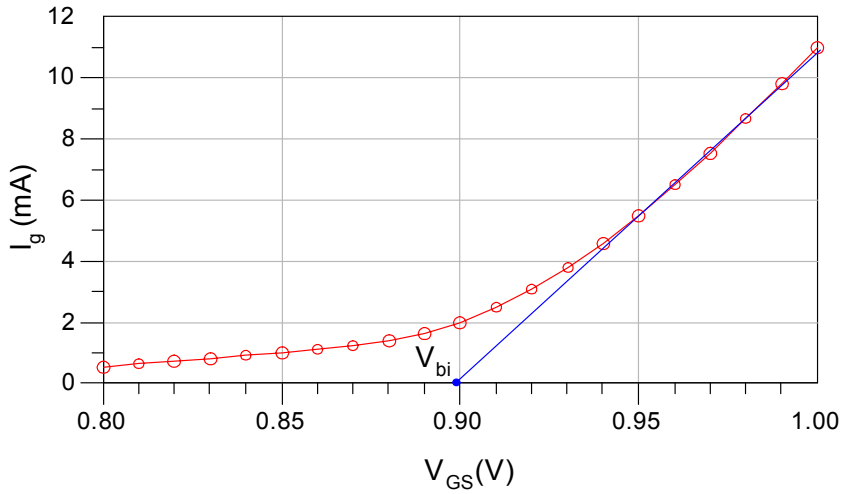


Figure 3.17. Extraction of diode built-in voltage from forward-bias diode characteristics at $V_{DS} = 0$.

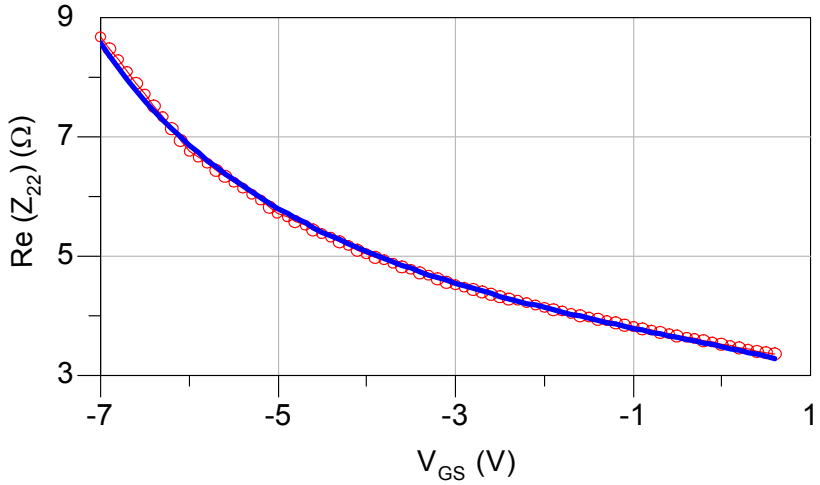


Figure 3.18. Extracted values of Re ($Z_{22}$) as a function of $V_{GS}$ between $V_p$ and $V_{bi}$; measurements (circles), curve fitting function (solid line).

To be sure that the extracted constants A and B are correct, linear regression technique can also be used here to extract these constants from the linear equation:

$$f(V_{GS}) = A + B\,x \tag{3.31}$$

where $x$ is given by

$$x = \frac{1}{1-\sqrt{\alpha}} \quad \text{and} \quad \alpha = \frac{V_{GS} - V_{bi}}{V_p} \tag{3.32}$$

Equation (3.31) can be plotted at various $V_p$'s. At the correct value of pinch-off voltage, a linear relation can be obtained. A and B can easily be extracted based on

the linear regression technique (LRT) as the intercept of the ordinary axis and the slope of the linear relation, respectively. This is illustrated in figure 3.19.

The difference between $R_D$ and $R_S$, which is defined by many authors as $\Delta R_{DS}$ can simply be obtained by solving equations (3.22, 3.23) resulting in [21, 33]:

$$\Delta R_{DS} = |R_D - R_S| = |\mathrm{Re}\,(Z_{22}) - 2\,\mathrm{Re}\,(Z_{12})| \tag{3.33}$$

Now, combining this equation and the extracted $(R_D + R_S)$ that are given by constant A from figure 3.19, both source and drain extrinsic resistances can be extracted. Then the channel resistance $R_C$ can be obtained from Eq. (3.22) followed by the extraction of parasitic gate resistance $R_G$ using Eq. (3.21).

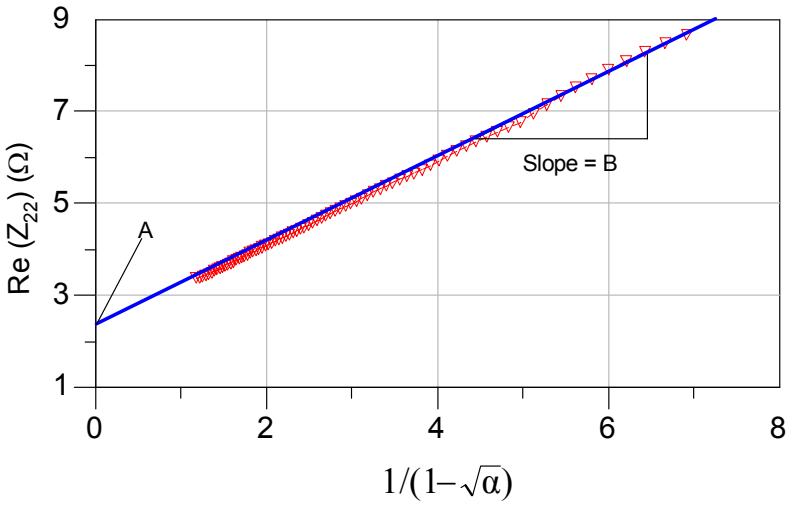


Figure 3.19. Modified diagram according to Eq. (3.31) at the exact value of pinch-off voltage; LRT in solid line resulting in $(R_S + R_D)$ extraction.

Table 3.2 summarizes all extracted values for the parasitic SiC MESFET equivalent circuit elements.

| | | | | | |
|---|---|---|---|---|---|
| $C_{PG}$ | 1 (pF) | $R_G$ | 1.2 Ω | $L_G$ | 0.88 (nH) |
| $C_{PD}$ | 0.6 (pF) | $R_D$ | 1.6 Ω | $L_D$ | 1 (nH) |
| $C_{PGD}$ | 0.2 (pF) | $R_S$ | 1 Ω | $L_S$ | 11 (pH) |

Table 3.2. Extracted extrinsic SiC MESFET equivalent circuit elements.

## 3.5 SiC MESFET Intrinsic Parameters Extraction

The extraction of the intrinsic small signal elements is based on the procedure given by Dambrine *et al* [29].These elements are determined from measured small signal parameters according to equations (3.6 – 3.13) as a function of frequency at a

given operating point $V_{gs}$, $V_{ds}$. All extracted elements are average values over all measured frequency points.

To get accurate and reliable values of the intrinsic parameters, the extracted values may be considered as starting values within an optimization process using Advanced Design System Simulation (ADS) of Agilent. Figure 3.20 illustrates the simulated and measured S-parameters on Smith diagram, covering the frequency band from 20 kHz to 4 GHz at $V_{gs}$ = -7 V and $V_{ds}$ = 30 V. The simulated S-parameters are in good agreement with the measured S-parameters. Similar results were obtained at different bias points. The return transmission parameter $S_{12}$ seems to have a relatively large discrepancy compared to the other parameters. This might be acceptable since the value of $S_{12}$ is small compared to $S_{21}$. All other measured and modeled S-parameters are almost coincided which shows how reliable our extraction procedure is.

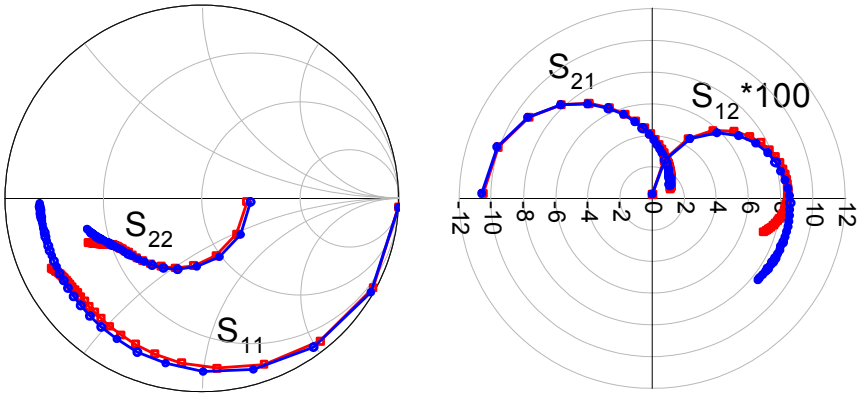


Figure 3.20. Measured (squares) and simulated (circles) S-parameters of SiC MESFET. Frequency range: 20 kHz to 4 GHz, $V_{ds}$ = 30 V and $V_{gs}$ = -7 V.

The extraction technique was applied to the measured S-parameters of the device at multiple $V_{gs}$ and $V_{ds}$ bias voltages. Figure 3.21 shows the extracted nonlinear parameters at multiple bias points.

Referring to $C_{gs}$ diagram (Figure 3.21 (a)), the graph seems physically meaningful. The value of $C_{gs}$ increases as $V_{gs}$ increases since the reverse bias voltage across the gate-source junction decreases. It is well known from the junction physics that the depletion capacitance increases as the reverse bias voltage decreases because the depletion region width decreases. Also, the value of $C_{gs}$ increases as $V_{ds}$ increases. The reason is, when $V_{ds}$ increases, the reverse bias voltage across the gate-drain junction increases, and in turn the gate-drain depletion width increases. On the other

hand, the gate-source depletion width reduces which results in higher values of $C_{gs}$. Since $V_{ds}$ does not directly affect the depletion width of the gate source junction, the dependence of $C_{gs}$ on $V_{ds}$ is not strong.

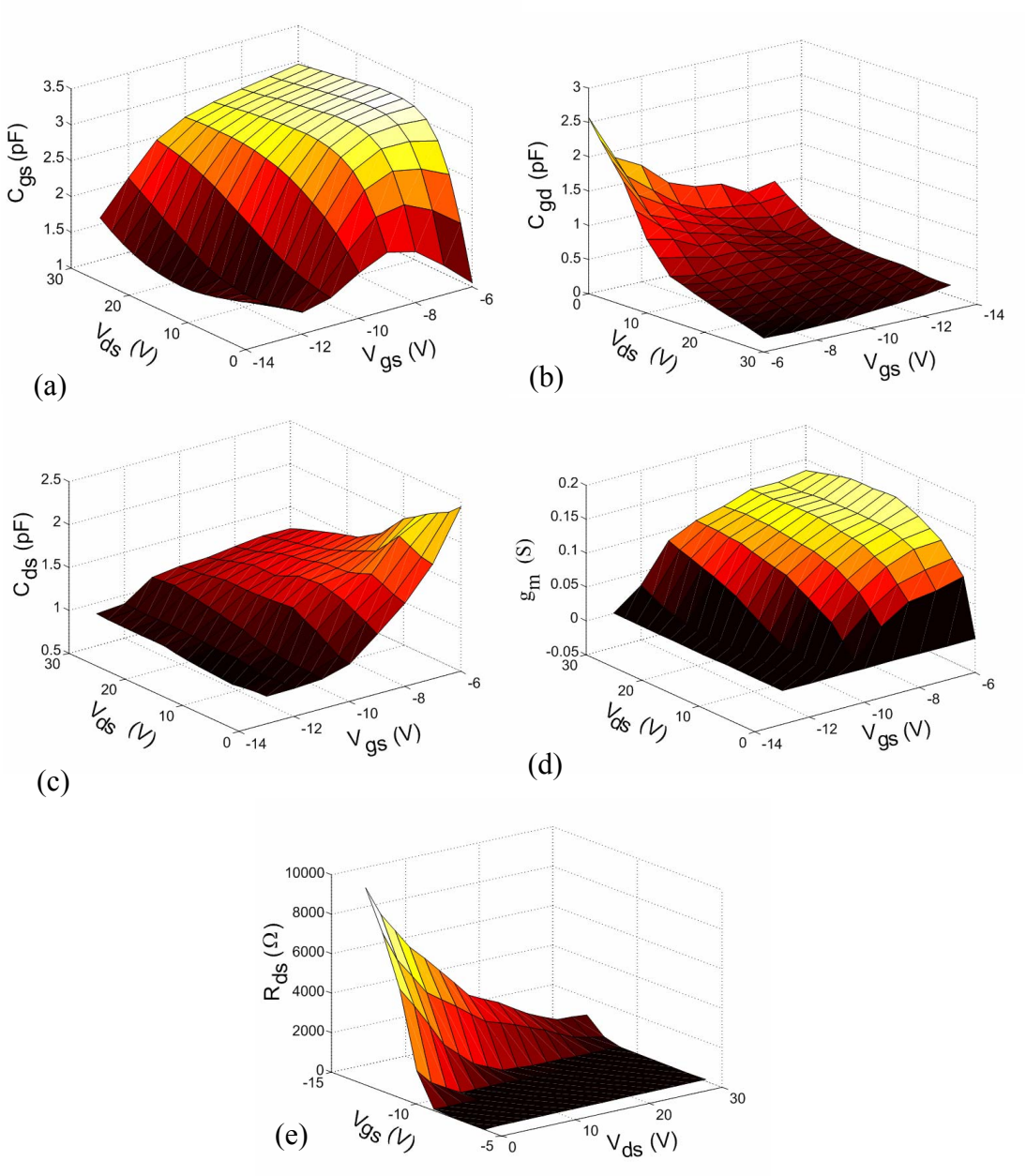


Figure 3.21. Extracted nonlinear parameters as a function of internal control voltages: a) gate-source capacitance, b) gate-drain capacitance, c) drain-source capacitance, d) transconductance and e) drain-source resistance.

Similar conclusions can be drawn from the $C_{gd}$ plot in figure 3.21 (b). The behavior is perfectly the opposite to that of $C_{gs}$ because increasing the depletion region width towards one side diminishes the depletion region width on the other side.

The characteristic of $C_{ds}$ is shown in figure 3.21 (c) which provides good evidence that $C_{ds}$ is less affected by the bias voltages specially for larger values of $V_{ds}$. Many authors, for this reason, assume that $C_{ds}$ is constant. However, $C_{ds}$ shows declination with $V_{gs}$ at smaller values of $V_{ds}$.

The transconductance $g_m$ is plotted in Figure 3.21 (d) which shows reduction in the value as $V_{gs}$ decreases. The plot supports the theoretical expectations. Since all values of $V_{ds}$ are in the saturation region, the dependence of $g_m$ on $V_{ds}$ is very slight in this region. Figure 3.21 (e) explains the dependence of $R_{ds} = 1/ g_{ds}$ on $V_{gs}$ and $V_{ds}$. $g_{ds}$ is highly dependent on $V_{gs}$ and weakly dependent on $V_{ds}$ in the saturation region. This observation is evident from the $I_{ds}$-$V_{ds}$ characteristic curves of MESFET devices.

# CHAPTER FOUR

# LARGE SIGNAL MODELING OF SIC MESFETS

The interest in power amplifier design based on SiC MESFET as a new technology necessitates the development of accurate large signal models that can predict the maximum output power level, achievable power added efficiency (PAE), intermodulation behavior and other nonlinear phenomena over the whole bias and frequency range, using harmonic balance (HB) simulation. This chapter presents a model incorporating empirical expressions for DC, capacitance and frequency dispersion. The accuracy of the new model will be verified in small signal as well as large signal performance.

## 4.1 Classification of device models

The goal in semiconductor device simulation is, of course, to maximize the physical accuracy and minimize the computational time and hardware required for performing the simulation. However, as these two demands usually are mutually exclusive, the complexity of the simulation model is adjusted to the minimal needs of the user. Simulation models can be divided into two categories: Physical models and empirical models.

### 4.1.1 Physical models

Physical models are based on the device physics. The model parameters are composed of geometrical and process parameters. The problem of physical modeling is that converting the semiconductor equations to voltage-current relations is not easy. Circuit models require currents and charges as explicit expressions of voltages and temperature. These functions are the solutions of the nonlinear semiconductor equations, and usually they do not have expressions in closed form. Several

approximations have to be made and accuracy is degraded. There are special device simulators that solve the equations in 2D or 3D, but this kind of modeling is too heavy for circuit simulation where the circuit can consist of thousands of devices. Physics-based models are not very flexible. They are valid for limited device topologies.

There are two principal types of physical models that are applied to device design and characterization. The most straightforward of these is based on a derivative of equivalent- circuit models, where the circuit element values are quantitatively related to the device geometry, material structure, and physical processes. The second approach is more fundamental in nature and is based on the rigorous solution of the carrier transport equations over a representative geometrical domain of the device. These models use numerical solution schemes to solve the carrier transport equations in semiconductors often accounting for hot electrons, quantum mechanics (HEMTs), EM, and thermal interaction. In particular, a key advantage is that physical models allow the performance of the device to be closely related to the fabrication process, material properties, and device geometry. This allows performance, yield, and parameter spreads to be evaluated prior to fabrication, resulting in a significant reduction in the design cycle (and cost). Furthermore, since physical models can be embedded in circuit simulations, the impact of device–circuit interaction can be fully evaluated. A further advantage of physical models is that they are generally intrinsically capable of large-signal simulation. Physical models have been implemented using either analytical expressions or numerical algorithms. Snowden's text [34] provides a useful summary. Analytical models clearly have the advantage of rapid solution, requiring only modest computation (possible on a modern programmable calculator), whereas numerical models require a greater amount of computational power and effort. The speed of many numerical models is no longer prohibitive for CAD and models can be fully evaluated in seconds on more powerful desktop computers. The tradeoff between analytical models and numerical models is usually considered in terms of speed and accuracy—many of the analytical models lack the detail and fidelity of their numerical counterparts.

Early analytical models of microwave FETs were based on derivatives of proven JFET models, such as that of the Lehovec and Zuleeg's model published in 1970 [35]. In 1974, Pucel *et al.* [36] introduced a physical analytical model for MESFETs based

on a two-region (ohmic and saturation) description of device operation. Equivalent-circuit element values for the intrinsic device were predicted from the model. Ladbrooke [37] described comprehensive physics-based equivalent-circuit models for MESFETs and HEMTs, taking into account surface effects and dispersive trapping phenomena [37] (see also [38]). Many of the analytical transistor models derive from charge-control analysis, originally proposed by Johnson and Rose in 1959. Ando and Itoh's 1990 paper presented a more recent model for HEMTs [39]. Shur proposed an easily implemented analytical model for GaAs MESFETs in 1978. Delagebeaudeuf and Linh described an analytical treatment for early studies on HEMTs in 1982. Trew *et al.* [41], [42] reported a model that is particularly suited to large-signal characterization of FETs. The most common approach to physical modeling relies on 2-D simulations, solving the drift-diffusion or energy-transport approximations for cross sections of the semiconductor devices. This type of model, which has been applied to silicon bipolar transistors, MOSFETs, MESFETs, HBTs, and HEMTs, is now highly developed and several commercial simulators exist. However, even with the advent of powerful workstations and advanced numerical techniques, this class of model remains relatively slow, requiring many thousands of CPU seconds to simulate even a small number of bias points. Recent work has focused on EM interaction with the device, such as in Megahed and El-Ghazaly's work (see [42]).

Fast numerical algorithms and models developed over the past ten years have led to the introduction of commercial microwave CAD software that is orders of magnitude faster than earlier physical models. An important example of this class of simulator uses algorithms based on a quasi-two-dimensional (Q2D) descriptions, pioneered by Carnez and Cappy *et al.* [40], Snowden and Pantoja [44], Sandborn *et al.*, and Cook and Frey [45], have already been shown to be an effective and accurate method of representing short-gate length MESFETs. More recently, HEMT models, such as those of Morton and Drury [46], incorporating a quantum mechanical charge-control model, have been shown to provide excellent agreement between measured and simulated data up to at least 100 GHz. Cappy's group extended the Q2D model to include noise analysis in their HELENA program. Snowden's team focused on the application of these models to microwave and millimeter-wave CAD and especially large-signal analysis and, in 1997, their Leeds physical model was integrated into the

Hewlett-Packard Microwave Design System. The Q2D FET models are based on the efficient numerical solution of a coupled set of transport equations, which describe conservation of carrier density, momentum, and energy. Recent work has lead to the incorporation of electrothermal effects into FET and HBT models, which requires the coupled solution of the transport equations and heat generation/flow equations. The challenge of electrothermal modeling requires the temperature within the active device to be related not only to the self-heating of the device in question, but also to that of adjacent elements, and is also a strong function of the die dimensions, mounting surface and ambient temperatures.

Other temperature-dependent phenomena which are known to be important in limiting the performance of microwave transistors, include trapping effects and breakdown, can be addressed in this type of simulation. It should be noted that it is generally necessary to consider a 3-D domain to achieve accurate electrothermal modeling, and this increases the computational burden.

### 4.1.2 Empirical models

Empirical or semi-empirical models are best suited for circuit simulation purposes. The equivalent circuits are usually based on the device physics but the voltage-current and voltage-charge relations of the elements may be partly or very heuristic. For example, the famous hyperbolic expression of drain current in the Curtice model [47] and many other models are not based on the physics of the device. The characteristics just resemble tanh curves, and the tanh function was chosen to approximate the measurement data. Empirical and semi-empirical models are flexible. The model parameters can be fitted to various devices based on measurements. Perhaps the most significant work on microwave transistor equivalent-circuit modeling for MESFETs and high electron- mobility transistors (HEMTs) occurred from 1975 to 1990, when the foundations were laid for all the models used in today's CAD. One of the first large-signal equivalent-circuit FET models was proposed by Van Tuyl and Liechti in 1974, which was later simplified by Curtice in 1980, who introduced a "quadratic model," using a square law dependency for the "ohmic" region and a function to model saturation in the drain–source current (see [48]). It was well suited to dc and small-signal characterization, although it had shortcoming at low values of $V_{ds}$ and for negative values of $V_{ds}$. Several enhancements to this model

followed, notably the popular cubic model developed with Ettenburg in 1985. Tajima's models of 1981 and 1984 achieved a very good fit to dc characteristics and were used in large-signal analysis. Materka and Kacprzak introduced a more tractable model in their 1983 and 1985 papers (see [49]) based on Taki's 1978 model, with fewer parameters, which again provided good fits to measured dc data. Statz *et al.*'s 1987 model [50] (also known as the Raytheon model) also demonstrated good accuracy, overcoming some of the limitations of the early Curtice model, although it still omitted some effects such as pinch off voltage dependency on $V_{ds}$. Statz's model, like that of Larson's 1987 model, used a polynomial fit for the current saturation regime. A modified form of the Statz model was developed by Triquint, designated the Triquint's Own Model (TOM), which improved the accuracy. Jastrzebski's model from the same era followed the more common formulation. The Root model, which was developed explicitly for CAD, is an excellent example of the later type of microwave FET model [47]. In 1992, Angelov *et al* [51], has added more degrees of freedom on Chalmers model (see also [52]). Most of these models are empirical in nature, requiring extensive dc and RF data to obtain good fits to measured results. Many of these models have been used in the most commercial simulators. Golio's books provide a very good review of many of these models [43], [53 - 54]. Many of the original MESFET models have been modified for use with HEMTs, by changing the transconductance and capacitance formulations. Notable examples are the Curtice, Materka-Kacprzak [49], and Angelov [52] models. The HEMT is generally a little more difficult to model, although excellent agreement between modeled and measured data is frequently obtained, as in Brazil's more recent models [55].

## 4.2 Model Description

Our approach is based on a multiple bias small signal model. The extrinsic elements of the small signal model are extracted from Cold-FET operation whereas the intrinsic parameters are calculated directly from measured network parameters at various bias points as presented in chapter 3. The equivalent circuit of the proposed nonlinear model is shown in figure 4.1. The nonlinear elements are the gate-drain diode $d_{gd}$, the gate-source diode $d_{gs}$, the static drain current source $I_{dsDC}$, the gate-

source capacitance $C_{gs}$, the gate-drain capacitance $C_{gd}$, and the drain-source capacitance $C_{ds}$ as well as the dispersion current source $I_{dsRF}$.

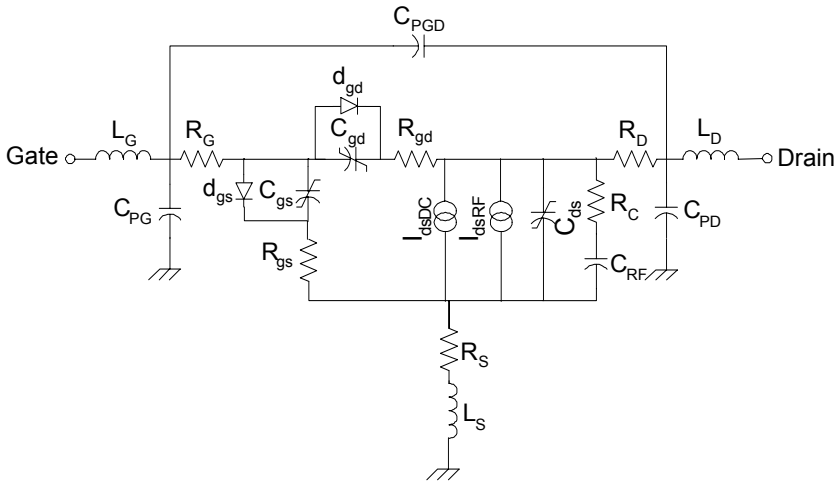


Figure 4.1. Large signal model of SiC MESFET

### 4.2.1 DC Characterization

Description of the drain-source current ($I_{ds}$) dependency of gate-source and drain-source voltage by algebraic expressions is presented in the models used in the commercial simulators. In this section, examples of simulated versus measured I-V characteristics for a SiC MESFET are given for some models. The DC model parameters have been obtained after optimization using the Advanced Design System simulator (ADS). Based on this process, the average absolute difference between simulated and measured drain current can be minimized. An objective function ε is defined in equation (4.1) to compare the deviations between the simulation using ADS and the measurements:

$$\varepsilon = \frac{1}{N}\sum_{i}\left\{\frac{\left|I_{ds,m} - I_{ds,s}\right|^2}{I_{ds,m}{}^2}\right\} \tag{4.1}$$

where N is the number of bias points. Based on the minimum value of the error function, the derived model can be considered more accurate compared to the other CAD models. The model parameters and the values of the error function for the used models are listed at the end of the section.

### 4.2.1.1 Curtice Cubic Model

The cubic model by Curtice and Ettenberg [48] relies on a third-order polynomial to model the saturation current as a function of both $V_{gs}$ and $V_{ds}$:

$$I_{ds} = \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right)\tanh\left(\gamma_2 V_{ds}\right), \tag{4.2}$$

where

$$V_1 = V_f\left(1+\beta_2\left(V_{ds0} - V_{ds}\right)\right), \tag{4.3}$$

The tanh function is used to model the switchover between the linear and saturation region, $\gamma_2$ being the saturation parameter. $\beta_2$ models the pinch-off voltage dependence on the drain-source voltage. Parameters $A_0$, $A_1$, $A_2$ and $A_3$ are polynomial fitting coefficients, and $V_{ds0}$ is the drain-source voltage at which the polynomial coefficients are evaluated. The simulated results in figure 4.2 give good agreements to the measurements in the linear region, however slight differences between them can be noticed in the saturation region. Table 4.1 presents the extracted model parameters.

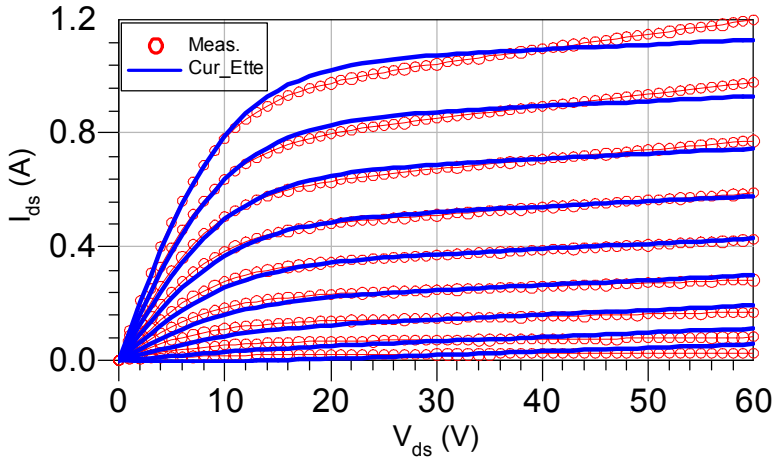


Figure 4.2. Measured (symbols) and calculated (solid lines) DC characteristics of the CRF24010 based on Curtice cubic model, $V_{gs}$ = –13 V to –5 V, step 1 V.

| Model Parameter | $A_0$ (A) | $A_1$ (A/V) | $A_2$ (A/V$^2$) | $A_3$ (A/V$^3$) | $V_{ds0}$ (V) | $\gamma_2$ (1/V) | $\beta_2$ (1/V) |
|---|---|---|---|---|---|---|---|
| Value | 1.987 | 0.167 | -8.45e$^{-3}$ | -7.3e$^{-4}$ | 12.12 | 0.099 | 6.1e$^{-4}$ |

Table 4.1. Extracted DC parameters of Curtice cubic model.

### 4.2.1.2 Materka-Kacprzak Model

The drain-current in Materka-Kacprzak model [49] is given by

$$I_{ds} = \left(I_{dss} + S_s V_{ds}\right)\left(1 - \frac{V_{gs}}{V_{th} + \gamma V_{ds}}\right)^{E + K_E V_{gs}} \tanh\left(\frac{S_L V_{ds}}{I_{dss}\left(1 - K_G V_{gs}\right)}\right) \qquad (4.4)$$

where $I_{dss}$ is the saturation current for $V_{gs} = 0$, $V_{th}$ the threshold voltage, $\gamma$ the drain voltage dependence of the threshold voltage, and $S_L$ and $K_G$ the linear region drain and gate slope parameters. The parameters E and $K_E$ modify the quadratic behavior. E is the constant, and $K_E$ is the $V_{gs}$-dependent part of the exponent. $S_s$ is the $V_{ds}$ slope parameter in the saturation region. The resulting DC simulations based on this model together with measurements are illustrated in figure 4.3. Better agreement can be achieved. The model parameters are extracted and depicted in table 4.2. A summary of the results will be given at the end of the section.

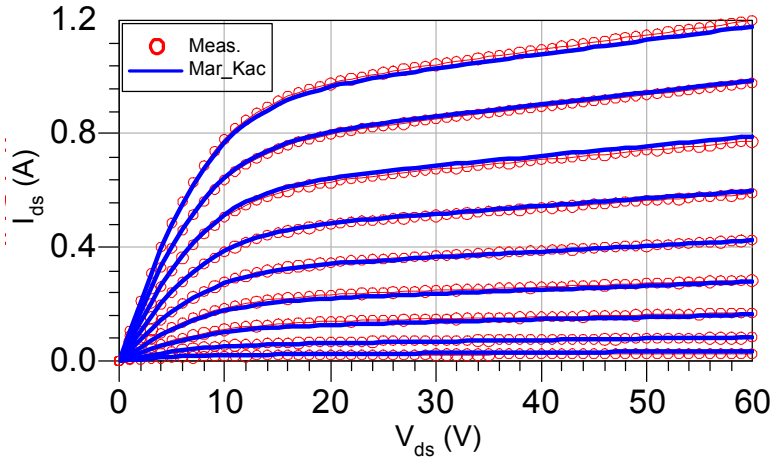


Figure 4.3. Measured (symbols) and calculated (solid lines) DC characteristics of the CRF24010 based on Materka-Kacprzak model, $V_{gs}$ = –13 V to –5 V, step 1 V.

| Model Parameter | $I_{dss}$ (A) | $S_s$ (S) | $S_L$ (S) | E (1/V) | $K_E$ (1/V) | $K_G$ (1/V) | $V_{th}$ (V) | $\gamma$ (1/V) |
|---|---|---|---|---|---|---|---|---|
| Value | 1.29 | $6.7e^{-2}$ | $-8.45e^{-2}$ | 0.145 | -0.183 | $-7e^{-3}$ | -13.2 | $-5.9e^{-3}$ |

Table 4.2. Extracted DC parameters of Materka-Kacprzak model.

### 4.2.1.3 Statz Model

The model by Statz *et. al*. [50], also called the Raytheon model, is based on the tanh model, but has two main improvements that make it very interesting. $I_{ds}$ is calculated as:

For $0 < V_{ds} < \frac{3}{\alpha}$

$$I_{ds} = \frac{\beta\left(V_{gs} - V_{th}\right)^2}{1+\Theta\left(V_{gs} - V_{th}\right)}\left[1-\left(1-\frac{\alpha V_{ds}}{3}\right)^3\right]\left(1+\lambda V_{ds}\right) \tag{4.5}$$

For $V_{ds} \geq \frac{3}{\alpha}$

$$I_{ds} = \frac{\beta\left(V_{gs} - V_{th}\right)^2}{1+\Theta\left(V_{gs} - V_{th}\right)}\left(1+\lambda V_{ds}\right) \tag{4.6}$$

The middle term in the expression for the linear region is a polynomial approximation of the tanh function that saves computation time without sacrificing too much accuracy. It is replaced by one in the saturation region. The denominator containing the parameter Θ is empirically chosen to give a good fit for both large and small values of ($V_{gs}$ - $V_{th}$). It has been shown that the current of a MESFET can be well described by a quadratic expression only near the pinch-off point, elsewhere the behavior is better described by a square root expression, which behaves quite linearly at high $V_{gs}$ values. The use of the denominator smoothly connects the quadratic law at low $V_{gs}$ values to the linear behavior at high $V_{gs}$ values. Measured and calculated DC characteristics based on this model are shown in figure 4.4. from the figure it is observed that a very good matching between the measured and the simulated DC characteristics and it may be considered the most accurate one compared to the previous models.

### 4.2.1.4 TOM3 Model

This model can predict the negative output conductance in the high dissipated power region, which occurs due to self-heating. The TOM3 DC drain-source current is calculated using the following equations [56]:

$$I_{ds} = \beta\left(V_G\right)^Q\left(1+\lambda V_{ds}\right)\frac{\alpha V_{ds}}{\left(1+\left(\alpha V_{ds}\right)^k\right)^{\frac{1}{k}}} \tag{4.7}$$

where

$$V_G = QV_{st}\ln\left(1+e^u\right) \tag{4.8}$$

$$u = \frac{V_{gs} - V_{th} + \gamma V_{ds}}{QV_{st}} \tag{4.9}$$

and

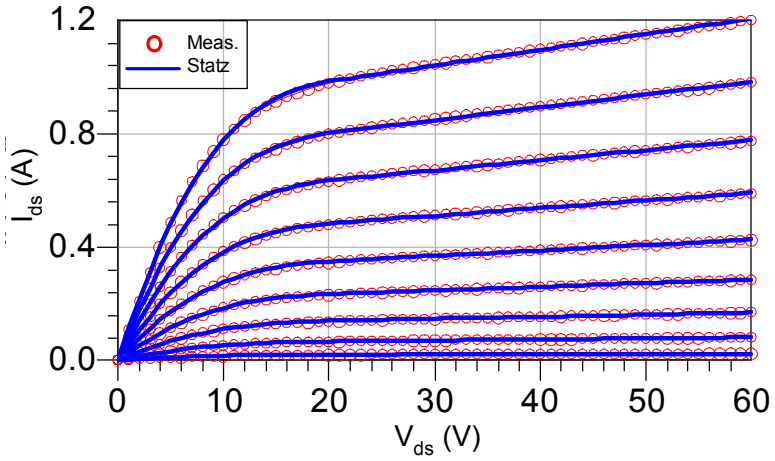


Figure 4.4. Measured (symbols) and calculated (solid lines) DC characteristics of the CRF24010 based on Statz model, $V_{gs}$ = –13 V to –5 V, step 1 V.

| Model Parameter | Θ (1/V) | α (1/V) | λ (1/V) | $V_{th}$ (V) | β ($A/V^2$) |
|---|---|---|---|---|---|
| Value | 0.034 | 0.136 | $-6.53e^{-3}$ | -13.3 | 0.0136 |

Table 4.3. Extracted DC parameters of Statz model.

$$V_{st} = V_{st0}\left(1 + M_{st0}V_{ds}\right) \tag{4.10}$$

where β, Θ, λ, α, and k are fitting parameters and $V_{th}$ is the threshold voltage. $V_{st0}$ and $M_{st0}$ are the sub-threshold parameters. DC simulations based TOM3 model and measurements are shown in figure 4.5. A slight increase in the accuracy of this model can be observed compared to the Statz model. Table 4.4 indicates the extracted values of the model parameters.

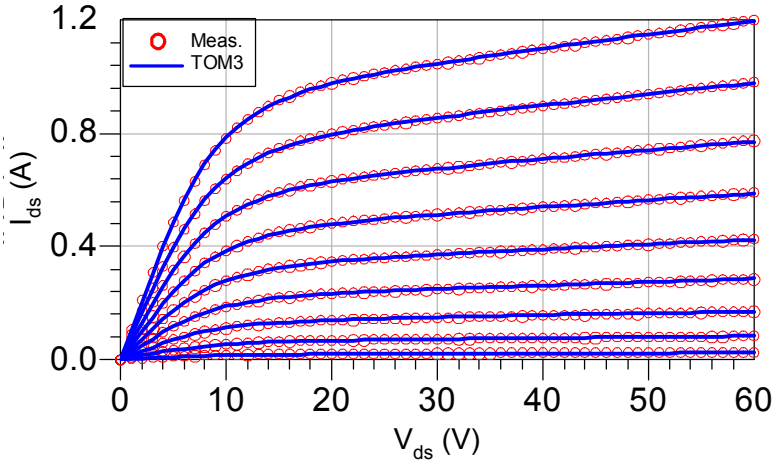


Figure 4.5. Measured (symbols) and calculated (solid lines) DC characteristics of the CRF24010 based on TOM3 model, $V_{gs}$ = –13 V to –5 V, step 1 V.

| Model Parameter | α (1/V) | β (A/V$^2$) | γ | λ (1/V) | Q | $V_{st0}$ (V) | $M_{st0}$ (1/V) | $V_{th}$ (V) | k |
|---|---|---|---|---|---|---|---|---|---|
| Value | 0.11 | 0.0196 | 6.25e$^{-5}$ | 4.9e$^{-3}$ | 1.76 | 0.083 | 5.5e$^{-5}$ | -13.2 | 2.72 |

Table 4.4. Extracted DC parameters of TOM3 model.

### 4.2.1.5 Modified Chalmers (Angelov) Model

The Chalmers model uses tanh and polynomial approximations instead of the square law [52]. The model is characterized by the gate voltage $V_{pk}$ of the peak transconductance instead of the threshold voltage parameter $V_{th}$. $I_{pk}$ is the drain current for the maximum transconductance.

$$I_{ds} = I_{pk}\left(1+\tanh(\psi)\right)\left(1+\lambda V_{ds}\right)\tanh(\alpha V_{ds}) \tag{4.11}$$

where

$$\psi = P_1(V_{gs}-V_{pk}) + P_2(V_{gs}-V_{pk})^2 + P_3(V_{gs}-V_{pk})^3 + \ldots \tag{4.12}$$

and

$$P_1 = P_{sat}\left(1+\frac{B_1}{\cosh^2\left(B_2 V_{ds}\right)}\right) \tag{4.13}$$

Parameters $P_{sat}$, $B_1$, $B_2$, $P_2$ and $P_3$ are fitting parameters. The saturation parameter α is slightly modified in this approach to meet the measured data [74]:

$$\alpha = \alpha_r + \alpha_1\left(\alpha_2 + \tanh(\psi)\right) \tag{4.14}$$

where $\alpha_r$, $\alpha_1$ and $\alpha_2$ are saturation parameters. In addition, $V_{pk}$ has different values in the linear and saturation ranges:

$$V_{pk} = V_{pk0} + (V_{pks} - V_{pk0})\tanh(\alpha V_{ds}) \tag{4.15}$$

where $V_{pk0}$ and $V_{pks}$ are the gate voltages for peak transconductance in the linear and saturation ranges, respectively. Although a large number of model parameters are used in the computation process, this modified model can be considered as more accurate compared to other used models. Figure 4.6 shows an excellent agreement between the measured and simulated DC characteristics and the corresponding extracted model parameters are given in table 4.5.

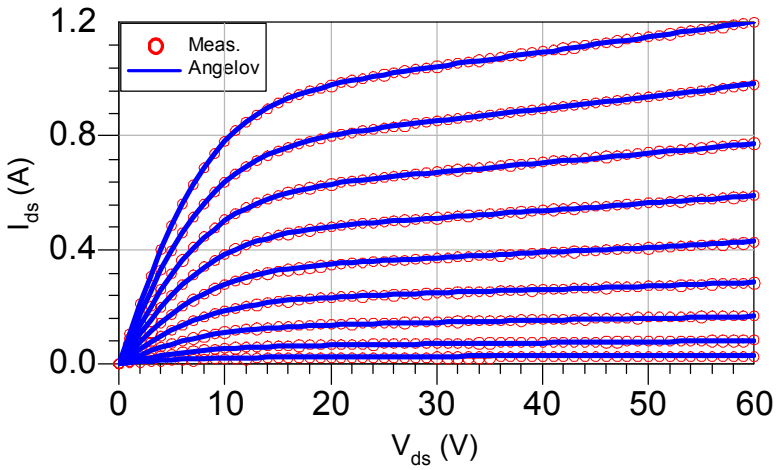


Figure 4.6. Measured (symbols) and calculated (solid lines) DC characteristics of the CRF24010 based on Angelov model, $V_{gs}$ = –13 V to –5 V, step 1 V.

| Model Parameter | $I_{pk}$ (A) | $\alpha_r$ | $\alpha_1$ | $\alpha_{\square}$ | $\alpha_s$ | $B_1$ | $B_2$ |
|---|---|---|---|---|---|---|---|
| Value | 0.599 | 0.109 | 0.0014 | 4.11 | 0.23 | 0.246 | 0.167 |
| Model Parameter | $P_{sat}$ | $P_2$ | $P_3$ | $\lambda$ | $V_{pk0}$ (V) | $V_{pks}$ (V) | |
| Value | 0.251 | 0.0165 | 0.0046 | 0.0046 | -6.98 | -6.9 | |

Table 4.5. Extracted DC parameters of the modified Angelov model.

The values of the error function (Table 4.6) indicate that the modified Angelov model has the minimum error function compared to other used models. So, based on this model, performance of our derived model can be accurately predicted.

| Model | Curtice-Ettenberg | Materka-Kacprzak | Statz | TOM3 | Angelov |
|---|---|---|---|---|---|
| Error | $2e^{-3}$ | $8.2e^{-4}$ | $7.14e^{-4}$ | $2.9e^{-4}$ | $4e^{-5}$ |

Table 4.6. Comparison of the error function values of the most used models in ADS simulation.

## 4.2.2 Capacitive Modeling

Capacitance modeling is becoming more and more important as the operating frequencies increase. The conductive part dominates at low frequencies, but nonlinear capacitances contribute more and more not only to the frequency response, but also to the harmonic distortion and intermodulation distortion if the frequencies increase. It is

no longer adequate that the model predicts the capacitance only at some bias point. Nonlinearities are important as well. There are two main approaches to gate charge modeling, the capacitance and charge approaches. Based on the capacitive approach, we will continue in this step of device modeling to describe capacitance voltage characteristics of the device. The model of Angelov *et al* [52] addresses the problem of dual voltage dependence of the device capacitances.

The nonlinear capacitances are gate-source capacitance $C_{gs}$, gate-drain capacitance $C_{gd}$, and drain-source capacitance $C_{ds}$. Each capacitance is extracted from the measured S-parameters at various bias points and modeled using continuous single empirical functions. The functions of nonlinear capacitances used in this modeling are as follows [59, 60]:

$$C_{gs} = C_{gsp} + C_{gs0}(1+\tanh\psi_1)(1+\tanh\psi_2) + C_{gs0}\left[V_{gs} + \frac{\ln\cosh(\psi_1)}{P_{11}}\right](1-\tanh^2\psi_2)P_{21} + C_{gd0}\left[V_{gd} + \frac{P_{400}\ln\cosh\psi_4}{P_{41}}\right](1-\tanh^2\psi_3)P_{31} \tag{4.16}$$

$$C_{gd} = C_{gdp} + C_{gd0}(1+P_{400}\tanh\psi_4)(1+\tanh(\psi_3)) - C_{gd0}\left[V_{gs} + \frac{\ln\cosh\psi_1}{P_{11}}\right](1-\tanh^2\psi_2)P_{21} \tag{4.17}$$

$$C_{ds} = C_{dsp} + C_{ds0}.(1+\tanh\psi_5)).\tanh(\psi_6) \tag{4.18}$$

$$\psi_1 = P_{10} + P_{11}V_{gs} \tag{4.19-a}$$

$$\psi_2 = P_{20} + P_{21}V_{ds} \tag{4.19-b}$$

$$\psi_3 = P_{30} + P_{31}V_{gs} \tag{4.19-c}$$

$$\psi_4 = P_{40} + P_{41}V_{gd} \tag{4.19-d}$$

$$\psi_5 = P_{50} + P_{51}V_{ds} \tag{4.19-e}$$

$$\psi_6 = P_{60} + P_{61}V_{gs} \tag{4.19-f}$$

More than one hundred bias-dependent measured S-parameter sets were used to determine the capacitance-voltage behavior of the device. It has been found, that the extracted $C_{gs}$, $C_{gd}$ and $C_{ds}$ data fit pretty well with the nonlinear equations given in (4.17) through (4.19). In this representation, we do not integrate the capacitance towards charges, but use directly the bias-dependent capacitances. Energy conservation condition in this case is given by

$$\begin{bmatrix} C_{gs}+C_{gd} & -C_{gd} \\ -C_{gd} & C_{ds}+C_{gd} \end{bmatrix} = \begin{bmatrix} \dfrac{\partial^2 E}{\partial V_{gs}^2} & \dfrac{\partial^2 E}{\partial V_{ds}\partial V_{gs}} \\ \dfrac{\partial^2 E}{\partial V_{gs}\partial V_{ds}} & \dfrac{\partial^2 E}{\partial V_{ds}^2} \end{bmatrix} \tag{4.20}$$

where **E** is the total energy stored in the nonlinear capacitances. Using the capacitance equations, it is possible to recover the conserved energy by two path-independent line integrations of measured $C_{ij}$ matrix elements as follows:

$$\begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{\partial Q_g}{\partial V_{gs}} & \dfrac{\partial Q_g}{\partial V_{ds}} \\ \dfrac{\partial Q_d}{\partial V_{gs}} & \dfrac{\partial Q_d}{\partial V_{ds}} \end{bmatrix} \tag{4.21}$$

Figure 4.7 and figure 4.8 show the simulated dependencies of $C_{gs}$ on the drain-source and gate-source voltages. The results correlate well with the measured dependencies. $C_{gs}$ is an increasing function of the drain-source and gate-source voltages. $C_{gd}$ dependencies are more complicated, as shown in figures 4.9 and 4.10. In the saturated drain voltage region, $C_{gd}$ slightly increases when the gate voltage is increased. At low drain voltages, $C_{gd}$ increases with increasing gate voltage and decreases with the drain voltage increasing. From these figures, it is obvious that simulations correlate with measurements.

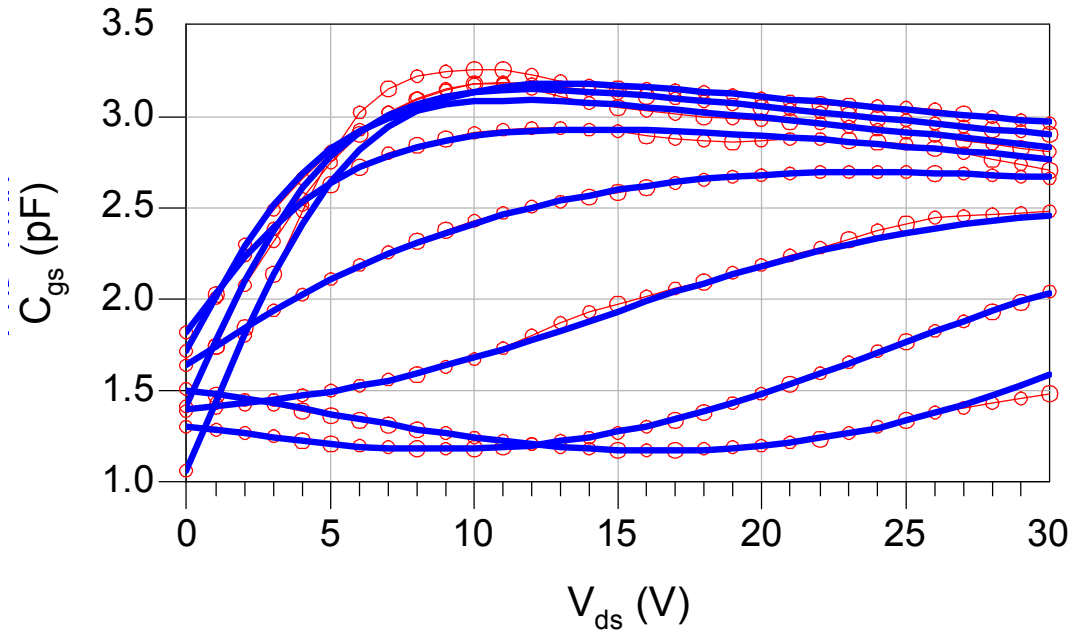


Figure 4.7. Measured (symbols) and modeled (solid lines) gate-source capacitance $C_{gs}$ versus $V_{ds}$; $V_{gs}$ varies from – 13 V (bottom) to - 6 V (top), step 1 V.

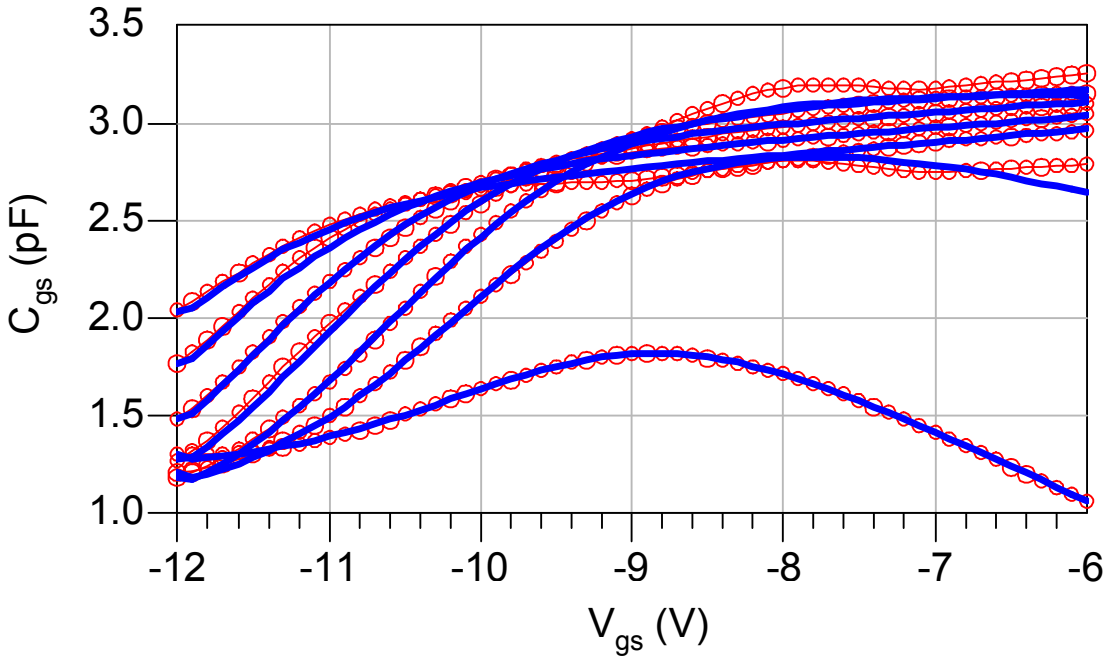


Figure 4.8. Measured (symbols) and modeled (solid lines) gate-source capacitance $C_{gs}$ versus $V_{gs}$; $V_{ds}$ varies from 0 V (bottom) to 30 V (top), step 5 V.

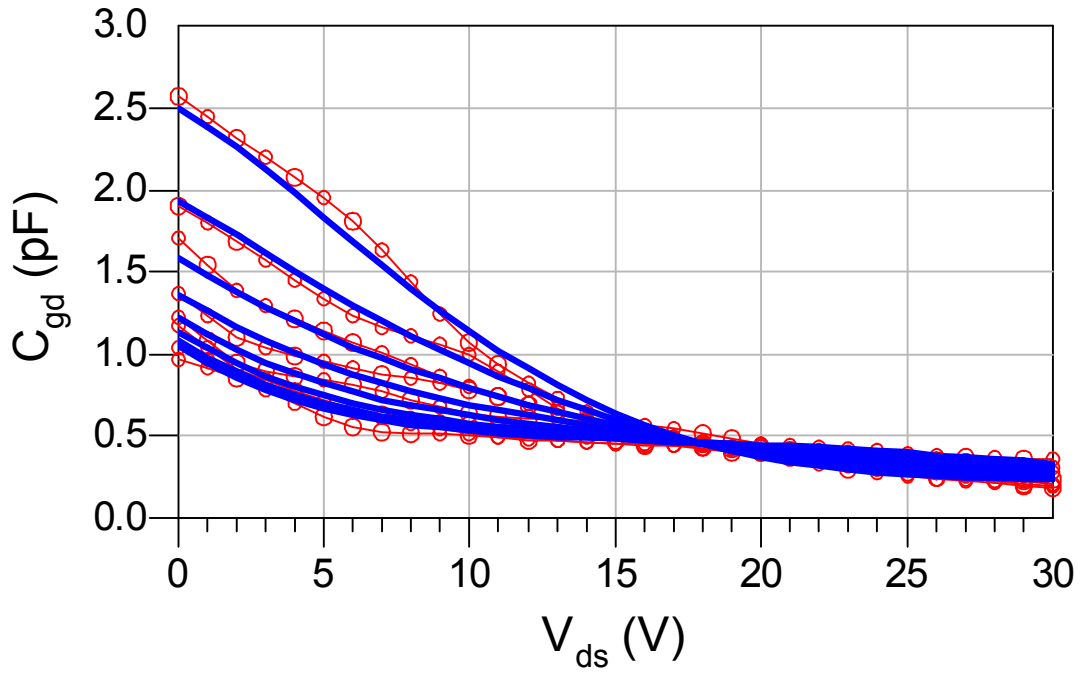


Figure 4.9. Measured (symbols) and modeled (solid lines) gate-drain capacitance $C_{gd}$ versus $V_{ds}$; $V_{gs}$ varies from – 13 V (bottom) to - 6 V (top), step 1 V.

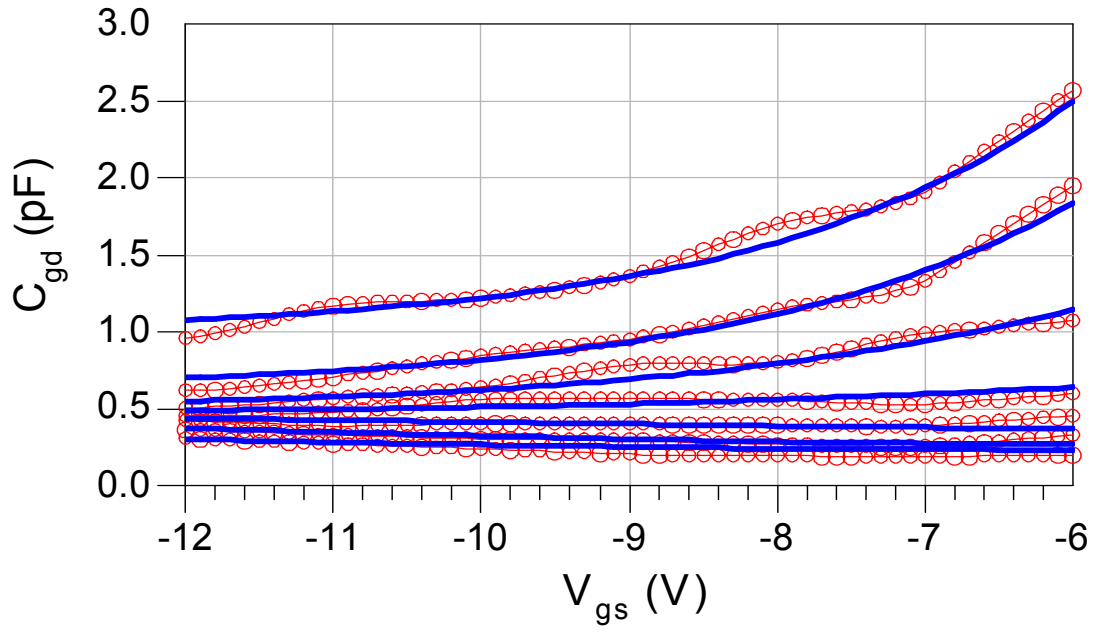


Figure 4.10. Measured (symbols) and modeled (solid lines) gate-drain capacitance $C_{gd}$ versus $V_{gs}$; $V_{ds}$ varies from 0 V (bottom) to 30 V (top), step 5 V.

Dependency of $C_{ds}$ on gate-source voltage and drain-source voltage are illustrated in figures 4.11 and 4.12. $C_{ds}$ increases with increasing gate voltage and decreasing drain voltage. From these figures, we can see that fairly good agreement with measured data is obtained.

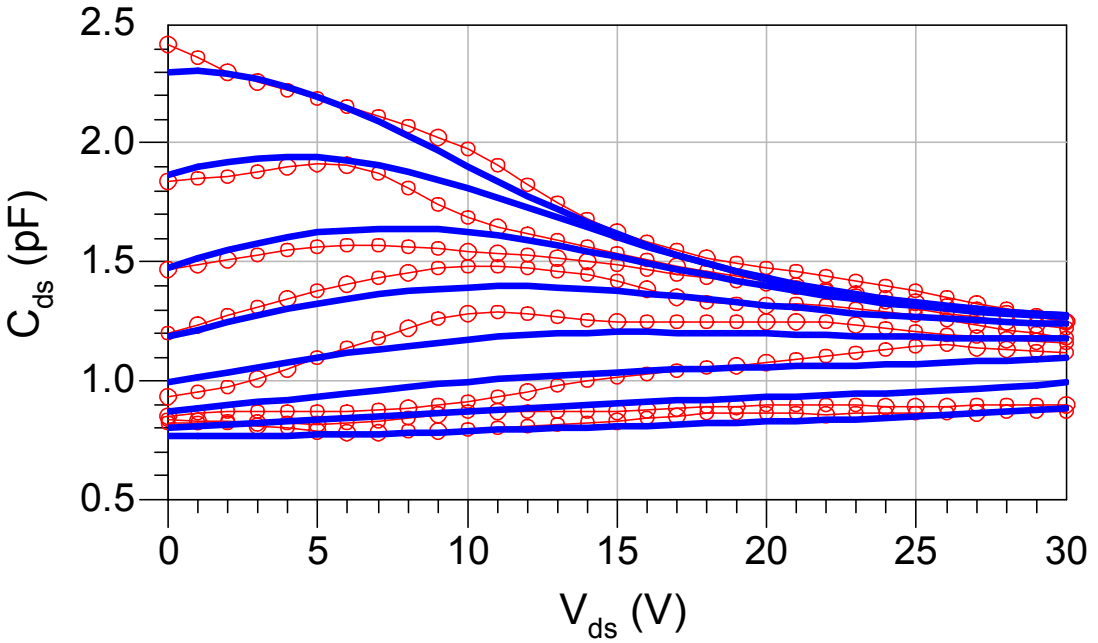


Figure 4.11. Measured (symbols) and modeled (solid lines) drain-source capacitance $C_{ds}$ versus $V_{ds}$; $V_{gs}$ varies from – 13 V (bottom) to - 6 V (top), step 1 V.

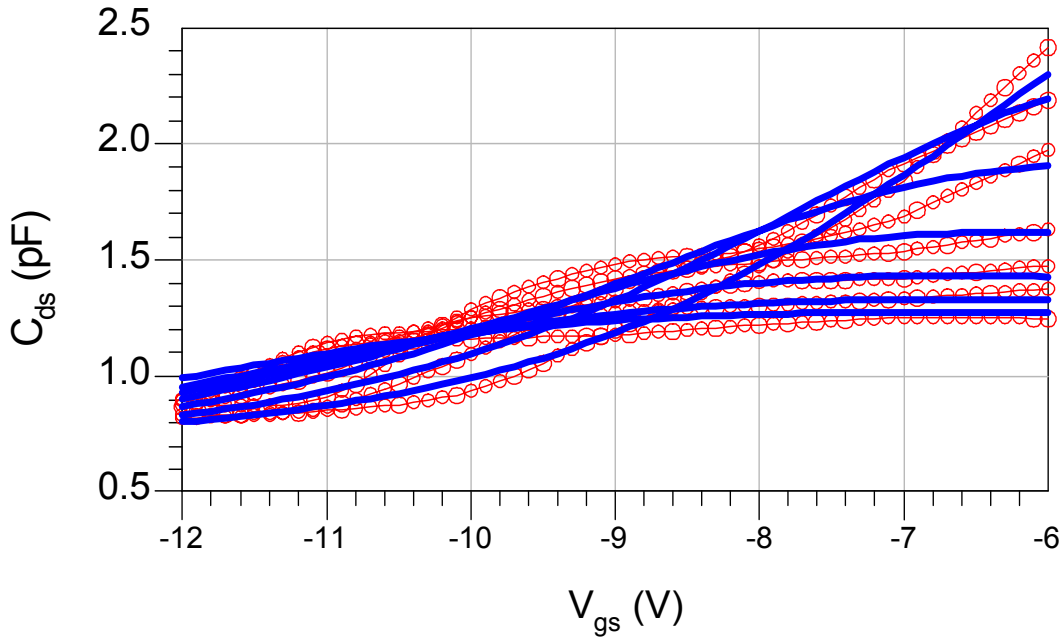


Figure 4.12. Measured (symbols) and modeled (solid lines) drain-source capacitance $C_{ds}$ versus $V_{gs}$; $V_{ds}$ varies from 0 V (bottom) to 30 V (top), step 5 V.

### 4.2.3 Frequency Dispersion

The RF current characteristics are different from DC curves. The difference comes from low-frequency dispersion effects such as deep level trapping. A model that does not account for the difference of the output conductance at DC and RF cannot accurately predict both values simultaneously [57]. This concept is important for amplifier design because the DC output conductance is used to set the quiescent bias point, while the RF output conductance, in part, determines the RF matching circuit and is used to predict RF output level. The best model would predict both to a reasonable level of accuracy. A possibility to describe the difference between low frequency and RF behavior is to use different DC and RF current sources. E.g., the RF current source can be obtained by integration of the small signal transconductance $g_m$ and output conductance $g_{ds}$, respectively:

$$I_{dsRF} = \int g_m dV_{gs} + g_{ds} dV_{ds} \tag{4.22}$$

A way to eliminate the differences between high- and low-frequency output conductances is to add a capacitive coupled resistive branch ($R_C$, $C_{RF}$) to the output as shown in figure 4.1. The physical basis of the model is explained in [57]. The resistance $R_C$ is selected to be a bias-dependent hyperbolic function in order to eliminate dispersion effects in the complete large signal range. This is important with

respect to the ability of the model to predict the overall nonlinear behavior with high accuracy and reliability.

$$R_C = R_{C\min} + \eta_1 / (1 + 1/R_{C\max} + \eta_2 \tanh(\psi)) \tag{4.23}$$

$R_{Cmin}$ and $R_{Cmax}$ represent the minimum and maximum dispersion resistances, respectively, and $\eta_1$ and $\eta_2$ are functions of $V_{gs}$, $V_{ds}$. The parameters of (4.23) are being found by optimization of $S_{22}$ at several bias points. Verification of frequency dispersion modeling is finally demonstrated in figure 4.13.

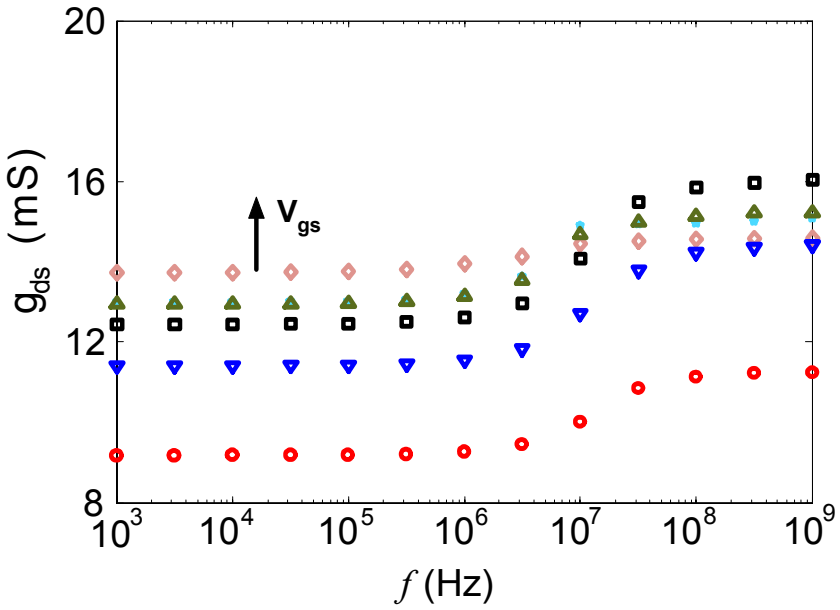


Figure 4.13. Dispersion of the output conductance at $V_{ds}$ = 30 V.
$V_{gs}$ = -11 V to – 6 V, step 1 V.

## 4.3 Model Verification

The proposed model has been implemented as a user-defined model into the harmonic balance circuit simulator ADS from Agilent and small and large signal simulations were accomplished. A part of the model verification is to use the ADS installed Cree's model for comparison to the derived model. The derived model will also be verified explicitly in chapter 6. A single-stage wideband power amplifier using the Cree SiC MESFET CRF24010 has been designed and its performance based on the derived model has been verified.

### 4.3.1 Power Performance

Simulated output power, gain compression and power added efficiency versus input power have been compared on the base of both models. Figure 4.14 shows the

results at $f$ = 1 GHz, $V_{DS}$ = 30 V and $I_D$ = 500 mA. (Cree model (symbols), this work (solid lines)). A very good agreement concerning power gain and output power can be observed whereas the PAE curves show a slight difference.

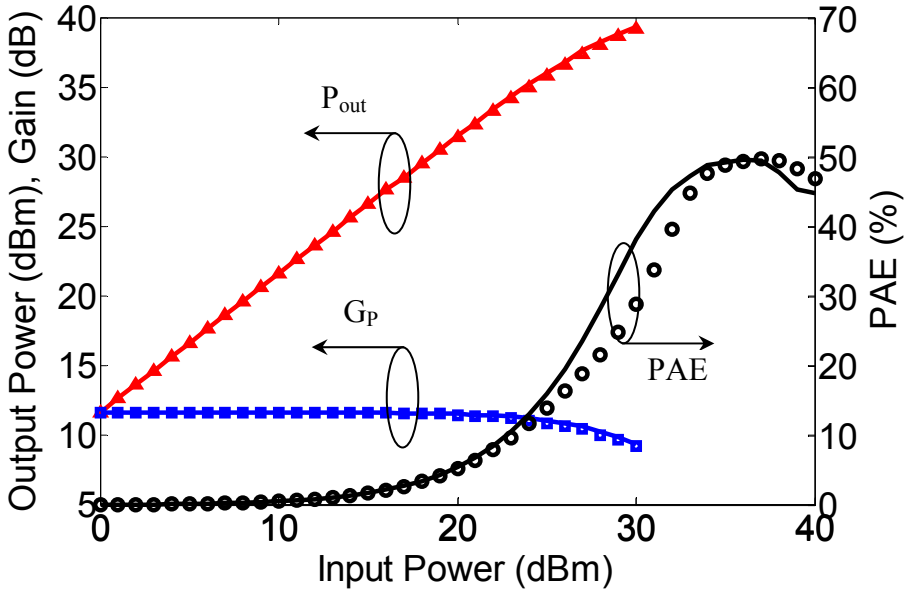


Figure 4.14. Power performance verification of the derived model (solid lines) compared with the Cree model (symbols). $f$ = 1 GHz, $V_{DS}$ = 30 V and $I_D$ = 500 mA.

Power performance of the derived model is also tested at various bias points. At $I_D$ =500 mA, $f$ = 1 GHz, the predicted output power ($P_{out}$) and power gain ($G_P$) are obtained at different drain voltages.

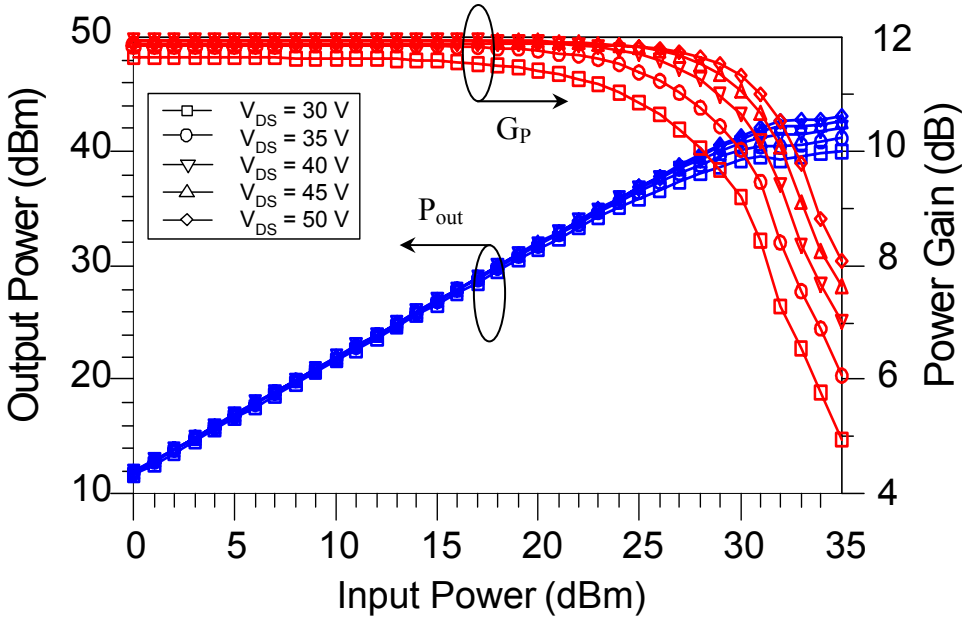


Figure 4.15. Power performance verification of the derived model at different drain source voltages, $f$ = 1 GHz.

Figure 4.15 shows multi-bias diagrams of the modeled $P_{out}$ and $G_P$ from $V_{DS}$ =30 V…50 V, step 5 V. At 1 dB compression point, the predicted output power increases from 37 dBm at $V_{DS}$ = 30 V to 41 dBm at $V_{DS}$ = 50 V. 1 dB gain compression point also varies from 10.5 dB to 11 dB as $V_{DS}$ increases from 30 V to 50 V.

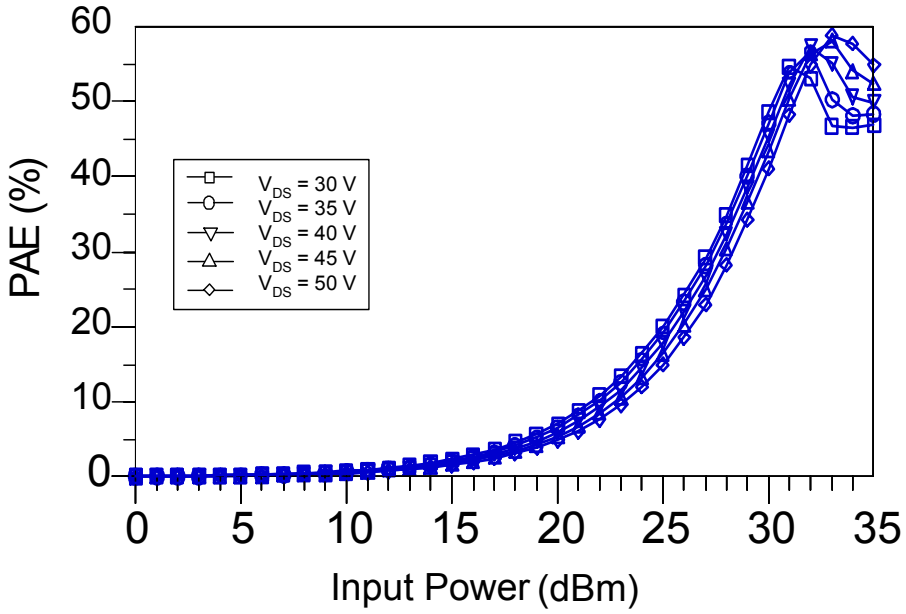


Figure 4.16. Power added efficiency of the derived model at different drain source voltages, $f$ = 1 GHz.

Figure 4.16 shows the corresponding power added efficiency (PAE) at the same operating point ($f$ =1 GHz, $I_D$ = 500 mA). The maximum PAE of the derived model also increases from 53 % at $V_{DS}$ = 30 V to 58 % at $V_{DS}$ = 50 V.

### 4.3.2 Linearity Performance

Two-tone measurements with spacing of 200 kHz are carried out at $f$ = 1 GHz and second- and third-order intermodulation products of both models are compared in figure 4.17. Again, the comparison shows good agreement. Output second-order intercept point OIP2 and third-order intercept point OIP3 of 72 dBm and 51 dBm, respectively, can be extracted [58].

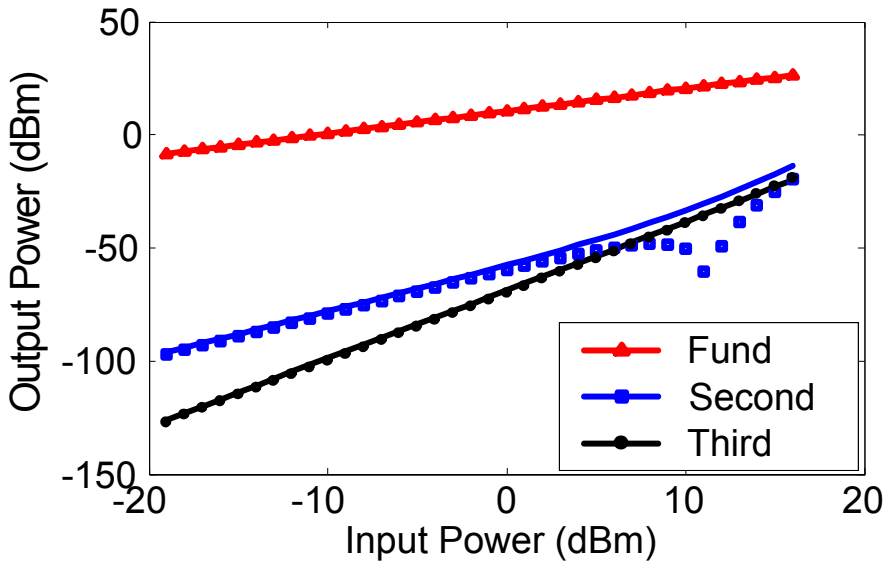


Figure 4.17. Two-tone test: Comparison of the derived model (solid lines) and Cree's model performance (symbols) @ $f$ = 1 GHz, $V_{DS}$ = 30 V and $I_D$ = 500 mA.

Linearity performance of the derived model is verified with swept frequency from 1 MHz to 2.5 GHz. Output second- and third-order intercept points (OIP2 and OIP3) for both the Cree model (symbols) and our model (solid lines) at $V_{DS}$ = 30 V and $I_D$ = 500 mA are shown in figure 4.18. An OIP3 of about 50 dBm can be obtained. Excellent agreement between both models can be achieved for OIP3, however, a slight difference of 5 dBm in OIP2 between the derived model and the Cree model can be observed.

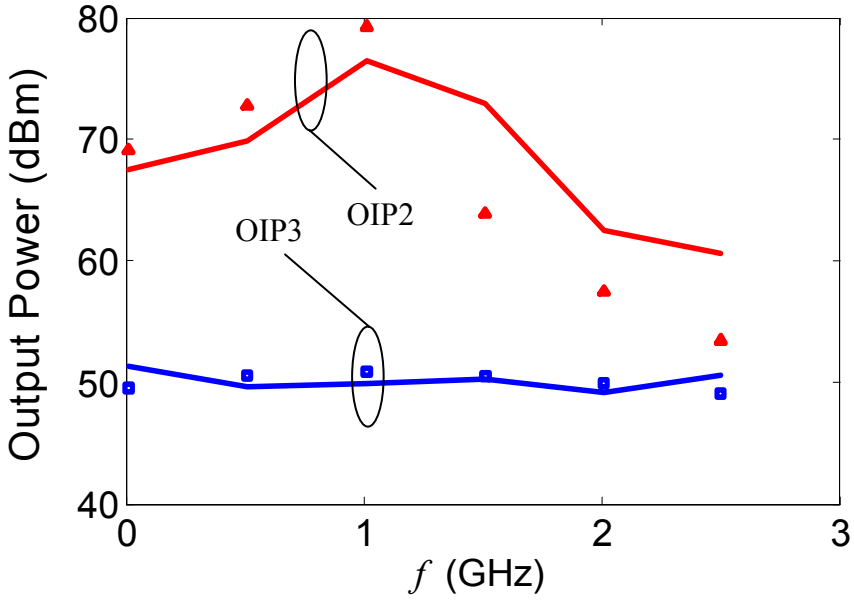


Figure 4.18. Sweep of output intercept points with frequency at $V_{DS}$ = 30 V and $I_D$ = 500 mA: solid lines ⟶ derived model, symbols ⟶ Cree model.

Single-tone linearity performance of the derived model has been studied on the base of AM-AM and AM-PM response. AM-AM distortion is created by variation of the amplifier gain as a function of input power while AM-PM distortion is defined as change of the phase between input and output signals with varying input power. Mathematically, AM-AM and AM-PM distortions are defined by

$$AM - AM = \frac{\partial G_P}{\partial P_{in}} \tag{4.24}$$

$$AM - PM = \frac{\partial \phi(G_P)}{\partial P_{in}} \tag{4.25}$$

where $\phi(G_P)$ is the transmission phase in degrees. Figure 4.19 shows the measured and simulated AM-AM and AM-PM conversions of the power stage at 1 GHz. The AM-AM response has a compression characteristic, which is rather soft up to the 1 dB compression point. However, the AM-PM response shows a maximum distortion of 0.5 deg/dB in the linear region and 4 deg/dB in saturation (above 1 dB compression point). The figure also shows an excellent agreement between both models. In chapter 6, as an application of the derived model in large-signal mode, measurements of a single-stage wideband power amplifier based on SiC MESFET will be compared to the modeled performance as a further step in model validation.

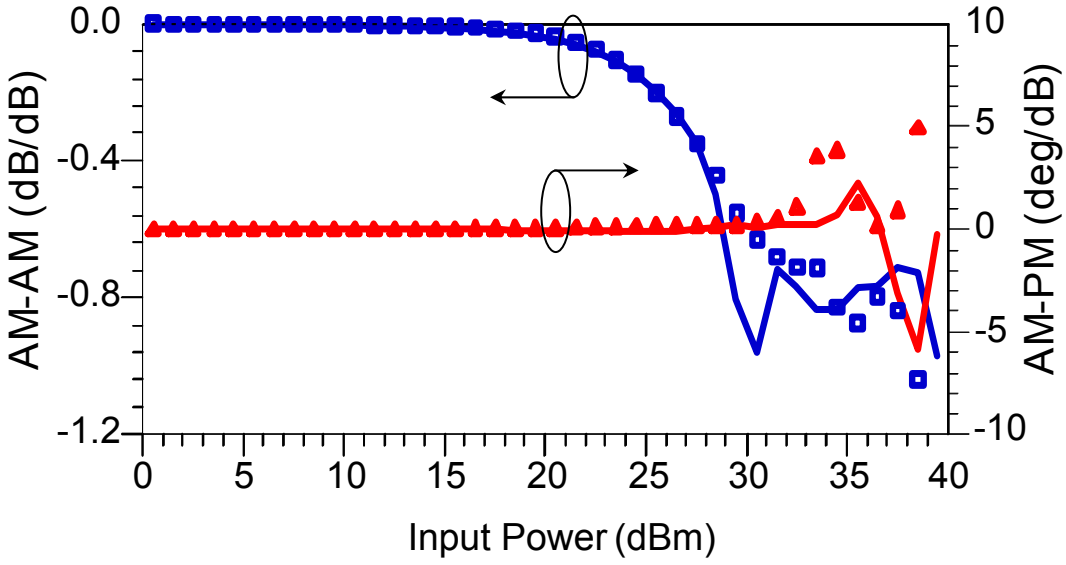


Figure 4.19. AM-AM and AM-PM conversions: Comparison of the derived model (solid lines) and Cree's model performance (symbols) @ $f$ = 1 GHz, $V_{DS}$ = 30 V and $I_D$ = 500 mA.

# CHAPTER FIVE

# WIDEBAND POWER AMPLIFIER DESIGN

For a given device technology, broadband amplifier design is constrained by the gain-bandwidth product, impedance matching limitation and other requirements, and various broadband techniques are attempted and utilized in order to achieve the desired broadband performance [72], [73]. In this chapter, a design procedure for broadband power amplifiers is presented in detail. Power gain, stability and various broadband matching techniques are discussed. A low loss DC biasing network also has been developed to meet the desired broad bandwidth. Design examples of different broad-band power amplifiers are introduced. First, a 5 watt single stage power amplifier based SiC MESFET has been designed [71]. Then, a two stage high gain power amplifier has been developed [58]. Further work based on SiC dies in two cases has been done. For the first time, in a step towards design, an ultra wideband power amplifier (from 1 MHz up to 5 GHz) based on SiC technology has been simulated. Results will be presented and discussed in details in the next chapter.

## 5.1 Power Amplifier structure

Figure 5.1 depicts a typical block diagram of an amplifier circuit. The central block represents an amplifier (transistor) which is characterized by its S-parameters. The amplifier's S-parameters are included in data sheets provided by the manufacturer of the device. The left and right blocks represent the input matching network (IMN) and the output matching network (OMN) of the amplifier. These are necessary to provide good impedance matching between the amplifier circuitry. The transistor is biased through the gate biasing network (GBN) and the drain biasing network (DBN). The design procedure of the power amplifier consists of stability

analysis, gain calculations, matching circuit determination and direct current (DC) biasing. Elaboration of these steps will be done in the following sections.

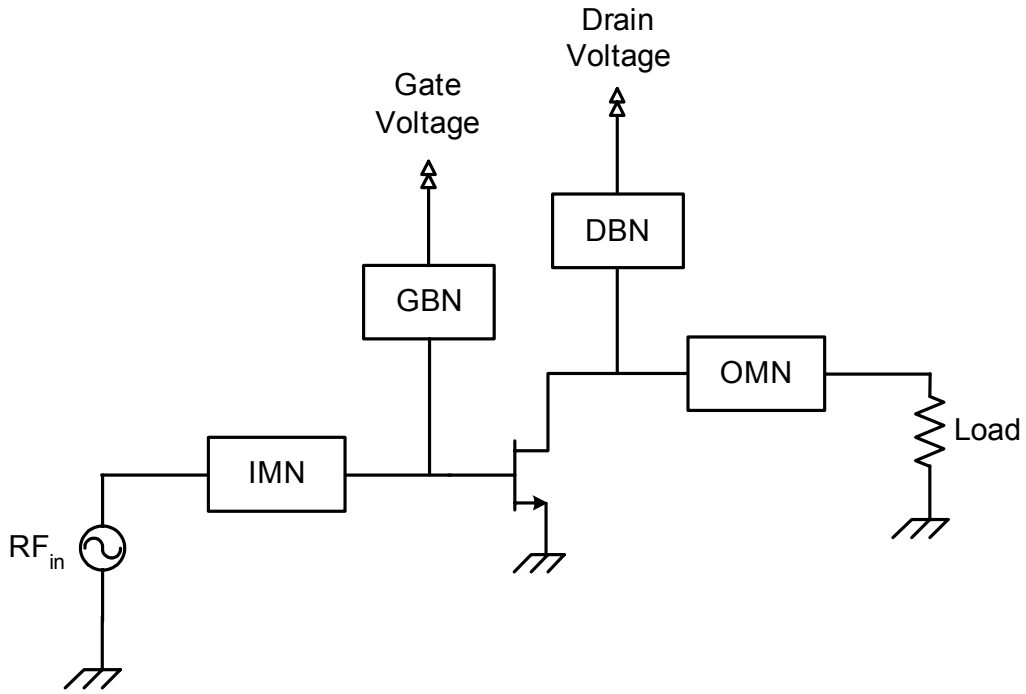


Figure 5.1. Basic structure of single stage amplifier.

## 5.2 Broadband matching

### 5.2.1 Bandwidth limitation

The broadband power amplifier design can be simplified to the broadband conjugate match at the input and broadband load-pull match at the output of the device. Normally a matching network will produce the desired match at one frequency and matching degradation will occur at the other frequencies. Fano [61] has derived a complete set of integrals that predict the gain-bandwidth restrictions for the lossless matching networks terminated in arbitrary load impedance. For the network shown in figure 5.2 (a), the best reflection coefficient Γ that can be achieved over a frequency range is restricted by the integral

$$\int_0^\infty \ln\left|\frac{1}{\Gamma}\right| d\omega \le \frac{\pi}{RC} \tag{5.1}$$

This equation shows that the product of the bandwidth Δω and ln |1/Γ| cannot be greater than π/RC. Therefore, if matching is required over a certain bandwidth, it can be obtained at the expense of the reduced matching (less power transfer) or higher |Γ|.

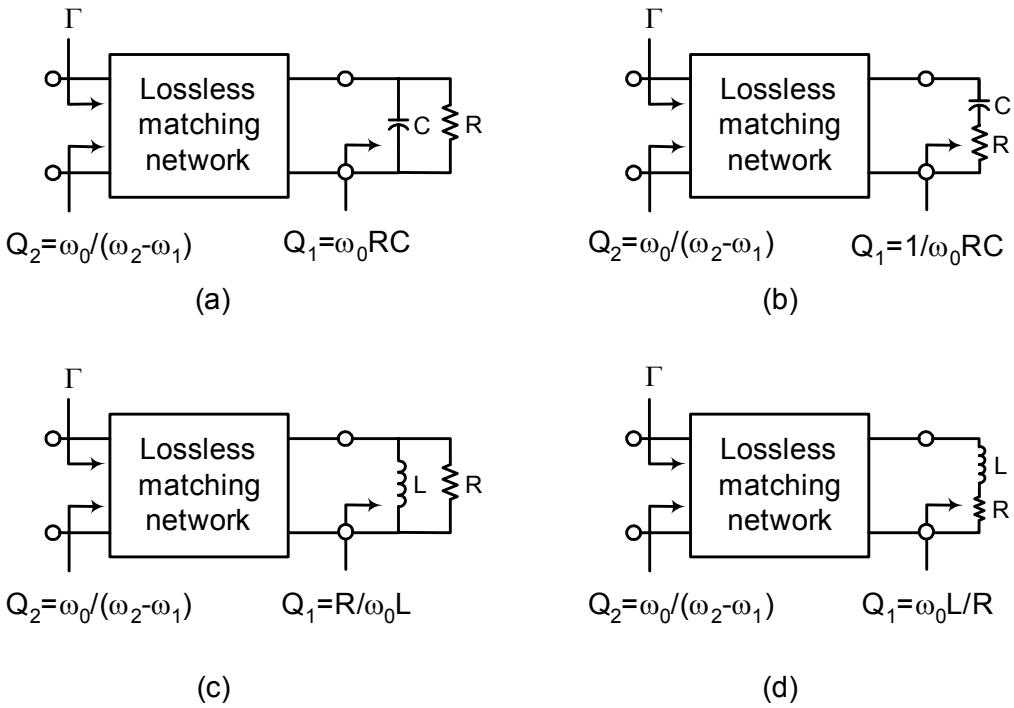


Figure 5.2. Network topologies used in the calculation of the gain-bandwidth limitations.

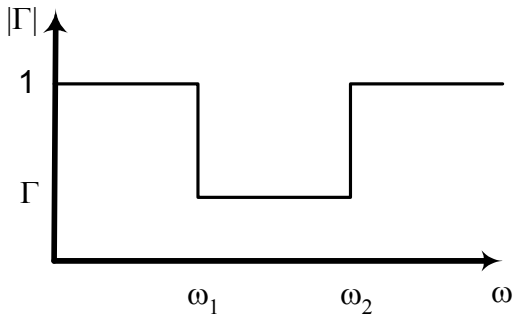


Figure 5.3. Optimum values of |Γ|.

The ideal matching situation is obtained when |Γ| is constant in the desired bandwidth (from $\omega_1$ to $\omega_2$) and equals to 1 outside that range, as illustrated in figure 5.3. It can be derived from equation (5.1) that

$$\left|\Gamma\right| = e^{-\pi/(\omega_2-\omega_1)RC} = e^{-\pi Q_2/Q_1} \tag{5.2}$$

where $Q_1 = R/X$ for parallel network or X/R for series network as shown in figure. 5.2 and $Q_2 = \omega_0/(\omega_2-\omega_1)$ (reciprocal of fractional bandwidth). Ideally this is the best |Γ| (lowest) that can be obtained in the band. For a given bandwidth ($Q_2$), a lower $Q_1$ can produce lower |Γ|. Therefore, a load impedance with lower $Q_1$ can achieve better broadband matching. For the matching of the transistor, figure 5.2 (a)

represents the simplified output circuit model of the device and figure 5.2 (b) represents the simplified input circuit model of the device. As a result, a smaller RC product for the output and a larger RC product for the input of the device are preferred to achieve broadband matching. However, normally lower Qs at the input and output of the device result in lower maximum available gain. Therefore there is always a tradeoff between the broadband matching and available gain for the device.

### 5.2.2 Bandwidth extending methods

Most broadband design techniques include two categories: interstage networks (including the input and output network), and feedback networks (or the combination of both methods). From a network viewpoint, broadband design involves 1) removing or canceling the poles nearest the jω axis, 2) changing the positions of the remaining poles to realize the desired transfer characteristic (filter characteristics such as Butterworth or Chebyshev, etc). Both 1 and 2 can be achieved by the employment of interstage networks or using feedback. Interstage networks can be either lossless (consist only of L, C elements) or lossy (include R elements with the L and C elements). Some commonly used techniques for bandwidth extending are described briefly below [62].

#### 5.2.2.1 Feedback

Feedback technique has the advantages of increasing bandwidth, stabilizing gain, establishing and controlling input/output impedances, reducing parametric sensitivities and reducing distortion. There are four basic feedback configurations: shunt-shunt, shunt-series, series-shunt and series-series. An example of the shunt-shunt case (shown in figure 5.4 (a)) is a common-source FET with a shunt feedback resistor R connected from the drain node back to the gate node. The gain, input and output impedances are reduced in the shunt-shunt configuration. An example of a series-series configuration (Figure 5.4 (b)) would be a resistor in series with the source terminal of a common-source FET. In that case, the gain would be reduced, but the input and output impedances are increased as a result of the feedback. Sometimes more than one feedback topology can be used to take full advantage of the benefits of the feedback. Darlington technique based on two transistors shunted with a feedback resistor has been presented and modified by Armijo *et al* [72]. This technique suffers

from PAE reduction because the transistors do not saturate at the same time. Krishnamurthy *et al* [73] has improved this approach by adding a resistor between the transistors. The new technique called $f_\tau$ doubler can overcome the previous problem and increase the bandwidth, however, resulting in output power reduction and increased circuit complexity.

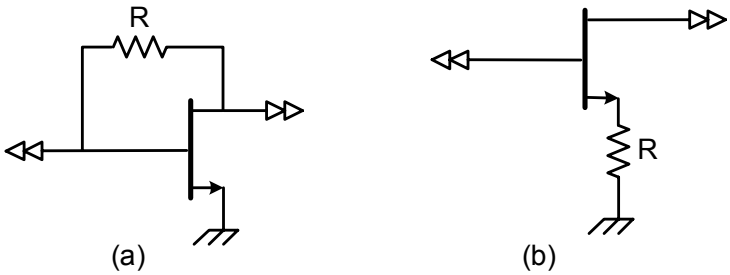


Figure 5.4. Feedback configurations: (a) Shunt-shunt, (b) Series-series.

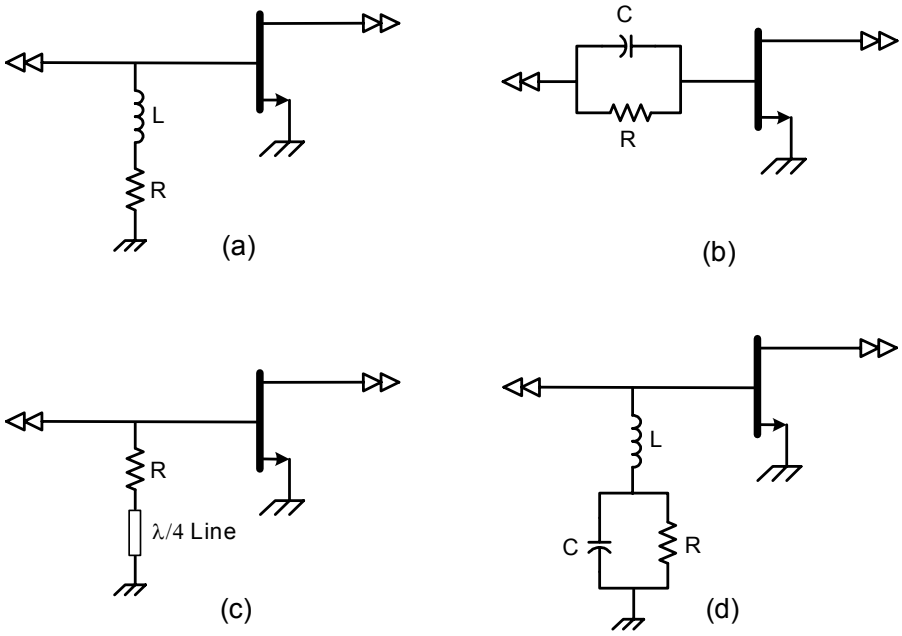


Figure 5.5. lossy match networks at the input of the device (a) R-L shunt network, (b) R-C series network, (c) R-λ/4 line network, (d) R-L-C shunt network.

### 5.2.2.2 Lossy Match

The lossy match is superior to pure resistive broad-banding. Resistors are used in the matching networks to provide lossy gain compensation. One of the lossy match networks (R-L branch) at the input of the active device is shown in figure 5.5 (a). At frequencies well below the upper edge of the band, the R-L behaves as a pure shunt resistance R. However, for frequencies approaching the upper band edge, the effective

branch impedance increases because of the inductors' series impedance. There are also the series-connected parallel R-C network (Figure 5.5 (b)), the shunt R-λ/4 line network (Figure 5.5 (c)) and the shunt R-L-C network (Figure 5.5 (d)) that can achieve similar broadband matching at the input of the device. Lossy matching is normally avoided at the output for achieving best efficiency and output power.

### 5.2.2.3 Broadband LC lowpass matching networks

1. Single-section lowpass LC network:

The single-section lossless lowpass LC matching network is one of the simplest matching networks [63]. The main reason of choosing a lowpass LC network over other LC networks is that we need to have a DC supply path. This network can realize perfect impedance transformation at one single frequency and have good match over a certain frequency range. Figure 5.6 (a) shows the network when the load resistor $R_L$ is larger than the source resistor $R_S$ and figure 5.6 (b) shows the network when the load resistor $R_L$ is smaller than the source resistor $R_S$. Here we only illustrate the situation of real source and load impedance transformation, since we can always absorb the reactive parts into the LC network. We can calculate the values of L and C by transforming the parallel network into series network as shown in figure 5.7 (a). We use $-X_P$ to denote the reactance of the capacitance, and $-X_P^*$ and $R_L^*$ as the transformed reactance and resistance, where

$$X_P^* = \frac{X_P R_L^2}{X_P^2 + R_L^2} \tag{5.3}$$

$$R_P^* = \frac{X_P^2 R_L}{X_P^2 + R_L^2} \tag{5.4}$$

For perfect match, it should be designed to achieve: $X_S = X_P^*$, $R_S = R_L^*$ in figure 5.7 (b), which is the equivalent circuit of the network shown in figure 5.6 (a). Therefore, we can obtain the desired L and C values by defining the Q value of the network.

For $R_L > R_S$,

$$Q = \sqrt{\frac{R_L}{R_S} - 1}, \quad X_S = \omega L - Q R_S, \quad X_P = 1/\omega C - R_L / Q. \tag{5.5}$$

For $R_L < R_S$,

$$Q = \sqrt{\frac{R_S}{R_L} - 1}, \quad X_P = 1/\omega C - R_S/Q, \quad X_S = \omega L - Q.R_L. \tag{5.6}$$

The bandwidth of the LC network is determined by the Q value of the circuit and is inversely proportional to Q. As we can see from those equations, given the source and load impedance $R_S$ and $R_L$, Q is fixed for the simple single-section lowpass LC network. The larger the ratio of impedance transformation $R_L / R_S$ (or $R_S / R_L$), the higher is the Q value of the network. As a result, we don't have much control over the bandwidth of those simple single-section LC networks for given $R_S$ and $R_L$. For broadband matching network design, we need to improve the bandwidth characteristic of those LC networks.

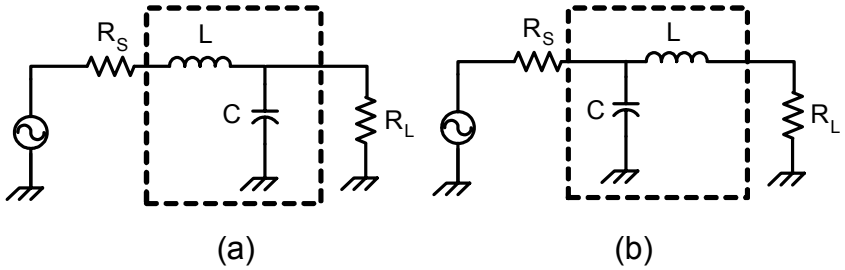


Figure 5.6. Lowpass LC matching networks for (a) $R_L > R_S$, (b) $R_L < R_S$

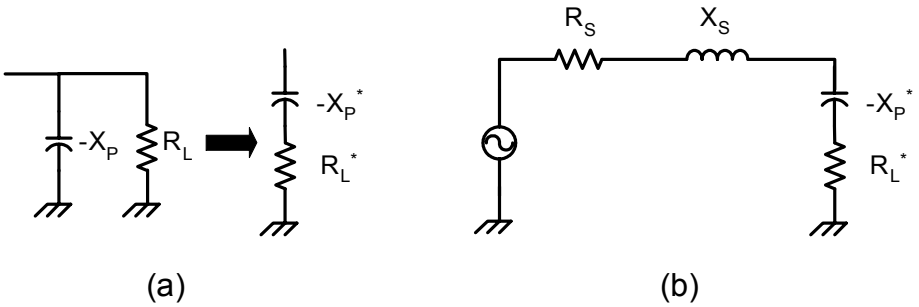


Figure 5.7. (a) Transform from parallel to series network ($X_P = 1/\omega C$), (b) The equivalent circuit of figure 5.6 ($X_S = \omega L$).

2. Multi-section low pass LC networks

Since the bandwidth of the LC network is inversely proportional to the Q value, we have to design low Q, LC networks to achieve the broadband matching. Naturally, we can employ multi-section LC networks, each has a lower impedance transformation ratio, as shown in figure 5.8 (assuming $R_L > R_S$). The intermediate impedances are decided by distributing the impedance transformation ratio equally among N sections, that is $R_1/R_S = R_2/R_1 = \ldots = R_L/R_N = (R_L/R_S)^{1/N}$. As a result, the Q

of the network will be reduced from the single-section value of $Q_1 = \sqrt{\frac{R_L}{R_S} - 1}$ to $Q_N = \sqrt{\left(\frac{R_L}{R_S}\right)^{1/N} - 1}$ .

With knowledge of the intermediate impedances, the L and C values of each section can be obtained using the same formula as in the design of single-section LC networks.

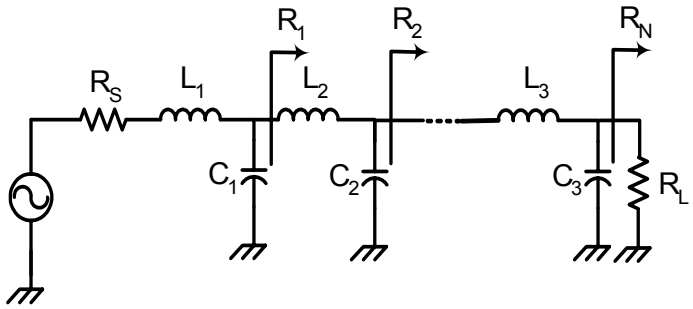


Figure 5.8. Multi-stage low Q LC matching networks ($R_L > R_S$).

Practically, the implemented matching networks based on lumped elements can only be valid up to 2 GHz or lower. Distributed matching networks based on microstrip technique can be used. Conversion from lumped elements to microstrip approach can simply be achieved based on the Hammerstad [64] and Mongia [65] formulas as follows:

1. Bulk wavelength λ:

For the calculation of the transmission line lengths it is necessary to know the wavelength. It is determined by

$$\lambda = \frac{1}{f\sqrt{\varepsilon_{r,eff}\,\varepsilon_0\,\mu_0}} \tag{5.7}$$

with $\varepsilon_{r,eff}$ as the effective permittivity of the microstrip line, $\varepsilon_0$ as the permittivity constant, $\mu_0$ as the permeability constant and $f$ for the used operation frequency. For the estimation of start up values for the simulation, it is sufficient to calculate with the relative permittivity $\varepsilon_r$, the calculated length will be a bit shorter than the real length. See [66] for further details on calculating $\varepsilon_{r,eff}$.

2. Lumped Inductance replaced by a transmission Line: (Figure 5.9)

An inductance can be replaced by a microstrip transmission line. Its inductance is defined by the length and the width of the distributed element.

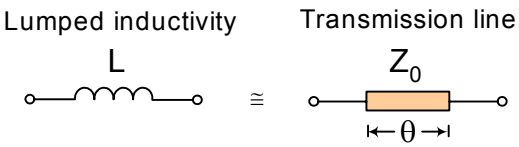


Figure 5.9. Substitution of a lumped inductance by a transmission line.

The width corresponds to the transmission line impedance $Z_0$. For given impedance, the length depends on the operating wavelength. With Eq. 5.8, the length of the line can be calculated by the angle $\theta$.

$$\omega L = Z_0 \sin\theta, \quad \theta \le 45^\circ \qquad (\lambda/4 \equiv 90^\circ) \tag{5.8}$$

3. Grounded lumped inductance connected replaced by a short circuit transmission *line:* (Figure 5.10)

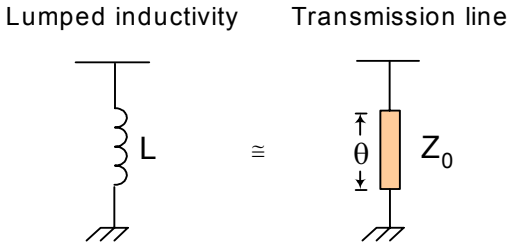


Figure 5.10. Substitution of a lumped inductance by a transmission line.

The RF ground connection could be either made by a radial stub or short circuit (also for DC) transmission line. While a radial stub warrants a low impedance, the direct connection using a wire or a via results in an additional inductance. The radial stub can be substituted by a lumped capacitor as well. Eq. 5.9 gives the needed length and/or width.

$$\omega L = Z_0 \sin\theta, \quad \theta \le 90^\circ \qquad (\lambda/4 \equiv 90^\circ) \tag{5.9}$$

4. Grounded lumped capacitor replaced by an open transmission line: (Figure 5.11)

Using an open ended transmission line gives a capacitor. The capacity at a given frequency is defined as a function of $\theta$ and $Z_0$:

$$\omega C = \frac{\tan\theta}{Z_0}, \quad \theta \le 90^\circ \qquad (\lambda/4 \equiv 90^\circ) \tag{5.10}$$

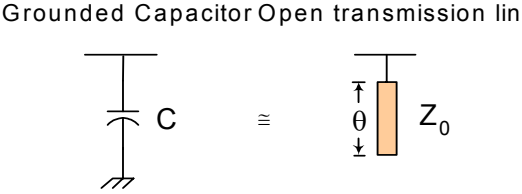


Figure 5.11. Substitution of a lumped capacitor by an open circuit transmission line.

## 5.3 Design Procedure

Designing a broadband amplifier, that is, one which has nearly constant gain over a prescribed frequency range is a matter of surrounding a transistor with external elements in order to compensate for the variation of forward gain $|s_{21}|$ with frequency. This can be done in either of two ways: first, negative feedback or second, selective mismatch of the input and output circuitry. We will use both methods in our work.

### 5.3.1 PA Specifications and Transistor Choice

The first and most important step in a power amplifier design process is to select a suitable transistor for the power stage in order to meet the required specifications of the amplifier. In this work, the design goals were a wide frequency range from 10 MHz to above 2 GHz with a considerably flat gain of ≥ 20 dB and a maximum output power of up to 5 W. Because of the power requirements and the limited operating voltage of LDMOS and HBT devices, impedance transformation would be necessary when using such devices. This is a serious drawback because ultra broadband impedance transformation is complicated. SiC MESFETs overcome this problem and allow drain source voltages of more than 100 V. For a specific output power, the high breakdown voltage makes the possibility to use low current, resulting in high output impedance. Consequently the impedance matching at the output becomes easier using this technology.

The CREE CRF-24010 SiC MESFETs has been selected as power stage for our application. It is specified for applications up to 3 GHz and 10 W of output power. A small signal gain of up to 15 dB is achievable. For the driving stage a GaAs FET (Fujitsu FLL177ME) with the following specifications has been used:

Output power at 1 dB compression point ≈ 32.5 dBm

Small signal gain ≈ 12.5 dB at 2.3 GHz

### 5.3.2 Stability

Stability is a crucial issue when designing PAs because of the combination of capacitive shunt feedback and series feedback, which will include both a resistive and an inductive part that can lead to instability. The power amplifier must be stable under all operating frequencies and all possible load terminations [67]. In other words, we

have to design the power amplifier to reach "unconditional" stability, which means that no matter what the amplifier load is, it does not exhibit spurious oscillations even with drive levels and supply voltages outside their nominal values. Stability considerations can be determined from the S parameters, the matching networks and the terminations of the power amplifier.

The two-port network shown in figure 5.12 is said to be unconditionally stable at a given frequency if the real parts of $Z_{IN}$ and $Z_{OUT}$ are greater than zero for all passive load and source impedances. If the two-port network is not unconditionally stable, it is potentially unstable. That is, some passive load and source terminations can produce input and output impedances having a negative real part. The stability test should be done for every frequency in the desired range

In terms of reflection coefficients, the necessary conditions for unconditional stability at a given frequency are

$$|\Gamma_S| < 1, \tag{5.11}$$

$$|\Gamma_L| < 1, \tag{5.12}$$

$$\Gamma_{IN} = \left| S_{11} + \frac{S_{12}.S_{21}.\Gamma_L}{1 - S_{22}.\Gamma_L} \right| < 1, \tag{5.13}$$

$$\Gamma_{OUT} = \left| S_{22} + \frac{S_{12}.S_{21}.\Gamma_S}{1 - S_{11}.\Gamma_S} \right| < 1 \tag{5.14}$$

where $|\Gamma_S|$, $|\Gamma_L|$ are the source and load reflection coefficients and $|\Gamma_{IN}|$, $|\Gamma_{OUT}|$ are the input and output reflection coefficients of the two-port network. The solutions of (5.11- 5.14) give the required conditions for the two-port network to be unconditionally stable.

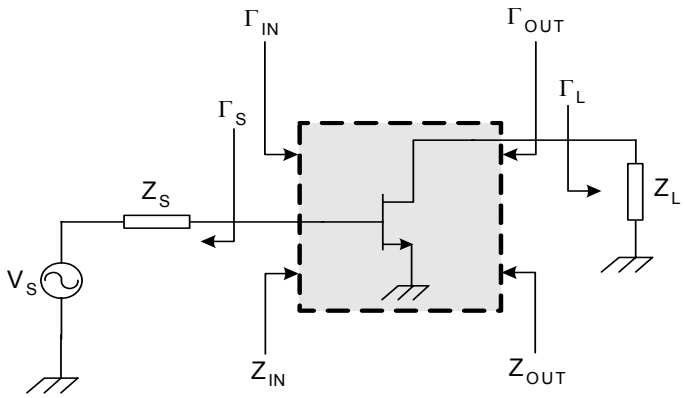


Figure 5.12. Block diagram of a RF amplifier.

The necessary and sufficient conditions for a two-port network to be unconditional stable are [68]

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}.S_{21}|} > 1, \tag{5.15}$$

$$|\Delta| = |S_{11}.S_{22} - S_{12}.S_{21}| < 1. \tag{5.16}$$

There are two ways to overcome the stability problem of the transistor amplifier. The first is to use some form of feedback to stabilize the amplifier. The second is to use a graphical analysis to determine the regions where the values of $\Gamma_S$ and $\Gamma_L$ (source and load reflection coefficients) are less than one, which means the real parts of $Z_{IN}$ and $Z_{OUT}$ are positive.

Substituting the values of $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$ in equations (5.13) and (5.14) and solving for $\Gamma_S$ and $\Gamma_L$ result in the stability circles. The radii and centers of the circles are given by [69].

1. Output Stability Circle,

$$r_L = \left| \frac{S_{21}.S_{12}}{|S_{22}|^2-|\Delta|^2} \right| \tag{5.17}$$

$$C_L = \frac{\left(S_{22}-\Delta.S_{11}^*\right)^*}{|S_{22}|^2-|\Delta|^2} \tag{5.18}$$

2. Input stability circle

$$r_S = \left| \frac{S_{21}.S_{12}}{|S_{11}|^2-|\Delta|^2} \right| \tag{5.19}$$

$$C_S = \frac{\left(S_{11}-\Delta.S_{22}^*\right)^*}{|S_{11}|^2-|\Delta|^2} \tag{5.20}$$

The stability circles need to be plotted in the Smith chart to determine the stable regions or in other words, the regions where values of $\Gamma_S$ and $\Gamma_L$ produce $|\Gamma_{OUT}| < 1$ and $|\Gamma_{IN}| < 1$. Stabilizing a device to be used in a wideband design with resistive loading at the input and/or with voltage-shunt feedback is realistic. Figure 5.13 shows a combination of series loading ($C_S$ and $R_S$) and voltage-shunt feedback ($C_F$ and $R_F$) in a realistic topology from which stability of the device can be achieved.

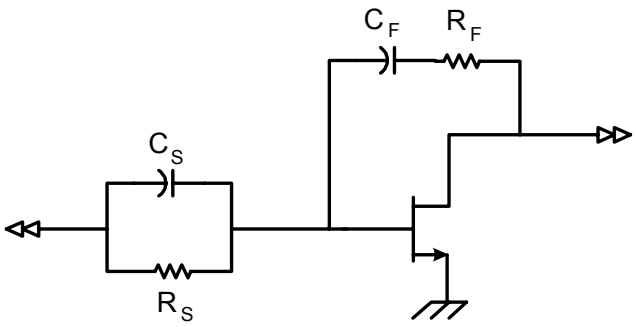


Figure 5.13. Passive-network stabilization.

As we said before, MESFET transistors are conditionally stable, therefore, it is possible to first stabilize the used transistor using a resistive loading. The DC biasing circuit should be taken into account when analyzing stability, i.e. it is part of the input and output network. Even though it is designed to present high impedance to the RF signal at the design frequency, it is not a real open circuit.

An optimization process using Advanced Design System Simulator (ADS) has been accomplished and iterative values for the resistive loading resulting in a stable system could be extracted. Figure 5.14 illustrates the stability factor versus at $V_{DS}$ = 30 V and $I_D$ = 500 mA.

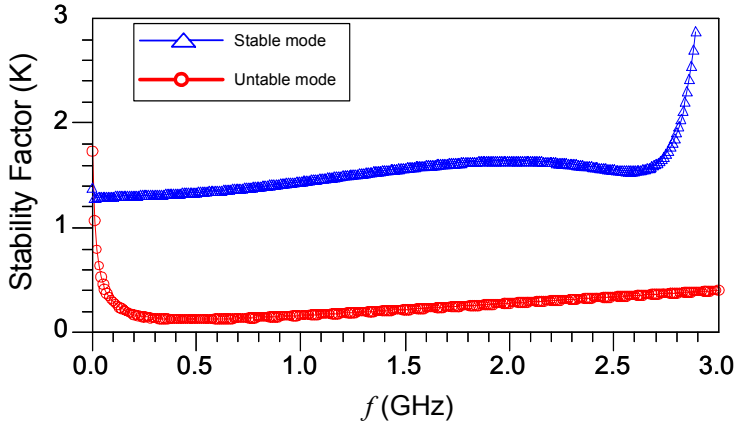


Figure 5.14. Stability factor of the SiC MESFET versus frequency.

### 5.3.3 Power Gain

The main issue of designing PAs is the power gain, rather than voltage gain and current gain. Generally, power again can be defined as

$$G = 10 \log \frac{P_{OUT}}{P_{IN}} \quad \text{(dB)} \tag{5.21}$$

Otherwise, several power gain equations appear in the literature and are used in the design of microwave amplifiers, such as transducer power gain $G_T$, available power gain $G_A$, and operating power gain $G_P$. The transducer power gain, $G_T$, is defined as the ratio of the power delivered to the load to the power available from the source and is given by

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{5.22}$$

The available power gain, $G_A$, is defined as the ratio of the power available from the network to the power available from the source. The following equation describes the ratio in terms of the reflection coefficients as

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{OUT}|^2} \tag{5.23}$$

The power gain $G_P$ is defined as the ratio of the power delivered to the load to the input power to the network and can be given by

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{5.24}$$

When input and output are both conjugately matched to the two port, then the gain is maximized and $G_P = G_T = G_A$. It is required to design an amplifier with small signal gain with gain ripple of ± 1 dB. The prescribed small signal gain with small fluctuations can be achieved from a two stage PA using a simple shunt feedback technique. Such form also improves the amplifier stability. Based on the analysis given in the literature (Appendix A), the values of $R_{Fi}$ that satisfy the desired gain are given by [70]:

$$R_{Fi} = Z_0\left[1+|S_{21}|\right] \quad \text{for } |R_F| > Z_0 \tag{5.25}$$

where $Z_0 = 50$ Ohm, $|S_{21}|^2$ is the small signal gain of the stage. The feedback capacitor is used to bypass only the RF signal and block the DC between gate and drain. Figure 5.15 shows the small signal gain of a single stage amplifier before and after adding a shunt feedback network followed by optimizing both input and feedback networks for maximum gain flatness and minimum input return loss. It can be seen in the figure that a gain flatness of ± 1 dB over the operating bandwidth has been achieved.

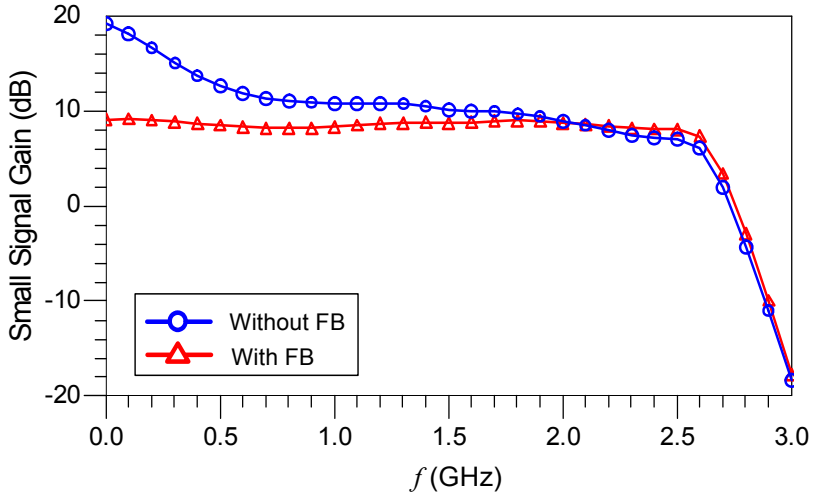


Figure 5.15. Small signal gain of the SiC MESFET with and without feedback network.

### 5.3.4 Broadband DC Biasing Network

In this section, design of a DC biasing circuit that isolates RF from DC in the desired bandwidth is presented. It simply consists of an inductance (choke) and a capacitance in T-junction (DC feeding and blocking). While designing the broadband choke, it is required to get a large enough inductance at low frequencies and at the same time a sufficiently high self-resonance frequency (SRF) [11]. These requirements can be met using ferrite-loaded coils. An efficient and accurate technique was used that depends mainly on building a large number of different air-core and ferrite coils with different sizes (their values depend on the core material, number of turns, wire length and height of core), then testing each one on a board such as in figure 5.16. Reflection and transmission coefficients and the input impedance are measured. The three coils in combination with a small resistor in between two parallel bypass capacitors have been found as a suitable solution (see Figure 5.17). The capacitance values $C_1$ and $C_2$ are selected to give very low reactance over the whole operating frequency range. Together with the low impedance resistor they are responsible, too for supporting absolute stability over the whole operating range of the amplifier. The DC blocking capacitors ($C_B$) have to provide a good RF through over the whole bandwidth.

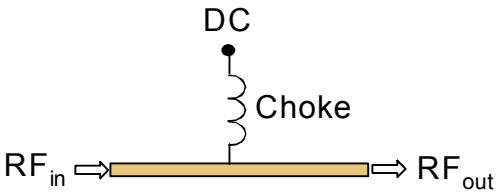


Figure 5.16. Schematic of the board for the choke under test.

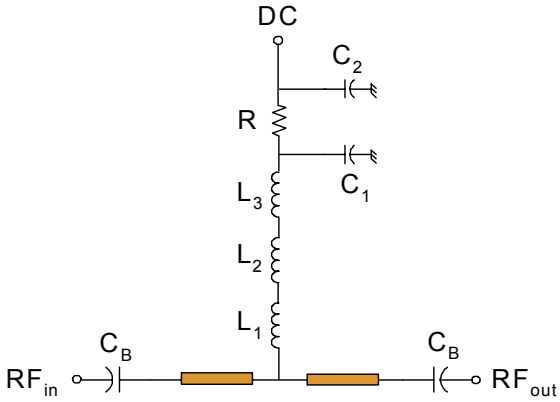


Figure 5.17. DC biasing network.

Figure 5.18 shows the simulated and the measured reflection and transmission coefficients of the proposed combination over the desired frequency range. From the diagram, a maximum loss of 0.4 dB and a RF isolation of greater than 20 dB can be achieved. Excellent agreement between the simulated and the measured results can also be observed.

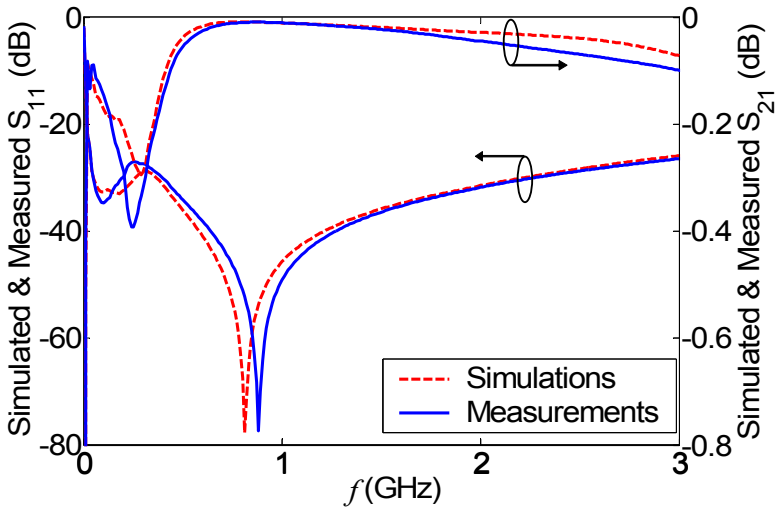


Figure 5.18. Simulated and measured S-parameters of broadband choke.

The values of the DC blocking capacitors ($C_B$) can be chosen such that they do not influence the matching of the circuit. This means, the impedance of these

capacitors at the frequency of interest has to be small enough to be considered as a short for RF signals.

$$C_B = \frac{1}{2\pi f_{low} |Z_{Cblock}|} \tag{5.26}$$

### 5.3.4.1 DC-DC Converter

When biasing MESFETs, power sequencing becomes very important in order to ensure that the amplifier is not overstressed. From I − V curves it can be observed that if the drain voltage would be applied first, while the gate remained unbiased, then the current through the device would be at its maximum, consequently it may destroy the device. Instead, the negative voltage should be applied first, which holds the FETs pinched off to keep power dissipation low until the drain voltage reaches its desired value. Based on the above requirements, a DC-DC converter for the two stage power amplifier has been developed. Figure 5.19 shows a block diagram for a DC converter biasing two different FETs while the complete PCB layout of the converter is illustrated in figure 5.20. The developed DC converter consists mainly of three blocks: a voltage regulator to limit the input voltage to the desired drain voltage, a negative charge pump to convert the positive voltage into a negative one, and finally a MOS switch which is controlled by the negative gate voltage. The switch output only goes on when the controlled voltage is low and vice versa to ensure the power sequence of the MESFETs.

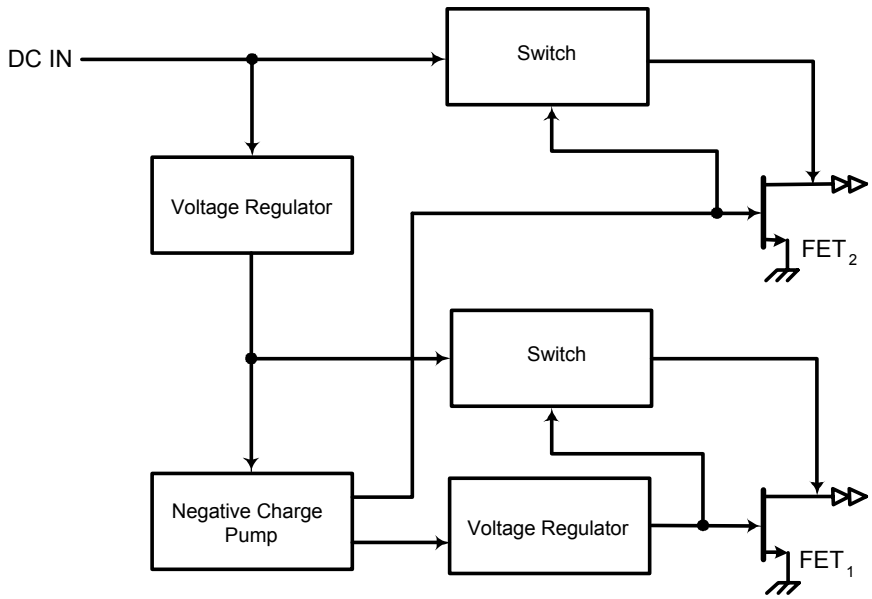


Figure 5.19. Block diagram of the DC-DC converter for the two stage power amplifier.

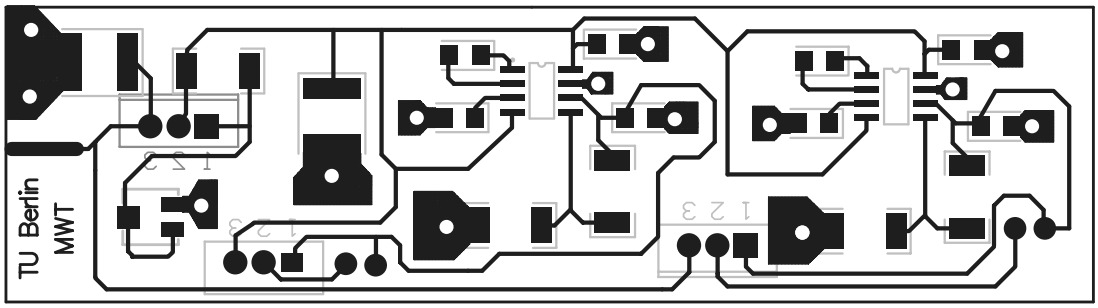


Figure 5.20. PCB layout of DC biasing network for the two stage power amplifier.

## 5.3.5 Output matching for maximum output power

### 5.3.5.1 Power matching techniques

Power matching is the most important process in the power amplifier design procedure. Generally, power matching techniques can be divided into two categories, namely, designs based on measured load-pull characteristics and the simple load line method. The design technique emphasized here is the load line approach or the Cripps method [15].

1. Load pull method

The design procedure of the power amplifier is basically the same as that of a small signal amplifier. However, there is an important issue to be considered: the network analyzer used to measure S-parameters of transistors can only operate under small signal conditions. In fact, due to the high mismatch of the power transistors (before implementing matching networks), even under sufficient output power for the network analyzer, the measured results will be significantly different from the actual characteristics. Hence, how to measure the transistor characteristics under large signal conditions for PA operation becomes a vital point for PA design.

The load-pull methods are the conventional way for power transistor measurement. A load-pull test measurements setup shown in figure 5.21 consists of the device under test (DUT) with some form of calibrated tuning device at its output. The output tuner centered between a driver amplifier and an attenuator is adjusted to maximize the output power. The tuner impedance and associated output power for enough additional tuner settings are then measured to plot constant power contours on

a Smith chart. A set of load-pull data may take weeks, days or minutes to compile, depending on the degree of complexity, expense, and time invested in the equipment.

By load-pull measurement, the optimum input and output load impedance (power contours) on the Smith chart are obtained. We can design match networks to achieve the desired output power and input reflected power levels. This method is the most accurate for power matching. However, the measurement process is quite heavy and complicated, so that all details must be considered carefully. High cost of the instrument equipment is another disadvantage of this method.

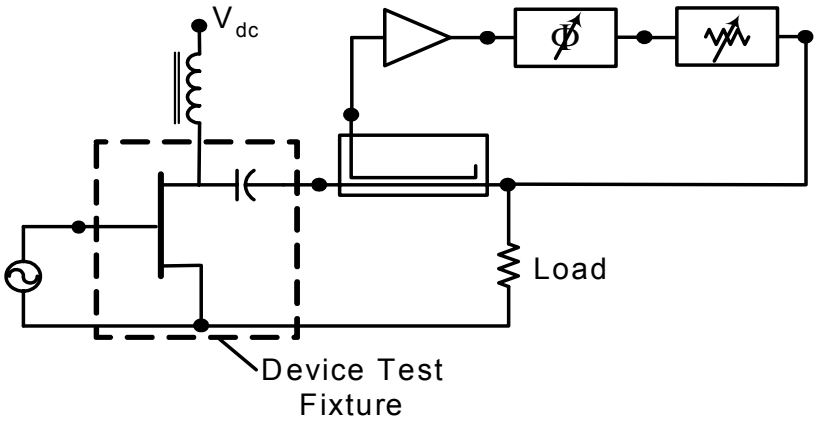


Figure 5.21. Active load pull measurement system.

2. Cripps method:

Cripps method (Optimum load-line method) is a simple but effective approach to achieve maximum output power; it is very effective for the MESFET power amplifier design. Figure 5.22 illustrates the simple yet effective optimum load line (Cripps method) theory to achieve maximum output power.

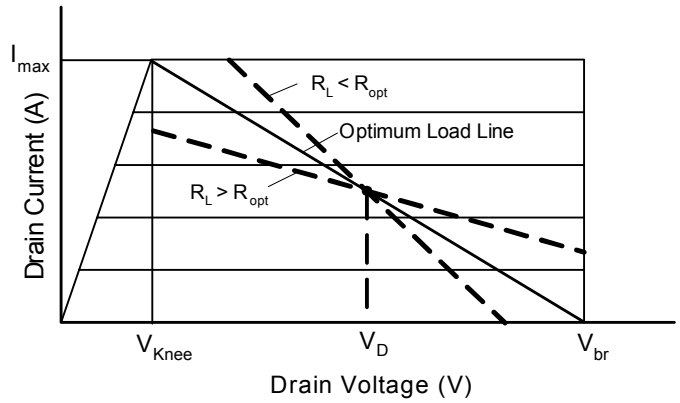


Figure 5.22. Load-line method.

Assuming the DC-IV curve of a device is bounded by its maximum drain current Imax, knee voltage $V_{knee}$ and drain breakdown voltage $V_{br}$, and the device is biased in

class A mode ($V_D = (V_{br} - V_{knee}) / 2$, $I_D = I_{max}/2$), then the optimum load for the maximum output power would be:

$$R_{opt} = \frac{V_D - V_{knee}}{I_{\max}/2} \tag{5.11}$$

Since in that situation, the device could achieve the maximum current and voltage swing at the same time, and the power delivered to the load would be

$$P_{opt} = \frac{1}{8}(V_{br} - V_{knee})I_{\max} = \frac{1}{8}\frac{(V_{br} - V_{knee})^2}{R_{opt}} = \frac{1}{8}I_{\max}^2 R_{opt} \tag{5.12}$$

If $R_L > R_{opt}$, then the voltage boundary would be the limiting factor and the power delivered to the load is given by

$$P_{RF} = \frac{1}{2}\frac{(V_{br} - V_{knee})^2}{R_L} = P_{opt}\frac{R_{opt}}{R_L} < P_{opt} \tag{5.13}$$

Similarly, for $R_L < R_{opt}$, with which the device is limited by the current boundary, the power delivered to the load is

$$P_{RF} = \frac{1}{8}I_{\max}^2 R_L = P_{opt}\frac{R_L}{R_{opt}} < P_{opt} \tag{5.14}$$

When the load is no longer a pure resistance, then the load line is no longer a straight, instead, it becomes an ellipse. The major axis of the ellipse lies along the load line for maximum RF output power and the ellipse is bounded by $0 < I_D < I_{max}$ and $V_{knee} < V_D < V_{br}$.

### 5.3.5.2 Output Matching Network Design

Numerical load pull optimization has been performed at the highest frequency to indemnify the 5 W output power at 2.4 GHz. In our broadband application load pull characterization at lower frequencies is less important because the optimum load impedance is not sustainable over the full bandwidth. On the other hand, power requirements at lower frequencies become more and more relaxed, too. Figure 5.23 shows the circuit topology to extract the load pull contours based on ADS simulation. The parameters $R_{F2}$, $C_{F2}$, $R_{S2}$ and $C_{S2}$ were predefined in the previous sections while the load tuner has been swept. Figure 5.24 (a) shows the output power versus the load at 2.4 GHz.

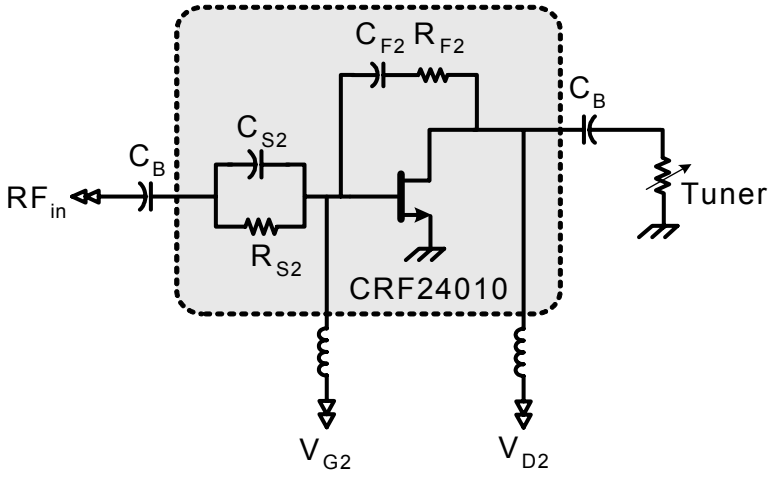


Figure 5.23. Load pull tuning based on the developed model.

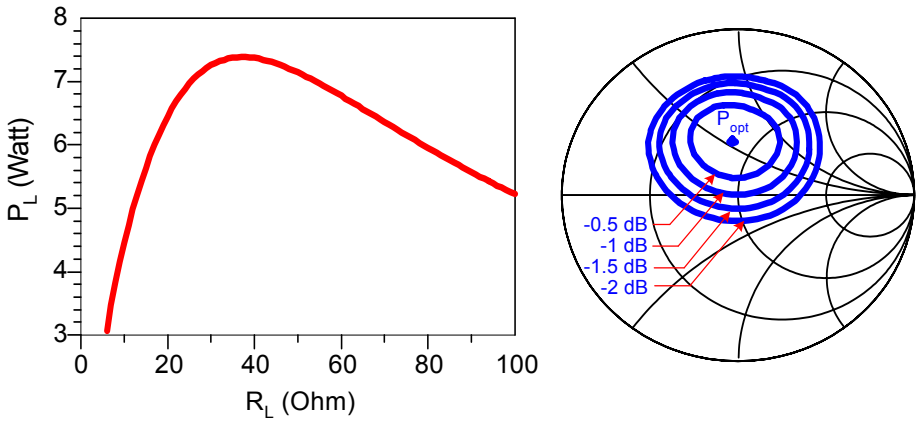


Figure 5.24. (a) Output power of the power stage transistor (CRF24010) versus load, (b) Simulated load pull contours at $f = 2.4$ GHz.

From the figure, a maximum output power of 7.4 W at 37 Ohm can be achieved. In the same manner, the optimization procedure has been continued to extract the optimum source impedance which is found to be 4 +j 4 Ohm at 2.4 GHz. The optimum output power has been slightly increased by 0.2 W. The simulated load pull data at the optimum load are shown in figure 5.24 (b).

The design of the output matching network synthesis (OMN) was started as described in [13], [14]. Initial load and source impedance values were taken from load pull analysis. Further goals of this first design cycle were little network complexity, gain flatness, an output return loss and an output power of at least 10 dB and 5 W, respectively over the full bandwidth. It has been found that the design goal can be firstly achieved by a simple LC low pass network. The final design has been realized using microstrip elements as shown in figure 5.25 (a) and the corresponding simulated

output return loss is shown in figure 5.25 (b). At least 10 dB output return loss can be achieved over the frequency band (0.01-2.4 GHz). By this procedure, the load impedance of the interstage matching network (optimum source impedance of the SiC FET) was found, too.

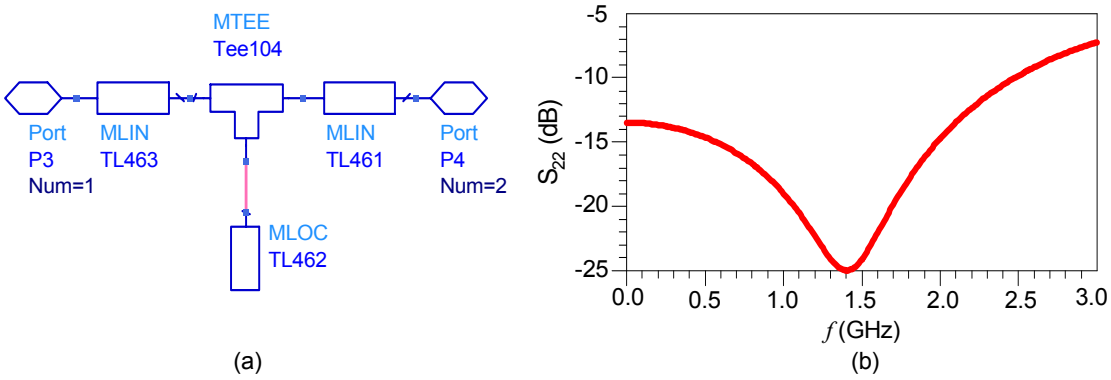


Figure 5.25. (a) Output matching network topology, (b). Simulated output return loss of the power stage amplifier.

## 5.3.6 Input matching for maximum gain

For the GaAs driver FET load pull analysis was performed, too. The procedure of extracting the optimum load and source impedances which result in maximum output power from the driver stage has been manipulated in the same manner as presented in detail in the previous section. Figure 5.26 depicts the circuit diagram used in the load pull technique. Based on ADS model (Fujitsu FLL177ME), the optimum load and source impedances were found to be 15 Ohm and 2 Ohm, respectively at 2.4 GHz result in maximum output power of 1.68 W from the driver. Figure 5.27 (a) shows the driver output power at various load resistances while the simulated load pull data at the optimum load and source impedances are depicted in figure 5.27 (b).

The input matching network was found in a similar manner using a 50 Ω match and the GaAs FET input impedance as source and load impedances for the matching network. Three matching sections (a microstrip line together with an open stub in low-pass form) had to be used at the input to realize the high impedance transformation ratio necessary for matching the 50 Ω source impedance. Figure 5.28 (a), (b) show respectively, the input matching network structure and the corresponding input return loss after adding the network. It can be observed that

maximum input return loss of 10 dB in the frequency range from 10 MHz to 2.4 Ghz can be obtained.

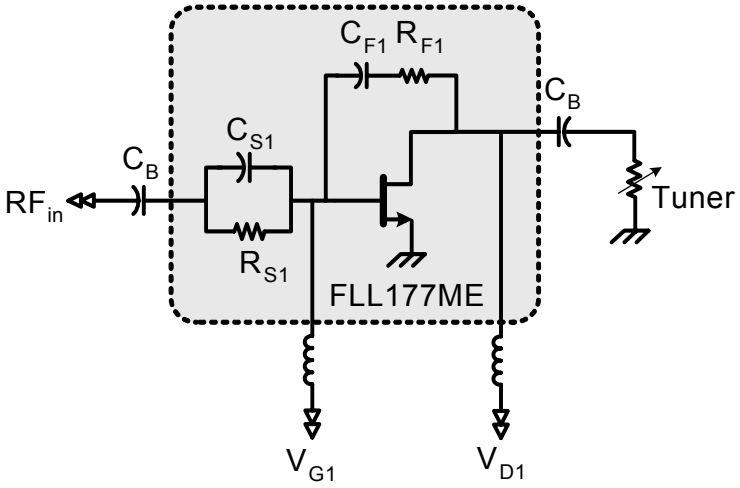


Figure 5.26. Load pull tuning of the driver GaAs FET.

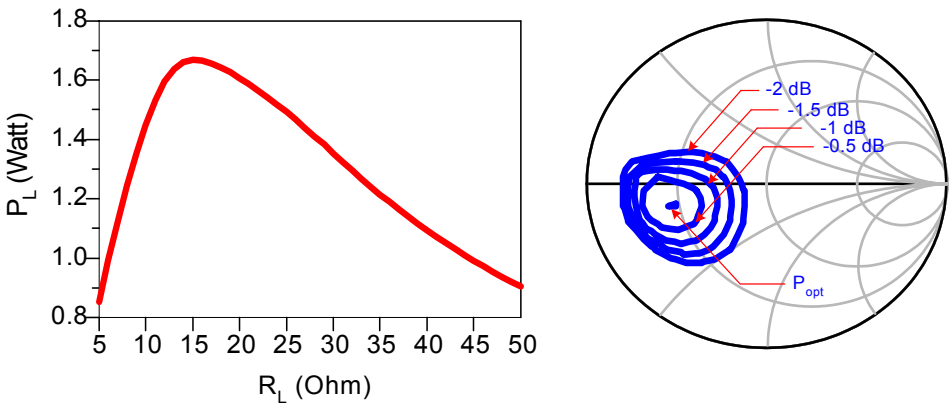


Figure 5.27. (a) Output power of the driver transistor (FLL177ME) versus load, (b) Simulated load pull contours at $f = 2.4$ GHz.

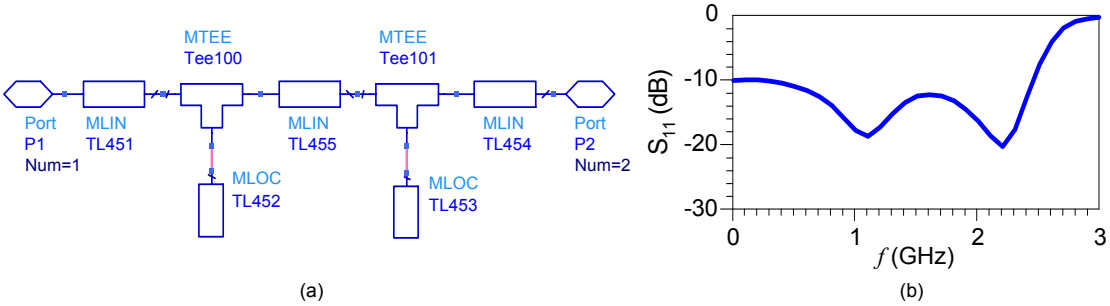


Figure 5.28. (a) Input matching network of the driver stage, (b) Simulated input return loss.

## 5.3.7 Interstage Matching Network design

An interstage method for broadband amplifier design suitable for CAD has been developed. The concept topology is shown in figure 5.29 (a). Both driver and power

stages have a gain that decreases with increasing frequency. The specifications for a good input and output match will require that the input and output matching networks have a constant gain over the frequency range of the amplifier (i.e., flat gain response). The interstage matching network must provide a gain having a positive slope with increasing frequency to compensate for the transistor roll-off and therefore, to give an overall flat frequency response. The so found load impedance together with the source impedance of the SiC power FET have used as input data for synthesis and optimization of the interstage matching network (ISMN) with respect to maximum and flattened power transfer. A tapered microstrip line together with a low-pass section has been found as most suitable solution as shown in figure 5.29 (b).

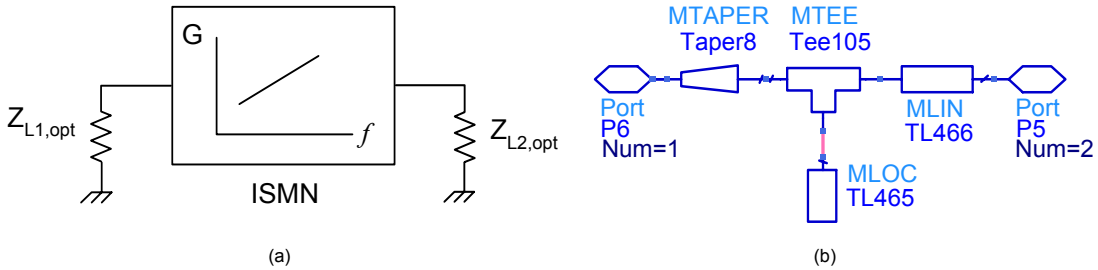


Figure 5.29. (a) Interstage matching topology, (b) ISMN network.

After finding the initial topologies and element values by the described procedures, the final design parameters were found by an overall optimization of all amplifier design parameters. During this final step, the described design strategy has been found to be very suitable. The circuit simulations were performed by using Agilent ADS Simulator. The substrate material data are based on ROGERS 4003 laminate with a permittivity of 3.38 and a thickness of 0.51 mm.

## 5.4 Design examples

The procedure of designing the matching circuits for an unconditional stable power amplifier is summarized in the following steps:

1. Select the transistor to provide the required output power
2. Obtain the optimal load impedance of the power stage for maximum output power from load-pull simulation using large signal model or using load line method.
3. Design the output matching circuit as an impedance transformer to transfer 50 Ohm into the optimum load impedance of the output stage.

4. Design the input matching circuit to provide a conjugate match between the input impedance and 50 Ohm so that a good input return loss can be obtained.

5. Design the interstage matching circuit with a positive gain slope to flatten the overall power gain of the amplifier.

6. Optimize the input and interstage matching circuits for the best performance in terms of input VSWR, power gain, and gain ripple.

7. Perform analysis using a large signal model to obtain output power, power added efficiency, and power gain at 1 dB compression point.

8. Repeat any previous steps if the large signal performance requirements are not satisfied.

In this section, we introduce five power amplifier generations; 5 W wideband single stage and two stage power amplifiers, an ultra wideband PA (up to 5 GHz) based on a SiC Die with saturated output power ≥ 37 dBm. The last example will be a 10 W narrowband PA using a SiC Die MESFET. All the matching networks in the design have been developed based on microstrip transmission lines. Measured and simulated results of the implemented amplifiers will be presented and discussed in the next chapter in more detail.

### 5.4.1 5 W wideband single stage PA

As discussed in Sec. 5.2, a SiC MESFET has been selected to give 37 dBm typical power at its 1 dB compression point. A feedback branch with $R_{F2}$ = 200 Ohm for 9 dB small signal gain and $R_{S2}$ of 2 Ohm for K >1.3 have been selected. The design begins with synthesizing the output load network. The network must transform the 50 Ohm load impedance to the optimum load impedance $Z_{opt}$ required by the FET. The optimum load impedance has been determined with the aid of load pull data based on the derived model for the SiC MESFET as discussed in Sec. 5.3.2, $R_{opt}$ was found to be 37 Ohm at 2.4 GHz.

Using the target values for the terminating impedance, a lumped element matching network has been synthesized based on the presented analysis in Sec. 5.2. Then the lumped element components have been converted to a distributed structure. Computer optimization based on ADS Simulator has been used to trim the network performance.

Taking into consideration the optimum source impedance of $4 + j4$ Ohm at 2.4 GHz, the input matching network has been synthesized in a similar manner in lumped element form. The network has been converted to microstrip topology. Amplifier gain flatness has been achieved by only optimizing the input network of the complete circuit. The complete schematic including the bias circuitry, SMT library parts, vias, and appropriate microstrip matching elements is illustrated in figure 5.30.

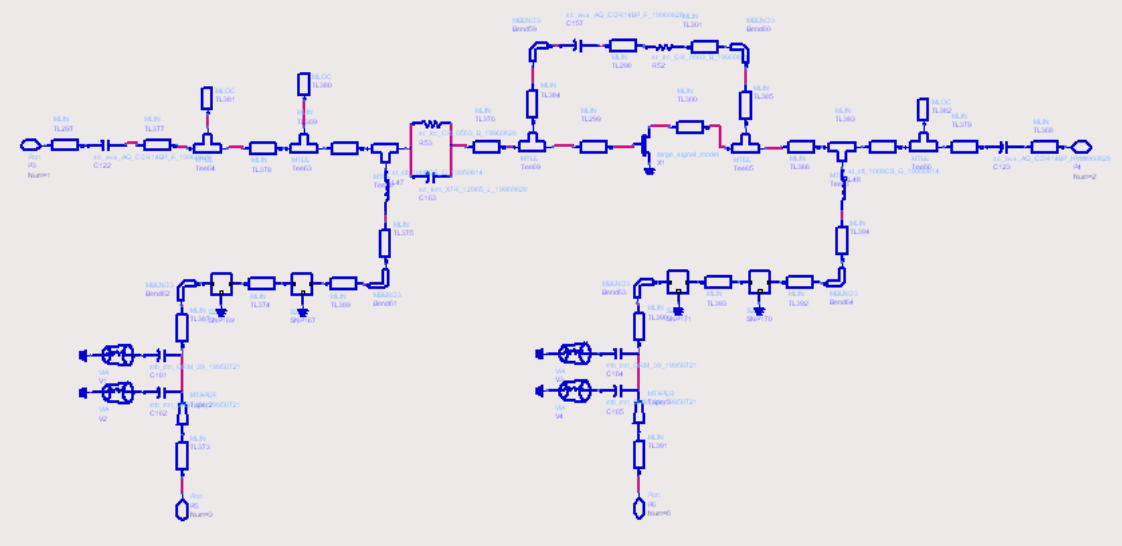

Figure 5.30. Schematic diagram of the power stage amplifier.

The resulting small signal gain, stability factor and input and output return losses are shown in figure 5.31. Power and linearity performance of the power stage amplifier will be presented and discussed in detail in the next chapter.

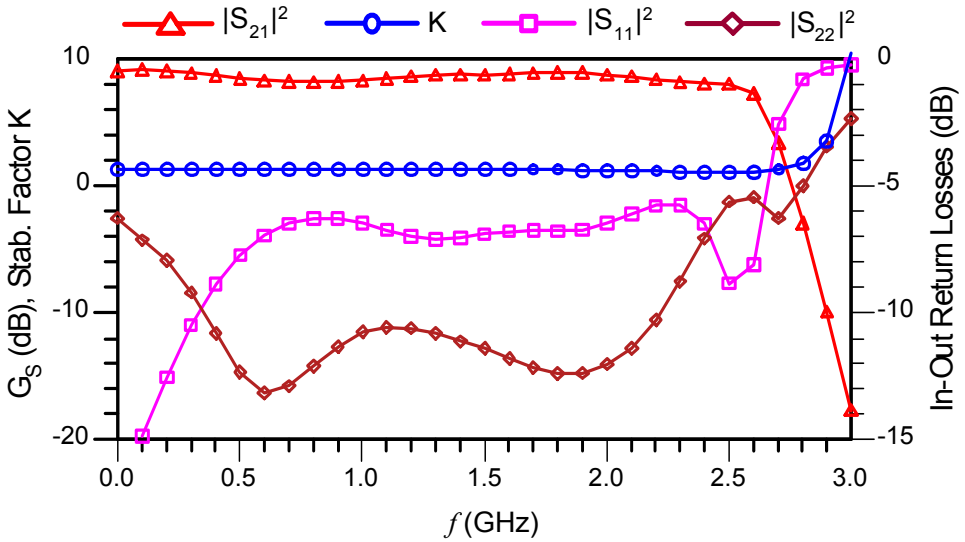


Figure 5.31. Small signal performance of the power stage.

### 5.4.2 5 W wideband two stage PA

It is always necessary to have a driver that provides enough power for the last stage which contains the largest size of power device. The amplifier consists of three basic networks: input network, interstage network and output network. As in the case of single stage PA design, the output matching network for maximum output power has been designed to terminate the SiC MESFET with the optimum load impedance, the input network of the driver stage must provide high input return loss and maximum available gain. The interstage network is used to provide the necessary gain shaping required compensating for the roll-off of each FET and power transfer performance between amplifier stages. This can be accomplished by using a tapered microstrip line between the stages. Thus the completed amplifier can exhibit flat gain and power performance for broadband operation. The synthesized networks are usually in a lumped element form, which are later converted to the distributed form. Excellent gain flatness performance for small signal operation is obtained based on the method described by Mellor [50]. The problems in designing multistage amplifiers with lossless networks can be eliminated or at least significantly reduced by either employing RF feedback techniques or some form of lossy matching networks such as the series combination illustrated in figure 5.13. The feedback resistors, $R_{F1}$ and $R_{F2}$ are selected to be 220 Ohm and 200 Ohm, respectively, for obtaining an overall gain of 23 dB, with small fluctuations of ± 1 dB. Input and interstage matching networks have been optimized in order to improve the gain performance and minimize the input return loss. Figure 5.32 shows the schematic diagram of the implemented amplifier.

Simulated small signal amplifier performances are depicted in figure 5.33. It is observed from this figure that a high gain of 23 ± 1 dB in the operating bandwidth can be achieved. Acceptable input and output return losses of 7 dB and 8 dB, respectively can be satisfied.

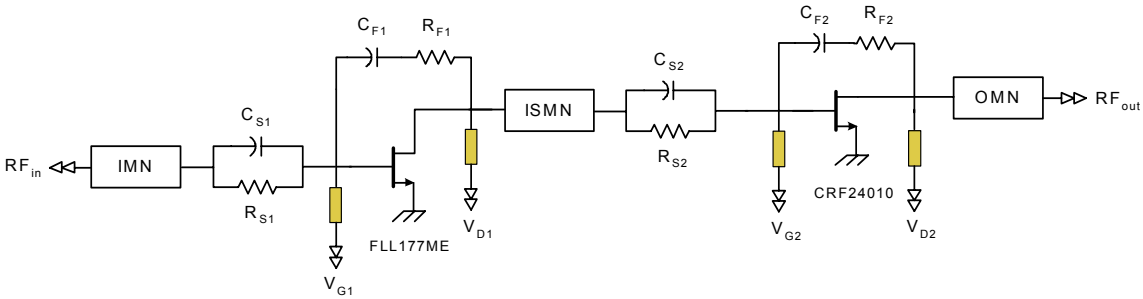


Figure 5.32. Schematic diagram of two stage power amplifier.

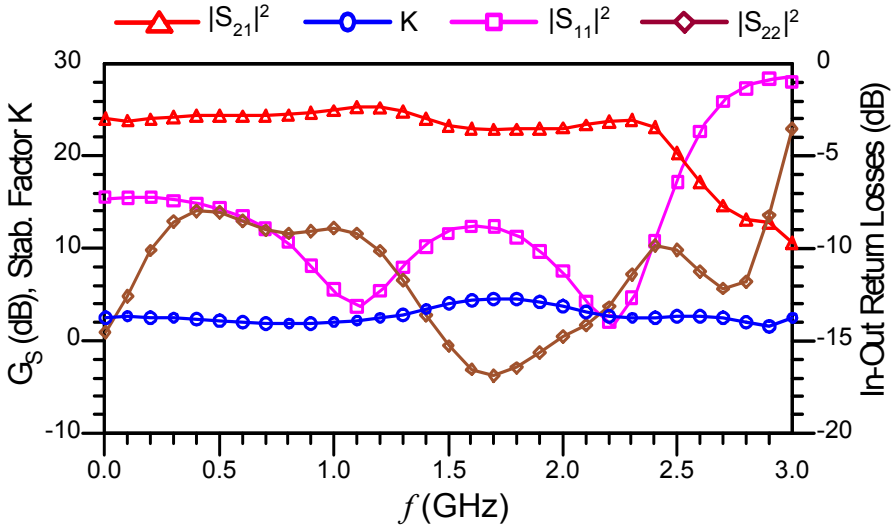


Figure 5.33. Small signal performance of two stage power amplifier.

### 5.4.3 5 W ultra wideband single stage PA using SiC Die

The new SiC CRF24010 chips have also been used in this work. An ultra wideband PA operating in the frequency range 1 MHz – 5 GHz has been simulated. Input and output matching networks based on multisection microstrip technique have been developed. Gain flatness of ± 1 in the operating bandwidth can be achieved by inserting a R-C feedback combination between gate and drain. The schematic diagram of a single stage PA using a SiC chip is shown in figure 5.34 while the corresponding simulated small signal performances are illustrated in figure 5.35. 6 ± 1 dB small signal gain and ≥ 9 dB output return loss can be seen in the figure.

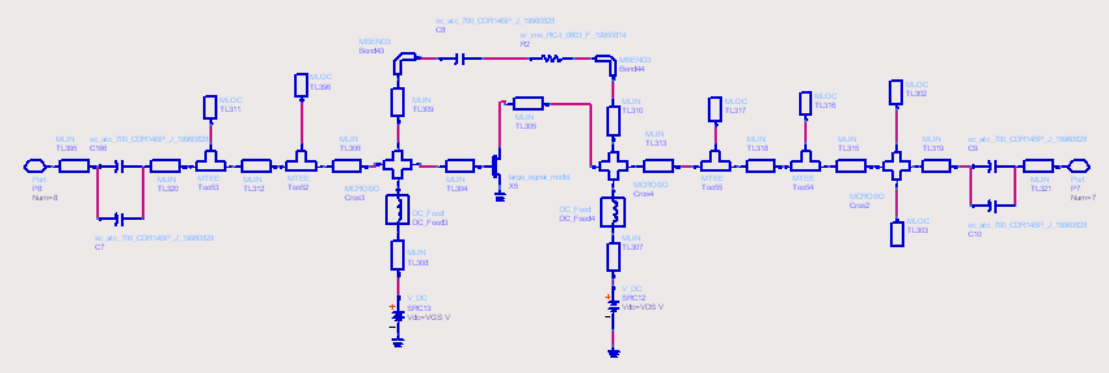

Figure 5.34. Schematic diagram of the power stage using a SiC Die.

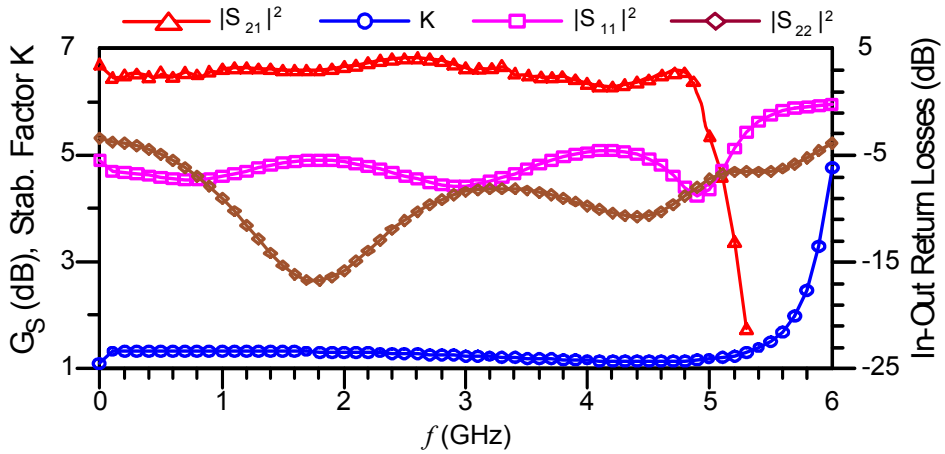


Figure 5.35. Small signal performance of the 5 W ultra broadband single stage PA using a SiC Die.

### 5.4.4 5 W ultra wideband two stage PA using SiC Die

High gain is also desired in power amplifier design. A driver stage based EFA960B Die from EXCELICS with the presented specifications in table 5.1 has been used. A two stage ultra wideband, high gain power amplifier has been designed.

| | |
|---|---|
| Output Power (dBm) | 36 |
| Gain at 2 GHz (dB) | 16 |

Table 5.1. Specifications of EXCELICS GaAs FET from datasheet.

In the same manner as described in example (2), the interstage network has been designed to compensate the roll off of the driver and power stage MESFETs. Continuing the work done in the previous example for both input and input matching networks, a multisection interstage matching network based on microstrip to meet such broad-bandwidth has been used. Figure 5.36 shows the schematic diagram of the simulated amplifier.

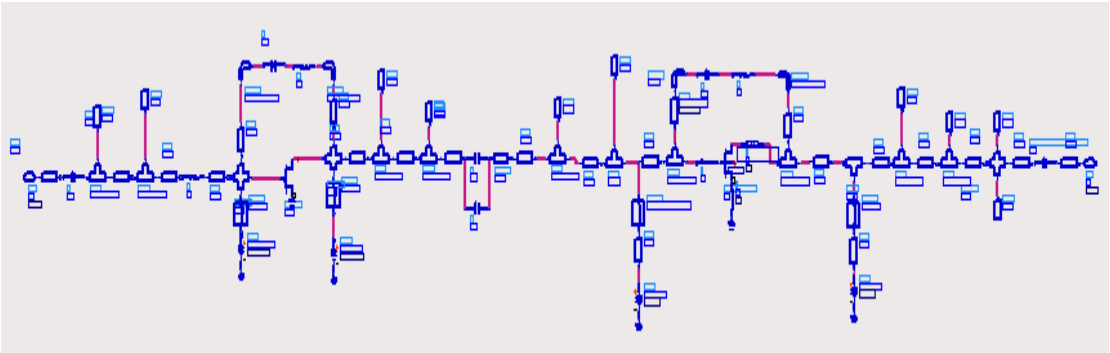

Figure 5.36. Schematic diagram of the ultra broadband two stage PA using a SiC Die.

Figure 5.37 illustrates the simulated small signal performance of the simulated amplifier. A small signal gain of 17 ± 1 dB at the cost of poor input matching can be obtained. Except for the small frequency band from 0.1 GHz to 0.8 GHz, an output return loss of ≥ 6 dB can be achieved. This values can be improved if additional work can be spent.

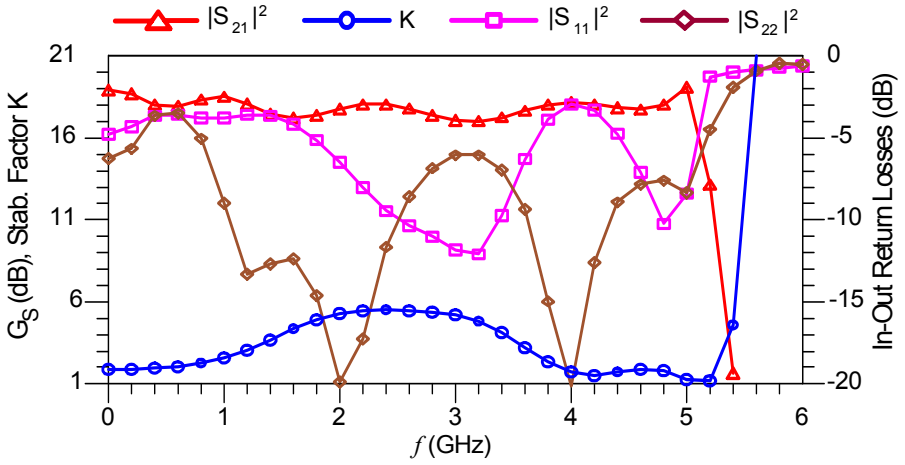


Figure 5.37. Small signal performance of the 5 W ultra broadband two stage PA using a SiC Die.

## 5.4.5 10 W high gain single stage PA using a SiC Die

In this example, the derived model for the CRF24010 SiC MESFET has been used in the harmonic balance ADS simulator to achieve 10 W (40 dBm) output power over a frequency range from 3.1 GHz to 3.5 GHz. An amplifier with 15 dB gain over the prescribed bandwidth is required. An output matching network using the lumped elements has been developed whereas the chip input impedance has been transformed to 50 Ohm via two inductors and a short circuit stub as shown in figure 5.38.

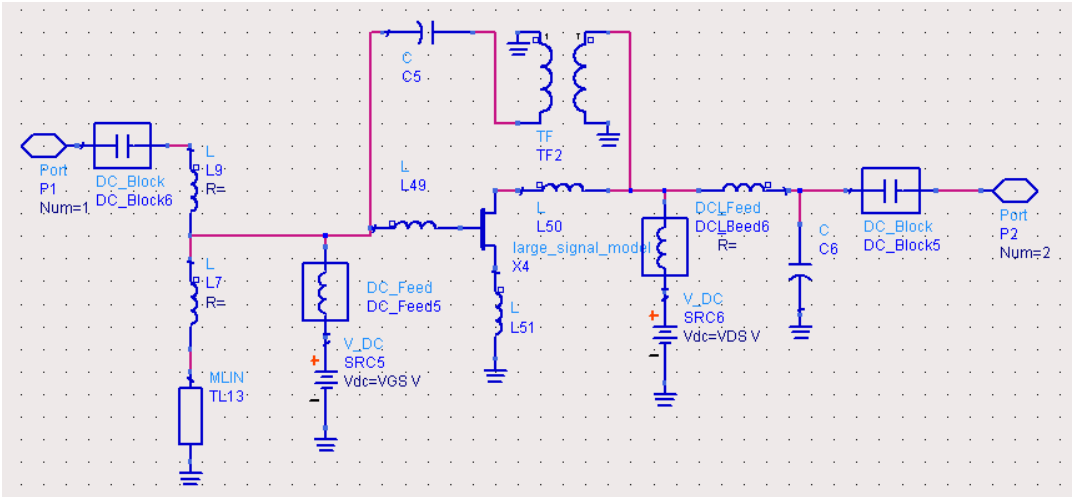


Figure 5.38. Schematic diagram of the high gain 10 W power amplifier.

Maximum flat gain can be obtained in this case by canceling the reactance between gate and drain. This can be done by adding a capacitance with the same value of $C_{gd}$ and a 1:1 ideal transformer. The input matching network together with the feedback compensation have been optimized to achieve maximum flat gain, and minimum input return loss. Figure 5.39 shows the simulated small signal results: small signal gain $G_S$ greater than 17 dB with ± 0.5 dB, and input and output return losses of greater than 8 and 10 dB respectively, have been achieved. The large signal performance of the designed amplifier will be presented and discussed in detail in the next chapter.

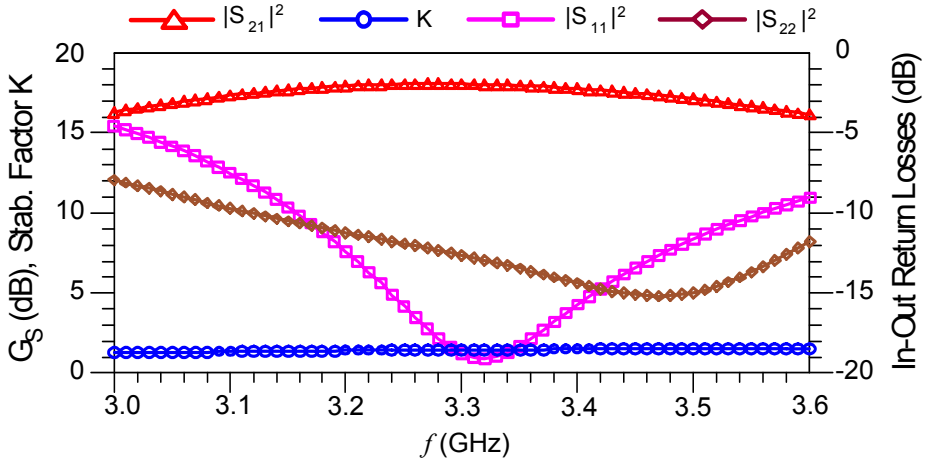


Figure 5.39. Small signal performance of the 10 W high gain single stage PA.

# CHAPTER SIX

# POWER AMPLIFIER PERFORMANCE

Power amplifier performance includes small signal performance, power performance (output power, power gain, and power added efficiency) and linearity performance (AM-AM and AM-PM conversions, and intermodulation distortion based on two tone measurements (second– and third– order intercept points)). Small signal and large signal simulations of the designed amplifiers based on the derived model will be presented and discussed in this chapter in details. As discussed in chapter 5, we have presented five different power amplifier categories; two of them (single stage wideband power amplifier and two stage wideband power amplifier) based on SiC MESFET have been designed and measured. Measurements of the designed amplifiers will be compared to the simulations. Impact of the driver stage on the overall performance of two stage PA will be discussed. Simulation performance of the other categories (ultra wideband single stage PA, ultra wideband two stage PA, and high power narrow band PA) based on SiC MESFET Die, will also be presented and discussed in this chapter.

## 6.1 Small Signal Performance

In this section, we introduce the simulated and measured small signal performance of two amplifiers: a 5 W wideband single stage PA, and a 5 W wideband PA. S-parameter simulation has been performed using the Advanced Design System (ADS) from Agilent *Eesof* while the small signal measurements have been accomplished with a vector network analyzer (VNA) as shown in figure 6.1.

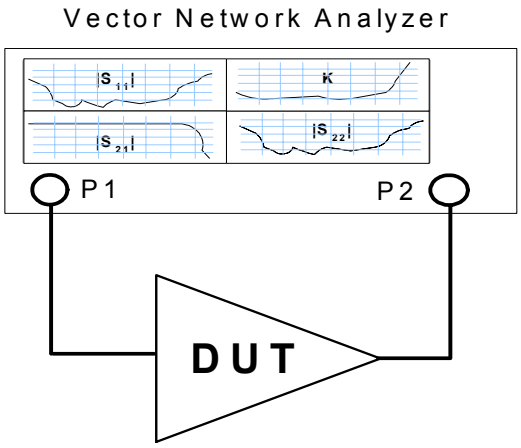


Figure 6.1. Measurement setup of small signal performance.

### 6.1.1 5 W Wideband Single Stage PA

The small-signal S-parameters were measured at $V_{DS}$ = 30 V, $I_D$ =500 mA. Figures 6.2, 6.3 show the simulated small signal gain, the stability factor (K) and the return loss compared to the measured results. Both simulated and measured gain show a low ripple (± 1 dB) over the frequency range from 10 MHz to 2.4 GHz. Small signal gain of 8 ± 1dB and stability factor of greater than 1.3 can be obtained. Good agreement can be observed, too.

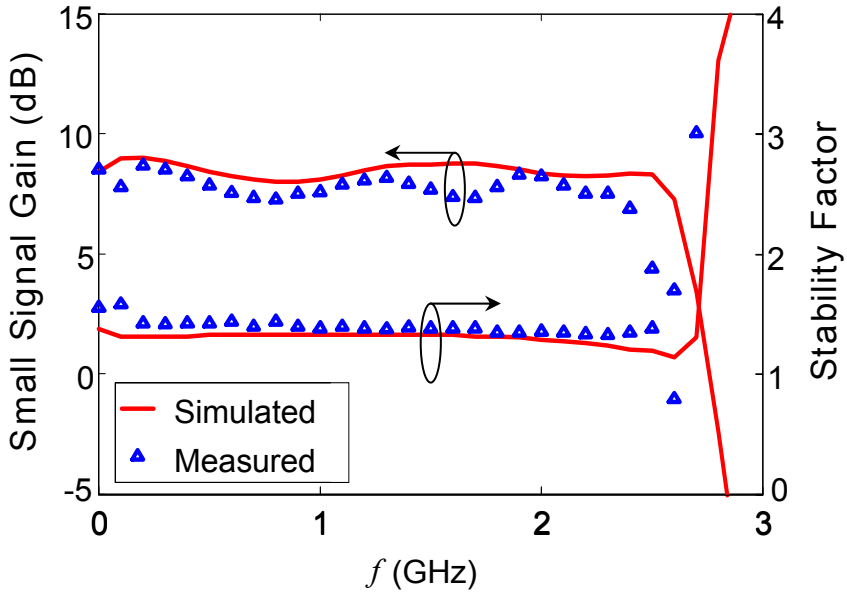


Figure 6.2. Simulated and measured gain and stability factor of the single stage PA.

Regarding the return loss diagram, a min output return loss of 7 dB can be achieved. However, poor (but acceptable) input matching in the frequency range (1.6 GHz…2.3 GHz) can also be observed.

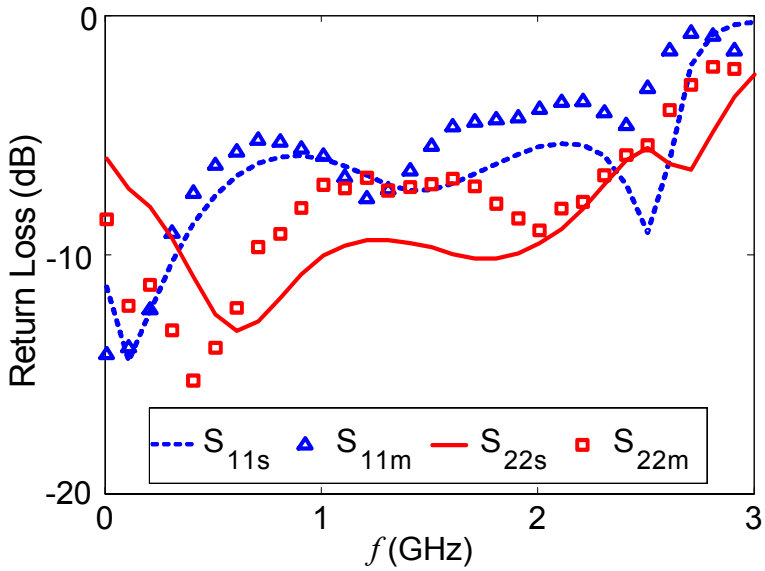


Figure 6.3. Simulated and measured return loss of the single stage PA.

### 6.1.2 5 W Wideband Two Stage PA

Small signal gain, stability factor and input and output reflection coefficients were measured using a network analyzer. Bias data were $V_{D1} = 10$ V, $I_{D1} = 350$ mA, $V_{D2} = 30$ V and $I_{D2} = 500$ mA, respectively. Figure 6.4 shows wideband characteristics from 10 MHz to 2.4 GHz with a small signal gain of 23 ± 1 dB and a stability factor K > 1.3.

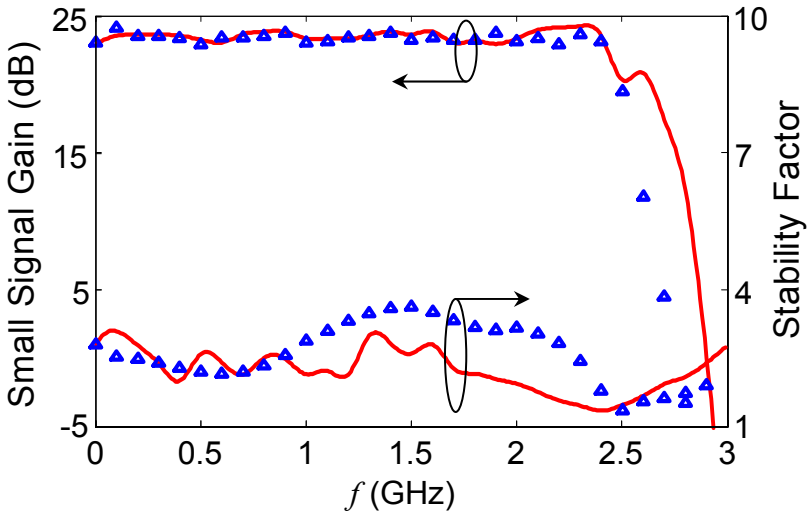


Figure 6.4. Simulated (solid lines) and measured (symbols) gain and stability factor of the two stage PA.

A very good agreement can be observed for the gain while the measured K-factor is considerably higher. The reasons for that are additional losses of microstrip lines; SMD-devices and the substrate implemented not precisely enough in the related

models. Figure 6.5 shows input and output return loss. In tendency, simulated and measured results match pretty well. The reason for the deviation of a few dB is the same as for the K-factor. While the output matching is very satisfactory, we will spend some work in the future to further improvement of the input matching.

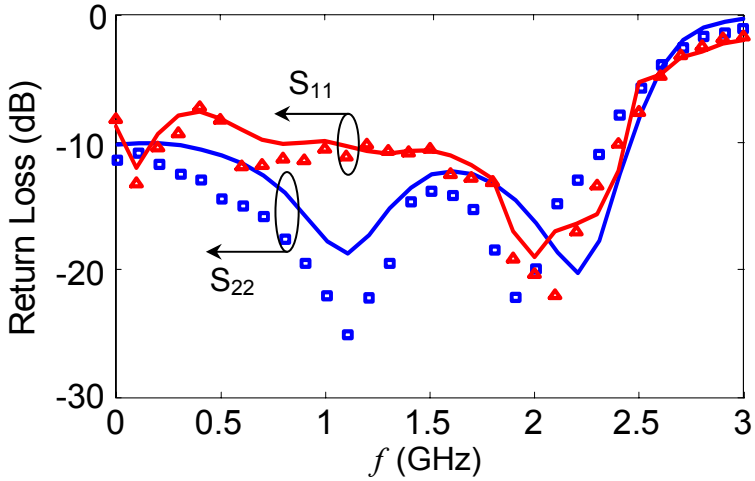


Figure 6.5. Simulated (solid lines) and measured (symbols) return loss of the two stage PA.

## 6.2 Power Performance

Harmonic balance simulation has been used to predict the output power ($P_{out}$), power gain ($G_P$), power added efficiency (PAE), and harmonic distortion of the implemented power amplifiers based on the derived model (see chapter 4). Power measurement setup as illustrated in figure 6.6 is based on the VNA as a measuring unit, an amplifier with high gain and sufficient output power as driver stage (Driver) to increase the power at the input of the device under test (DUT) since the driving power from VNA at port (P1) is not sufficient in most cases (especially for the single stage PA) to drive the DUT. Specifications of the driver amplifier used in our measurements are given in table 6.1.

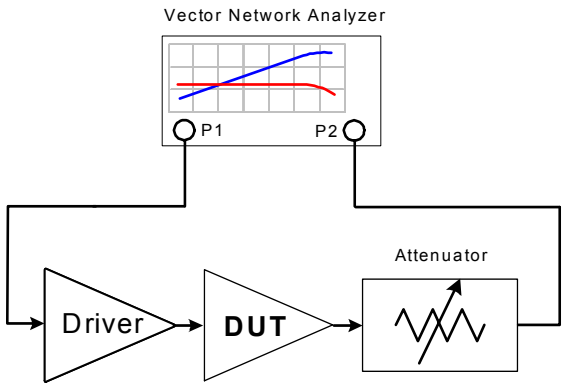


Figure 6.6. Power performance measurement setup.

| | |
|---|---|
| Operating Bandwidth | 10 MHz…4.1 GHz |
| Power Gain | 33 dB |
| Output Power | 30 dBm |
| Output $IP_3$ (OIP3) | 38 dBm |

Table 6.1. Specifications of the driver amplifier.

### 6.2.1 5 W Wideband Single Stage PA

The proposed model has been implemented as a user-defined model into the harmonic balance circuit simulator and small and large signal simulations were accomplished. Simulated output power, gain compression and power added efficiency of the SiC power stage based on the derived model have been compared to the measurements. Figure 6.7 shows the results at $f = 1$ GHz, $V_{DS} = 30$ V and $I_D = 500$ mA. A very good agreement concerning power gain and output power can be observed whereas the PAE curves show a slight difference.

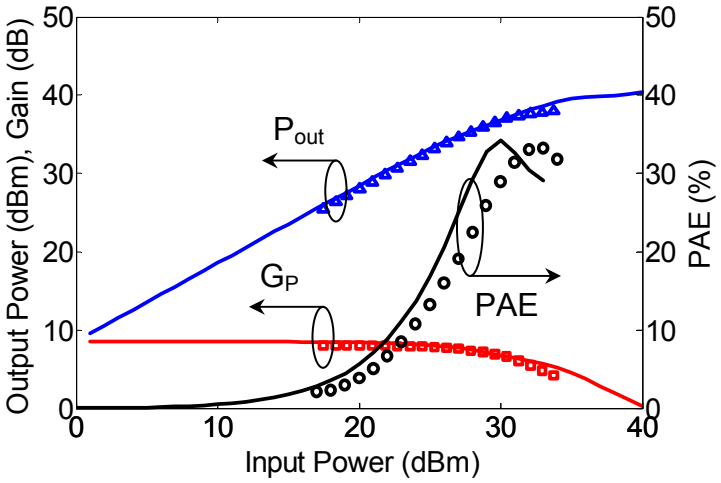


Figure 6.7. Measured (symbols) and simulated (solid lines) power performance of a single stage PA based on the derived model: $f = 1$ GHz, $V_{DS} = 30$ V, $I_D = 500$ mA.

The power performance process measurements have been done over the whole operating frequency range (10 MHz…2.4 GHz), and the output power and power gain have been extracted at the 1 dB compression point. Figure 6.8 shows the simulated (solid lines) and measured (symbols) extracted values of the output power ($P_{out}$), power gain ($G_P$), and the input power ($P_{in} = P_{out} - G_P$) versus frequency. It is obvious from the figure that min $P_{out}$ of 37 dBm, max PAE of 33 % and min $G_P$ of 7 dB have been obtained. With a very good agreement between simulations and measurements, only ± 1dB gain ripple also has been observed.

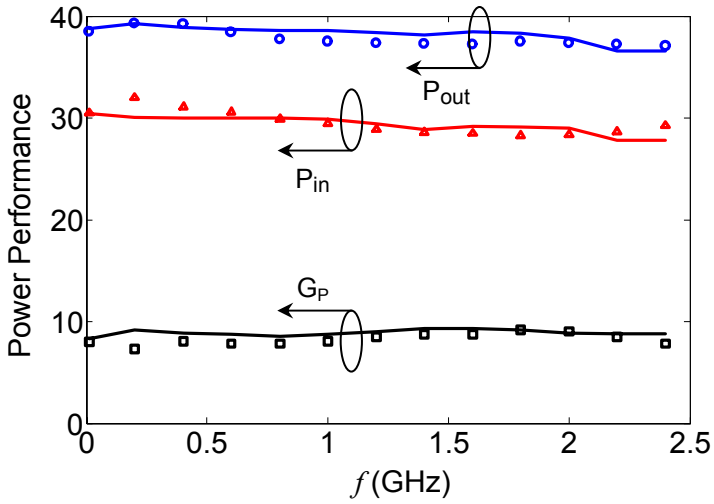


Figure 6.8. Simulated (solid lines) and measured power performances of the single stage PA over the operating frequency range: $V_{DS}$ = 30 V and $I_D$ = 500 mA.

### 6.2.2 5 W Wideband Two Stage PA

The power measurements were performed using a RF signal generator in conjunction with a microwave medium power amplifier as power source. Figure 6.9 shows output power, power gain and PAE versus input power at 1 GHz for the bias parameter $V_{D1}$ =10 V, $I_{D1}$ = 350 mA, $V_{D2}$ = 30 V and $I_{D2}$ = 500 mA. From the figure, an output power of at least 37 dBm, power gain of 22 ± 1 dB and PAE of 28 % at 1 dB power compression point can be taken.

PA performance versus frequency is finally depicted in figure 6.10. Up to 2.4 GHz, an output power and power gain of 37 dBm and 22 ± 1 dB ($P_{1dB}$), respectively were obtained. The required input power at $P_{1dB}$ is shown in figure 6.10, too.

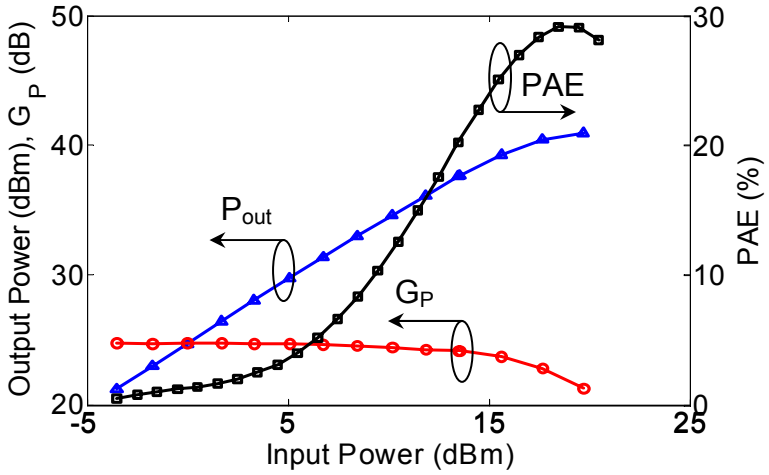


Figure 6.9. Measured power performance of the two stage PA at 1 GHz.

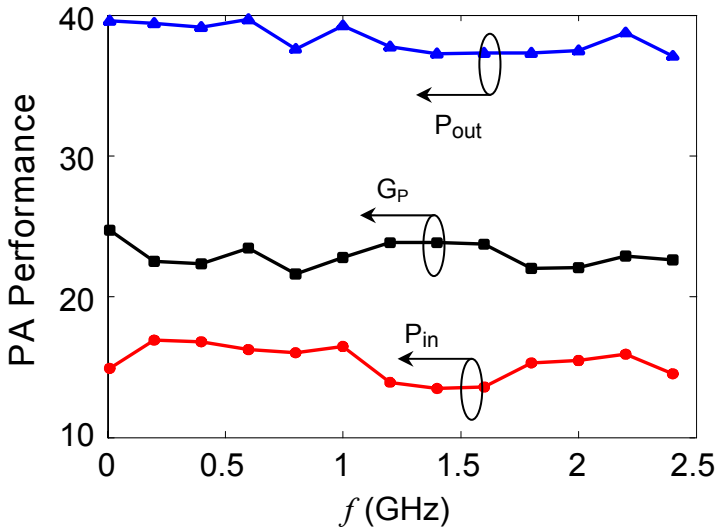


Figure 6.10. Measured power performance of the two stage PA over the operating frequency range: $V_{DS}$ = 30 V and $I_D$ = 500 mA.

### 6.2.3 5 W Ultra Wideband Single Stage PA Using SiC Chips

Harmonic balance simulations of an ultra wideband PA based on SiC chips has been performed. Figure 6.11 illustrates the circuit topology used in the power performance simulation. WB-symbol_using_chip in the schematic represents the circuit diagram given in chapter 5 (Figure 5.34).

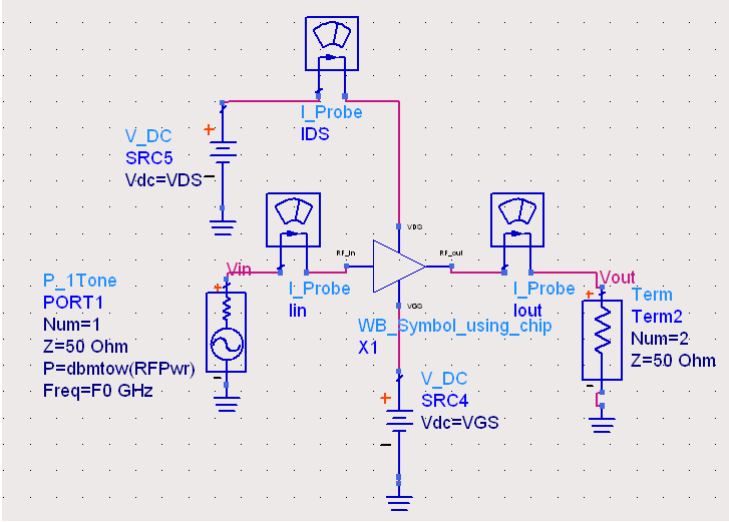


Figure 6.11. Schematic diagram of single-tone HB simulation.

At $f$ = 1 GHz, $V_{DS}$ = 30 V, $I_D$ = 500 mA, the power performance of the amplifier has been simulated. By sweeping the input power (from 0 dBm to 40 dBm), output power, power gain and power added efficiency can be calculated in terms of $V_{out}$, $I_{out}$, $I_D$ and $P_{in}$. Figure 6.12 shows the simulated power performance of the single stage PA

at $f$ = 1 GHz. An output power of 37.5 dBm, a power gain of about 5.5 dB at the 1 dB compression point and max PAE of 30 % have been obtained.

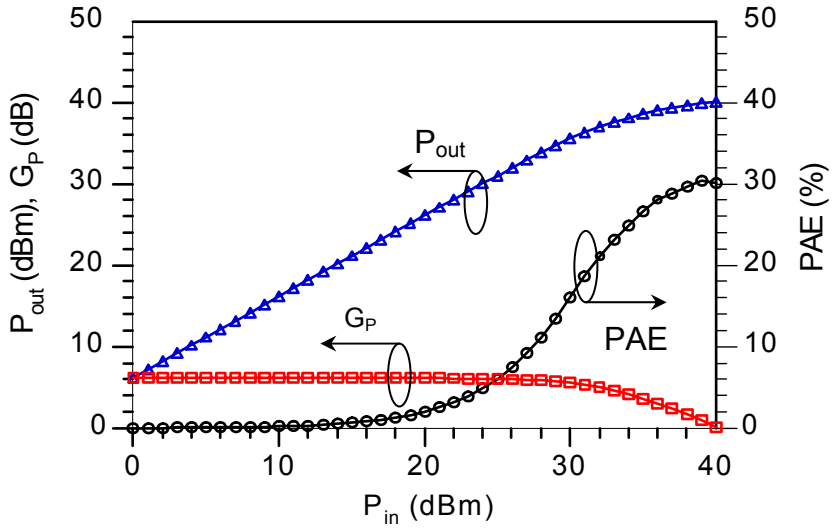


Figure 6.12. Simulated power performance of the ultra wideband single stage PA at 1 GHz.

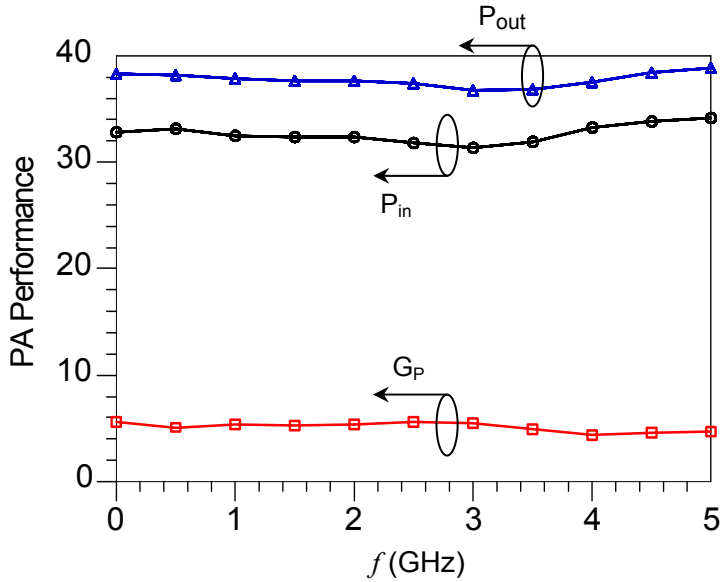


Figure 6.13. Simulated power performance of the ultra wideband single stage PA over the operating frequency range: $V_{DS}$ = 30 V and $I_D$ = 500 mA.

Power performance of the ultra wideband PA has been simulated over the entire bandwidth and output power and power gain at the 1 dB compression point have been extracted. Figure 6.13 illustrates the extracted output power, power gain and input power ($P_{out}$ - $G_P$). From the figure, an excellent broadband power performance can be observed. Output power of at least 37 dBm and power gain of 5.5 ± 1 dB can be obtained.

### 6.2.4 5 W Ultra Wideband Two Stage PA Using SiC Chips

In this section, we present the power performance of a two stage PA based on SiC chips. The simulated small signal performance of the implemented amplifier has been introduced in chapter 5, however HB simulation will be done based on the schematic diagram shown in figure 6.14.

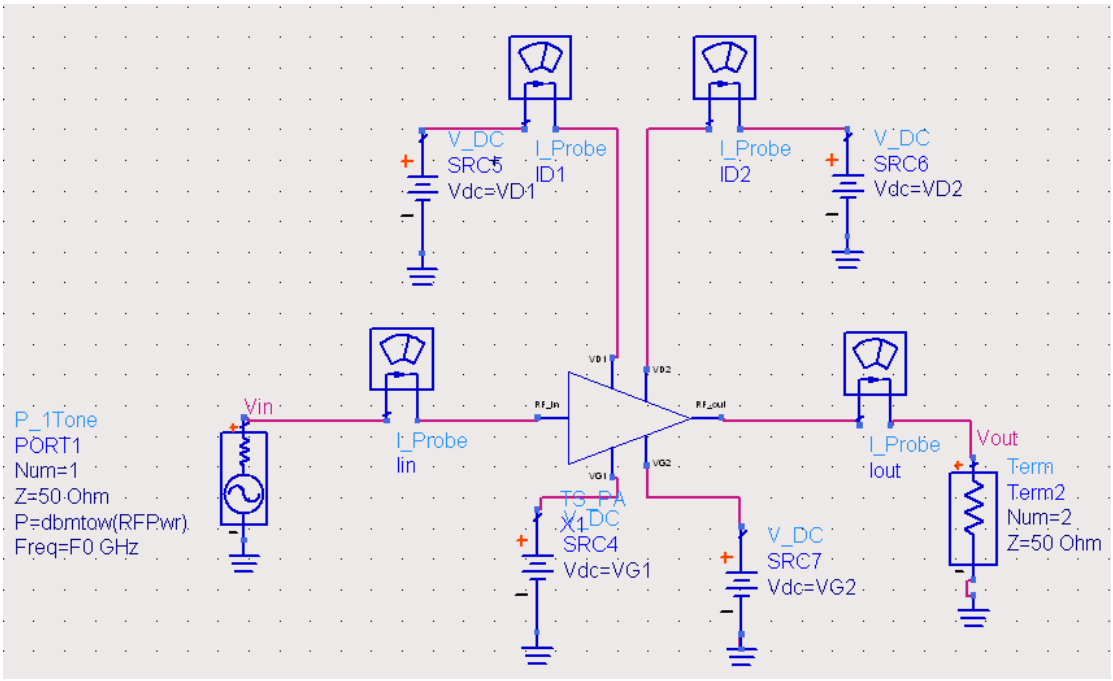


Figure 6.14. Schematic diagram of single-tone HB simulation for the ultra WB two stage PA.

Regarding the diagram, a user defined symbol is used instead of the circuit diagram given in chapter 5 (Figure 5.36). With a two stage PA, it is expected that high gain can be achieved, however the PAE will be reduced because of the (DC) dissipated power in the driver stage. Output power and power gain will be calculated in the same manner as in the previous example based on $V_{out}$, $V_{D2}$ and $I_{out}$ while PAE can be determined in this case from the following equation

$$PAE = \frac{P_{out} - P_{in}}{(V_{D1} I_{D1} + V_{D2} I_{D2})} \tag{6.1}$$

At $V_{D1}$ = 10 V, $I_{D1}$ = 350 mA, $V_{D2}$ = 30 V and $I_{D2}$ = 500 mA, the input power has been swept at $f$ = 1 GHz, output power, power gain and PAE have been extracted. Figure 6.15 shows the power performance of the ultra wideband two stage PA. Adding the driver stage increases the 1 dB power gain to 17.5 dB compared to 5.5 dB in case of the single stage PA. The impact of the driver stage on the PAE of the two

stage PA is also observed. Referring to max PAE of 30 % in case of the single stage PA, the max PAE of the two stage PA has been reduced to about 25 %. Impact of the driver stage on the linearity performance will also be discussed in the next section.

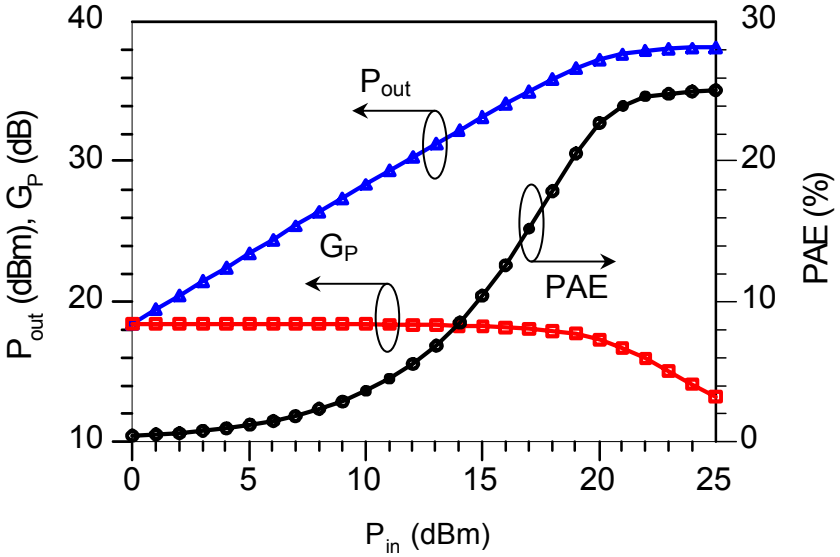


Figure 6.15. Simulated power performance of ultra WB two stage PA at 1 GHz.

### 6.2.5 10 W High Gain Single Stage PA Using SiC Chips

In the frequency range (3.1 GHz…3.5 GHz), a high power single stage PA has been designed based on SiC chips. Design details and small signal performance of this amplifier are given in chapter 5. Figure 6.16 illustrates the simulated output power, power gain and PAE as a function of the input power at $f$ = 3.3 GHz.

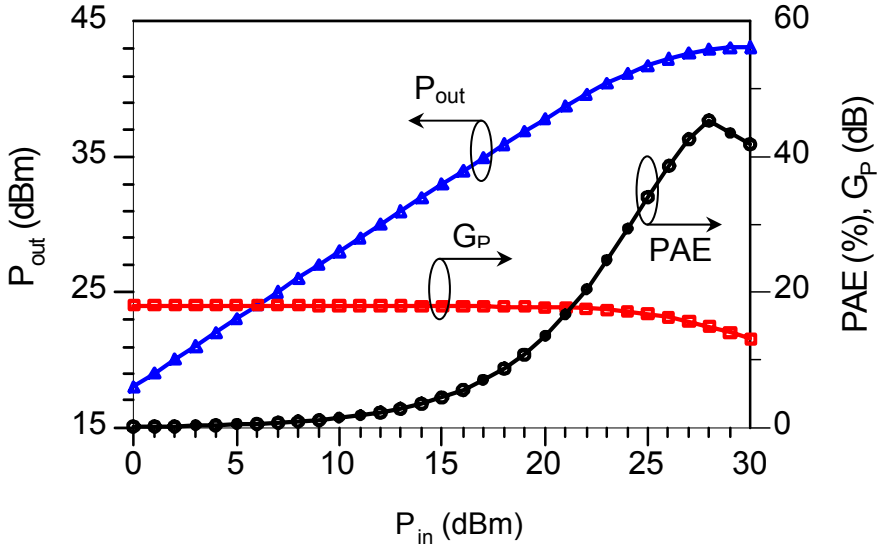


Figure 6.16. Simulated power performance of the 10 W high gain single stage PA at 3.3 GHz.

An 1 dB input compression point of 25 dBm, power gain of 16 dB and output power of 41 dBm can be obtained. The figure shows that a max PAE of 45 % compared to 30 % in case of the 5 W single stage PA.

## 6.3 Linearity Performance

Traditional intermodulation distortion (IMD) measurements that use two identical signal generators, two identical driver amplifiers in order to obtain the same power at the input of the power amplifier to be measured (DUT) through a very good directional coupler is considered too difficult to construct resulting in a lot of errors that make the linearity measurements inaccurate. A new simple and accurate measurement setup based on an enhanced multitone signal generator (ESG) and a power spectrum analyzer (PSA) from Agilent together with an intelligent enhanced multitone studio based predistortion technique is considered.

The measurement setup used in this case is shown in figure 6.17. The Signal Studio for Enhanced Multitone software by Agilent is used to correct the nonlinearity caused by ESG internal amplifiers, driver and low pass filter, using a predistortion technique. A PC is connected to the measurement setup during the correction process. An enhanced signal generator (ESG) is used to generate multitone signals that may be more accurate compared to the traditional systems used in IMD measurements.

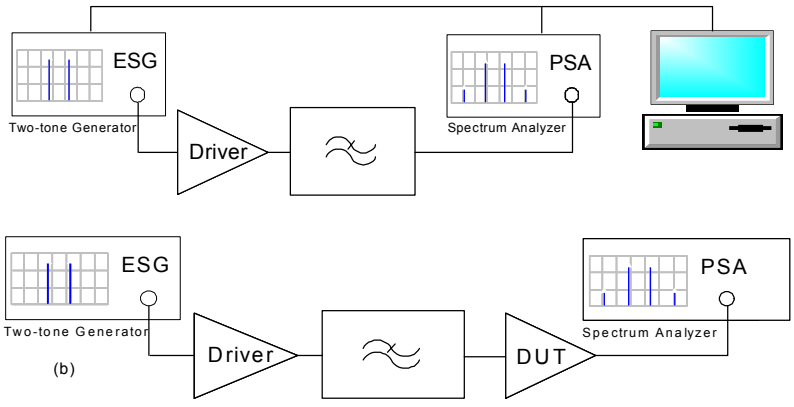


Figure 6.17. Two-tone measurement setup based on the Agilent Mulitone Studio:
a) IMD cancellation b) IMD measurements of DUT.

### 6.3.1 5 W Wideband Single Stage PA

AM-AM and AM-PM conversions are usually used to model the nonlinearity of an amplifier. These conversions model the amplitude and phase of the fundamental signal with increasing amplitude, and therefore nonlinearities are characterized as changes in the fundamental signal [58]. These additional characterizations can give a more accurate representation of nonlinear distortions in an amplifier. AM-AM distortion is created by variation of the amplifier gain as a function of input power while AM-PM distortion is defined as the change of the phase between the input and output signals with varying input power. Figure 6.18 shows the measured and simulated AM-AM and AM-PM conversions of a single stage PA at 1 GHz. The AM-AM and AM-PM measured performances are quite good with a maximum deviation of only 0.3 (dB/dB) and 0.25 (deg/dB), respectively at the fundamental gain compression (AM-AM). Good matching between measurements and simulations can be achieved.

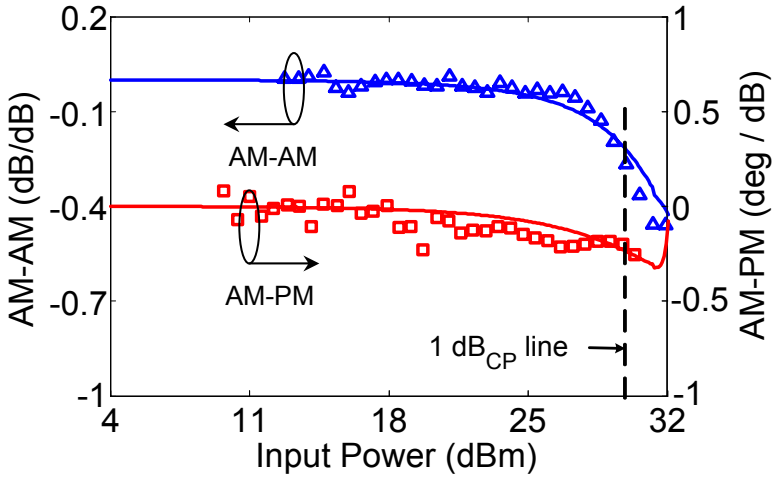


Figure 6.18. AM-AM and AM-PM response of single-stage PAs at $f$ = 2 GHz: measurements ⟶ (symbols) and simulations ⟶ (solid lines).

Measured and simulated AM-AM and AM-PM distortions have been extracted over the entire bandwidth and depicted in figure 6.19 at 1 dB$_{CP}$. The figure shows a very satisfying agreement between measurements and model based simulations with only a few percent deviation. Very low values for AM-AM and AM-PM distortions of 0.45 (dB/dB) and 0.75 (deg/dB), respectively have been achieved over the full band at 1 dB$_{CP}$.

Linearity has also been characterized performing two-tone intercept point measurements. Two closely spaced input tones of equal amplitude were applied to the

amplifier at $f$ and $f + \Delta$, respectively where $\Delta$ is the frequency spacing between the two tones. The fundamental, second and third order components were determined using a spectrum analyzer as a function of input power. An enhanced multi-tone signal generator (Agilent-ESG) was used to provide the two tone signal at $f = 1$ GHz with frequency spacing $\Delta = 200$ kHz and $P_{in} = 16$ dBm. The output amplitude spectrum was taken from the spectrum analyzer (Agilent PSA) as shown in figure 6.20.

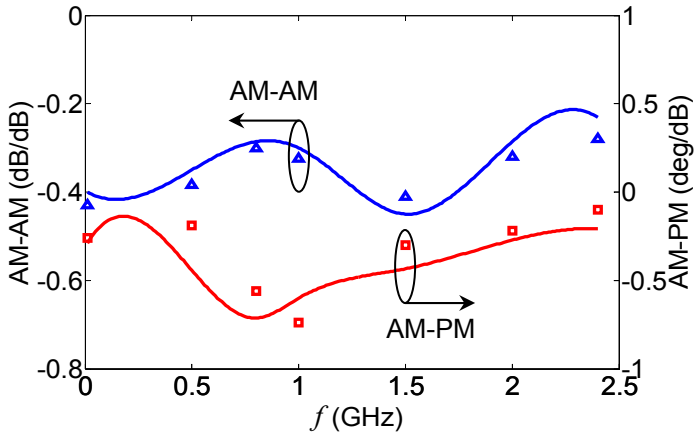


Figure 6.19. Measured (symbols) and modeled (solid lines) AM-AM and AM-PM response of the SiC power stage versus frequency: $V_{DS} = 30$ V, $I_D = 500$ mA.

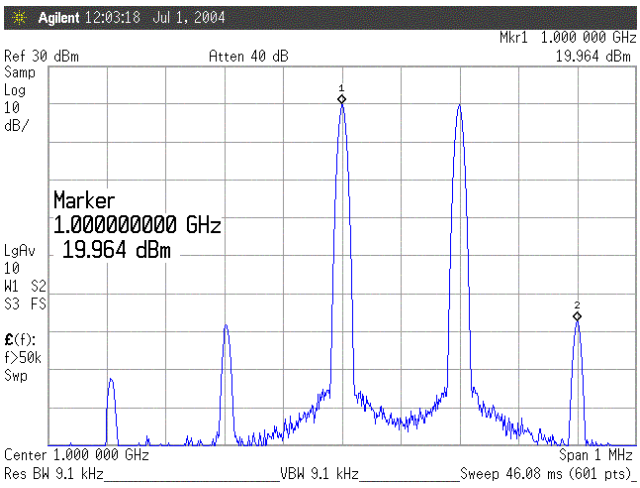


Figure 6.20. Two-tone measurement of the wideband single stage PA at $P_{in} = 0$ dBm, $f = 1$ GHz and $\Delta = 200$ kHz.

An input power sweep was applied and the output second and third order intercept point (OIP2 & OIP3) were finally calculated using the equation

$$OIPn = P_{out} + (\text{Harmonic Suppression}) / (n-1) \qquad (6.2)$$

where *n* is the order of the harmonic. Figure 6.21 shows the fundamental, second and third order harmonics as a function of the input power. The diagram shows that an OIP2 and OIP3 of 71 dBm and 51 dBm, respectively, have been achieved. Bias parameters were $V_{DS} = 30$ V, $I_D = 500$ mA. The extracted second and third order intercept points at different frequencies are presented in figure. 6.22. Over the entire bandwidth, an OIP2 > 70 dBm and an OIP3 > 49 dBm have been achieved.

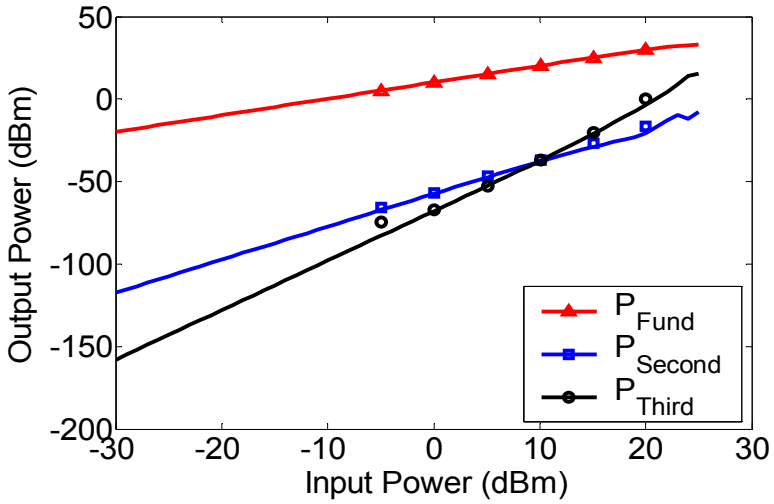


Figure 6.21. Two-tone measurements (symbols) and simulations (solid lines) of the single stage PA at 1 GHz, Δ = 200 kHz.

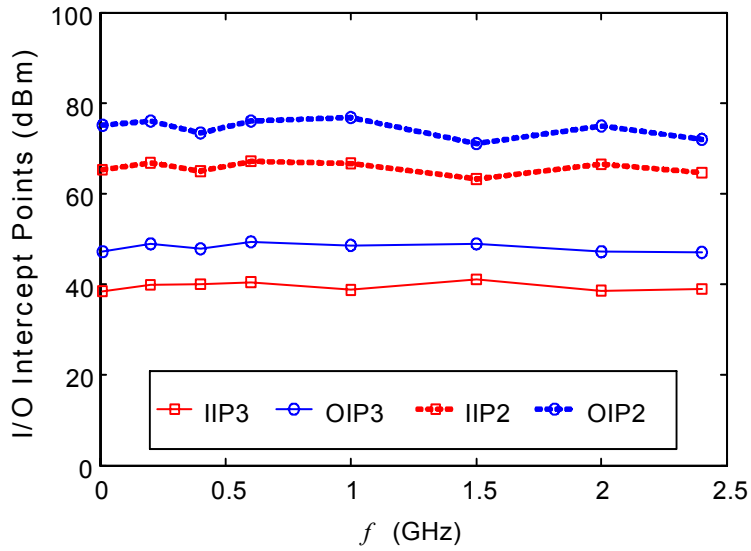


Figure 6.22. Extrapolated input and output intercept points of the wideband single stage PA at $V_{DS}$ = 30 V and $I_D$ = 500 mA.

## 6.3.2 5 W Wideband Two Stage PA

Additional amplifier characterizations can give a more accurate representation of nonlinear distortions in an amplifier. Figure 6.23 shows both amplitude and phase

characteristics at 2 GHz. The amplifier shows very low AM-AM and AM-PM values of max. 0.1 (dB/dB) and 0.23 (deg/dB) at $f = 2$ GHz. Regarding the power stage diagram in figure 6.18, impact of the driver can be noticed. Adding or subtracting the driver harmonics as a vector results in increasing or decreasing the overall AM-AM and AM-PM distortions.

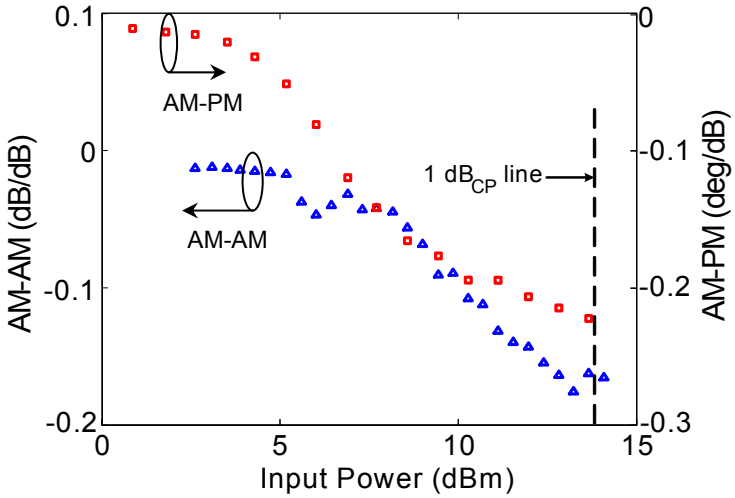


Figure 6.23. AM-AM (triangles) and AM-PM (squares) response of two-stage PA at $f = 2$ GHz.

Broadband single tone performance using AM-AM and AM-PM conversions as measure of PA linearity can be also achieved. The extracted values of these conversions have been done at 1 dB$_{CP}$. Figure 6.24 shows both amplitude and phase characteristics at 1 dB$_{CP}$ versus frequency.

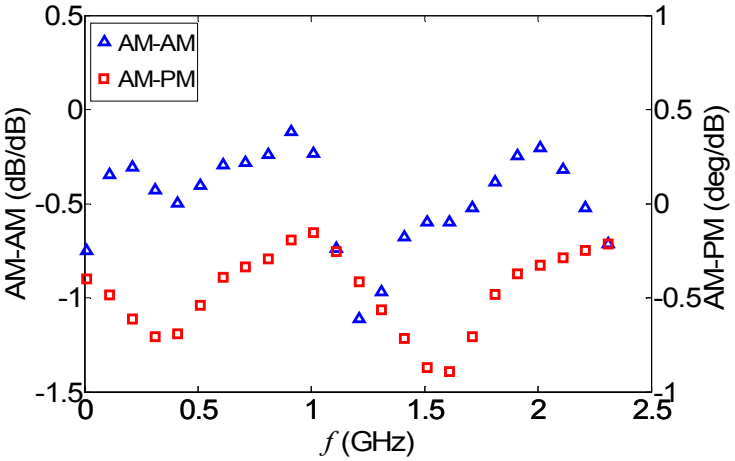


Figure 6.24. Measured AM-AM (triangles) and AM-PM (squares) conversions of the two stage PA versus frequency.

The two stage design exhibits AM-AM and AM-PM values of up to -1.2 (dB/dB) and -1 (deg/dB) over the full bandwidth. Both values are about twice the amount of

the power stage alone and are from that point of view acceptable. Although these values are pretty low, too, they could be improved by a larger driver FET.

Two-tone measurements have also been used to predict the linearity performance of the two stage PA. The measurements have been done at $V_{D1}$ =10 V, $I_{D1}$ =350 mA, $V_{D2}$ = 30 V,$I_{D2}$ =500 mA, and a tone spacing of 200 kHz. Figure 6.25 shows the amplitude spectrum of the implemented amplifier on the PSA at $f$ = 1 GHz and $P_{in}$ = 0 dBm. It is observed from the figure that an IMD of about 55 dBc can be obtained, resulting in an OIP3 of about 48 dBm.

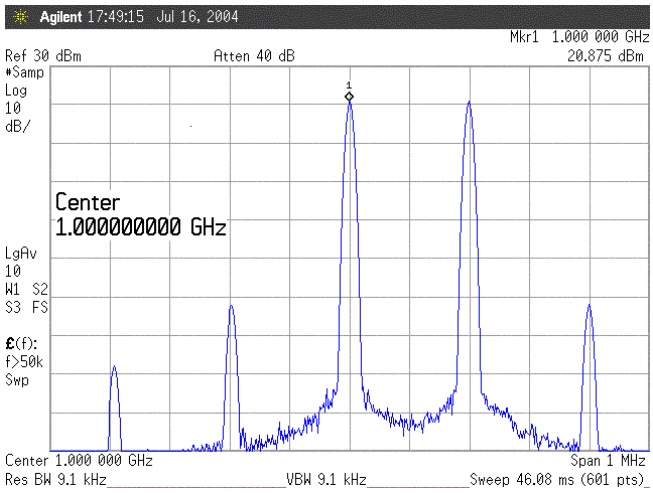


Figure 6.25. Two-tone measurement of the two stage PA at Pin = 0 dBm, $f$ = 1 GHz and $\Delta$ = 200 kHz.

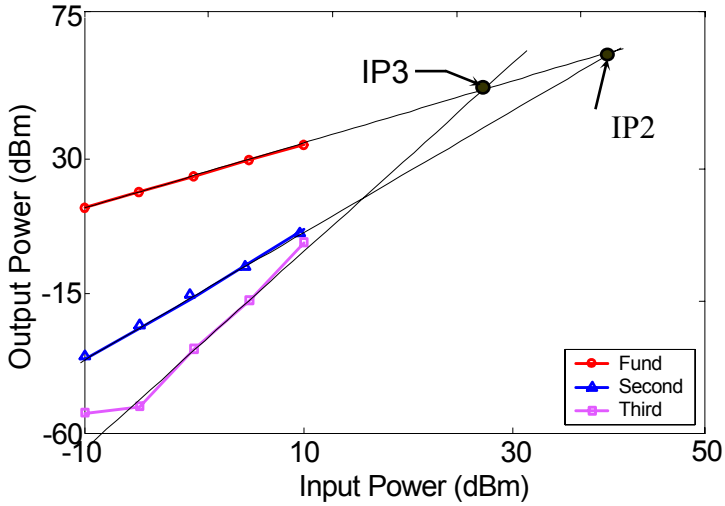


Figure 6.26. Two-tone measurements of two stage PA at 1 GHz, $\Delta$ = 200 kHz.

Geometrically, the intercept point can be obtained by extrapolating two lines with different slopes as indicated in figure 6.26. At various input power levels, first, second

and third-order harmonics have been measured and their values have been depicted versus the swept input power as shown in the figure.

The intercept point of the first- and second-order harmonics represents the second-order intercept point while the third-order intercept point is given by the intersection of both the first- and third-order harmonics. From the diagram, an OIP2 of 62 dBm and an OIP3 of 48 dBm have been achieved.

Over the entire frequency band, two-tone test of the designed PA at the same bias point and the same tone spacing of 200 kHz has been done. Figure 6.27 illustrates the extracted output intercept points in the frequency range from 10 MHz to 2.4 GHz. An OIP3 of at least 47 dBm and an OIP2 of at least 61 dBm can be achieved. It is observed when comparing the results of both the single stage and the two stage PA that the driver stage also plays an important rule in degrading the linearity of the amplifier.

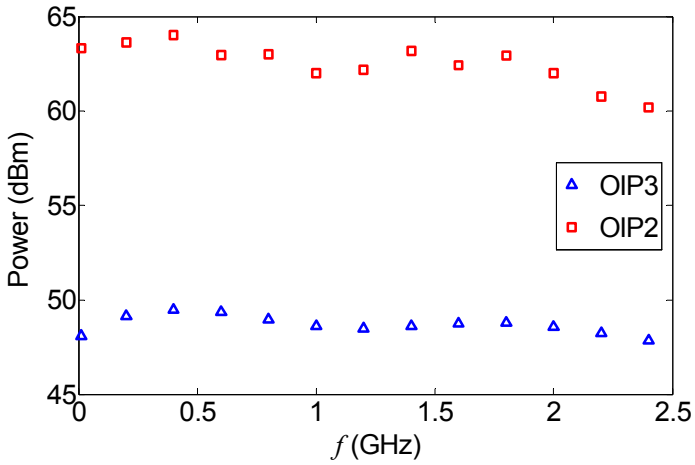


Figure 6.27. Extracted output intercept points of the wideband two stage PA: $V_{D1}$ = 10 V, $I_{D1}$ = 350 mA $V_{D2}$ = 30 V and $I_{D2}$ = 500 mA.

### 6.3.3 5 W Ultra Wideband Single Stage PA Using SiC Chips

In this section, single tone measurements have been performed at $f$ = 1GHz and AM-AM and AM-PM conversions of an ultra wideband single stage PA have been extracted. Figure 6.28 shows the AM-AM and AM-PM distortions versus input power at $V_{DS}$ =30 V and $I_D$ = 500 mA. Max AM-AM and AM-PM distortions of 0.25 (dB/dB) and 0.75 (deg/dB), respectively have been occurred at the fundamental gain compression.

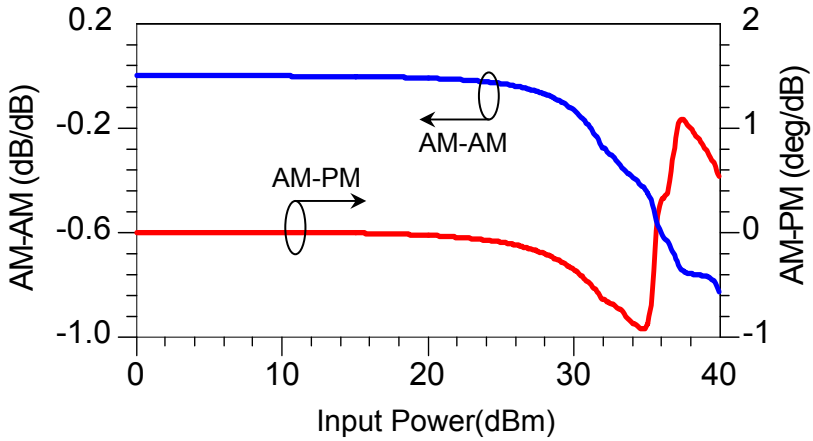


Figure 6.28. Amplitude and phase conversions of the ultra WB single stage PA at $f = 1$ GHz.

Two-tone measurements of an ultra wideband single stage PA have been implemented. Referring to figure 6.11, the single-tone generator has been replaced by a two-tone signal generator. IMD performances have been accomplished at $f = 1$ GHz with tone spacing $\Delta = 200$ kHz. At $V_{DS} = 30$ V and $I_D = 500$ mA, first, second and third harmonics have been extracted as a function of the swept input power as shown in figure 6.29. Extrapolated OIP2 and OIP3 of 68 dBm and 53 dBm respectively can be achieved.

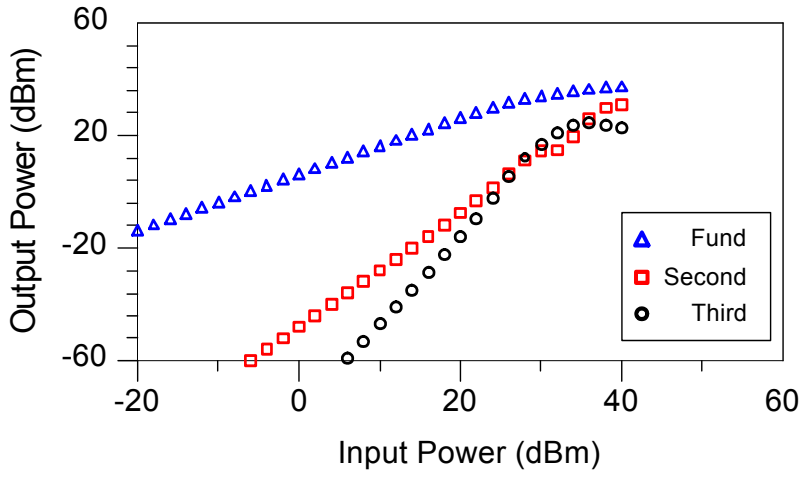


Figure 6.29. Simulated two-tone performance of the ultra WB single stage PA at $f = 1$ GHz and $\Delta = 200$ kHz.

The two-tone performance of the implemented amplifier has been repeated at various frequencies that cover the range from 1 MHz to 5 GHz and second-order and third-order intercept points at the input and the output have been extracted. Figure 6.30 indicates the extracted input and output intercept points versus frequency. The figure shows that a min OIP2 of 64 dBm and a min OIP3 of 51 dBm.

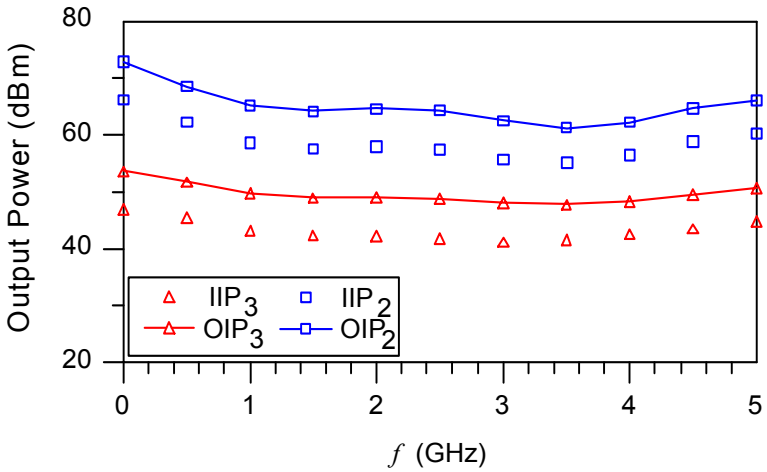


Figure 6.30. Extracted input and output intercept points of the ultra WB single stage PA: $V_{DS}$ = 30 V and $I_D$ = 500 mA.

### 6.3.4 5 W Ultra Wideband Two Stage PA Using SiC Chips

The impact of the driver stage can be observed when simulating the single tone measurements. Transmission amplitude and phase variations with respect to the swept input power are illustrated in figure 6.31. Referring to the AM-PM diagram of the ultra wideband single stage PA (Figure 6.28), the AM-PM conversion of the two stage PA has been increased to 3 (deg/dB) at 1 dB gain compression which reflects the impact of the driver stage on the amplifier performance.

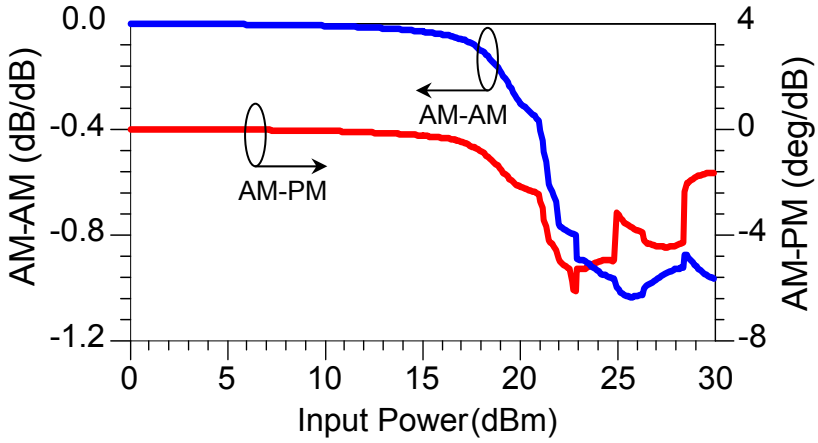


Figure 6.31. AM-AM and AM-PM conversions of the ultra WB two stage PA at 1 GHz.

Two-tone measurements of the ultra wideband two stage PA have also been performed. Comparing to the ultra wideband single stage PA, the impact of the driver stage can be observed. At the same operating point ($f$ = 1 GHz and $\Delta$ = 200 kHz), the input power has been swept and first-, second- and third-order harmonics have been extracted. Figure 6.32 indicates the resulting two-tone performance of the

implemented amplifier. Second- and third-order intercept points can be geometrically extrapolated as the intersections of first-order, second-order and the first-order and third-order harmonics, respectively. OIP2 and OIP3 of 62 dBm and 48 dBm respectively can be obtained.

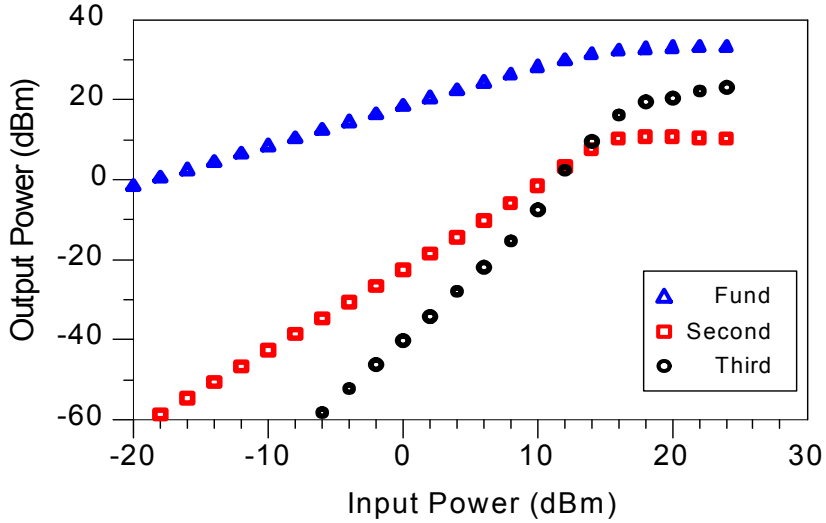


Figure 6.32. Two-tone performance of the ultra WB two stage PA: $f$ = 1 GHz and $\Delta$ = 200 kHz.

### 6.3.5 10 W Narrow Band Single Stage PA Using SiC Chips

In this section, single- and two-tone measurements of a high power single stage PA have been performed. The single-tone harmonic distortion can be measured by means of AM-AM and AM-PM conversions while the intermodulation distortions can be measured by means of the harmonic intercept points. AM-AM and AM-PM distortions of the implemented amplifier have been simulated using HB from ADS and are shown in figure 6.33.

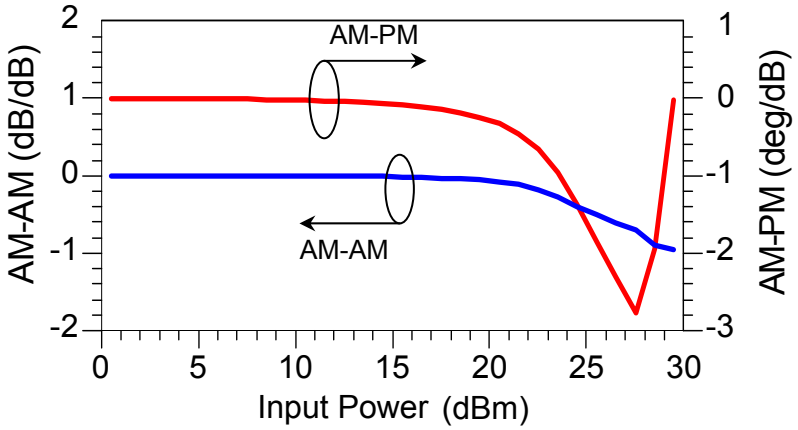


Figure 6.33. AM-AM and AM-PM conversions of the 10 W high gain single stage PA at 1 GHz.

From the figure, the single-tone linearity performance can be measured at the fundamental gain compression (AM-AM) and it has been observed that max phase distortion of 0.2 (deg/dB) can be done. Two-tone measurements have been performed at $f = 1$ GHz with a tone spacing of 200 kHz. By sweeping the input power, fundamental, second- and third-order harmonics have been simulated. Figure 6.34 illustrates the output harmonics versus the input power. Extrapolated OIP2 and OIP3 of 71 dBm and 50 dBm, respectively, can be obtained.

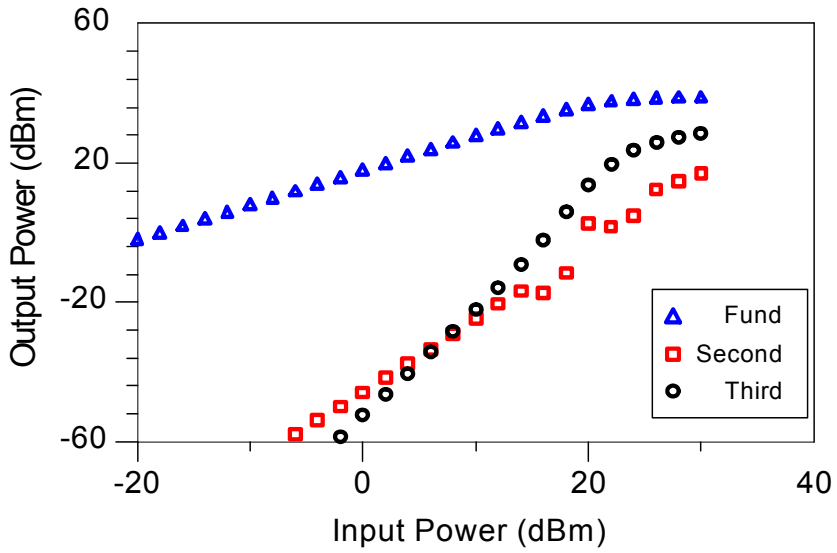


Figure 6.34. Two-tone performance of the 10 W high gain single stage PA at $f = 3.3$ GHz and $\Delta = 200$ kHz.

# CONCLUSION

In this thesis, features of wide bandgap materials that provide high RF power density, excellent PAE performance, high break down voltage, and high frequency operation have been used to implement broadband power amplifiers. An accurate model for SiC MESFET has been developed. A novel systematic procedure has been used to extract the extrinsic model parameters based on Cold-FET measurements. The intrinsic model elements have been extracted from S-parameter measurements at various bias conditions.

A large signal table-based model for SiC MESFET based on Angelov's formulation has been developed. Dispersions in the transconductance and output conductance were interpreted. The new model has been implemented as a user-defined model in the harmonic balance circuit simulator ADS. The model has been verified by comparing its power and linearity performance with Cree's model based on this transistor and they were found very close to each other.

Based on the derived model, five different generations of power amplifiers have been implemented. In the first generation, a 5 watt wideband single stage power amplifier using a SiC MESFET has been designed. The frequency range covers 10 MHz to 2.4 GHz with a small-signal gain of $8 \pm 1$ dB. A broadband choke structure with a new technique was developed to obtain good isolation and low loss over the desired bandwidth. Input and output matching networks and shunt feedback topology were introduced to increase the bandwidth. At $V_{DS} = 30$ V and $I_D = 500$ mA, power performance measurements with PAE of almost 33%, an output power of $\geq$ 37 dBm and 7 dB power gain over the operating bandwidth were achieved. Two-tone measurements at frequency spacing of 200 kHz were also done and OIP2 and OIP3 of 70 dBm and 49 dBm, respectively, were obtained. AM-AM and AM-PM distortions were also measured and the results are discussed.

In the second generation, a 5 W two stage wideband RF power amplifier has been designed using a SiC MESFET power stage, covering the frequency range from 10 MHz to 2.4 GHz. $\pm$ 1 dB gain flatness has been achieved over the bandwidth by

combining feedback and matching circuits properly. Small signal S-parameters, power performance, and intermodulation characteristics were measured. Impact of the driver stage based on a GaAs MESFET on the overall amplifier performance has been presented and discussed. Compared to the single stage PA, a higher gain of 22 ± 1 dB and a lower PAE of 28 % can be observed for the two stage PA. The linearity performance of the two stage PA has been presented, too. An OIP3 of 47 dBm can be achieved compared to 52 dBm from the single stage PA. The two stage design exhibits AM-AM and AM-PM values of up to -2 (dB/dB) and -1 (deg/dB) over the full bandwidth. Both values are about twice the amount of the power stage alone and are from that point of view acceptable. Although these values are pretty low, too, they could be improved by a larger driver FET.

An ultra wideband 5-W single stage PA based on SiC MESFET Die has been developed in the third generation. The simulated amplifier covers the frequency bands from 1 MHz to 5 GHz. Small signal and harmonic balance simulations based on ADS have been accomplished. An output power of 37 dBm, power gain of 5.5 dB and PAE of 30 % have been obtained. AM-AM and AM-PM conversions as a single-tone measurement have also been simulated and 0.75 deg/dB of AM-PM distortion at the fundamental compression has been found. Two-tone test with a tone spacing of 200 kHz has also been performed and the minimum values of OIP2 and OIP3 have been found to be 68 dBm and 53 dBm, respectively.

An extension of the third generation concerning the power gain improvement has also been demonstrated in the fourth one. An ultra wideband 5-W two stage PA has been simulated. The driver stage is based on a GaAs FET Die from Excellics, while a SiC MESFET Die has been used in the power stage. Input, output, interstage and feedback networks based on microstrip technique have been designed. Small signal as well as large signal performance have been simulated. Small signal gain of 17.5 dB, input and output return losses of 5 dB and 8 dB, respectively, over the frequency band from 1 MHz to 5 GHz have been achieved. Impact of the driver stage on the power and linearity performance of the amplifier has also been discussed. Compared to the single stage PA performance, a higher power gain of 17 dB, a lower PAE of 25 % in the power performance of the two stage PA can be achieved. Amplitude and phase distortion of the implemented amplifier have been demonstrated at 1 GHz. Although an AM-PM of 3 deg/dB has been found at the gain compression point, the

implemented two stage amplifier still has low sensitive distortion. At 1 GHz, two-tone test with a tone spacing of 200 kHz has been simulated, resulting in OIP2 and OIP3 of 64 dBm and 51 dBm, respectively. Regarding the third generation linearity performance, the impact of the driver stage on the amplifier performance can be observed.

The fifth and final generation of the simulated power amplifiers in this work is a 10 W, high gain single stage PA based on a SiC MESFET Die. In this case, feedback compensation technique using a transformer has been used to eliminate the reactance of the gate-drain capacitance, resulting in a high gain of $16 \pm 0.5$ dB over the frequency range (3.1 GHz…3.5 GHz). Input and output matching networks have been designed for maximum gain and maximum output power. Return losses of 9 dB and 12 dB at the input and output, respectively, have been achieved. Power and linearity performances of the simulated amplifier have been simulated with ADS harmonic balance. An output power of 40 dBm, power gain of 16 dB, PAE of 45 % at 3.3 GHz have been obtained. At 3.3 GHz, single-tone and two-tone tests have been also simulated. AM-AM and AM-PM conversions of 0.2 dB/dB and 0.2 deg/dB, respectively at the fundamental gain compression has been found. With a tone spacing of 200 kHz, the extrapolated OIP2 and OIP3 values were found to be 71 dBm and 50 dBm, respectively.

From the presented work, the SiC MESFET technology appears to be very suitable for power applications up to the lower GHz range. The last three generations of the implemented amplifiers will be improved and fabricated in the near future.

# APPENDIX A

# INTERMODULATION DISTORTION ANALYSIS

In the two-tone test, the input test signal consists of two sinusoids with frequencies closely spaced in the band of interest as shown in (A.1)

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \tag{A.1}$$

If an amplifier exhibits a nonlinear transfer characteristic and is excited with a two-tone signal (A.1), the output signal will contain second, third and higher order harmonics and intermodulation products. The output signal y(t) then is

$$\begin{aligned} y(t) &= c_1 x(t) + c_2 x^2(t) + c_3 x^3(t) + \ldots \\ &= c_1 \left(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)\right) + c_2 \left(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)\right)^2 + c_3 \left(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)\right)^3 + \ldots \end{aligned} \tag{A.2}$$

A second effect of nonlinearity on RF PAs is the intermodulation. In intermodulation, a nonlinear circuit excited with two input sinusoids results in an output, containing components at new frequencies. In the general case, these new frequencies will be of the form as described in equation (A.3).

$$\omega = \pm m\omega_1 \pm n\omega_2 \tag{A.3}$$

In equation (A.3), ω is the new frequency; $\omega_1$ and $\omega_2$ are the original frequencies in radians per second ($\omega = 2\pi f$). *m* and *n* are positive integers including zero. $m + n$ is equal to the order of distortion.

Not all newly created frequencies belong to the group of intermodulation products. Intermodulation products are the result of the interaction of fundamentals and harmonics of different order. Harmonics are typically not referred to as intermodulation products. Intermodulation products arise from the $x^2(t)$, $x^3(t)$ and higher order terms of the power series expansion. Products created by the $x^2(t)$ term are second order products and products created by the term $x^3(t)$ are third order

products. Returning to the two-tone input signal of Eq. (A.1), it can be seen from the full expansion of (A.2) that the following intermodulation products appear:

Second order intermodulation products:

$$c_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + c_2 A_1 A_2 \cos(\omega_1 - \omega_2)t \tag{A.4}$$

For $A_1=A_2$, term (A.4) changes to term (A.5):

$$c_2 A_1^2 \cos(\omega_1 + \omega_2)t + c_2 A_1^2 \cos(\omega_1 - \omega_2)t \tag{A.5}$$

In Eqs (A.4) and (A.5), $A_1$ and $A_2$ are the amplitudes of the two-tone input signal and $c_2$ is the second order coefficient. $\omega_1$ and $\omega_2$ are the fundamental frequencies in radians per second.

Third order intermodulation products:

$$\begin{aligned}&\frac{3}{4}c_3 A_1^2 A_2 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}c_3 A_1^2 A_2 \cos(2\omega_1 - \omega_2)t + \\ &\frac{3}{4}c_3 A_1 A_2^2 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}c_3 A_1 A_2^2 \cos(2\omega_1 - \omega_2)t\end{aligned} \tag{A.6}$$

Again, for $A_1=A_2$, Eq (A.6) takes the following form

$$\begin{aligned}&\frac{3}{4}c_3 A_1^3 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}c_3 A_1^3 \cos(2\omega_1 - \omega_2)t + \\ &\frac{3}{4}c_3 A_1^3 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}c_3 A_1^3 \cos(2\omega_1 - \omega_2)t\end{aligned} \tag{A.7}$$

In terms (A.7), $A_1$ and $A_2$ are the amplitudes, $c_3$ is the third order coefficient of the power series, and $\omega_1$ and $\omega_2$ are the two input frequencies in radians per second. In Eqs. (A.5) to (A.7) harmonics are not considered.

Eq (A.7) indicates that as input amplitude $A_1$ increases by a factor of two, the third order intermodulation product goes up by a factor of eight due to the exponent of value three in the terms $3 c_3 A_1^3/4$. A factor of two in voltage equals 6 dB and a factor of eight equals 18 dB.

Of great interest are intermodulation products appearing in the vicinity of the carrier frequency. These are third order intermodulation products of the form $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$. Figure A.1 depicts the two tones with the intermodulation distortion (IMD) of interest. The two fundamental tones of a two-tone signal are the two innermost lines in figure A.1. Third order intermodulation products appear at frequencies $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$. The outermost tones at frequencies $3\omega_1-2\omega_2$ and $3\omega_2-2\omega_1$ are fifth order intermodulation products.

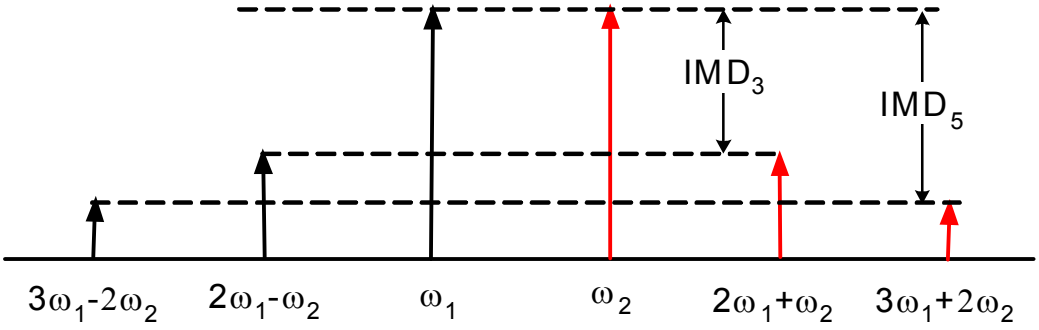


Figure A.1. Frequency spectrum of intermodulation distortion.

# APPENDIX B

# INTRINSIC SMALL SIGNAL MODEL

The intrinsic small-signal model of MESFET devices which consists of 8 elements: $C_{gs}$, $R_{gs}$, $C_{gd}$, $R_{gd}$, $g_m$, $\tau$, $R_{ds}$, and $C_{ds}$ is shown in figure 3.1. This appendix demonstrates the derivation of the Y-parameters of this model described by equations (3.5). It also explains how the intrinsic parameters can be derived in equations (3.6).

## B.1 Derivation of Intrinsic Y-Parameters

Figure B.1 shows the intrinsic model out of figure 3.3 separately. The figure shows the intrinsic circuit as a two-port network. The terminal voltage relations of this two-port network can be expressed in terms of the Y-parameters as [16]:

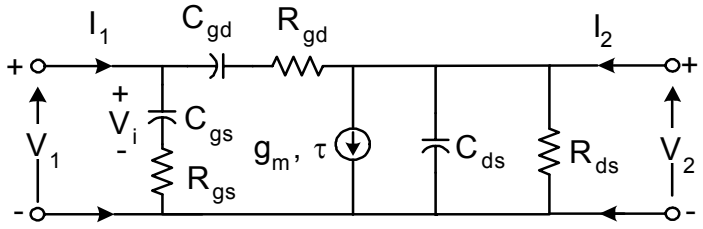


Figure B.1. Intrinsic model for MESFET.

$$I_1 = y_{11} V_1 + y_{12} V_2 \tag{B.1a}$$

$$I_2 = y_{21} V_1 + y_{22} V_2 \tag{B.1b}$$

The Y-parameters of equations (B.1a) and (B.1b) can be calculated for the circuit of figure B.1 as:

$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} = \frac{1}{R_{gs} + \frac{1}{j\omega C_{gs}}} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} = \frac{j\omega C_{gs}}{1 + j\omega R_{gs} C_{gs}} + \frac{j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \tag{B.2a}$$

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = \frac{I_m - \frac{j\omega c_{gd}}{1 + j\omega R_{gd} C_{gd}} V_1}{V_1} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_{gs} C_{gs}} - \frac{j\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \tag{B.2b}$$

$$y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} = \left(\frac{-I_1}{V_2}\right) = -\frac{j\omega C_{gd}}{1+j\omega R_{gd} C_{gd}} \tag{B.2c}$$

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} = g_{ds} + j\omega C_{ds} + \frac{j\omega C_{gd}}{1+j\omega R_{gd} C_{gd}} \tag{B.2d}$$

Applying simple mathematical manipulations, all Y-parameters can be rewritten in the form of equation (3.5) where the index 'i' is omitted for simplicity.

## B.2 Derivation of Intrinsic Parameters

Equations (B.2a) through (B.2d) form eight equations into eight unknowns; each equation can be split into real and imaginary equations. Therefore, these equations can be solved for the intrinsic parameters. The real and imaginary parts of all Y-parameters are known after de-embedding them from the measured S-parameters. Since the real and imaginary parts of $y_{11}$, $y_{12}$, and $y_{22}$ are needed in the following derivation, we can write them separately as:

$$\mathrm{Re}(y_{11}) = \frac{\omega^2 R_{gs} C_{gs}^2}{|D_1|^2} + \frac{\omega^2 R_{gd} C_{gd}^2}{|D_2|^2} \tag{B.3a}$$

$$\mathrm{Im}(y_{11}) = \omega\left(\frac{C_{gs}}{|D_1|^2} + \frac{C_{gd}}{|D_2|^2}\right) \tag{B.3b}$$

$$\mathrm{Re}(y_{12}) = \frac{\omega^2 R_{gd} C_{gd}^2}{|D_2|^2} \tag{B.3c}$$

$$\mathrm{Im}(y_{12}) = -\omega\left(\frac{C_{gd}}{|D_2|^2}\right) \tag{B.3d}$$

$$\mathrm{Re}(y_{22}) = g_{ds} + \frac{\omega^2 R_{gd} C_{gd}^2}{|D_2|^2} \tag{B.3e}$$

$$\mathrm{Im}(y_{22}) = \omega\left(C_{ds} + \frac{C_{gd}}{|D_2|^2}\right) \tag{B.3f}$$

where

$$D_1 = 1 + j\omega R_{gs} C_{gs} \tag{B.3g}$$

$$D_2 = 1 + j\omega R_{gd} C_{gd} \tag{B.3h}$$

Adding equation (B.3b) to equation (B.3d) reveals the following:

$$\mathrm{Im}(y_{11}) + \mathrm{Im}(y_{12}) = \frac{\omega C_{gs}}{|D_1|^2} \tag{B.4}$$

On the other hand, adding equation (B.3a) to equation (B.3c) leads to the following:

$$\mathrm{Re}(y_{11}) + \mathrm{Re}(y_{12}) = \frac{\omega^2 R_{gs} C_{gs}}{|D_1|^2} \tag{B.5}$$

Dividing equation (B.5) by equation (B.4) eliminates $D_1$:

$$\omega R_{gs} C_{gs} = \frac{\mathrm{Re}(y_{11}) + \mathrm{Re}(y_{12})}{\mathrm{Im}(y_{11}) + \mathrm{Im}(y_{12})} \tag{B.6}$$

The right hand side of equation (B.6) can be assumed to be equal to a variable $d_1$; thus equation (B.6) can be rewritten as:

$$\omega R_{gs} C_{gs} = d_1 \tag{B.7}$$

where

$$d_1 = \frac{\mathrm{Re}(y_{11}) + \mathrm{Re}(y_{12})}{\mathrm{Im}(y_{11}) + \mathrm{Im}(y_{12})} \tag{B.8}$$

Also, $D_1$ can be written in terms of $d_1$:

$$D_1 = 1 + d_1 \tag{B.9}$$

Substituting $D_1$ from equation (B.9) into equation (B.4), $C_{gs}$ can be evaluated:

$$C_{gs} = \frac{(1 + d_1^2)}{\omega}(\mathrm{Im}(y_{11}) + \mathrm{Im}(y_{12})) \tag{B.10}$$

$C_{gs}$ can be substituted in equation (B.7) to get $R_{gs}$:

$$R_{gs} = \frac{d_1}{(1 + d_1^2)(\mathrm{Im}(y_{11}) + \mathrm{Im}(y_{12}))} \tag{B.11}$$

$C_{gd}$ and $R_{gd}$ can be calculated in a similar manner. Divide equation (B.3c) by equation (B.3d) to remove $D_2$:

$$\omega R_{gd} C_{gd} = d_2 \tag{B.12}$$

where

$$d_2 = \frac{\mathrm{Re}(y_{12})}{\mathrm{Im}(y_{12})} \tag{B.13}$$

$D_2$ can be expressed in terms of $d_2$ as:

$$D_2 = 1 + jd_2 \tag{B.14}$$

Substitute $D_2$ into equation (B.3d) to estimate $C_{gd}$:

$$C_{gd} = \frac{\mathrm{Im}(y_{12})}{\omega}\left(1 + d_2^2\right) \tag{B.15}$$

Substitute $C_{gd}$ into equation (B.12) and rearrange to get $R_{gd}$:

$$R_{gd} = -\frac{d_2}{\left(1 + d_2^2\right)\mathrm{Im}(y_{12})} \tag{B.16}$$

The complex transconductance $G = g_m e^{-j\omega\tau}$ can be evaluated from the complex parameters $y_{21}$ and $y_{12}$. The second term of $y_{21}$ in equation (B.2b) can be removed by subtracting equation (B.2c) from (B.2b):

$$y_{12} = y_{21} = \frac{G}{1 + jd_1} \tag{B.17}$$

G can be extracted from equation (B.17):

$$G = \left(y_{21} - y_{12}\right)\left(1 + jd_1\right) \tag{B.18}$$

The magnitude and phase of G represent $g_m$ and $(-\omega\tau)$, respectively:

$$g_m = |G| = |(y_{21} - y_{12})|\left(1 + d_1^{\,2}\right) \tag{B.19}$$

$$\tau = -\frac{1}{\omega}\angle(G) \tag{B.20}$$

The last two parameters $g_{ds}$ and $C_{ds}$ can be calculated using equations (B.3c) through (B.3f). Adding equation (B.3c) to equation (B.3e) results in gds, while adding equation (B3.d) to equation (B.3f) and rearranging results in $C_{ds}$:

$$g_{ds} = \mathrm{Re}(y_{22}) + \mathrm{Re}(y_{12}) \tag{B.21}$$

$$C_{ds} = \frac{\mathrm{Im}(y_{22}) + \mathrm{Im}(y_{12})}{\omega} \tag{B.22}$$

In summary, equations (B.10), (B.11), (B.15), (B.16), (B.19), (B.20), (B.21), and (B.22) constitute the solution set of the intrinsic parameters at single-frequency measurements.

# APPENDIX C

# DETERMINATION OF BROADBAND GAIN BASED ON RESISTIVE FEEDBACK

Feedback is used to reduce the nonlinear distortion products in an amplifier. As the output power increases, the intermodulation products will increase in magnitude. Resistive feedback will reduce the magnitude of these products. The most important application of feedback is in broadband amplifiers. Broadband amplifiers of increasing bandwidth can be realized simply by increasing the negative feedback, which of course lowers gain. When higher gain is required, more stages are cascaded in the final amplifier. Analysis of extracting the relation that combine the amplifier gain with the feedback resistance will be presented.

Figure C.1 illustrates the MESFET transistor with shunt feedback and its corresponding simplified small signal model at low frequencies shunted with a resistance $R_F$ between gate and drain. The low frequency analysis of this circuit will give an understanding of the circuit operation.

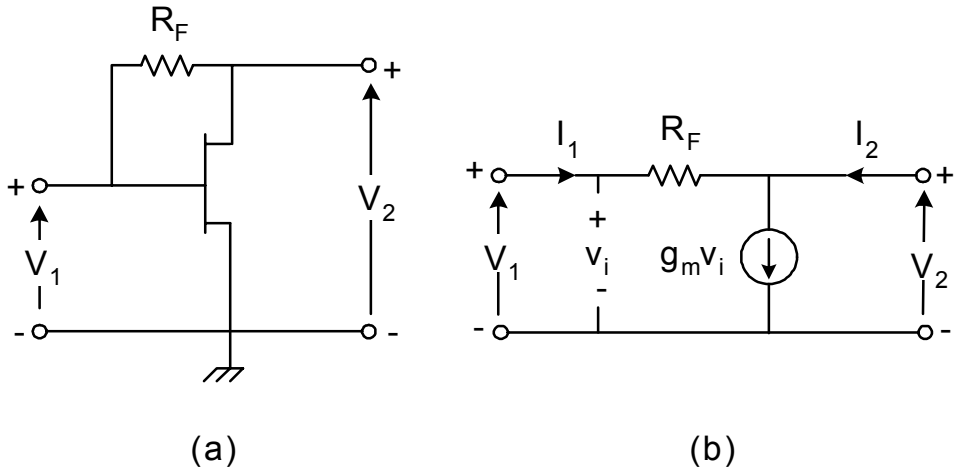


Figure C.1. (a): MESFET with shunt feedback, (b): Feedback equivalent circuit.

From Y-parameter theory, the admittance matrix for the two-port network can be written as

$$[I]=[Y][V] \tag{C.1}$$

or

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}=\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{C.2}$$

where

$$y_{11}=\frac{1}{R_F} \tag{C.3a}$$

$$y_{12}=-\frac{1}{R_F} \tag{C.3b}$$

$$y_{21}=g_m-\frac{1}{R_F} \tag{C.3c}$$

$$y_{22}=\frac{1}{R_F} \tag{C.3d}$$

The Y-parameters can be converted to the S-parameters for the design purpose. Then the S-parameters can be expressed in terms of the resistances and transconductance as follows [C.1]:

$$S_{11}=S_{22}=\frac{1}{D}\left[1-\frac{g_m Z_0^2}{R_F}\right] \tag{C.4a}$$

$$S_{12}=\frac{2Z_0}{DR_F} \tag{C.4b}$$

$$S_{21}=\frac{1}{D}\left[-2g_m Z_0+\frac{2Z_0}{R_F}\right] \tag{C.4c}$$

where

$$D=1+\frac{g_m Z_0^2}{R_F}+\frac{2Z_0}{R_F} \tag{C.4d}$$

For a perfect voltage standing wave ratio in the input and output port, VSWR = 1, the required condition is $S_{11} = S_{22} = 0$. Then

$$\frac{g_m Z_0^2}{R_F}=1 \tag{C.5}$$

Substituting of Eq. (C.5) into Eq. (C.4c) yields

$$S_{21} = \frac{Z_0 - R_F}{Z_0} \tag{C.6}$$

If $|R_F| > Z_0$, $|S_{21}|$ is negative. Equation (C.6) indicates that the $S_{21}$ parameter depends only on $R_F$, not on the other S-parameters. Therefore, the gain flattening can be accomplished by using parallel feedback over a broadband frequency. Then

$$R_F = Z_0\left(1 + |S_{21}|\right) \quad \text{for } |R_F| > Z_0 \tag{C.7}$$

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