A 96 % efficient high-frequency DC-DC converter using E-mode GaN DHFETs on Si

A 96% Efficient High-Frequency DC–DC Converter Using E-Mode GaN DHFETs on Si

Jo Das, *Member, IEEE*, Jordi Everts, *Member, IEEE*, Jeroen Van Den Keybus, Marleen Van Hove, Domenica Visalli, Puneet Srivastava, *Student Member, IEEE*, Denis Marcon, *Student Member, IEEE*, Kai Cheng, Maarten Leys, Stefaan Decoutere, Johan Driesen, and Gustaaf Borghs

***Abstract*—III-Nitride materials are very promising to be used in next-generation high-frequency power switching applications. In this letter, we demonstrate the performance of normally off AlGaN/GaN/AlGaN double-heterostructure FETs (DHFETs) using a boost-converter circuit. The figures of merit of our large (57.6-mm gate width) GaN transistor are presented: $R_{\mathrm{ON}} * Q_G$ of 2.5 $\Omega \cdot$ nC is obtained at $V_{\mathrm{DS}} = 140$ V. The switching performance of the GaN DHFET is studied in a dedicated high-frequency boost converter: both the switching times and power losses are characterized. We show converter efficiency values up to 96.1% at 500 kHz and 93.9% at 850 kHz at output power of 100 W.**

***Index Terms*—Converters, efficiency, GaN, high voltage, power field-effect transistors (FETs), SPICE.**

I. Introduction

FOR power switching applications, there is a trend to increase the switching frequency in order to reduce the size of the converter design. In this perspective, GaN-based materials have attracted a lot of attention because of their outstanding properties such as high power density and high breakdown voltage [1], [2]. Moreover, it has been shown that these heterostructures can be grown onto large-diameter Si substrates [3], which is of course a major cost advantage.

For switching applications, enhancement-mode (E-mode) devices are usually preferred. Different concepts have been proposed in the literature [4]–[6] to convert the GaN device from the conventional depletion mode (D-mode) to E-mode.

We have recently shown that E-mode operation can be obtained by selective removal of the *in situ* grown passivation layer under the gate [7]. We will show the potential of this approach for high-frequency power conversion applications. In the literature, some demonstrations of GaN-based devices in converter circuits have been already shown. An efficiency value of 97.8% for D-mode devices on SiC has been demonstrated [2]. For E-mode devices, recently, efficiency values of 96% at 200 kHz have been presented [8].

In this letter, we discuss the results of a boost converter with a compact design for a frequency range between 300 kHz and 1 MHz. High efficiency values at high switching frequencies are demonstrated, proving the high potential of the GaN technology.

II. Device Fabrication and Characterization

The GaN devices are fabricated starting from a Si_3N_4/$Al_{0.45}Ga_{0.55}N$/GaN/$Al_{0.18}Ga_{0.82}N$ metal–organic chemical-vapor-deposition-grown heterostructure on a 100-mm Si$\langle 111 \rangle$ substrate ($\rho > 5000\ \Omega \cdot$ cm) [9]. The III-nitride heterostructure is capped with a 50-nm *in situ*-grown Si_3N_4 layer in order to passivate the surface and prevent strain relaxation of the $Al_{0.45}Ga_{0.55}N$ layer [10]. To process the layers into devices, the following steps are executed: device isolation, ohmic contact formation, gate fabrication, Si_3N_4 passivation, and deposition of an interconnection layer.

The III-nitride heterostructure is designed in such a way that E-mode devices are obtained: by scaling down the $Al_{0.45}Ga_{0.55}N$ top-layer thickness below 5 nm, and by selectively removing the *in situ* Si_3N_4 under the gate, positive threshold voltages can be obtained [7]. In this letter, we have used a 4-nm-thick $Al_{0.45}Ga_{0.55}N$ top barrier layer. The GaN channel layer and $Al_{0.18}Ga_{0.82}N$ buffer layer thickness are 150 nm and 1 μm, respectively.

On-wafer transfer characteristic measurements are done on small devices, with total gate width $W_G = 200$ μm and gate length $L_G = 1.5$ μm. From these measurements, threshold voltage $V_T = 0.15$ V, ON-resistance $R_{\mathrm{ON}} = 12\ \Omega \cdot$ mm, and maximum saturation current $I_{\mathrm{DS}} = 0.4$ A/mm are extracted. The OFF-state breakdown voltage (measured at gate voltage $V_{\mathrm{GS}} = 0$ V) depends on gate–drain gap L_{GD} and the buffer thickness [11]. For $L_{\mathrm{GD}} = 8$ μm, we obtained V_{BD} as high as 550 V, where V_{BD} is defined as the drain voltage at which the leakage current I_{DS} increases to 1 mA/mm. Note that, although the average V_{BD} measured on small test devices is 550 V, we will limit the operating voltage of the final GaN switching device in the converter setup to 200 V in order to avoid any possible device degradation during operation.

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J. Das, M. Van Hove, D. Visalli, P. Srivastava, D. Marcon, K. Cheng, M. Leys, S. Decoutere, and G. Borghs are with the Interuniversity Microelectronics Center (IMEC), 3001 Leuven, Belgium (e-mail: jdas@imec.be).

J. Everts is with the Department of Electrical Engineering, Research Group ELECTA, Katholieke Universiteit Leuven, 3001 Leuven, Belgium, and also with the Katholieke Hogeschool Limburg (KHLim), 3590 Diepenbeek, Belgium.

J. Van Den Keybus is with Triphase, 3001 Leuven, Belgium.

J. Driesen is with the Department of Electrical Engineering, Research Group ELECTA, Katholieke Universiteit Leuven, 3001 Leuven, Belgium.

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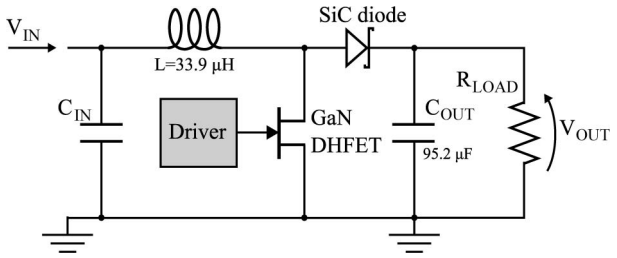

Fig. 1. Boost converter schematic. A driver is designed in order to provide both negative and positive gate voltages in a frequency range up to 6 MHz.

III. Boost Converter: Design and Realization

To show the potential of the GaN double-heterostructure FET (DHFET) devices for high-frequency power switching applications, a high-frequency hard-switching boost converter is constructed, as this is often used, e.g., for power factor correction. Starting from the dc and C–V characterization of the devices, a SPICE model for the GaN DHFETs was made prior to the converter design. We have already shown before that the model is scalable to large gate-width GaN devices [12]. For this letter, GaN DHFETs with total gate width $W_G = 57.6$ mm are used. To integrate these GaN DHFETs into the boost converter circuit, the dies are packaged onto an AlN carrier acting as a heat spreader. Mounting is done using a 25-μm -thick AuSn preform layer in order to obtain an excellent heat transfer between the GaN die and the carrier. Furthermore, AlN is mounted in a next step on an additional Cu heat sink.

The schematic of the circuit is shown in Fig. 1. A SiC diode (Cree C3D04060, 600 V, 4 A) is used because of its very low recovery current. The converter has a custom-made gate driver circuit [13], which can deliver drive signals up to 6 MHz. The voltage range of the gate driver is adjustable, making it possible to deliver negative voltages. This way, both D-mode (normally on) and E-mode (normally off) devices can be used in the setup. Finally, special attention was paid to the compactness of the converter. Therefore, an ultracompact planar inductor ($L = 33.9$ μH) was developed in-house, with a volume of only 19.2 cm^3. However, a disadvantage of the small inductance is the bigger hysteresis loss per cycle.

IV. Converter Results

Using the boost converter setup, the dynamic ON-resistance $R_{\text{ON-DYN}}$ and gate charge values Q_G of the GaN transistor are measured [13]. $R_{\text{ON-DYN}}$ is calculated as $V_{\text{DS}}/I_{\text{DS}}$ during the ON-state of the transistor in the boost converter. $R_{\text{ON-DYN}} = 0.23\ \Omega$ and only shows a minor increase with increasing OFF-state drain voltage $V_{\text{DS,OFF}}$, proving the absence of surface or bulk electron trapping in the device. Q_G is determined by integrating the gate drive current during the turn-on switching of the transistor. From these measurements, a total gate charge value of 11 nC is obtained at $V_{\text{DS,OFF}} = 140$ V, resulting in $R_{\text{ON}} * Q_G$ as low as 2.5 $\Omega \cdot$ nC for the E-mode GaN DHFET. This value is comparable with commercial Si-based 200-V-rated MOS transistors but significantly higher compared with commercial devices from EPC [14]. The Q_G value of our GaN devices, which is still relatively high due to the very thin top AlGaN layer, could still be improved by scaling down the gate length to submicrometer dimensions.

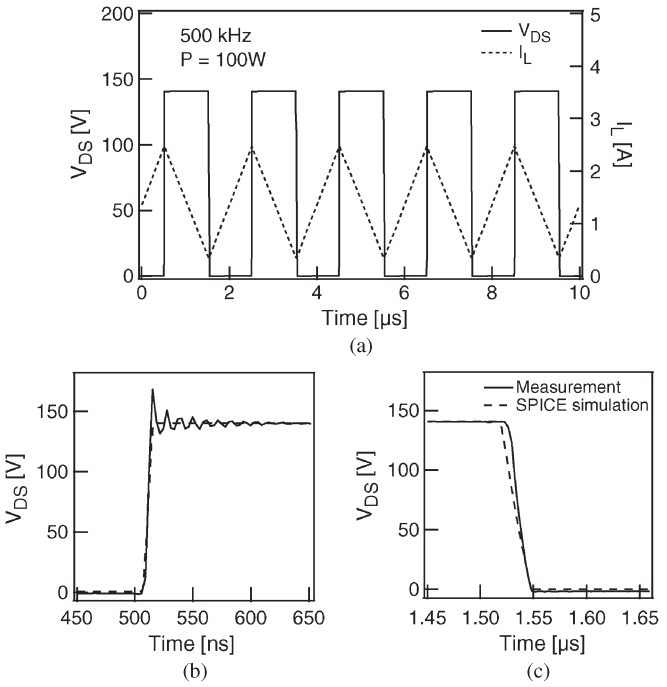

Fig. 2. (a) Boost converter transient behavior: both drain voltage V_{DS} of the GaN DHFET and current I_L through the inductor are shown. (b) and (c) Detailed switching behavior of the GaN DHFET: the measured drain voltage V_{DS} is compared with the simulated behavior using SPICE simulations. (b) Rise time of 5 ns and (c) fall time of 20 ns are obtained.

Fig. 2 shows the switching behavior of the E-mode GaN DHFET. We can see that the measured rise and fall time values are in close agreement with the SPICE simulations. Note that the gate was switched between 2 and -8 V, whereas the output voltage of the converter was at 140 V. The two reasons for the negative gate voltage are to obtain a faster turnoff of the device and to avoid unintended switching imposed by disturbances. For the turn-on, the maximum gate voltage is limited to 2 V to avoid an excessive current in the Schottky gate diode. As a result, the fall time $t_{\text{FALL}} = 20$ ns of the drain voltage is much higher than the rise time $t_{\text{RISE}} = 5$ ns. To reduce the fall time, the maximum allowable gate voltage should be increased beyond 2 V. Therefore, it would be an advantage to replace the Schottky gate by a MOS gate so that a larger positive gate swing can be obtained.

In a next step, the boost converter efficiency was measured as a function of the switching frequency and output power (see Fig. 3). Duty cycle D was kept constant at 50%. The highest efficiency values were obtained at $P_{\text{OUT}} = 100$ W: at 500 and 850 kHz, efficiency values as high as 96.1% and 93.9%, respectively, are obtained. Note that the efficiency (at constant P_{OUT}) slightly depends on V_{OUT} (and, thus, also on I_{OUT}). This is mainly because the conduction losses are higher at higher output currents. To the best of our knowledge, this is the highest efficiency reported for E-mode GaN DHFETs on Si substrates at these high switching frequencies. It clearly shows the high potential of GaN-on-Si devices for high-frequency power switching applications compared with commercial Si-based MOSFET devices [15], [16].

To have a better understanding of the efficiency limitations in the converter, we analyzed the power losses in the converter

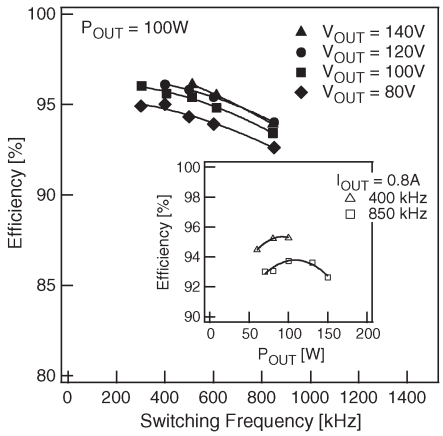

Fig. 3. Converter efficiency versus switching frequency. The duty cycle (50%) and $P_{\rm OUT}$ (100 W) are constant. At 500 kHz and $V_{\rm OUT} = 140$ V, maximum efficiency of 96.1% is obtained. (Inset) Efficiency as a function of the output power at two different switching frequencies, i.e., 400 and 850 kHz.

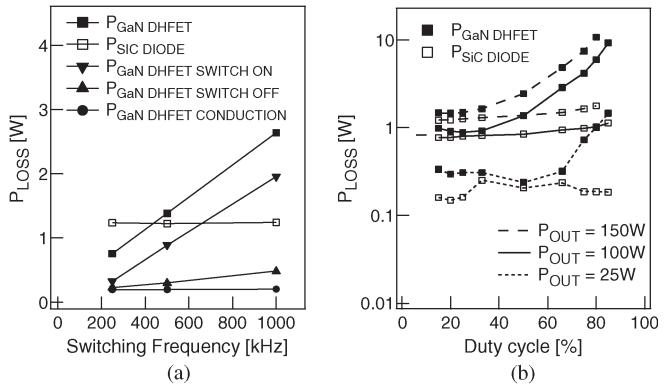

Fig. 4. (a) Simulation of the SiC diode losses ($P_{\rm SiC\text{-}DIODE}$) and GaN DHFET losses ($P_{\rm GAN\text{-}DHFET} = P_{\rm CONDUCTION} + P_{\rm SWITCH\text{-}ON} + P_{\rm SWITCH\text{-}OFF}$) as a function of the switching frequency. Duty cycle $D = 50\%$, $P_{\rm OUT} = 100$ W, and $V_{\rm OUT} = 140$ V are constant. (b) Simulation of $P_{\rm GAN\text{-}DHFET}$ and $P_{\rm SiC\text{-}DIODE}$ at different $P_{\rm OUT}$ as a function of D. $V_{\rm OUT} = 140$ V and $f = 500$ kHz are kept constant.

using SPICE simulations. Fig. 4(a) shows the losses of the SiC diode and the GaN DHFET as a function of the switching frequency. It is clear that, at high switching frequencies, the GaN DHFET losses are dominated by the switch-on losses because of the relatively high fall time of the drain-to-source voltage. Note that the losses of the gate driver are less than 3% of the total losses, and therefore, they are not included in the figure. By a comparison of the SPICE simulation and measurements, we can also estimate the parasitic losses (e.g., inductor and interconnection losses), which are around 2 W at $P_{\rm OUT} = 100$ W and $f = 500$ kHz. Fig. 4(b) shows the diode and DHFET losses for different duty cycles and different $P_{\rm OUT}$. From this figure, it is clear that the DHFET losses are dominant at higher duty cycles because of the higher DHFET conduction losses at these conditions.

V. Conclusion

A 100-W compact boost converter has been designed for a frequency range up to 1 MHz using a GaN-on-Si E-mode device and a SiC diode. Low switching times ($t_{\rm RISE} = 5$ ns and $t_{\rm FALL} = 20$ ns) and $R_{\rm ON} \times Q_{\rm G} = 2.5\ \Omega$.nC at $V_{\rm DS} = 140$ V are demonstrated. Moreover, high conversion efficiency values of 96.1% and 93.9% are obtained at switching frequencies of 500 and 850 kHz, respectively, showing the high performance of the E-mode GaN-on-Si DHFETs.

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