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Waveguide-Coupled Nanolasers in III-V Membranes on Silicon

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ABSTRACT

Semiconductor nanolasers provide an attractive route towards high density photonic integrated circuits in low power applications such as optical interconnects. In this paper we present the concept of a waveguide-coupled nanolaser for integration in a CMOS compatible photonic platform. We exploit metallic and dielectric confinement to provide high quality factors exceeding 500 in a wavelength-scale cavity, that provides efficient cooling and cross-talk immunity due to the metal coverage. We present simulations detailing the design considerations for high quality factors and efficient waveguide coupling. Optical and electrical simulations predict room temperature operation at $1.55 \mu\text{m}$ with a threshold current of $120 \mu\text{A}$ and a differential quantum efficiency of 0.16. We also discuss briefly the challenges of fabricating these devices and integrating them in the photonic platform.

Keywords: photonic circuits, nanophotonics, nanolasers, metallo-dielectric lasers, III-V membrane.

1. INTRODUCTION

Semiconductor nanolasers with metallo-dielectric cavities are considered as promising light sources for ultra-dense photonic integration [1]. These devices have generated a large interest in view of their potential for low current operation, ultra-fast modulation, large scale integration, cross talk immunity and excellent cooling properties. Such lasers exploit metallic and dielectric confinement to provide high quality factors allowing lasing at room temperature in wavelength-scale cavities with active regions well below $1 \mu\text{m}^2$ footprint [2].

For its use in photonic integrated circuits, efficient waveguide coupling to a photonic wire is mandatory. In this paper, we present the design of a waveguide-coupled nanolaser and discuss the fabrication challenges. A schematic representation of the laser design is presented in Fig. 1. The laser is compatible with a photonic platform, where a III-V membrane is bonded to a CMOS wafer using a polymer (BCB). This enables very dense photonic circuits tightly integrated with their electrical driver and receiver circuits in low power applications such as optical interconnects [3].

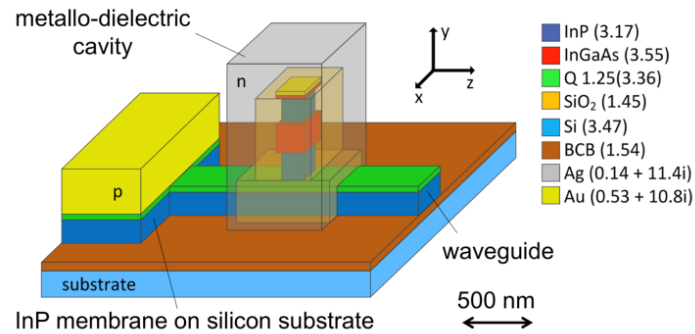


Figure 1. Model of a metallo-dielectric nanolaser coupled to an InP-membrane waveguide. The legend shows the material refractive index at $1.55 \mu\text{m}$.

This paper is organized as follows. In the first section, the optical design is presented. In the second section, electrical and thermal simulations are introduced. Then, the challenges to fabricate the device are briefly discussed in the next section. Finally, some conclusions regarding the expected performance of the nanolaser are presented.

2. OPTICAL SIMULATIONS

The optical design of the laser cavity and its coupling to an InP-waveguide was performed with three-dimensional finite-difference time-domain simulations. The cavity supports a TE-polarized mode with high quality factor. The optimized parameters are highlighted in Fig. 2a, where t is the SiO₂ dielectric thickness, h is the height of the InP bottom post and s is an undercut. A thick dielectric decreases the absorption into the metal,

but also increases the radiative leakage due to a poor confinement. The bottom post controls the Q-factor as well as the coupling to the waveguide. A short post enhances the laser optical efficiency at the expense of a Q-factor decrease. The undercut is introduced to increase the Q-factor, while maintaining a relatively short post to simplify the fabrication process. The optimum values of these parameters were found to be $t = 175 \text{ nm}$, $h = 400 \text{ nm}$, $s = 60 \text{ nm}$. The detailed design is described in [4].

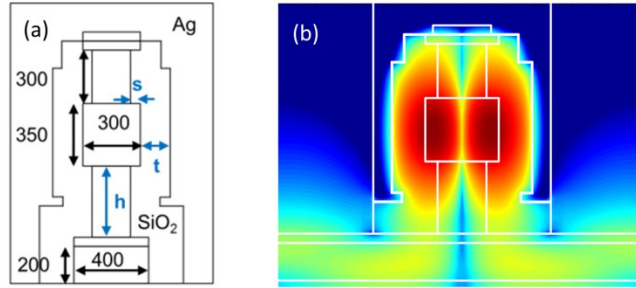


Figure 2. (a) Transversal cross section of the parameterized cavity with dimensions in nanometers. (b) Colour plot of $\log(|E|^2)$ showing the coupling between the lasing mode and the waveguide along the longitudinal cross section.

After the optimization of a symmetric pillar cavity, the longitudinal dimension (along the outcoupling waveguide) of the pillar was increased to enhance the waveguide coupling, which in turns enhances the differential quantum efficiency. The differential efficiency is defined as the number of photons injected into the waveguide divided by the total number of photons generated in the cavity. Furthermore, the resonant wavelength can be adjusted, since it increases linearly with the cavity length. As it can be seen in Fig. 3, a cavity length of 400 nm results in a resonant wavelength near $1.55 \mu\text{m}$, a Q-factor exceeding 500 and a differential efficiency of 0.16. Considering a confinement factor of 0.33, the threshold gain is calculated to be 815 cm^{-1} , which is expected to be achievable at room temperature.

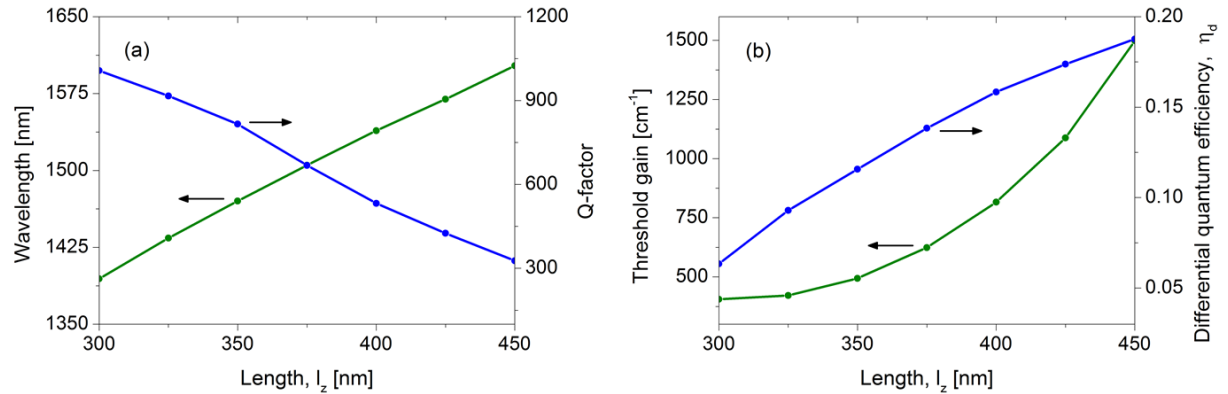


Figure 3. (a) Resonant wavelength and Q-factor as a function of cavity length. (b) Threshold gain and differential quantum efficiency, assuming a unity internal quantum efficiency.

3. ELECTRICAL AND THERMAL SIMULATIONS

Electrical simulations were carried out with the self-consistent Poisson solver nextnano++ to determine the threshold current. A detailed description of such simulations can be found in [5]. Table 1 shows the semiconductor layer stack considered for the electrical simulations.

Table 1. Semiconductor layer stack considered for electrical and thermal simulations.

Thickness [nm]	Material	Doping [$1/\text{cm}^3$]
50	n-InGaAs	$1 \cdot 10^{19}$
200	n-InP	$5 \cdot 10^{18}$
100	n-InP	$1 \cdot 10^{18}$
350	i-InGaAs	-
100	p-InP	$3 \cdot 10^{17}$
100	p-InP	$5 \cdot 10^{17}$
100	p-InP	$1 \cdot 10^{18}$
100	p-Q1.25	$2.4 \cdot 10^{19}$

Using nextnano++, the dependence of the Fermi levels in valence and conduction bands as a function of current density can be calculated. This allows to calculate the optical material gain with Fermi's golden rule at a temperature of 300 K [6]. The resulting gain spectra are presented in Fig. 4a for current densities ranging from 20 to 200 kA/cm^2 . The material gain at 1550 nm is plotted in Fig. 4b as a function of the current density. The threshold gain of 815 cm^{-1} determined by the optical simulations is reached with a current density of 100 kA/cm^2 corresponding to a threshold current $I_{th} = 120\text{ }\mu\text{A}$ for the nanolaser with an active area cross section of $300 \times 400\text{ nm}^2$.

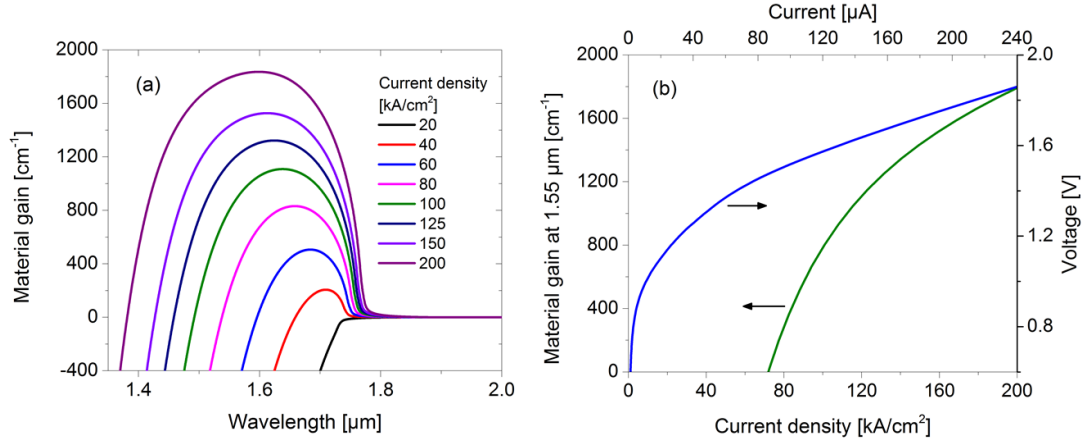


Figure 4. (a) InGaAs material gain for different current densities. (b) Material gain at $1.55\text{ }\mu\text{m}$ and voltage through the device as a function of current.

The current-voltage characteristics of the diode are plotted in Fig. 4b. The device has a total resistance of $2.25\text{ k}\Omega$. This is a combination of the p-side contact ($400\text{ }\Omega$), where the current is transported in a 100 nm thin quaternary layer on top of the waveguide, the p-doped region of the laser diode ($1000\text{ }\Omega$) and the ohmic contact on the n-doped side of the pillar ($850\text{ }\Omega$), where we assume a contact resistance of $1 \cdot 10^{-6}\text{ }\Omega\text{cm}^2$. When driving a current through the device the high resistive regions contribute to heat generation as it is shown in the inset of Fig. 5, while the optical absorption in the metal coating of the cavity can be neglected.

If no self-heating is considered, the optical output power grows linearly with the drive current I as $P_{out} = \eta_d(I - I_{th})hc/\lambda e$ as it is plotted in Fig. 5. Here, $\eta_d = 0.16$ is the differential quantum efficiency and $I_{th} = 120\text{ }\mu\text{A}$ is the threshold current for an emission wavelength of $\lambda = 1.55\text{ }\mu\text{m}$. Figure 5 also shows the temperature in the laser as a function of the drive current for one laser per 800 , 1500 , and $3000\text{ }\mu\text{m}^2$, calculated with a three-dimensional finite element model. To calculate the laser temperature we assume packaging with a high performance heat sink as described in reference [7] with a junction-to-ambient heat transfer coefficient of $7000\text{ W/(m}^2\text{ K)}$. In the linear model, an optical output power of nearly $40\text{ }\mu\text{W}$ is reached for a current of $425\text{ }\mu\text{A}$ and a voltage of 1.98 V corresponding to an efficiency of 4.8% . In a real laser device, the self-heating produces a clamp in the output power. Additionally, since the heat dissipation in realistic packaging is limited, a compromise between integration density and available optical power will need to be found.

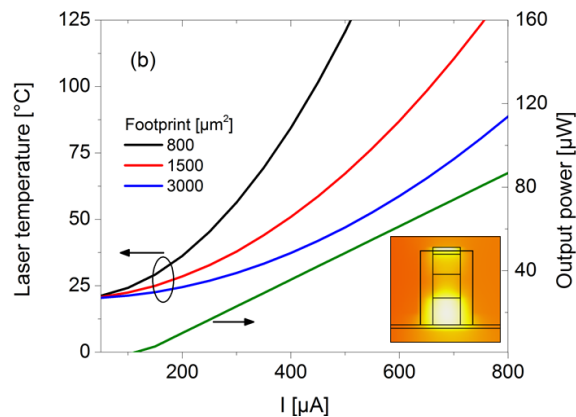


Figure 5. Laser temperature and estimated output power as a function of drive current. The inset shows a colour plot of the temperature distribution in the cavity. White: high temperature. Orange: low temperature.

4. FABRICATION CONSIDERATIONS

The device fabrication consists in a complex series of steps. It involves different processes, such as: electron beam lithography, optical lithography, plasma-enhance chemical vapour deposition techniques, reactive ion etching processes, wet-chemical etching, thermal and electron-beam evaporation of metals, rapid thermal annealing, etc. Among the most critical steps are: the vertical etching of the pillar cavity, the creation of an undercut to achieve high cavity Q-factor and the alignment of the overlay lithography to fabricate the laser pillar on top of the waveguide. Figure 6 shows pictures taken with a scanning electron microscope of our current efforts to fabricate the device. More details regarding the challenges to fabricate such metallo-dielectric nanolaser will be discussed during the presentation.

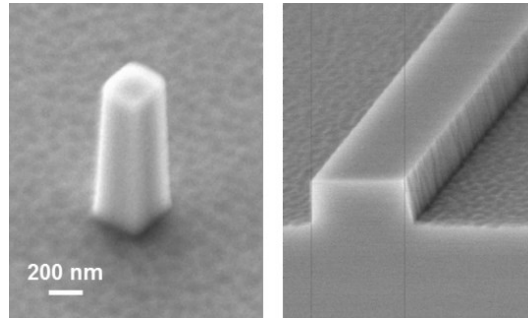


Figure 6. Left: III-V semiconductor pillar intended to form the laser cavity. Right: InP-waveguide structure.

5. CONCLUSIONS

The design of a metallo-dielectric nanolaser was presented. Optical, electrical and thermal simulations were carried out to predict the performance of such a laser, resulting in a cavity Q-factor of 532 with a threshold gain of 815 cm^{-1} and a threshold current of $120 \mu\text{A}$. Using a high performance heat sink, output powers of $40 \mu\text{W}$ seem feasible at a voltage of 1.98 V and a current of $425 \mu\text{A}$. A compromise between the device footprint and the maximum output power was identified. The device fabrication will be discussed during the presentation.

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