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CIRCUIT DESIGN IN COMPLEMENTARY ORGANIC TECHNOLOGIES

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. C.J. van Duijn, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op dinsdag 25 november 2014 om 16:00 uur

door

Sahel Abdinia

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List of abbreviations

Abbreviation	Description
AC	Alternating Current
ADC	Analogue to Digital Convertor
Al_2O_3	Aluminium Oxide
AM	Amplitude Modulation
AMOLED	Active-Matrix Light-Emitting Diode
AND	AND Logic Gate
ASK	Amplitude-Shift Keying
BCD	Binary Coded Decimal
BW	Band Width
C14-PA	a N-tetradecylphosphonic Acid
C-2C	Capacitor-double-Capacitor
CAD	Computer Aided Design
CDR	Clock and Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
COSMIC	Complementary Organic Semiconductor Metal Integrated Circuits
CRU	Code Recognition Unit
CYTOP	a Fluoropolymer Dielectric
DAC	Digital to Analogue Converter
DC	Direct Current
D-FF	Data Flip Flop
D-latch	Data latch
DNL	Differential Nonlinearity
DNLmax	Maximum DNL
ED	Envelope Detector
ELR	Extrapolation of the Linear Region
ENOB	Effective Number Of Bits
ESD	Electro-Static Discharge
FF	Flip Flop
FOC	Foil On Carrier
FPD	Flat Panel Display
FW	Finger Width
Gen.1 and 2	Generation one and two of S2S technology
GND	Ground
HF	High Frequency
IC	Integrated Circuit

Abbreviation	Description
INL	INtegral Nonlinearity
INLmax	Maximum INL
ITO	Indium Tin Oxide
IVM	Identity Verification Module
LSB	Least Siginificant Bit
LUMO	Lowest Unoccupied Molecular Orbital
MC	Monte Carlo
MF	Multi-Finger
MIM	Metal-Insulator-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Master-Slave
MSFF	Master-Slave Flip-Flop
MTR	Multiple Trapping and Release
N3004	N-type Active Material
NAND	Not-AND logic gate
NOR	Not-OR logic gate
n-OSC	n-type OSC
n-OTFT	n-type OTFT
n-TFT	n-type TFT
O_2	Oxygen
OLED	Organic Light Emitting Diode
OR	OR logic gate
OSC	Organic Semiconductor
OTA	Operational Transconductance Amplifiers
OTFT	Organic Thin-Film Transistor
PCE	Power Conversion Efficiency
PDN	Pull-Down Network
PEM	Name of the designed mask-sets (e.g. PEM1a, PEM1b, PEM2a, etc)
PEN	Polyethylene naphthalate
PFBT	pentafluorobenzenethiol
Ph-PXX	3,9-diphenyl-peri-xanthenoxanthene
p-OSC	p-type OSC
p-OTFT	p-type OTFT
PTAA	polytriarylamine
p-TFT	p-type TFT
PUN	Pull-Up Network
PWM	Pulse-Width Modulation
PαMS	poly(α-methylstyrene)

Abbreviation	Description
QQVGA	Quarter-Quarter Video Graphics Array
R2R	Roll-to-Roll
R-2R	Resistance-double-Resistance
RF	Radio Frequency
RFID	Radio Frequency Identificagtion
RM	Reset Module
S/D	Source/Drain terminals
S2S	Sheet-to-Sheet
SAM	Self-Assembled Monolayer
SAR	Successive-Approximation-Register
SC	Switched-Capacitor
SNDR	Signal-to-Noise-and-Distortion-Ratio
SNR	Signal-to-Noise-Ratio
SR-FF	Set-Reset Flip Flop
TCR	Temperature Coefficient of Resistance
T-FF	Toggle Flip Flop
TFT	Thin-Film Transistor
TG	Transmission Gate
Ti-Au	Titanium-Gold
TLM	Transmission Line Model
TSPC-FF	True Single Phase Clock Flip Flop
VRH	Variable Range Hopping
W2W	Wafer-to-Wafer
XOR	Exclusive-OR logic gate

List of symbols

Symbol	Description
μ	Mobility
μ_n	n-type mobility
μ_p	p-type mobility
C_{GD}	Gate-drain capacitance
C_{ins}	Insulator capacitance
C_L	Load capacitance
C_P	Parasitic capacitance
C_S	Sampling capacitance
$C_{tot\text{-}0}$	OTFT parasitic capacitance for L and W equal to zero
dL/dV_{DS}	OTFT channel parameter
$E_{G\text{-}SD}$	Gate layer enclosure on S/D contacts
$E_{OSC\text{-}SD}$	OSC layer enclosure on S/D contacts
E_p	OTFT channel parameter
f_{clk}	Clock frequency
FW	Finger-width
G_i	Gain of i^{th} stage
g_m	OTFT transconductance
$g_{m,n}$	n-OTFT transconductance
$g_{m,p}$	p-OTFT transconductance
G_{max}	Maximum gain
G_t	OTFT channel parameter
H_i	i^{th} harmonic
I_{00}	OTFT contact parameter
I_c	Contact current
I_D	Drain current
I_L	Load current
I_{off}	OTFT off-current
I_{on}	OTFT on-current
I_{rev}	Contact current (I_c) coefficient
$K_B T/q$	Thermal voltage
L	Nominal channel length
L_{early}	OTFT channel parameter
M	Mean value
N_t	density of trap states at the channel-insulator interface
n	Number of OTFT channels

Symbol	Description
q	Injected charge
R_i	Resistance of i^{th} resistor
R_c	Contact resistance
R_L	Load resistance
R_{off}	1. OTFT channel parameter 2. Transistor off-resistance
R_{on}	OTFT on-resistance
S	Sub-threshold swing, sensor sensitivity
T	Temperature
t_{clk}	Clock period
V_0	OTFT contact parameter
V_b	OTFT channel parameter
V_c	OTFT contact voltage
V_{dd}	Supply voltage
V_{diode}	OTFT contact parameter
V_{DS}	Drain-source voltage
$V_{g,min}/V_{00}$	OTFT contact parameter
V_{GS}	Gate-source voltage
V_{high}	Inverter high output voltage level
V_{low}	Inverter low output voltage level
V_M	Average voltage
V_{PP}	Peak-to-peak voltage
V_{RF}	RF voltage
V_{SS}	OTFT channel parameter
V_T	Threshold voltage
V_{Tn}	n-type threshold voltage
V_{Tp}	p-type threshold voltage
V_{trip}	Inverter trip point
W	Nominal channel width
W_{eff}	Effective channel width
W_p/W_n	Ratio of the width of p-type to n-type OTFTs in an inverter
γ_c	OTFT contact parameter
γ_t	OTFT channel parameter
η	OTFT contact parameter
σ	Standard deviation
τ	Time constant

1 Introduction

The concept of “ambient electronics”, referring to electronics embedded extensively in common environments, has emerged in recent years. Embedding intelligence in surfaces such as walls, ceilings, clothes, and packages will improve safety, security, and convenience in everyday life [1]. We will refer to these novel applications as “smart systems-on-foil”. Such systems require characteristics that are not met by silicon-based technologies, for example mechanical flexibility and large-area integration at a low cost. The standard crystalline and amorphous silicon technologies require high processing temperatures which are incompatible with flexible surfaces [2]. The possible alternative solutions, such as the thin chip technology [3] and substrate transfer from silicon-on-insulator wafers[1] [4], currently require a fabrication procedure that is not suitable to large-area applications, is complex and, hence, costly. Therefore, there is a growing need for technologies to build electronics with different characteristics from what mainstream silicon technology provides.

Since organic semiconductors allow for low-temperature processing, organic-based devices can be implemented on substrates such as plastic sheets, papers, and cloth [1]-[2]. In addition, some organic materials in solution can be deposited and patterned with conventional graphic art printing processes, promising a simple, fast, and low-cost fabrication flow [5]-[11]. Being flexible and able to cover large areas, organic electronic circuits could be unobtrusively integrated on ambient surfaces and consumer goods.

Though mature organic technologies usually comprise only p-type transistors, in recent years complementary organic transistors have also been developed [12]-[18]. This advancement makes organic technologies more suited for implementing complex circuits, due to the intrinsic lower operating voltage, higher speed, and higher robustness provided. The availability of both p-type and n-type transistors with relatively high performance and stability is an important advantage of organic technologies compared to the low-temperature oxide-based technologies such as [19]

[1] A thin film of Silicon is built on an layer of oxide lying on a thick silicon substrate, later removed by subtracting methods

and [20] which lack p-type transistors.

All the above-mentioned features make complementary organic technology an appealing platform to attain the aims of ambient electronics through smart systems realized on plastic foils, or systems-on-foil. The ability to integrate on the same substrate all the functionalities to realize a complete system is the differentiating advantage of complementary organic electronics.

1.1 Organic circuits: state of the art

Organic smart systems-on-foil need to acquire data from the environment or from digital sources, perform the required data conversion and analysis, and store, display, or transmit the collected data. Some of these functions have been already achieved in several implemented applications, while others are more challenging for organic electronics to accomplish. The implemented applications and the challenges and progress are discussed in the following sections.

1.1.1 Implemented applications

Basic functions based on organic electronics have been shown in several research works, including e.g. backplane matrices for displays [21]-[25], light emission and detection [26]-[29], mechanical and thermal sensors [30]-[34], and actuators [35]-[36]. In addition to these functions, several digital and analogue circuits need to be realized in organic technologies in order to minimize the need for hybrid integrations with silicon chips and keep cost low. These circuits, for instance, should provide analogue signal conditioning interfaces, perform data conversion, control the data flow, and restore synchronization. To give a more specific example, radio-frequency identification (RFID) tags which can interface sensors and actuators are the focus of a considerable part of organic electronics research. After first demonstration of a capacitively-coupled organic RFID tag working at 13.56 MHz [37], more complex versions have been shown. For instance, in [38] an inductively-coupled 64-b RFID tag was presented, and in [39], a 128-b tag has been discussed, which incorporates Manchester encoding and an anti-collision protocol.

First organic analogue to digital converters (ADCs) and digital to analogue

converters (DACs) were shown in [40]-[42] and [43]-[44], respectively. These data converters implemented in different technologies employ various architectures to tackle the resolution and linearity challenge. For example, [40] adopts a delta-sigma structure and reaches a signal to noise and distortion ratio (SNDR) of 24.5dB. The 6-bit ADC in [41] has a successive-approximation-register (SAR) architecture with a maximum integral nonlinearly (INL) of 0.6 LSB and 3 LSB with and without calibration (off-chip SAR logic). In [42], a simple VCO-based structure is used to achieve an INL of 1LSB at the same resolution (6 bit), without using any calibration. In all cases, the circuits are very slow and only suitable for quasi-static signals. A DAC is discussed in [43] with a C-2C architecture comprising only twenty organic thin-film transistors (OTFTs) and seventeen capacitors. In [44], 129 OTFTs are used to realize a current-steering DAC. Due to the use of OTFTs instead of capacitors, the current-steering DAC is more than 50-times smaller and three orders of magnitude faster than the C-2C DAC. At 6-bit resolution, the maximum INL is 1.16 LSB for the former and 0.8 LSB for the latter.

In the digital domain, different line-select drivers for displays based on OTFTs were realised in [45]-[47]. Specifically, the 240-stage shift register in [47] achieves a complexity level of more than thirteen-thousand transistors. In addition, an 8-bit microprocessor was implemented in [48]. The microprocessor can execute user-defined programs at an operation speed of 40 instruction-per-seconds. Recently, Inkjet printing techniques were used in [49] to implement a 8-bit RFID transponder comprising p-only inverters and NANDs with almost 300 OTFTs.

Most of the state of the art presented above is related to p-type only technologies. In recent years, several methods have been exploited to integrate complementary transistors after first demonstrations of stable n-type organic. In [7], solution-based techniques such as spin coating are used together with photolithography to realize a CMOS RFID transponder chip mostly composed of digital circuits. The 48-stage shift register in [14] is implemented by evaporating p- and n-type organic semiconductors with a coarse shadow mask. The SAR ADC in [41] is based on transmission-gates (TGs) which are manufactured using a similar approach. Ultra-fine shadow masks are employed in [15] and [16] to fabricate complementary logic circuits with a few

hundreds of transistors. Circuits with lower number of transistors are also implemented using direct inkjet printing[2] [17]. In [10], a complementary organic technology based on screen-printing[3] techniques is shown, with typical mobility of around 0.02 cm²/Vs for both p- and n-type OTFTs. Ultra-low-voltage logic gates [12] and high-speed ring oscillators [13] have also been realized using complementary organic technologies.

Hybrid complementary TFT-based technologies have also been developed in recent years [50] incorporating p-type OTFTs and n-type solution-processed metal-oxide TFTs. This technology has been used to implement circuits on flexible substrates, such as a bidirectional RFID tag [51] and a microprocessor [52] with an architecture similar to [48], but much faster thanks to the complementary technology with a good balance in the mobilities of p-type and n-type TFTs.

Table I summarizes the characteristics of a representative set of implemented organic circuits. It is worth noting that many of the circuits are implemented in p-only technologies due to the scarcity of a stable and robust complementary process. In addition, in the implementation of all these circuits lithographic-based techniques were used. A few of these circuits are shown in Figure 1.

1.1.2 Challenges and progress

Despite all the advancements described, various intrinsic and extrinsic characteristics of organic technologies limit the level of complexity and performance in the circuits. Organic electronic generally aims at applications that do not require high performance, e.g. ambient temperature monitoring and display drivers. Nevertheless, to be able to play a substantial role in future electronics, organic circuits need to communicate with silicon-based circuits based on certain standards. Therefore, specific requirements such as high-frequency (HF) rectification or low-voltage functionality are inevitable at times [53]-[54].

[2] The material in solution is used as “ink” in an inkjet printer to form droplets using techniques such as thermal or piezoelectric drop-on-demand (DOD) [130].

[3] The ink is pushed through a screen comprising a fine mesh. The pattern is defined by filling certain openings of the mesh with a stencil material [129].

Table 1. List of applications implemented based on organic circuit

Ref.	Circuit	Technology	#Tran.	Year
[14]	Shift register	Complementary	864	2000
[45]	Shift register	p-only	1888	2004
[46]	Display driver	p-only	≈4000	2005
[37]	Capacitive-coupled RFID tag	p-only	1938	2007
[38]	Inductive-coupled RFID tag	p-only	≈420	2008
[7]	Transponder chip	Complementary	168	2009
[39]	RFID tag including anti-collision	p-only	1286	2009
[43]	C-2C DAC	Complementary	22	2009
[15]	Decoder	Complementary	≈200	2009
[40]	Delta-sigma ADC	Dual-gate p-only	≈70	2010
[41]	SAR ADC (the logic is off-chip)	Complementary	53	2010
[16]	AC power-meter	Complementary with floating gate	609	2011
[44]	Current-steering DAC	p-only	129	2012
[48]	Microprocessor	Dual-gate p-only	3381	2012
[42]	VCO-based ADC	Dual-gate p-only	N.A.	2013
[48]	Shift register	Dual-gate p-only	13440	2014

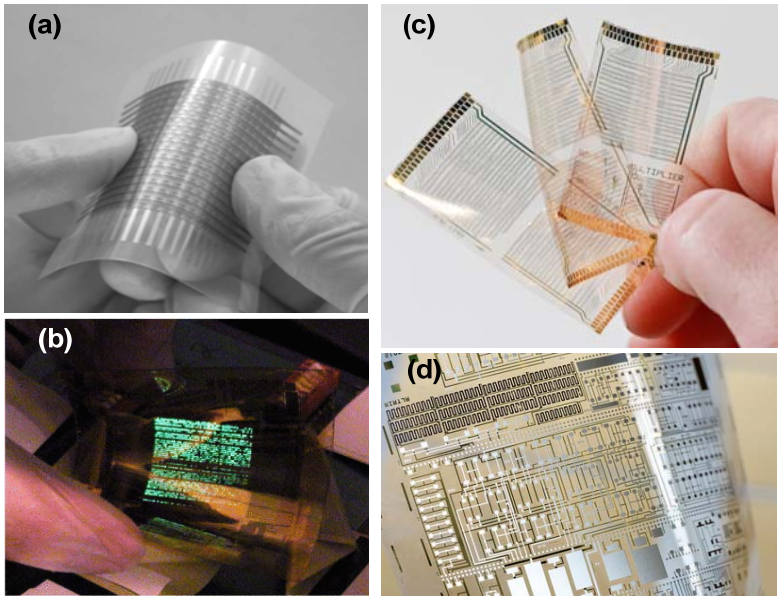


Figure 1. Some applications implemented using organic technologies: (a) artificial skin based on a matrix of organic sensors [34], (b) all-organic integrated flexible display [22], (c) microprocessor on foil [48], (d) ADC and other ICs on foil.

Typically the mobility (μ) of OTFTs is in the order of 0.1 cm^2/Vs and does not surpass 0.5-1 cm^2/Vs. This characteristic, along with a typical minimum feature size of several microns and large overlap parasitic capacitances, limit the speed of organic circuits. For instance, the microprocessor in [48] works at a clock frequency of 40 Hz, and the sampling frequency of the delta-sigma ADC in [40] is 500Hz. There have been many efforts to achieve OTFTs with high field-effect mobility, reaching around 10 cm^2/Vs for p-type [55] and 1 cm^2/Vs for n-type [56]. In addition, submicron OTFTs with minimum channel length of 0.8 μm have been implemented using high-resolution silicon masks [57]. Some techniques to reduce the parasitic overlap capacitances in printed OTFTs have also been investigated. For example in [58], thanks to the self-alignment of layers in inkjet-printed OTFTs, the registration errors and, thus, the parasitic capacitances are substantially reduced. However, the use of high-precision or un-conventional techniques for organic technologies can weaken or eliminate some attractive features such as low-cost and simplicity. The same holds when very high mobility materials are used, as these semiconductors are usually very crystalline small molecules which are hard to process.

In addition to low mobility, OTFTs may suffer from high threshold voltages (V_T), as in [10]. As a result, circuits based on these OTFTs function only at high supply voltages, making the realization of portable and battery-powered applications very cumbersome. This situation is exacerbated for circuits in unipolar[4] technologies which have intrinsically higher power consumption. In recent years several approaches have been developed to realize high-capacitance dielectrics at low temperatures, reducing the supply voltage of organic circuits considerably, especially in the case of digital circuits [53], [59]. In [43] and [44], the DACs are functional at voltages as low as 3 V, and the organic decoder in [15] works at 2 V. However, most applications realized in organic technologies till now use power supplies in the range of a few tens of volts [7], [14], [16], [38]-[42], [46], [48].

Another key factor limiting the complexity of organic circuits is the relatively high

[4] In this dissertation, the term “unipolar” is used for technologies incorporating only one type of transistor (p- or n-type)

variability in the characteristics of OTFTs [60], [61]. These variations result from the use of low-temperature and low-cost techniques which allow only limited control on the process. The global (large-area) and local (small-area) variations in the characteristics of the process lead to considerable deviations from the target device performance and thus in soft faults at the circuit level. In addition, the occurrence of defects during the process causes functional failures or hard faults. Environmental and bias instabilities also add to the parameter variations in some technologies. Such shortcomings are seriously limiting the complexity and performance of organic circuits, especially in case of unipolar technologies where the lack of n-type transistors further exacerbates the sensitivity to device variations. This problem becomes even more prominent in technologies employing printing techniques, due to the low degree of spatial correlation typical of printing processes, which translates in even worse matching and larger variability in the transistors. That is why circuits implemented based on printed OTFTs [5]-[10] are mainly limited to digital electronics or large-area switch matrices.

1.2 Role of complementary technologies

Currently, organic p-only technologies are the most reliable in terms of hard faults. Indeed, state-of-the-art p-only circuits have reached the complexity level of thirteen-thousand OTFTs [47], compared to a few hundreds OTFTs in complementary circuits. However, when complementary technologies become reliable enough to offer a comparable hard yield, the maximum circuit complexity will be limited by soft faults to which complementary circuits are far less vulnerable.

Due to the lack of n-type OTFTs, p-only logic gates mostly employ zero-V_{GS}[5] or diode-connected transistors as load [62]. The load transistor is thus permanently conducting, and the gates sustain very low switching speeds and/or high static power consumption. In addition, when load and drive p-OTFTs have the same V_T, the output pull-up and pull-down are unbalanced, leading to an asymmetric transfer curve and a very low noise margin. Therefore, digital circuits in single-V_T unipolar technologies are

[5] Zero-Gate-Source voltage. This kind of load is used only for technologies which provide normally-on (or depletion) transistors.

very sensitive to variability and suffer seriously from poor robustness. The circuit robustness can be increased by addition of an extra gate to each OTFT [63], [47]. The dual gate technology allows for tuning the V_T of transistors in order to have a more balanced pull-up and pull-down and, thus, an improved noise margin. In this case, an external biasing is needed to set the back-gate voltage.

In the analogue circuit domain, almost no well-known architecture in CMOS technology can be exploited in unipolar technologies. Unipolar OTFTs are typically normally-on, and being such, sink diode-connected transistors do not work in saturation [64]. Consequently, current mirrors can be used neither as an active load nor to provide reference bias currents [65], also meaning that auto-biasing cannot be realized. In addition, not only are transmission-gates (TGs) unavailable, but, due to the depletion characteristics of most p-only OTFT technologies, switches cannot be turned off without the use of charge pumps or external biasing. Therefore, switched-capacitor (SC) architectures are typically very cumbersome, or unpractical. Another disadvantage of unipolar technologies is the very limited input common-mode range of p-only amplifiers. Indeed, due to the different DC levels of the input and output voltages, cascading gain-stages does not lead to a large gain improvement [65], or necessitates large AC coupling capacitors, which have poor yield.

In summary, unipolar technologies impose many restrictions on circuit design, which can strongly limit the performance, robustness and practical applicability of organic electronics. This clarifies the role that complementary technology could play in facilitating the design and improving the robustness and performance of OTFT-based circuits. Indeed, complementary circuits provide a better power-delay product, intrinsically-lower supply voltage for a given threshold voltage level, higher noise margin, larger resilience to variability, and more design options (especially in case of analogue and mixed-signal design). Although dual-gate transistors can also improve circuit robustness, the development of crystalline-silicon CMOS technology teaches us that the use of a complementary technology is the most promising route to further improve the complexity of analogue and digital organic circuits.

The realization of a reliable and stable organic complementary technology, however, is hampered by technical challenges at the process level. For instance, air-

stable and high-mobility n-type organic semiconductors are not widespread. In addition, the organic material deposited first can easily degrade when it is exposed to the processing steps related to the second material [7]. In general, the added complexity of the complementary process increases the probability of hard faults. That is why a mature complementary organic technology is not yet available and, as depicted in Table I, the most complex applications based on organic circuits thus far have been realized in p-only technologies.

1.3 Problem statement

From the prior art discussed in Section 1.1, it is clear that, despite the potentials of organic technologies and their recent advancements, many challenges hinder the design and implementation of circuits based on OTFTs. OTFTs suffer from low mobility, large feature size, high threshold voltage, high variability, and environmental and bias instability. These characteristics unfavourably affect speed, gain, power, and yield of organic circuits as well as their level of integration and complexity. Therefore, the main challenge is to improve performance and robustness of organic circuits in order to enable implementation of the target applications.

1.4 Aim of the thesis

The aim of this thesis is to explore circuit and system design in complementary organic technologies. We focus on using the characteristics of complementary technologies to improve circuit performance and robustness, taking into account current-state drawbacks of these technologies such as immaturity and relatively large amount of defects. To achieve this goal, we study the characteristics of state-of-the-art manufacturing processes for complementary OTFTs and the modelling of these OTFTs. This knowledge allows us to carry out a technology-aware design procedure starting from devices and building blocks and reaching complete systems-on-foil. For doing so, we investigate the design at different abstraction levels including architecture, circuit, and layout. In addition, we do a study on the device-level parametric variability and its effect on circuit design. From a practical point of view, considering the challenges we are confronting to realize circuits in organic electronics, we specifically focus on the following aspects:

- Complementary digital circuit design to achieve high noise-margin and low-voltage logic
- Complementary analogue and RF circuit design to achieve performant and reliable circuits
- Design of mixed-signal systems-on-foil combining logic, energy scavengers, and reliable analogue circuits for sensing and actuating applications

1.5 Scope of the thesis

In this work, we focus on the design of three systems-on-foil in complementary organic technologies:

- A display driver
- An ADC for ambient temperature monitoring
- An RFID tag based on the so-called “silent tag” communication protocol[6]

These applications have been selected based on their industrial impact and are the lead applications of the Framework 7 European project “Complementary Organic Semiconductor Metal Integrated Circuits” (COSMIC).

Two technologies are used to implement the above applications, namely:

- A wafer-to-wafer technology (W2W)
- A sheet-to-sheet technology (S2S)

These technologies have characteristics that make them suitable for different types of applications and are discussed later in the thesis. The display driver is designed in W2W technology which is compatible with the current flat panel display (FPD) industry. On the other hand, the ADC and RFID tag are designed for the printing-based S2S technology. The designs are, thus, technology-aware, meaning that they take into account the specific characteristics of each technology. We discuss several digital and analogue building blocks tailored to the specific applications for each technology. Finally, we integrate the different building blocks in complex systems.

[6] A type of reader-talks-first protocol in which the RFID tag only sends a reply to the reader when it receives its unique identity code

1.6 Original contributions

This work advances in multiple ways the state-of-the-art of OTFT-based circuits and systems using two novel complementary technologies:

Wafer-to-Wafer (Lithographic technology)

- First-level statistical characterization of OTFT parametric variations
- Logic-style selection based on the specific characteristics of W2W technology
- Design and characterization of a display driver. The circuit works at the lowest supply voltage achieved by an organic line driver and it exploits the largest number of OTFTs in a complementary organic technology to-date

Sheet-to-sheet (Printing technology)

- First-level statistical characterization of Gen.1 and Gen.2[7] OTFT parametric variations
- Logic-style selection based on specific characteristics of the S2S technology
- Design and characterization of:
  - A dynamic flip-flop to reduce the area of printed logic (first experiment of printed dynamic logic)
  - A comparator exploiting input offset cancellation and achieving high accuracy (input accuracy ±50mV at 40V supply)
  - A resistor-based DAC (first printed DAC) achieving 7-bit linearity
  - HF rectifiers in Gen.1 and Gen.2 technology
  - The first ADC printed on foil
  - A temperature monitor system incorporating an ADC and a sensor on foil
  - Building blocks of an RFID tag on foil, including silent tag logic and power scavenging

The above achievements lead to:

[7] Two generations of S2S technology have been studied (See Section 2.2)

- A step-by-step advancement in the level of complexity of complementary organic circuits towards the implementation of systems-on-foil
- A platform to factually compare different state-of-the-art complementary technologies and explore what they can offer in comparison with unipolar technologies

1.7 Outline of the thesis

This thesis is divided in two main parts. Part I concerns the OTFT technology, modelling, and building block design addressed in chapters 2 to 5. Part II, including chapters 6 to 8, focuses on the implementation of three systems-on-foil.

Chapter 2 introduces the various fabrication methods, TFT architectures, and typical layout rules adopted by the two main technologies used in this work, namely S2S and W2W. The main differences between the two versions of S2S technology, designated Gen.1 and Gen.2, are also pointed out. The electrical characterizations and models of the S2S and W2W complementary OTFTs are described in chapter 3, after a qualitative description of the operation and performance of OTFTs. In addition, the parametric variations which were extracted and used for circuit design are presented in this chapter.

The design and experimental characterization of a large set of digital blocks in the S2S and W2W technologies are illustrated in Chapter 4. Chapter 4 also includes a comparison of different implementation styles (e.g. fully-static and dynamic) to help choose the architecture that fits better to the specific characteristics of each technology. In Chapter 5, we show the design and characterization of several analogue and mixed signal blocks tailored for applications targeted by the S2S technology. These circuits include operational transconductance amplifiers (OTAs), comparators, DACs, and rectifiers. Single-stage OTAs in the W2W technology are also presented in this chapter.

The illustration of systems-on-foil starts with chapter 6 which presents a line driver on foil and its tests with a flexible display in the W2W technology. Chapter 7 shows the design and characterization of an ADC and a sensor on foil, and the implementation and test of a temperature monitor based on the aforesaid circuits. A

printed passive reader-talks-first RFID tag based on the silent tag communication protocol is presented in chapter 8. Finally, conclusions are drawn in Chapter 9.

PART I

COMPLEMENTARY OTFT TECHNOLOGY, MODELLING, AND BUILDING-BLOCK DESIGN

2 Complementary OTFT Technology

In this chapter, we introduce the characteristics of the S2S and W2W technologies used in this work to implement different circuits and systems-on-foil. For each technology, we explain the process flow, the device configuration, and the typical layout rules. The knowledge of these characteristics is paramount to carry out a technology-aware circuit design.

2.1 Introduction

An OTFT consists of a stack of different thin layers deposited on a flexible substrate, such as plastic foil or paper. These layers form the source/drain (S/D) contacts, gate electrode, gate dielectric, and active layer (channel) of the TFT. Depending on the position of the S/D contacts and gate electrode with respect to the organic semiconductor (OSC), various TFT structures with some differences in their electrical performance can be realised.

As explained in the introduction, a variety of methods have been used to deposit and pattern the individual layers of complementary OTFTs. Examples include evaporation of organic semiconductors through coarse [14] or ultra-fine [15] shadow masks, and ink-jet printing [17]. In this work, two complementary organic technologies have been exploited, namely sheet-to-sheet (S2S) [66] and wafer-to-wafer (W2W) [67]. The S2S and W2W technological platforms concern different manufacturing modes in terms of toolset and materials, technology specifications, and foil size. The process in S2S technology is performed directly on 11×11 cm^2 sheets of plastic and is based on semiconductors in solution. The OTFTs are manufactured using screen-printing techniques. In W2W technology, the manufacturing process is based on evaporated semiconductors and is performed on plastic foils laminated on 6-inch wafer carriers. The employed photolithography techniques help to achieve highly integrated OTFTs with small footprints.

In Section 2.2 and 2.3, the various fabrication methods and TFT architectures adopted by S2S and W2W are illustrated, respectively. In addition, the typical layout rules for each technology are discussed. Section 2.4 summarises the highlights of S2S and W2W technologies.

2.2 Sheet-to-sheet (S2S) fabrication process

Some potentially attractive features of organic electronics, e.g. the high-throughput fabrication, are associated with the possibility to manufacture electronics using processes that are compatible with conventional graphic arts printing processes,

such as Gravure-printing[8] and screen-printing [5]-[11]. The interest in printed electronics is nurtured by the possibility to formulate organic functional materials like insulators, conductors and semiconductors in ink-like fluids that can actually be printed: printing organic technology could foster the widespread use of organic electronics applications for a substantial improvement in the quality of every-day life [8]. In the S2S technology, OTFTs and other components such as capacitors and resistors are implemented using screen-printing techniques. The manufacturing process is carried out in CEA-Liten, Grenoble, France.

Two versions of the S2S technology were utilised in this work, namely Gen.1 [10] and Gen.2 [66]. Both of these versions make use of organic compounds as semiconductor and dielectric materials, and are implemented by similar technological steps. However, the use of different materials and elaborated optimized processing steps improves the performance of Gen.2 OTFTs, at the expense of increasing the process complexity and potentially increasing the transistor variability. In the next subsections, first the general technological steps in S2S technology are described. Then, the main differences in Gen.1 and Gen.2 process flows are highlighted. Finally, the typical layout rules in S2S technology are presented.

2.2.1 S2S general process flow

Figure 2 shows the general process flow of the S2S technology [68]. The fabrication starts from a 125-µm-thick gold-plated Polyethylene naphthalate (PEN) substrate. First, the gold (Au) layer is patterned by laser ablation[9] to form the source/drain (S/D) electrodes and first layer of connections. The thickness of this layer is 30 nm, and the line/space resolution is 5 µm. In case of large-area circuits which need a high number of laser masks, the patterning of the gold layer could be performed by photolithography instead of laser ablation. All the next steps are carried out by printing-based techniques. The n-type OSC is first patterned by printing methods, defining patterns corresponding to individual devices. After annealing at 100 °C in

[8] A very high-throughput printing technique based on a metal cylinder with an engraved or etched pattern of cells which are filled with ink [129]

[9] Removal of material from the surface by irradiating it with a (usually pulsed) laser beam

normal atmospheric condition, the p-type material is deposited by screen printing. The thickness of the active layer is about 50-200 nm. At the next step, the common fluoropolymer dielectric (CYTOP®) is screen-printed and annealed to form an 800-nm-thick dielectric layer. The vias are left open to allow the formation of interconnections between gate and source/drain layers. Finally, a conductive silver (Ag) ink is screen-printed as the gate layer and second-level interconnections. A final annealing at 100 °C is also performed. The process registration of all printed layers is about ±25 µm. The final thickness of the stack is around 5 µm. The whole process fabrication is performed in air.

The cross section of the resulting top-gate bottom-contact OTFT is shown in Figure 3. It should be noticed that the top-gate approach, together with the fluorinated polymer used as dielectric, ensure a good protection of the semiconductor layers from environmental aggression, and that the OTFTs are stable in air for months.

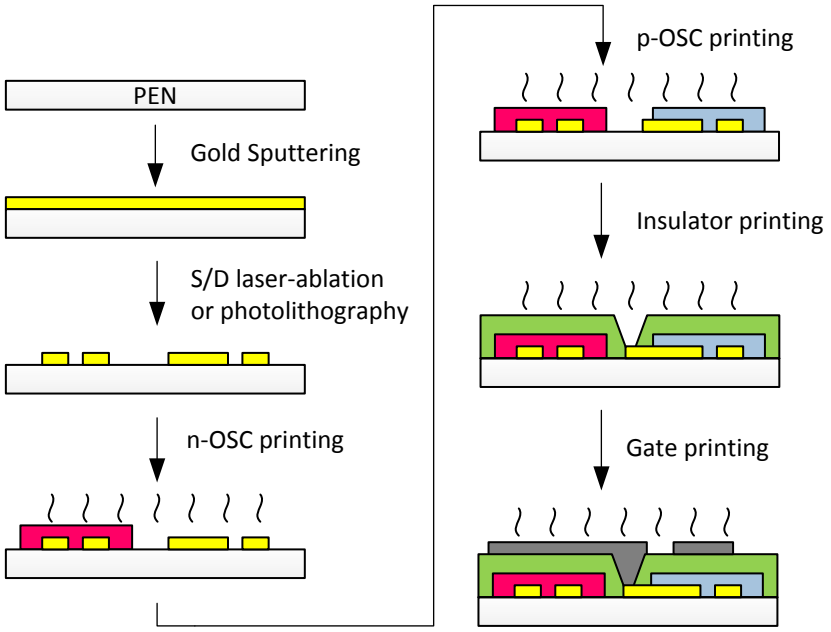


Figure 2. General fabrication process flow for S2S technology [68]

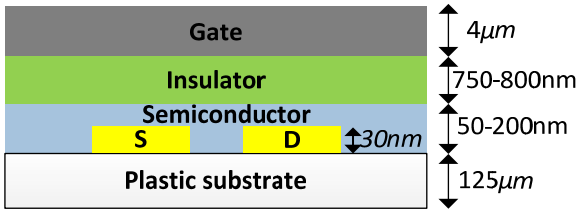


Figure 3. Cross section of the top-gate bottom-contact OTFT in S2S technology

2.2.2 Differences between Gen.1 and Gen.2 flows

Although both Gen.1 and Gen.2 follow the steps depicted in Figure 2, the type of used semiconducting materials is different. Gen.1 uses amorphous polymers which give thin, uniform and reproducible layers and lead to robust and reliable OTFTs. The typical mobility of OTFTs is 0.06 cm^2/Vs for n-type and 0.04 cm^2/Vs for p-type. In Gen.2, several approaches are adopted to improve the performance (especially the mobility) of OTFTs, including the use of micro-crystalline small-molecule semiconductors in solution. While Gen.1 employs a perylene diimide derivative as n-type and a polytriarylamine (PTAA) derivative as p-type OSC, in Gen2 a Polyera ActivInk® and TIPS-Pentacene are used as n-type and p-type OSCs, respectively. In addition, some treatments have been added to the flow in order to optimise the electrical injection from S/D contacts to the semiconductor and the morphology of the small-molecule semiconductor layers. As a result, Gen.2 OTFTs have a mobility of about 10 times better that Gen.1 OTFTs.

Figure 4 shows the process flow for Gen.2 [66], highlighting the operations which were added to each step. After the first steps regarding the patterning of S/D contacts, a self-assembled monolayer (SAM) is deposited to optimize injection of electrons from the contacts to the lowest unoccupied molecular orbital (LUMO) of the n-type OSC. After the n-type OSC is patterned by printing methods, the S/D electrodes and the PEN in p-type areas are cleaned by an O_2 UV-free plasma for 180 s to prepare the surface for the SAM deposition and p-type OSC printing. Then, as in Gen.1 flow, the dielectric is screen-printed and annealed, followed by screen-printing and annealing of the gate layer. The plasma surface treatment of PEN and gold electrodes in p-type areas is required to increase the wettability of the p-OSC on PEN and to improve the

injection of holes between the source/drain electrodes and the p-OSC. In the CMOS flow, the main issue is to ensure that the plasma treatment does not cause noticeable changes in the already-processed n-OSC. Experiments [69] show that a UV-free plasma treatment can sufficiently clean the surface without damaging the n-OSC. Resistors have also been integrated in this process. To form the resistors, a carbon ink is screen-printed right before printing the gate layer. The nominal resistivity is 35 kΩ/sq.

Detailed descriptions of the process flows, optimizations, and characterisations are given in [10] and [68] for Gen.1, and in [66], [68], and [69] for Gen.2.

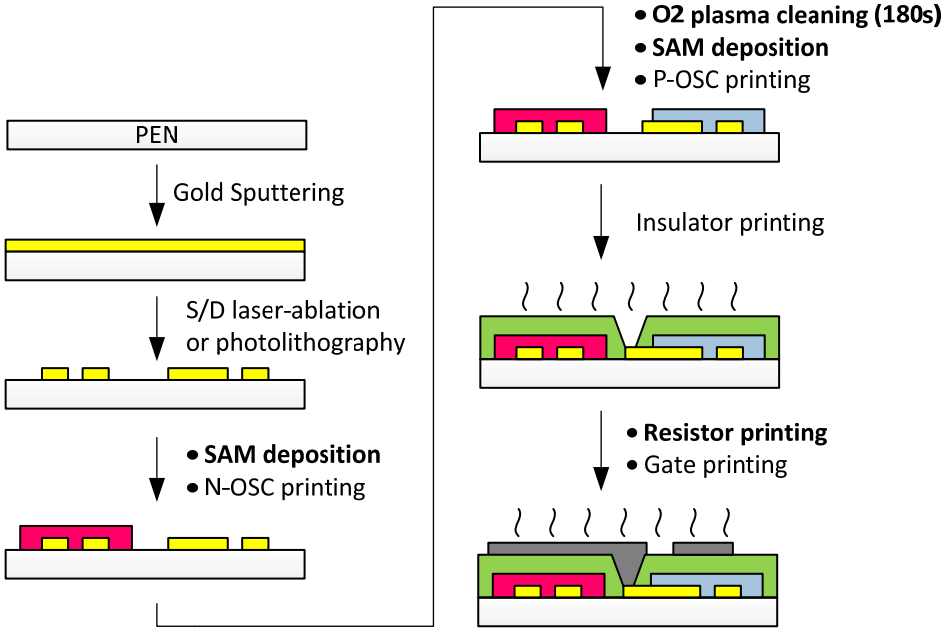


Figure 4. Fabrication process flow for Gen.2 S2S technology [66], the operations which are added to each step compared to the general process flow are bolded.

2.2.3 Typical layout rules

In general, the layout rules in organic technologies differ from those in silicon technologies. This difference is more substantial in case of printing-based technologies which considerably limits the control over the dimensions, both within a given layer, and at the level of registration among layers. These limitations typically

result in very large feature sizes compared to traditional lithographic approaches, even when a foil is used as substrate. In this section we describe some of the typical design rules. These rules have important effects on characteristics of OTFTs and on the area-consumption of the circuits.

Figure 5 shows the top-view of the transmission line model (TLM) and multi-finger (MF) OTFTs. The former has a more-accurately defined channel width and is used for transistor characterization, while the latter is more compact and is used in circuits. The number of channels (*n*) in this MF OTFT is two, and *W* is the nominal channel width. The minimum channel length (*L*) and finger width (*FW*) are normally 20 µm, but it is also possible to use channel lengths as short as 5 µm. Obviously, this comes at a risk of lower yield, since there is a probability of shorted S/D. The gate and OSC islands have the same size and position with respect to S/D fingers, meaning that there is no enclosure of gate on OSC. Since the OTFTs are normally-off (off at V_{GS}=0), the registration errors between gate and OSC layer are not expected to cause un-controlled conductive paths in the organic semiconductors.

It can readily be observed that the employed printing techniques impose a 400-µm overlap of Gate and OSC on S/D fingers and vice versa. This large overlap leads not only to a large transistor footprint, but also to very large overlap and channel capacitances. In addition, the regions of the OSC islands that extend beyond the edge of the fingers' tips can also contribute to the total current. As a result, the effective channel width (W_{eff}) is larger than the nominal width, *W*, shown in Figure 5.

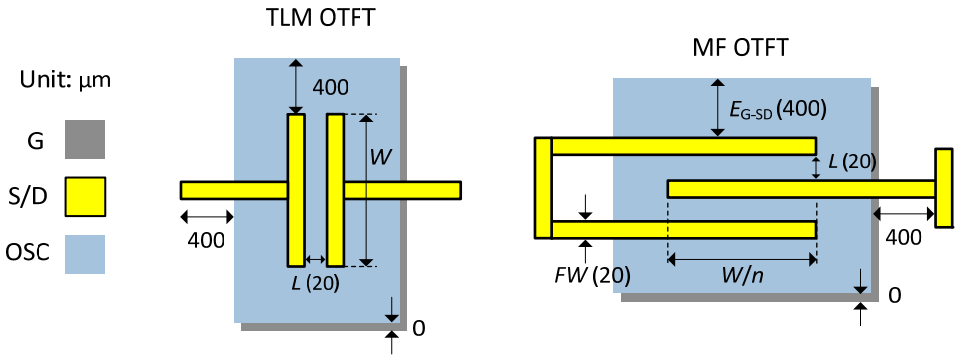


Figure 5. Layout of TLM and MF OTFTs in S2S (numbers are in µm)

Another important requirement of printing is the large distance between OTFTs. Indeed, in S2S technology the distance between OTFTs is 1000 µm. The initial design rule for distance between p- and n-type islands was 4000 µm (first designs), but after several checks it was changed to 1000 µm for the digital part of the design. The above rules imply that the footprint of an inverter in S2S technology is at least around 7 mm^2. In addition, the area consumption of circuits is a strong function of the number of transistors.

It is also worth mentioning that currently in this technology only two metal layers are available, namely S/D and Gate layers. Consequently, in circuits with high complexity, a large portion of the consumed area is devoted to routing. The area consumption could be remarkably reduced if additional metal layers were introduced to the technology.

2.3 Wafer-to-Wafer (W2W) fabrication process

As it is clear from the discussion in Section 2.2.3, a major issue in implementing organic complementary circuits is the integration level, which can be characterised by the area per logic gate. In complementary technologies, this area especially depends on the required spacing between complementary transistors. Using photolithography to pattern the semiconductors allows for closer and smaller p- and n-type islands and, thus, considerably higher level of integration. This technique is used in the W2W technology to realise highly-integrated transistors from evaporated organic semiconductors. The manufacturing process is carried out in Imec, Leuven, Belgium, in collaboration with HOLST centre in Eindhoven, The Netherlands.

2.3.1 Process flow

The W2W process, depicted in Figure 6 [67], is based on a foil-on-carrier (FOC) approach. The fabrication starts on a PEN foil which is laminated on a 6-inch silicon wafer. The layers for gate electrodes, gate insulator, and S/D contacts are patterned in sequence by photolithography. The metal and insulator materials are Ti-Au and Al_2O_3. The resulting metal-insulator-metal (MIM) stack has a thickness of about 160nm, with 30 nm for the metal layers and 100 nm for the insulator layer.

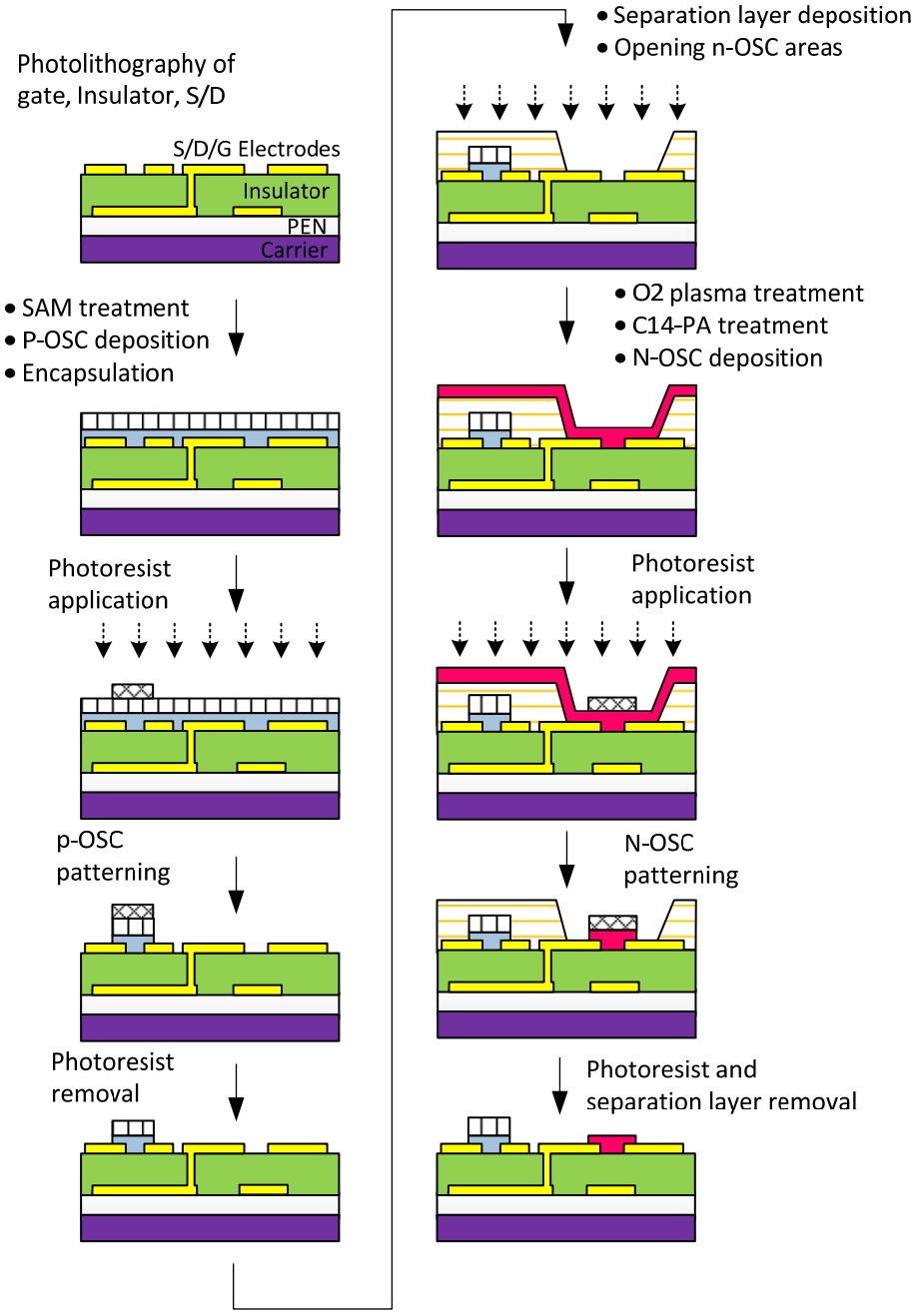


Figure 6. Process flow for W2W technology [67]

The MIM stack is then treated with pentafluorobenzenethiol (PFBT) in order to form a SAM on the gold contacts. Afterwards, a thin layer of poly(α-methylstyrene) (PαMS) is spin-coated on the substrate, to passivate the dielectric and improve the p-type semiconductor morphology. The p-type semiconductor is 3,9-diphenyl-peri-xanthenoxanthene (Ph-PXX), synthesised in-house and purified by thermal gradient sublimation. Ph-PXX is evaporated on the substrate at a substrate temperature of 68 ℃ to form a 30 nm layer.

At this step, in addition to the patterning of p-OSC, the sample needs to become ready for the steps regarding n-type TFT. The employed p-OSC has a high thermal and chemical stability, making the p-type TFTs perfectly suited to be processed first in the complementary integration flow. To further protect the p-type TFTs from the next cleansing, heating, and treatment steps, 200 nm of parylene-C is deposited as encapsulation layer. To create isolated p-type semiconductor islands and remove the extra p-type material, first a photoresist is applied to reduce the potential damage caused by patterning. After patterning the p-type active layers, a layer of fluorinated polymer is deposited everywhere on the substrate as separation layer. The separation layer can further reduce the damage of the following processes to the p-type active layer.

Subsequently, the n-type areas are opened by photolithography for the n-type active layer deposition. After applying oxygen plasma to clean the n-type areas, a n-tetradecylphosphonic acid (C14-PA) treatment is applied to improve the morphology and passivate the trap states on the dielectric. Then the substrate is transferred into a vacuum chamber for n-type material evaporation. N3004, provided by Polyera Corp., is evaporated on the substrate at a temperature of 120 ℃ to form a 30-nm-thick layer. After N3004 deposition, the n-type active layer is fully patterned by the photoresist technology. Remaining residues of photoresist and separation layer are removed by corresponding solvents.

The highest temperature in the flow is 120 ℃. Besides the thermal evaporation of p-type and n-type semiconductors, all the steps are done in ambient air condition. The process is similar to that of the current FPD industry [67], with minimum feature size of 5μm.

The cross-sections of the resulting p- and n-type OTFTs are shown in Figure 7. The advantage of this bottom-gate bottom-contact structure is that contacts are prepared before the deposition of organic semiconductor. Thus, the process is compatible with vacuum-deposited small-molecule organic semiconductors which form a structure sensitive to the following steps. On the other hand, the OSC layer is exposed to the atmosphere, making it vulnerable to the effects of humidity and atmospheric gases. That is why the OTFTs in W2W technology suffer from bias stress and threshold shift when measured in air. To overcome this problem, an appropriate passivation should be applied to the TFTs after the final process step.

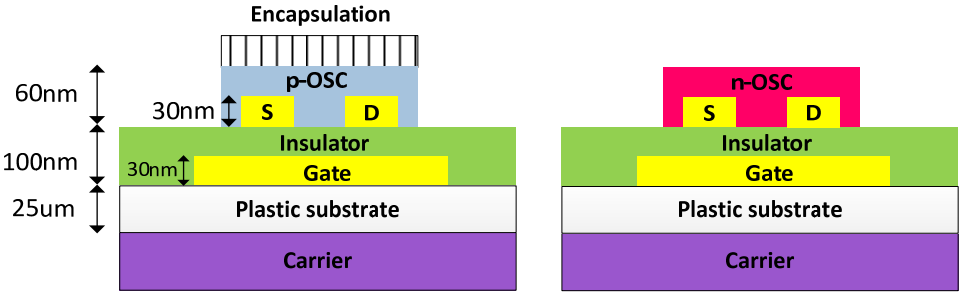


Figure 7. Cross-section of bottom-gate bottom-contact OTFTs in W2W

2.3.2 Typical layout rules

Figure 8 shows the top-view of a multi-finger W2W OTFT with, in this case, the number of channels (*n*) equal to two. The minimum channel length (*L*) and finger width (*FW*) are normally 5 µm, but it is also possible to use channel lengths as small as 2 µm at the risk of lower yield (shorted S/D). Three patterning masks, called well in Figure 8, have also been foreseen to enable future local encapsulation of p- and n-type OTFTs separately or together.

The overlap of OSC on S/D ($E_{OSC\text{-}SD}$) and Gate on S/D ($E_{G\text{-}SD}$) is 10 µm and 25 µm, respectively. The gate extends beyond the semiconducting island to prevent formation of a parasitic conductive path between S/D contacts in normally-on OTFTs [70]. As a result, major parts of source drain contacts are overlapping with the gate metal causing an increased parasitic overlap capacitance. The S/D fingers extend beyond the gate by 25 µm. As mentioned before, the semiconductor and gate islands are

relatively small. In addition, the OTFTs of any type can be placed as close as 60 µm to each other (this is possible mainly because of the vapour-deposition techniques exploited to deposit the semiconductors). Consequently, the footprint of an inverter in W2W technology is only 0.05 mm^2. However, a large portion of circuits' area is consumed again by routing due to the presence of only two metal layers.

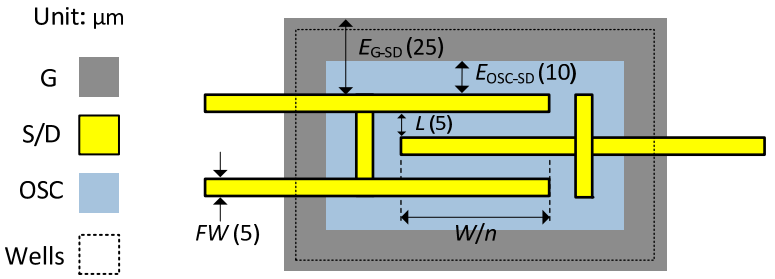


Figure 8. Layout of OTFTs in W2W technology (numbers are in µm)

2.4 Highlights of the S2S and W2W technologies

Table 2 summarises the highlights of the S2S and W2W technologies, both of which implement OTFTs and other components with low temperature processes on foil. The use of printing-based techniques in the S2S technology results in a simple and fast process compared to the lithographic-based W2W technology. An 11x11 cm^2 foil in S2S technology can be processed in up to one day, while the processing of the W2W 6-inch sample requires several days (still much shorter compared to silicon-based circuits). In addition, the W2W foil needs to be detached from the carrier carefully without damaging the circuits.

Table 2. Highlights of S2S and W2W technologies

Technology	S2S	W2W
Methods	Printing-based	Lithographic-based
Substrate	11x11 cm^2 plastic foil	Plastic foil on a 6-inch wafer
Inverter footprint	7 mm^2	0.05 mm^2
#Metal layers	2	2
Components	OTFTs, capacitors and resistors	OTFTs and capacitors
OTFT structure	Top-gate bottom-contact, staggered	Bottom-gate bottom-contact, coplanar

The above-mentioned characteristics of S2S technology make it a high-throughput and thus, low-cost technology, which may realize many breakthroughs foreseen for organic electronics. However, the large feature size, OTFT footprint, and the distance required between OTFTs which are necessitated by the printing methods employed result in a large are consumption and parasitics in the S2S technology. As mentioned before, the footprint of an inverter in the S2S technology is 7 mm^2, compared to 0.05 mm^2 in the W2W technology which can manufacture highly integrated OTFTs. The process in W2W technology is also compatible with the technologies used for flat panel display backplanes, and thus, is especially suitable for applications related to flexible displays.

A limiting factor in both technologies at the current state is that only two layers of metal are available and, as a result, the area consumption due to routing is remarkably high in complex circuits. Regarding the components available, S2S technology can manufacture resistors in addition to OTFTs and capacitors. The resistors can be used as highly linear components to improve the linearity of analogue circuits.

The S2S OTFTs have a top-gate bottom-contact structure, while W2W OTFTs are bottom-gate bottom-contact. Due to the characteristics of the structures, the S2S OTFTs are stable in air, while the W2W OTFTs need extra encapsulation layers to be stable. Based on the position of the channel formed in OTFTs, S2S and W2W OTFTs are considered staggered and coplanar, respectively. As explained in the next chapter, the energy barrier at the contact-semiconductor interface, which limits the carrier injection, is typically more dominant in coplanar OTFTs than in staggered OTFTs. More details about staggered and coplanar structures and the energy barrier are given in Section 3.2.

3 OTFT Modelling and Characteristics

Considering that a standard OTFT model is not established yet, in this chapter we give a brief explanation about the models used in our design. The operation of OTFTs in general is explained qualitatively and, for each technology, the models used to describe the OTFT performance are presented. The OTFT characterization masks designed for model parameter extraction are also described. We also summarize the typical model parameter values and the typical characteristics of OTFTs and give some characterization of OTFT variability.

3.1 Introduction

There are fundamental differences in physics and operation between OTFTs and Silicon MOSFETs. To design complex circuits in organic technologies, the specific behaviour of OTFTs should be taken into account. That is why having a physics-based compact model able to reproduce electrical characteristics of OTFTs is of paramount value.

Due to the wide range of fabrication approaches and materials, a “standard” structure and model has not been defined for OTFTs yet. Consequently, various compact analytical models have been developed, as reported in [71]-[78], to address the specific characteristics of given technology processes, e.g. materials and geometries. These OTFT models assume different charge carrier transport mechanisms in organic materials, including variable range hopping (VRH) [79] and multiple trapping and release (MTR) [80].

We designed mask sets containing hundreds of single devices in both S2S and W2W technologies. These OTFTs were used by modelling experts to characterise and model OTFTs. In this chapter, we show the models that were used in this work to design OTFT-based circuits, without giving the details of parameter extraction, which goes beyond the scope of this dissertation. In addition, we present the parametric variations which were extracted and used for circuit design. Section 3.2 explains the operation and performance of OTFTs, especially in comparison with Silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) which are familiar to circuit designers. Section 3.3 introduces the OTFT models used for design in S2S technology and gives details on the typical characteristics of S2S OTFTs and their parametric variability. The same details on model and characteristics for W2W technology are presented in Section 3.4. Section 3.5 summarises and compares the characteristics of the S2S and W2W OTFTs.

3.2 OTFT operation and performance

As opposed to the well-known Silicon MOSFETs, which use doped semiconductors and work in inversion[10], OTFTs normally utilise intrinsic semiconductors and work in accumulation. In a (p- or n-type) OTFT, the voltage applied to the gate-source (V_{GS}) (p- or n-type) accumulates carriers at the semiconductor-insulator interface creating a conducting channel (accumulation regime). In other words, the OTFT acts like a capacitor with capacitance C which at a given V_{GS} admits a certain number of carriers, CV_{GS}. When a voltage is applied to the drain-source (V_{DS}), the carriers that are free from the channel or channel-insulator interface traps contribute to the drain-source current (I_D). The OTFT turns off when V_{GS} is such that the channel area is depleted (depletion regime). Figure 9 shows where the channel is formed in staggered and coplanar TFTs (these words refer to the position of S/D contacts with respect to OSC and insulator, as shown in the picture).

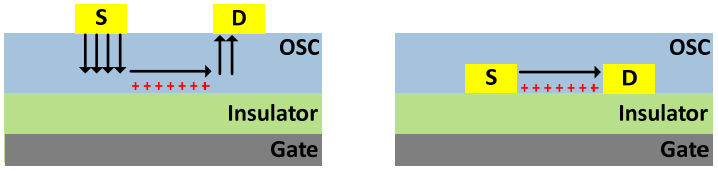


Figure 9: Channel formed in bottom-gate staggered (left) and coplanar (right) TFTs

The transfer characteristic curve of OTFTs resembles that of Silicon MOSFET. When a transistor is off, the drain current is limited to the charge leakage through the depleted semiconductor film or the gate insulator. In a MOSFET at zero V_{GS} the leakage through the Silicon semiconductor is due to two diodes biased in reverse polarization, and the high quality insulator (Silicon oxide) allows for extremely reduced leakage through the gate. This is not easily the case in OTFTs, which typically employ relatively leaky organic dielectrics. For these reasons, the off-current (I_{off}) in OTFTs can become comparably high, and I_{on}/I_{off} ratio is an important characterization parameter for OTFTs.

[10] The channel is comprised of minority carriers generated when the applied V_{GS} inverts the majority carrier population at the semiconductor-insulator interface.

When the transistor is turning on (V_{GS}>V_{onset}[11]), the drain current starts to increase due to the carriers that have sufficient thermal energy to overcome the V_{GS}-controlled energy barrier at the source contact [2]. This sub-threshold current is mainly due to diffusion and depends exponentially on V_{GS}. Its physical model is still very much under debate in literature at the moment [81]-[82]. The V_{GS} at which the current starts to increase above a given significant value, e.g. twice I_{off}, is called the onset voltage (V_{onset}). The sub-threshold swing[12] (S) in Silicon is determined by the ratio of the density of trap states at the channel-insulator interface (N_t) and the insulator capacitance (C_{ins}). In Silicon MOSFETs the density of the interface traps is very small and the semiconductor-insulator has a high quality interface, resulting in a close-to-ideal value (60 mV/decade) for S. On the contrary, large S values (e.g. several V/decade [69]) are typically measured in OTFTs.

For Silicon MOSFETs, the threshold voltage V_T is the minimum V_{GS} required to induce strong inversion. In OTFTs, which operate in accumulation rather than inversion, threshold voltage does not hold the same physical meaning [2]. However, it is still an important parameter to determine the operating voltage of a transistor. Several alternative methods have been explored for defining and measuring the OTFT threshold voltage [83]. In this work, and according to a common approach in the field of OTFT modelling [84], V_T is extracted from the OTFT measured characteristics using the same current-voltage relations as a Silicon MOSFET:

$$I_D = \frac{\mu C_{ins} W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \quad for\ |V_{GS} - V_T| > |V_{DS}| \tag{1}$$

$$I_D = \frac{\mu C_{ins} W}{2L}(V_{GS} - V_T)^2 \quad for\ |V_{GS} - V_T| < |V_{DS}| \tag{2}$$

in saturation and linear regime, respectively. V_T in this case is used as a parameter that

[11] Onset voltage

[12] The inverse slope of log(ID) in the sub-threshold region of the transfer characteristics graph

characterises the OTFT performance in the linear and saturation working regimes. It should be mentioned that, due to the dependence of OTFT mobility on applied gate voltage, the transfer characteristics typically deviate from quadratic behaviour. As a result, the threshold voltage value estimated using this method is not accurate. Other methods have also been developed to define and extract the threshold voltage for OTFTs. For example in [85], threshold voltage is the gate-source voltage at the boundary between the region where I_D-V_{GS} dependence is exponential (sub-threshold or weak accumulation region) and the region where the I_D-V_{GS} dependence is a power-law (above-threshold or strong accumulation region). This voltage marking the boundary of weak and strong accumulation regions is shown by V_b in this work.

The OTFTs' field-effect mobility μ, which is the other very important parameter to evaluate the OTFT performance, is also extracted based on Equations (1) and (2). The mobility in OSCs, however, is strongly dependent on the molecular arrangement in the solid state structures of the organic semiconductor, and also on temperature and applied V_{GS}. This is due to the charge transport mechanisms in OSCs, where the electronic wave functions are localised to a few or even individual molecules. According to the VRH model for charge transport [79], charge carriers hop between these localised states by quantum-mechanical tunnelling through energy barriers. Since the hopping is thermally activated, the mobility increases with temperature. The carriers accumulated due to the applied V_{GS} fill the lower-energy states. When V_{GS} is increased, the additional carriers will occupy sites with higher energy, requiring less activation energy to jump to neighbouring states. In other words, there the probability of hopping becomes higher and, as a result, the mobility increases with V_{GS}.

Another characteristic affecting the performance of OTFTs is the injection of carriers at the source and drain contacts [77], [86]. Here an energy barrier at the interface between the S/D contacts and the semiconductor, due to the misalignment between the work function of the contacts and the energy levels at which the carriers move in the semiconductor, limits the charge carrier injection. The voltage drop due to the injection barrier is often modelled with a reversed biased Schottky diode, or simply with a resistance between the contact and the channel called "contact resistance" (R_c). Other factors contribute to the contact resistance: among them the

presence of a non-accumulated semiconductor region between the contact and the channel, which is typical of staggered OTFT structures (Figure 9). On the other hand, as shown in Figure 9, in a staggered structure the whole S/D contact can contribute to the injection (wide contact area), while in a coplanar structure the injection can happen only through the contact edges (small contact area) [87]. On top of the small injection area, OTFTs with coplanar configuration also suffer from more structural disorder in the semiconductor film at the interface with the contacts, and thus, in general, show higher R_c. The presence of contact resistance typically leads to a nonlinear output curve at low V_{DS} values.

3.3 Modelling of S2S OTFTs

Since S2S technology is used not only for digital applications, but also for complex analogue and mixed signal circuits, the availability of an accurate model is of paramount importance. That is why the model for S2S OTFTs includes both channel and contact effects, though these OTFTs have a staggered structure and are thus less affected by parasitic contact resistances. In order to characterise OTFTs in S2S technology, we designed a mask set including hundreds of transistors as well as several capacitors and resistors. The 11×11 cm^2 foil, shown in Figure 10, was divided in 36 dies[13], four of which were allocated to alignment marks. Four other dies were devoted to resistors and test circuits including inverters and ring oscillators and the rest contained OTFTs with different channel lengths and widths. As it is explained in Section 3.3.1, the availability of transistors with a wide range of channel length (L) is critical for an accurate OTFT modelling. For this reason, we included TLM structures with L ranging from 5 to 400 µm. The MF OTFTs all have an L equal to 20 µm, which is the length used in almost all the designs, and channel widths (W) ranging from 500 to 8000 µm. The measured transfer and output characteristics[14] of these transistors were fitted by modelling experts to an accurate physically-based compact model [88]. We

[13] This division is required due to the characteristics of the employed laser ablation technique: the area of each "die" can be covered by one laser ablation mask (which has a limited size).

[14] Drain-source current versus gate-source voltage (transfer characteristics) and drain-source voltage (output characteristics)

added the effects of parametric variations to this model in order to enable statistical characterizations of circuits in different versions of the technology [89]-[91].

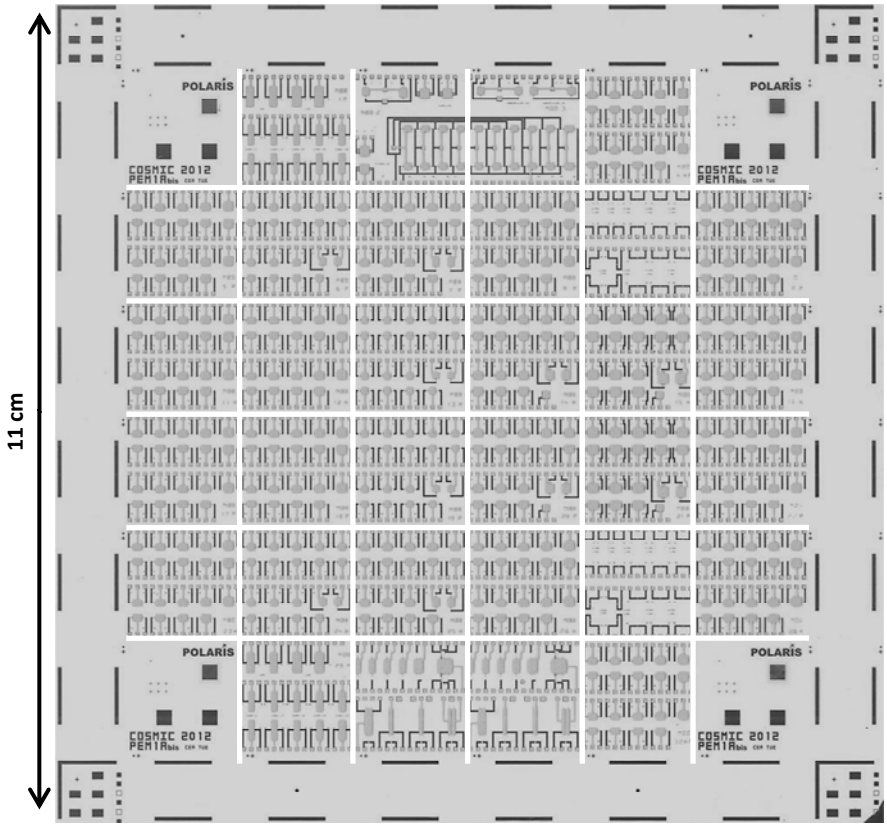


Figure 10. Picture of S2S device characterization foil (PEM1a). The white grid shows the division of dies

3.3.1 OTFT model for Gen.1

The OTFT model includes the channel and contact current equations (DC model), parasitic capacitance, and parametric variability.

DC model: The model for Gen.1 OTFTs [91] takes into account the channel behaviour and the contact effects. The channel transport is modelled based on VRH and assumes an exponential distribution of traps in the semiconductor. The drain current is a power law of the gate-source potential, which is in agreement with the electrical measurements of long channel transistors. The characteristic of long-

channel OTFTs is hardly affected by the energy barrier at the contact. When the transistor operates in accumulation, the current expression reads [73], [75]

$$I_{\mathrm{D}} = \frac{W}{L}\left[G_{\mathrm{t}}\left(V_{\mathrm{A}}^{\gamma_{\mathrm{t}}} - V_{\mathrm{B}}^{\gamma_{\mathrm{t}}}\right)\left(1 + \frac{V_{\mathrm{DS}} - V_{\mathrm{c}}}{L \times E_{\mathrm{p}}}\right) + \frac{V_{\mathrm{DS}}}{R_{\mathrm{off}}}\right] \tag{3}$$

where W and L are the channel width and length, respectively. V_{A} and V_{B}, which are described in Equations (4) and (5), define the relation of the drain current with the gate-source and drain-source voltages. V_c is the voltage drop at the source, caused by the injection barrier at the injecting contact. The other parameters, namely G_{t}, γ_{t}, E_{p}, and R_{off}, are used to fit the OTFT measured characteristics to the model, based on the physical understanding of the OTFTs. It was explained in the previous section that the field-effect mobility of OTFTs is dependent on both temperature and gate-source voltage. This dependence is described through parameters G_{t} and γ_{t}. γ_{t} is related to the disorder in the organic semiconductor, and the pre-factor G_{t} is a function of several physical and geometrical parameters including temperature T, energetic disorder, spatial charge localization, and gate-insulator capacitance C_{ins}. E_p takes into account the channel length modulation, and R_{off} considers the bulk current related to unintentional doping in the organic semiconductor.

In sub-threshold regime, the measured drain current increases exponentially with the gate voltage. Such behaviour could be attributed to deep trap states [92]. The above-threshold and the sub-threshold regimes are combined according to the interpolation function presented in [77]:

$$V_{\mathrm{A}} = V_{\mathrm{ss}} \ln\left[1 + exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{c}} - V_{\mathrm{b}}}{V_{\mathrm{ss}}}\right)\right] \tag{4}$$

$$V_{\mathrm{B}} = V_{\mathrm{ss}} \ln\left[1 + exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{DS}} - V_{\mathrm{b}}}{V_{\mathrm{ss}}}\right)\right] \tag{5}$$

where V_{SS} represents the sub-threshold slope, and V_{GS} and V_{DS} are the gate-source and drain-source voltages, respectively. V_{b} is the voltage marking the boundary of exponential region (weak accumulation) and power-law region (strong accumulation)

of the current curve and is associated with the semiconductor flat-band voltage[15]. In above threshold regime and for a device in saturation, the current relation can be re-written as:

$$I_{\mathrm{D}} = \frac{W}{L} G_{\mathrm{t}} (V_{\mathrm{GS}} - V_{\mathrm{c}} - V_{\mathrm{b}})^{\gamma_{\mathrm{t}}} \tag{6}$$

In Equation (6), the effects of the semiconductor bulk current ($\frac{V_{\mathrm{DS}}}{R_{\mathrm{off}}}$) and the channel length modulation ($\frac{V_{\mathrm{DS}} - V_{\mathrm{c}}}{L \times E_{\mathrm{p}}}$) are assumed to be negligible. From this formula, it can be readily observed that, as opposed to the Silicon MOSFET (Equation (2)), the I_{D}-V_{GS} relationship is not quadratic. As mentioned before, this is due to the dependence of the mobility on temperature and gate-source voltage. In addition, it is clear that the voltage drop at the injecting contact (V_{c}) may play an important role in the characteristics of OTFTs.

Electrical characteristics of p-type OTFTs with a channel length ranging from 200 µm to 20 µm scale with the transistor channel length, and are accurately modelled with Equations (3)-(5), assuming a zero V_{c}. This suggests that the channel transport is the dominant physical mechanism. On the contrary, the electrical characteristics of n-type OTFTs do not scale with the transistor channel length. Indeed, the normalised drain current of a transistor with L = 20 µm is lower than that of a transistor with L = 200 µm. This experimental behaviour suggests that contact effects [86], [87] are limiting the current. The contact resistance in these transistors is mainly related to the limited injection at the source contact induced by the presence of a reversed biased Schottky diode, the conductivity of which is strongly modulated by the gate bias. The current injected by the source contact as a function of the gate-source voltage (V_{GS}) and contact potential drop (V_{c}) is modelled as in [93]:

[15] V_{b} corresponds to the semiconductor flat-band voltage in OTFTs with a high gate-insulator capacitance (C_{ins}), and in some works is considered as threshold voltage.

$$I_{\mathrm{c}} = I_{\mathrm{rev}}\left[1 - exp\left(-\frac{V_{\mathrm{c}}}{\eta(k_{\mathrm{B}}T/q)}\right)\right] \tag{7}$$

where

$$I_{\mathrm{rev}} = WI_{00}exp\left(\sqrt[4]{\frac{|V_{\mathrm{c}}| + V_{\mathrm{c}}}{2V_{\mathrm{diode}}}}\right)\left(1 + \left(\frac{|V_{\mathrm{GS}}| + V_{\mathrm{GS}}}{2V_0}\right)^{\gamma_{\mathrm{c}}}\right) \tag{8}$$

and η, I_{00}, V_{diode}, and γ_{c} are the contact parameters[16]. K_BT/q is the thermal voltage (0.026 V) and V_0 is 1 V. The electrical characteristics of n- type OTFTs are modelled as the series of an "ideal transistor" and a reverse biased Schottky diode. Therefore, p- and n-type transistors have the same channel model, while only for n-type transistor the contact diode is added. The schematic model is shown in Figure 11.

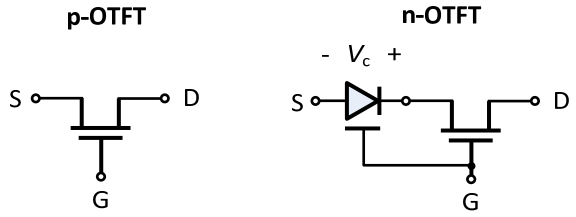


Figure 11. The schematic model for p-type (left) and n-type (right) OTFTs in Gen.1

Typical characteristics: Figure 12(a) and (b) show the measured (symbols) and modelled (lines) characteristics of n-type and p-type transistors with dimensions (W/L) equal to 1000µm/20µm [91]. The transfer characteristics (left panels) are given for two different V_{DS} of 1 V and 40 V, and the output characteristics (right panels) are shown for three different V_{GS}, namely 20 V, 30 V, and 40 V. In all the cases the model is in agreement with the measurements.

It is worth noting that despite the proven presence of contact effects in n-OTFTs, the low-V_{DS} output characteristic curve stills keeps a linear shape. However, the n-type OTFTs show lower saturation voltage ($V_{\mathrm{DS,sat}}$) than the p-type ones, even though the

[16] V_{diode} here is just a constant contact parameter and not the voltage across the diode.

parameter V_b (see Table 4) is nearly the same. This is due to the parasitic contact resistance, which causes a voltage drop at the injecting contact (source), thus reducing the overdrive voltage of the OTFT and lowering $V_{DS,sat}$. In other words, the threshold voltage V_T in n-OTFTs is higher than that in p-OTFTs.

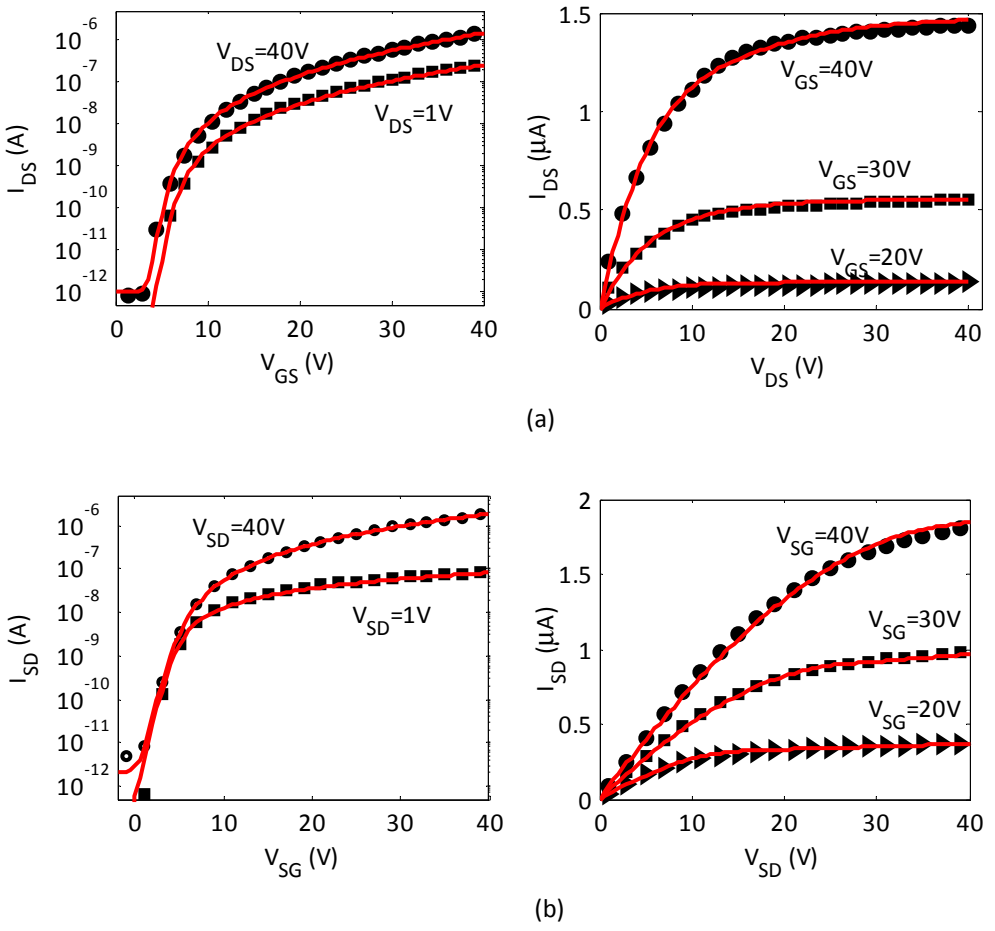


Figure 12. Measured (symbols) and modelled (line) transfer and output characteristics of (a) n-type and (b) p-type transistors with W/L=1000μm/20μm

Table 3 summarises the electrical characteristics of OTFTs on one foil made in Gen.1 S2S technology, reported in [10]. I_{off} is the minimum measured I_D, and I_{on} is I_D at $V_{GS}=2V_T-V_{onset}$ for transfer characteristics measured at V_{DS} equal to 1 V. V_T, calculated based on the classic extrapolation of the linear region (ELR) method, is typically around 14 V for n-OTFTs and 10 V for p-OTFTs. The typical value for μ_n and μ_p is

0.023 cm^2/Vs and 0.025 cm^2/Vs, respectively. The mobility is calculated from Equation (9) based on transfer characteristics in saturation.

$$\mu = \frac{2L}{WC_{\mathrm{ins}}}\left[\left(\frac{\mathrm{d}}{\mathrm{d}V_{\mathrm{GS}}}\sqrt{I_{\mathrm{D}}}\right)_{\mathrm{max}}\right]^2 \tag{9}$$

Table 3. Typical electrical characteristics of OTFTs in Gen.1 S2S technology [10]

	I_{off} (A)	I_{on} (A)	V_T (V)	μ (cm^2/Vs)
n-OTFT	2.8e-12	1.6e-6	14.1	0.023
p-OTFT	6.1e-12	1.9e-6	-10.3	0.025

Parasitic capacitances: The formula used for total capacitance (C_{tot}) of transistors is based on MF OTFTs capacitance measurements at different V_{GS} biases, while the source-drain terminals were shorted. The layout of a MF transistor with two channels (n = 2) is shown again in Figure 13 where L is the channel length, W is the total channel width, and $E_{\mathrm{G\text{-}SD}}$ is the enclosure of gate layer on S/D fingers. We included the following empirical formula in the model to calculate the parasitic capacitance of any MF transistor:

$$C_{\mathrm{tot}} = C_{\mathrm{tot}-0} + C_{\mathrm{ins}}\left(\frac{W}{n}\right)\left((n+1)FW + 2E_{\mathrm{G-SD}}\right) + C_{\mathrm{ins}}L\left[W + 2(n-1)E_{\mathrm{G-SD}}\right] \tag{10}$$

C_{ins} (insulator capacitance) is equal to 23.6 pF/mm^2. Figure 13 shows how each term in Equation (10) is attributed to different areas of the OTFT (hashed areas). $C_{\mathrm{tot\text{-}0}}$ is actually the parasitic capacitance of an OTFT island with channel length and width equal to zero and is obtained from experiment. The second term takes into account the W-dependant area when L=0. The third term is related to the channel area.

Since the transistors have a multi-finger structure, the calculated capacitance was divided between source and drain according to number of fingers at each side. It is worth noting that Equation (10) is valid only when the device is in the accumulation regime and at frequencies lower than 1 kHz. At these frequencies, $C_{\mathrm{tot\text{-}0}}$ alone is equal to 11 pF and is the dominant part of the capacitance for OTFTs with small W and L

(calculated C_{tot} for a W/L of 500/20 typically used in logic circuits is 17 pF). The parasitic capacitance decreases at higher frequencies (the semiconductor accumulation cannot follow anymore the voltage variations) and for frequencies higher than 3 MHz, the S/D-gate overlap capacitance is dominant (measured C_{tot} of around 4-5 pF for W/L of 500/20). [94] describes a more accurate and comprehensive but complex model for the OTFTs in the S2S technology. This model has not yet been included in computer aided design (CAD) environment.

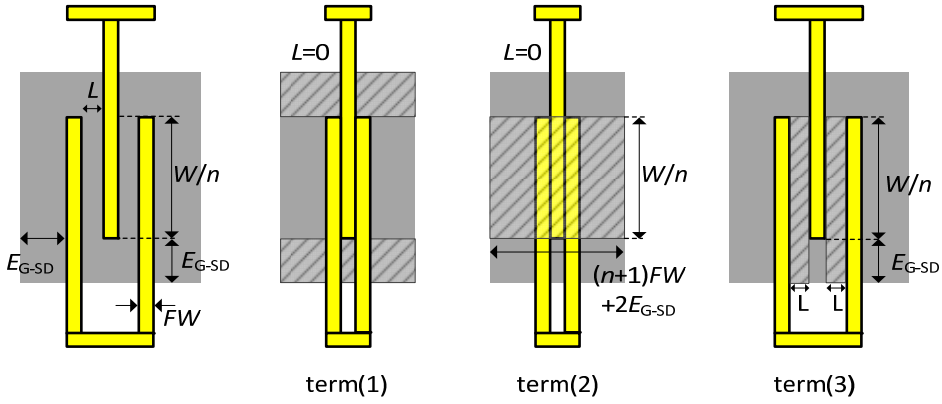


Figure 13. The layout of a S2S OTFT (left) and the area (hashed) attributed to each term of C_{tot} in Equation (10).

Variability: Because of the parametric variability in printed OTFTs, statistical characterization is crucial for having a reliable estimation of circuit functionality. Some research has been carried out to statistically characterise OTFTs in different technologies [95], but a comprehensive study of OTFT's variation and matching is lacking.

For Gen.1 transistors, the variability of four channel parameters, namely G_t, γ_t, V_b, and V_{ss}, was extracted from a set of measured devices [89]. These parameters characterize the transistor's electrical characteristics including mobility, threshold voltage, and sub-threshold slope. Table 4 summarises the nominal value of all the transistor parameters, and the standard deviation (σ) of the four channel parameters which were statistically characterised. We used these data to run Monte Carlo (MC) simulations based on uncorrelated Gaussian variations, within the limits derived from

the OTFT measurements [91]. The results of nominal and statistical simulations of fundamental circuits based on this model are presented in Chapters 4 and 5.

Table 4. The nominal value and standard deviation (σ) of Gen.1 OTFT parameters

		Channel Parameters						Contact Parameters			
		G_t (S/cm)	γ_t	E_p (V/μm)	R_{off} (Ω)	V_b (V)	V_{ss} (V)	V_{diode} (V)	η	I_{00} (A/ μm)	γ_c
n-OTFT	**Nominal**	7.75e-13	3.39	0.1	2e15	5.4	1	35	110	64.17e-16	3.5
	σ	2.73e-13	0.5	-	-	1.55	0.12	-	-	-	-
p-OTFT	**Nominal**	2.01e-11	2.01	10	5e14	-3.69	1	-	-	-	-
	σ	8.9e-12	0.1	-	-	0.3	0.13	-	-	-	-

3.3.2 OTFT model for Gen.2

The OTFT model for Gen.2 [88] is based on the same principles as Gen.1 explained in Section 3.3.1, and the formulas are very similar. Again, the model includes channel and contact current equations, the parasitic capacitance, and the parametric variability.

DC model: The channel current expression is close to Equation (3):

$$I_D = \frac{W_{eff}}{L_{early}}\left[G_t\left(V_A^{\gamma_t} - V_B^{\gamma_t}\right) + \frac{V_{DS}}{R_{off}}\right] \tag{11}$$

G_t, γ_t, and R_{off} are channel parameters (as defined for Equation (3)), and V_A and V_B are defined by Equations (4) and (5), respectively. L_{early}, equal to $L - (dL/dV_{DS})V_{DS}$, takes into account the increase of the saturated current with increasing V_{DS} (role of E_p in Gen.1 model[17]). dL/dV_{DS} is calculated from experimental data. W_{eff} is higher than the nominal channel width W, taking into account the effect of the transistors' layout on the transistor total current (see Section 2.2.3).

The electrical characteristics of neither p- nor n-OTFTs scale with the transistor channel length, suggesting the presence of a contact effect as in Gen.1 n-OTFTs (see Section 3.3.1). Both types of OTFTs are modelled as the series of an "ideal transistor" and a reverse biased Schottky diode, as shown in Figure 14. The contact current

[17] This difference in incorporating the channel length modulation effect is only due to the fact that the model was fitted using two different programs by different groups.

expression for Gen.2 OTFTs based on the reversed biased Schottky diode is:

$$I_{\mathrm{c}} = I_{\mathrm{rev}}\left[1 - exp\left(-\frac{V_{\mathrm{c}}}{\eta(k_{\mathrm{B}}T/q)}\right)\right] \tag{12}$$

where I_{rev} is calculated from:

$$I_{\mathrm{rev}} = WI_{00}exp\left[\left(\frac{|V_{\mathrm{c}}| + V_{\mathrm{c}}}{2V_{\mathrm{diode}}}\right)^{\alpha_{\mathrm{c}}}\right]\left(\left(\frac{V_{\mathrm{g,min}}}{V_{00}}\right)^{\gamma_{\mathrm{c}}} + \left(\frac{|V_{\mathrm{GS}}| + V_{\mathrm{GS}}}{2V_0}\right)^{\gamma_{\mathrm{c}}}\right) \tag{13}$$

and η, I_{00}, V_{diode}, α_{c}, $V_{\mathrm{g,min}}$, and γ_{c} are the contact parameters. $K_{\mathrm{B}}T/q$ is the thermal voltage (0.026 V) and V_0 is 1 V. The factor $exp\left[\left(\frac{|V_{\mathrm{c}}|+V_{\mathrm{c}}}{2V_{\mathrm{diode}}}\right)^{\alpha_{\mathrm{c}}}\right]$ takes into account the Schottky barrier lowering induced by the electric field at the source contact. The factor $\left(\frac{V_{\mathrm{g,min}}}{V_{00}}\right)^{\gamma_{\mathrm{c}}}$ is an empirical expression to fit the V_{GS}-dependence of diode reverse current.

Typical characteristics: The Gen. 2 technology characteristics have altered during the years that we carried out different design phases, due to the efforts to optimise the process flow. That is why we have used different values for model parameters during various design phases. Nevertheless, the more general electrical characteristics such as mobility and threshold voltage have not undergone dramatic changes. Table 5 summarises the electrical characteristics of OTFTs on one foil made in Gen.2 S2S technology, reported in [66]. The calculation of the parameters is based on what was explained in Section 3.3.1 for Gen.1 OTFTs. V_{T} is typically higher than V_{T} of Gen.1 OTFTs, around 18 V for n-OTFTs and 20 V for p-OTFTs. The mobility is more than two orders of magnitude higher, with μ_{n} of 0.55 cm^2/Vs and μ_{p} of 1.5 cm^2/Vs.

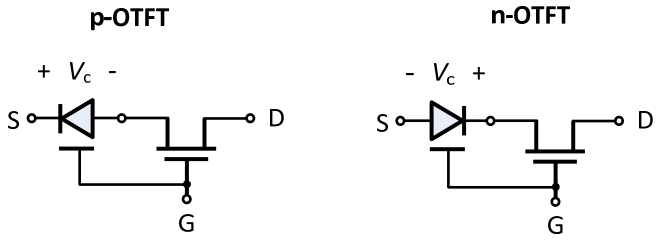


Figure 14. The schematic model for p-type (left) and n-type (right) OTFTs in Gen.1

Table 5. Typical electrical characteristics of OTFTs in Gen.2 S2S technology [66]

	I_{off} (A)	I_{on} (A)	V_T (V)	μ (cm^2/Vs)
n-OTFT	5e-14	1e-6	18	0.55
p-OTFT	2e-13	2e-6	-20	1.5

Parasitic capacitances: As Gen.1 OTFTs, Equation (10) is used to calculate the total capacitance of transistors.

Variability: In Gen.2 technology, the variations in channel parameters, namely G_t, γ_t, V_b and V_{ss} are calculated from long-channel transistors, assuming constant R_{off} and dL/dV_{DS}. From this analysis, G_t and γ_t show a correlation. The mean values of these parameters were used to extract the variations of the main contact parameters, namely η, I_{00}, V_{diode}, α_c, γ_c, from transistors with L equal to 20 µm. Table 6 summarises mean value (M) and standard deviation (σ) of the OTFT model parameters.

Table 6. The mean value (M) and standard deviation (σ) of Gen.2 OTFT parameters

	Channel	G_t (S/cm)	γ_t	dL/dV_{DS} (µm/V)	R_{off} (Ω)	V_b (V)	V_{ss} (V)
n-OTFT	*M*	1.62e-11	2.80	0.05	1e15	7.3	3.5
	σ	Correlated	0.1	-	-	2.7	2.0
p-OTFT	*M*	3.47e-9	1.76	0.05	1e15	-5.4	2.67
	σ	Correlated	0.1	-	-	1.8	0.69
	Contact	α_c	$V_{g,min}$ (V)	I_{00} (A/µm)	η	V_{diode} (V)	γ_c
n-OTFT	*M*	0.16	0.16	8.15e-14	32.8	0.4	2.48
	σ	0.013	-	2.4e-14	9.9	0.29	0.084
p-OTFT	*M*	0.36	0.16	5.86e-14	13.7	1.51	2.85
	σ	0.062	-	3.18e-14	7	0.90	0.28

The obtained data are used to run Monte Carlo (MC) simulations based on Gaussian variations, within the limits derived from the OTFT measurements and considering the correlation [89], [90]. The results of nominal and statistical simulations of the circuits based on this model are presented in Chapters 4 and 5.

3.4 Modelling of W2W OTFTs

For OTFT characterization in W2W technology, we designed a mask set including hundreds of transistors as well as several capacitors. The 6-inch wafer, shown in Figure 15, was divided in nine 3x3 cm^2 dies. The OTFT characterization block was repeated in all dies except one and included transistors with channel lengths ranging from 2 to 20 µm and channel widths from 70 to 1400 µm. Particularly, OTFTs with W/L equal to

70/5 and 140/5 were placed in different areas of each die. The same transistors were also placed in the scribe-lines in between the dies. Some test circuits such as inverters and ring oscillators were also included. We fitted the measured characteristics of these transistors to a model similar to that of the S2S OTFT's channel. We also extracted the variations of the threshold voltage and mobility in W2W OTFTs [96].

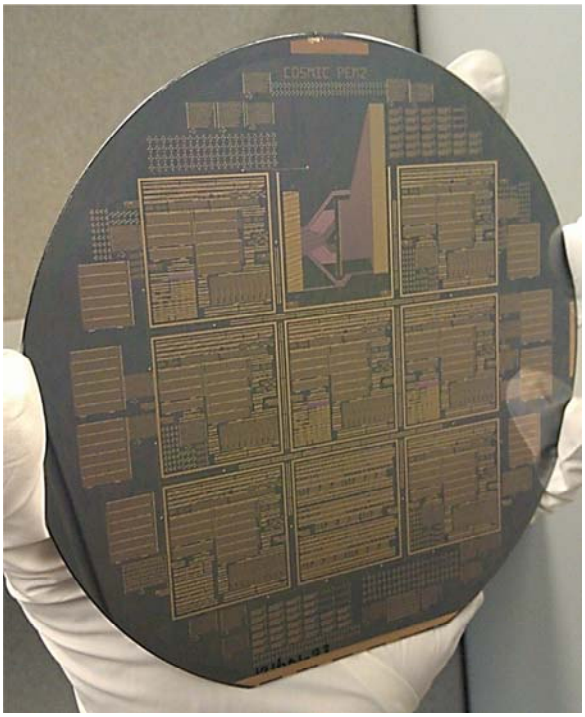


Figure 15. Picture of W2W characterization foil (PEM2)

DC model: the model for W2W OTFTs [96] takes into account only the channel behaviour. The current expression is defined by Equations (3)-(5) explained in Section 3.3.1, after removing the contact voltage drop (V_c). The parameters are G_t, γ_t, E_p, R_{off}, V_{ss}, and V_b, defined in Section 3.3.1.

It should be noted that, though it may be an issue in coplanar TFTs [97], the contact resistance has not been taken into account in the model used here. Therefore, the model is not very accurate when the transistor is biased in linear region or at high drain currents. Nevertheless, as it is shown in Section 4.3, the model gives a good estimation of the static characteristics of digital gates and accurately predicts the

stage delay. This makes the model accurate enough for the designs that will be made in the W2W technology, which are all digital.

Typical characteristics: Figure 16 shows the measured transfer characteristics (symbols) of twenty-four p- and n-type transistors with W of 140 and L of 5 µm, together with the simulated curves of the typical transistor (solid line) [96]. The measurements are performed at V_{DS} of 10 V (absolute value). Table 7 summarises the main electrical parameters of OTFTs on one die made by W2W technology [96]. Both μ and V_T are calculated based on the classic method mentioned in Section 3.3.1. The V_T of both p- and n-type OTFTs is around zero, and the typical value for μ_n and μ_p is 0.7 cm^2/Vs and 0.1 cm^2/Vs, respectively.

Parasitic capacitances: the formula used to estimate the total parasitic capacitance is same as Equation (10), replacing $E_{Gate\text{-}SD}$ with $E_{OSC\text{-}SD}$ (in this technology the organic semiconductor island is always enclosed within the gate area). For this technology, $C_{tot\text{-}0}$ has a negligible effect since the area it is attributed to (gate-semiconductor overlap for zero W and L) is much smaller than the total area. C_{ins} is 0.7 nF/mm^2, and the calculated C_{tot} for a W/L of 140/5 (typical size used in logic) is 13 pF.

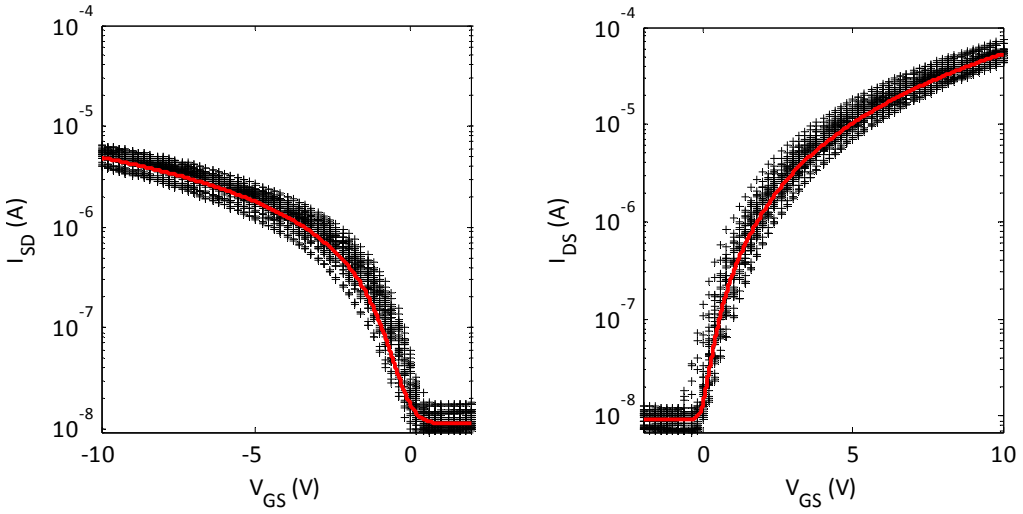


Figure 16. Measured transfer characteristics of twenty-four p-type (left) and n-type (right) transistors with W/L=140µm/5µm (symbols) and the equivalent model (solid line) at V_{DS}=10 V (absolute value).

Table 7. Typical electrical characteristics of OTFTs in W2W technology [96]

	I_{off} (A)	I_{on} (A)	V_T (V)	μ (Cm^2/Vs)
n-OTFT	1e-8	3.5e-5	0.5 to 1	0.7
p-OTFT	1.5e-8	4e-6	-0.3 to 0.3	0.1

Variability: We measured the transfer characteristics of forty transistors per type to study the parametric variability in W2W technology. The measured transistors are distributed on different spots of a 3×3-cm^2 die in five blocks (B1-B5). Each block contains sixteen transistors with L equal to 5 µm and W equal to 70 or 140 µm. To study the variation in OTFTs, we extracted the threshold voltage and mobility for each transistor [96]. Figure 17 shows the number of occurrences of different V_T values for all OTFTs, and Table 8 summarizes the mean value (M) and standard deviation (σ) of V_{Tp} and V_{Tn} over the whole die and in each block. We can observe that, considering the complete measurement population, V_{Tn} is much more variable than V_{Tp}. However, looking at the values of σ and μ in each block of transistors, we can see that the local variations in n-type OTFTs are comparable with that in p-type transistors. From Figure 17 it is also clear that there are occurrences of OTFTs with positive V_T for p-type and negative V_T for n-type transistors. As a result, the transistors could be normally-on (non-zero drain current at zero-V_{GS}). The same details about variations are provided in Figure 18 and Table 9 for μ. The typical mobility of p-type and n-type OTFTs on this die is around 0.1 cm^2/Vs and 0.7 cm^2/Vs, respectively. σ is around 5 to 25% in all cases, but n-type mobility is (in relative terms) slightly less variable than p-type.

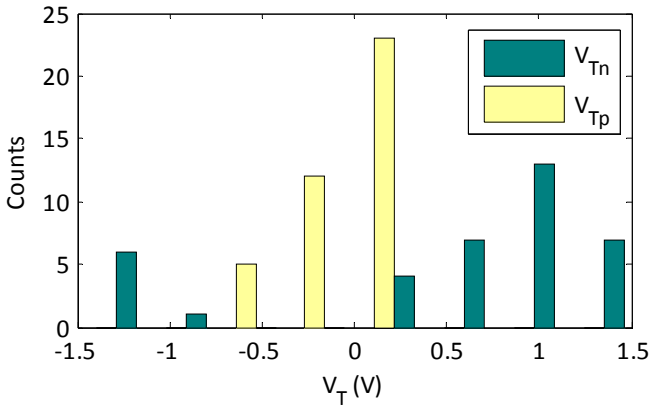


Figure 17. Number of occurrences for threshold voltage of forty p-type (V_{Tp}) and n-type (V_{Tn}) transistors on a W2W die

Table 8. The mean value (M) and standard deviation (σ) of V_{Tp} and V_{Tn} on the whole die as well as in each block of sixteen transistors (B1-B5)

		Die	B1	B2	B3	B4	B5
V_{Tp} (V)	M	0.05	-0.3	-0.1	0.2	0.2	0.3
	σ	0.30	0.20	0.20	0.18	0.14	0.15
V_{Tn} (V)	M	0.6	-1.1	0.5	1.0	1.5	1.0
	σ	0.96	0.58	0.21	0.18	0.36	0.18

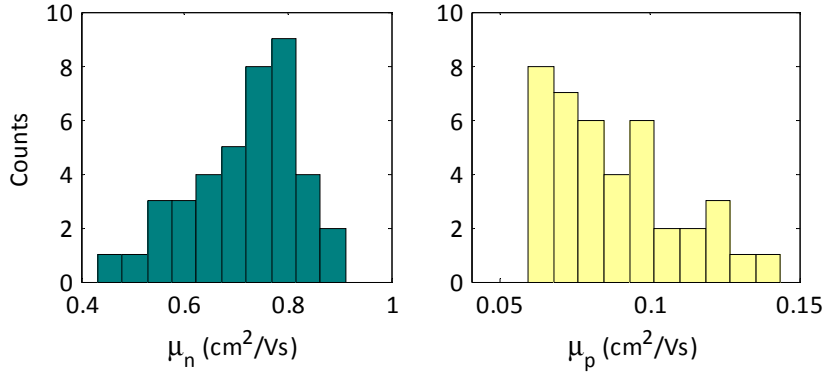


Figure 18. Number of occurrences for mobility of forty p-type (μ_p) and n-type (μ_n) transistors on a die.

Table 9. The mean value (M) and standard deviation (σ) of μ_p and μ_n over the whole die as well as in each block of sixteen transistors (B1-B5)

		Die	B1	B2	B3	B4	B5
μ_{Tp} (V)	M	0.09	0.07	0.11	0.08	0.08	0.10
	σ	0.02	0.02	0.02	0.02	0.01	0.03
μ_{Tn} (V)	M	0.72	0.79	0.75	0.74	0.57	0.75
	σ	0.11	0.08	0.11	0.05	0.07	0.06

3.5 Highlights of the S2S and W2W OTFT characteristics

The very different characteristics of S2S and W2W technologies, resulting from different fabrication techniques, make these technologies suitable for different kinds of applications. Nevertheless, it is possible to compare the characteristics of these OTFTs to understand the cons and pros of each one. Here we consider three important parameters including mobility, threshold voltage, and parasitic capacitance. In the following discussions, always the latest version of the S2S technology (Gen.2) has been considered, unless otherwise is mentioned.

The mobility of S2S OTFTs is in general higher than that in W2W OTFTs, but the

values are in the same order of magnitude. It is worth noting that as opposed to S2S technology and other common organic technologies, in W2W technology the n-type mobility is higher than p-type. The ratio of mobility for p-type to n-type OTFTs (μ_p/μ_n) is typically 1/7 in the W2W technology, compared to 3/1 in Gen.2 S2S technology (1/1 in Gen.1). Due to a more balanced mobility ratio, the dimensioning of logic circuits in S2S technology can be more balanced, as explained in Chapter 4.

Although C_{ins} is 30 times smaller in the S2S technology compared to that in the W2W technology (23.6 pF/mm^2 versus 0.7 nF/mm^2), the total parasitic capacitance of the minimum transistor size typically used in both technologies (W/L around 25-28) is in the same order of magnitude, and slightly higher for the S2S OTFT. This is due to the large feature size and other layout rules imposed by the printing technology which in total result in a lower speed in S2S technology, as illustrated in Chapter 4.

The threshold voltage is around 20 V for S2S OTFTs, compared to around zero or even lower (normally-on OTFTs) for W2W ones. In the following chapters (4 and 5), it is shown that how this characteristic affects the circuit design in each technology.

Another important highlight is the on-off ratio which is around three orders of magnitude better in the S2S technology compared to the W2W technology. The relatively high off current in W2W OTFTs is due to the charge leakage partly through the gate insulator (gate current in the order of several nA) and partly through the depleted semiconductor film.

4 Digital Circuit Design

This chapter gives a detailed description of digital circuit design in organic complementary technologies, both S2S and W2W. The design and characterization of several digital building blocks based on different architectures are shown. The characteristics of fundamental building blocks provide a platform to compare different technologies. In addition, the design consideration specific to each technology and the logic design style which suits best the characteristics of each technology are discussed. Among these circuits, the first dynamic gate and flip-flop ever manufactured in an organic technology are demonstrated based on S2S technology. In addition, a W2W 32-stage shift register is reported that has the highest transistor count in a complementary organic technology to date.

4.1 Introduction

The main challenge in digital design using organic technologies is the yield. As discussed in Section 1.2, complementary technology improves the soft yield remarkably by enhancing the robustness of logic gates to variability. The hard yield, however, remains a major problem. Indeed, state-of-the-art complementary technologies are still in the early development phase and have not reached the same low-defectivity level of unipolar technologies. While shift registers with more than 13k OTFTs are reported based on unipolar technologies [47], the highest transistor count reported in a complementary technology was till now 864 for a shift register working at 80 V [14] (before our work [96]).

In this chapter, we show the design and experimental characterization of a large set of digital blocks for S2S and W2W technologies. The kind of building blocks chosen for implementation, namely combinatorial gates and flip-flops (FFs), is tailored for organic electronics applications in general and the target applications of this dissertation specifically. The combinatorial gates and FFs together can build, for instance, shift-registers and code generators for display drivers and RFID tags. The design is performed based on the models reported in Chapter 3 and the related simulations are presented. For logic circuits in each technology, different implementation styles such as fully-static and transmission-gate based (TG-based) are discussed. In S2S technology, dynamic logic is also considered. For each implementation, first the characterization of single gates is illustrated and then more complex blocks, namely flip-flops (FFs), are shown. Finally, different implementations are compared in order to select the architecture that fits better to the specific characteristics of each technology[18].

Section 4.2 and 4.3 discuss the digital blocks in S2S and W2W technologies, respectively. Section 4.4 gives some final remarks on digital circuit design in these two technologies.

[18] The terms W2W and S2S refer to the specific wafer-to-wafer and sheet-to-sheet technologies used in this work and are not widely used acronyms.

4.2 Digital design in S2S technology

The concerns about yield in organic technologies become more prominent for printing technologies such as S2S in which the footprint of only one inverter is at least 7 mm^2. Since this large area consumption is mainly due to the layout rules for the spacing between OTFTs, it is paramount to achieve the desired function and performance using the lowest possible number of transistors.

The applications in S2S technology we are focusing on are ADCs and RFID tags. For tasks such as data comparison and synchronization we need combinatorial as well as sequential logic. For example, both the counting ADC (discussed in Chapter 7) and RFID tag (discussed in Chapter 8) use counters. We start from fully-static blocks in Section 4.2.1, and then explore transmission-gate (TG) and dynamic architectures in Sections 4.2.2 and 4.2.3, respectively. Section 4.2.3 shows the first reported dynamic logic in an organic technology [89]. In each section, we first focus on single combinatorial gates like inverters and NANDs and then proceed with flip-flops (FFs) as the basic memory elements needed to build sequential logic. Finally, we do a comparison between the different architectures in Section 4.2.4.

We designed six mask sets containing our different circuits in S2S technology. The level of circuit complexity increased in each design compared to the previous one, starting from single devices on foil (PEM1a, Figure 10), going to several building blocks and, finally, complete systems-on-foil. Figure 19 shows the second designed foil (PEM1b) containing most of the digital building blocks that are discussed in this chapter.

Figure 20 shows how the building blocks were measured using a probe station and DC quadrant probes. We used two probe-combs, each comprising fourteen probes with 1 mm pitch. The pad landing area was 500x500 μm^2. The DC measurements were performed by an Agilent 8-slot Precision Measurement Mainframe (E5270B). The AC signals were generated using arbitrary waveform generators and checked by a 4-channel mixed signal oscilloscope. All the measurements were performed in air.

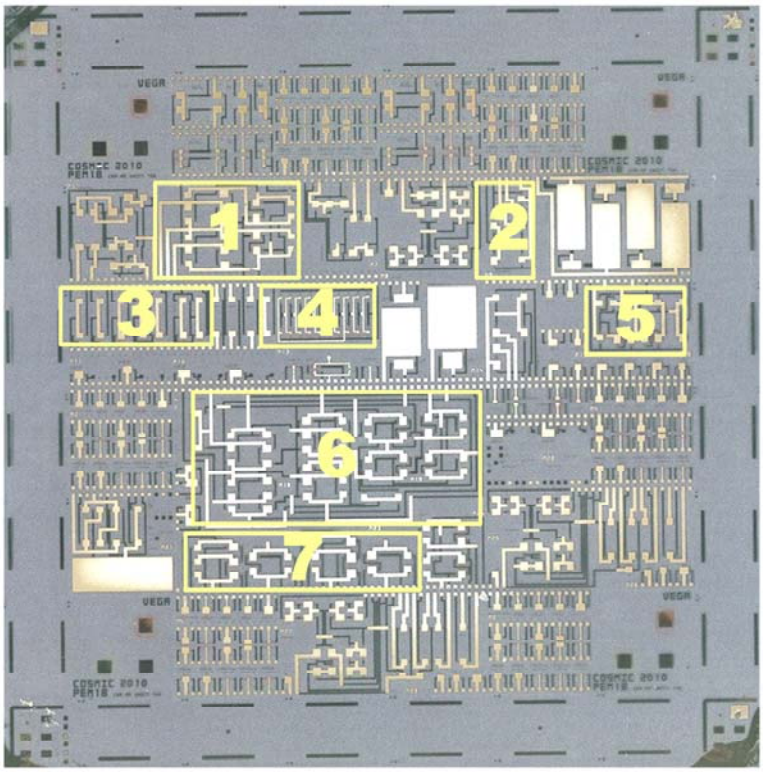


Figure 19. Picture of the foil containing several building blocks (PEM1b). Digital blocks are individually shown: 1. JK-FF, 2. Dynamic NAND, 3.Inverters, 4. Ring oscillator, 5. TSPC (dynamic) FF, 6. MS (fully-static) FF, NAND/NOR gates.

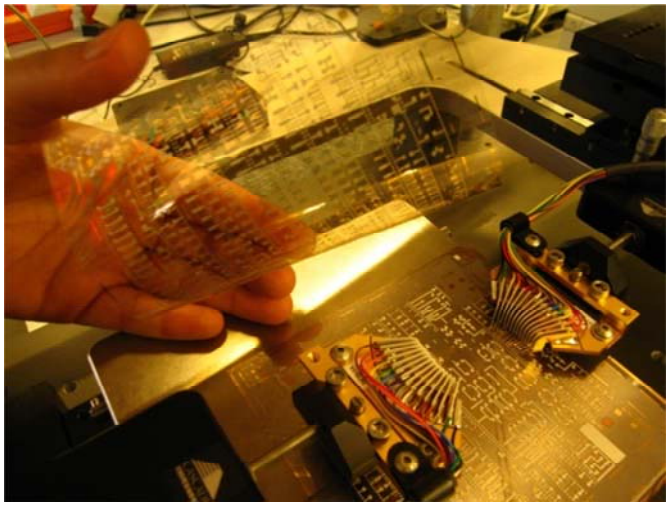


Figure 20. Measurement of S2S foils using a probe station

The S2S digital circuits are usually functional at supply voltages of 10 V or higher. However, to be compatible with analogue circuits which are functional only at higher voltages (see Chapter 5), most of the measurements are shown at V_{dd} equal to 40 V. All the results are related to circuits processed in Gen.2 technology process, except when Gen.1 is clearly mentioned (See Section 2.2.2 for Gen.1 and Gen.2 processes).

4.2.1 Fully-static blocks

Fully-static blocks such as inverters are usually used as indicators of the functionality and performance in a certain technology. In this section we explore the characteristics of fully-static circuits including single gates and FFs in S2S technology.

4.2.1.1 Single gates

The single gates discussed here include inverters and NAND/NOR gates.

Inverters: Important static characteristics of an inverter include the output voltage levels (V_{high} and V_{low}), the trip point (V_{trip}), and the maximum gain (G_{max}). The dynamic performance is usually characterised through the stage delay in ring oscillators. These characteristics are widely used to compare the digital circuit performance of different technologies.

In a complementary inverter, the ratio of the width of p-OTFT to n-OTFT (W_P/W_N) is determined mainly based on the ratio of μ_p to μ_n. In our designs for Gen.1 this ratio was 1/1, while in Gen.2 we used 1/2 or 1/3 in different phases of technology development. The use of larger n-OTFTs was avoided due to the extra parasitic capacitance they would add, and to the limited advantage in the position of the trip point that a large n-type device would add.

The design and simulations we carried out based on the model described in Section 3.3. Due to the high variability of the organic transistors characteristics, however, a fully reliable prediction of circuit performance is difficult to achieve. We implemented the parametric variations in a computer aided design (CAD) environment and used it to run Monte Carlo (MC) simulations. To make MC simulations possible, a Spectre (Circuit Simulator) model including OTFT models written in Verilog-A modelling language was used. Spectre generates automatically,

for each transistor in the schematic, a unique parameter set in line with the average and the standard deviation of every parameter of the Verilog-a model. These parameter sets are used to perform MC simulations.

Figure 21 presents the results of 100 iterations of an MC simulation for Gen.1 (left panels) and Gen.2 (right panels) inverters, including the transfer characteristics and the histogram of V_{trip} [91]. The simulation shows that, thanks to the complementary architecture, and despite the pronounced variability, the inverter is functional with acceptable noise margin in all the simulated cases and its transfer characteristic curves are centred at $V_{dd}/2$. It also illustrates that Gen.2 OTFTs have a higher variability compared to Gen.1 ones. This is probably the result of more complex fabrication steps adopted to improve the performance of Gen.2 OTFTs. MC simulations were also taken into account for choosing a suitable W_p/W_n ratio. For example, as shown in [89], inverter 1/1 and 1/2 have very similar trip point and noise margin according to the nominal simulations. In the MC simulations (on 100 iterations), however, the 1/2 inverter shows a better behaviour since its transfer characteristics curves are slightly more centred at $V_{dd}/2$ and less scattered.

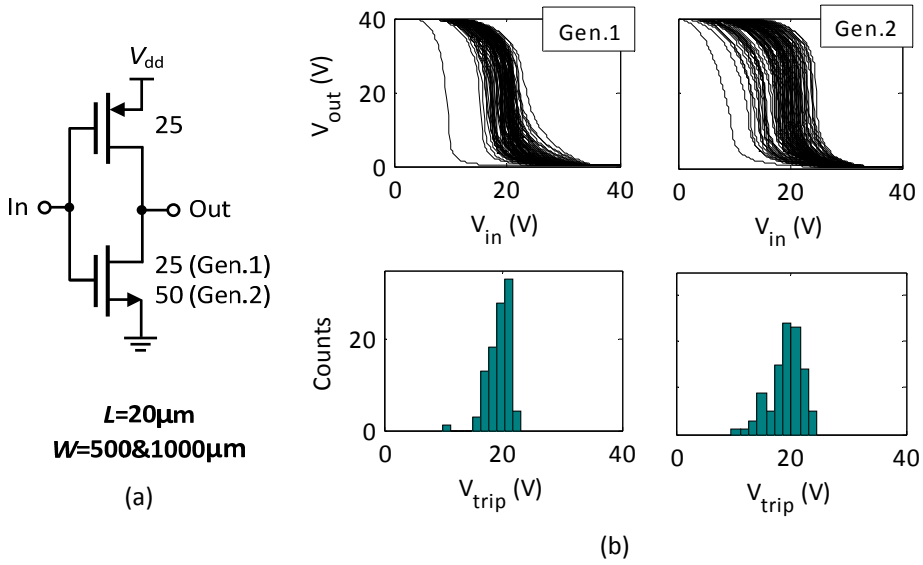


Figure 21. (a) Schematic of the complementary inverter (b) 100 iterations of an MC simulation for an inverter in Gen.1 (left panels) and Gen.2 (right panels). The (W/L) ratio is given in the schematic.

In addition to the first characterization tape-outs that included several single inverters, all other S2S tape-outs included some inverters too, to enable technology characterizations. Figure 22 indicates the status of the complementary technology during first phases of development by showing the transfer characteristics of nine inverters on one of the first samples manufactured in Gen.2 technology and measured in April 2011. The inverters suffered from severely low yield, due to e.g. shorted S/D-gate or high variations.

There has been a remarkable progress in the technology after the first phases, although it is still under modification and improvements. Figure 23 shows the measurements of inverters representing 10 different foils manufactured in Gen.2 process recently. The median value for DC gain and V_{trip} is around 32 dB and 20 V at V_{dd} of 40 V. V_{high} and V_{low} are close to V_{dd} and ground (GND). Figure 24 shows the same measurements in grey, and highlights the transfer characteristics of one inverter and the nominal simulations based on the model extracted for the same version of the technology. The measurements of the inverter at V_{dd} of 20 V and 10 V are also added. The results are obtained on the foil reported in [90]. It should be noted that hysteresis is negligible, less than 0.2 V at 40 V V_{dd}. V_{trip} and G_{max} are 22 V and 30 dB. The same tests on inverters on the foil reported in [91] processed in Gen.1 resulted in a typical V_{trip} and G_{max} of 19.3 V and 34 dB.

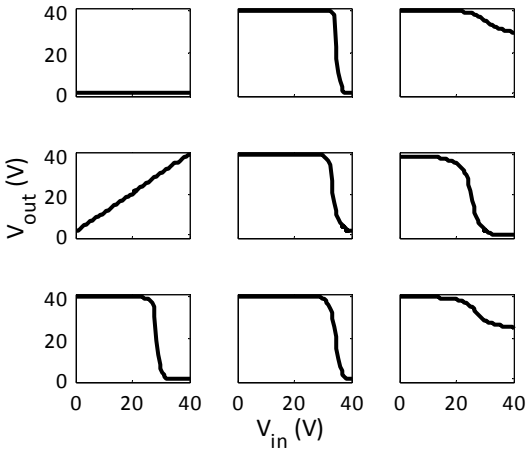


Figure 22. Measurement of nine inverters on one of the first samples manufactured in Gen.2 process (April 2011)

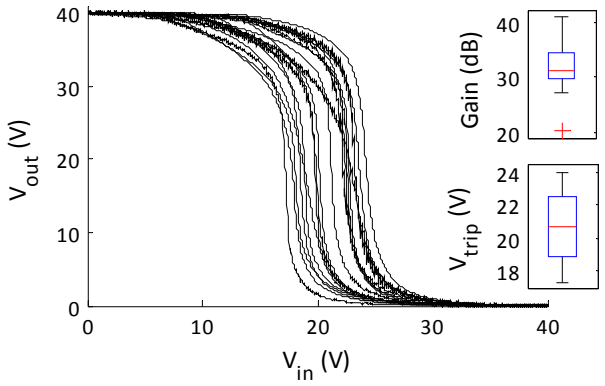


Figure 23. Measurements of inverters representing 10 different foils manufactured in Gen.2 (the insets show the boxplot of gains and trip points).

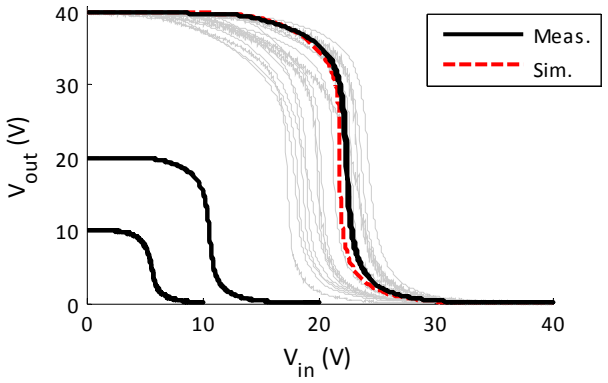


Figure 24. Measurements (black solid line) and simulation (red dashed line) of one of the inverters among many manufactured in Gen.2 (light gray lines). The measurements are shown V_{dd} equal to 10, 20, and 40 V.

Comparison between the experimental results and the simulations based on the described model show that the model can well predict the behaviour of the circuits. Although in some cases the experimental results may be quantitatively different from the nominal simulations, they fit very well in the range of performance predicted by the MC simulations.

The schematic and measurements of a 7-stage ring oscillator on the same foil (

[90]) is shown in Figure 25. The oscillation frequency is 75 Hz and 0.5 kHz at 20 V and 40 V supply voltages, respectively. This corresponds to a stage delay of 143 µs at 40 V. However, stage delays as low as 60 µs have also been measured in this technology [66]. For Gen.1 inverters measured at 40 V, stage delays of 1 ms and 0.43 ms are reported in [10] and [98], respectively.

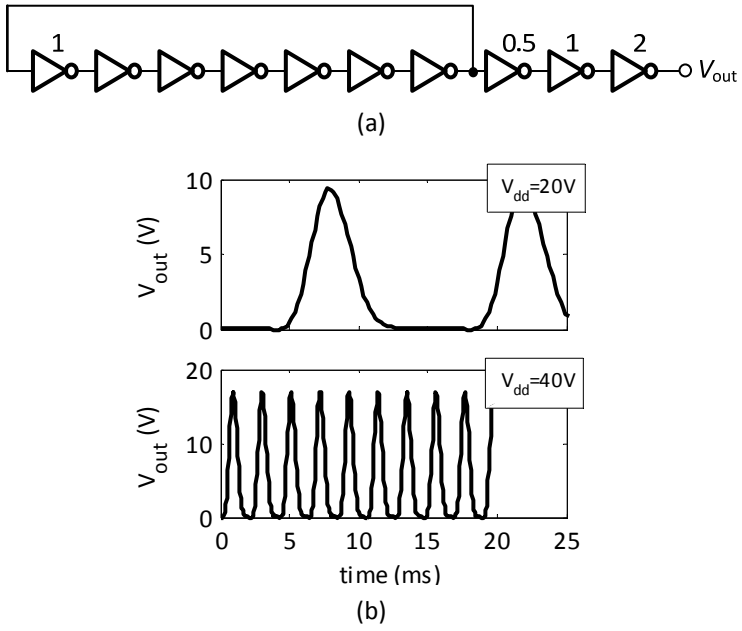


Figure 25. (a) Schematic of a 7-stage ring oscillator and (b) its measurements at 20 V and 40 V

NAND and NOR gates: Fully-static NAND and NOR gates in S2S technology were designed according to classic topologies and sized based on inverter measurement and simulations, as shown in Figure 26(a). Single NAND and NOR gates with different fan-outs and fan-ins were implemented only on characterization foils, but they were always included in the next designs as a part of larger circuits. Figure 26(b) presents the measurement and simulation of a NAND gate on the same foil as that of the inverters in Figure 24 [90]. V_A was set at V_{dd} and V_B was swept from 0 to V_{dd} and vice versa, and the same procedure was repeated swapping the inputs. It should be mentioned that NAND gates with larger fan-ins were also implemented, but as expected, the tests were often not successful. This is due to the large on-resistance

(R_{on}) of OTFTs, affected by the large threshold voltages ($R_{on}=1/\mu C_{ins}(W/L)(V_{GS}-V_T)$), which makes the pull-down network weak when more than two OTFTs are cascaded. That is the reason why in more complex circuits NAND gates with, for instance, 3-inputs will be typically implemented using cascaded 2-input NANDs.

Our quasi-static measurements on a NAND gate in Gen.1 show similar results [91].

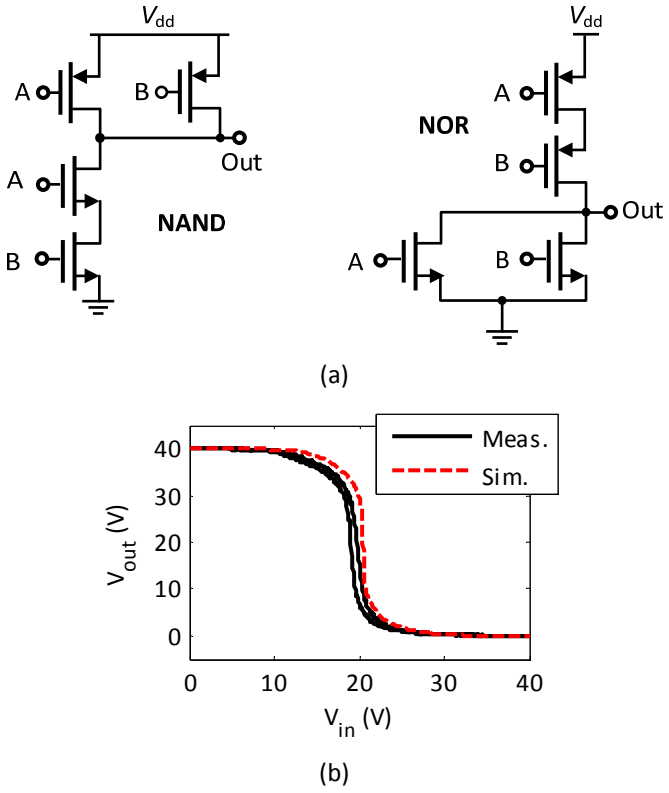


Figure 26. (a) Schematic of NAND and NOR gates, (b) Measurements of a NAND gate for one input set at V_{dd} (40 V) and the other swept from 0 to V_{dd} and vice versa.

4.2.1.2 Flip-flops

Figure 27 shows the schematic of a fully-static JK-FF, together with simulation and measurement results [90]. Each three-input NAND gate is made of 6 transistors, and the FF consists of 20 transistors in total. The circuit was measured at the clock frequency (f_{clk}) of 100Hz and keeping the input "J" equal to negated "K" ($J = \overline{K}$) to obtain a D flip-flop truth table. The outputs Q and $\overline{Q}$ change at each rising edge of the

clock signal (Clk). The simulation results based on the dynamic model are reasonably close to the experimental results.

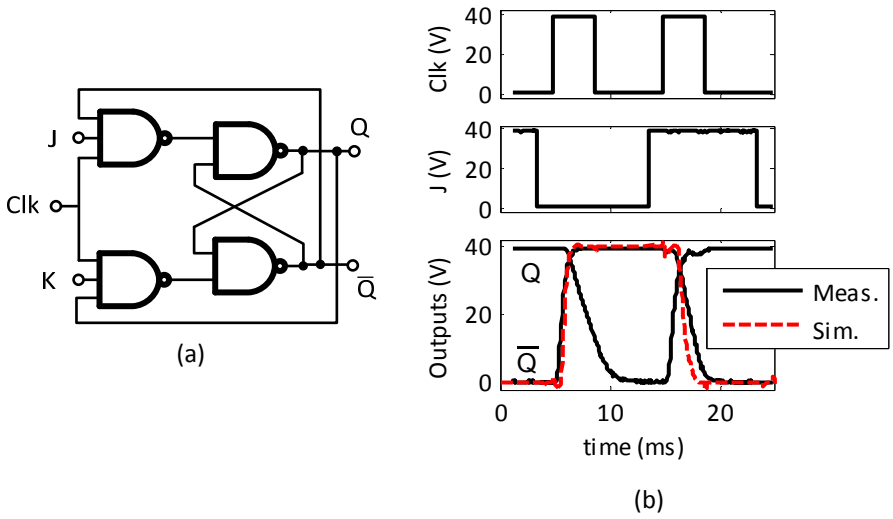


Figure 27. (a) Schematic of JK-FF, (b) measurements and simulation of the JK-FF at f_{clk} of 100 Hz.

4.2.2 Transmission-gate (TG) blocks

In a complementary technology, TG-architectures can be used to implement gates such as the exclusive OR (XOR) with much lower complexity compared to fully-static implementations. In addition, FFs based on TGs comprise a lower number of transistors, with positive effects on area consumption and hard yield. Here we discuss relevant TG-based single gates and FFs implemented in S2S technology. The TG-based blocks are not shown in Figure 19 since there were included in another design (PEM2b shown in Figure 39).

4.2.2.1 Single gates

An important function in many digital circuits, such as that of a silent tag, is a code comparison [99]. The code comparison can be easily performed by an XOR gate, which is complex in fully-static implementations, but could be easily implemented using TGs. Figure 28 shows the schematic and measurements of an XOR gate at different logic states. For each state, one input is constant and the other one is swept back and forth.

This gate behaves correctly, but it is obviously not static and does not show gain for all input configurations. When used as a part of other circuits, the XOR has always been used with an inverter at the output to provide enough gain and ensure sufficient driving capability.

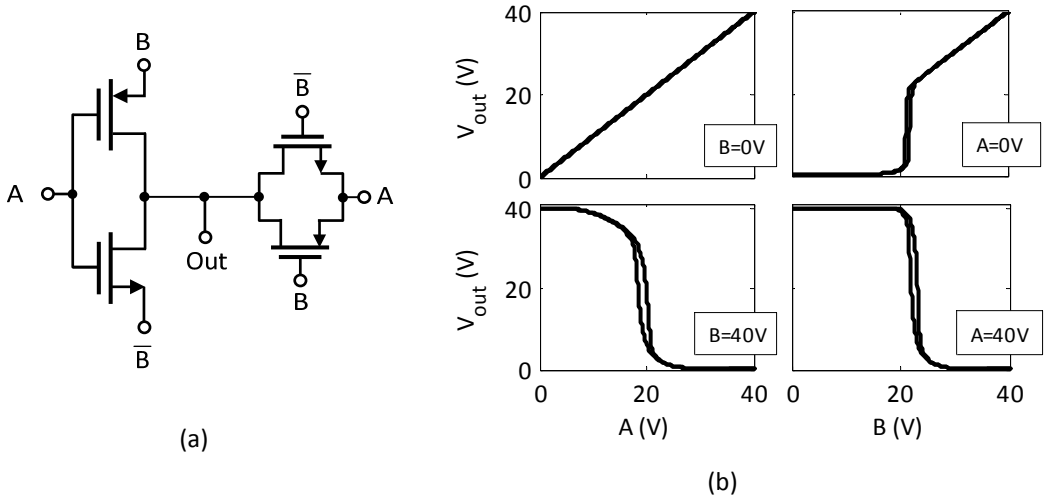


Figure 28. (a) The schematic of a TG-based XOR gate and (b) measurements at different input states

4.2.2.2 Flip-flops

Figure 29 depicts the schematic of the TG-based master/slave data flip-flop (D-FF) with asynchronous reset. An active Reset signal immediately resets the output of both master and slave latches and thus the output Q. When the Reset is deactivated, Q will change at the next falling edge of the Clk. Other variations of the TG FF have also been implemented, for example, by swapping the NOR and NAND gates to have a preset control. In all cases, it is avoided to implement the reset/preset function through the feedback loops, to keep the probability of having a functional FF even if the inverter or TG used in the feedback are not functional.

First, a D-latch similar to the master latch in Figure 29 is measured, as shown in Figure 30. The latch is transparent when the Clk is high. $\overline{Q}$ is the negation of D when Clk is high and then remains constant. Figure 31 shows the measurement of the D-FF. In Figure 31(a) D-FF is measured with deactivated Reset, and Q follows D at each

falling edge of the Clk. Figure 31(b) shows the functionality of the asynchronous reset, when D is high.

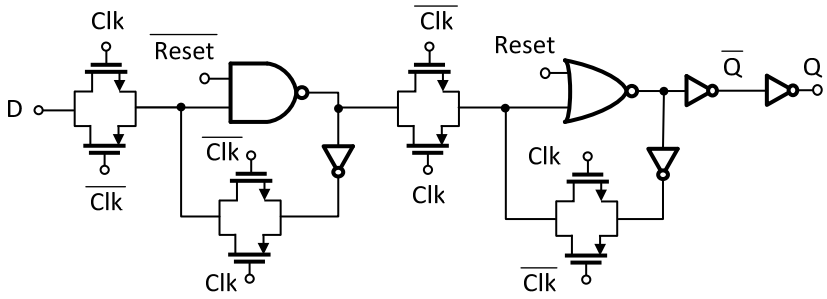


Figure 29. (a) Schematic of a master/slave TG D-FF with asynchronous reset

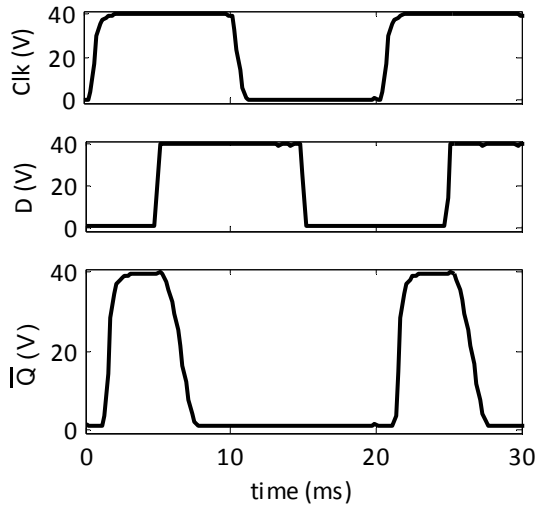


Figure 30. Measurements of a D-latch at f_{clk} of 50 Hz. The latch is transparent when the Clk is high ($\overline{Q}$ is shown).

In view of designing counters, Toggle FFs (TFFs) were manufactured based on the TG D-FF, by either directly connecting $\overline{Q}$ and D [100], or using an XOR gate at the input to provide a toggle control signal. Both TFFs were successfully measured. The maximum measured frequency was 500 Hz and 100 Hz at V_{dd} of 40 V and 20 V, respectively.

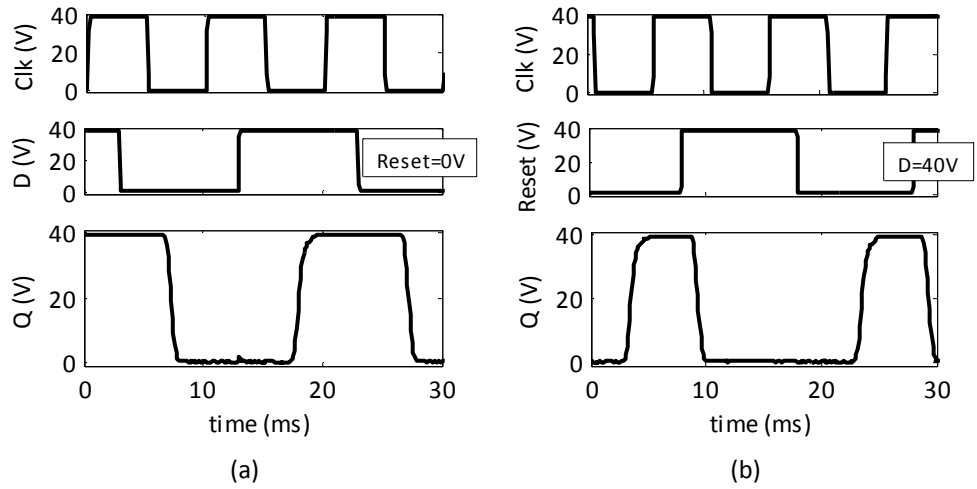


Figure 31. (a) D-FF measurement while reset is inactive. Q follows D at each falling edge of Clk, (b) D-FF measurement while D is 40 V, Q remains low when Reset is high. In both measurements f_{clk} is 100 Hz.

4.2.3 Dynamic blocks

Digital circuits based on dynamic logic not only achieve a good speed performance, but also consume a smaller area due to the lower transistor count compared to both fully-static and TG-based implementations.

The operation of dynamic logic relies on the dynamic storage of the logic values on the different circuit nodes. Charge leakage, charge sharing, capacitive coupling and clock-feed through can easily destroy the logic state on these nodes when they are in high impedance. Indeed, normally careful design and high-quality design automation tools are employed to design dynamic digital circuits in well-known CMOS technologies [101]-[102]. In this section, we show the implementation of dynamic single gates and FFs in S2S technology.

4.2.3.1 Single gates

We implemented dynamic NAND gates followed by a static inverter used to buffer the output for measurement purposes. Figure 32(a) shows the schematic of a NAND gate realised using a p-type precharge transistor and a pull-down network (PDN) of n-type transistors to implement the logic function. The same gate was also

manufactured using an n-type discharge transistor and a pull-up network (PUN), but the circuit measured on this specific foil was not functional. Such an implementation is expected to be faster since only p-type OTFTs with higher mobility perform the logic. The measurement results for the input values AB=01 and AB=11 are shown in Figure 32(b) [90]. When Clk is low (precharge phase), the dynamic output (Out_d) goes high, driving the static output (Out) to ground. As expected, when Clk is high, Out goes high only if both of the inputs (A and B) are high. So the overall gate works as an AND. f_{clk} is 150Hz and V_{dd} is 40V.

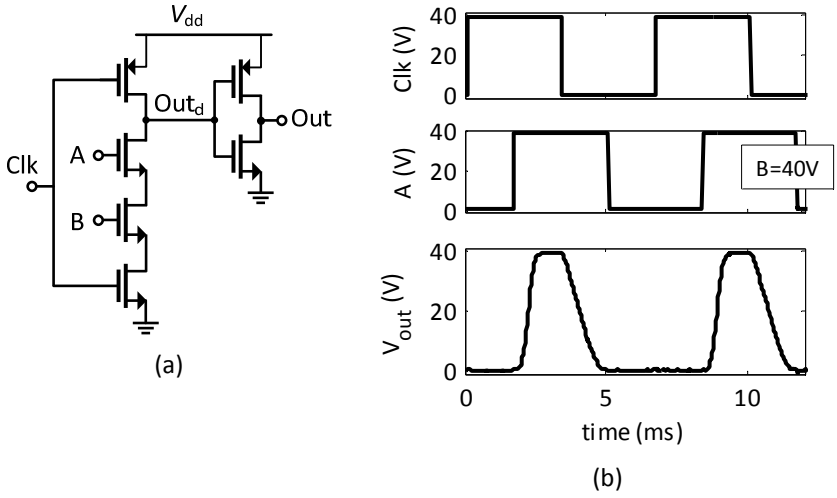


Figure 32. (a) Schematic of a dynamic NAND gate with an static inverter at the output, (b) experimental characterization of the gate for two states (AB=01 and AB=11) at f_{clk} of 150 Hz.

4.2.3.2 Flip-Flops

We designed and measured a dynamic true single phase clock (TSPC) FF [90]. The TSPC FF shown in Figure 33(a) consists of only 11 transistors, compared to the 36 and 20 transistors needed for fully-static and TG-based MSFFs, respectively.

Figure 33(b) shows the experimental results of TSPC-FF measurements [103]. When Clk is low, the first stage is transparent and its output (X1) is equal to the complement of D, while the second stage is precharging (X2=high) and thus, the third stage (X3) is in hold state. When the Clk switches to high, the second stage evaluates the input and depending on the value of X1, X2 stays high (for X1=low) or goes to low

(for X1=high). Therefore, at the positive edge of Clk, Q changes state depending on the value of D, while Q remains constant when the Clk goes low. The measurement clock frequency in the figure is 100Hz. This is the first dynamic FF ever shown manufactured with OTFTs.

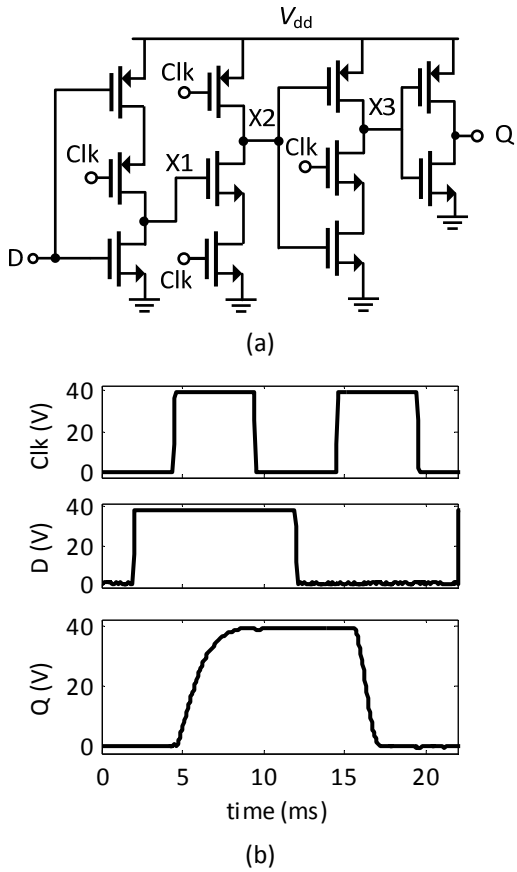


Figure 33. (a) Schematic of the dynamic flip-flop, (b) experimental characterization of the flip-flop at f_{clk} of 100 Hz.

4.2.4 Logic style selection

Fully-static logic blocks are simple and robust, thus suitable for implementing reliable circuits based on elementary gates such as inverters and NANDs. However, when it comes to more complex logic such as FFs, a fully-static implementation can be too expensive in terms of area, especially in a printing technology. As explained before, the area consumption of circuits implemented using printing techniques is a

strong function of the number of transistors. This is due to the typical requirements of printing, which set a large minimum distance between n-type and p-type semiconductors, making it difficult to have a compact design. In the specific case of master-slave (MS) FFs needed for many applications, the high transistor count of the fully-static implementations makes them difficult to use. The area of one fully-static MS FF in our technology is 15.75 cm^2 (the available area of a sheet is only 100 cm^2).

In S2S OTFTs there is a well-defined region of V_{GS} where for both types of transistors are off. In other words, n-type OTFTs have a positive threshold and p-type OTFTs a negative one. This characteristic provides the opportunity to implement transmission gates (TGs) and dynamic logic. Therefore, certain digital circuits can be manufactured in a much smaller area compared to fully-static implementations, while accepting a larger vulnerability to soft faults. The TG FF in S2S technology occupies an area around four times smaller than a fully-static MSFF.

The remarkably low transistor count in dynamic FFs makes dynamic logic particularly appealing for S2S technology, in which the circuit area is strongly dependant on transistor count. However, the issues regarding the reliability of dynamic digital circuits become more substantial when organic transistors with high variations and high parasitic capacitance are used. The lack of high-quality automation design tools exacerbates the situation. For example in the case of the TSPC FF (Figure 33), with an area almost 10 times smaller than the fully-static MSFF, the circuit is very sensitive to clock slope [104]-[105] and suffers from glitch problems [105]. In addition, when used in architectures such as T-FF, stability issues may arise [106].

When accurate design tools which include a complete statistical characterization of the dynamic behaviour will be available, the use of dynamic logic can well improve the area consumption in S2S technology. At the present state, TG-based logic which offers lower area compared to fully-static implementations and higher robustness compared to dynamic logic is a good intermediate solution, and we will pursue this choice further to implement more complex digital circuits in S2S technology.

4.3 Digital design in W2W technology

The application in W2W technology we are focusing on is a line driver. As it will be

discussed in Chapter 6, the key building block for display drivers is a flip-flop. Similar to the discussions in Section 4.2 for S2S digital design, we explore first fully-static blocks in Section 4.3.1, and then transmission-gate architectures in Sections 4.3.2. Finally, we discuss about the selection of the architecture for logic circuits in W2W technology in Section 4.3.3. The fully-static shift register demonstrated in Section 4.2.1 has the highest transistor count in a complementary organic technology to date [96].

We designed three mask sets in W2W technology containing single transistors and characterization blocks, up to complex digital circuits on foil. The building blocks discussed in this section were manufactured on the W2W characterization foil shown in Figure 15 (PEM2). The building block measurements were performed using a probe station placed in a glove box under controlled atmospheric condition. Six single probe needles were used for the measurements. The DC measurements were performed using a Semiconductor Parameter Analyser and the digital AC signals were created by synchronized Arbitrary Waveform Generators and measured by a mixed-signal oscilloscope.

The W2W digital circuits are first measured at a 10 V supply voltage and then tested at lower voltages. Due to the smaller OTFT threshold voltages in this technology, circuits are functional at 3 V and even lower in some cases.

4.3.1 Fully-static blocks

As discussed before, fully-static logic blocks such as flip-flops are simple and robust, but comprise a high number of transistors, making them likely to have high area consumption. In this section, we explore the characteristics of fully-static blocks implemented in W2W technology.

4.3.1.1 Single gates

In W2W technology with an n- to p-type mobility of around 7, we set the ratio of the width of p-OTFT to n-OTFT (W_P/W_N) in an inverter to 4/1. The design and simulations we carried out based on the model described in Section 3.30. The nominal simulation of the inverter is shown in Figure 34, together with measurements of

eleven inverters distributed on the die [96]. It should be mentioned that also in this technology, the yield has improved on the final samples (reported here) compared to the first manufactured samples.

The measurement was performed at 5 V and 10 V supply voltages. The data show that despite all the variations, the curves are centred at around $V_{dd}/2$. This means that, thanks to the complementary technology, the noise margin and thus reliability is much higher compared to typical inverters in similar single-gate p-only organic technologies [48]. The figure also shows that the model provides a good estimation of the inverter performance. The median of gain and trip point is around 22 dB and 4.5 V for 10V supply.

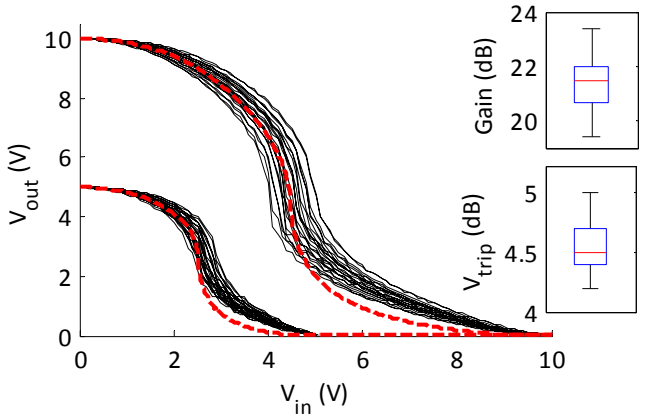
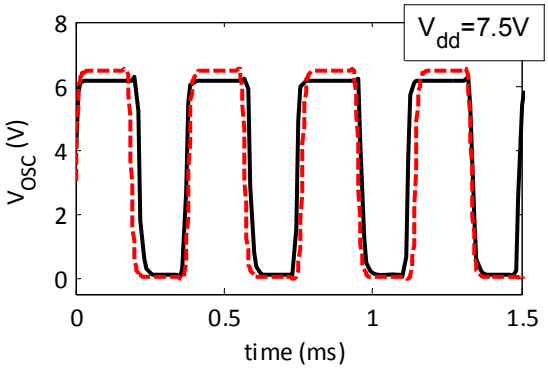


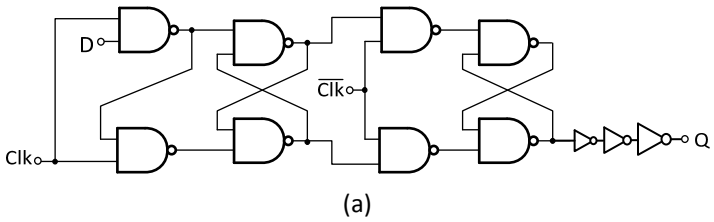
Figure 34. Measurements of eleven complementary inverters (solid lines) and nominal simulation of inverters (dashed lines). The insets show the boxplot of gains and trip points.

Figure 35 presents the measured and simulated output of a 19-stage ring-oscillator at supply voltage (V_{dd}) of 7.5 V [96]. The output load is 1 MΩ. The measured and simulated frequencies of the ring-oscillator at V_{dd} from 2 V to 10 V are also given in the table, showing a good agreement between dynamic simulations and measurements. The measured frequency at 2 V and 10 V supply voltage are equivalent to stage delays of 53 and 7.3 µs, respectively.

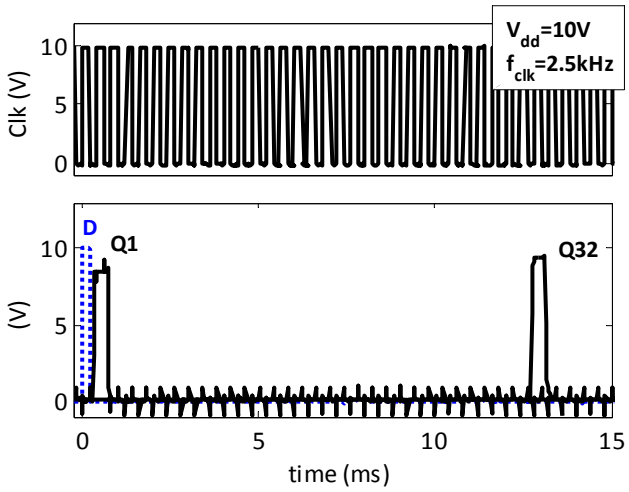


V_{dd} (V)	2	3	4	5	7.5	10
Measured freq. (kHz)	0.5	1	1.4	1.7	2.6	3.6
Simulated freq. (kHz)	0.7	1.1	1.5	1.8	2.6	3.4

Figure 35. Measured (solid line) and simulated (dashed line) output of a 19-stage ring-oscillator at V_{dd} of 7.5 V. The table shows the measured and simulated frequency of the ring oscillator at different supply voltages.



(a)



(b)

Figure 36. (a) Schematic of the fully-static MSFF, (b) measurements of a 32-stage fully-static shift register at V_{dd}=10 V and f_{clk}=2.5 kHz. Q1 and Q32 are shown.

4.3.1.2 FFs

Figure 36(a) shows the schematic of a fully-static master-slave FF designed in W2W technology. A 3-stage buffer was used at the output. The largest designed transistor width is 5000 µm. We measured the cascade of thirty-two FFs (32-stage shift register) to have an estimation of the yield in this technology. The shift register input (D) propagates through the stages at each rising edge of the Clk. In Figure 36(b), the 2.5-kHz Clk signal and the 1st and 32nd outputs of the driver measured at V_{dd} of 10 V are presented. The peak-to-peak output reaches almost full-swing. The current consumed at 10 V is 68 µA. We measured four 32-stage shift registers: two of them were fully functional, and another one was working till the 22nd stage [96].

4.3.2 Transmission-gate blocks

The TG-based FF shown in Figure 37(a) is typically used in complementary organic technologies such as [14], [100]. We also designed and measured a 32-stage shift register based on this FF [96]. Measurements are performed at 10-V V_{dd} and 1-kHz f_{clk}, as shown in Figure 37(b). Only the outputs of even stages are shown in the graph, with an added vertical offset to improve clarity.

4.3.3 Logic style selection

Compared to fully-static implementations, TG-based FFs have a lower number of transistors and therefore, they are smaller and less vulnerable to defects. However, an important requirement to guarantee the correct functionality of TG-based MSFFs is that the TGs are switched off at V_{GS} equal to zero. In other words, there must be a well-defined range of V_{GS} (around zero) where both p-type and n-type transistors are off. This is not always the case in W2W technology since OTFTs could be normally on. To illustrate this point more clearly, the histogram of OTFTs' V_{onset} is shown in Figure 38. According to the definition in Section 3.2, V_{onset} marks the voltage at which the transistor starts to turn on and the drain current becomes significantly higher than the off current. This value, as shown in Figure 38, is in most cases positive for p-type and negative for n-type, meaning that there could be a significant leakage at V_{GS} equal to zero. Consequently, whenever the Clk signal goes off, TGs are likely to go from a fully-on state to slightly-on, instead of turning completely off. This can easily result in

problems such as racing between the master and the slave FFs, seriously deteriorating the reliability of the TG-based line drivers.

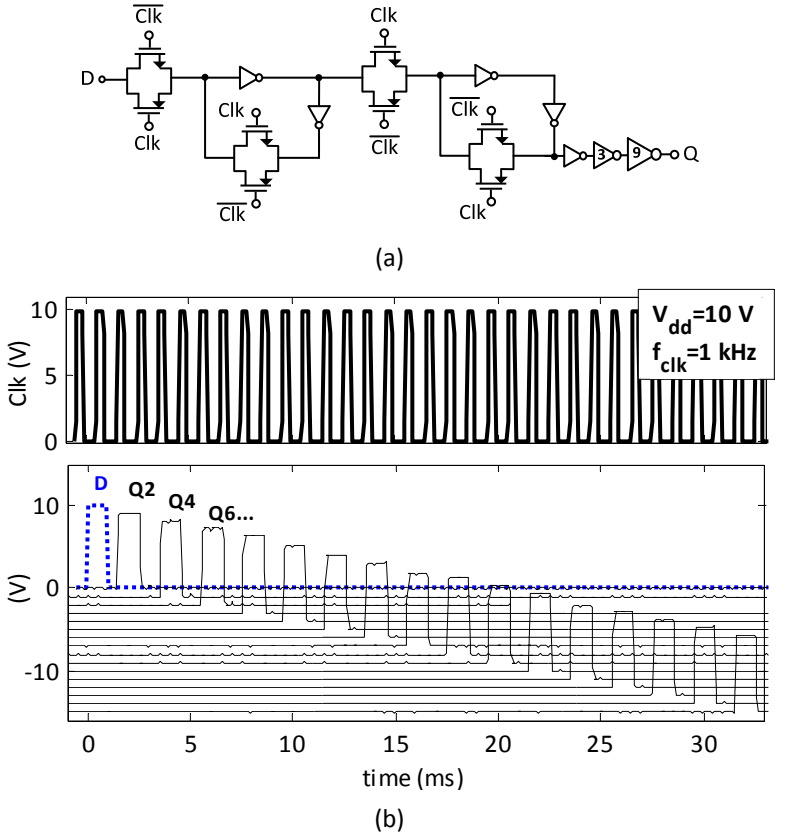


Figure 37. (a) Schematic of TG-based FF, (b) measurements of a 32-stage TG-based shift register at V_{dd}=10 V and f_{clk}=1 kHz. Q2, Q4, Q6, … to Q32 are shown with an added vertical offset for clarity.

From this perspective, fully-static FFs are more robust with respect to threshold voltage variations. In this architecture, the decision-making OTFTs are always strongly on, and the slightly-on transistors can only cause an increase in the power consumption. The drawback of this circuit is, however, that it comprises twice as many transistors as the TG-based FF.

Since in W2W technology the logic gates are quite compact and p- and n-type transistors could be placed close to each other, doubling the number of transistors does not lead to an excessive increase in area. It should be noted that a considerable

portion of the area in final applications is usually devoted to buffers and routings which are common between both implementations. Indeed, a 32-stage shift register implemented in W2W technology based on TGs counts 704 OTFTs and has an area of 0.88 cm^2 (including buffers), while a fully-static one with 1216 transistors has an area of 1.17 cm^2, that is only 1.3 times larger. Therefore, fully-static logic is a good choice for implementing digital circuits in W2W technology.

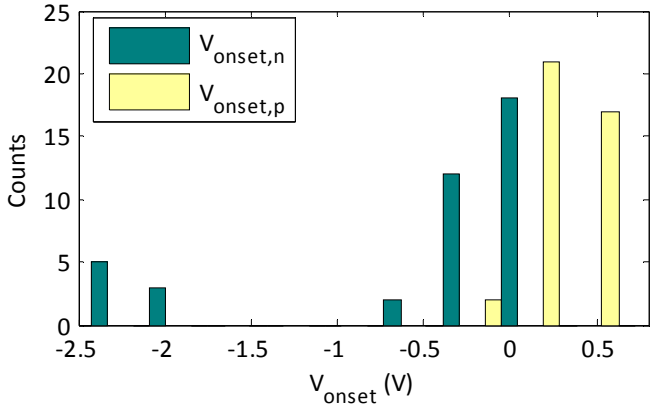


Figure 38. Number of occurrences for onset voltage (V_{onset}) of forty p-type and n-type transistors on a W2W die

4.4 Digital design highlights

From the results presented in this chapter it can be concluded that the hard yield of the complementary organic technologies has improved in recent years, resulting in an increase in the circuit level of complexity from a few functional inverters among many implemented to functional FFs with different structures. However, the circuit complexity is still limited by hard faults. Indeed, the noise margin of the inverters (as an indication of the soft faults) in both technologies is close to ideal, remarkably better than that of p-only inverters which have the same number of OTFTs and do not use extra biases for a dual gate. The same is valid regarding the inverters output voltage swing. In summary, if the technology hard yield is further improved, the circuit level of complexity can be improved remarkably.

Compared to the S2S technology, circuits with a high number of OTFTs can be more easily implemented in the W2W technology, because of its high level of OTFT

integration. Indeed, as shown in the following chapters, circuits with more than a thousand OTFTs have been already achieved in W2W technology, while for the S2S technology this is lower than two-hundred transistors. However, it should be noted that the area that the S2S technology can process successfully is much larger than that of the W2W technology at the current state (to have a clear view, compare again the footprint of an inverter which is fourteen times larger in S2S).

Another important difference between the two technologies is the suitable logic style which is especially dependant on OTFT characteristic at zero V_{GS}. Since S2S OTFTs are strongly off at V_{GS}=0, it is possible to implement TG-based and even dynamic logic. That is an important advantage, especially knowing that fully-static FFs are not feasible in S2S technology due to the excessive area consumption (See Sections 4.2.4). Indeed, in presence of a reasonably detailed dynamic model, the use of dynamic logic in complex circuits can remarkably improve the circuit area consumption in S2S technology. In W2W technology, the occasional occurrence of normally-on OTFTs reduces the reliability and robustness of TG-based and dynamic logic. Fully-static logic is a good choice for this technology. Due to the compact placement of transistors, a fully static FF is not excessively larger than the commonly-used TG-based one, while it is much more reliable.

5 Analogue and Mixed-Signal Circuit Design

This chapter gives a detailed description of analogue and mixed-signal circuit design, focusing in particular on the S2S printing organic complementary technology. The design and characterization of several building blocks based on different architectures are shown. After discussing simple differential OTAs, a mismatch-free comparator exploiting offset-cancellation techniques is demonstrated, able to resolve differential input voltages as small as 50 mV, a remarkable sensitivity achieved by printed electronics. A printed DAC, the first ever demonstrated, is also shown. This DAC, based on a "R-2R" resistive network, achieves a maximum INL of 0.04 LSB at a resolution level of 4 bits. In addition, the HF behaviour of printed diode-connected OTFTs is studied and a four-stage rectifier is presented.

5.1 Introduction

As explained in Section 1.2, the characteristics of unipolar organic technologies limit the performance of analogue circuits in several ways. A few unipolar organic amplifiers have been implemented [107]-[109], and some techniques have been employed to improve the reliability and performance of analogue circuits [60], [64], [110]. All of these techniques are based on the use of dual-gate OTFTs. Dual-gate OTFT technologies are also used in [40] and [42] to implement first delta-sigma and VCO-based ADCs, respectively. The state of the art of analogue and mixed-signal circuits implemented with organic TFTs remains, however, in a pioneering stage.

The lack of reliable analogue circuits hinders the implementation of fully-integrated mixed-signal systems such as smart sensors and RFID tags, which, on the other hand, would be especially attractive applications of low-cost, high-throughput technologies like the organic printing processes.

Analogue and mixed-signal design can be facilitated exploiting a complementary technology which, indeed, enables the use of well-known CMOS circuit architectures, promising increased performance and robustness. For example, SC architectures are used in [41] to implement an inverter-based comparator and a C-2C DAC for a SAR ADC. Single-stage amplifiers in complementary organic technologies have been reported in [111] and [98]. The OTFT performance and matching, however, remain important challenges to the advancement of OTFT-based analogue circuits.

In Section 5.2, we show the design and characterization of several analogue and mixed signal blocks tailored for applications targeted by S2S technology. These circuits include operational transconductance amplifiers (OTAs), comparators (for ADCs), DACs, and rectifiers (for RFID tags). In addition, simulations of an AM demodulator based on the measured Gen.1 comparator and rectifier are presented.

Section 5.3 contains measurements of single-stage OTAs in W2W technology. Since the application targeted for W2W technology, namely display driver, contains only digital blocks, we have not explored further details of analogue design in W2W technology. The highlights of analogue design in complementary organic technologies achieved in this work are discussed in Section 5.4.

5.2 Analogue design in S2S technology

Printing technologies are mainly used to fabricate digital electronics or large-area switch matrices [5]-[10]. This is mostly due to the low yield and, especially, to the large mismatch typical of printed OTFTs, which results from the low degree of spatial correlation intrinsic to printing processes. Besides, in general, fully-printed OTFTs show a worse performance compared to vacuum-deposited or photolithography-based OTFTs [98].

We start from simple OTAs in Section 5.2.1 to characterize the performance of printed OTFT-based analogue circuits. Then we show several comparators and a DAC in Sections 5.2.2 and 5.2.3 respectively. These circuits are the blocks that we will use to implement a counting ADC (discussed in Chapter 7). The design of comparators together with envelope detectors and rectifiers discussed in Section 5.2.4 put the basis for the implementation of an RFID radio interface (discussed in Chapter 8), including AM demodulation of the incoming carrier, which is indispensable for reader-talks-first protocols[19]. The simulation of an AM demodulator based on some of the measured comparators and envelope detectors is presented in 5.2.5.

Analogue circuits with different complexity levels were included in some of the mask sets we designed for S2S technology. The design and simulations were based on the models explained in Section 3.3. Figure 39 shows the third designed foil (PEM2a) containing some of the analogue building blocks that are discussed in this chapter.

The general measurement setup is similar to that explained in Section 4.2 and shown in Figure 20. It is interesting to stress that all measurements have been performed in air, and that measurements have been extended on a period of several weeks. The S2S analogue circuits are usually measured at 40 V or higher supply voltages, due to the large threshold voltage of S2S OTFTs. Circuits implemented by

[19] In a “reader-talks-first” RFID system, the reader sends an energising field (a carrier signal typically at radio frequency) which is modulated with a call message to the transponders. The tags need to demodulate and read this call message (typically AM-modulated due to simplicity), before deciding whether to answer the reader. In a “tag-talks-first” system, on the other hand, the reader just sends the energising field with no modulation, and tags send a response as soon as they convert the energising field to power.

both Gen.1 and Gen.2 versions of S2S technology are discussed.

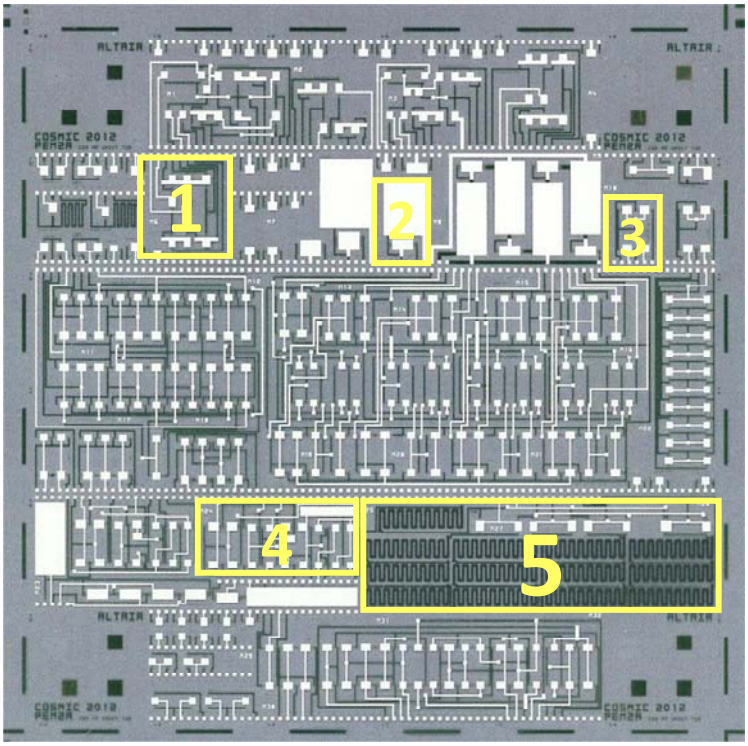


Figure 39. Picture of the foil containing several building blocks (PEM2a). Some analogue blocks are individually shown: 1. Two-stage OTA/Comparator (Figure 43), 2. Envelope detector, 3. Single-stage OTA, 4. Two-stage inverter-based comparator (Figure 45), and 5.R-2R DAC. Most of the other blocks are digital.

5.2.1 OTAs

We first designed a simple differential amplifier with a current-mirror active load, shown in Figure 40. This circuit was manufactured using both Gen.1 and Gen.2 technologies.

Gen.1: The simulation and measurements of the OTA manufactured in Gen.1 technology is depicted in Figure 41 [91]. The circuit was measured quasi-statically while one of the inputs (V_{in+}) was set at a specific voltage and the other input (V_{in-}) was swept back and forth from 0 to 40 V. The measurements are shown for different values of V_{in+}, namely 15 V, 20 V, and 25 V, and at an external bias current of 0.3 µA. The amplifier shows a relatively low offset in this case (good OTFT matching), although

it has a hysteresis of about 1 V, due to drifting of the OTFTs characteristics under bias. The measured amplifier gain for V_{in+} of 20 V is about 29 dB.

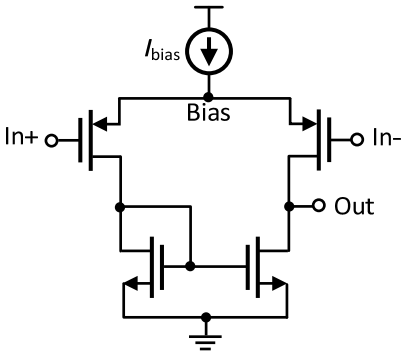


Figure 40. Schematic of the OTA

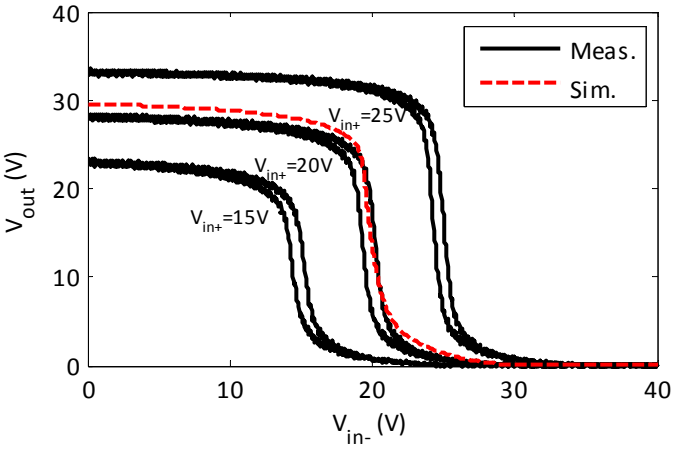


Figure 41. Gen.1 OTA simulation and measurements: output voltage vs. input voltage (V_{in-}) measured at different V_{in+} values are shown. The simulation shows the case when V_{in+} is equal to 20 V. I_{bias} is 0.3 µA.

Gen.2: Figure 42 presents the measurements of three samples of the same OTA manufactured in Gen.2 technology [90]. The circuit was measured quasi-statically while one of the inputs (V_{in+}) was set at a specific voltage and the other input (V_{in-}) was swept back and forth from 0 to 40 V. An external bias current (I_{bias}) of 2 µA was applied and the voltages at the bias node and output node were measured. The gain ranges from 25.1 to 28 dB, relatively close to that in the Gen.1 OTA. It should be noted that

both Gen.1 and Gen.2 OTAs were biased in sub-threshold region where the intrinsic voltage gain is higher[20] and directly affected by the sub-threshold swing (usually slightly better in Gen.1 OTFTs).

The output offset ranges in the measured samples from 1.5 to 4 V. These Gen.2 OTAs show a higher offset compared to the measured Gen.1 OTA. It was previously shown that Gen. 2 OTFTs suffer from higher variations compared to Gen.1 OTFTs, based on the OTFTs characterization and modelling and the resulting MC simulations (Figure 21). This measurement could be a sign that Gen.2 OTFTs have a poorer matching compared to those in Gen. 1. However, many more characterizations would be needed before conclusions in this sense can be drawn.

DC and AC measurements of other OTAs in S2S technology are presented in [112].

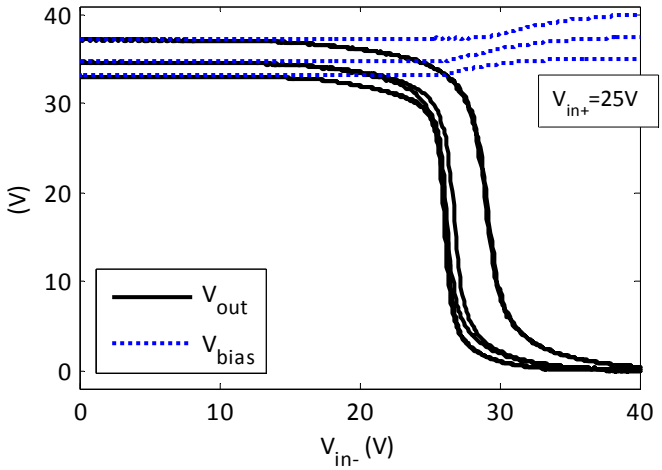


Figure 42. Measurements of two samples of Gen.2 OTAs on two different foils: the voltages at the bias and output nodes are measured when In+ is set at 25 V and the voltage at In- is swept. I_{bias} is 2 µA.

5.2.2 Comparators

Several design considerations need to be taken into account in the design of a

[20] Intrinsic gain here means the gain at a constant channel length (L), which is higher at a lower bias current (gain=$g_m R_{out}$, $R_{out} \propto I_D^{-1}$ and $g_m \propto I_D^{0.5}$).

comparator in organic technologies. In differential architectures, the relatively large device mismatch causes a large offset. One example is the OTA of Figure 40(a) which could be used as a very simple differential comparator. However, a remarkably high offset is measured in different samples of this structure (see Figure 42). Offset cancelation schemes for a differential amplifier needs several capacitors and switches, which could lead to yield problems. Therefore, a simpler approach may be desirable. We studied different architectures for Gen.1 and Gen.2 versions of S2S technology.

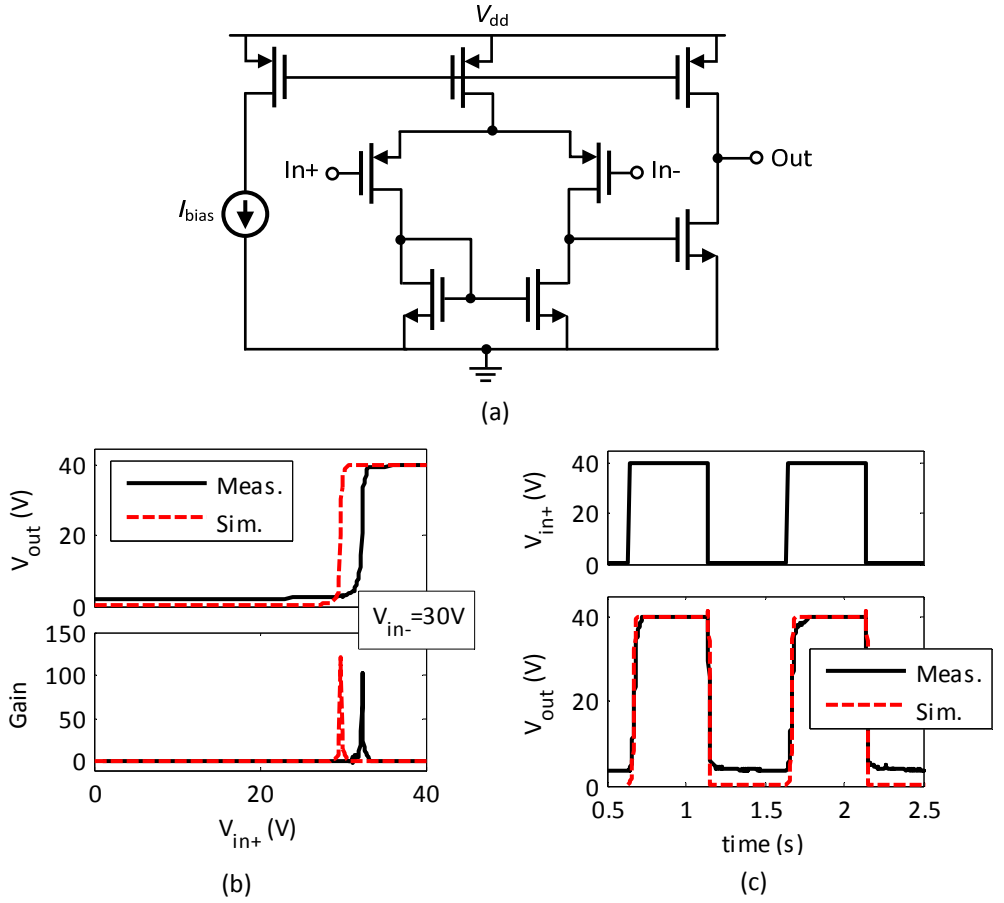


Figure 43. (a) Schematic of the comparator manufactured in Gen.1, (b) quasi-static measurement at V_{in-}=30 V and I_{bias}=0.15 µA, (c) Dynamic measurements at f_{clk} of 1 Hz.

Gen.1: We designed the two-stage OTA depicted in Figure 43(a) to be used in open loop as a comparator. The static and dynamic behaviour of the comparator were

measured at 40 V supply voltage, 30 V common-mode voltage, and 0.15 µA bias current. Figure 43(b) shows the result of static simulation and measurements while the negative input (V_{in-}) was set at 30 V and the positive input (V_{in+}) was swept. A gain of 40 dB was achieved, and the measured input offset was in this case 2 V.

For dynamic measurements shown in Figure 43(c), V_{in-} was set to 30 V and a 1 Hz pulse signal was applied to V_{in+}. The measured full-swing rise and fall time are 40 ms and 10 ms, respectively. The total load capacitance at the output node due to the measurement instruments was 37 pF. These measurements confirm that offset cancellation techniques are mandatory to obtain acceptable comparator accuracy. Indeed the observed 2-V offset corresponds to a best-case maximum effective number of bits (ENOB) of just about 2 bits for the comparator used in an ADC with full scale input equal to the supply level.

Gen.2: The schematic of a simple dynamic comparator designed for Gen.2 is illustrated in Figure 44(a). A non-differential mismatch-insensitive architecture was chosen in order to avoid problems with the large offset that can affect printed circuits, due to the device mismatch typical of printing technologies.

When Clk is high (reset phase), the transmission gate S1 and S2 put the inverter in unity-gain and charge the capacitor *C* to the voltage difference between the negative input (V_{in-}) and the trip point of the inverter. When the Clk goes low (comparison phase), transmission gate S3 connects the top plate of *C* to V_{in+}, and the signal voltage across *C*, which is equal to (V_{in+}- V_{in-}) is amplified by the inverter.

Figure 44(b) and (c) show the dynamic measurement results of the comparator at 50Hz and 20Hz clock frequency and for different input values (V_{in}= V_{in+}-V_{in-}) [90]. This simple comparator is able to detect input signals as small as 200mV, as shown in Figure 44(c): a remarkable performance for a printed circuit. It should be highlighted that this is possible because the complementary technology enables the use of pass-gates and simple offset cancellation strategies. This solution is rather insensitive to slow common mode disturbances at the inputs, but it is sensitive to power supply noise, being non-differential. Its low TFT count, however, makes it a good candidate for the state of the art of S2S technology, which is still affected by relatively high

defectivity.

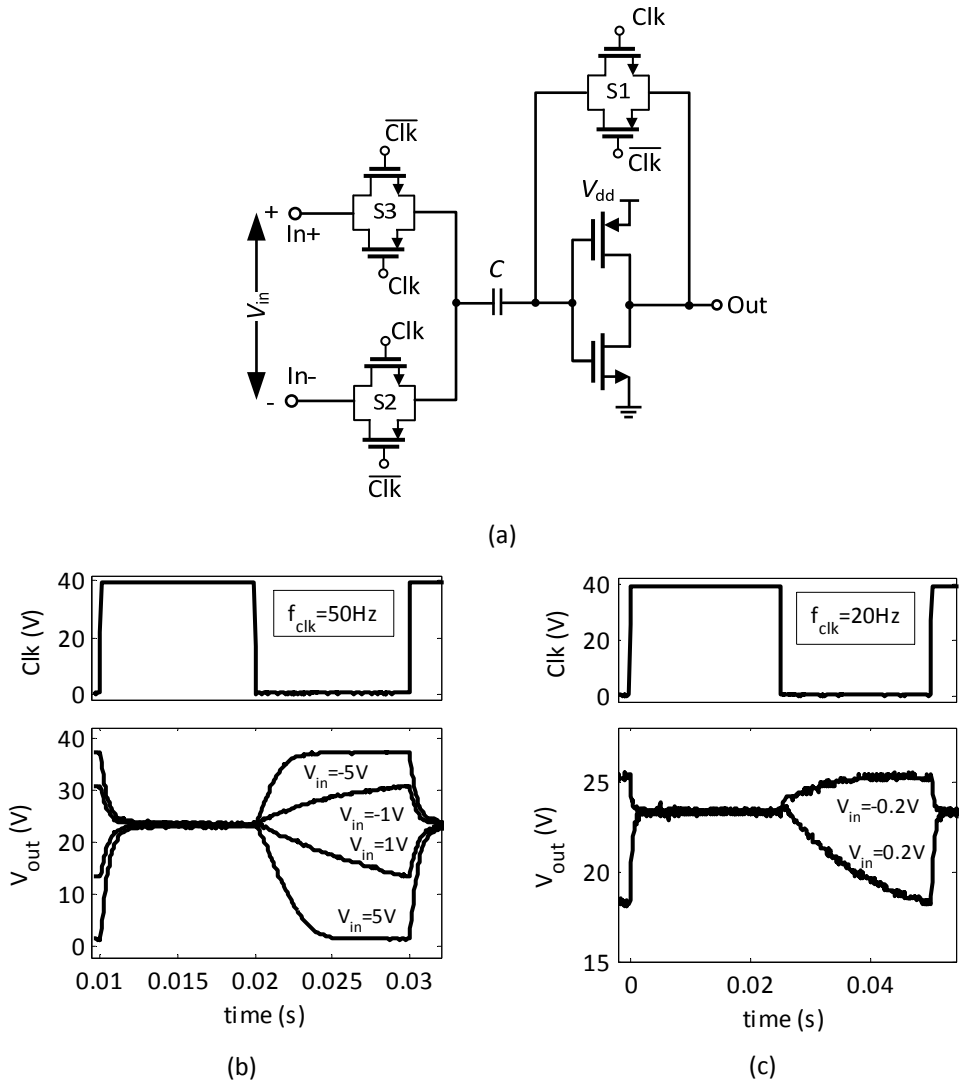


Figure 44. (a) Schematic of the inverter-based comparator manufactured in Gen.2, (b) comparator measurement results @ f_{clk}=50 Hz and V_{in}=±5, ±1 V, (c) comparator measurement results @ f_{clk}=20Hz and V_{in}=±0.2 V.

The offset-zeroed inverter-based comparator of Figure 44(a) is self-biased and has a rail-to-rail common-mode input range, but needs a quite large AC-coupling capacitor at the input, due to large parasitic capacitors of the complementary inverter (even more critical in a printing technology) and the charge injection caused by the several

switches used [41]. Using a cascade of this architecture to achieve a higher gain as in [41] could remarkably increase the area of the comparator and affect its yield. To avoid such issues, we used the architecture of Figure 44(a) as the first stage, and a comparator based on current copiers [113] as the second one. This circuit is presented in Figure 45.

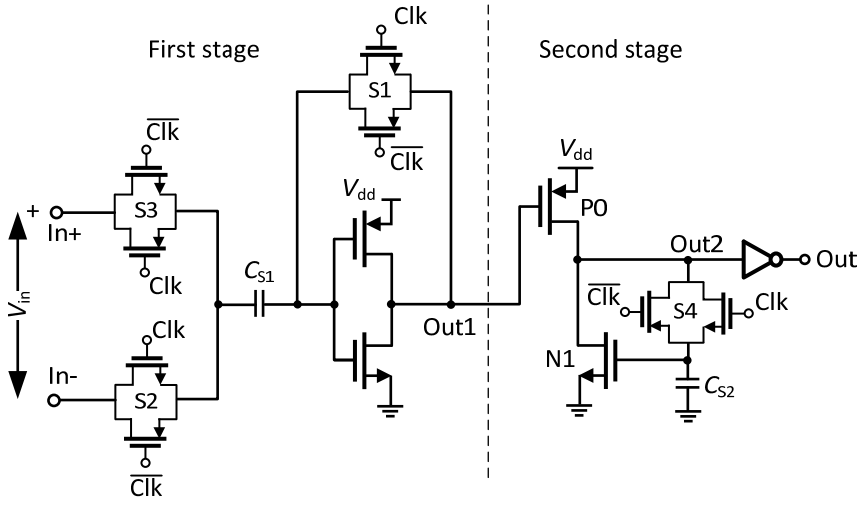


Figure 45. Schematic of the two-stage dynamic comparator manufactured in Gen.2

This comparator works as follows: During the reset phase (high Clk), the inverter is in unity-gain and V_{trip} is applied to the gate of P0, so the current of P0 is dependent on V_{trip}. This current is copied in the (in this phase) diode-connected transistor N1 (the current copier). During the comparison phase (low Clk), V_{in+}-V_{in-} (the voltage across C_{S1}) is amplified by a factor A_1 from the inverter in the first stage (V_{out1}=A_1 (V_{in+}-V_{in-})). At the same time S4 opens and the gate-source voltage of N1 is held by the capacitor C_{S2}. So, while N1 wants to keep the same value of current as when Clk was high, the gate voltage of P0 is now A_1(V_{in+}-V_{in-}). This situation causes a current-comparison at the output node (Out2) which will bring the output of the comparator to V_{dd} or ground.

To analyse the gain of each stage of this comparator, we need to take into account the large parasitic capacitances shown in Figure 46 in the simplified schematic of the first and second stages of the comparator. The steady-state gains of the first and second stage can be written according to Equations (14) and (15), respectively.

$$\left|\frac{V_{\mathrm{out1}}}{V_{\mathrm{in1}}}\right| \approx \frac{C_{\mathrm{S1}}}{C_{\mathrm{P1}}} = \frac{C_{\mathrm{S1}}}{2C_{\mathrm{GD}}} \tag{14}$$

$$\left|\frac{V_{\mathrm{out2}}}{V_{\mathrm{in2}}}\right| \approx \frac{g_{\mathrm{m,p}}}{g_{\mathrm{m,n}}}\left(1 + \frac{C_{\mathrm{S2}} + C_{\mathrm{P3}}}{C_{\mathrm{P2}}}\right) = 2 + \frac{C_{\mathrm{S2}}}{C_{\mathrm{GD}}} \tag{15}$$

The capacitances $C_{\mathrm{S1\text{-}2}}$ and $C_{\mathrm{P1\text{-}3}}$ are indicated in Figure 46, C_{GD} is the gate-drain capacitance of the OTFTs, $g_{\mathrm{m,p}}$ and $g_{\mathrm{m,n}}$ are the transconductances of p- and n-type OTFTs P0 and N1, respectively, which are assumed to be equal. In addition, despite the 1/2 ratio used for p- and n-type OTFTs, it is assumed that the parasitic capacitance of the OTFTs is equal. This is a valid assumption since the dominant part of the parasitic capacitance, which is related to the area of the semiconductor islands, is equal for these OTFTs (See Equation (10)).

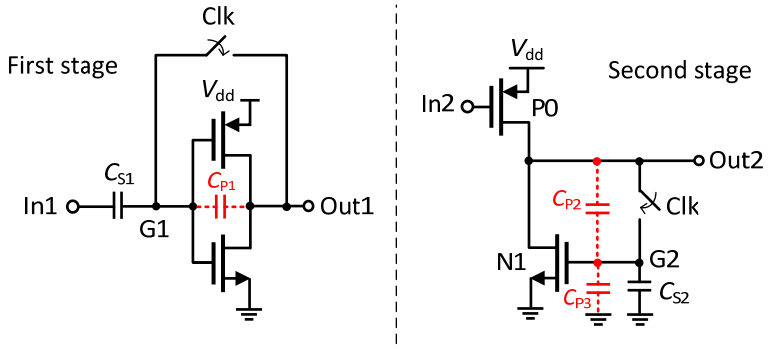


Figure 46. Simplified schematic of the two stages of the comparator in Figure 45 including parasitic capacitances

Equations (14) and (15) show that to achieve the same gain, C_{S1} needs to be more than twice as large as C_{S2}. Typically C_{S1} is chosen not only based on the gain requirements, but also on minimization of the effect of clock feed-through and charge injection of the switches at the input node (In1 in Figure 46). These effects can dramatically affect the sensitivity of the comparator and are much stronger on the Capacitance C_{S1} (to which connect three switches) than on C_{S2} (only one switch). In our design C_{S1} and C_{S2} are 500 pF and 50 pF, respectively.

It is worth noting that the parasitic capacitances C_{P1} and C_{P2} play a positive role in reducing voltage variations as a result of the charge injection and clock feed-through

at the “hold” nodes G1 and G2. Indeed the voltage change due to switching charge injections at the nodes G1 and G2, which we indicate with ΔV_{g1} and ΔV_{g2} respectively, can be expressed as:

$$\Delta V_{g1} = \frac{q}{(C_{S1} + (1 + A_1)C_{P1})} \tag{16}$$

$$\Delta V_{g2} = \frac{q}{(C_{S2} + (1 + A_2)C_{P2})} \tag{17}$$

q is the injected charge, and A_1 and A_2 are the DC gains from G1 and G2 to the output nodes Out1 and Out2, equal to $(g_{m,p}+g_{m,n})R_{out1}$ and $g_{m,n}R_{out2}$, respectively.

The important drawback of the current copier comparator is its limited input range, but this is not an issue in our case as the bias point of the second stage is fixed by the trip point of the inverter.

The measurement results of one sample of the two-stage comparator of Figure 45 [100] are shown in Figure 47. Here the voltage at nodes Out2 and Out are shown for f_{Clk}=70 Hz and V_{in}=+0.4 V and -0.4 V. The output is valid during the Clk-low phase, and settles in 3 ms. Other samples of the comparator have been measured and demonstrated similar performance. Specifically, a comparator with minimum resolvable input of ±0.3 V at 70 Hz could resolve a 50-mV change at the input when measured at 20 Hz. The better accuracy at lower clock frequency is not surprising, as small input overdrives always result in a slower comparator response (the so-called comparator time-walk). This measurement result, shown in Figure 48, proves that despite the high parametric variations in printed OTFTs, it is still possible to achieve a sensitivity as good as 0.16 LSB at 7-bit resolution level (50 mV at 40-V supply) using a simple but effective architecture.

The same sample of comparator was also measured at a supply voltage of 20 V instead of the usual value of 40 V, achieving a sensitivity of 200 mV at f_{Clk} of 20 Hz. Therefore, depending on the required speed, this architecture could also be used at lower supply voltage with a reasonable accuracy. This is an important advantage of such architectures compared to SC OTA-based architectures as that in [112] which, in

the same technology, works at a minimum supply voltage of 50 V.

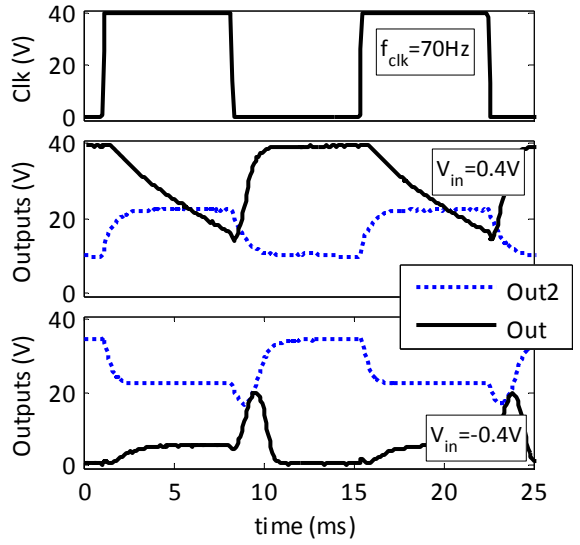


Figure 47. Measurement of the Gen.2 two-stage comparator (Figure 45) at f_{clk}=70 Hz and V_{in}=±0.4 V

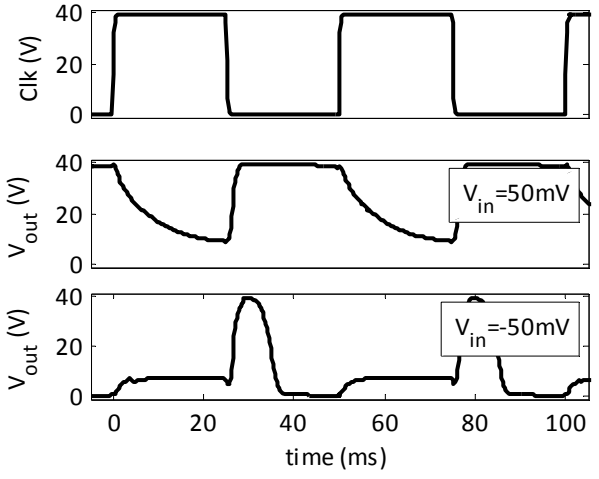


Figure 48. Measurement of the Gen.2 two-stage comparator (Figure 45) at f_{clk}=20 Hz and V_{in}=±50 mV. Only V_{out} (the voltage at node Output) is shown.

The above measurements were performed by applying and external clock signal (Clk_{ext}), while Clk and $\overline{Clk}$ were generated on-foil using a cascade of inverters. If Clk and

$\overline{\text{Clk}}$ signals are fully symmetrical, the clock-feed through errors could be eliminated thanks to the use of CMOS switches (TGs). To investigate the effect of clock-feed-through on the comparator sensitivity, the comparator was also measured by applying both Clk and $\overline{\text{Clk}}$ signals externally. In this case, the comparator resolved voltages as small as 0.2 V at 70 Hz (compared to 0.3 V at a similar condition with internal clock signals). As expected, due to the large value of geometric (overlap) capacitances, clock-feed through plays an important role in limiting the sensitivity, even though the use of TGs reduces this effect. The use of a clock generator that can better control Clk and $\overline{\text{Clk}}$ signals could improve the accuracy at the expense of more area consumption.

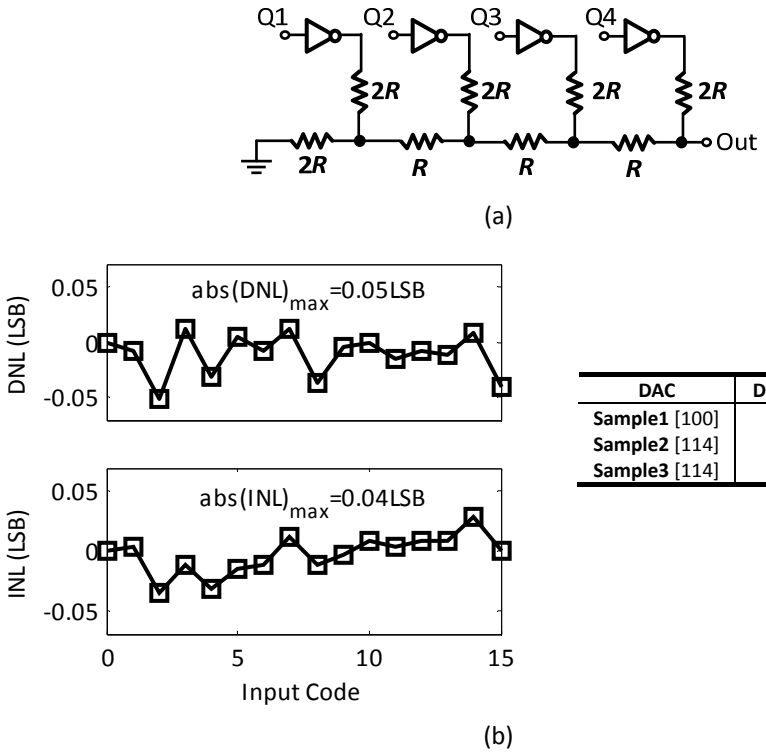
5.2.3 DAC

As a component typically used in analogue to digital converters (ADC), a digital to analogue converter (DAC) has typically a dominant effect on the linearity of the ADC system [100]. In a printed circuit, the use of capacitors or resistors as the main components of the DAC can improve this linearity, by providing a better matching compared to printed OTFTs. Indeed, the electric characteristics of resistors or capacitors depend on far less process steps and material properties than the characteristics of OTFTs, and thus resistors and capacitors are typically better matched than TFTs. Since the use of capacitors in the S2S process is impractical, due to leakage currents at the low frequencies (~100Hz) typical of organic circuits, resistors are preferred. In addition, the high resistivity of resistors in S2S technology (nominal value 35 kΩ/sq) allows us to use a smaller area compared to capacitor-based options.

We designed and implemented a 4-bit R-2R DAC shown in Figure 49(a) [100], [114]. The size of the unit resistors (6 MΩ) was chosen to ensure a negligible effect of the on-resistance of the inverters used at the input of the DAC on the ADC's linearity, and without limiting the speed of the system the circuit is part of ($\tau = RC_L = 0.1\ ms$). To give an example, the clock period (t_{clk}) of the comparator for an acceptable accuracy is 14 ms).

Three samples of the DAC were measured (on different foils), achieving in the best case a maximum integral nonlinearity (INL_{max}) of 0.05 LSB and maximum differential nonlinearity (DNL_{max}) of 0.04 LSB [114]. Figure 49(b) shows the measured DNL and INL

of this sample, and summarises the measurement results of three samples. In the worst case, maximum DNL is 0.24 LSB, and maximum INL is 0.42 LSB [100].



DAC	DNL_{max} (LSB)	INL_{max} (LSB)
Sample1 [100]	0.24	0.42
Sample2 [114]	0.05	0.04
Sample3 [114]	0.08	0.07

Figure 49. (a) Schematic of 4-bit R-2R DAC, (b) The measured DNL and INL of one of the ADC samples (figure), and the absolute value of the measured maximum DNL and INL of three samples (table).

The best sample was also measured at 20 V, showing an INL_{max} of 0.07 LSB at 4 bits or around 0.1 V. This is almost equal (slightly better probably due to measurement errors) to the DAC measured at 40 V with an INL_{max} of 0.125 V. This shows that the printed resistors nonlinearity is dominant and the effect of the inverters resistance (which is affected by the supply voltage) is negligible. Therefore, it is possible to use the R-2R DAC at lower supply voltages with a reasonable performance.

5.2.4 Rectifiers

An important challenge for OTFTs is the high frequency (HF) performance and rectification efficiency needed by applications such as RF energy scavenging in passive

RFIDs. Indeed, working at frequencies above a few megahertz is challenging for organic TFTs, since mobility typically does not exceed 0.5-1 cm^2/Vs [115]-[116] and the parasitic capacitances are large. Moreover, the typical high threshold voltage of OTFTs greatly impacts the rectifier power conversion efficiency (PCE). State-of-the-art organic rectifiers adopt either vertical Schottky diodes [117]-[118] or diode-connected OTFTs. The former provide the best performance in terms of operating frequency thanks to the very thin organic semiconductor layer. The latter are preferred when the rectifying diode has to be embedded in a complete RFID system, as it avoids specific technology steps and reuses the OTFTs [117]. However, in this case the rectifier performance is affected by the large channel length and thus by the long time-of-flight[21] of the charge carriers in the channel. This problem is particularly severe in printed OTFTs (which have a minimum practical channel length of 10 µm and very large parasitic capacitances due to the semiconductor island outside the channel).

To investigate experimentally the performance of an S2S printed OTFT used as rectifying device for the HF RFID frequency (13.56MHz), we measured a diode-connected OTFT with an external load under different input and load conditions. The adopted measurement setup for the rectifier characterization is shown in Figure 50 [91]. Measurements were carried out on foil by means of a Cascade Summit 12000 prober. The output voltage was measured by means of a semiconductor parameter analyser. The proposed setup was preferred to a resistive load configuration since it allows characterization for different input signal amplitudes at a constant load current (I_L). The rectifier performance was also explored at different input frequencies. A discrete C_L of 100 nF was used. The measurements were performed in both Gen.1 and Gen.2 versions of S2S technology.

Gen.1: For Gen.1, a p-type transistor was used as the rectifying device due to its better mobility. The OTFT *W* and *L* are 36000 µm and 10 µm, respectively. The minimum channel length was adopted for better frequency behaviour, though in other digital and analogue circuits the minimum channel length adopted is 20 µm.

[21] From the definition of mobility, assuming a constant electric field in the channel, we have $t_{flight} = L^2/\mu V_{DS}$

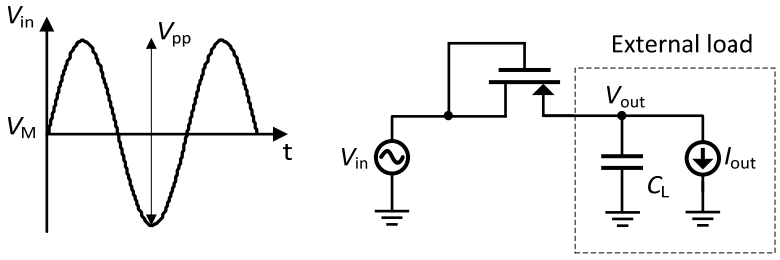


Figure 50. The measurement setup of rectifier/envelope detectors

Figure 51 shows the measured output voltage (absolute value) of the Gen.1 rectifier at different frequencies (100 Hz to 13.56 MHz) and load currents (0 to 100 nA). For these measurements the input signal has an average value V_M = -25 V, and a peak-to-peak value V_{PP} = 30 V, so the peak voltage value experienced by the rectifier is -40 V. At quasi-static frequencies (100 Hz) and when no current is driven from the rectifier (I_L=0), the voltage drop from the peak value is close to V_b, the gate-source voltage needed to start strong accumulation, equal to -3.7 V for a p-type Gen.1 OTFT (See Equation (4)-(5) and Table 4). Driving even very small amounts of current (10 nA and 100 nA) causes a higher drop at the output voltage, due to the channel resistivity which is characterized by parameters such as the threshold voltage, V_T.

By increasing the frequency, the actual rectifier performance degrades regardless of the load current. At around 10 kHz (called here knee frequency), the rectified output voltage at I_L of 100 nA starts to have a significant drop compared to the low-frequency value. As illustrated in the Figure 51, the low-frequency performance is well estimated by simulations, while the performance degradation at higher frequencies is not predicted well by the model. Indeed, the model does not include the high frequency effects such as lowering of the effective mobility which could be due to a less efficient hopping transport when the time available for carriers to hop is remarkably reduced. At 13.56 MHz, the rectified output voltage drops by 10% and 18% when measured at 10 nA and 100 nA load currents, respectively. These results are obviously dependent on the transistor width.

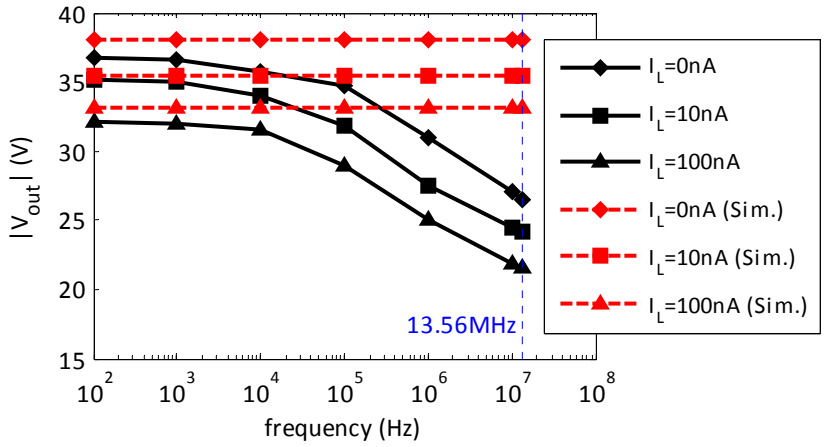


Figure 51. Gen.1 Rectifier output voltage (absolute value) as a function of input frequency at different load currents. Solid lines show measurement results and dashed lines show simulations. The input V_M and V_{pp} (Figure 50) are -25 and 30 V, respectively.

The characteristics of the rectifier are further explored in Figure 52 which shows the rectifier output voltage (absolute value) for two different values of V_{PP} (15 V and 30 V) under an open-circuit condition (I_L = 0 A). At quasi-static frequencies (100 Hz), the output voltage drop compared to the input voltage peak (-32.5 and -40 V) is almost equal and around 3.3 V for both cases. Therefore, the rectified voltage is considerably higher for the larger V_{pp}, as expected. The output voltage starts to decrease when the frequency is increased in both cases. At higher frequencies (>100 kHz), this decrease becomes more dramatic for V_{out} at V_{pp}=30V, so that at 13.56 MHz, V_{out} value is quite close for the two cases. This trend may indicate that the low-frequency performance of the rectifier is limited by the OTFT threshold voltage, and thus, the larger overdrive leads to a considerably larger output. The high frequency behaviour, on the other hand, is compatible with a mobility-limited performance, so that at high frequencies the large overdrive is not as effective as it is at low frequencies.

Gen.2: In the Gen.2 version of the S2S technology, the OTFT mobility has been increased by about a factor 10 compared to that in Gen.1 and, thus, an improvement in the high-frequency performance of the transistors is expected. Therefore, we used both p-type and n-type diode-connected OTFTs with *W* of 2000 µm and *L* of 10 µm

and measured the resulting rectifier in a similar way as done for Gen.1 OTFTs. Several samples were measured on a specific S2S foil, showing similar results.

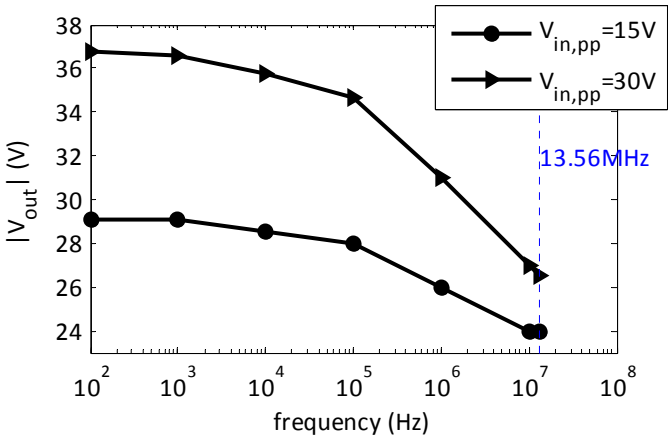


Figure 52. Gen.1 Rectifier output voltage as a function of input signal amplitudes for different input frequencies (I_L = 0 A)

Figure 53 shows the measured output voltage of one Gen.2 rectifier at different frequencies (from 100 Hz to 13.56 MHz) and load currents (0 to 100 nA for p-type and 0 to 10 nA for n-type). For these measurements the input signal has an average value V_M = ±25 V, and a peak-to-peak value V_{PP} = 30 V (to have a peak value of +40 V for n-OTFT and -40 V p-OTFT). For both transistor types, at quasi-static frequencies (100 Hz) and no output current (I_L=0), the voltage drop from the peak value is close to V_b which has a nominal value of 7.3 V for n-OTFTs and -5.4 V for a p-OTFTs in Gen.2 (See Table 6). In this case, the frequency at which the rectified output voltage at I_L of 100 nA starts to have a significant drop (knee frequency) is around 100 kHz for p-type and 10 kHz for n-type OTFT (which can be explained by the difference in mobility).

The rectifier output voltage for two different values of V_{PP} (15 V and 30 V) under an open-circuit condition (I_L = 0A) is shown in Figure 54. The general trend is similar to that observed in Gen.1. Similarly, having a higher V_{pp} is less effective when the frequency is high. However, there is still a considerable difference between the output values at 13.56 MHz, especially for the p-type rectifier. In other words, having a higher overdrive voltage is more effective in the Gen.2 rectifier, due to the higher mobility. Therefore, using threshold voltage cancellation techniques could still improve the

performance of the Gen.2 rectifiers, even at high frequencies.

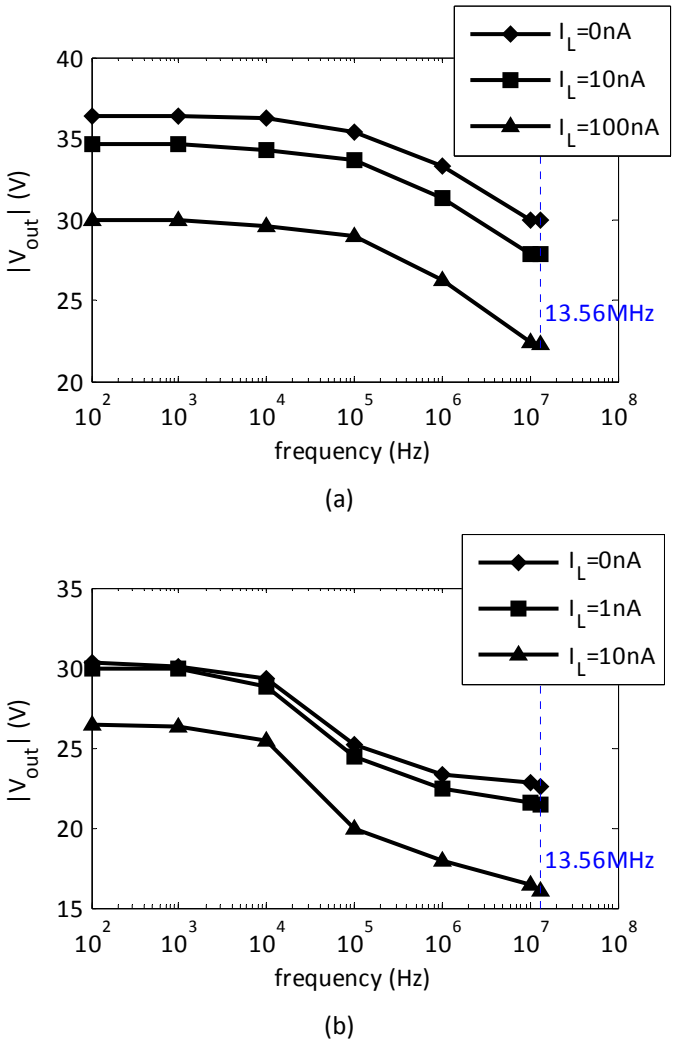


Figure 53. Gen.2 Rectifier output voltage (absolute value) as a function of input frequency at different load currents for (a) a p-OTFT and (b) an n-OTFT. V_M and V_{pp} (Figure 50) are -25 and 30 V, respectively.

To further compare the results of Gen.1 and Gen.2, the sizes (W/L) of the transistors used in the rectifier (2000µm/10µm and 36000µm/10µm, respectively) must be taken into account. It can be concluded that for a similar current density a Gen.2 rectifier has a significantly higher output voltage than that of Gen. 1. Moreover, as depicted in Figure 51 and Figure 53(a), the knee frequency of a p-type Gen.1

rectifier is an order of magnitude higher.

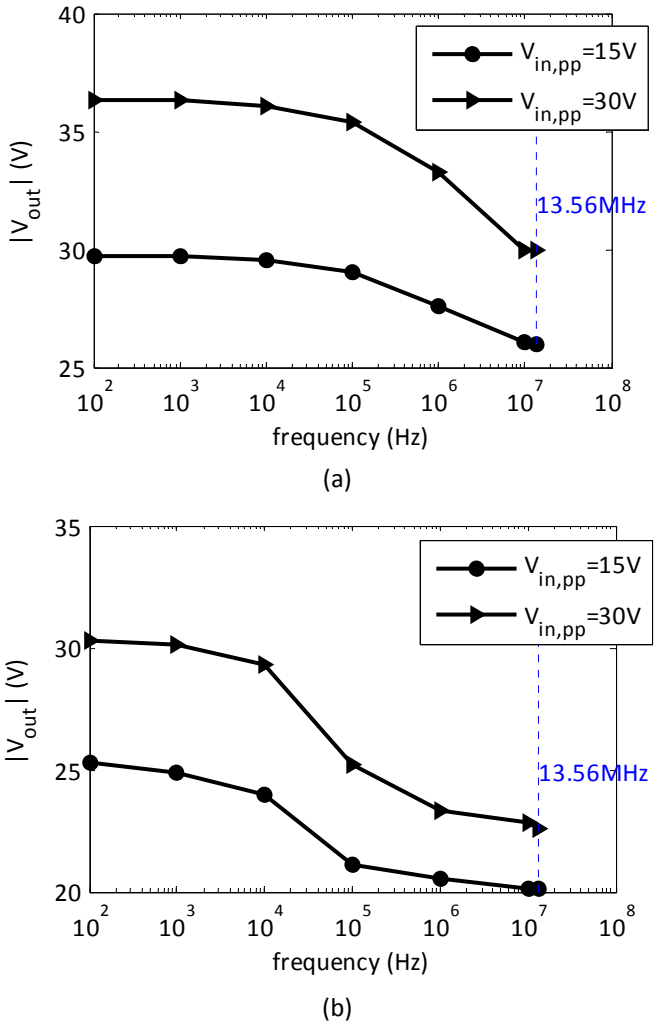


Figure 54. Gen.2 Rectifier output voltage as a function of input signal amplitudes for different input frequencies in (a) a p-OTFT and (b) an n-OTFT (I_L = 0 A)

It should be mentioned that the performance of rectifying diodes is strongly affected by mobility and sub-threshold slope, the parameters that change remarkably on different foils. Therefore, the performance of the rectifiers on different foils is quite different.

In Gen.2, we also designed and measured a four-stage rectifier based on the

Dickson charge pump [119] with only a single-ended AC input source. A simple two-stage charge pump (voltage doubler) employing diode-connected p-OTFTs (due to their better mobility compared to n-OTFTs in S2S technology) is shown in Figure 55(a). The DC input has been grounded, as required by passive harvesting applications. Since the performance of such a circuit is substantially affected by the threshold of the transistors [120], threshold voltage cancellation techniques are usually employed, as shown in a simplified schematic in Figure 55(b).

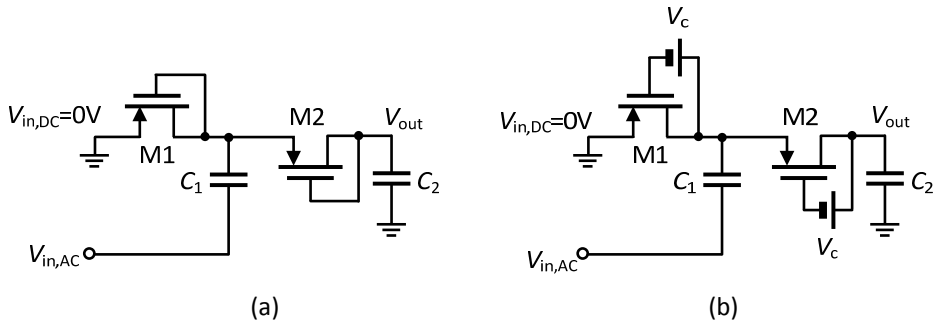


Figure 55. (a) A 2-stage charge pump (voltage doubler), and (b) a simplified schematic for the charge pump incorporating threshold-cancellation techniques

Since in S2S technology the threshold voltage is quite high (around 20 V), the threshold cancellation technique explained in [120]-[121] has been incorporated in our rectifier shown in Figure 56(a). The voltage waveforms at the nodes of the rectifying chain in a Dickson-like charge pump have equal AC amplitudes, alternating phases, and progressively increasing DC components. These inherent properties of the voltage waveforms can be employed to generate a bias offset between the gate and drain terminals of the transistors, in a way similar to that shown in Figure 55(b). This results in an effect similar to reducing the OTFT threshold voltage [121].

As shown in Figure 56(a), in our four-stage rectifier the gate of the p-OTFTs is not shorted to its drain, but is connected to another node on the chain which provides a lower DC voltage, at the same AC phase. For example, the gates of M2 and M3 is connected to V_0 (ground) and V_1, respectively. In case of M4, the gate could be connected either to V_2 or V_0, the nodes in the chain that provide a DC voltage lower than the voltage at M4 drain (V_{out}). In this circuit, the gate is connected to V_0 which

has a lower DC voltage compared to V_1. This choice results in a higher V_{GS} for M4 which is especially suitable for low peak-to-peak inputs, but can result in large reverse currents in M4 when V_{out} goes higher than the OTFT threshold voltage. The first OTFT in the chain (M1) is an n-type so that its gate can be connected to a higher DC voltage generated by the chain (A p-OTFT must remain diode-connected). Similar to M4, M1's gate could be connected either to V_{out} and V_2, and in this case V_{out} has been preferred. This threshold cancellation technique, together with the multiple-stage approach, was used to enable a reasonable V_{out} at lower peak-to-peak input voltages.

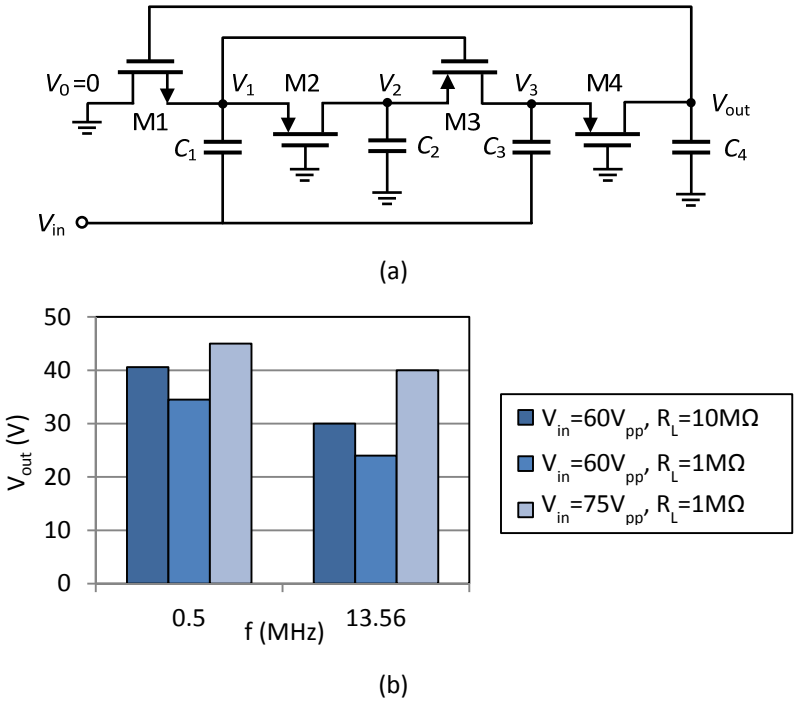


Figure 56. (a) Schematic of a 4-stage charge pump incorporating threshold voltage cancellation (b) the measured rectifier output (V_{out}) under different load and input conditions

Figure 56(b) shows the measured V_{out} of the rectifier under different load and input conditions. Specifically at 13.56 MHz, the rectifier with 1 MΩ load (R_L) generates 40 V and 24 V for input peak-to-peak voltages ($V_{in,pp}$) of 75 V and 60 V, respectively. It is important to notice that the input RF wave, in this case, has an average value of 0 V, as it will happen in the actual RFID tag. As discussed in Chapter 8, the foreseen load of

our RFID tag is 1 MΩ. The rectifier, thus, is able to generate the required voltage (as high as 40 V) to power the HF RFID tag, even if it requires a rather large peak-to-peak input voltage.

5.2.5 AM demodulator

Demodulation is an enabling function in applications such as RFID tags based on the standard "reader talks first" concept, where the RFID tags must have the capability to receive enabling messages coming from the interrogator (as in a silent tag). The main building blocks of an AM demodulator, as shown in Figure 57(a), are an HF envelope detector and a voltage comparator. The envelope detector extracts the low-frequency envelope from the high-frequency carrier, and the comparator converts the envelope signal in a full-swing output data stream, providing the demodulated signal.

Here we first employ the measured Gen.1 envelope detector (Figure 50) and the two-stage continuous-time comparator (Figure 43) to simulate a complete AM demodulator system. The envelope detector is implemented with a rectifying device and an RC series load that is chosen according to the envelope frequency to provide a first-order low-pass filtering in the voltage domain. This simulation was performed in order to study the functionality of the measured building blocks when combined to form the AM demodulator of Figure 57(a).

The simulation results are shown in Figure 57(b) [91], where an 80-$V_{p\text{-}p}$ signal is applied to the input. A data rate of 10 Hz was chosen, which is reasonable based on comparator measurements. The carrier frequency for simulation was set to 10 kHz, since it is the highest frequency at which the simulation and measurements of the envelope detector are in close agreement. At this frequency, a modulation index of 30% is large enough to surpass the offset of the comparator and achieve correct functionality. The lowest graph of Figure 57(b) shows the output of the comparator when either a single-stage OTA (Figure 40(a)) or a two-stage OTA (Figure 43(a)) are employed as a comparator.

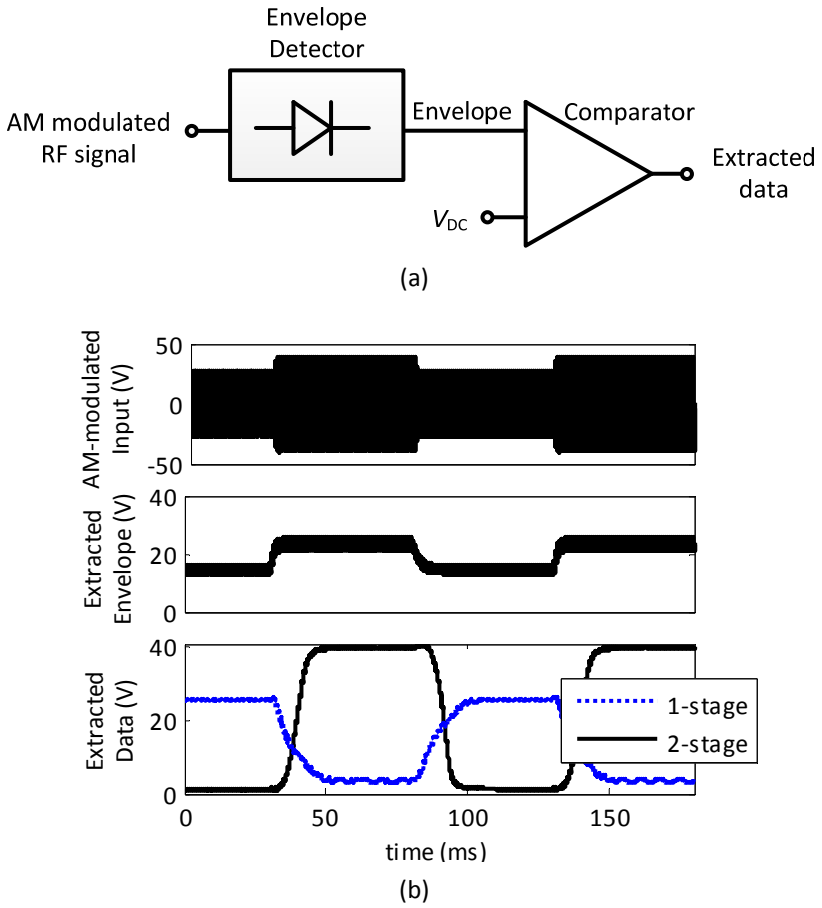


Figure 57. (a) Structure of a demodulator for recovering an AM-modulated data, (b) AM-demodulator simulation. The extracted data is shown for a single-stage OTA (Figure 40(a)) or a two-stage OTA (Figure 43(a)) are employed as a comparator.

At the high frequencies needed for practical applications, the performance of the envelope detector degrades and an increase of the modulation index would be required. To avoid the need to increase the modulation index, which is inconvenient from the point of view of the reading distance and requires large DC storage capacitors on the tag, it is necessary to improve the circuit performance. From the technology perspective, this can be done by increasing the OTFT mobility (as has been done indeed in Gen.2) and lowering its threshold. From the circuit perspective, the negative effect of the threshold voltage on the envelope detector can be reduced using rectification schemes including threshold cancellation. The offset in the

comparator can be also reduced for example using auto-zeroing techniques. To further study the performance of the circuits for practical applications at HF, a model that takes into account the effects of charge transport characteristics on high-frequency performance of OTFTs would be needed. This is a complex modelling problem which is beyond the scope of this work and is open for further investigations.

5.3 W2W OTA

Simple single-stage OTAs similar to those in S2S technology were included in W2W masks to provide a basic estimation of analogue circuit performance in W2W OTFT technology. The OTAs incorporating an n-type input differential pair (which in W2W have a better mobility compared to p-type OTFTs) is depicted in Figure 58(a).

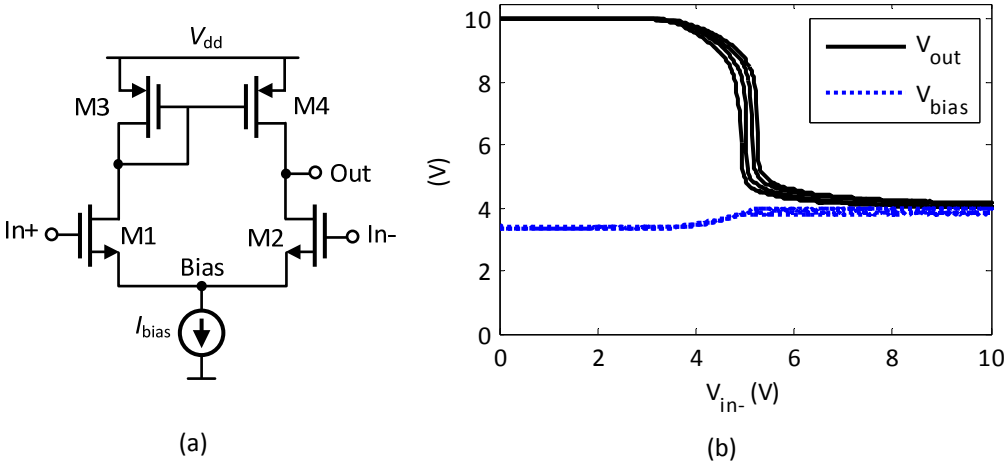


Figure 58. (a) Schematic of the OTA implemented in W2W technology, (b) Measurements of two samples of OTA: the voltages at the bias and output nodes are measured when In+ is set to 5 V and the voltage at In- is swept. I_{bias} is 1 µA.

Figure 58(b) presents the measurements of two samples of the OTA. The circuit was measured quasi-statically while In+ was set at a specific voltage and the other input was swept back and forth from 0 to 10 V. An external bias current (I_{bias}) of 1 µA was applied and the voltages at the bias node and output node were measured. The worst-case measured output offset and hysteresis are 0.3 V and 0.15 V, respectively. This offset corresponds to around 0.5 LSB at a 4-bit resolution and 10-V supply. The gain ranges from 34 to 36.4 dB (biased in sub-threshold regime). This shows the

potential of W2W technology to implement OTAs with relatively high gain and reasonable offset. The use of SC-based architectures, however, could result in unreliable circuits due to the probability of the switches being normally on (See Section 4.3.3).

5.4 Analogue design highlights

In this chapter we showed that, using simple non-differential architectures incorporating offset-cancelling techniques, it is possible to implement circuits with a very good accuracy in a printing organic technology including complementary transistors. The use of linear resistors together with such techniques can help us to implement systems with accuracies which are high-enough for the applications targeted by organic electronics. S2S OTFTs can also be used in HF rectifiers and envelope detectors for power scavenging purposes in passive RFID tag systems.

PART II

IMPLEMENTED SYSTEMS-ON-FOIL

6 Display Driver

In this chapter a low-voltage line driver for displays designed and fabricated in a complementary organic technology on foil (W2W) is presented. The line driver topology is chosen based on the statistical characterization of the fabricated TFTs. The 32-stage fully-static line driver including buffers comprises 1216 transistors. It works at supply voltages as low as 3.3 V, reaching a 1-kHz clock frequency, and occupying an area of 25x4.7 mm^2. The complementary TFT technology is compatible with the process used to manufacture flat-panel display backplanes and the line driver is successfully tested with a QQVGA OLED-based display.

6.1 Introduction

The fact that OTFTs can be manufactured on large-area flexible substrates makes organic electronics a promising platform for manufacturing large and fully-flexible active-matrix displays [22]-[23]. The realization of OTFT-based driving circuitry in a technology compatible with that of the display backplane allows the integration of driving circuitry with e.g. active-matrix light-emitting diode (AMOLED) displays, to achieve a fully-flexible system. This integration will also reduce the cost of the complete display module and increase the system reliability by reducing the footprint, the number of interconnects, and manufacturing complexity [45].

For organic display drivers, the performance demanded by commercial displays is challenging in terms of speed and power consumption. Nearly all state of the art organic drivers (e.g. [45] and [46]) are indeed implemented using p-only technologies, which have potentially higher power consumption and lower speed compared to complementary technologies. A complementary organic technology was developed in [14] and exploited to fabricate a 48-stage shift register which could be used as a line driver. Nevertheless, the high supply voltage (80 V), required by the thick gate dielectric used, makes this solution unusable for portable battery-powered equipment, where power consumption is a major concern [54], [45].

In this chapter, we use the W2W technology (Described in Chapter 2) to manufacture a line driver on foil, which is presented in Section 6.2. The driver is tested with QQVGA OLED displays. This system test is discussed in Section 6.3 and some conclusions are drawn in Section 6.4.

6.2 Line driver circuit

Although printed OTFT-backplane for AMOLED displays have also been shown [122], the current FPD technology is most compatible with technologies similar to the W2W approach. Figure 59(a) depicts the schematic of a 32-stage line driver, which is a shift register generating sequential voltage pulses for addressing the rows of a matrix backplane. Based on the considerations about architecture choices in W2W technology, a fully-static line driver based on the D-FF of Figure 36 was implemented for the system tests. As explained in Section 4.2 and based on W2W OTFT variability

studies, this circuit topology provides a reliable solution. The designed line driver comprises 1216 OTFTs and has an area of 25x4.7 mm^2. This is the highest transistor count ever reached by an organic complementary circuit to date. The highly-integrated complementary OTFTs in W2W technology allow for implementation of a robust fully-static line driver without excessive area consumption.

As depicted in Figure 59(b), the complementary line driver works at a supply voltage as low as 3.3 V with f_{clk} equal to 1 kHz [96]. This is the lowest supply voltage achieved by an organic line driver. The clock frequency reaches 2.4 kHz at a 10-V supply voltage. Power consumption can be estimated to 2.3 µW/stage for a 3.3 V supply. Such low-voltage driving circuitry is compatible with portable and low-power applications and could enable integration with Silicon electronics without the need for specific interfaces.

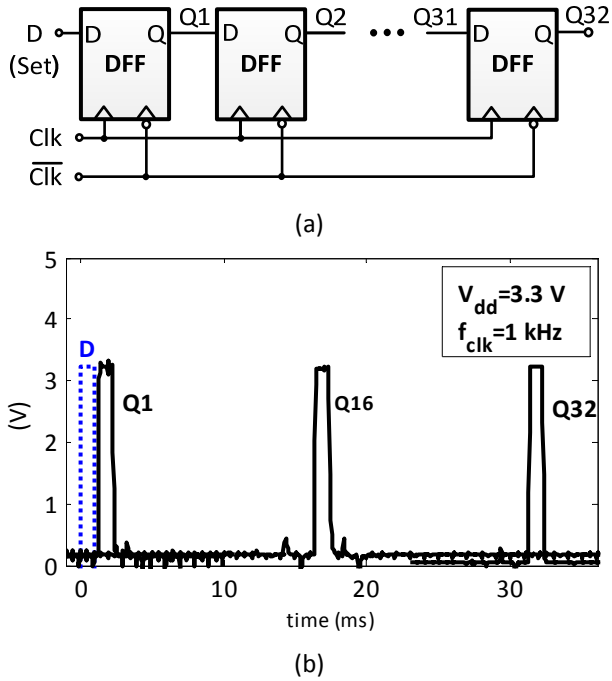


Figure 59. (a) The schematic of a 32-stage line driver, (b) measurements of the driver: Q1, Q16 and Q32 are shown.

Table 10 summarises the characteristics of the line driver in this work and compares it with some organic line-drivers/shift-registers reported in literature. It

should be noted that [45] and [47] need a suitable DC tuning voltage in addition to the supply voltage. We can observe the remarkably lower power consumption even compared to the complementary shift register in [14], due to the low supply voltage used. Even at this low supply voltage, the speed is much higher than that in [47] and is in the same order of magnitude of that reached in [45] and [46]**.** Of course, p-only technologies are in a more advanced state in terms of hard yield and, as a result, the level of complexity (number of OTFTs and stages) is higher in recent p-only line drivers [46]**-**[47]. The display driver in this work has the highest number of OTFTs in a complementary organic circuit to date [96]. The area consumption per stage is reasonable despite the use of a fully static architecture with a high number of OTFTs. Two line drivers out of four measured were fully functional, and another one was working till the 22nd stage [96].

Table 10. Comparison of our line driver with other organic line drivers previously reported in literature

Characteristics	*[14]*	*[45]*	*[46]*	*[47]*	This work
Technology	Complementary	p-only	p-only	Dual-gate p-only	Complementary
#Stages	48	32	240	240	32
#OTFTs	864	1888	≈4000	13440	1216
V_{dd} (V)	80	25	60	20	3.3
Power (μW/stage)	120	6250	N.A.	33	2.3
f_{clk} (kHz)	0.5	5	4	0.07	1
Area (mm^2/stage)	N.A.	N.A.	N.A.	2.9	3.7*

* includes total routings (divided by the number of stages)

6.3 System test

After stand-alone measurements of the driver using a probe station, the organic circuits were connected to a system demonstrator using a mechanical connector. Figure 60 shows the block diagram of the tested system. The 32-bit line driver is connected to a (five times) tiled 160×120 QQVGA OLED display [123] through mechanical connectors (each line driver output drives five lines). Buffers were included in the organic circuit to drive the display. The Silicon test circuitry also provides buffers at the input of the display in order to enable testing the driver at different supply voltages without affecting the functionality of the display.

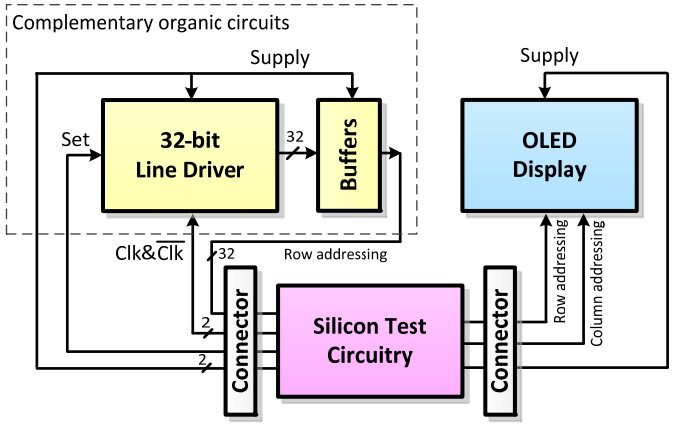


Figure 60. Block diagram of the display driver testing system

Figure 61 shows the photographs of the die containing two samples of the line driver, one of which is in contact with the mechanical connector. In addition, the photograph of the working 160×120 display is presented. The images on the display are tiled since the driver has only 32 outputs. The frame rate in this test was 30 Hz.

6.4 Highlights

In this chapter, the capability of a technology compatible with that of flat-panel displays (W2W) to manufacture line drivers on foil is demonstrated. The availability of robust and low-area line drivers in such a technology enables the integration of the driving circuitry with organic-based displays in order to achieve flexible systems at a lower cost and complexity. Furthermore, we demonstrate the feasibility of using complementary organic driving circuitry to implement portable and mechanically-flexible applications based on active-matrix displays, due to the low power consumption of the line driver. The low voltage performance of the line driver is closely compatible with Silicon electronics and AMOLED Displays based on high-efficiency OLEDs (which have around 2.5 to 3 V supply voltages [53], [124]). The speed at which the line driver is currently functional is suitable for applications such as e-reading for which a refresh rate of around 10 Hz is sufficient [46]. However, to work with AMOLED displays for advanced applications, frequencies up to 10 MHz could be required [53]. For OTFTs to perform in such applications, improvements in

characteristics including mobility (in the order of 1 cm^2/Vs) and reduced lateral dimensions (1 µm or less) are needed [53].

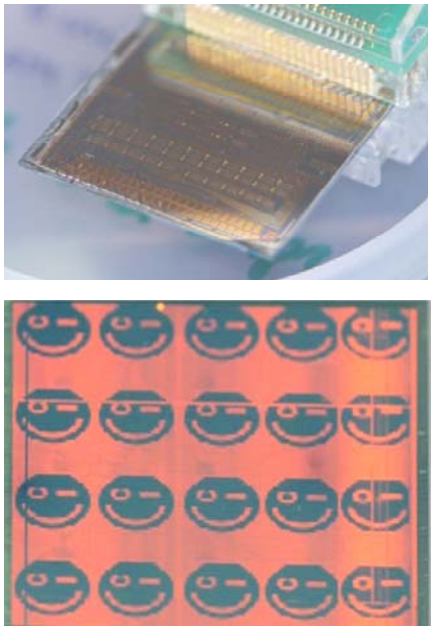


Figure 61. Photographs of a die containing two 32-stage line drivers (and other building characterization circuits) and the image generated on the display using the driver. One line driver is connected to the display through a mechanical YOKOWO connector (which can be seen in the top figure)

7 Temperature Monitor

This chapter presents two key circuits for implementing sensor-based applications in organic electronics: an ADC and a temperature sensor. The 4-bit ADC is fabricated with a printed organic complementary process (S2S technology) and features an integrated resistive DAC. Measurements of the ADC show 25.7dB SNR and 19.6dB SNDR at 2 Hz bandwidth, demonstrating, for the first time, the capability of OTFT printing technologies to fabricate data converters. According to further measurements of the ADC building blocks, achieving resolutions up to 7 bit is already feasible using the same architecture and manufacturing technology. The resistive temperature sensor is fabricated in a roll-to-roll technology on a plastic foil. The ADC is tested together with the sensor in a system to monitor ambient temperature.

7.1 Introduction

OTFTs printed on large-area thin plastic substrates enable applications exploiting sensors that do not require high-speed or high-resolution, e.g. smart surfaces and coarse ambient temperature monitors. Such devices can be printed at a low cost on, for instance, food packaging, to monitor ambient parameters such as storage temperature. This can provide the consumers with information on the exact status of the packaged food, instead of a rough and conservative estimation of the expiration date. Thus, a large part of the huge yearly food waste could be prevented.

A major block required for implementing sensor-augmented systems like temperature monitors is the ADC, which is typically comprised of several analogue and digital circuits. Although printed OTFTs have already been used to design circuits [5]-[10], this design is mainly limited to digital circuits or large-area switch matrices. As mentioned before, major challenges in the design of printed circuits are the relatively high variability in the characteristics of the OTFTs, and the high rate of hard faults (at the state of the art, yield is acceptable only for a circuit complexity of ~100 transistors). However, improved robustness to TFT variability can be enabled using a complementary technology, instead of common p-only solutions.

The goal of this chapter is to implement a temperature monitor using organic technologies. The block diagram of such a sensor-augmented system is shown in Figure 62.

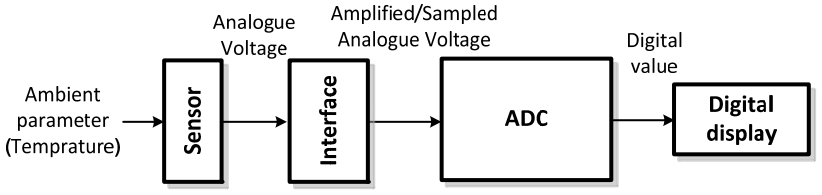


Figure 62. Simplified block diagram of a temperature monitor

The sensor reads the ambient parameter (here, temperature) as an analogue voltage which is then amplified/sampled by the sensor interface. This signal is converted to a digital value by an ADC, and sent to a digital display. Two main blocks of this system, namely the ADC and sensor implemented on foil, are presented in

Sections 7.2 and 7.3, respectively. The system test setup, which includes the presented ADC and sensor, together with its measurement results are discussed in Section 7.4, and some conclusions are drawn in Section 7.5.

7.2 ADC

The ADC is designed in the Gen.2 S2S technology (described in Chapter 2) based on the building blocks presented in Chapters 4 and 5. The structure of the designed 4-bit counting ADC is shown in Figure 63. It consists of three main blocks: a 4-bit "R-2R" DAC, a ripple counter and a comparator. The counter converts the clock signal to a BCD code, which is in turn converted to an analogue signal by the DAC (V_{DAC}). The DAC output is compared to the input signal (V_{in}) using the comparator. Whenever the comparator changes its state, the counter is stopped and the present count is the digital output (Dig-out). Since the employed comparator has an auto-zeroed architecture and its output is valid only during one clock cycle (after the settling time), a flip-flop is exploited to filter the output of the comparator and hold the valid comparison result (Stop). This result is used to generate the clock signals for the counter (Clk_C and $\overline{Clk_C}$) and stop it at the right time. The ripple counter is reset asynchronously at the end of each conversion cycle.

The ripple counter is based on the TG-based D-FF shown in Figure 29 with $\overline{Q}$ and D connected to obtain a toggle (T)-FF. The outputs of the counter (Q1-4) for a clock frequency of 67 Hz are presented in Figure 64. The design and measurements of the DAC used in the ADC are thoroughly explained in Section 5.2.3. The measurements of the ADC presented here are based on the DAC shown in Figure 49, which provides a maximum INL and DNL of 0.42 LSB and 0.24 LSB, respectively. The ADC was measured using a 67Hz Clk_{ext} input, but the measured samples of the counter were typically functional at frequencies up to 500 Hz. The design of the auto-zeroed comparator is discussed in Section 5.2.2, its schematic and measurements are presented in Figure 45 and Figure 47. The specific comparator sample used in our ADC resolves ±0.4 V at 70 Hz, equivalent to 0.16 LSB at 4 bit resolution and 40 V supply.

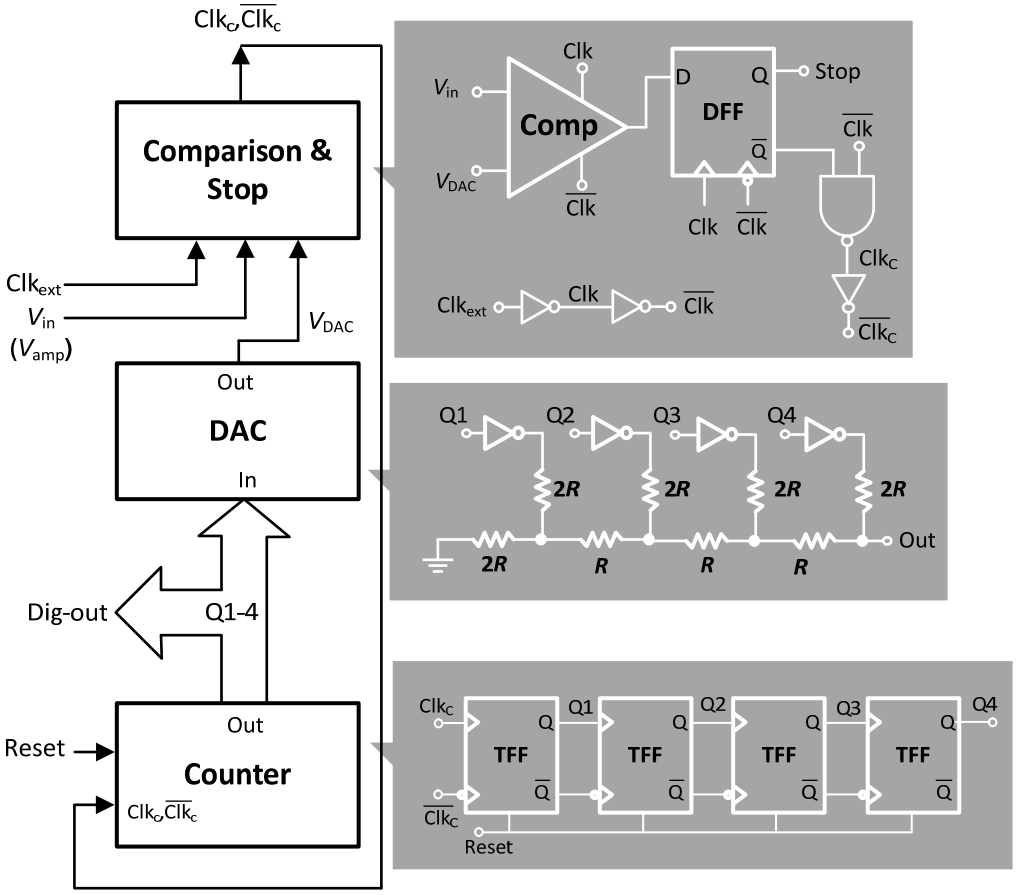


Figure 63. Structure of the 4-bit counting ADC (left) and the schematic of its building blocks (right)

Figure 65 shows the results of a dynamic measurement of the ADC [100]. Each conversion takes ~240 ms (16 clock cycles at 66.67 Hz), and the ADC sample rate is thus 4.17 Hz. The input signal is full-scale and its frequency is 2.05 Hz. First, an ideal staircase generated by a waveform generator was applied to the comparator to evaluate its performance (the graph with ideal DAC). The measured SNDR in this case is 22 dB. This value decreases to 19.6 dB when the real DAC output (without any calibration) was applied to the comparator. The SNR is in both cases about 25.7 dB. The power consumption of the full ADC at 40 V supply is 540 µW, mostly consumed in the comparator at reset phase during which the inverter is biased at V_{trip} (high gain region). The active area is 21.8 cm^2. To the author's knowledge, this is the first

reported ADC manufactured with printed electronics [100]. These measurements were performed on a foil where ADC blocks were implemented separately and were tested using external connections. The blocks were later integrated on one foil, shown in Figure 66, to form the complete printed 4-bit counting ADC whose functionality was successfully tested in the final system.

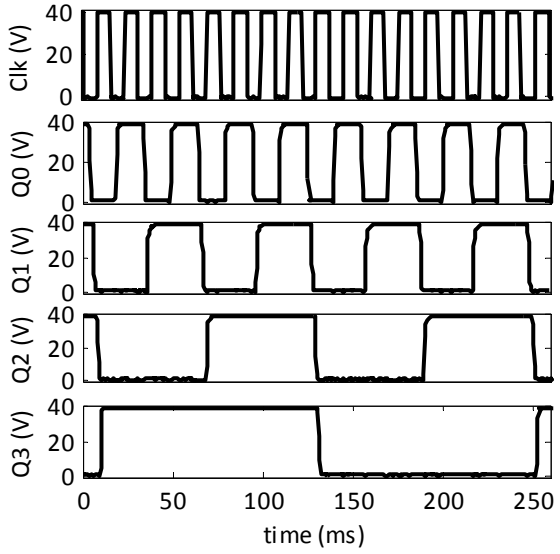


Figure 64. Counter outputs (Q1-Q4) measured at f_{clk} of 67 Hz

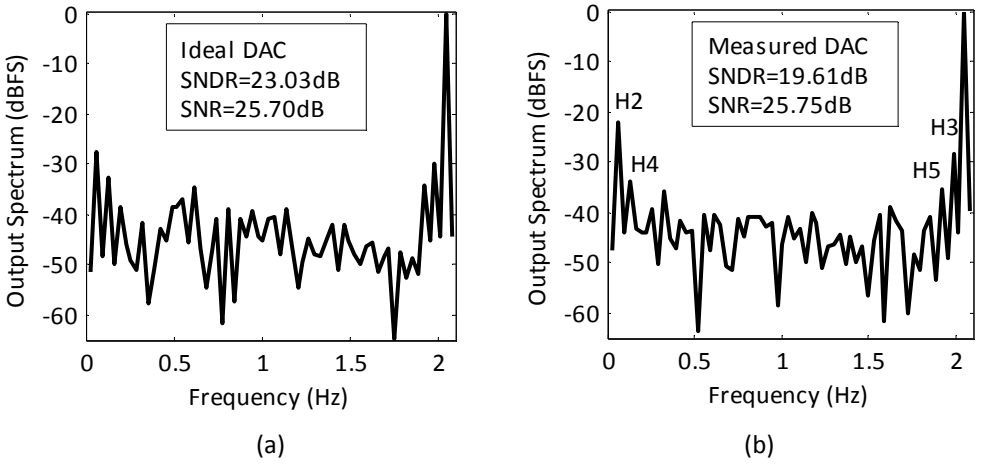


Figure 65. Measured output spectrum of the ADC (a) based on an ideal DAC (generated using a waveform generator) and (b) based on a measured DAC (H2-H5 show the first harmonics)

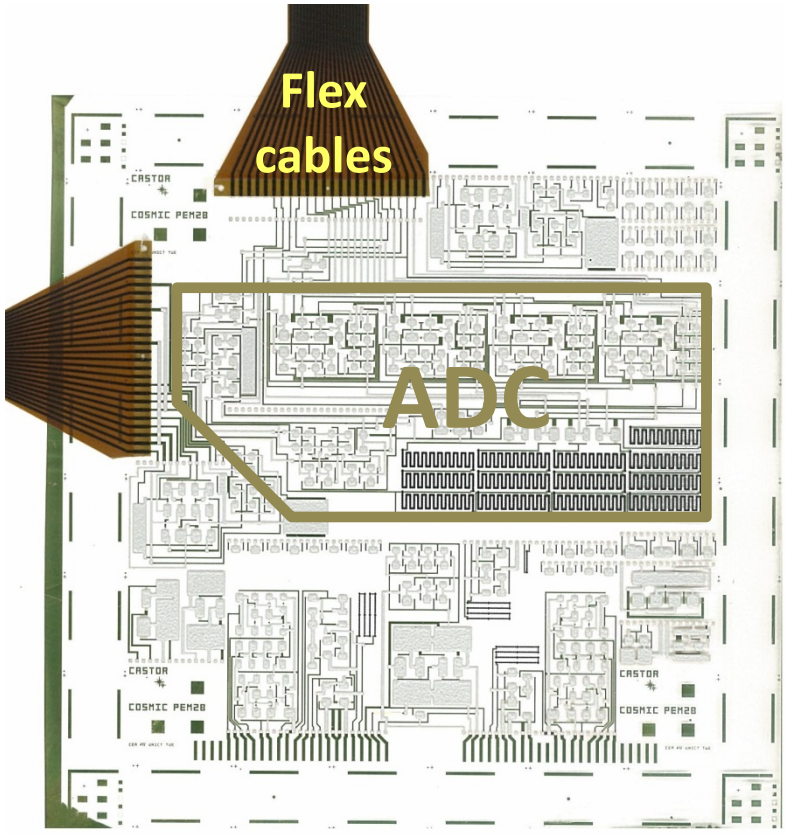


Figure 66. The foil containing the fully-integrated 4-bit counting ADC (PEM2b-top1)

The above measurements demonstrate that at 4-bit level, the DAC limits the linearity of the ADC. However, the measurements on other DAC samples from later batches (presented in Section 5.2.3) show a maximum INL of 0.05 LSB (at 4-bit resolution) which is equivalent to 0.4 LSB at 7-bit resolution level [114]. Considering that the measurements of the comparator in Section 5.2.2 have also shown a sensitivity as high as 0.16 LSB at a 7-bit resolution (50 mV at 40V supply), it can be concluded that using the same building blocks and architecture, it is readily possible to achieve higher resolutions using the S2S printing technology.

Table 11 and Table 12 provide a summary of the performance reported for state-of-the-art organic DACs and ADCs, respectively. Due to remarkable differences in the characteristics of the organic technologies employed, it is difficult to compare in detail

the performance of DACs and ADCs implemented based on OTFTs. The most important highlight about the circuits in this work is that they are implemented using printing techniques, while the other circuits are mostly implemented using more common techniques such as lithography.

Table 11. Comparison of our printed DAC with state-of-the-art organic DACs

Characteristics	*[43]*	*[44]*	**This work**	
Technology	Complementary*	p-only	**Printed** complementary	
Architecture	C-2C	Current-steering	R-2R	
Resolution (bit)	6	6	4	
#OTFTs	22 (17 capacitors)	129	8 (13 resistors)	
V_{dd} (V)	3	3.3	40	20
DNL@6b (LSB)	0.6	0.69	0.2	0.32
INL@6b (LSB)	0.8	1.16	0.16	0.28
Area (mm^2)	392	12	700	

* on glass

Table 12. Comparison of our printed ADC with state-of-the-art organic ADCs

Characteristics	*[40]*	*[41]*	*[42]*	**This work**
Technology	Dual-gate p-only	Complementary	Dual-gate p-only	**Printed** complementary
Architecture	Delta Sigma	SAR*	VCO-based	Counting-based
Resolution (bit)	4.1**	6	6	4
#OTFTs	70	53	N.A	148
V_{dd} (V)	15	3	20	40
SNR (dB)	26.5	N.A.	48	25.7
SNDR (dB)	24.5	N.A.	N.A.	19.6
BW (Hz)	15.6	100	~0.08	2
Power (μW)	1500	10.8	48	540
Area (mm^2)	260	616 (analogue only)	19.4	2180

* off-chip logic
** ENOB evaluated from the SNR

As given in Table 11, unlike the DACs in [43] and [44]**,** the DAC in this work has an architecture based on resistors which provide a better matching compared to printed OTFTs and do not suffer from droop problems at the low frequencies typical of organic circuits. The measured DNL and INL at 40 V and 20 V have been recalculated for 6-bit resolution to make comparison easier. The printed DAC shows a very good linearity. Lowering the supply voltage from 40 V to 20 V does not have a remarkable effect on DNL and INL. The high area consumption is due to the requirements of printing.

In comparison with other architectures summarised in Table 12, the architecture of our ADC is extremely simple, which makes it suitable for our printing technology. The

SAR architecture needs a more complex logic and could be employed to improve the speed, when the technology is in a more advanced state in terms of yield. The linearity in delta sigma and VCO-based architectures is highly dependent on the characteristics of OTFTs (controlled by the back gate in [40] and [42]**)**, while in our counting-based architecture it is dominantly affected by the resistors. Other characteristics of ADCs such as power and area are highly dependent on the technology employed.

7.3 Sensor

The sensor tested with the ADC is manufactured in a roll-to-roll (R2R) organic technology [125]-[126] on a polyester film treated to provide a high surface-tension, suitable for printing. Each sensor consists of two temperature-sensitive resistors used in a voltage-divider architecture. The schematic of the sensor and a foil containing several sensor samples are shown in Figure 67. The two resistors, R_{ITO} and R_{carbon}, are manufactured using two different materials, namely indium tin oxide (ITO) and carbon, with temperature coefficient of resistance (TCR) equal to -4500 ppm/°C and -400 ppm/°C, respectively.

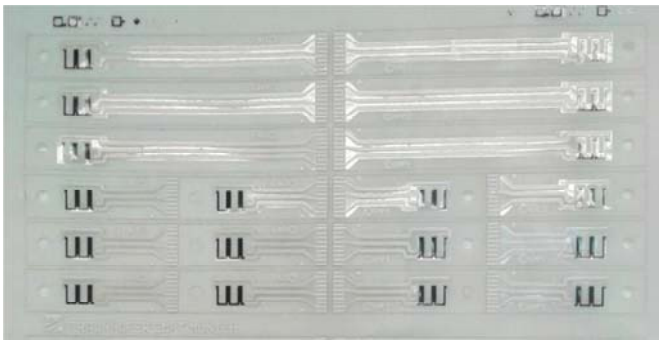


Figure 67. The schematic of the temperature sensor and the foil containing implemented sensor samples

The change of resistance ($\Delta R=R_2-R_1$) between R_2, the resistance at temperature T_2, and R_1, the resistance at temperature T_1, can be written as

$$\Delta R = \mathrm{TCR}.\Delta T.R_1 \tag{18}$$

where $\Delta T=T_2-T_1$, and TCR is the temperature coefficient resistance for the resistor under investigation.

Using Equation (18) and Equation (19) for the output of the voltage divider (V_{sense}), the change in the sensor output ($\Delta V_{sense}=V_{sense,2}-V_{sense,1}$) with temperature can be calculated as:

$$V_{\mathrm{sense}} = \frac{R_{\mathrm{carbon}}}{R_{\mathrm{ITO}} + R_{\mathrm{carbon}}} V_{\mathrm{dd}} \tag{19}$$

$$\begin{aligned} \Delta V_{\mathrm{sense}} &= \frac{2(TCR_{\mathrm{carbon}} - TCR_{\mathrm{ITO}})\Delta T}{3(3 + (TCR_{\mathrm{carbon}} + 2TCR_{\mathrm{ITO}})\Delta T)} V_{\mathrm{dd}} \\ &\cong \frac{-TCR_{\mathrm{ITO}} V_{\mathrm{dd}}}{4.5} \Delta T \end{aligned} \tag{20}$$

In the calculation it is assumed that R_{ITO} is twice larger than R_{carbon} at initial temperature ($R_{ITO,1}=2R_{carbon,1}$), which is in accordance with the values of resistors used in the implemented sensors. The approximation is valid for $|TCR_{carbon}|<<|TCR_{ITO}|<<1$ which is the case here. Under these hypotheses, for a ΔT of 1 °C, ΔV_{sense} is 40 mV at a V_{dd} of 40 V.

From Equation (20) it can be observed that ΔV_{sense} does not change linearly with ΔT. In other words, the sensitivity ($S=\Delta V_{sense}/\Delta T$) is not a constant value. This point is shown more clearly in Figure 68 where the calculated R_{ITO}, R_{carbon}, ΔV_{sense}, and S are plotted versus temperature (for $R_{ITO,1}=2R_{carbon,1}=0.7$ MΩ to be close to actual values on foil). For a range of 40 °C, the sensor sensitivity changes from 33 to 43 mV/°C, equivalent to about 10% linearity error $(S-\bar{S})/\bar{S}$ or a maximum deviation for V_{sense} from the linear curve $(\Delta V_{\mathrm{sense}} - \overline{\Delta V_{\mathrm{sense}}})$ of about 4 mV. If the sensor output is amplified by 10 using the sensor interface to be readable by the comparator of the ADC (reaching a sensitivity around 0.4 V/°C), this intrinsic nonlinearity translates to 40 mV or 0.02 LSB (at 4-bit resolution and 40-V input range) at ADC input. This amount is half of the best-case maximum measured DAC DNL (0.04 LSB). So the intrinsic nonlinearity of the

sensor is negligible compared to the nonlinearity in the ADC.

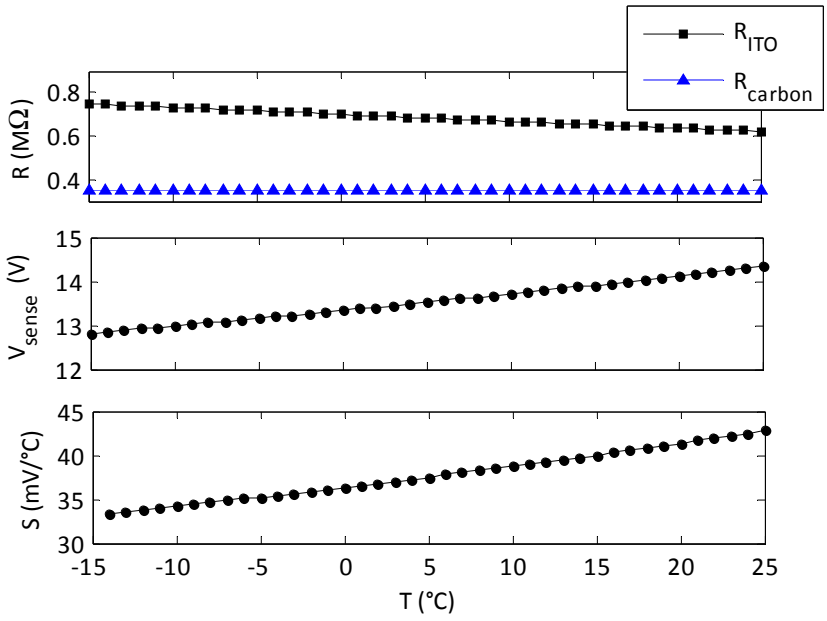


Figure 68. Calculated resistance values (R), output voltage (V_{sense}) and sensitivity (S) of the resistive sensor

The actual measured output voltages of twelve samples of the sensor are shown in Figure 69. The measurement is performed using a probe station with a thermal chuck, at a temperature range of -15 °C to 25 °C with a step of 5 °C and a supply voltage of 40 V. The trend is similar in all the cases, though the average output level is different in different cases. This is due to the different absolute value of resistors in different sensor samples. Indeed, the measurements of resistor values at room temperature (22 °C) show that the R_{ITO}/R_{carbon} ratio in these samples ranges from 1.8 to 2.4. The measured mean value of R_{ITO} is 702 kΩ, with a standard deviation of 7.5 %. R_{carbon} has a measured mean value of 343 kΩ and a standard deviation of 12.2 %.

The nonlinearity observed in the sensors can be characterized by $\Delta V_{\mathrm{sense}} - \overline{\Delta V_{\mathrm{sense}}}$. The mean value and standard deviation of the maximum non-linearity error based on the twelve measured samples are 25.7 mV and 20 %, respectively. The measured non-linearity is thus much larger than the one estimated by Equation (20). If the sensor output is amplified by a gain of 10, this nonlinearity translates to a DNL for the ADC of

around 260 mV or 0.1 LSB, still acceptable for a system with 4-bit resolution and full scale equal to the supply voltage.

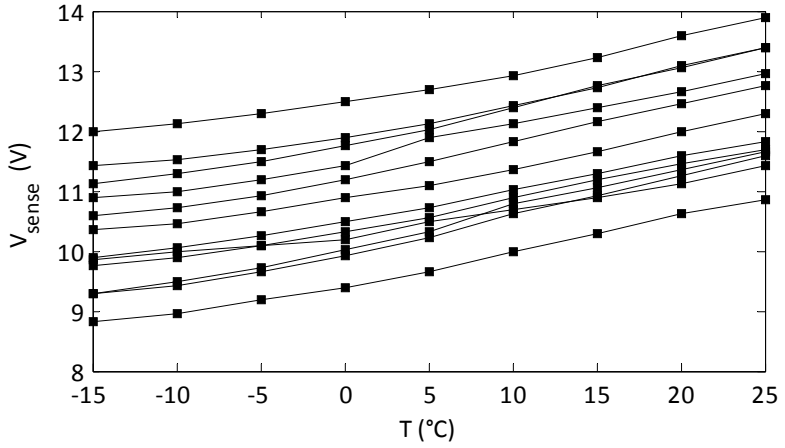


Figure 69. Measured output voltage versus temperature of twelve samples of the sensor[22]

7.4 System test

Figure 70 shows the block diagram of the testing system for the temperature monitor. For demonstration purposes, in this system the sensor interface and the driving of the digital display are made with silicon electronics on PCB (Silicon Test Platform in the figure).

The sensor converts the ambient temperature to a voltage (V_{sense}), which is sent to the silicon test circuitry. A sensor interface amplifies the sensed voltage (V_{amp}) and sends it to the input of the ADC on foil, which has been the main focus of this chapter. The control signals including reset and clock are provided by a Silicon microcontroller. The ADC converts the input to a digital value equivalent to the read temperature. This digital output is sent back to the microcontroller and shown on a segmented display.

Figure 71 shows photos of the measurement setup, including the boards for silicon test platform, sensor interface, and electrostatic discharge (ESD) protection. The

[22] Courtesy of S. Abbisso (STMicroelectronics)

connections to the sensor and ADC are implemented using flex cables. The picture below shows the measurement at an ambient temperature of 18.4 °C.

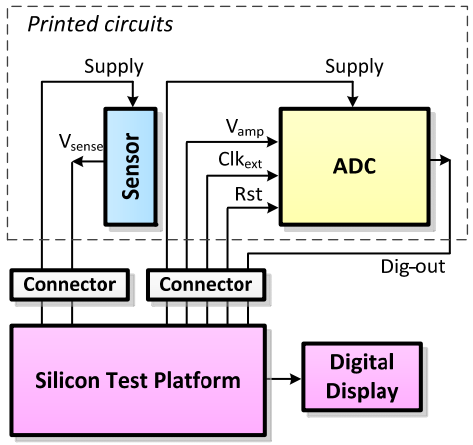


Figure 70. Block diagram of the temperature-monitor testing system

7.5 Highlights

The ADC shown in this chapter is the first one implemented using a printing technology, with a complexity far beyond the printed circuits reported before. 148 OTFTs and 13 resistors were printed in an area as large as 2180 mm^2. The ADC resolution can also be improved to the level of 7 bits, using a very simple architecture. To manufacture ADCs with such resolutions, the use of dynamic logic can prevent from going to non-feasible area consumptions (for example for the 7-bit counter).

The printed sensor in this work has a very simple architecture. The resistor-based sensor in the R2R technology reaches a linearity suitable for 4-bit resolution.

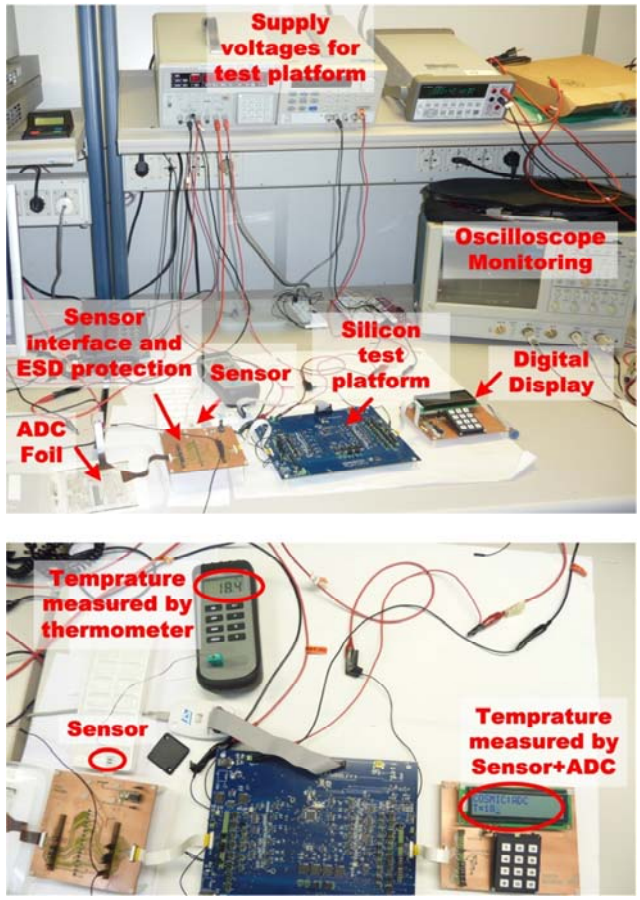


Figure 71. Photo of the temperature-monitor measurement setup

8 RFID Tag

In this chapter, the design of a printed RFID tag in S2S technology is presented. The design includes the front-end circuitry for power scavenging, envelope detection and clock and data recovery. In addition, the digital design to implement the RFID based on a "silent tag" communication protocol is shown.

8.1 Introduction

Silicon RFID tags pose limitations in terms of cost. Such shortcomings could be addressed by using printed organic electronics, thus enabling a widespread use of RFID tags, e.g. as a replacement for barcodes.

13.56-MHz capacitive and inductive coupled organic RFIDs have been already demonstrated using p-only organic technologies [37]-[38], and a complementary organic transponder was presented in [7]. However, high-frequency rectification and demodulation, typically needed in RFID tags, remain a challenge for printed OTFTs with their typically low mobility, large feature size and very high parasitics.

Another challenge for printed tags is to incorporate anti-collision and security mechanisms. Although a 128-b transponder incorporating Manchester encoding and a simple anti-collision protocol has been already shown in a p-only organic technology [39], the level of complexity that printed technologies can currently achieve is much lower. One way to prevent security issues with a reasonably low circuit complexity is to use the so-called silent tag protocol [127]. A silent tag is a type of reader-talks-first RFID tag which only replies when presented with its unique identity. An intelligent object tracking system can supply specific readers with the tag identities that can possibly fall in their range, and follow the objects as they move around. The advantage of the silent tag is that a search is possible only if the list of the tags that can be offered to the reader (e.g. the tags present in a shop) is known in advance. In this way tag security is ensured with no need for encryption, thus allowing for a far simpler implementation.

In this chapter, a printed passive reader-talks-first RFID tag based on the silent tag communication protocol is presented. The RFID tag is implemented in S2S technology. The simplified block diagram of such a system is shown in Figure 72. First a power scavenger generates power from the incoming AM-modulated RF signal. The scavenger supplies power to the receiver and the code recognition unit (CRU). The receiver extracts the envelope from the AM-modulated input signal and recovers the clock and data. Then the CRU decides whether the incoming data matches the identity of the tag, and only if it does, triggers a response back to the reader, which is sent

using load modulation. The circuits related to power scavenging and code recognition are explained here in Section 8.2, while clock and data recovery block (receiver) is presented elsewhere [99]. The system test schemes are depicted in Section 8.3 and some conclusions are drawn in Section 8.4.

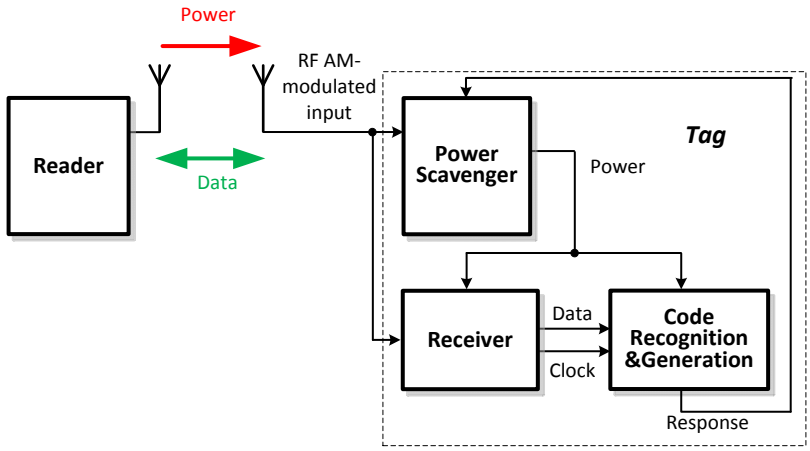


Figure 72. Simplified block diagram of a reader-talks-first RFID tag based on the silent tag communication protocol

8.2 RFID circuits

The different blocks of the tag circuitry are explained in this section in two parts: the front-end unit including the rectifier and receiver, and the code recognition unit.

8.2.1 Front-end

The architecture of the RFID tag front-end including the power scavenger and receiver is shown in Figure 73 [99]. The power scavenging is performed by a rectifier which generates the supply voltage (V_{dd}) for the tag circuitry. The receiver consists of an active envelope detector (ED) and clock/data recovery circuitry (CDR). Both ED and the rectifier are inductively coupled to the reader by means of a three-coil antenna on foil. In this way, the rectifier receives a single-ended full-scale RF input signal (which improves its efficiency), while the envelope detector receives a fully-differential RF signal. This is needed due to the fully-differential architecture adopted by the ED, which is more robust to common-mode disturbance in the RF transmission. The 3-coil antenna is manufactured on a separate foil by an R2R technology [125]-[126] and then

assembled to the RFID foil.

The input code adopts a pulse-width modulation (PWM) scheme shown in Figure 74, with bit “1” and “0” corresponding to a duty cycle of 70% and 30% high, respectively. This choice enables the presence of a constant time period among subsequent rising edges, which can be exploited to extract the clock directly from the AM envelope. In this way we can avoid timing schemes based on the division of the RF carrier, which are common in silicon solutions, but cannot be implemented by organic electronics at the state of the art.

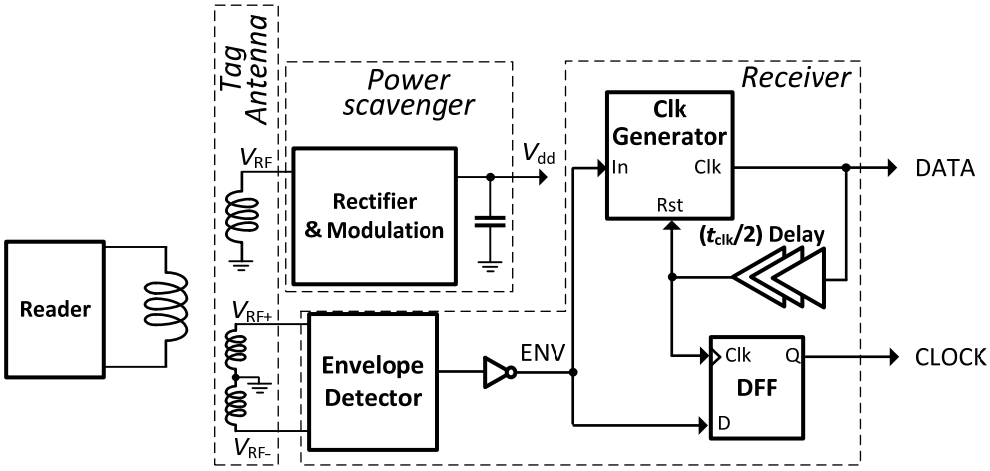
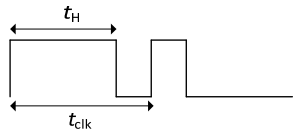


Figure 73. RFID tag front-end



Bit=1→ $t_H=0.7t_{clk}$
Bit=0→ $t_H=0.3t_{clk}$

Figure 74. Input code PWM scheme

In Chapter 5 it was shown that a rectifier based on OTFTs can generate enough power for a typical RFID tag in S2S technology. Figure 75 shows the circuit used in the final version of the rectifier. It is similar to the rectifier presented in Section 5.2.4 (Figure 56 [99]). In this rectifier, however, the threshold compensation scheme is more

conservative, since the gate of M1 and M4 is connected to V_2, instead of being connected to V_{out} and V_0, respectively. This is to prevent high leakage currents in M1 and M2 when they are in reverse bias and the output voltage is higher than their threshold voltage, around 20 V (This is explained in more details in Section 5.2.4).

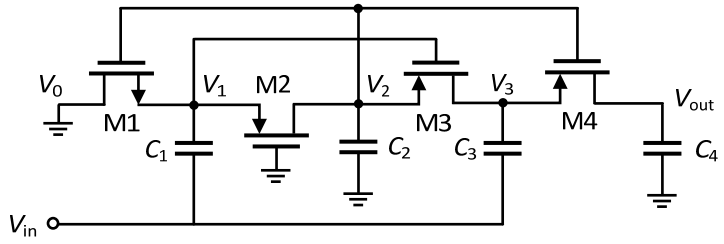


Figure 75. Rectifier used in the final version of RFID tag

The receiver, which mainly includes an envelope detector, a clock generator and a D-FF, works as follows [99]: ED extracts the 13.56MHz amplitude-shift keying (ASK) envelope and drives the recovery circuitry. The clock generator detects the ENV signal rising edge, thus providing a synchronizing clock (CLOCK) to the code recognition circuitry. CLOCK is properly delayed and then used by the D-FF to extract DATA by sampling the ENV signal at the right moment. The delay is implemented by a cascade of inverters charged with a capacitance. The clock generator and D-FF are implemented based on dynamic logic, similar to what was explained in Section 4.2.3.2.

The key block that determines the receiver's performance is the ED. Instead of a traditional diode-based EDs, the ED is made up of a p-type common-source differential pair with a self-biased n-type OTFT and an RC filter as load. The ED also includes a pseudo-differential comparator which provides a quasi rail-to-rail signal at its output ($\overline{ENV}$) that is suitable for the digital circuits. Such an architecture guarantees a large-swing for the ED output without extra amplification. Measurements show that the ED is able to demodulate the data from an RF input with a modulation depth as low as 25 %, thanks to the active detection scheme. The maximum input data bit rate is 75 b/s, and the RF input is 80 V_{pp}. More details on the schematics and measurements of the ED, which have been performed at the University of Catania, Italy, are given in [99].

It should be noted that for correct functionality of the receiver, the ripple at the supply voltage resulting from the modulated input needs to be filtered out. Considering the AM frequency range of the input data (specified to 50-100 Hz) and the load offered by the tag (around 1 MΩ), a large capacitance (tens to hundreds of nanofarad) is needed at the output of the rectifier. This capacitance and other passive components needed by the Delay block and the ED RC filter in the receiver are placed as external components on the antenna foil (manufactured by an R2R technology) where enough area is available.

To send a response back from an RFID tag to the reader, the impedance connected to the tag antenna is changed using load modulation techniques, in a way that it is easily detectable at the reader side. A transistor is continuously turned on and off by a code generator, and thus, the current flowing through it is modulated. In this way, the power dissipated in the antenna load is changed, changing the impedance seen by the antenna at the same frequency as the code generator. The load modulation transistor can be placed behind the rectifier (between V_{dd} and ground, called DC modulation) or in front of the rectifier (between V_{RF} and ground, called AC modulation).

In organic RFIDs, normally DC load modulation is used, in order to keep the minimum number of OTFTs working at high frequency [128]. In our case, however, this is not possible due to the large capacitance needed at the output of the rectifier; any signal with frequencies around and higher than 50 Hz (which is typically the case for a code generator circuit in our technology) would be filtered out, and thus not sent back to the reader. That is why we included AC load modulation on the tag for communication with the reader. Thus, a transistor is placed in parallel with the rectifier at the output of the antenna, driven by a ring oscillator which is in turn activated by the code-recognition unit. This is enough to send a “yes” signal to the reader according to the silent tag protocol, and thus a code generator is not needed.

8.2.2 Code-recognition unit

The code-recognition unit (CRU), shown in Figure 76(a), is designed to receive a sequence of “reset” and “identity” codes and, thus, consists of two modules: the reset module (RM) and the identity verification module (IVM). The RM synchronizes all the

tags in the reader range with the start of the following identity transmission code. The IVM compares the received code with the tag identity and in case of code matching enables the response back to the reader by using a load modulator. The CRU blocks are designed using TG-based architectures explained in Section 4.2.2. Details on the schematic of CRU blocks are shown in Figure 76(b).

In the RM, a 2-bit counter adds up the number of zeros in the input code (any "one" in the input resets the counter). After receiving four consecutive zeros (r_1r_2=11 and r=0), RM sends a reset signal (RESET-OK) to the IVM. This will announce the arrival of a new identity code to the IVM by clearing all its FFs and latches. If there is a discrepancy between clock and data (the data is delayed compared to the clock), signal "r" may go temporarily high, before the counter is reset by the arrival of next "1" in the data flow. Since RESET-OK is used to activate/lock some SR-latches asynchronously, it is important to prevent such temporary wrong activations. The D-latch in RM Logic block eliminates the possibility of sending such a false reset[23].

The identity comparison is performed in the Comparator Logic block through an XOR gate. At each clock, the 2-bit counter and a logic array at its output generate the correct tag identity code corresponding to the bit being received (the logic array is included in the IVM Logic block). In case of a un-match the comparator output ($\overline{\mathrm{Match}}$) goes high and resets the counter. In this case $\overline{\mathrm{Match}}$ remains high till the next Reset-OK is received, resetting $\overline{\mathrm{Match}}$ to zero. Otherwise, the operation will continue till all bits of the identification code are received and successfully compared. When this happens, the counter "Carry" bit generated in IVM Logic will go high and set IDENTITY-OK active, thus triggering the reply back. The output signal "TRIGGER", which activates a ring oscillator, remains high until the next Reset-OK is received.

[23] This Dlatch was not included in the first version of design reported in [99] where SR latches were not used.

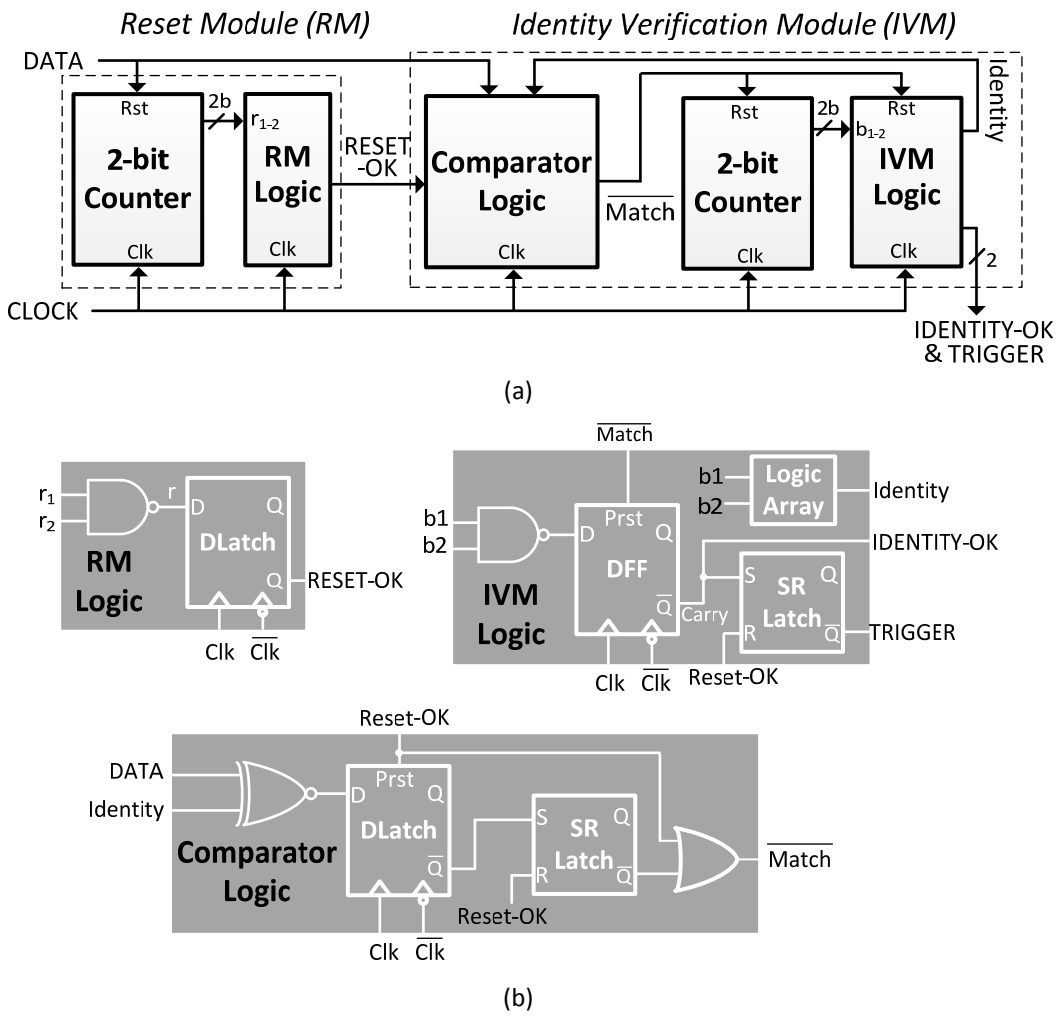


Figure 76. (a) Block diagram of the code recognition unit (CRU) including reset module (RM) and identity verification module (IVM), (b) more detailed schematic of the CRU blocks

The measured operation of the CRU is shown in Figure 77 for a tag with an identity of “0011”, where the measured IDENTITY-OK signal is not activated when the input code “0001” is received, and goes high only after “0000-0011” is received.

The photo of the first version of the RFID implemented as blocks on two foils is shown in Figure 78. The blocks were later put together in one design for final tests.

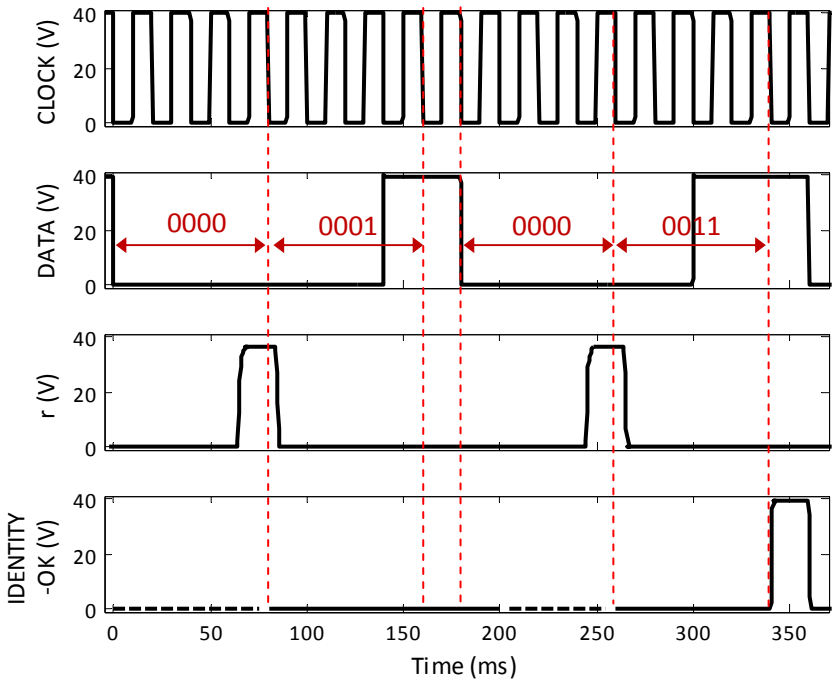


Figure 77. Measurements of the code recognition unit for a tag with identity of 0011 [99]

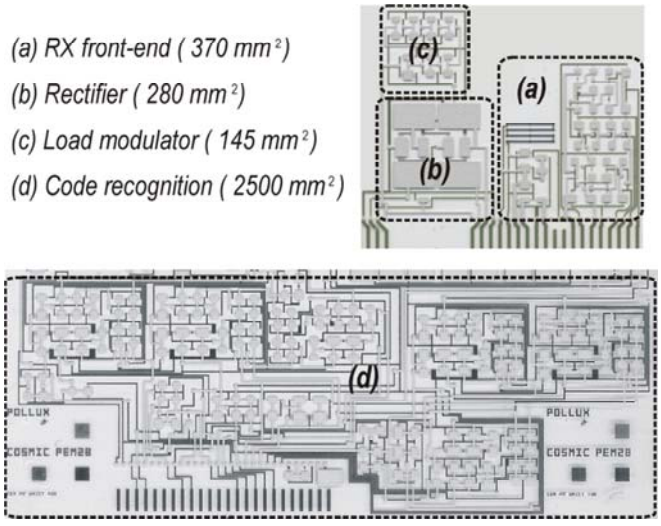


Figure 78. Photo of the first implementation of RFID blocks (in PEM2b-Top1 and -Top2)

8.3 Test system schemes

Figure 79 shows the block diagram of the system designed for testing the RFID tag. As it is shown in the figure, the complementary organic circuits discussed in Section 8.2 are manufactured by the S2S technology. The antenna is implemented using an R2R technology which has the capability of developing thick metal layers for realising the antenna. This technology also has the capability of manufacturing passive components at a very low cost, and has also been used to realise organic circuits. However, currently the yield is not enough for the level of complexity needed by the RFID tag.

On the S2S foil, the code recognition unit and front-end unit (receiver and power scavenger) can be tested through two separate connectors, namely Connector 1 and 2, to which many internal signals of the circuits are connected for thorough circuit characterization/debugging. The third connector is used for direct assembly to the foil developed by an R2R technology. In addition to the 3-coil antenna, the R2R foil contains the external passive components needed for the receiver and rectifier. The connection between the tag blocks is also provided through this foil. In this way, it is possible to characterize the blocks separately before they are connected for the final test.

The full RFID system has been designed and fabricated, and is presently under test.

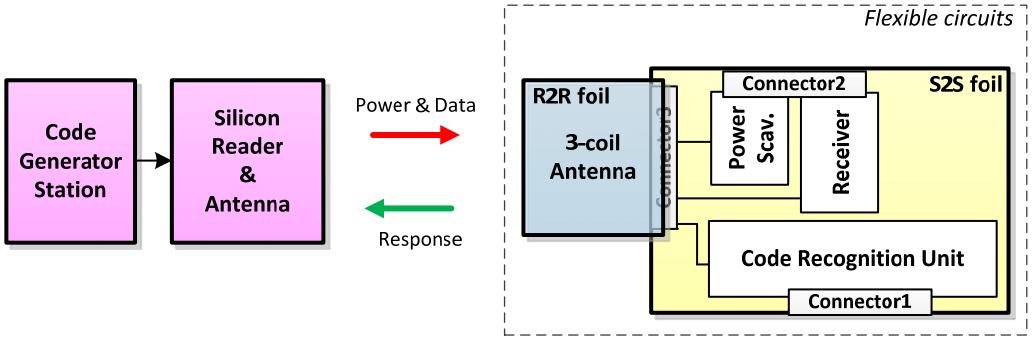


Figure 79. Block diagram of the RFID testing system

8.4 Highlights

As mentioned before, the tests on the RFID tag are still on-going. At the current state, the most important conclusion is that a complex logic is implemented, further improving the reached complexity of printed digital circuits to 210 OTFTs. Using this architecture, the number of RFID bits can be easily increased without excessively increasing the number of transistors and the area. Indeed, by using a 4-bit counter instead of the current 2-bit one in IVM, the number of bits could be increased to 16. Such an improvement seems to be feasible for S2S technology, especially if the area consumption is reduced by using dynamic logic. Other blocks of the RFID have also been already shown [99], suggesting that implementing a printed RFID tag based on the reliable silent tag protocol is fully feasible.

9 Conclusions

This dissertation focuses on the design of circuits and systems implemented on foil exploiting complementary organic technologies. The circuits investigated are the core of specific applications targeted by organic electronics. Organic technologies provide a promising platform for the implementation of large-area and low-cost applications on flexible substrates, but suffer from poor yield and performance. Many aspects of the performance of OTFT-based circuits could be improved by the use of complementary technologies which, however, are at a very early development stage. Our design explores a variety of circuits in two novel complementary technologies, namely W2W and S2S, starting from single transistor level and reaching a relatively high level of complexity.

This study provides a platform to factually compare different state-of-the-art complementary technologies. The use of different manufacturing methods in the W2W and S2S technologies makes them very different in terms of technology characteristics and thus, circuit design and performance. Moreover, these approaches are different from an application perspective. Printing technologies such as the S2S are most suitable for novel organic electronic applications that exploit the potential of organic technologies for low cost and large area implementations. The W2W technology, on the other hand, is based on conventional lithographic-based methods and better suits display-based applications.

The highest level of complexity (in terms of OTFT count) achieved by a printing technology (210 OTFTs in the code recognition unit of the RFID tag in Chapter 8) is around five times lower than that accomplished by the complementary W2W technology. The large footprint of devices and gates in the S2S technology makes it impractical (at the state of the art) for applications requiring more than a few hundreds of OTFTs. In addition, due to the remarkably smaller size of W2W OTFTs and circuits, and to their reduced parasitics, the performance of the W2W circuits in terms of speed is better compared to the S2S ones. This happens despite the fact that the mobility of the S2S OTFTs is higher, and S2S p- and n-type mobilities are better balanced (in the specific technologies used in this work). Circuits in the W2W technology work at a much lower supply voltage, thanks to the possibility to use thinner dielectrics, and thus to achieve lower threshold voltages in the W2W platform.

The W2W technology, however, needs an extra encapsulation layer to prevent the OTFTs from deterioration in air, while the S2S OTFTs are stable in air (due to the OTFT top-gate structure explained in Chapter 2). The availability of linear resistors in S2S technology increases the available options for the design of linear circuits.

One of the most important conclusions which can be drawn based on this work regards the level of circuit complexity achievable using state-of-the-art complementary organic technologies compared to unipolar approaches: the complexity of complementary circuits in terms of number of OTFTs is not very far from that of unipolar organic ones. The highest number of OTFTs in a circuit achieved by a lithography-based complementary technology is 1216 (display driver of Chapter 6). The very same platform, but incorporating p-only OTFTs, was used to implement an RFID transponder with only 300 OTFTs. A similar (but not the same) platform was used in [48] to implement a 3381-OTFT microprocessor using a dual gate technology. Of course, higher levels of complexity have been achieved in different unipolar technologies, but due to the differences e.g. in the MIM-stack preparation and defectivity, the comparison would not be fair.

Regarding printing-based technologies, we demonstrate that complementary printing technologies have reached a level of maturity high enough for implementing complete systems-on-foil such as the ADC in Chapter 7. This is a remarkable advancement compared to the previously-reported printed circuits e.g. the simple transponder chip based on a 15-stage ring oscillator (less than forty OTFTs in [6]). It is also interesting to observe the large surface area that the S2S technology has been able to successfully process using simple and fast printing techniques (21.8 cm^2 for the ADC). This shows the potential of the current technology for large-area and low-cost applications.

For the advancement of OTFT-based complementary circuits in terms of complexity and performance, a technology-aware circuit design is vital. Such a design is based on a good understanding of the technology characteristics and limitations, and also a regular feedback to the technologists to help locate the technology's weak points, based on the measurement results both at device and circuit level. That is how in this research the level of circuit complexity in terms of number of OTFTs as well as

the functionality has been improved step-by-step during several designs, from single OTFTs to complete systems-on-foil in both technologies.

For digital design, two important characteristics to be taken into account are the good noise margin (as a principal figure of merit) and the relatively poor hard yield of complementary technologies (at least at the state of the art). Another characteristic to be considered is the process limitations in controlling the dimensions and spacing of different OTFT layers, embodied by the design rules. Last but not least, a big impact on circuit functionality comes from OTFT parameter variation. This last aspect plays a significant role in choosing the best logic style. Considering all these factors, in W2W technology fully-static logic is favoured over other kinds of architectures. In the S2S technology, on the other hand, the designed logic is mostly TG-based. The demonstration of functional printed dynamic logic (Chapter 4) in the S2S technology promises a considerable area-consumption reduction, which could be better exploited if more reliable dynamic models would be available. However, it is recommended to avoid the use of dynamic logic to implement gates with large fan-ins. This is due to the large on-resistance of the OTFTs (especially because of the large threshold) which also hinders the implementation of large fan-in single gates using fully-static architectures.

In analogue and mixed-signal design, especially for printing technologies, the first principle is to keep the circuits as simple as possible. This is important, mainly because of the large OTFT parametric variations. For the same reason, it is better to rely on OTFT matching as little as possible and exploit (linear) passive components such as resistors (as in the DAC presented in Chapter 5). The use of simple offset-cancelling techniques based on switches, which is enabled in complementary approaches by the availability of transmission gates, can also drastically improve the circuit accuracy/resolution (e.g. in comparators in Chapter 5). The HF performance which is paramount in some applications is still mainly limited by mobility, minimum length and contact resistance in TFTs used as rectifiers. However, in the recent version of the technology which has a higher mobility, the use of threshold-voltage cancelling techniques can improve rectifier performance.

In comparison with the p-only organic circuits, the W2W circuits implemented in this work demonstrate how drastically the circuit power-delay product and the supply

voltage are improved when a complementary technology with a low threshold voltage is employed. In addition, despite all the variations, complementary inverters in both S2S and W2W technologies show a close to ideal noise margin. This is impossible to achieve in p-only inverters based on two OTFTs, unless dual-gate OTFTs are employed, but then at the cost of extra complexity and the need for extra biasing and suitable control.

Due to scarcity of complex unipolar printed circuits, we cannot directly compare the performance of the S2S technology with their equivalent unipolar version. However, unipolar technology limits the design options which could be used to improve the performance. The choice of architecture we made in this work for the S2S circuits is very illustrative in that: the use of the simple and effective TG-based architectures, employed in this work for both digital and analogue design, is not possible in p-only technologies. This is only one example. Indeed, almost all the complex p-only analogue circuits make use of dual-gate OTFTs which, to-date, have not been manufactured using a printing technology.

As a concluding remark, in this work we demonstrate that complementary organic technologies are already capable of manufacturing systems-on-foil suitable for novel applications such as flexible displays, sensor-augmented ADCs, and RFID tags. At the technology level, future work on reducing the hard faults and increasing the lifetime, together with shrinking the design rules and thinning the dielectric, could make a further remarkable improvement in circuits. At a higher level, a more accurate device modelling focusing on the parametric variability and dynamic characteristics will also be greatly beneficial to circuit design.

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2. S. Abdinia, F. Torricelli, G. Maiellaro, R. Coppard, A. Daami, S. Jacob, L. Mariucci, G. Palmisano, E. Ragonese, F. Tramontana, A.H.M. van Roermund, and E. Cantatore, "Variation-based design of an AM demodulator in a printed complementary organic technology," *Organic Electronics*, vol. 15, no. 4, pp. 904-912, 2014.
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Summary

Circuit Design in Complementary Organic Technologies

Organic thin film transistors (OTFTs) can be implemented on flexible substrates using low-cost fabrication processes. These characteristics allow OTFT-based circuits to be ubiquitously and unobtrusively embedded on surfaces and goods to improve safety, security, and convenience in everyday life. Application examples include flexible displays, smart sensor embedded in food package and large-area sensing surfaces. However, the design and implementation of OTFT circuits is hindered by the OTFTs' poor performance, large feature size, and high variability, which unfavourably affect speed, gain, power consumption and yield of organic circuits as well as their level of integration and complexity. This situation is exacerbated by the early development stage of complementary OTFT technologies which, if available, could improve the circuit robustness and performance compared to the commonly used p-only OTFT processes. Most of the state of the art organic circuits are based on p-type only technologies, and few circuits are implemented using very low-cost printing-based techniques.

This dissertation investigates circuit and system design exploiting complementary organic technologies. It is divided into two main parts. Part I, including Chapters 2 to 5, focuses on the technology characteristics, OTFT modelling, and building blocks design. Part II, presents the design of so-called systems-on-foil, based on the knowledge from Part I. Three such systems are discussed in Chapters 6 to 8.

Our focus is to improve circuit performance and robustness using two novel complementary organic technologies, developed in the EU FP7 project COSMIC. Pursuant to this goal, we first study the characteristics of these technologies, thoroughly explained in Chapter 2. One of these processes is lithographic and wafer-based: it will be designated as "wafer-to-wafer" (W2W) technology. The other process is printed and based on free-standing foils: it will be called "sheet-to-sheet" (S2S) technology. Each technology is most suitable for certain applications. For example, the W2W technology is well compatible with flat panel display technologies and, thus, suitable for flexible display applications. The S2S technology, on the other hand, is

potentially very cheap and high throughput. These characteristics make it especially suitable for applications which require low cost, such as RFID tags.

In order to design circuits using the OTFTs manufactured with the above-mentioned technologies, we study and model the characteristics of the OTFTs in Chapter 3. The models use known approaches to describe the drain current (DC model) and parasitic capacitances. A brief study of OTFT parametric variations is also performed to provide an estimation of circuit functionality. Based on this knowledge, we carry out a technology-aware design procedure at different abstraction levels including layout, circuit and architecture. We start from device level characterizations, and proceed with digital and analogue building blocks design and characterization. The digital and analogue building blocks are presented in Chapters 4 and 5, respectively. These blocks are used to implement different systems-on-foil, presented in Chapter 6 for W2W technology and in Chapters 7 to 8 for the S2S one.

In the W2W technology, the digital design and logic-style selection is performed based on the specific characteristics of the technology (e.g. the good level of OTFT integration), OTFT statistical characterization (which shows the possibility to have normally-on OTFTs), and several building block measurements. In this technology, a fully-static logic implementation, which is more robust than transmission-gate (TG) logic to the threshold voltage variability, is chosen. The drawbacks of static design in terms of higher transistor count, larger area and potential hard-yield loss are minimized in the W2W process thanks to the small TFT footprint and low defect density. This logic style is thus used to implement a display driver. This circuit works at the lowest supply voltage ever achieved by an organic circuit of this kind and achieves the highest number of OTFTs in a complementary organic circuit to-date. The display driver, which is manufactured in a technology compatible with the current flat panel display (FPD) processes, allows for the integration of the driving circuitry with a flexible display. This approach would improve mechanical flexibility, lower costs and reduce complexity.

A similar approach is exploited in S2S technology to design digital circuits based on printed OTFTs. Printing processes typically suffer from higher parametric variations compared to lithography-based technologies. However, for the first time, we

demonstrate dynamic gates and flip-flops in the S2S technology, showing that it is possible to decrease considerably area consumption in printed digital circuits by using dynamic logic. For more complex digital circuits in S2S technology, Transmission Gate-based logic with lower area compared to fully-static implementations and higher robustness compared to dynamic ones is chosen as best compromise for the current state of technology development. Several analogue circuits are also realised and characterised in S2S technology, including a “mismatch-free” comparator achieving an unprecedented accuracy level (50 mV offset), and the first printed DAC ever reported (better than 7 bit linearity). Furthermore, the HF performance of rectifiers in S2S technology is characterized. These building blocks are used to implement the first ADC printed on a foil, which is used together with a sensor-on-foil in a temperature monitor system. Finally, a printed RFID tag including silent tag logic and energy scavenging is designed and manufactured.

In conclusion, exploiting novel complementary organic processes, we designed and characterized digital circuits which achieve high noise-margin and low-voltage operation. In addition, we demonstrated performant and reliable analogue circuits, and mixed-signal systems-on-foil combining logic, energy scavengers, and analogue circuits for sensing and actuating applications. This study led to a significant advancement in the level of complexity of complementary organic circuits towards implementation of systems-on-foil. In addition, our work provides a platform to factually compare different state-of-the-art organic complementary technologies and explore what they can offer in comparison with unipolar technologies.

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Biography

Sahel Abdinia was born on 18 September 1983 in Rasht, Iran. After finishing the High School of mathematics and physics in 2001, she studied Electrical Engineering at the Gilan University in her hometown. She received her Bachelor's degree in 2006, after which she started her Master studies focusing on integrated circuit design. In 2009, she graduated from KN Toosi University in Tehran, Iran, and started to teach electronics in higher education institutes in Iran. From 2010, she started a PhD project at Eindhoven University of Technology, Eindhoven, The Netherlands. The results of this project are presented in this dissertation.