Polarization converter post-processing for integrated polarization independent SOA

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***Abstract*— Post-processing of a polarization converter (PC) in an experimental industrial generic foundry process is demonstrated. Insertion of the PC halfway an SOA reduced its polarization dependence from 14 dB to 3 dB.**

Keywords: post-processing, polarization converter, InP, photonic integration.

I. INTRODUCTION

In the European FP7 project EuroPIC, generic photonic foundry processes are being developed based on the integration technologies of Oclaro and the Fraunhofer HHI. In a generic approach the most frequently used photonic building blocks (BBs) can be integrated using a standardized process [1]. However, a polarization converter (PC) is not yet included in the current foundry processes. In this paper we report the post-processing of a passive PC in a PIC fabricated in the experimental foundry process of Oclaro. The existing structures in the chip allow us to test the PC in a polarization independent SOA (PI-SOA) configuration; the connection between the post-processed PC device and pre-processed test structures is obtained using tapered waveguides. First, we will briefly explain the PC working principle and its role in a PI-SOA circuit. Next, we will describe the simulations performed to optimize the tapered waveguides connections. Then we will go through the post-processing steps. The last section shows the measurement results.

II. POLARIZATION-INDEPENDENT SOAS

A single section passive PC is an optical waveguide with a sloped cladding (Fig. 1) connected to straight input-output waveguides. The geometry should be such that the PC can support the two modes M_1 and M_2, +45° and -45° rotated with respect to the TE vector. The two modes recombine into the TM mode in the straight output waveguide, after equal excitation of the two modes by an input TE mode, and propagation along a half beat length $L_{PC} = \pi/(\beta_1 - \beta_2)$ [2]. Here β_n is the propagation constant of the mode M_n. The PC shape has been optimized for the Oclaro layer-stack. Details about the performance and tolerance analysis will be presented in a future paper [3]. A PI-SOA consists of a passive PC placed between two identical SOAs. Fig. 2 shows the circuit working principle with a PC that gives a full conversion from TE to TM and vice versa ($C = P_{out}^{converted}/P_{out}^{total} = 1$). Such a PC works as a half-wave plate. The output power in the case of a TE and TM polarized mode is shown as well, with $G(TE)$ and $G(TM)$ the gain of the SOA in the TE and TM case. Thus, by using a full conversion PC, this circuit gives a signal amplification independent of the input polarization (i.e., assuming that the SOAs are not in saturation. In the case of $C \neq 1$, the output power is $P_{out} = CP_{in}G(TE)G(TM) + (1-C)G(TE)^2$ for a TE input mode and $P_{out} = CP_{in}G(TE)G(TM) + (1-C)G(TM)^2$ for a TM input mode. Thus, the output power depends on the input polarization. We use this circuit as test structure for our PC.

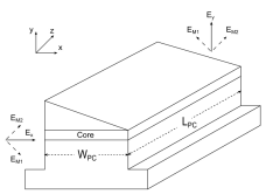

Fig. 1: single section passive PC with sloped cladding.

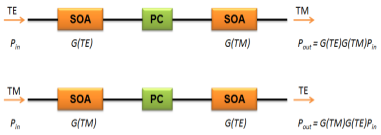

Fig. 2: PI- SOA working principle.

III. TAPER CONNECTIONS

In a PI-SOA test structures (Fig. 3) the SOAs are defined in a direction perpendicular to the major flat, whilst the PC is defined in a direction parallel to the major flat, to etch a sloped top cladding. Tapers allow the connection between the PC (post-processed at COBRA) and the rest of the circuit (pre-processed by Oclaro). A 5 µm distance between the tapers is kept to provide some tolerance for the PC post-processing with tapered input-output waveguides. A tradeoff between device performances and dimensions leads to the choice of the taper length L_T and width W_T. The performance is evaluated in terms of coupling coefficient $k = P_{out}/P_{in}$. A pair of tapers, both 5 µm wide and 100 µm long, give a $k = 0.95$. Since in the PI-SOA test structure the PC is connected by two pairs of coupled tapers, $k = 0.90$; thus, the device has 0.5 dB extra losses due to the taper connections. A 500 µm space is left in between the Oclaro tapers for post-processing of the PC together with input-output tapered waveguides.

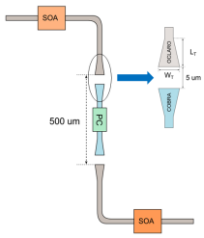

Fig.3: PI-SOA test structure and OCLARO-COBRA taper connection.

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IV. POST-PROCESSING

The PC post-processing consists of two sequential processes: the protection of the pre-processed circuit and the PC post-processing. The pre-processed chip is protected with 400 nm of silicon nitride and with photo-resist. The photo-resist AZ 4533 is spun for 30 sec at 2500 RPM and soft baked for 20 min at 95°C; the spinning time and speed define the thickness of the photo-resist. A photolithography mask is used to open the areas for the PC processing. After the exposure, the photo-resist is developed using AZ-developer diluted 1:1 ratio in H_2O for 2 min and 30 sec. The last step is the photo-resist hard baking. The temperature is ramped from room temperature to avoid strain in the photo-resist, which causes cracks. At 200°C the photo-resist is baked for 20 min. The chip is then ready for the PC processing. First, O_2-hhplasma is applied to promote the adhesion between the EBL resist (ZEP) layer and the silicon nitride layer, which is already underneath the photo-resist; afterwards, the ZEP is spun on the chip. The ZEP layer remains quite uniform from the middle of the opened areas (around 350 nm thick) to 5 µm away from the Oclaro tapers (400 nm); so the structures can be exposed everywhere with the same EBL dose. The PC is processed in two EBL exposures: 1) definition of a rectangular area used to etch the slope in the cladding with HCl; 2) definition of the PC waveguide together with input and output tapered waveguides. The straight sidewalls are etched in the ICP. However, in our first experiments, the post-processed structures show a guiding layer undercut. One of the reasons is that during the wet etching (HCl etching or cleaning steps) the presence of light influences the etch rate. This is known as the photo-electrochemical effect (PEC) and it can be enhanced by the presence of the back metal contact. A cleaning with phosphoric acid has been performed with and without light to verify this hypothesis. The sample cleaned in the dark shows a smaller undercut. Fig. 4 shows the protected Oclaro taper and the COBRA taper with the guiding layer undercut on the real chip, and the post-processed PC on a dummy sample.

V. MEASUREMENTS

In the measurement setup the output fiber of a tunable laser, working at $\lambda = 1550\,\text{nm}$, is connected to a polarization controller. The polarization controller is used sub-sequentially to minimize and maximize the PI-SOA output power to obtain P_{out}^{min} and P_{out}^{max}. We calculate $P_{diff} = P_{out}^{max} - P_{out}^{min}$ for two test structures: one with the PC (SOAs_PC) and one without PC (SOAs_noPC). In SOAs_noPC the PC is replaced with a deep etched passive waveguide 1.5 µm wide. The measurement results (TABLE I) show that P_{diff} is significantly smaller if the PC is present.

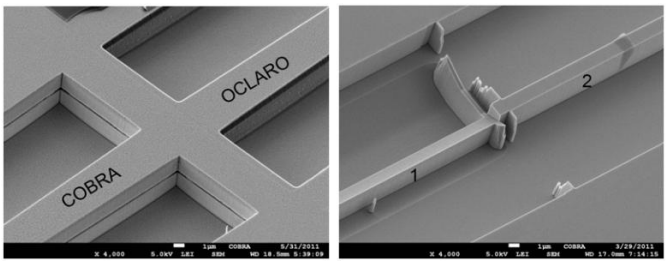

Fig. 4: Oclaro taper and COBRA taper with guiding layer undercut (left); PC (1) with input waveguide (2) on a dummy sample (right).

TABLE I. MEASUREMENTS RESULTS FOR THE POLARIZATION INDEPENDENT SOA

	SOAs length	Drive current I	P_{in}	P_{out}^{max}	P_{out}^{min}	P_{diff}
SOAs_PC	500 µm	35 mA	5 dBm	-16 dBm	-19 dBm	3 dB
SOAs_noPC	300 µm	25 mA	0 dBm	-2 dBm	-16 dBm	14 dB

The losses are high due to the guiding layer undercut. We also measured the losses in an Oclaro passive test structure without taper connections (Bends _Oclaro) and then we compared the result with two passive test structures with taper connections. The first one is made by Oclaro (Bends_tapers_Oclaro); in the second one the central tapered waveguide has been post-processed at COBRA (Bends_tapers_COBRA). The comparison between Bends _Oclaro and Bends_tapers_Oclaro shows that the taper connections introduce 0.5 dB losses (TABLE II) which matches the simulations. Bends_tapers_COBRA has another 0.5 dB extra losses most likely introduced by the guiding layer undercut.

TABLE II. MEASUREMENTS RESULTS FOR TAPER CONNECTION LOSSES

	P_{in}	P_{out}
Bends_Oclaro	0 dBm	-5.3 dBm
Bends_tapers_Oclaro	0 dBm	-5.8 dBm
Bends_tapers_COBRA	0 dBm	-6.3 dBm

VI. CONCLUSIONS

A PC has been post-processed on an Oclaro chip containing test structures for PI-SOAs. The connection between the devices processed by Oclaro and COBRA is realized through tapers which give 0.5 dB extra losses. During the post-processing the Oclaro structures are completely protected. However, a guiding layer undercut of the post-processed structures occurred due to the photo-electrochemical effect. Further tests will verify if the undercut starts to take place during the ICP etching. Measurement results show that the polarization dependence of two SOA's in series reduced from 14 dB to 3 dB with the PC in-between, indicating the presence of a significant polarization conversion.

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