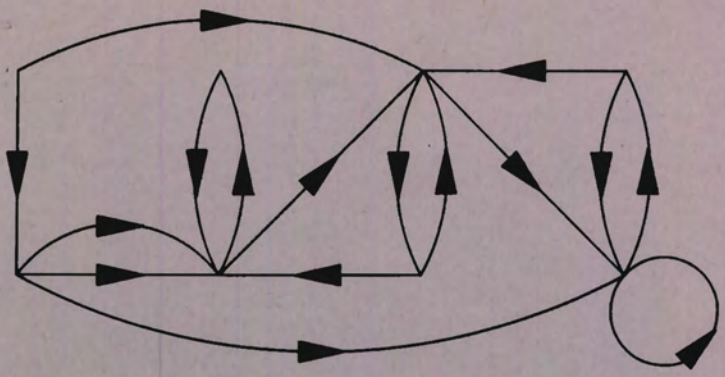
Contributions to switched capacitor filter synthesis



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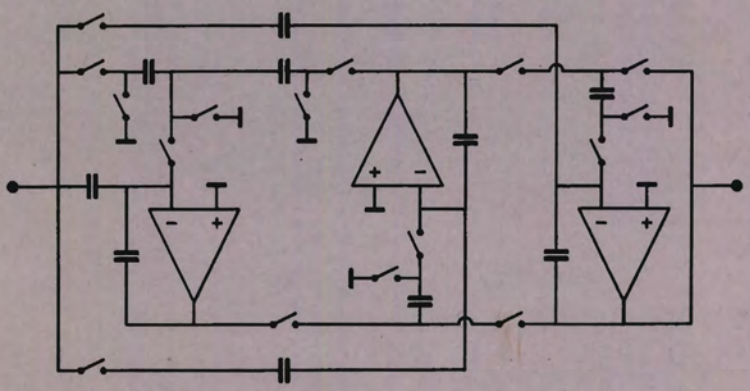

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PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de Rector Magnificus, prof. dr. F.N. Hooge, voor een commissie aangewezen door het College van Dekanen in het openbaar te verdedigen op dinsdag 28 juni 1988 te 14.00 uur

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Aan Marti,
Stan en Ledje

CONTENTS

1. INTRODUCTION AND SUMMARY.

After A.Fettweis published his theory of resonant-transfer circuits [1] in 1968[1], the appearance of the famous Fried paper [2] in 1972 and a next few years of relative silence, the development of switched capacitor (SC) filters from a basic concept into a manifold applied commercial product is one of unusual speed.
A number of reasons can be given for their popularity.
SC filters

- are low cost,
- need a small chip area,
- are low power,
- are accurate, don't need tuning after production,
- on the other hand, the filter transfer can be transformed to another frequency range by simply changing the clock frequency; this can be attractive for adaptive filter applications,
- are fully implementable in standard MOS processes,
- can be combined with digital circuits on one chip.

As a starting point for many SC filter synthesis methods, other important categories of filters, such as LC, active RC and digital are used.
The main reason for this is a historical one. In the early days of the application of switched capacitors, designers and network theorists had already gathered a huge amount of knowledge and experience, especially in the field of continuous-time filters. It were these designers and theorists who were the first to approach this new offspring and put their stamp on it.
One of the reasons for the unusual speed of the development of switched capacitor filter theory was the available knowledge and experience they brought along.
Though much of the existing theories could be transformed in a more or

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[1] *In fact J.C. Maxwell mentioned the principle of switched capacitors already in 1873 in his book "A treatise on electricity and magnetism".*

less straight forward way to make them suitable for SC filters, the similarity between SC filters and other filter categories is only on the surface.
One of the most typical SC aspects and also the most pressing problem is the existence of stray-capacitances on the final integrated chip. These parasitics are not even an order of magnitude smaller than the desired capacitors. The effects of this dominant error source have to be minimized in advance, by a strays-insensitive design.

The synthesis methods that will be proposed in this thesis do not rely on a continuous-time or digital prototype filter as a starting point, but on the properties of switched capacitors themselves and the requirement of strays-insensitivity with the implications of this demand.

In order to reduce the complexity of this approach and not get lost in too many degrees of freedom, these synthesis methods are restricted to circuits with a biphase clock. This restriction is not in conflict with industrial interest: a great majority of the industrial produced SC filters belong to this above-mentioned class.
As a follow-up of this work the possibilities of an extension of this approach to circuits with a multiphase clock could be investigated.

Before we will focus on these synthesis methods, first some basic principles that are implicitly used in this thesis will be cleared up in chapter 2.
In chapter 3, some analysis methods for SC filters are considered. This is done fore two reasons. In the first place these methods will give the reader a way to verify the transfer of the circuits that will be presented in the next chapters. In the second place one of these methods will be an important tool for the synthesis methods that are proposed in this thesis. The first considered method is straight-forward and powerful, but on the other hand also very cumbersome. After being confronted with an example of this method in appendix A, the reader will appreciate the fact that often in practical situations many non-idealities of the circuit may be neglected. In these cases, the second presented method, which is

derived from the first one, may be used. This method is already less cumbersome, but the third and final approach, which is based on Signal Flow Graphs (SFG's), is the most convenient. Moreover, the restrictions for its application will turn out to correspond nicely with the constraints for SC circuits to be strays-insensitive. As an extension of this method a representation for finite gain effects of the amplifiers will be proposed.

In chapter 4 the basic concepts for strays-insensitive synthesis are considered. As a starting point the known Hasler constraints will be used, but in an extended form. In parallel the SFG based analysis will be simplified further. The obtained analysis method is extremely simple and very well suited for a reversed application as a synthesis tool. At this stage, the problem of strays-insensitive synthesis of biphase clocked circuits has been reduced to the composition of an appropriate SFG from branches of a very small set. Three synthesis methods, based on this approach will be proposed in this thesis. The first two of them are briefly considered in chapter 4.

In chapter 5 the third, and most important synthesis method of this thesis, based on the application of 'Strays-insensitive Design Graphs' (SDG's) is explained. Examples are given, one of which is actually built as a bread-board circuit and used as a verification. Furthermore attention is payed to sensitivity properties and possible solutions are given for synthesis with finite gain amplifiers.

As a validation, the SDG method is compared with several other existing methodologies in chapter 6.

Chapter 7 can be seen as a separate part of this thesis, describing an 'Equivalent Immittance Converter' (EIC). This building block for SC circuits is comparable with a Generalized Immittance Converter in active-RC synthesis and may result in filters with very few circuit elements. A fourth order Butterworth filter using this concept was realized as an NMOS integrated circuit, measurement results of which are also given in this chapter. Although the EIC building block is insensitive to the most important bottom-plate strays of the desired capacitors, it is sensitive to other strays. However, as will be shown, these other strays can be compensated for. An interesting property of this EIC is the fact that its finite amplifier-gain effects can be represented by loading equivalent admittances.

Finally, in chapter 8, some conclusions will be made and suggestions are given for a follow-up.

2. SOME BASIC PRINCIPLES FOR THE ANALYSIS AND SYNTHESIS OF SWITCHED CAPACITOR FILTERS.

In this chapter we will briefly discuss some basic principles that are used in this thesis. For a more extensive description the reader is referred to one of the many books [3-6] about these subjects.

SC filters belong to the class of time-variable analog sampled-data systems which are commonly described in the z-domain. Therefore in section 2.1 we will discuss the z-transformation and furthermore a number of transformations from the continuous-time to the discrete-time domain and vice versa.

In section 2.2 the realization of capacitors in MOS technology is considered.

2.1 TRANSFORMATION METHODS.

A sample-sequence x(n), obtained by a periodic sampling of a signal x(t) at moments $t = nT$, such that

$$x(n) = x(nT) = x(t)\Big|_{t=nT} \tag{2.1}$$

can be represented by its z-transform, defined as:

$$X(z) = Z\{x(n)\} = \sum_{n=-\infty}^{\infty} x(n)z^{-n} \tag{2.2}$$

for all z where X(z) converges.

In fact this z-transform plays a comparable role in the description of discrete-time signals as the Laplace s-transform does for continuous-time signals.

Here z can be considered as a shift-operator: a multiplication of X(z) with z corresponds with a shift of the sequence x(n) over one sample, or equivalently a time-shift of the signal x(t) over an interval T. Noting that this time-shift can be represented in the Laplace s-domain by a multiplication of the s-transform X(s) of the

signal $x(t)$ with e^{sT}, the validity of the following relation can be shown:

$$z = e^{sT} \tag{2.3}$$

This relation gives us the exact s⇔z transform. This can for example be used for the transformation of the transfer function of a continuous-time filter, expressed in s, into a corresponding transfer function for a discrete-time filter, expressed in z. However, the problem arises that a realizable s-domain transfer function, being a rational function in s, will be transformed into an unrealizable equivalent z-domain transfer function, being a rational function in $\frac{\ln(z)}{T}$ and *not* in z. The same problem arises when trying to transform a realizable z-domain transfer function into an s-domain equivalent transfer function, which results in a rational function in e^{sT} instead of in s. For that purpose other transformations than the exact relation (2.3) are used, five of which will be used in this thesis.

A. Matched-z transform.

Application of this transformation method means, that each transmission zero (pole) of a rational transfer function in s is transformed to a transmission zero (pole) of a corresponding transfer function in the z-domain or vice versa, using the exact relation (2.3). As it only concerns the transmission poles and zeros, this transformation does *not* result in an exact transformed transfer function. Nevertheless, for frequencies that are low with respect to the sample frequency $f_s = 1/T$, the transformed transfer function will be a good approximation for the exact transform, and has the advantage of being a realizable rational function. Because poles are transformed exactly with this method, poles in the left s-half-plane will be mapped on poles within the unit-circle in the z-plane and vice versa. This guarantees conservation of the stability of a filter after transformation.

B. Forward-Euler transform.

Using this method, the operator s in a continuous-time transfer-function is replaced by

$$s \rightarrow \frac{z-1}{T} \qquad (2.4a)$$

or inversely, z in a discrete-time transfer-function is replaced by

$$z \rightarrow 1+sT \qquad (2.4b)$$

Again a rational function in s is transformed into a rational function in z using this method. However, part of the left s-half-plane is mapped *outside* the unit-circle in the z-plane. This means that stable continuous-time filters, which have their poles in the left s-half-plane, may be transformed into instable discrete-time filters, having their poles outside the unit circle in the z-plane. However, apart from this potential instability, this transformation is a reasonable approximation for the exact transform for low frequencies with respect to the sample frequency f_s. Note that eq.(2.4b) can be considered to represent the first two terms of the Laurent polynomial expansion of the exact transform:

$$z = e^{sT} = 1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots \qquad (2.5)$$

C. Backward-Euler transform.

Here, the operator s of a continuous-time transfer function is replaced by

$$s \rightarrow \frac{1-z^{-1}}{T} \qquad (2.6a)$$

or conversely z is replaced by

$$z \rightarrow \frac{1}{1-sT} \qquad (2.6b)$$

In this case the left s-half plane is mapped within the unit-circle of the z-plane, so conservation of stability is guaranteed when this

method is used for the transformation of a continuous-time transfer function into a discrete-time transfer function. However, also the jω-axis of the s-plane and part of the right s-half-plane is mapped within this unit circle. This means that using this method much of the selectivity of continuous-time filters is lost. Also for this method the resulting transfer function will be a reasonable approximation for frequencies that are low enough with respect to the sample-frequency f_s.
When eq.(2.6b) is rewritten as

$$z^{-1} \rightarrow 1-sT$$

this can be considered as representing the first two terms of the Laurent polynomial expansion of

$$z^{-1} = e^{-sT} = 1 - sT + \frac{(sT)^2}{2!} - \frac{(sT)^3}{3!} + \ldots . \qquad (2.7)$$

D. Bilinear transform.

Using this transform, s is replaced by

$$s \rightarrow \frac{2}{T}\,\frac{z-1}{z+1} \qquad (2.8a)$$

or conversely, z is replaced by

$$z \rightarrow \frac{1+sT/2}{1-sT/2} \qquad (2.8b)$$

Now the left s-half-plane is mapped within the unit-circle in the z-plane and the jω-axis is mapped onto this unit circle. Stability is preserved and also filter selectivity. When a bilinear transformed transfer function is transformed back to the s-domain using the exact substitution (2.3), it can be shown to be identical to the original transfer, except for a frequency warping with respect to the original transfer function. By means of 'pre-warping' one can in advance correct for this effect. The bilinear transform is probably the most popular in filter design.
When the division of (2.8b) is carried out, this results in an expansion:

$$z \rightarrow 1 + sT + \frac{(sT)^2}{2} + \frac{(sT)^3}{4} + \ldots \qquad (2.9a)$$

the three first terms being equal to the expansion of the exact transform:

$$z = 1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots \qquad (2.9b)$$

For frequencies that are low with respect to the sample frequency, this transform results in a good approximation for the exactly transformed transfer function, even without prewarping.

E. Lossless Discrete Integration (LDI) transform.

In this case s is replaced by

$$s \rightarrow \frac{z^{1/2} - z^{-1/2}}{T} \qquad (2.10a)$$

or conversely z is replaced by

$$z \rightarrow 1 + \frac{(sT)^2}{2} + sT\sqrt{1 + \frac{(sT)^2}{2}} \qquad (2.10b)$$

Here, with $z^{1/2}$ we mean the principle value of the root of z.
Also for this case the left s-half plane is mapped within the unit-circle in the z-plane and the $j\omega$-axis onto this unit circle. Again when an LDI transformed transfer function is transformed back to the s-domain using the exact substitution (2.3), it can be shown to be identical to the original transfer, except for a frequency warping with respect to the original transfer function. This frequency warping can be corrected for in advance again by the application of pre-warping.
The first three terms of the polynomial expansion for eq.(2.10b)

$$z \rightarrow 1 + sT + \frac{(sT)^2}{2} + \frac{(sT)^3}{8} + \ldots \qquad (2.11)$$

are again equal to that of the expansion of the exact transform of eq.(2.9b).
For frequencies that are low with respect to the sample frequency, this transform also results in a good approximation for the exactly

transformed transfer function, even without pre-warping.
As the realization of an LDI transformed integrator results in very simple SC structures, which are used as building blocks in many filters, this LDI transform is often used in SC filter synthesis.

2.2 REALIZATION OF CAPACITORS IN MOS TECHNOLOGY.

The ability of MOS circuits to store signal carrying charge packets for relative long time intervals is one of the main principles that gives us the opportunity to realize SC filters. In fact this is the same principle that made the realization of dynamic logic circuits and dynamic random-access memories possible. In this latter application charges are stored on relative inaccurate parasitic capacitances. In digital techniques one can afford these inaccuracies because of the noise margins that are usually assigned to the quantizing operation. In straight-forward analog applications these inaccuracies would automatically lead to inaccurate circuits. Therefore in this latter case we need precision capacitors. It is a remarkable fact that capacitors, realized in normal MOS processes, although they are stable in terms of temperature and voltage coefficients, show random processing variations on the order of 10 to 20%. Nevertheless SC filters, that are realized with these imperfect MOS capacitors are well-known for their accuracy. This is possible, because the properties of SC filters depend on the *ratio* of capacitances. Because of the good 'tracking' of capacitances on one chip, this ratio is reproducible with an accuracy within some tenths of percents. In contrast to SC filters, the properties of integrated active-RC filters depend on *products* of resistances and capacitances, which are badly reproducible.

Several types of MOS monolithic capacitors are known. The type that was especially added to the standard N500 NMOS process of the 'Eindhovense Fabricage Faciliteit voor IC's' (EFFIC) was the 'double-poly' capacitor, as depicted in fig.2.1.

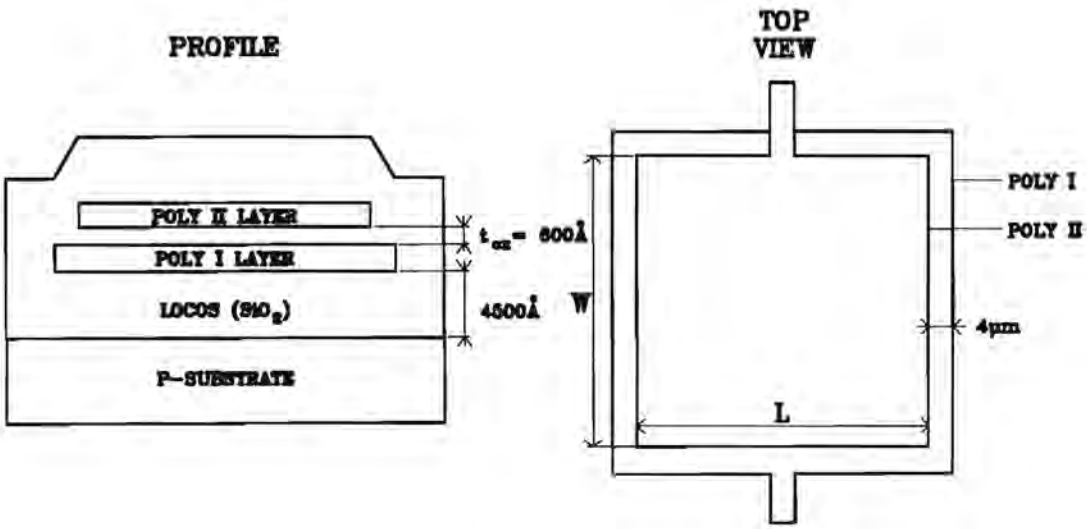

fig.2.1: Profile and top-view of a 'double-poly' MOS capacitor.

This capacitor is composed of a bottom-plate being the poly-I layer, a silicon dioxide dielectric layer, which is as thin as about 600Å (resulting in a capacitance of approx. $60\mu F/m^2$) and a poly-II layer as the capacitor top-plate.
Ideally the value of this MOS capacitor is given by

$$C = \frac{\epsilon_0 \epsilon_{ox} W L}{t_{ox}} \quad . \tag{2.12}$$

Therefore deviations in ϵ_{ox} , t_{ox} , W and L have a direct impact on the accuracy of the realized capacitance.
The area of the bottom-plate is larger than that of the top-plate, as shown in fig.2.1. This makes this configuration relative insensitive for mask-alignment tolerances. However, effects like undercutting still cause errors due to deviations of W and L. In order to minimize the effects due to these deviations, capacitances are composed of unit capacitors, which all have the same geometry and are expected to have about the same edge effects. Because SC filter characteristics depend on capacitance *ratios*, the resulting errors are greatly reduced.
Deviations of ϵ_{ox} are relatively small with respect to the other error sources.
The most important error source in practice are variations in the oxide thickness t_{ox} . In a standard MOS process these variations are

in the order of magnitude of 10%. Again due to the fact that SC filters are only dependant on capacitance *ratios*, the common errors due to these thickness deviations will cancel. The dependency of these deviations of the position on the chip are small: typical 1 to 10 ppm/μm. Long range gradients can be compensated for by common-centroid capacitor layouts, but this is not often done in practical SC filter realizations. Approximate temperature coefficients for these capacitors are 10 to 50 ppm/K, voltage coefficients are about 20 to 200 ppm/V.

As can be seen from fig.2.1 the oxide layer between the bottom-plate of the desired capacitor and substrate is only in the order of magnitude of 7.5 times as thick as the thin oxide between the the bottom and top-plates. This results in a parasitic capacitance between this bottom-plate and substrate of approx. 13% of the desired capacitance. With other parasitics connected to this bottom-plate taken into account the total parasitic may be as high as 15 to 20%. Because the thickness of the oxide layer between substrate and bottom-plate depends on a number of MOS process parameters, compensation methods for these bottom-plate parasitics are not very reliable.
The parasitics of the top-plate to ground (substrate) are an order of magnitude smaller than the bottom-plate strays. The most important top-plate parasitics are that of the interconnections which highly depend on the carefulness of the layout designer. However, due to the switches, amplifier in- and outputs etc., with their stray-capacitances the total parasitic from the circuit-node, to which this top-plate is connected, to ground will never be zero, and potentially influence the filter behavior.
For these reasons sensitivity to bottom-plate strays should by all means be avoided and sensitivity to other parasitics is undesirable.

3. ANALYSIS OF SWITCHED CAPACITOR FILTERS

Real-life switched capacitor filters suffer from all kinds of non-idealities such as

- *parasitic capacitances*
- *finite open-loop DC gain and bandwidth of the amplifiers*
- *finite on-conductance of the switches*
- *finite on-conductance of the amplifier outputs*
- *non-linearity of the (parasitic) capacitors, switches and amplifiers*
- *clock feedthrough*
- *thermal noise and flicker noise in the MOS-fets of the amplifiers and switches*
- *etc.*

that make the analysis of switched capacitor filters a tedious and complicated task.
For a more or less exact analysis of SCF's one is almost forced to make use of one of the numerous SC analysis computer programs [7-16] such as BSCAP, DIANA, DOSCA, DONES, PRSC, SCAPN, SCANAL, SCNAP, SCNET, SCYMBAL, SCOP, SWAP, SWICAP, SWINET, SWITCAP, WASCAP or WATSCAD, that can handle all or a number of the above-mentioned non-idealities. Fortunately however, in many applications most or all of these non-idealities have only a very small effect on the behavior of the filter. In these cases the analysis of a more or less idealized model of the real circuit may lead to results that approximate the actual behavior of the circuit close enough. In many cases the analysis 'by hand' of such a simplified circuit may be practicable feasible.

Many methods are known for such an analysis by hand [17-22], three of which are briefly examined here.
First we will consider a powerful but cumbersome analysis method based on charge conservation [19] (chapter 3.1).
From this first method a more restricted, but practical analysis procedure that applies 'z-domain equivalent circuits' [20] will be derived (chapter 3.2).

Finally a Signal Flow Graph (SFG) based analysis method [21] is examined (chapter 3.3). These SFG's will play an important role in this thesis, beacause they form a tool for the synthesis method, presented in chapter 4 and 5. As an extension of this analysis method, a representation for the finite gain of the operational amplifiers in the circuit will be proposed.

3.1 ANALYSIS BASED ON CHARGE CONSERVATION.

The first method that is considered here is based on charge conservation [19].
It is assumed that the leak of the capacitors, the input currents of the amplifiers and the conductances of the switches in the off-state are negligible. For not too low clock-frequencies and implementation in MOS-technology these assumptions seem reasonable. Furthermore the clock-phases are assumed to be non-overlapping.
For every clock-phase, contours are assigned, for which charge conservation is applicable.
Next the charge conservation is expressed in terms of voltages, using the charge to voltage relations of the capacitors and the (voltage to) voltage relations of the (voltage controlled) voltage sources.
Then the voltages at the sampling instants may be transformed to the z-domain and expressed in each other resulting in the input to output voltage relations of the circuit.

As an example of such an analysis the simple circuit of fig 3.1 is considered.

All elements in this circuit are considered ideal, except for the gain of the amplifier which has a single-pole roll-off:

$$V_3(s) = - \frac{A_o}{1 + \frac{sA_o}{\omega_u}} V_2(s) \qquad (3.1a)$$

or expressed in the time-domain:

$$\frac{1}{\omega_u}\frac{dv_3(t)}{dt} + \frac{1}{A_o}v_3(t) = -v_2(t) \qquad (3.1b)$$

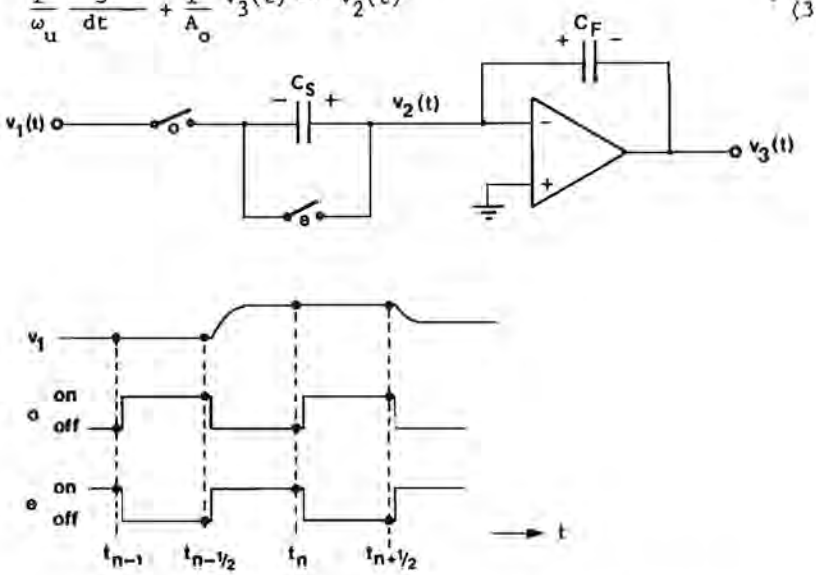

fig.3.1: Example circuit for an analysis method based on charge conservation.

Usually 'e' and 'o' are used to label switches, to indicate their control voltages as well as the time intervals (clock-phases) for which they are in the on-state.

The complete derivation of the transfer function of this circuit is given in appendix A. It should be mentioned that though the circuit taken into consideration is very simple and the only non-ideality taken into account is the frequency dependency of the amplifier gain, the analysis is rather tedious.

This example shows that though this method is powerful and nicely applicable, it is unpractical for analysis by hand of high order filters with a number of non-idealities.

3.2 ANALYSIS BASED ON THE APPLICATION OF Z-DOMAIN EQUIVALENT CIRCUITS.

A second method can be derived from the first one and is based on the

application of z-domain equivalent circuits [20].
The method can be explained as follows.

- First the circuit that has to be analyzed is split up into elementary SC building blocks.
- Then for these elementary building blocks z-domain equivalent circuits are derived which have the same port relations for the voltages and charge-increments in the z-domain for every clock-phase as the original circuit. These equivalent circuits are composed of z-domain equivalent admittances. These z-domain equivalent admittances represent the relations between the voltages and charge-increments in the z-domain in a similar way as 'normal' admittances describe the relations between voltages and currents in the Laplace s-domain.
- Next these z-domain equivalent building blocks are interconnected according to the topology of the original circuit.
- Finally this compound z-domain equivalent circuit, which reflects the relations between voltages and charge-increments of the original SC circuit is analyzed, using 'normal' KVL for the (z-transformed) voltages and KCL for the (z-transformed) charge-increments.

This method is less universal than the first one, because it is based on the assumption that momentary relations exist between the port voltages and charge increments at the sampling instants for every elementary SC building block separately. This assumption is not valid when non-idealities like finite on-conductances of the switches and amplifier output conductances or finite bandwidth of the amplifiers are taken into account.
Though this method is limited in its application it can handle some non-idealities like finite amplifier gain (without frequency dependency) and parasitic capacitances and has the advantage of being very well applicable for analysis by hand, even for higher order filters. Furthermore, for moderate switching frequencies the effects due to the finite amplifier bandwidth and output-conductance as well as the on-conductance of the switches are negligible.

In the original paper [20] an extensive library of SC 'elementary' building blocks using non-overlapping biphase switches and their z-domain equivalent circuits are given. It is however sufficient to know the z-domain equivalent circuits of the building blocks that are really elementary: switch, capacitor and voltage-controlled voltage source, to be able to analyze the same collection of SC circuits as with this extensive library.

Consider a capacitor C (fig.3.2), which is assumed to be an element in a SC circuit with a biphase non-overlapping clock. (Note that this analysis method is not by principle restricted to biphase-clock circuits only; extension to multiphase-clock circuits is easy and left to the reader).
The two clock-phases are again indicated by indices 'e' (for 'even') and 'o' (for odd), see fig.3.2.

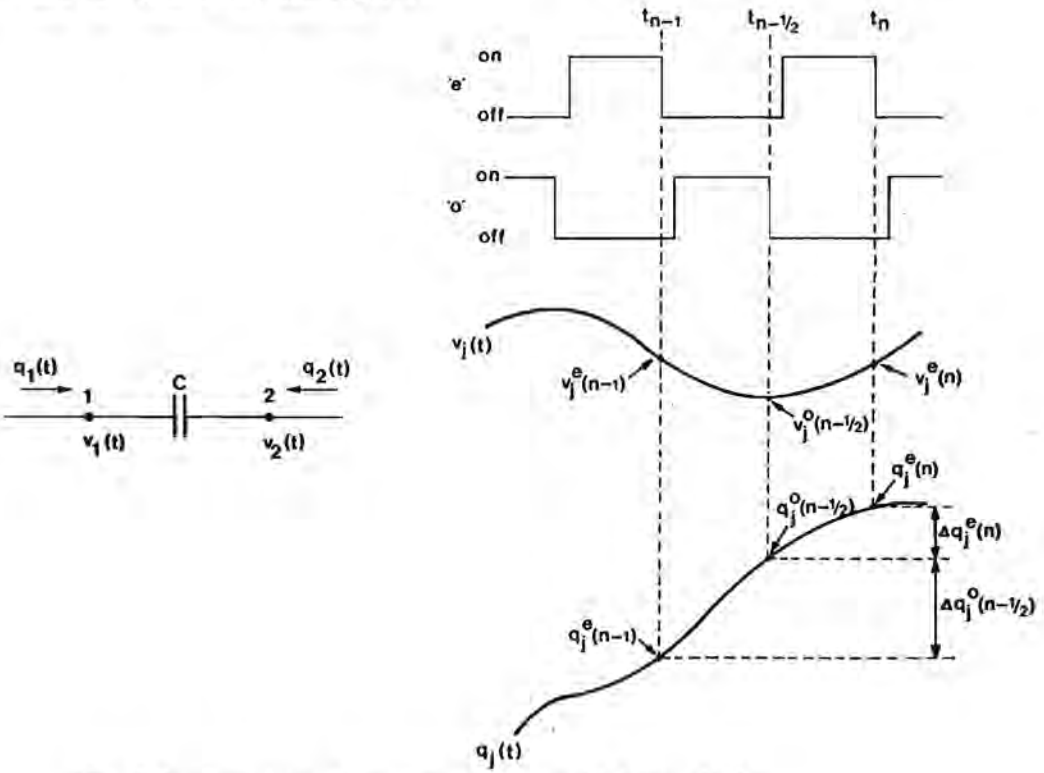

fig.3.2: Capacitor in a circuit with a biphase clock.

Using charge conservation, the following relations can be obtained:

$$\Delta q_1^e = q_1^e(n) - q_1^o(n-1/2) = C\,[v_1^e(n) - v_2^e(n) - v_1^o(n-1/2) + v_2^o(n-1/2)] \qquad (3.2a)$$

$$\Delta q_1^o(n-1/2) = q_1^o(n-1/2) - q_1^e(n-1) = C\,[v_1^o(n-1/2) - v_2^o(n-1/2) - v_1^e(n-1) + v_2^e(n-1)] \qquad (3.2b)$$

$$\Delta q_2^e(n) = -\Delta q_1^e(n) \qquad (3.2c)$$

$$\Delta q_2^o(n-1/2) = -\Delta q_1^o(n-1/2) \qquad (3.2d)$$

($\Delta q_1^e(n)$ being the charge flown into pole 1 during the interval $t_{n-1/2} < t \leq t_n$, etc.).

Or, after transformation to the z-domain:

$$\Delta Q_1^e = CV_1^e - CV_2^e - z^{-1/2}\,CV_1^o + z^{-1/2}\,CV_2^o \qquad (3.3a)$$

$$\Delta Q_1^o = CV_1^o - CV_2^o - z^{-1/2}\,CV_1^e + z^{-1/2}\,CV_2^e \qquad (3.3b)$$

$$\Delta Q_2^e = -\Delta Q_1^e \qquad (3.3c)$$

$$\Delta Q_2^o = -\Delta Q_1^o \qquad (3.3d)$$

These relations (3.3 a-d) between charge-increments ΔQ_i^j and voltages V_k^l can be represented by the z-domain equivalent circuit of fig.3.3.

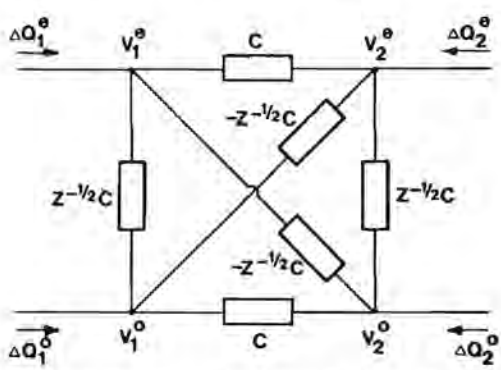

Fig.3.3: Z-domain equivalent circuit for the capacitor of fig.3.2.

The z-domain equivalent circuit for a switch which is in the on-state during clock-phase 'e' will be a short circuit in phase 'e' and an open circuit in phase 'o' (fig.3.4).
Of course clock-phase 'e' and 'o' may be mutually interchanged.

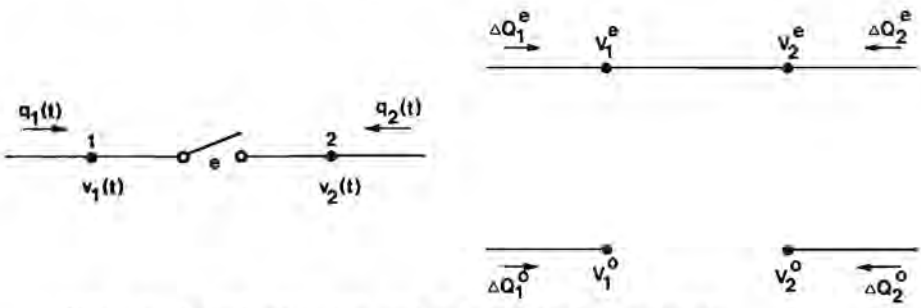

fig.3.4: Switch with its z-domain equivalent circuit.

The z-domain equivalent circuit for a voltage-controlled voltage source (or amplifier) with (frequency independent) gain A_o will consist of two VCVS'es, one for each clock-phase (fig.4.5).

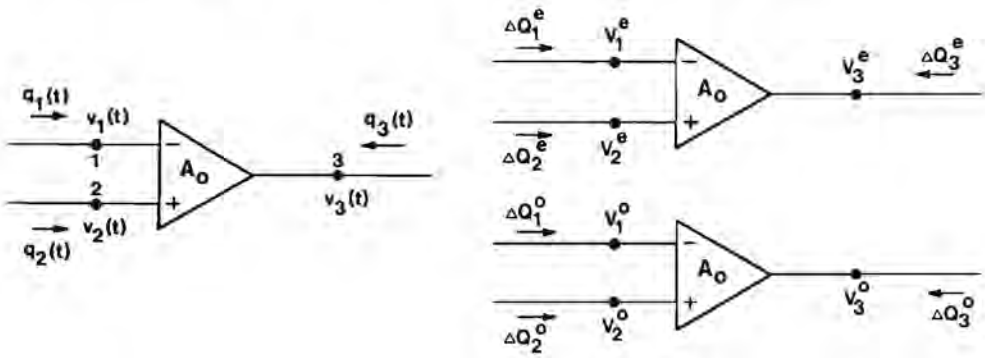

fig.3.5: Amplifier with its z-domain equivalent circuit

Now with the z-domain equivalent circuits for capacitors, switches and VCVS'es derived, the z-domain equivalents of more extensive circuits can be obtained.
As an example the circuit of fig.3.1 is analyzed using this method, where the gain A of the amplifier is taken A_o.

This equivalent circuit can further be simplified by removing the redundant admittances (drawn with a dashed line in fig.3.6).
Straight-forward analysis of this circuit yields

$$H^{oo}(z) = \frac{V_3^o(z)}{V_1^o(z)} = \frac{-C_s}{(1-z^{-1})\ (1+1/A_o)C_F + C_s/A_o} \qquad (3.4a)$$

$$H^{oe}(z) = \frac{V_3^e(z)}{V_1^o(z)} = \frac{-z^{-1/2}\ C_s}{(1-z^{-1})\ (1+1/A_o)C_F + C_s/A_o} \qquad (3.4b)$$

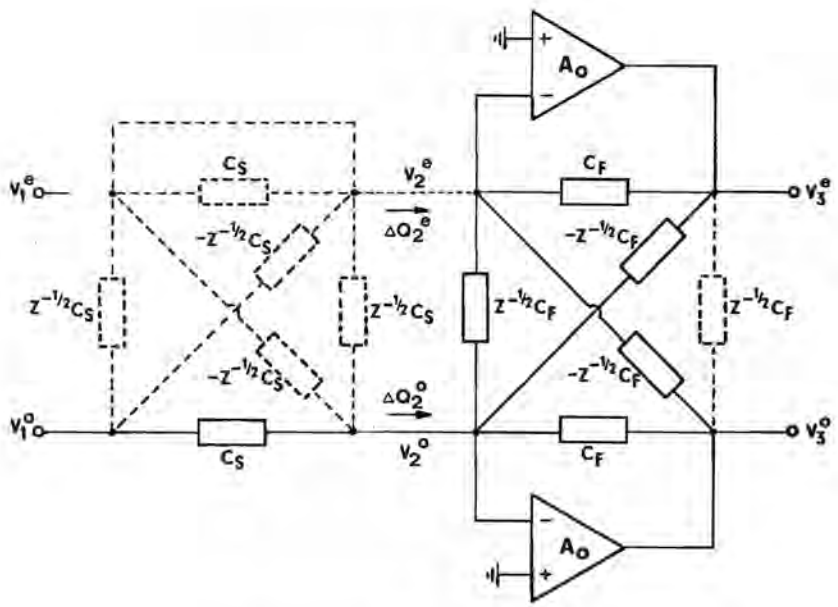

fig.3.6: Z-domain equivalent circuit for fig.3.1 with $A=A_0$.

representing a damped inverting Backward Euler integrator and a damped inverting LDI integrator respectively, in accordance with the results of the analysis in appendix A (with $\omega_u \to \infty$).

When all elements would be considered ideal, so for the circuit of fig.3.1 $A \to \infty$, the z-domain circuit of fig.3.6 could be simplified further. In that case admittance $z^{-1/2}C_F$ would be connected between two virtual ground nodes and thus be redundant (fig.3.7).

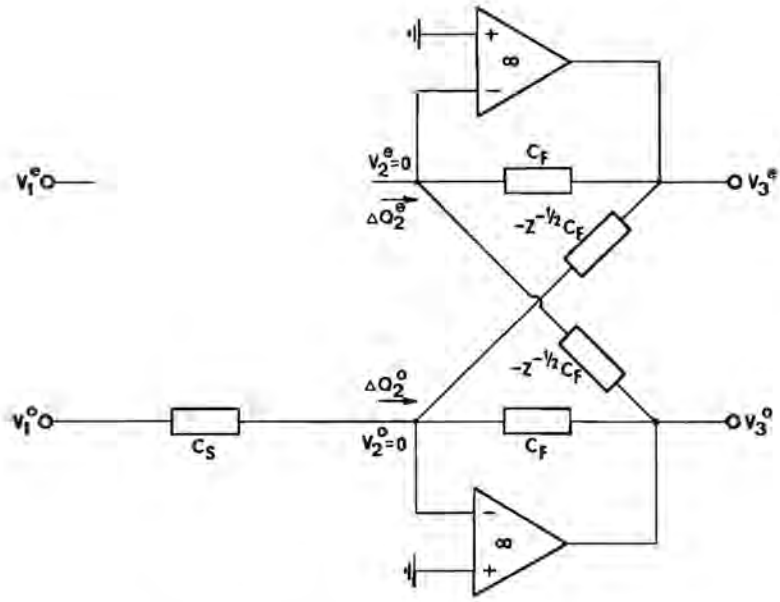

fig.3.7: Z-domain equivalent circuit for fig.3.1 with $A \to \infty$.

Now the analysis is even more simple and yields

$$H^{oo}(z) = \frac{V_3^o(z)}{V_1^o(z)} = \frac{-C_S}{(1-z^{-1})C_F} \tag{3.5a}$$

$$H^{oe}(z) = \frac{V_3^e(z)}{V_1^o(z)} = \frac{-z^{-1/2}C_S}{(1-z^{-1})C_F} \tag{3.5b}$$

So in the ideal case these BE and LDI integrators are undamped.

Note that in this ideal case, where $V_2^e = V_2^o = 0$ (virtual ground) the charge-increment ΔQ_2^o is completely specified by the voltage V_1^o and the capacitance C_S:

$$\Delta Q_2^o = C_S\, V_1^o \tag{3.6}$$

Furthermore the voltages V_3^e and V_3^o can be expressed in the

charge-increments ΔQ_2^o and ΔQ_2^e and the capacitance C_F as:

$$V_3^e = -\frac{1}{(1-z^{-1})C_F}\,\Delta Q_2^e - \frac{z^{-1/2}}{(1-z^{-1})C_F}\,\Delta Q_2^o \qquad (3.7a)$$

and

$$V_3^o = -\frac{1}{(1-z^{-1})C_F}\,\Delta Q_2^o - \frac{z^{-1/2}}{(1-z^{-1})C_F}\,\Delta Q_2^e \qquad (3.7b)$$

3.3 ANALYSIS BASED ON THE APPLICATION OF SIGNAL FLOW GRAPHS.

Relations (3.6), (3.7a) and (3.7b) can also be represented by a Signal Flow Graph [21], as depicted in fig.3.8.

Analysis of SC circuits based on SFG representation is the third and most convenient method considered here. It is also the most restricted method in its practical application. In order to be easily handled it

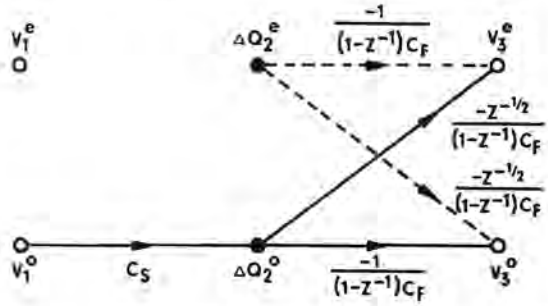

fig.3.8: Signal Flow Graph representation for the idealized circuit of fig.3.1.

is assumed that the circuit consists of (a number of) basic configurations as depicted in fig.3.9.

This basic configuration consists of an ideal operational amplifier

(with infinite gain[1] and bandwidth) and a grounded non-inverting input, combined with a feedback SC network N2, such that $V_2 = 0$ (virtual ground) and an input SC network N1 between an ideal voltage source V_1 (for example the output of an ideal operational amplifier) and this virtual ground node.

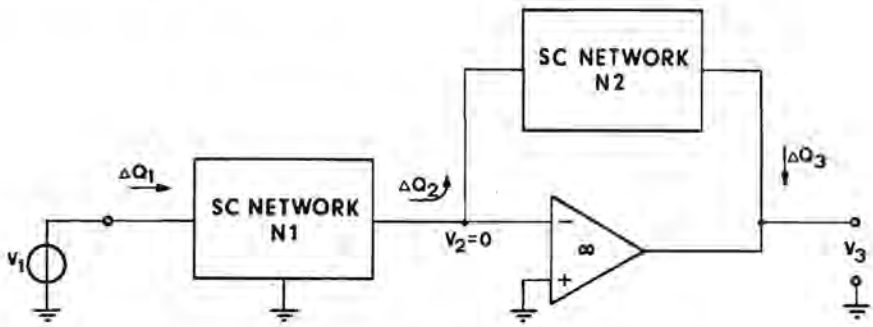

fig.3.9: Basic configuration for circuits in order to be conveniently analyzable by means of the considered Signal Flow Graph analysis method.

Of the 4n port variables of network N1 with an n-phase clock (V_1^Φ, ΔQ_1^Φ, V_2^Φ and ΔQ_2^Φ per clock-phase Φ), interrelated by a $2n \times 2n$ transmission matrix, 2n are redundant. ΔQ_1^Φ describes only the load of the ideal voltage source V_1, furthermore $V_2^\Phi = 0$ (virtual ground).
This reduces the size of the transmission matrix to $n \times n$.
For the same reasons also the size of the transmission matrix of network N2 can be reduced to $n \times n$: $V_2^\Phi = 0$ and ΔQ_3^Φ describes only the load of an ideal voltage source V_3.

The considered SFG analysis method is in fact based on a graph representation of the coupled transmission matrices of the 'input networks' (N1-type networks) with a signal flow from voltage nodes marked V_i^Φ to charge-increment nodes marked ΔQ_j^Φ and of 'opamp networks'

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[1] *At the end of this chapter an extension for this SFG analysis method will be presented that can also cope with finite gain amplifiers.*

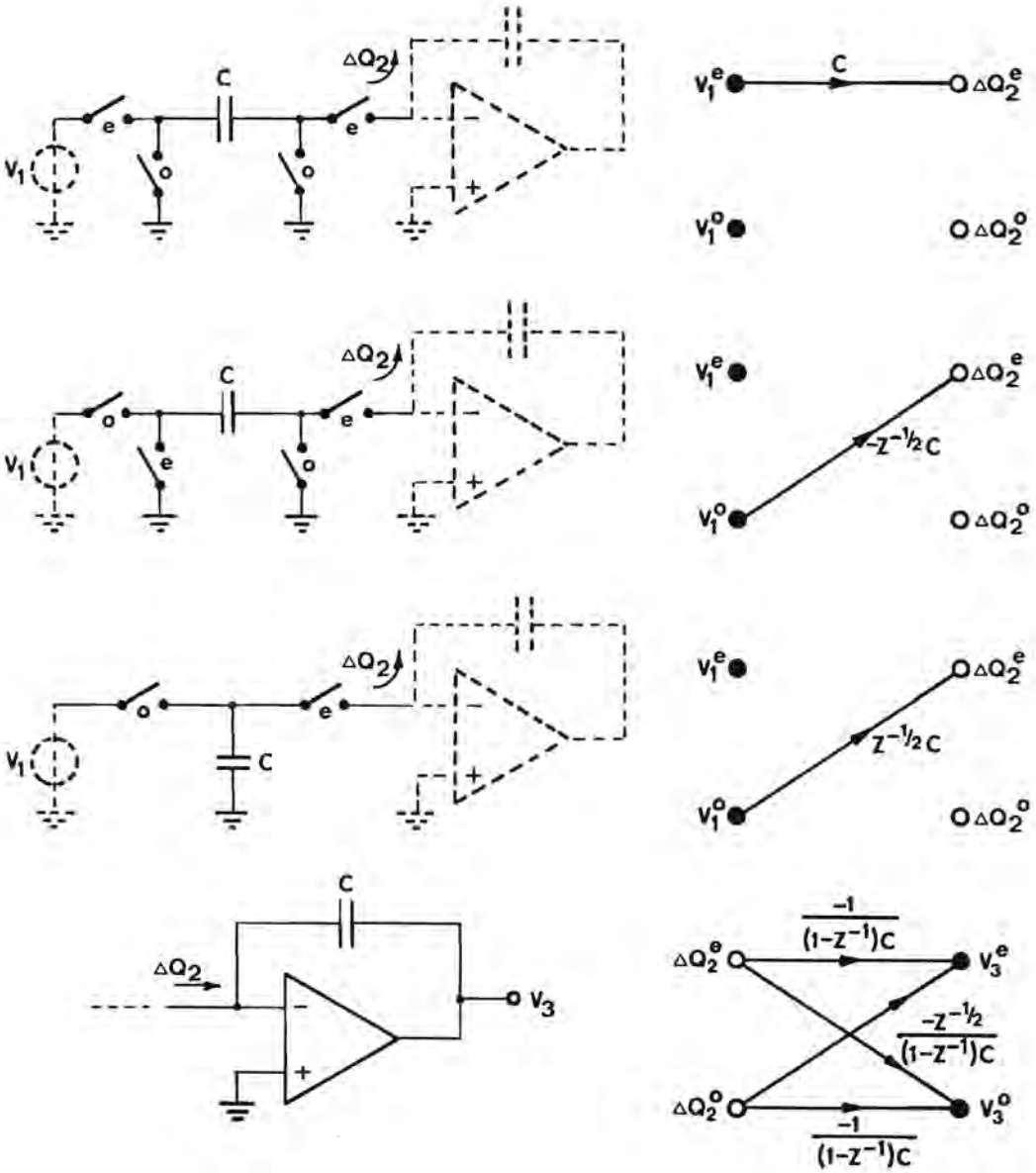


fig.3.10: Input networks and opamp network and their SFG representations.

(combining the operational amplifiers with their N2-type network) with a signal flow from charge-increment nodes marked ΔQ_k^{Φ} to voltage nodes marked V_l^{Φ}. (Here Φ refers to clockphase 'e' or 'o', indices i, j, k and l are related to nodes in the considered SC circuit.)
The composed SFG of the total circuit can then be analysed using for instance Mason's gain rule [26] or elimination of nodes, using elementary graph transformations [25].

In [21] a small library of biphase clock input and opamp networks is given with their corresponding SFG representation, part of which is redrawn in fig.3.10.

As an example using this method, the more complex circuit of fig.3.11 [23] will be analyzed.
This circuit consists of three different types of input networks and one type of opamp network, for which the corresponding SFG representation, given in fig.3.10, can easily be derived by the reader, or found in [21].

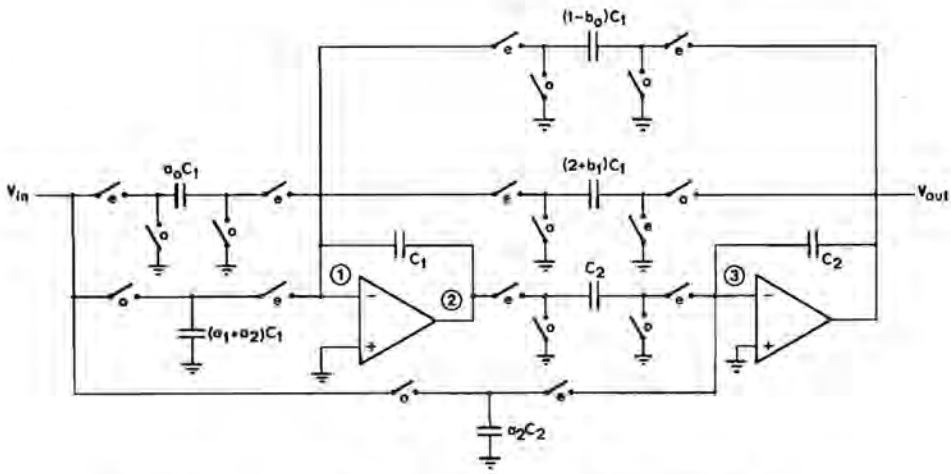


fig.3.11: Example circuit for the demonstration of SFG analysis.

The SFG representations of the input networks and opamp networks are now interconnected, according to the topology of the SC network of

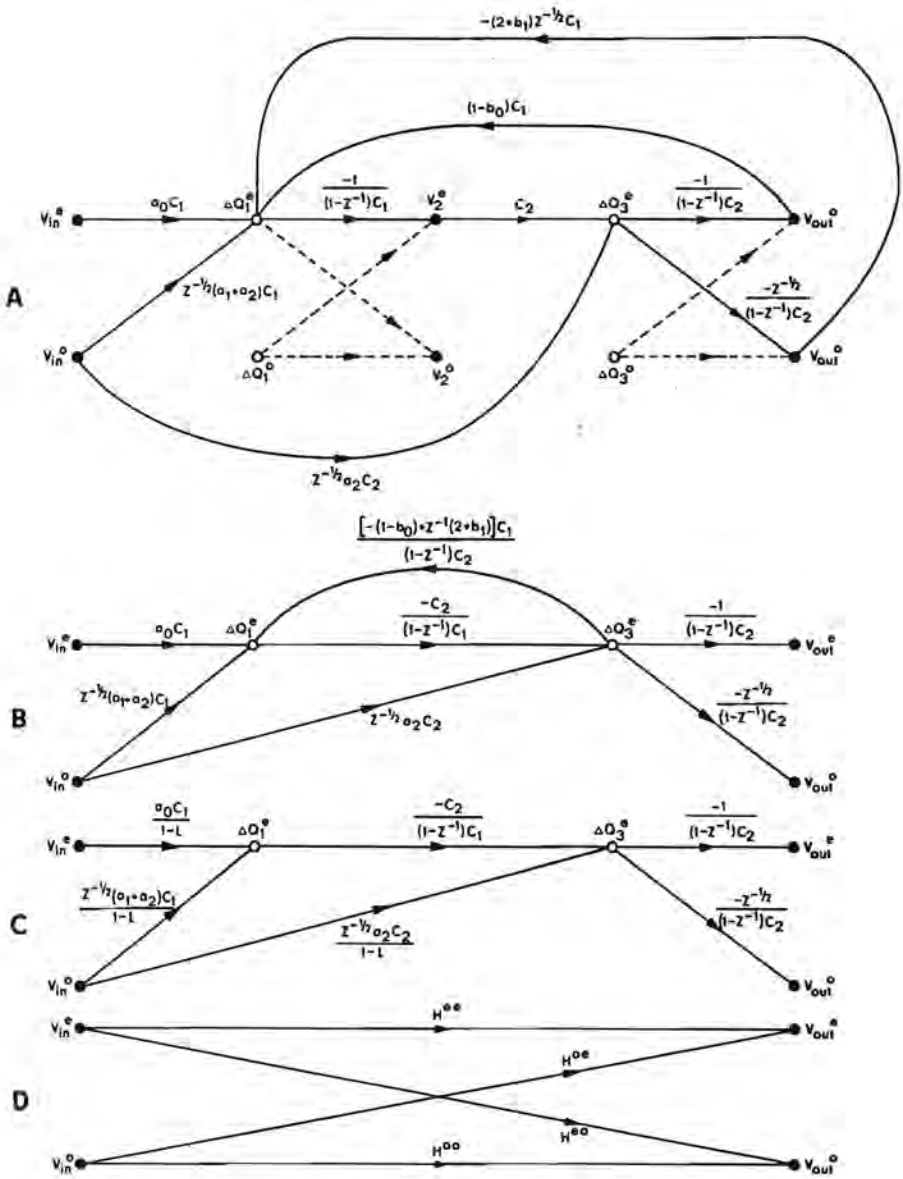


fig.3.12: SFG representation of the circuit of fig.3.10

a: SFG as a composition of elementary graphs of fig.3.11

b: simplified SFG with reduced number of nodes and branches

c: SFG after elimination of the loop

d: final SFG

fig.3.11, resulting in the SFG representation of the entire circuit as given in fig.3.12.
This SFG can be simplified by omitting the redundant branches of the opamp networks (dashed lines in fig.3.12a) and combining the two feedback branches, resulting in the SFG of fig.3.12b.
Then the loop with gain

$$L = \frac{(1-b_0) - z^{-1}(2+b_1)}{(1-z^{-1})^2}$$

can be eliminated (fig.3.12c), by dividing all branches ending on this loop by

$$1-L = \frac{b_0 + b_1 z^{-1} + z^{-2}}{(1-z^{-1})^2}$$

Finally elimination of the nodes marked ΔQ_2^e and ΔQ_3^e results in the SFG of fig.3.12d, with

$$H^{ee} = \frac{V^e_{out}}{V^e_{in}} = \frac{a_0}{b_0 + b_1 z^{-1} + z^{-2}} \qquad (3.8a)$$

$$H^{eo} = \frac{V^o_{out}}{V^e_{in}} = z^{-1/2}\, H^{oe} \qquad (3.8b)$$

$$H^{oe} = \frac{V^e_{out}}{V^o_{in}} = z^{-1/2}\, \frac{a_1 + a_2 z^{-1}}{b_0 + b_1 z^{-1} + z^{-2}} \qquad (3.8c)$$

$$H^{oo} = \frac{V^o_{out}}{V^o_{in}} = z^{-1/2}\, H^{oe} \qquad (3.8d)$$

If the input signal is fixed for a full clock period, such that $V^o_{in} = z^{-1/2}\, V^e_{in}$, then

$$H^{ee} = z^{1/2} H^{eo} = z^{-1/2} \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{b_0 + b_1 z^{-1} + z^{-2}} \qquad (3.9)$$

Note that the locations of the realizable poles and zeros are restricted. In order to prevent the need for negative capacitances both a_2/a_0 and $(a_1+a_2)/a_0$ have to be non-negative. Furthermore b_0 cannot exceed one, b_1 cannot be smaller than -2.

This SFG analysis method plays an important role here, because it will be used as a tool for the SC synthesis methods, presented in chapter 4.
Two further remarks need to be made about this analysis method.

1. An equivalent SFG representation of the opamp network is proposed here, as given in fig.3.13. This reflects the physical mechanisms in this network in a better way and has the advantage of resulting in more simple expressions for the branch gains.

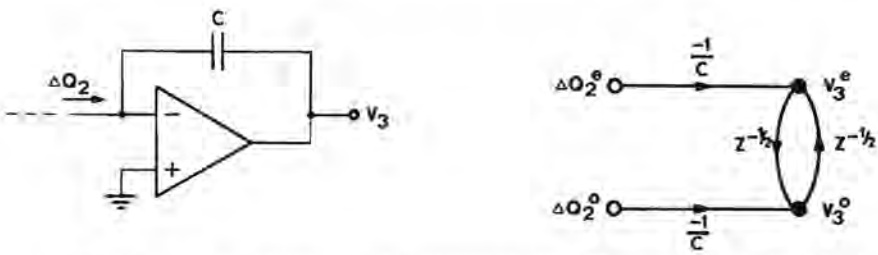


fig.3.13: Alternative SFG representation for an opamp network in a biphase clock circuit.

2. This analysis method can be extended, such that the finite gain effects of the amplifiers can be incorporated, as will be presented below.

When the opamp network of fig.3.13 has an amplifier with finite gain A_0 then

$$\Delta Q_2^e = C\,[(V_3^e - V_2^e) - z^{-1/2}(V_3^o - V_2^o)] \qquad (3.10a)$$

$$\Delta Q_2^o = C\,[(V_3^o - V_2^o) - z^{-1/2}(V_3^e - V_2^e)] \qquad (3.10b)$$

with V_2 being the voltage at the inverting amplifier input, which is no longer zero, but $V_2^e = -V_3^e/A_o$ and $V_2^o = -V_3^o/A_0$.
Now

$$\Delta Q_2^e = -C\,(1 + \frac{1}{A_0})\,(V_3^e - z^{-1/2}\,V_3^o) \qquad (3.11a)$$

$$\Delta Q_2^o = -C\,(1 + \frac{1}{A_0})\,(V_3^o - z^{-1/2}\,V_3^e) \qquad (3.11b)$$

or conversely:

$$V_3^e = -\frac{\Delta Q_2^e}{(1-z^{-1})\,C\,(1+\frac{1}{A_0})} - \frac{z^{-1/2}\Delta Q_2^o}{(1-z^{-1})\,C\,(1+\frac{1}{A_0})} \qquad (3.12a)$$

$$V_3^o = -\frac{\Delta Q_2^o}{(1-z^{-1})\,C\,(1+\frac{1}{A_0})} - \frac{z^{-1/2}\Delta Q_2^e}{(1-z^{-1})\,C\,(1+\frac{1}{A_0})} \qquad (3.12b)$$

or with remark 1 above:

$$V_3^e = -\frac{\Delta Q_2^e}{C\,(1+\frac{1}{A_0})} + z^{-1/2}\,V_3^o \qquad (3.13a)$$

$$V_3^o = -\frac{\Delta Q_2^o}{C\,(1+\frac{1}{A_0})} + z^{-1/2}\,V_3^e \qquad (3.13b)$$

The charge ΔQ_2 delivered by the input network will also be changed due to the finite amplifier gain.
For an input network consisting of an unswitched capacitor C_s between a voltage source V_1 and the inverting input of the amplifier (fig.3.14a)

$$\Delta Q_2^e = C_s[(V_1^e + V_3^e/A_0) - z^{-1/2}(V_1^o + V_3^o/A_0)] \qquad (3.14a)$$

$$\Delta Q_2^o = C_s[(V_1^o + V_3^o/A_0) - z^{-1/2}(V_1^e + V_3^e/A_0)] \qquad (3.14b)$$

The resulting SFG is given in fig.3.14b.

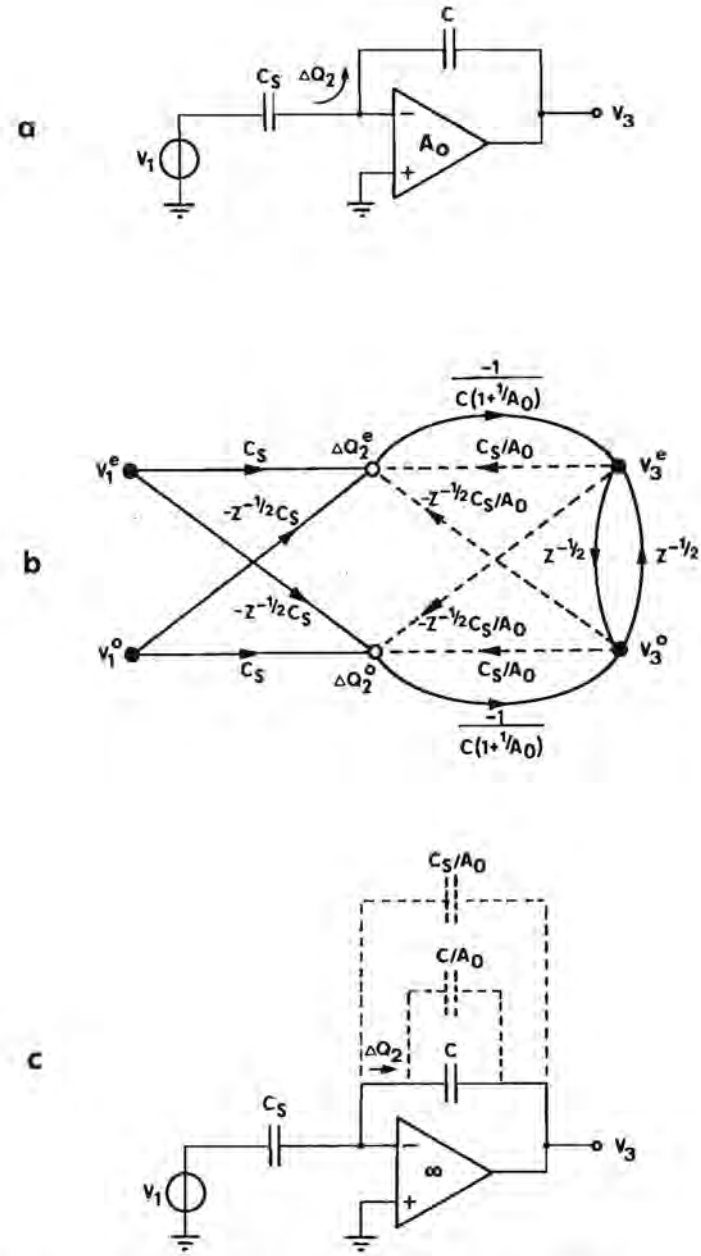


fig.3.14 a: SC circuit with finite gain amplifier
b: corresponding SFG representation
c: SC circuit with infinite gain amplifier and virtual capacitors.

The interesting observation can be made that the finite gain of the amplifier can be fully incorporated in virtual capacitors.
The four SFG branches representing the input capacitor C_s have four 'mirror-image' branches (dashed in fig.3.14b), that can be considered as branches representing a virtual capacitor C_s/A_0 between the output and inverting input of the amplifier.
The altered branch gains of the opamp network can be considered as the result of an extra feedback capacitor C/A_0 (fig.3.14c).
In appendix B a number of elementary SC circuits, that will play an important role in the next chapters, comprising finite gain amplifiers, with corresponding SFG's and virtual capacitor representation are tabulated.

4. SYNTHESIS METHODS FOR BIPHASE STRAYS-INSENSITIVE SWITCHED CAPACITOR FILTERS.

In chapter 4.1 we will first examine the consequences of strays-insensitivity, that we demand for our synthesis method. As a starting point, sufficient conditions known as the 'Hasler constraints' will be used. As it turns out, the blindfolded application of these constraints wrongly excludes a useful class of circuit nodes. Therefore we will permit this additional class, resulting in 'extended Hasler constraints', without releasing the strays-insensitivity demand. Combining these extended constraints with the exclusion of redundant circuit configurations results in a very limited set of possible SC structures.

As the extended Hasler constraints automatically result in circuits, for which the SFG analysis of chapter 3.3 is applicable, we will use this method as a tool for the synthesis. However, before this is done, the original SFG approach will be simplified further. As will be shown, the limited set of SC structures results in an even smaller set of allowable branches in the SFG description.

On the one hand we then have an extremely small set of allowable building blocks (branches), and on the other hand a very simple analysis method (SFG), that we will use in reverse as a synthesis tool.

Two synthesis methods, based on this concept, will be considered in this chapter. The first one is an exhaustive approach, briefly discussed in section 4.2. Next an SFG synthesis, based on node addition is considered in section 4.3.

Because of its importance for this thesis and the resulting extensiveness of its discussion, the treatment of a third method will be postponed to chapter 5.

4.1 BASIC CONCEPTS FOR STRAYS-INSENSITIVE SYNTHESIS.

In [24] Hasler formulates two topological constraints that guarantee insensitivity with respect to the following strays:

- of the desired capacitors from their bottom and top plates to ground,
- of the amplifier output and inverting and non-inverting amplifier inputs to ground as well as the parasitic capacitance between these two inputs,
- between the terminals of the switches and ground,

as depicted in fig.4.1.

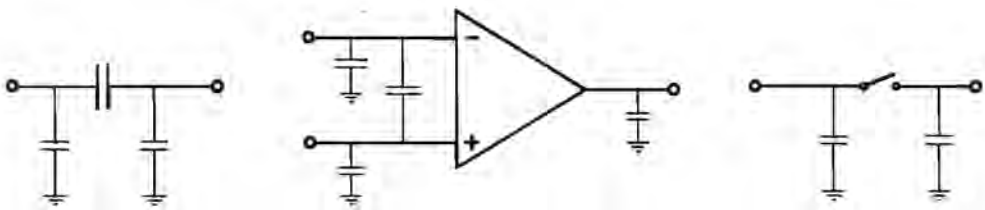


fig.4.1: Stray capacitances referred to by Hasler's constraints.

The following classes of nodes are defined:

- V-nodes: (voltage source nodes), comprising the operational amplifier output nodes, as well as the input nodes of the circuit;
- I-nodes: (virtual ground nodes), the input of an operational amplifier with negative feedback, whose other input is connected to ground;
- 0-nodes: ground nodes.

With these definitions the Hasler constraints can be formulated as follows:

1. In any clock-phase the circuit does not contain nodes other than V-nodes, I-nodes and 0-nodes;
2. A terminal of a capacitance is never switched from a V-node in one clock-phase to an I-node in the next phase.

This formulation is in fact an extension of the original Hasler constraints, which were stated for circuits with a biphase clock, to circuits with an n-phase clock.

The above mentioned constraints are sufficient conditions for strays insensitivity of SC filters.
In the original paper it is conjectured that this class contains essentially all stray capacitance insensitive filters. However, this conjecture will be contradicted here. The synthesis methods proposed in this thesis result in strays insensitive filters, but allow a class of nodes that is not mentioned in the first Hasler constraint. This class of nodes is what will be referred to as F-nodes: nodes that are floating.
As an example in fig.4.2 a circuit is given, that can easily be shown to be strays insensitive, although it contains an F-node in clock-phase 'e' (left plate of capacitor C_1).

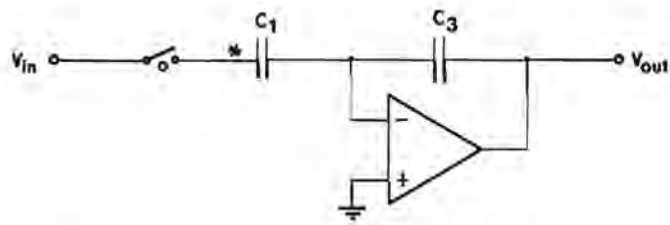


fig.4.2: Example of a strays insensitive circuit, containing an F-node in clock-phase 'e'.

Examples can be given of circuits that comprise one or more F-nodes, and essentially are strays-sensitive. Nevertheless it will be shown that for circuits with a biphase clock all non-redundant switched capacitor configurations comprising F-nodes are strays-insensitive. For the time being, F-nodes are added and yield what will now be called the extended Hasler restrictions. Afterwards the switched

capacitor configurations that contain F-nodes will be checked for strays insensitivity.

The first extended Hasler constraint makes the application of Signal Flow Graph analysis, as explained in chapter 3.3, convenient to apply.

Note that the first extended Hasler constraint actually assumes the operational amplifiers to be ideal.
However, as long as the gain of the amplifiers is sufficiently high (what in general already should be the case, in order to prevent the filter to have an unacceptable high sensitivity for this gain), the influence of stray capacitances is negligible.

In a strays insensitive SC circuit with a biphase clock (clock-phases 'e' and 'o') a capacitor with its 2 terminals (a and b) and 4 types of nodes (V, I, 0 and F) can be applied in 256 possible modes.
However, in order not to be redundant, at least one of its terminals should be connected to an I-node in at least one clock-phase. We will assume this to be the b-terminal in the 'o' clock-phase (of course the labels of the terminals (a/b) as well as of the clock-phases (e/o) can be mutually interchanged). This reduces the number of possible modes to 64.
Now, according with the second Hasler restriction, terminal b may not be a V-node in phase 'e'. This reduces the number of possible modes to 48.
There should at least be one terminal which is a V-node in one of the clock-phases, otherwise the capacitor is redundant. This reduces the number of possible modes further to 21.
According with the second Hasler constraint this V-node is not allowed to be an I-node in the other clock-phase. This reduces the number of possible modes further to 15.
These 15 possible modes are enumerated in table 4.1.

Of these 15 modes, mode 11 and 12 in table 4.1 are the same as mode 3 and 4 resp., because of clock-phase symmetry.
Mode 13 is a redundant mode, because the capacitor can't be charged nor discharged.

mode \ clock-phase / terminal	e a	o a	e b	o b	
1	0	V	0	I	
2	V	0	0	I	
3	F	V	I	I	
4	0	V	I	I	
5	V	V	0	I	
6	V	V	I	I	
(7)	V	V	F	I	
(8)	F	V	F	I	
(9)	F	V	0	I	
(10)	0	V	F	I	
(11)	V	F	I	I	as mode 3 (clock symm.)
(12)	V	0	I	I	as mode 4 (clock symm.)
(13)	V	F	F	I	redundant
(14)	V	F	0	I	redundant
(15)	V	0	F	I	redundant

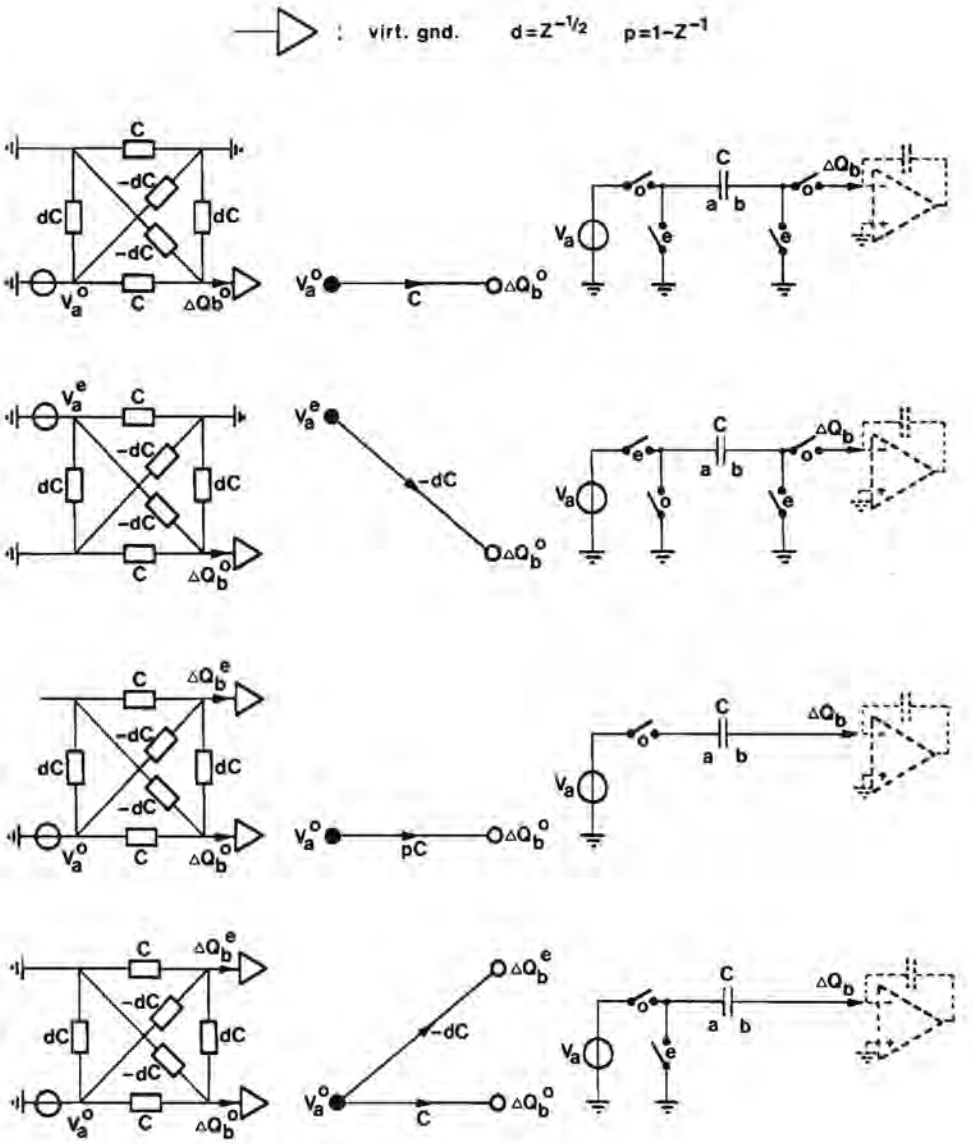
table 4.1: Modes for a (switched) capacitor configuration.

Mode 14 is a redundant mode, because though the capacitor can be charged it can't pass its charge to the I-node.
Mode 15 is a redundant mode, because though the capacitor can pass its charge to the I-node, it can't be charged.

It should be mentioned here, that mode 14 is sensitive for the stray capacitance connected to terminal a, and can serve as an example of stray sensitivity due to the application of an F-node. However, in consequence of the fact this mode is redundant, and therefore will not be used in the considered synthesis methods, this will be of no concern to us.

The remaining 10 modes are enumerated in table 4.2.

table 4.2: Modes for a non-redundant (switched) capacitor configuration: z-domain equivalent circuits, SFG representations and example circuits. (clock-phases 'e' and 'o' may be mutually interchanged)



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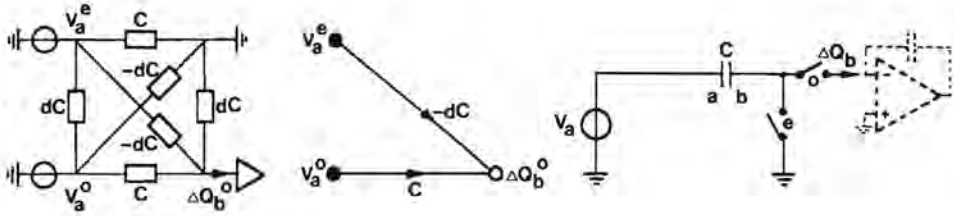
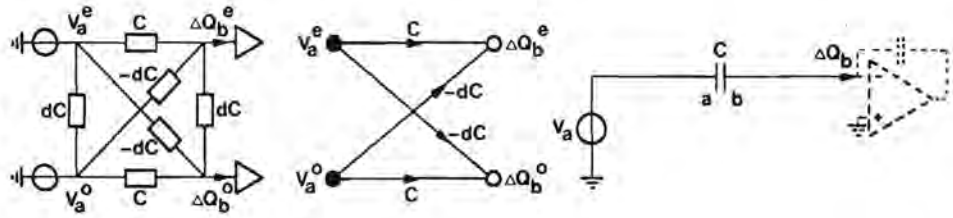
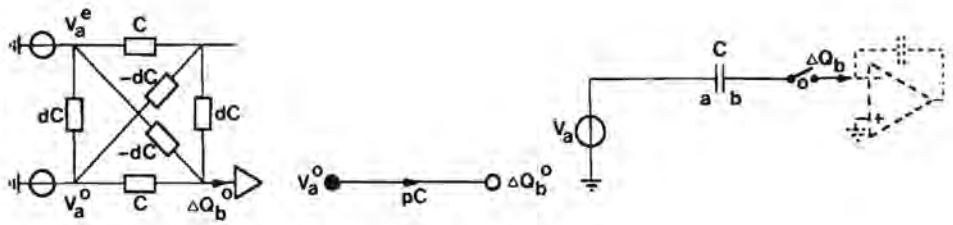

V_a^e
C
-dC
dC
dC
-dC
V_a^o
C
ΔQ_b^o
-dC
C
V_a
a
b
ΔQ_b

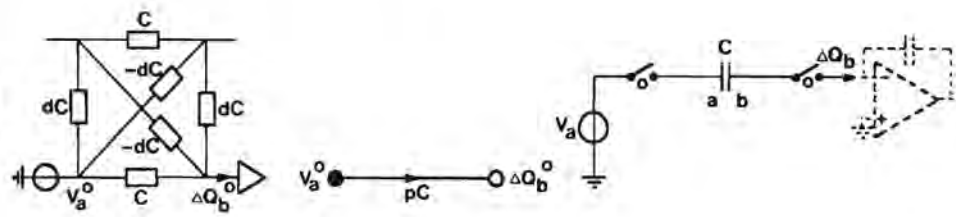
6


V_a^e
C
ΔQ_b^e
-dC
dC
dC
-dC
V_a^o
C
ΔQ_b^o
C
-dC
-dC
C
V_a
a
b
ΔQ_b

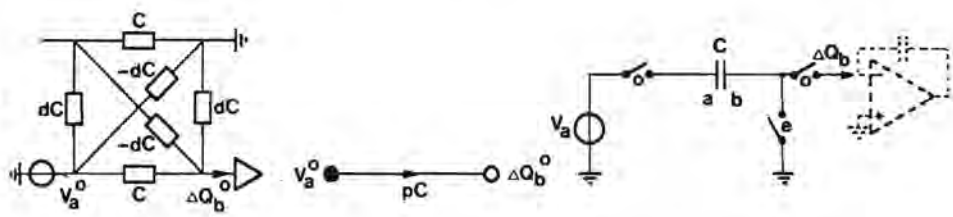
7


V_a^e
C
-dC
dC
dC
-dC
V_a^o
C
ΔQ_b^o
pC
C
V_a
a
b
ΔQ_b

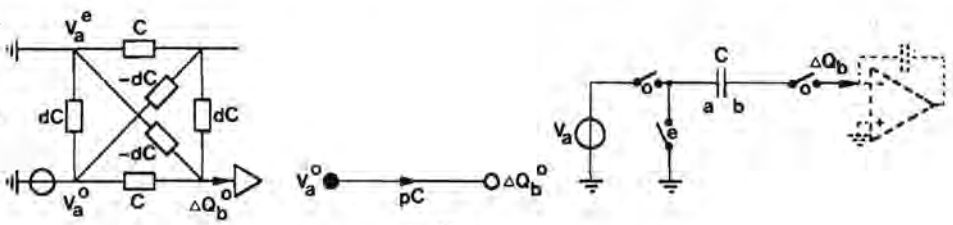
8


C
-dC
dC
dC
-dC
V_a^o
C
ΔQ_b^o
pC
C
V_a
a
b
ΔQ_b

9


C
-dC
dC
dC
-dC
V_a^o
C
ΔQ_b^o
pC
C
V_a
a
b
ΔQ_b

10


V_a^e
C
-dC
dC
dC
-dC
V_a^o
C
ΔQ_b^o
pC
C
V_a
a
b
ΔQ_b

Modes 3, 7, 8, 9 and 10 all realize the same transfer. Modes 8, 9 and 10 however apply one or more redundant switches and will not be used. When modes 3 and 7 are being compared, mode 3 has the slight advantage of having the switch stray capacitances at the voltage source side. In cases where the amplifier gain is rather low this is better than having them at the 'virtual ground' side of the desired capacitor.

Now mode 3 has to be checked for strays-insensitivity, because it contains an F-node. When the z-domain equivalent circuit is extended with the admittances representing the parasitic capacitances C_A and C_B (fig.4.3), ΔQ_B^e and ΔQ_B^o indeed turn out to be independent of these strays.

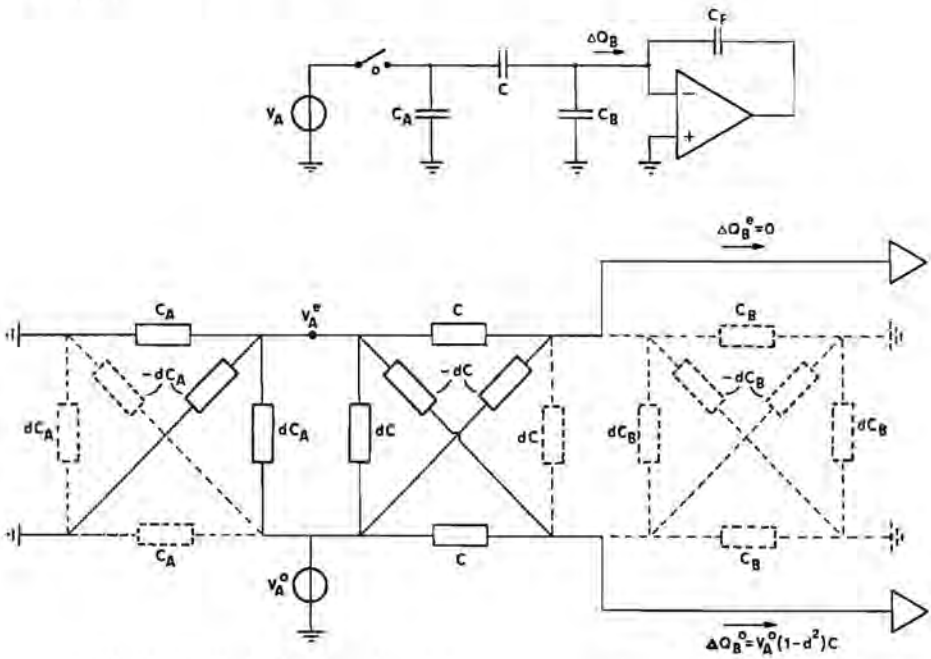
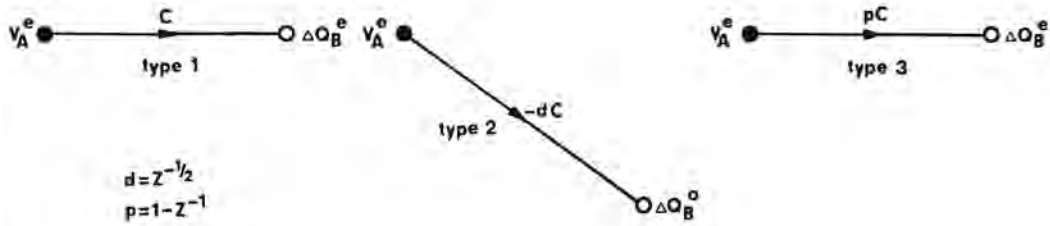


fig.4.3: Mode 3 circuit with stray capacitances and z-domain equivalent circuit (redundant equivalent admittances drawn with a dashed line).

In a similar way modes 7, 8, 9 and 10 can also be checked and found to be strays-insensitive. This has been omitted here, because these modes will not be used. This leaves modes 1 to 6 as the elementary input networks for strays insensitive biphase clocked SC filter synthesis.

A closer look at table 4.2 shows that the SFG representations of all non-redundant strays-insensitive (switched) capacitor configurations are composed of only three types of branches (fig.4.4).



type 1: +C -branch (modes 1, 4, 5 and 6)
type 2: -dC -branch (modes 2, 4, 5 and 6) $(d = z^{-1/2})$
type 3: +pC -branch (modes 3, 7, 8, 9 and 10) $(p = 1-z^{-1})$

fig.4.4: elementary SFG branches for input networks (clock-phases 'e' and 'o' may be mutually interchanged).

Now the opamp networks will be considered.
Since the clock-phases are nonoverlapping, we will demand a continuous-time feedback path around the operational amplifiers in order to guarantee stability. This results in 2 modes (fig.4.5), where again clock-phases 'e' and 'o' may be mutually interchanged.
The corresponding SFG representations will be referred to as 'type 4' and 'type 5' respectively.

All other SC networks around an operational amplifier are considered as input networks.

Knowing the set of allowable elementary graphs (type 1 to 5), these could serve as a starting point for a synthesis method based on Signal Flow Graphs. However, before this is done a further simplification will be proposed.

Temporarily all continuous-time feedback capacitors of the opamp networks will be scaled to a value of 1. This is no restriction, because the voltage transfer of the filter is determined by the ratios

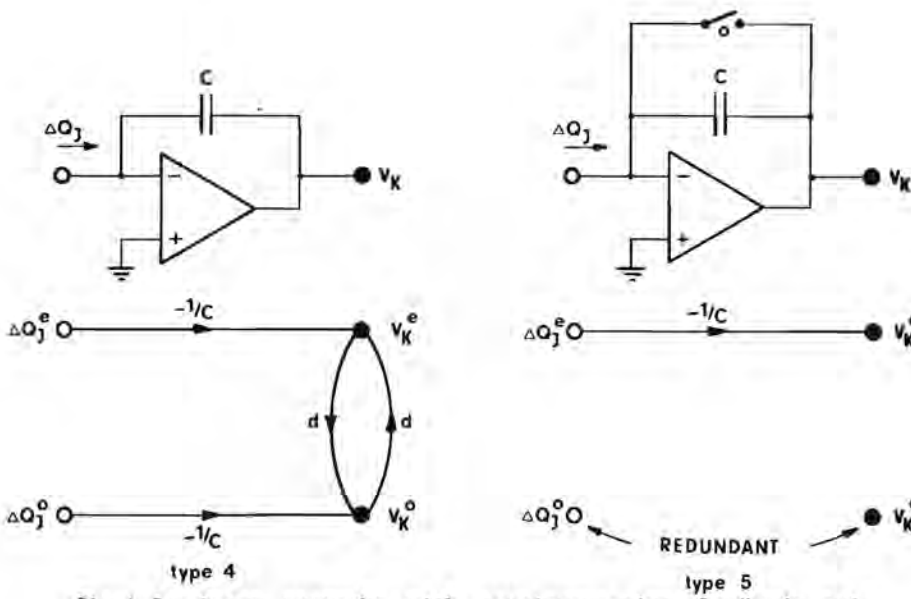


fig.4.5: Opamp networks with continuous-time feedback and corresponding SFG representations.

of the capacitors of the input networks and the capacitors of the opamp networks. Later on we will rescale these capacitors in order to minimize the total capacitance of the filter.

As a next step all charge-increment nodes in the SFG are changed in sign. This corresponds to multiplication of all branches (except for the branches of the d*d loop of the 'type 4' graph) with -1.
Every charge-increment node has only one branch leaving it. This is a branch with transfer 1, which ends on the voltage node of the same opamp network. Now all charge-increment nodes in the SFG are removed by means of contracting them in the voltage nodes of the corresponding opamp output.
The advantage of these steps is that the obtained SFG consists of voltage nodes only, and has a reduced number of branches.

The set of elementary SFG structures is given in fig.4.6.

Comparatively, the 'type 5' structure is of little value: it consists of an isolated node, at the price of an operational amplifier, a

switch and a capacitor (see fig.4.5).
Besides, because of the short circuit switch, the realization of this single node will have a deteriorated sensitivity for the finite bandwidth and slew-rate of the amplifier.

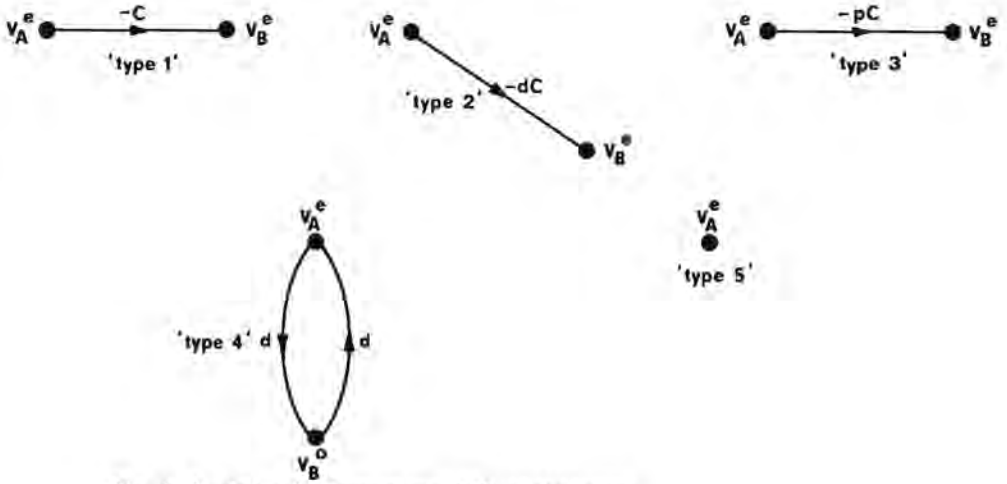


fig.4.6: Set of elementary SFG structures.

4.2 AN EXHAUSTIVE SYNTHESIS APPROACH.

The synthesis of strays-insensitive SC filters with a biphase clock can be considered now as the following problem: given the opamp network branches ('type 4' and rarely 'type 5') place the input network branches 'type 1', 'type 2' and 'type 3' in such a way, that the transmission of the total SFG is in accordance with the desired transfer function.
The opamp network branches could be regarded as the 'skeleton' of the filter (fig.4.7), which is to be completed by the input network branches, giving it its 'personality'.

One approach could be to place <u>all</u> possible input network branches, from every node to every node, calculate the input to output transfer of the graph, and remove all superfluous branches again. There is a restriction: in order to avoid possible stability problems, delay free loops containing more than one amplifier will not be allowed. (This

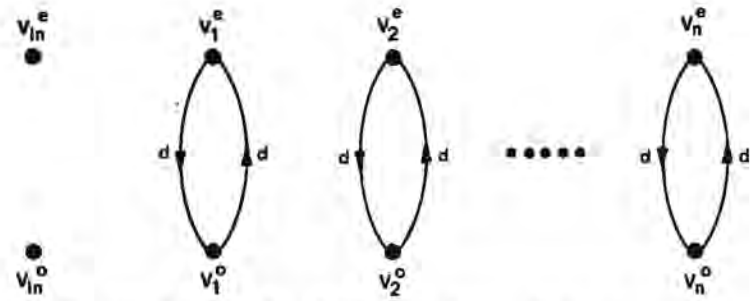


fig 4.7: 'Skeleton' of a filter, made up of its opamp network branches.

will be worked out in more detail in chapter 6). In the simplified SFG representation, as was proposed in this chapter, these loops can easily be determined: they form loops in the graph that are totally in one clock-phase, with exception of self-loops.
Nevertheless the number of branches left is still $4n^2+8n$, when there are n amplifiers involved, which makes this method unpractical for synthesis of higher order filters. Furthermore this approach can hardly be called a synthesis method, since it is actually an exhaustive search based on analysis. On the other hand, it could be an interesting basic concept for a computer program generating a library of all (for the given restrictions) possible canonic or pseudo canonic SFG's for a certain limited number of amplifiers.

4.3 SYNTHESIS BY ADDITION OF NODES.

Another approach is one which is based on a method that has already been applied [25] for the synthesis of digital filters.
The synthesis method in question is based on the observation that the complexity of expressions for the gain of the branches in a SFG can often be reduced by introducing new nodes. (This is in fact the opposite of SFG analysis based on node elimination [26]). It should be mentioned that the synthesis of digital filters using this method, is far more straight-forward than that of SC filters, because in our case we have to deal with clock-phases and furthermore with fixed signs of the branches.

This approach leaves much freedom to the designer in the sense of how to construct the transfer function and how to manipulate the corresponding graph in order to end up with branches from the allowed set only. This method will not automatically lead to a fixed filter structure, like many other synthesis methods do. As will be shown in an example, this method can sometimes generate a circuit that has one or more advantages with respect to other designs.
On the other hand this freedom means that almost at every step in this approach the designer has to choose between a number of alternatives. It is often difficult to predict which one will lead to 'the best' final circuit for his application. Although counter examples can be given, in practice trying to minimize the total complexity of all branches at every step often results in a canonic or pseudo-canonic circuit.

As an example for the application of this method a 2nd order notch filter will be designed.

In order to obtain a filter with good sensitivity properties, the transfer function will first be written in a suitable way, using a form that is more or less comparable with the one used in [28].
The desired form of the transfer function is:

$$H(z^{-1}) = \upsilon \frac{z^{-2} - z^{-1}(2-\sigma) + 1}{z^{-2} - z^{-1}(2+\mu-\epsilon) + (1+\mu)} = \frac{p^2\upsilon + d^2\gamma}{p^2 + d^2\epsilon + p\mu} \qquad (4.5)$$

with υ, γ, ϵ and $\mu > 0$, $\gamma = \sigma\upsilon$ $\quad d = z^{-1/2}$, $p = 1-z^{-1}$.

It can be shown that eq.(4.5) has a much better sensitivity property for its parameters than

$$H'(z^{-1}) = \upsilon \frac{z^{-2} + z^{-1}b + 1}{z^{-2} + z^{-1}a_1 + a_0}, \qquad (4.6)$$

especially for designs with a high Q or a relative high clock frequency.

Using Mason's rule, a transfer function

$$H = \frac{V_{out}}{V_{in}} = \frac{N}{D} = \frac{N}{1-D'} \qquad (4.7)$$

can be represented by a SFG as drawn in fig.4.8a.

Before this is done, the numerator and denominator of the considered transfer function are divided by p.
This is done for the following reason. The ('type 4') d^2-loops can be incorporated in the branches ('type 1, 2 and 3') ending on these loops, by dividing these latter branches by $1-d^2$= p (Mason's rule). When we restrict ourselves to the application of 'type 1, 2, 3 and 4' branches, any node in the SFG that is not an input node is an amplifier output node, and thus connected to a 'type 4' d^2-loop. This means that all 'type 1, 2 and 3' branches will be divided by p, so one is in fact working with branches -C/p, dC/p and -C. However, in fig.4.8 the self-loop connected to the filter output node (containing its d^2 loop) is explicitly drawn, so there may exist elements in the numerator or denominator with p^1. Powers of p higher than 1 are not possible: for instance p^2C could be written as a product (cascade) of branches $-pC_1$ * $-pC_2$, but the $-pC_1$ branch, which is not ending on the the filter output node would be divided by p.

The transfer function is now written as:

$$H(z^{-1}) = \frac{p\upsilon + \frac{d^2}{p}\gamma}{1 - \left[d^2 - \frac{d^2}{p}\epsilon - \mu \right]} \qquad (4.8)$$

thus in fig.4.8a

$$N = p\upsilon + \frac{d^2}{p}\gamma \qquad \text{and} \qquad D' = d^2 - \frac{d^2}{p}\epsilon - \mu \qquad (4.9)$$

and the SFG can be redrawn as given in fig.4.8b.
In the SFG only the $-\mu$ branch is directly realizable ('type 1').
By means of changing the sign of the output, the $p\upsilon$ branch is changed into $-p\upsilon$, which is also realizable ('type 3') (fig.4.8c.).

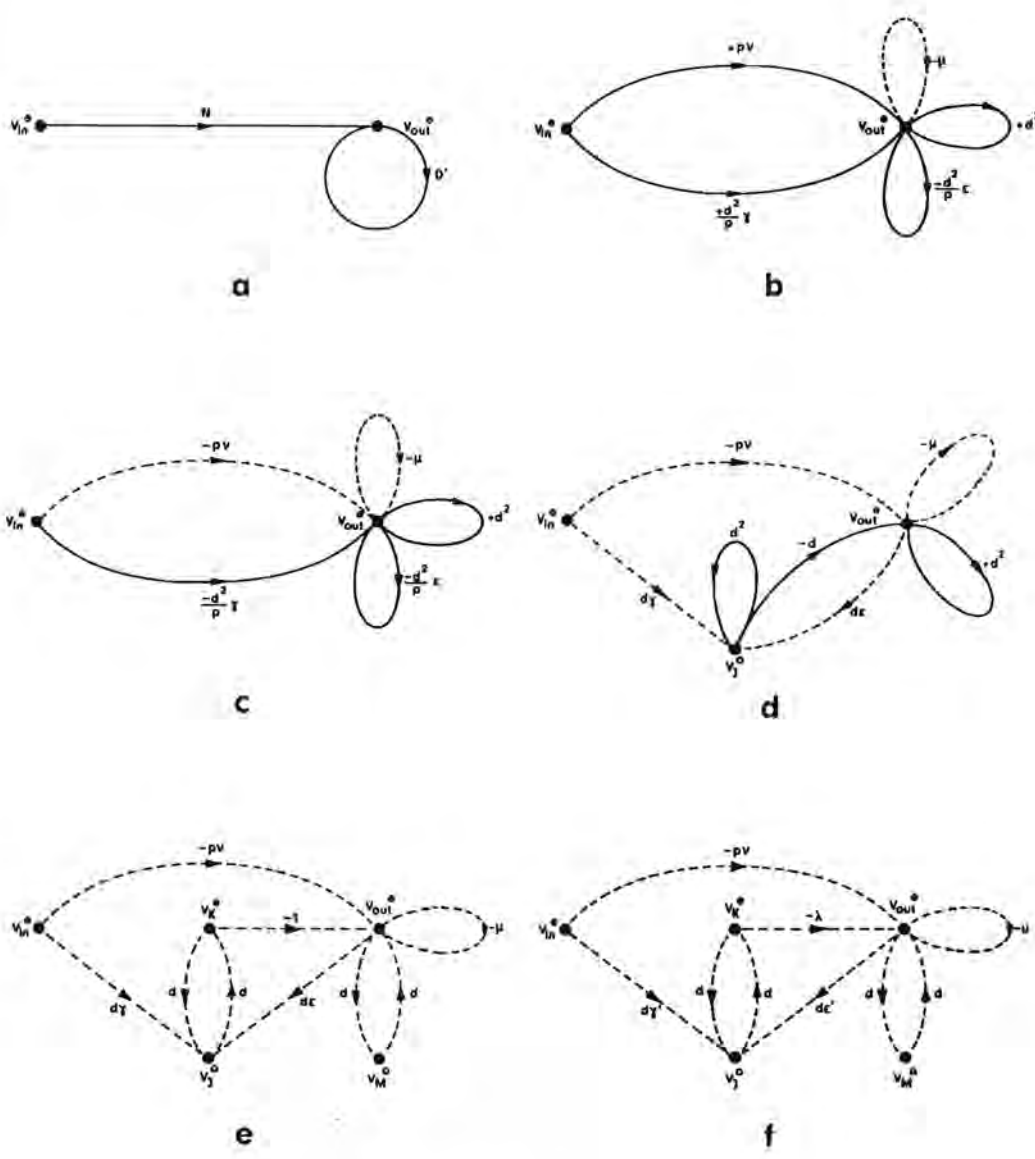


fig.4.8: Development of an elementary SFG (a) by way of a number of intermediate steps (b-e) into a directly realizable graph (f) (Directly realizable branches drawn with dashed lines).

There still are three branches left that are not directly realizable: the d^2 branch, the $\frac{-d^2}{p}\gamma$ branch and the $\frac{-d^2}{p}\epsilon$ branch. The latter two branches have the same kind of expression, which makes it obvious to try to combine their realizations. This has been done in fig.4.8d.
Of the three not directly realizable branches, two are d^2 loops, that can be realized introducing a node for each loop and the application of 'type 4' branches. The remaining -d branch can be realized as a cascade of an already existing d branch ('type 4') and a -1 branch ('type 1'), as shown in fig.4.8e.
The -1 branch may be rescaled to a value of $-\lambda$, when the $d\gamma$ and $d\epsilon$ branches are rescaled accordingly to a value of $d\gamma'=d\gamma/\lambda$ and $d\epsilon'=d\epsilon/\lambda$, resulting in the final SFG of fig.4.8f.
This rescaling has the advantage of resulting in more acceptable capacitor ratios, especially for relative high clock frequencies.

When we rename V_j^o to V_1^o, V_k^e to V_1^e and V_m^o to V_{out}^o, this final SFG can now be translated into a SC circuit, using table 4.2.
A direct translation results in the circuit of fig.4.9.

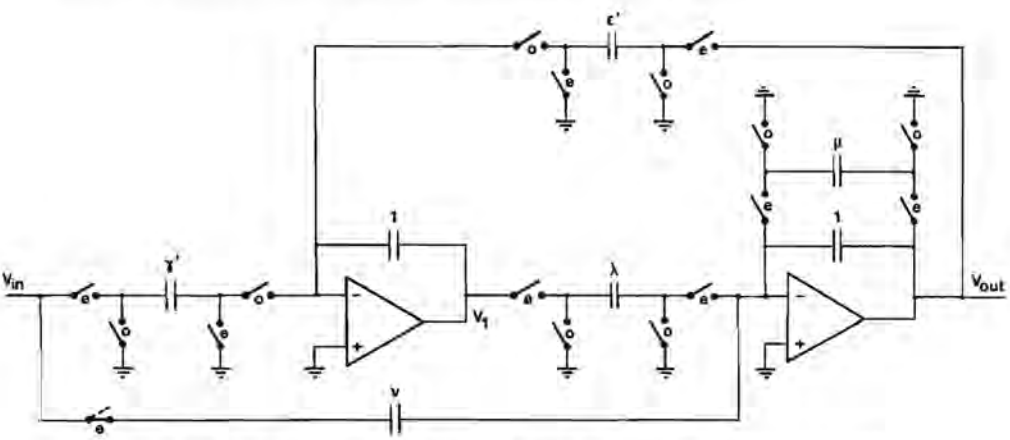


fig.4.9: SC circuit as obtained by a direct translation of the SFG of fig.4.8f, using table 4.2.

This circuit can be simplified, by means of the well-known 'switch-sharing' method: a closer look at the circuit reveals that there are many nodes that have the same voltage in both clock-phases and can thus be short-circuited. Then a great number of switches,

being active in the same clock-phase can be seen to function in parallel, so there are many redundant switches in the circuit, that can be omitted (fig.4.10).

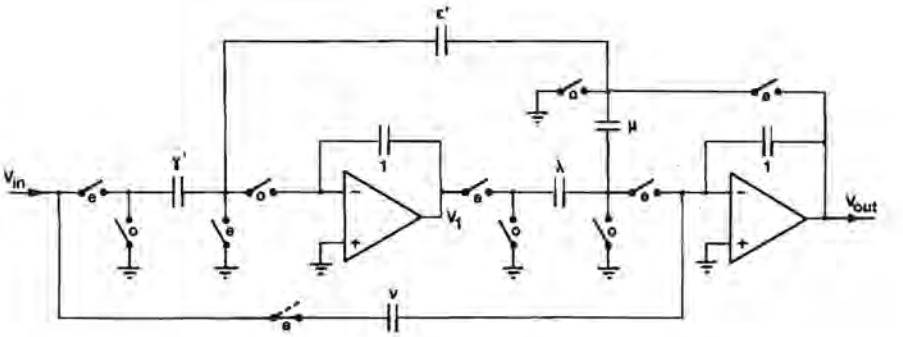


fig.4.10: Final circuit for a strays-insensitive notch filter, realizing the transfer function of eq.(4.5).

It is interesting to know, that exactly the same transfer function is realized by a different circuit, well-known as the 'Gregorian notch biquad' [29].

Since the formula for its transfer function equals that of eq.(4.8), it will have the same sensitivities for the capacitor values as for the circuit of fig.4.10.
However, a closer look at both circuits reveals a number of differences between them.
In the first place the lack of need for an input signal that is fixed over a full clock period (symbolized by the sample & hold circuit in fig.4.11) in the circuit of fig.4.10 can be mentioned. Furthermore, counting the switches in both circuits shows that there is one switch less in our circuit.
When the output voltage is only needed in clock-phase 'o', the switch drawn with a dashed line can be omitted, as will be shown in chapter 5, saving another switch.
In a design example, given by Gregorian in the same paper, the circuit is dimensioned for a notch frequency of 60 Hz, a 3-dB bandwidth of 58 Hz and a sampling frequency of 8 kHz. As it turns out there, the

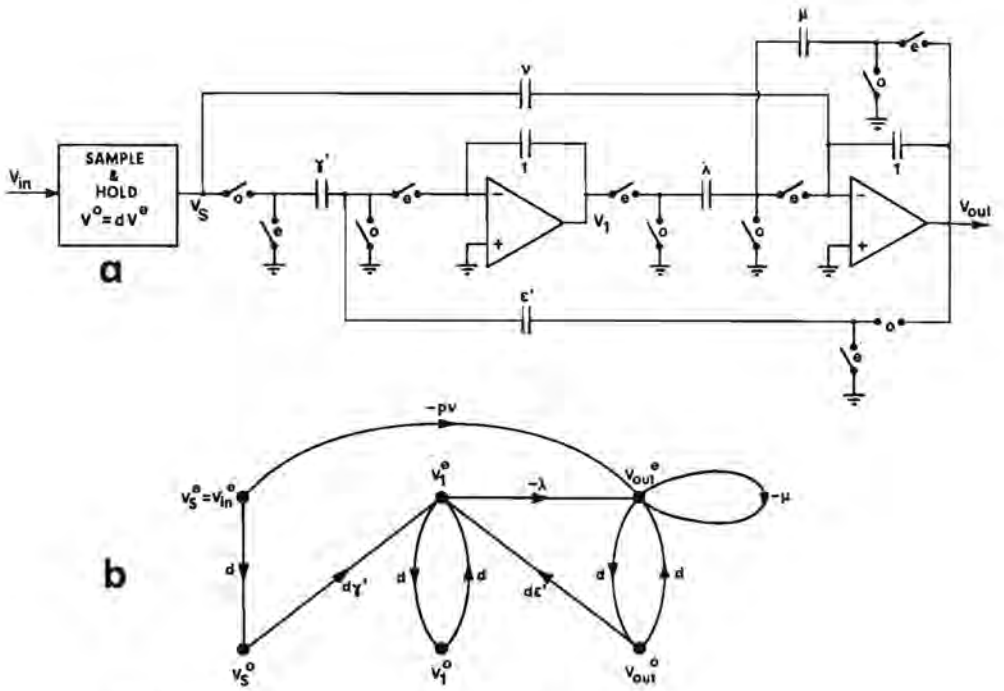


fig.4.11a: Gregorian notch biquad,
b: corresponding SFG representation.

values of capacitances μ and ϵ' are almost equal. This gives the possibility of saving additional components, by means of application of what will be called 'capacitor sharing'. This will be explained in more detail in chap.5. What it means here, is that capacitors μ and ϵ' can be realized using actually one 'shared' capacitor (fig.4.12).

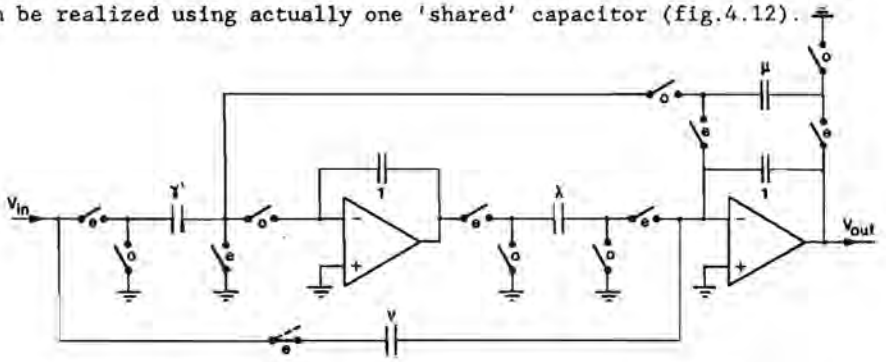


fig.4.12: Simplified version of the circuit of fig.4.10, obtained by the 'shared' application of capacitance μ.

With a very small correction on the capacitances γ' and λ, this circuit realizes exactly the same transfer function as the circuits of figs.4.11 and 4.12.
This 'capacitor sharing' is not possible for the Gregorian notch biquad.

5. SC SYNTHESIS BASED ON A 'STRAYS-INSENSITIVE DESIGN GRAPH'.

In this chapter another synthesis method is presented, which is also based on the application of a SFG, composed of branches of the basic set only ('types 1 - 5').
This method does not give the designer the same amount of freedom as the previous approach, but depends on a SFG with a more or less fixed structure.
One of the main advantages of this method is, that it is far more an algorithmic procedure than the approaches that were presented in sections 4.2 and 4.3.
Other essentials of the considered synthesis method are as follows.

- As an 'input' for this method, a normal transfer function in the z-domain, that has not been specially shaped, will be used. There is no need of a continuous-time prototype filter.
- The 'output' of this method is a strays-insensitive biphase clocked SC circuit with exactly enough degrees of freedom to optimize the dynamic range and to minimize the total capacitance.
- With the exception of a small class of transfer functions, this method is canonic in the number of amplifiers that are applied for their realization.
- For a majority of transfer functions, this method can also handle input signals that are not fixed over a full clock-period.
- On the other hand, the produced output signal itself is fixed over a full clock-period, making it compatible with other filter inputs. This allows us easy cascading of filter networks.
- The filter has no delay free loops containing more than one amplifier.
- The resulting filter structures have good sensitivity properties for their capacitors and amplifier gains in comparison with a number of other designs. Moreover these structures inherently have advantages for the sensitivity to the bandwidth of the applied amplifiers.

First, in section 5.1, two general Strays-insensitive Design Graphs (SDG's), with the above-mentioned properties, will be derived.

As an example, SC filters will be designed in section 5.2, using this SDG approach. Furthermore in this section possibilities for the reduction of circuit complexity and total capacitance, by the application of what will be called 'capacitor sharing' will be described.

One of the designs of section 5.2 was actually built as a breadboard circuit. In section 5.3 the measured amplitude diagram of this circuit will be compared with theoretical curve.

In section 5.4 the sensitivity of the SDG filters to variations of the capacitances, finite amplifier gain and finite amplifier bandwidth will be discussed.

Finally in section 5.5 it will be considered how to deal with amplifiers that have such a low gain, that it significantly affects the filter behavior.

5.1 STRAYS-INSENSITIVE DESIGN GRAPHS.

One of the problems that arise when constructing a maximally general SFG for the synthesis of an extensive class of transfer functions is the fact that the signs of the allowed branches (-C, +dC, -pC and d , with $C \geq 0$) are fixed. However, one can circumvent this limitation and realize a transfer of -dC by means of combining a d branch ('type 4') with a -C branch ('type 1'), as depicted in fig.5.1.

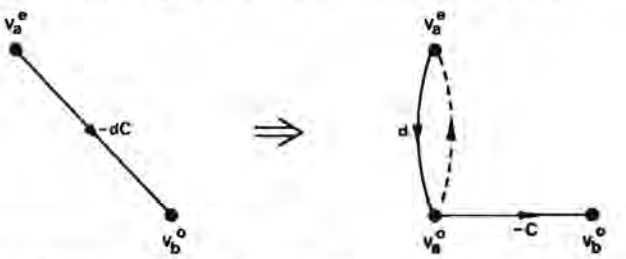


fig.5.1:Creation of a -dC 'branch' as a combination of a d branch ('type 4') with a -C branch ('type 1').

This will only work if there are no other branches ending on the V_a^o node.

In the following synthesis, we first take only the denominator of the transfer function into consideration. For this purpose, an adequate SFG is given in fig.5.2.

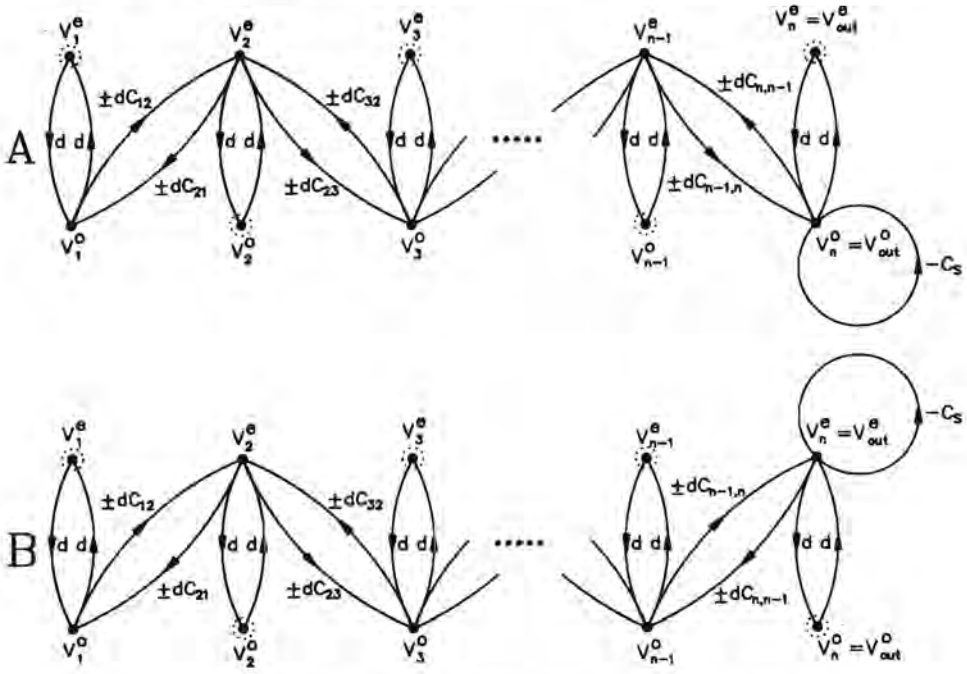


fig.5.2: Loop-structure for the realization of the denominator of the transfer function,
a: n odd,
b: n even.

Here the ±dC branches are in fact +dC branches ('type 2') or -dC branches, realized with the method of fig.5.1 (combining 'type 1 & 4').

To be able to apply the method of fig.5.1 in all situations, no 'type 1, 2 or 3' branches may end on the nodes marked with a dashed circle in fig.5.2.

The only sign that is really fixed is the sign of the $-C_s$ self-loop.

Using Mason's rule it can be shown that the product of the realized poles is

$$\prod_{i=1}^{n} z_{\text{pole } i} = \frac{1}{1+C_s} \qquad (5.1)$$

which thus yields the restriction:

$$0 < \prod_{i=1}^{n} z_{pole\ i} \leq 1. \qquad (5.2)$$

Of course the upper bound means no real restriction, because we are only interested in the realization of stable filters.
On the other hand the lower bound means that the class of transfer functions with an odd number of negative real poles in the z-domain can not be realized with the loop-structure of fig.5.2.
When needed, a negative real pole-zero 'doublet' (which we pay for in terms of circuit elements) could solve this problem. The exact position of this 'doublet' on the negative real z-axis can freely be chosen in the range $-1 < z < 0$, giving the designer a degree of freedom that can for instance be used for the minimization of the total capacitance of the filter. Note that this in fact increases the order of the filter by multiplying its transfer function with $(z + a)/(z + a)$, $0 < a < 1$. Another and often better method is trying to find a transfer function of one order higher than the original. This new transfer function (that of course should not have an odd number of negative real poles) can in general approximate the ideal filter transfer more closely than the original one.

Let us assume that only one branch, with transfer G, would be added to the loop structure of fig.5.2, starting at the input node V^e_{in} and ending on the output node (V^o_n for n odd or V^e_n for n even). In that case, using Mason's rule, the transfer function could be written as a continued fraction expansion:

$$H = \cfrac{G}{1 + \frac{1}{p} C_s - \cfrac{1 \pm \frac{d^2}{p^2} C_{n-1,n} C_{n,n-1}}{1 \pm \frac{d^2}{p^2} C_{n-2,n-1} C_{n-1,n-2} - \cfrac{1}{1 \pm \cdots \cdots \cdots - \cfrac{1}{1 \pm \frac{d^2}{p^2} C_{12} C_{21}}}}} \qquad (5.3)$$

Again, in this expansion, the only restriction turns out to be the sign of $+C_s$.

Next the realization of the numerator of the transfer function will be included.
It is assumed here that the input voltage is fixed during the odd clock-phase, such that $V^o_{in} = dV^e_{in}$. (Of course the 'e' and 'o' clock-phase may again be mutually interchanged).
Now branches from the input nodes to several amplifier output nodes are added, such that the marked nodes are not touched. This results in, what will be called a 'Strays-insensitive Design Graph, form 1' (SDG1), as depicted in fig.5.3.

Note that the signs of the -pC branches ('type 3') are fixed.
However, this is not in fact a restriction. In case we should need a +pC branch we use a -pC branch and change the polarity of the node on which this branch ends. Of course we also have to change the signs of all the other branches ending or starting on this node (except for the self-loops), but that is no problem because these are only + or -dC branches, which we can realize both.

The required number of operational amplifiers (represented by the 'type 4' d*d loops) equals the order n of the filter.

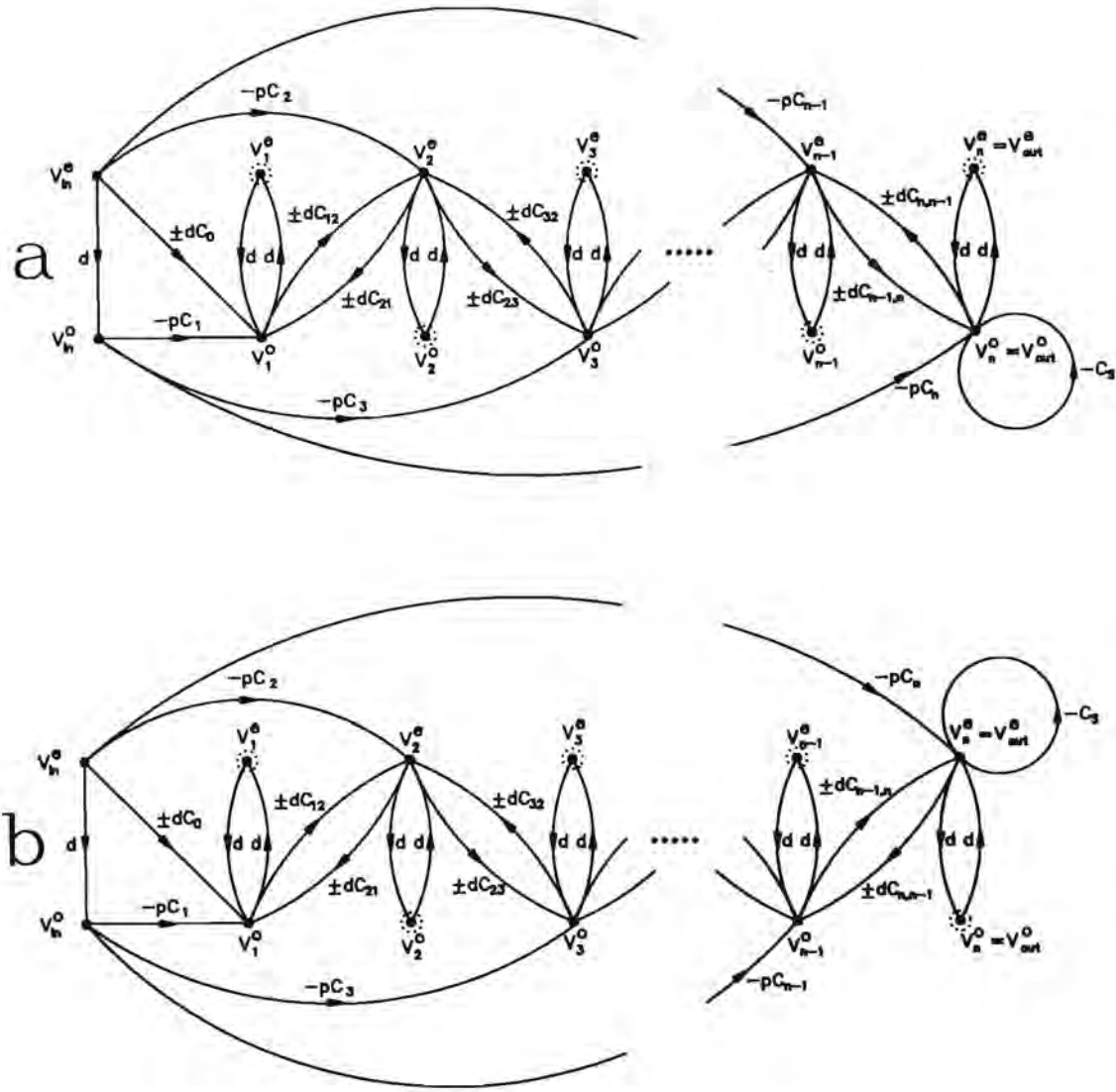


fig.5.3: Strays-insensitive Design Graph, form 1 (SDG1)

a: n odd

b: n even

The number of input network branches ('type 1, 2 and 3') equals 3n, which means that after having realized the 2n+1 filter coefficients we still have n-1 degrees of freedom left.
These can be used to optimize the voltage swings of all n-1 internal amplifier outputs by means of scaling all capacitors connected to the outputs of these amplifiers.
Furthermore we have n continuous-time feedback capacitors of the opamp networks that we scaled to 1, which means that we have n degrees of freedom that can be used to scale all capacitors connected to the n amplifier inputs in order to minimize the total capacitance.
The only delay free loop is the self-loop $-C_s$ containing only one amplifier, so no continuous-time loops of amplifiers are created here.

The SDG of fig.5.3 has the disadvantage to require a fixed input signal for a full clock-period.
It is also possible to compose a SDG, based on the same loop-structure of fig.5.2 with only a single input node for one clock-phase. This results in the 'Strays-insensitive Design Graph, form 2' (SDG2), as shown in fig.5.4.

Because this SFG has the same loop-structure as the graph of fig.5.3, the same remarks about the denominator of the transfer function can be made here.

As a result from the fact that signs of both $-pC_0$ and $-C_n$ are fixed in this graph, there is a restriction for the numerator of the transfer function that can be realized with this SDG2. Using Mason's rule it can be shown that the product of the realized transmission zeros is

$$\prod_{i=1}^{n} z_{zero\ i} = \frac{C_0}{C_0+C_n} \tag{5.4}$$

which yields:

$$0 \leq \prod_{i=1}^{n} z_{zero\ i} \leq 1 \tag{5.5}$$

The lower bound means that it is not possible to realize an odd number

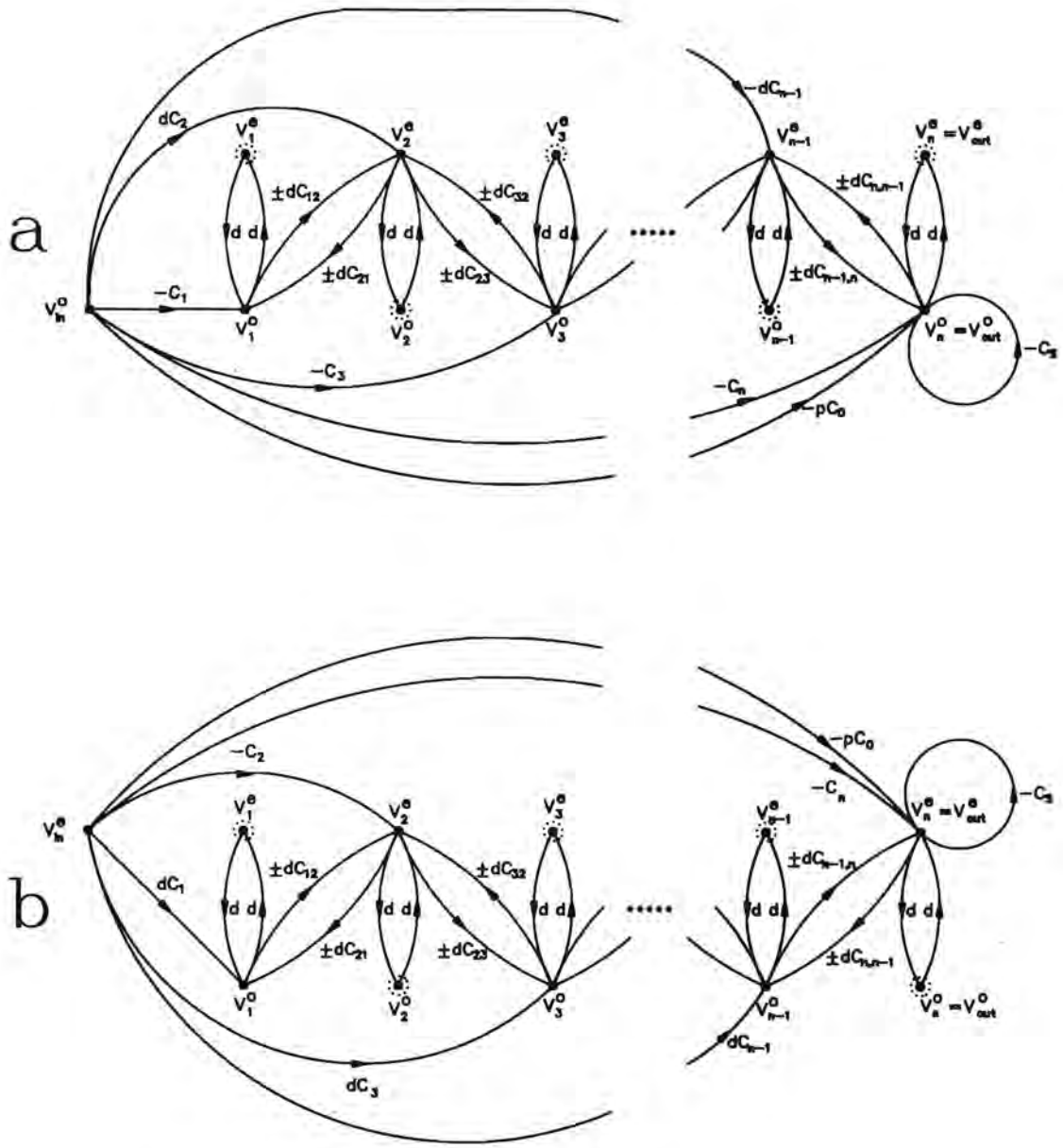


fig.5.4: Strays-insensitive Design Graph, form 2 (SDG2)

a: n odd

b: n even

of negative real zeros with this graph, except for the case that there is at least one zero at z = 0 (which means that $C_0 = 0$).
It should be clear that for transfer functions having less transmission zeros than poles, C_0 will automatically be zero and both of the above-mentioned limitations vanish.
In cases where the upper bound applies, the zeros outside the unit-circle can be transformed into the unit-circle by means of realizing their reciprocal values, provided that the phase-characteristic is unimportant.

5.2 DESIGN EXAMPLES.

As an example of the synthesis method of section 5.1 a third order filter will be designed, which approximates the fancy amplitude transfer function of fig.5.5 'as good as possible'.

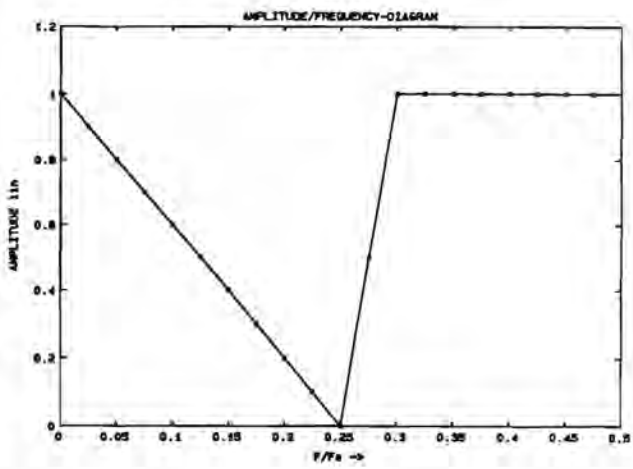


fig.5.5: Ideal amplitude transfer function.

Intentionally an amplitude transfer function was chosen here, for which it will be hard to find a ready available continuous-time prototype filter tabulated somewhere. In case of a synthesis method based on a continuous-time prototype one generally first has to

transform this amplitude transfer function to the continuous-time domain, using the inverse transform of that, on which the synthesis method is based. Then an appropriate continuous-time filter has to be searched for, which can then be transformed to the final SC filter circuit.

In our case the synthesis is completely carried out in the discrete-time domain. With a simple optimization program a third order discrete-time transfer function was calculated, that approximates the given characteristic of fig.5.5 in the least square sense on a set of frequencies $f = 0.025nf_s$, $n = 0,1,\ldots,20$, f_s being the sample frequency of the filter.

The obtained transfer function becomes:

$$H(d) = \frac{V_{out}}{V_{in}} = \frac{-1.529 + 0.984d^2 - 1.641d^4 + 0.749d^6}{-2.618 + 0.853d^2 - 0.678d^4 + d^6} \qquad (5.6)$$

$$(d = z^{-1/2})$$

and has the corresponding amplitude diagram drawn in fig.5.6.

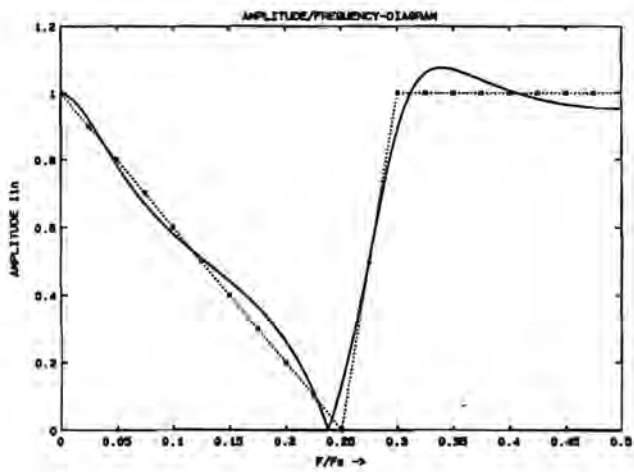


fig.5.6: Amplitude diagram for the transfer function of eq.(5.6).

Our SDG1 for the synthesis of third order filters, shown in fig.5.7,

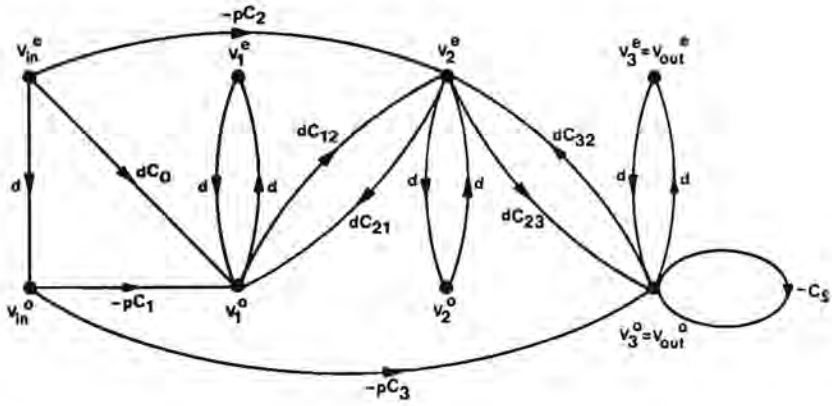


fig.5.7: SDG1 for third order filters.

corresponds with the transfer function:

$$H = d\,\frac{-C_3 - \frac{1}{p}C_2C_{23} + \frac{d^2}{p^2}(C_3C_{12}C_{21} - C_1C_{12}C_{23}) + \frac{d^2}{p^3}C_0C_{12}C_{23}}{1 + \frac{1}{p}C_s - \frac{d^2}{p^2}(C_{12}C_{21} - C_{23}C_{32}) - \frac{d^2}{p^3}C_sC_{12}C_{21}} \qquad (5.7)$$

Eq.(5.6) can be rewritten as

$$H = \frac{0.749 + \frac{1}{p}0.780 + \frac{d^2}{p^2}1.386 + \frac{d^2}{p^3}1.437}{1 + \frac{1}{p}1.618 + \frac{d^2}{p^2}3.940 + \frac{d^2}{p^3}1.443}. \qquad (5.8)$$

Comparing eq.(5.7) with (5.8) results in

$C_3 = -0.749$ $\quad C_2C_{23} = -0.780$ $\quad C_{12}C_{21}C_3 - C_1C_{12}C_{23} = 1.386$

$C_0C_{12}C_{23} = -1.437$ $\quad C_s = 1.618$ $\quad C_{12}C_{21} + C_{23}C_{32} = -3.940$

$C_sC_{12}C_{21} = -1.443$

Choosing $C_{12} = C_{23} = 1$ we obtain:

$C_0 = 1.437$ $C_1 = -0.718$ $C_2 = -0.780$ $C_3 = -0.749$ $C_s = 1.618$

$C_{12} = 1.000$ $C_{21} = -0.892$ $C_{23} = 1.000$ $C_{32} = -3.048$

The fact that C_1, C_2 and C_3 are negative means that we have to realize $-V_1$, $-V_2$ and $-V_3$ instead of V_1, V_2 and V_3.
Because we changed the sign of V_1 we also have to change the sign of C_0.

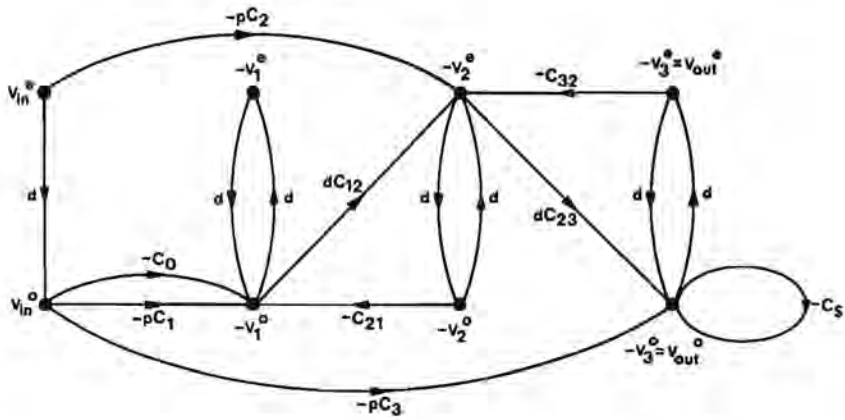


fig.5.8: Realizable SFG for the transfer function of eq.(5.6).

Now we have three negative capacitances: C_0, C_{21} and C_{32}. We can change their signs by means of realizing -dC as d*(-C), as was cleared up in fig.5.1.
This results in the SFG of fig.5.8.

The obtained SFG only consists from branches of the basic set and can therefore be transformed into a strays-insensitive SC circuit as depicted in fig.5.9, for which the number of switches has already been minimized using 'switch-sharing', as outlined before.

The reader will have noticed that the $-pC_1$ branch is not realized here using a 'mode 3' network (capacitor with series switch 'o'), but as an unswitched ('mode 6') capacitor. This is always allowed, wherever a

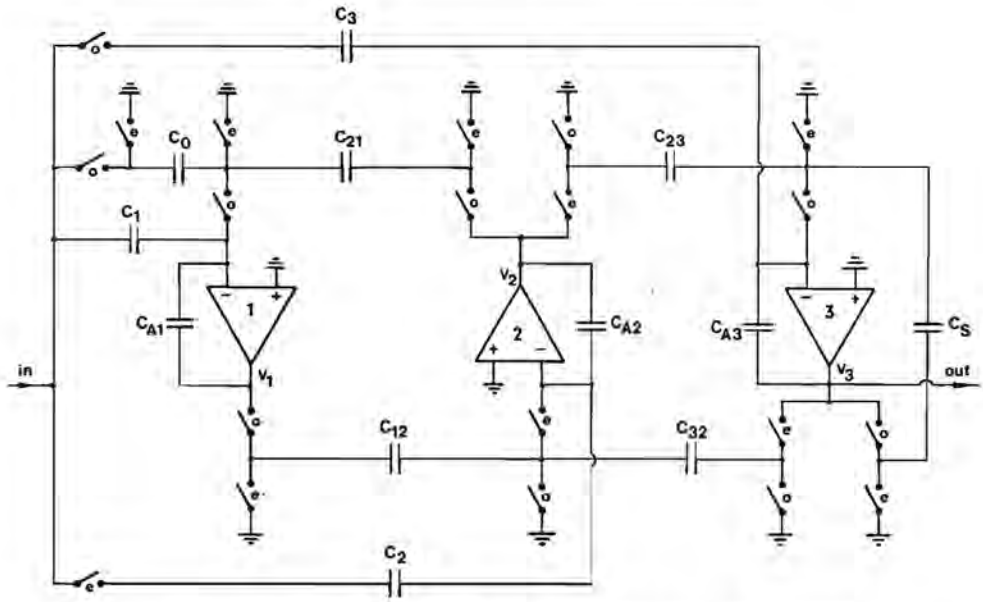


fig.5.9: Strays-insensitive SC filter, realizing the transfer function of eq.(5.6).

'type 3' branch in clock-phase 'o' (resp. 'e') ends on a 'type 4' d*d loop for which only the 'o' (resp. 'e') node has branches leaving it, as proved by the sequence of SFG's of fig.5.10.

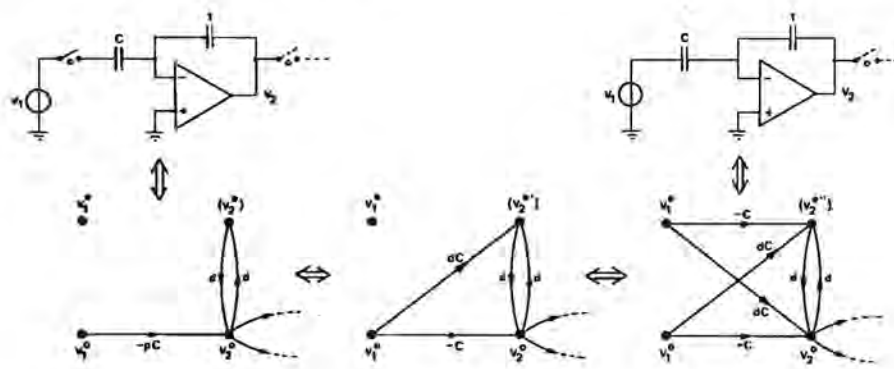


fig.5.10: Illustration of the redundancy of a switch 'o' in a 'mode 3' input network, when the corresponding opamp network is only sampled in clock-phase 'o'.

In the case of a capacitor with series switch 'o' (resp. 'e'), connected with a voltage node that changes only during phase 'o' (resp. 'e'), this switch is also redundant. In all other situations however, this series switch is essential and can not be omitted.

With capacitor values

$C_0 = 1.437$ $C_1 = 0.718$ $C_2 = 0.780$ $C_3 = 0.749$ $C_s = 1.618$

$C_{12} = 1.000$ $C_{21} = 0.892$ $C_{23} = 1.000$ $C_{32} = 3.048$

$C_{A1} = 1.000$ $C_{A2} = 1.000$ $C_{A3} = 1.000$

a SWITCAP [13] steady state simulation with a 1V input signal shows the following maxima at the various amplifier outputs:

$\max(V_1) = 3.035$ V for $f/f_s = 0$

$\max(V_2) = 2.399$ V for $f/f_s = 0.325$

$\max(V_3) = 1.075$ V for $f/f_s = 0.340$

In order to optimize the voltage swings of amplifiers 1 and 2 all capacitors connected with the output of amplifier 1 are scaled by a factor of $3.035/1.075 = 2.822$ (scaling of V_1^e and V_1^o) and all capacitors connected with the output of amplifier 2 by a factor of $2.399/1.075 = 2.231$ (scaling of V_2^e and V_2^o), such that $\max(V_1) = \max(V_2) = \max(V_3)$:

$C_0 = 1.437$ $C_1 = 0.718$ $C_2 = 0.780$ $C_3 = 0.749$ $C_s = 1.618$

$C_{12} = 2.882$ $C_{21} = 1.990$ $C_{23} = 2.231$ $C_{32} = 3.048$

$C_{A1} = 2.882$ $C_{A2} = 2.231$ $C_{A3} = 1.000$

Now all capacitors connected to each amplifier input are scaled for minimization of the total capacitance. All capacitors connected with the input of amplifier 1 are divided by 0.718 (scaling of ΔQ_1^e and ΔQ_1^o), those connected with the input of amplifier 2 by 0.780 (scaling of ΔQ_2^e and ΔQ_2^o) and those connected with the input of amplifier 3 by 0.749 (scaling of ΔQ_3^e and ΔQ_3^o), such that for every amplifier input the smallest capacitor connected with it is the unit capacitor (i.e.

the smallest available value):

C_0=2.001	C_1=1.000	C_2=1.000	C_3=1.000	C_s=2.160
C_{12}=3.618	C_{21}=2.772	C_{23}=2.979	C_{32}=3.908	
C_{A1}=3.930	C_{A2}=2.860	C_{A3}=1.335		

Another method that can often reduce the total capacitance and number of switches is what is called 'capacitor sharing' here. (This method was already applied in the notch biquad of fig.4.12.)
This method is based on the fact that a 'type 1' branch $-C_1$ and a 'type 2' branch dC_2 with $C_1 = C_2 = C$, leaving the same node, together can be replaced by one 'shared' 'mode 4' input network instead of the application of both a 'mode 1' and a 'mode 2' network (table 4.2), as illustrated in fig.5.11a.
The same kind of capacitor sharing can be done for a 'type 1' branch $-C_1$ and a 'type 2' branch dC_2 with $C_1 = C_2 = C$, ending on the same node that together can be realized by one 'shared' 'mode 5' input network, as illustrated in fig.5.11b.

The price that has to be payed for the application of the shared 'mode 4' network in fig.5.11a is the fact that one looses the possibility of scaling all capacitors connected with the input of amplifier 1 and scaling all capacitors connected with the input of amplifier 3 (for capacitance minimization) separately. In this case it is however easy to calculate whether the application of capacitor sharing is advantageous or not, as far as total capacitance is concerned.
By applying the shared 'mode 5' network one looses the possibility of scaling all capacitors connected with the output of amplifier 1 and scaling of all capacitors connected with the output of amplifier 3 (for optimization of the voltage swings at the outputs of these amplifiers) separately. In this case there will often be a trade-off between total capacitance and circuit complexity on the one side and dynamic range on the other.

In the SFG of fig.5.8 there are two candidates for 'capacitor sharing': the combination of the $-C_{32}$ branch with the dC_{12} branch and the combination of the dC_{23} branch with the $-C_s$ branch. For both pairs

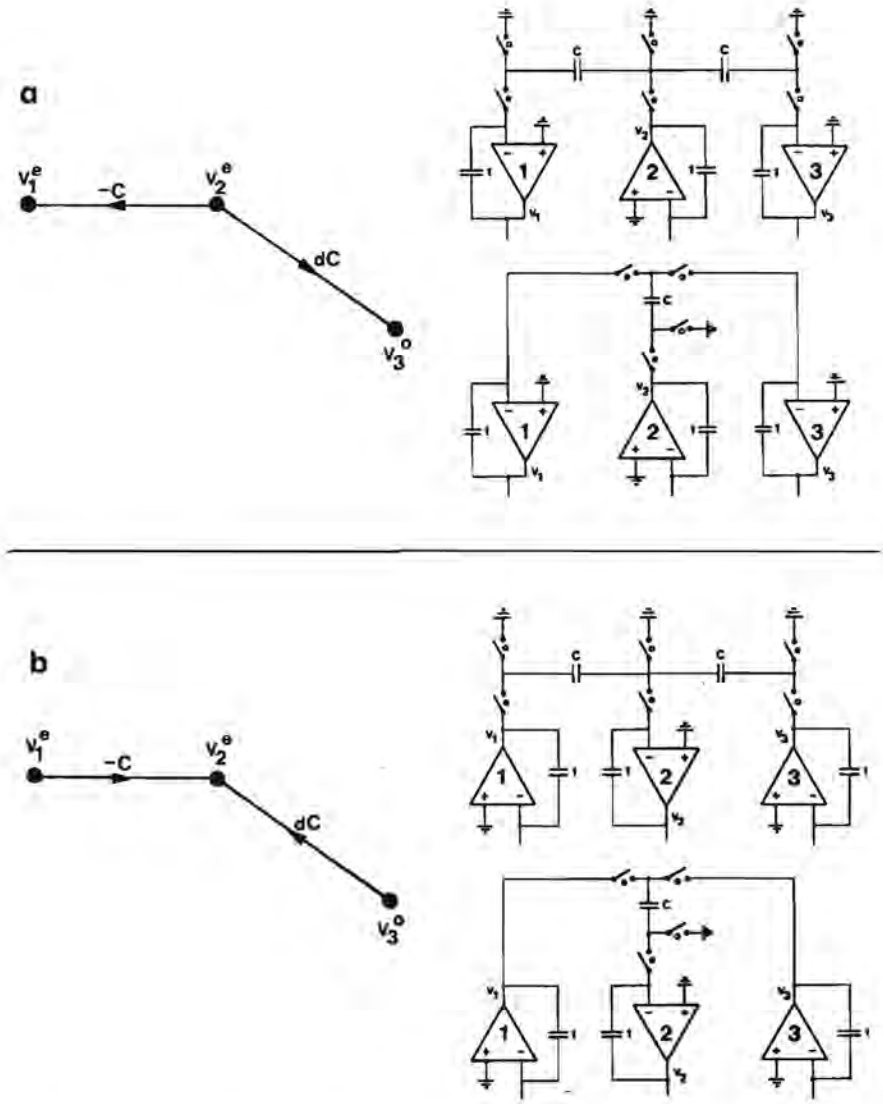


fig.5.11: Capacitor sharing a: for a 'type 1' and a 'type 2' branch leaving the same node,
b: for a 'type 1' and a 'type 2' branch ending on the same node.

a realization by means of a 'mode 4' input network is possible, as depicted in fig.5.12.

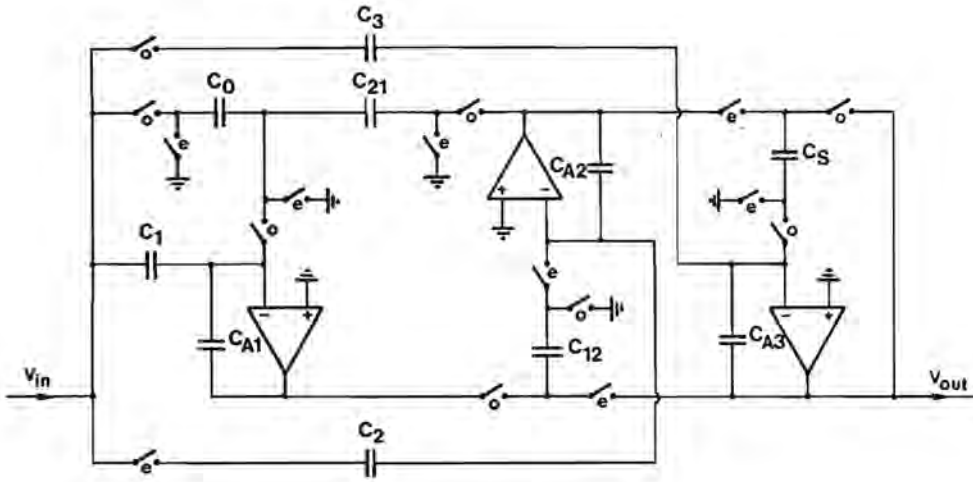


fig.5.12: Simplified version of the circuit of fig.5.9, obtained by the application of 'capacitor sharing' for capacitors C_{32} & C_{12} and C_{23} & C_s.

For this circuit the capacitances are:

$C_0 = 2.000$	$C_1 = 1.000$	$C_2 = 1.000$	$C_3 = 1.000$	$C_s = 2.160$
$C_{12} = 3.909$	$C_{21} = 2.008$	$C_{23} \rightarrow C_s$	$C_{32} \rightarrow C_{12}$	
$C_{A1} = 4.246$	$C_{A2} = 2.075$	$C_{A3} = 1.335$		

so the total capacitance is decreased from 28.563 to 20.733 (reduction of more than 27%) and the number of switches is reduced from 20 to 16. The price that was payed for this reduction is a small change in the maximum voltage swing at the amplifier outputs:

$\max(V_1) = 0.996$ V for $f/f_s = 0$

$\max(V_2) = 1.483$ V for $f/f_s = 0.325$

$\max(V_3) = 1.075$ V for $f/f_s = 0.340$

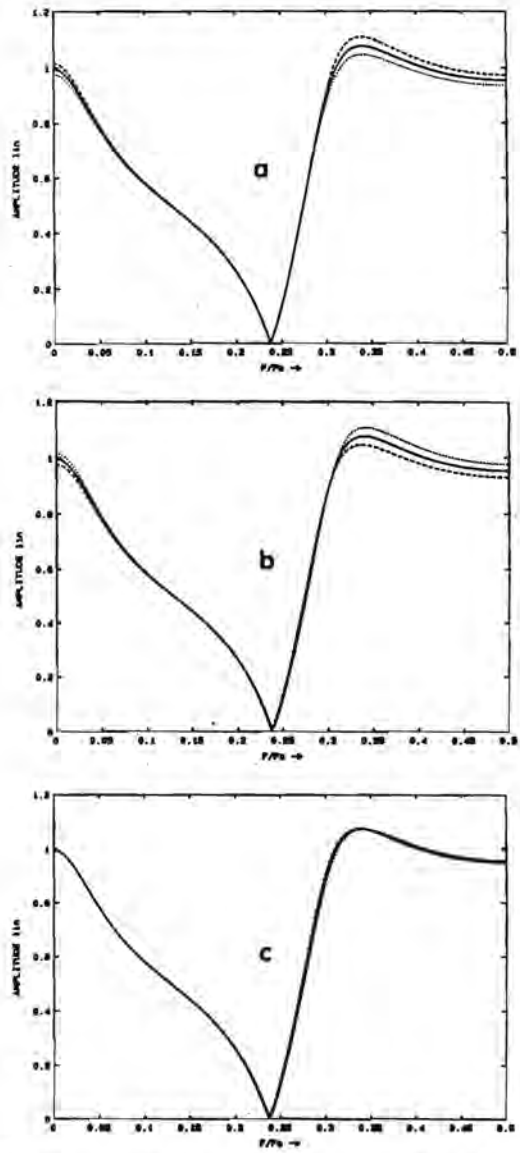


fig.5.13: Change of the amplitude transfer function for a ±2% variation of a: C_s (circuit of fig.5.9)

b: C_{23} (")

c: 'shared' C_s (circuit of fig.5.12)

——— : nominal value

..... : nominal value +2%

------- : nominal value -2%

The fact that the 'tracking' between two capacitors that are shared is implicitly guaranteed, often means a significant improvement of the sensitivity of the circuit for tolerances of these capacitances.
A very good example can be found in the 'sharing' of C_{23} with C_s in our circuit.
Fig.5.13 illustrates the change of the amplitude transfer function for a ±2% variation of C_s and C_{23} in the 'unshared' situation of fig.5.9 and for the same variation of C_s for the 'shared' situation of fig.5.12.
When two candidates C_i and C_j for 'capacitor sharing' have already about the same value, sharing is almost always advantageous, because in that case the loss of freedom of separately scaling for minimization of the total capacitance or optimization of the dynamic range is only a small drawback.
When, on the other hand, C_i and C_j have fairly different values, for instance $C_i \gg C_j$, then C_j can completely be shared and the remaining part $C_i - C_j$ has to be realized separately (this could be called 'partial capacitor sharing'). This can be done without sacrificing the freedom of separately scaling.
Only in cases where C_i and C_j differ too much for 'capacitor sharing', but their difference is smaller than the unit capacitance this 'partial capacitor sharing' will result in a small capacitance $|C_i - C_j| < 1$ and all capacitors connected with the same amplifier input as this small capacitor will have to be increased with a factor of $\frac{1}{|C_i - C_j|}$, which can be worse than the situation without sharing.

Using SDG2 as an alternative graph, other realizations for the transfer function of eq.(5.6) can be found.
As the loop-structure has not been modified, the denominator of the transfer function remains the same as in eq.(5.7). However, the branches from the input node to the amplifier output nodes have been changed, so the numerator has to be re-calculated:

$$H = \frac{-C_0 - \frac{1}{p} C_3 + \frac{d^2}{p^2}(C_2C_{23} + C_0C_{12}C_{21}) + \frac{d^2}{p^3}(C_3C_{12}C_{21} - C_1C_{12}C_{23})}{1 + \frac{1}{p} C_s - \frac{d^2}{p^2}(C_{12}C_{21} - C_{23}C_{32}) - \frac{d^2}{p^3} C_sC_{12}C_{21}} \qquad (5.9)$$

Comparing eq.(5.9) with (5.8) results in:

$C_0 = -0.749$ $C_1 = -0.741$ $C_2 = -0.718$ $C_3 = -0.780$ $C_s = 1.618$

$C_{12} = 1.000$ $C_{21} = -0.892$ $C_{23} = 1.000$ $C_{32} = -3.048$

Now using the familiar method, the signs of all capacitors are made positive, resulting in the SFG as drawn in fig.5.14, which can be transformed into the SC circuit of fig.5.15.

After optimization of the voltage swings at the amplifier outputs and minimization of the capacitors connected with each amplifier input, the following values for the capacitors are obtained:

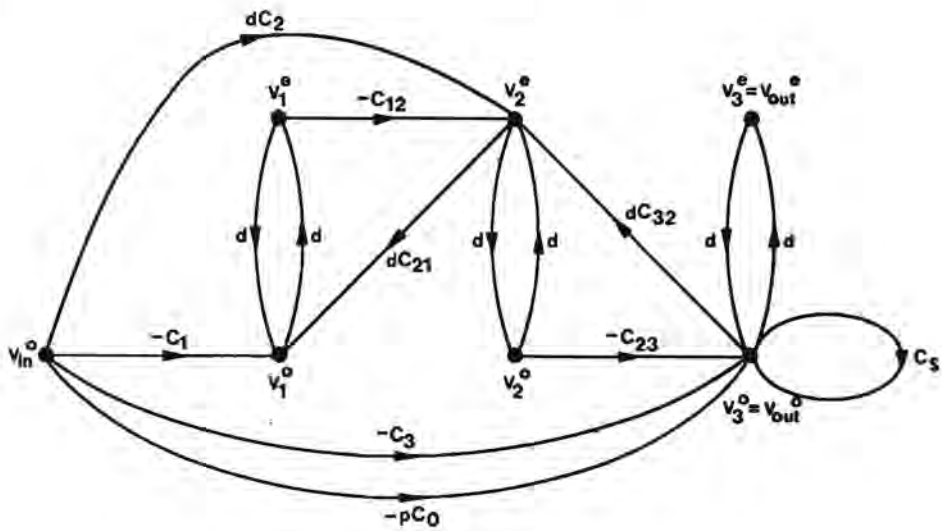


fig.5.14: Realizable SFG for the transfer function of eq.(5.6).

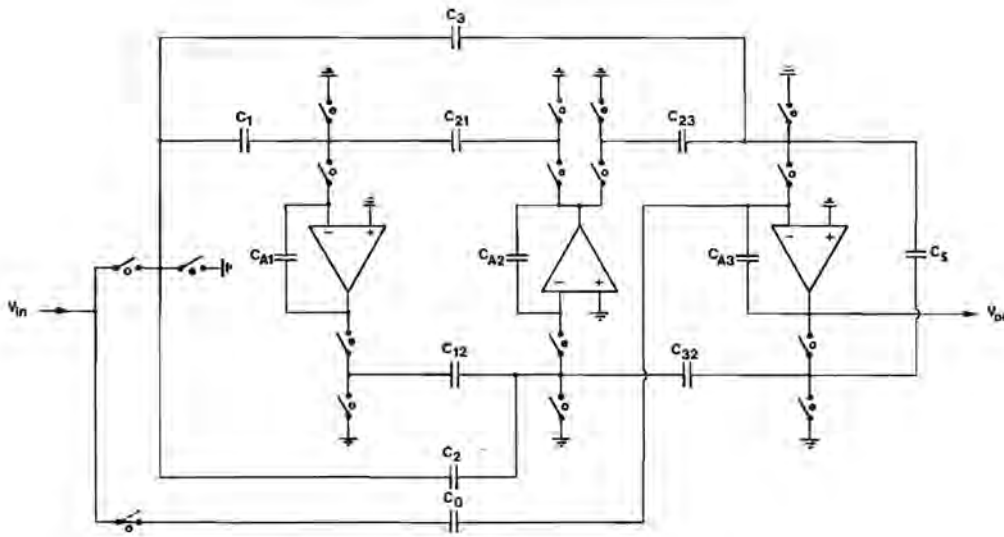


fig.5.15: SC realization of the SFG of fig.5.14.

$C_0 = 1.000$ $C_1 = 1.000$ $C_2 = 1.000$ $C_3 = 1.041$ $C_s = 2.160$

$C_{12} = 3.000$ $C_{21} = 2.994$ $C_{23} = 3.321$ $C_{32} = 4.245$

The total capacitance of 27.467 is comparable with that of the circuit of fig.5.9, which was 28.563.
The candidates for 'capacitor-sharing' in the circuit of fig.5.15 are:

1. C_1 & C_2
2. C_2 & C_3
3. C_1 & C_{21}
4. C_2 & C_{12}
5. C_{12} & C_{32}
6. C_s & C_{32}

When optimization of the voltage swings at the amplifier outputs is important, one can choose for a total sharing of C_1 & C_2 (both unit

capacitors) and partial sharing of C_{12}& C_{32} by means of sharing the common capacitance of 3.000 units with a separate realization of 1.245 units as a supplement for C_{32}. This results in saving 4 unit capacitors (reduction of 15%). The sensitivity for these shared capacitors can be shown to be improved with respect to the unshared situation. When the optimization of the voltage swings may be affected, further savings are possible.

5.3 MEASUREMENT OF A REALIZED SC FILTER DESIGN.

In order to verify the SDG synthesis method in practice, the circuit of fig.5.12 was actually realized, using CD4016 CMOS switches and LF356 operational amplifiers. The capacitors were sorted for a tolerance of less than 1%. The unit capacitance was chosen as 1 nF,

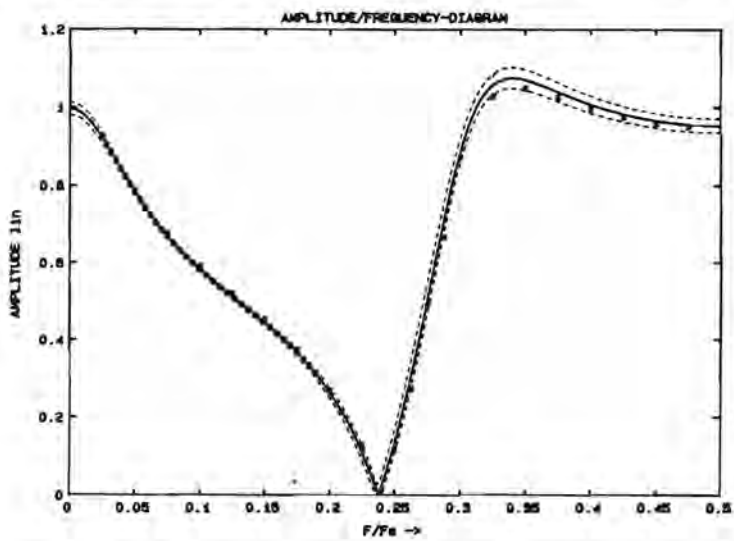


fig.5.16: Amplitude transfer function for the circuit of fig.5.12

x : measured data

——— : mean value } Monte Carlo simulation results for uncorrelated normal distributed errors with σ = 1% for each capacitor

-------- : mean value $\pm \sigma$ }

sample frequency f_s was 10 kHz. The data obtained by measurement of the amplitude transfer is depicted in fig.5.16, together with the results of a Monte Carlo simulation for uncorrelated, normal distributed errors with σ = 1% for each capacitor.

5.4 SENSITIVITY PROPERTIES OF SDG BASED SYNTHESIS.

Filter synthesis can be considered as a mapping of a transfer function onto a circuit structure. In practice the elements, with which this structure will be realized, are never ideal. Therefore it is important for every synthesis method to consider the sensitivity of the filter transfer to these non-idealities.
In this section we will focus on three sensitivity aspects:

- *sensitivity to capacitance deviations (section 5.4.1),*
- *sensitivity to amplifier gain (section 5.4.2),*
- *sensitivity to amplifier bandwidth (section 5.4.3).*

5.4.1 SENSITIVITY TO CAPACITANCE DEVIATIONS.

By mapping the transfer function onto a SC filter structure, its numerator and denominator coefficients are expressed in capacitances, that are actually realized by circuit capacitors. Deviations of these realized capacitances, due to production imperfections, temperature dependency etc. will affect the filter transfer.
The inaccuracy with which capacitors are realized in an MOS process are as bad as 10 to 20%, mainly caused by deviations of the thickness of the silicon dioxide dielectric layer. The reason why it is nevertheless possible to produce accurate MOS SC filters, is the fact that for these circuits the transfer is determined by capacitance ratios. In a good filter layout design, capacitors are composed of unit capacitors, which have a tracking inaccuracy in the order of magnitude of only 0.5%. In fact one of the main reasons for the popularity of SC filters is based on this accuracy property. On the other hand, it will be important to apply a synthesis, which carefully exploits this excellent property and does not spoil it, by generating

highly sensitive structures.
Besides desired capacitors, there are always many parasitic capacitances in a real-life SC circuit, as cleared up in chapter 2. In a strays-sensitive design these will considerably affect the filter transfer. As the SDG synthesis inherently generates strays-insensitive circuits, this will be of no concern to us.

In the adapted SFG analysis method, as presented in chapter 3, capacitance ratios are represented by branches in a graph. Using Mason's rule, the corresponding transfer function H(z), expressed in these ratios can easily be derived.
When we are interested in the sensitivity of this transfer for a specific capacitance ratio x, we can write H(z) as

$$H(z) = \frac{N(z)}{D(z)} = \frac{N_1(z) + xN_2(z)}{D_1(z) + xD_2(z)} \qquad (5.10)$$

with N_1, N_2, D_1 and D_2 being constants in x.
A measure for sensitivity is the relative sensitivity figure, defined as

$$S_x^H = -\frac{x}{H}\frac{\partial(H)}{\partial(x)}, \qquad (5.11)$$

assumed that $H \neq 0$. This represents the relative change of H due to a relative change of x. (For frequencies in the stopband one often uses half-relative or absolute sensitivity measures.)
Most often z is chosen as $z = e^{j\Omega}$, yielding a sensitivity measure for sinusoidal input signals.
Using this definition for eq.(5.10) results in

$$S_x^{H(z)} = \frac{xN_2(z)}{N_1(z) + xN_2(z)} - \frac{xD_2(z)}{D_1(z) + xD_2(z)} . \qquad (5.12)$$

As can be seen from eq.(5.12), H(z) can become highly sensitive to variations of x if

$$|xN_2(z)| \gg |N_1(z) + xN_2(z)| \qquad \text{or} \qquad (5.13a)$$

$$|xD_2(z)| \gg |D_2(z) + xD_2(z)| \qquad (5.13b)$$

This will be the case when location of poles or transmission zeros in the z-plane are determined by differences of large terms. Especially for poles close to the unit circle in the z-plane this situation should be avoided, because of the danger of instability.

In chapter 6, where SDG synthesis is being compared with a number of other approaches, its sensitivity to capacitance (ratio) variations turns out to be comparable or often better than for its competitors.

5.4.2 SENSITIVITY TO AMPLIFIER GAIN.

As was shown in chapter 3 and appendix B, finite amplifier gain can be represented by a deviation of the capacitors connected to it and virtual switched capacitors as an additional feedback. This deviation of the connected capacitors turned out to be inversely proportional to the amplifier gain. For a moderate gain, this effect will be small with respect to the above-mentioned 0.5% ratio inaccuracy of these capacitances. The virtual feedback switched capacitors are also inversely proportional to the amplifier gain and will cause a small damping, which will often be negligible in practical situations.
In cases where these finite gain effects can not be tolerated, one of the methods proposed in section 5.5 could be a solution.

5.4.3 SENSITIVITY TO AMPLIFIER BANDWIDTH.

A favorable property of the synthesis based on the SDG's of fig.5.3 and 5.4 is the fact that inherently a full decoupling of the amplifiers is achieved. It is well known that this is much of advantage for the sensitivity of the circuit to the gain-bandwidth products of its amplifiers, as will be briefly examined here.

Of the two second order SC circuits of fig.5.17 the one at the bottom is designed using the proposed SDG method, the one at the top using

another approach.

Except for a 180° phase shift, both circuits can be shown to have the same transfer functions in the ideal case:

$$H^{aa} = \pm \frac{z^{-1} C_{01} C_{12}}{(1 + C_{22}) - z^{-1}(2 + C_{22} - C_{12} C_{21}) + z^{-2}} \qquad (5.14)$$

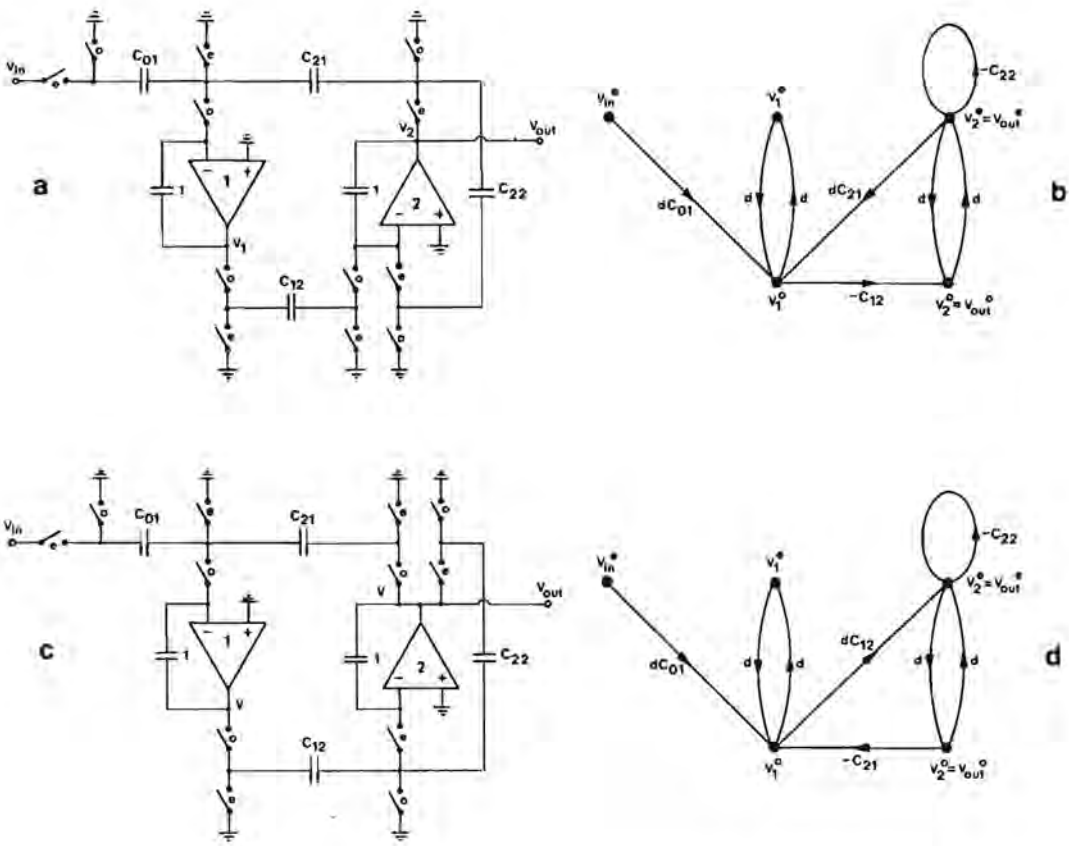


fig.5.17: Example circuits as an illustration of (de-)coupling of amplifiers

a: coupled circuit b: corresponding SFG

c: decoupled circuit d: corresponding SFG (=SDG)

When however the used amplifiers are modeled with one dominant pole, their frequency response differs significantly.
In both circuits of fig.5.17 amplifier 1 receives a step input at the beginning of clock-phase 'o'. Due to the finite GB-product its output will not produce a step but rather an exponential ramp (as shown in appendix A). In circuit (a) this exponential ramp is used as an input to amplifier 2. In circuit (c) however, this exponential ramp is sampled at the end of clock-phase 'o' by capacitor C_{12} and then used as a step input to amplifier 2 at the beginning of clock-phase 'e'.
In [30] and [31] a detailed analysis is given about this subject.
As an illustration both circuits of fig.5.17 were designed for a $Q = 10$, $f_o = f_s / 6$, a DC gain of 1 and $GB = 2.5\ f_s$.

SWITCAP simulation results shows a deviation of the amplitude diagram with respect to the ideal case for both circuits, as depicted in fig.5.18.

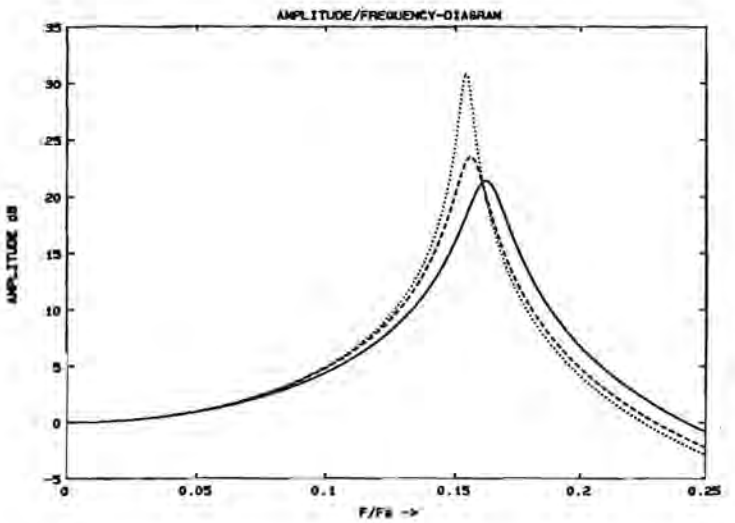


fig.5.18: Amplitude diagrams for the circuits of fig.5.17a and c.
——————— : GB = ∞ for both circuits
. . . . . : GB = 2.5 f_s 'coupled' form (fig.5.17a)
- - - - - - - - - - : GB = 2.5 f_s 'decoupled' form (fig.5.17c)

It should be clear that the coupled form of fig.5.17a (having a maximum transfer that is 9.4 dB higher at a frequency that is 5% lower than for the ideal case) is far more sensitive for the finite GB than the decoupled form of fig.5.17c (showing a maximum transfer that is 2.2 dB higher at a frequency that is 3.5% lower than for the ideal case).
In the simplified SFG representation of chapter 4, a circuit can easily be inspected for the presence of 'coupling', by checking every 'type 1' or '3' branch for the existence of a 'type 1', '2', or '3' branch ending on its tail.
Except for the self-loops $-C_a$, inspection of SDG1 and 2 shows no 'coupling'.

5.5 SC FILTER SYNTHESIS WITH FINITE GAIN AMPLIFIERS.

The synthesis method presented in section 5.1 was in principle based on the assumption that the operational amplifiers could be considered ideal. Although filters designed with the SDG method showed relatively low sensitivities to finite gain of the amplifiers, it is interesting to consider how to deal with amplifiers that have such a low gain that it significantly affects the filter behavior.

The first method that is discussed here is based on adding compensation networks, as proposed by Fischer and Moschytz [32].
The second method is the application of pre-distortion.

5.5.1 COMPENSATION NETWORKS FOR FINITE-GAIN AMPLIFIERS.

In chapter 3 and appendix B it is shown that effects due to the finite gain of the amplifiers can be represented in the SFG by adjusting the transfer of existing branches and adding new branches to the SFG of the ideal circuit.

For a basic building block for the SDG synthesis method, as depicted in fig.5.19a, this results in the SFG's of fig.5.19b and c.

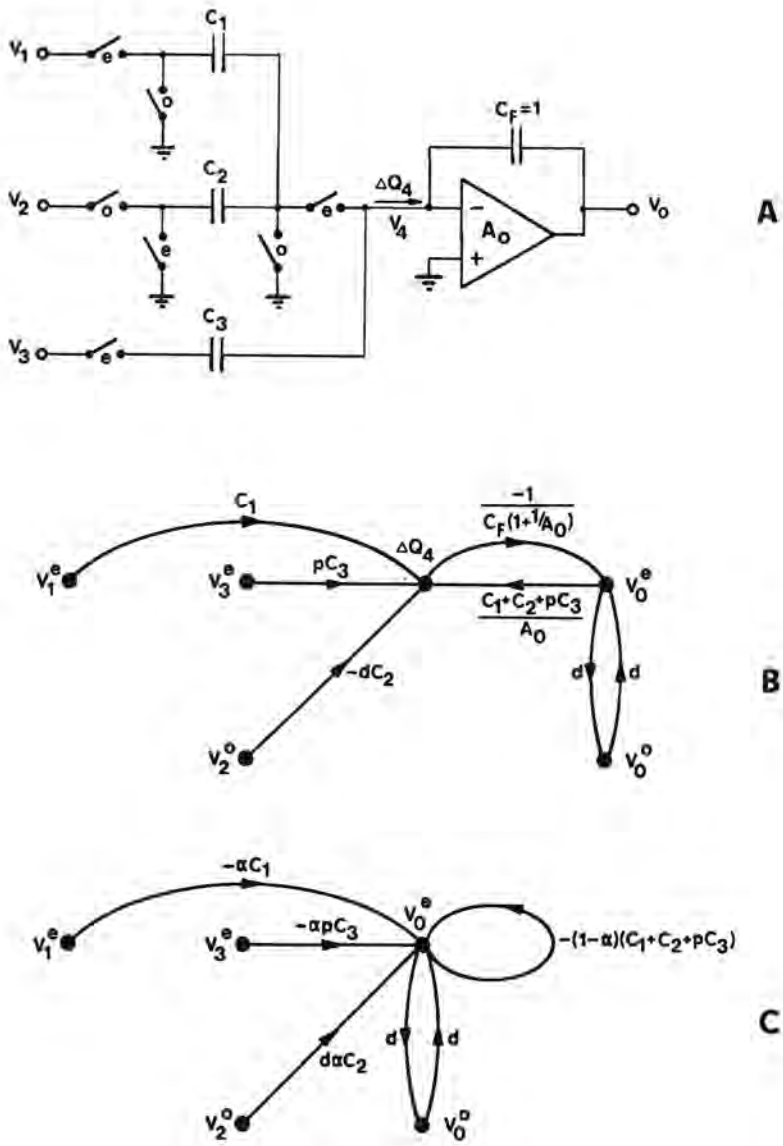


fig.5.19a: Basic building block for the synthesis method of chapter 3 with a finite-gain amplifier

b: corresponding SFG representation according to chapter 3

c: SFG representation with ΔQ node eliminated, $\alpha = \frac{A_o}{A_o+1}$.

The voltage V_o can be expressed in the voltages V_1, V_2 and V_3 as:

$$V_o^e = \alpha \frac{-C_1 V_1^e + dC_2 V_2^o - pC_3 V_3^e}{1 - d^2 + (1-\alpha)(C_1 + C_2 + pC_3)} \qquad (5.15a)$$

$$V_o^o = dV_o^e \qquad (5.15b)$$

In order to compensate for the finite-gain effects of the amplifier we will try to realize a counterbalance for the $(C_1+C_2+pC_3)/A_0$ branch in fig.5.19b, or similar for the $-(1-\alpha)(C_1+C_2+pC_3)$ self-loop in fig.5.19c. Because we need a transfer proportional to $1/A_0$ for this purpose it is obvious to use the voltage $V_4=-V_0/A_0$ at the inverting input of the amplifier. In order to prevent an undesired load, a unity-gain buffer is attached to this input. When the output of this buffer is connected to the switches of the input networks as depicted in fig.5.20a, this will result in the SFG's of fig.5.20b and c.

The voltage V_o can now be written as:

$$V_0^e = \alpha \frac{-C_1 V_1^e + dC_2 V_2^o - pC_3 V_3^e}{1 - d^2 + (1-\alpha)(pC_1 + pC_3)}$$

$$= \frac{\alpha}{1 + (1-\alpha)(C_1+C_3)} \cdot \frac{-C_1 V_1^e + dC_2 V_2^o - pC_3 V_3^e}{p} \qquad (5.16a)$$

$$V_0^o = dV_0^e \qquad (5.16b)$$

Note that no measures have to be taken to compensate for the pC_3 term. The total deviation with respect to the ideal case as it appeared in eq.(5.15) has been reduced to a magnitude error only.
If necessary this remaining magnitude error can also be (partly) compensated for, in this case by changing the circuit around the switched capacitors connected with the output of the finite-gain amplifier, as depicted in fig.5.21.

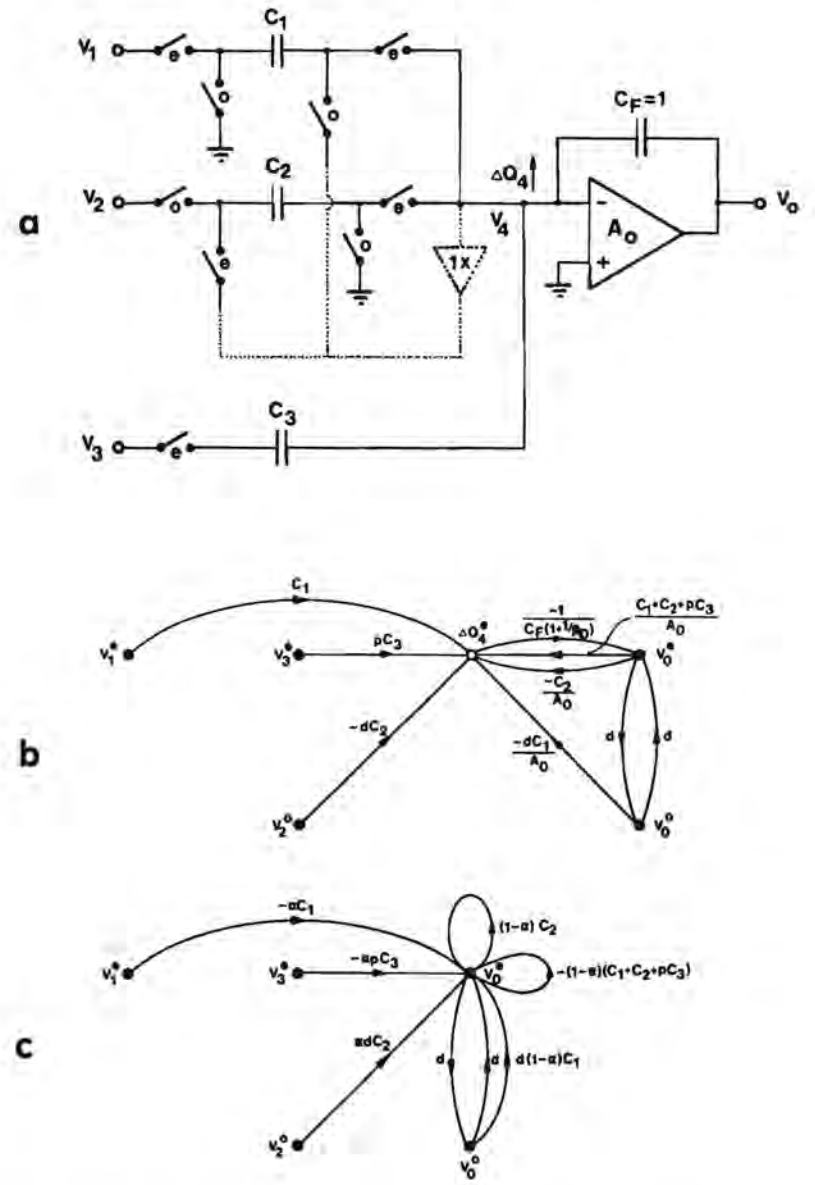
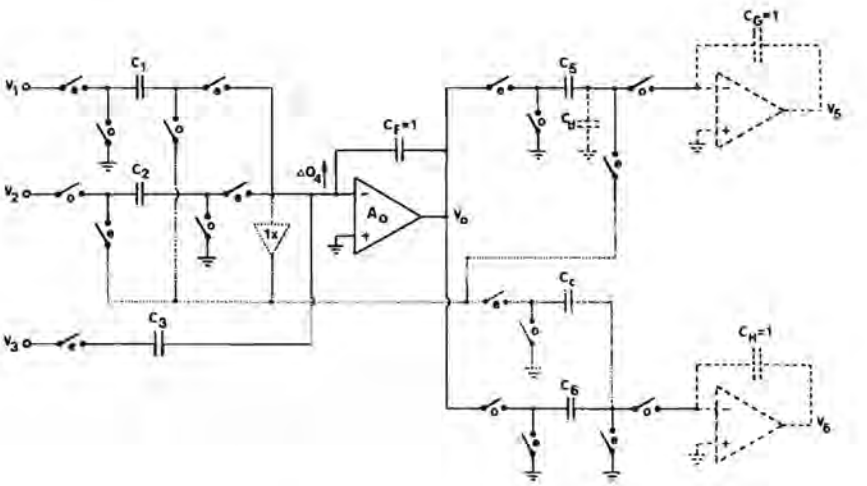


fig.5.20a: Circuit of fig.5.19a, extended with a compensation network

b: corresponding SFG representation

c: SFG representation with ΔQ node eliminated, $\alpha = \frac{A_o}{A_o+1}$.

a



b

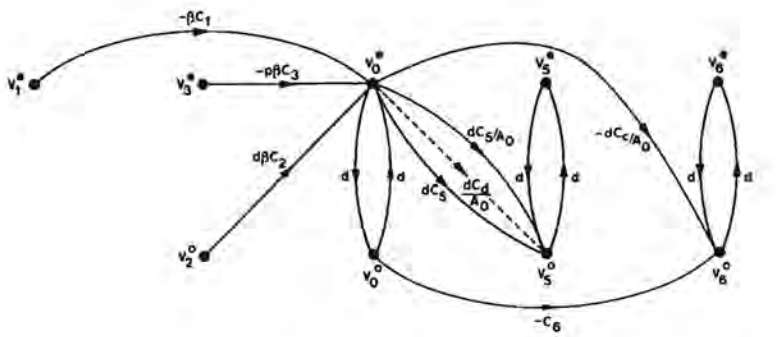


fig.5.21a: Circuit of fig.5.20a, extended with a compensation network for the remaining magnitude error

b: corresponding SFG representation, $\beta = \frac{\alpha}{1+(1-\alpha)(C_1+C_3)}$

When the compensation capacitor C_c is chosen such that

$$\beta\left(C_6 + \frac{C_c}{A_0}\right) = C_6$$

or equivalently

$$C_c = C_6\left(1 + \frac{C_1+C_3}{C_F}\right) \tag{5.17}$$

the transfer from V_1, V_2 and V_3 to V_6 is completely compensated for the finite gain of the considered amplifier.
In the original method, as presented by Fischer and Moschytz, capacitor C_d was not mentioned. The transfer to V_5 will in this case only partly be compensated for the finite amplifier gain.
When however capacitor C_d is added, such that

$$\beta\left(C_5 + \frac{C_5}{A_0} + \frac{C_d}{A_0}\right) = C_5$$

or equivalently

$$C_d = C_5\frac{C_1+C_3}{C_F} \tag{5.18}$$

then also the transfer from V_1, V_2 and V_3 to V_5 is completely compensated for the finite gain of the considered amplifier.

Note that the compensating network is not completely strays-insensitive, but as this affects only the compensation mechanism this is of little importance. Also possible deviations of the gain of the buffer have little influence.

In [32] some examples are shown of the improvements of the sensitivity of SC filters for the finite gain of the amplifiers due to the application of this compensation method. As it turns out, also the sensitivity for the finite bandwidth of the amplifiers is much reduced.

An advantage of this method is the fact that the compensation itself is automatic and does not have to be 'tuned' for the actual gain of the amplifiers. This means that this method will be relatively insensitive for parameter variations of the processing of the final integrated circuit.
On the other hand the increase of the complexity of the circuit is a drawback of this method.

5.5.2 A PRE-DISTORTION METHOD FOR FINITE-GAIN AMPLIFIERS.

Another approach, that can be applied when the designer has a reasonable close estimation of the non-idealities of the circuit elements he wants to compensate for, is that of pre-distortion.

This method can be compared with a procedure that is well-known for gunners. When they try to hit a certain object under stormy conditions, they point their cannon in fact beside the target, in such a manner that chances are optimal that they will actually hit it. When they miss, knowing how far they were beside the target, a correction is made and another attempt is done. This is repeated until they succeed.

In terms of filter design this means that the transfer function is distorted on purpose. This is done in such a way that the actual realized transfer of the filter that will be built with non-ideal components, is expected to approximate the desired transfer close enough.

As shown in appendix A, an analysis 'by hand' of a circuit with frequency dependant amplifiers is unfeasible, so in this case one is more or less forced to make use of a computer analysis program.
A simulation package which can cope with such finite amplifier bandwidth is the 'SWITCAP' [13] program.
Although this program is probably the most commonly used SC filter analysis program, it is also one of the most restricted in its kind. Simulation results are always numerical, no analytical analysis is available (in contrast with for instance 'SCYMBAL' [12], 'SCANAL' [10] and 'WATSCAD' [15]). Another way of computation of an appropriate pre-distortion by means of calculated sensitivities is also not possible with 'SWITCAP', because of the lack of output of sensitivity figures.

Therefore another method was used, that turned out to work very well in a practical feasible way. The method is iterative and is based on the following approach (fig.5.22).

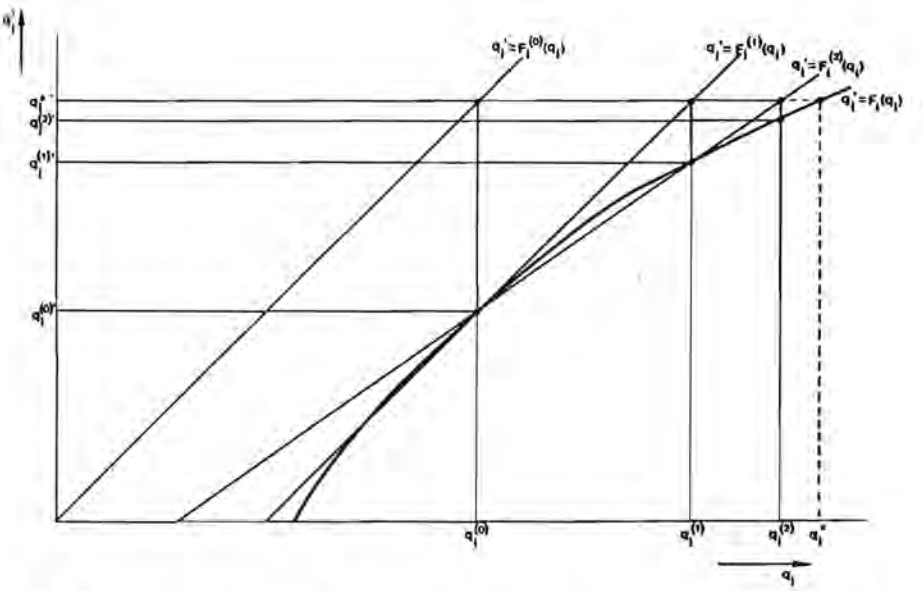


fig.5.22: Illustration for the iterative approach for finding q_i^* that will be mapped on $q_i^{*'}$ by an unknown function F_i.

A pole (or transmission zero) q_i of our 'target' transfer function will be mapped on a pole (or transmission zero) q_i' according to

$$q_i' = F_i(q_i) \quad , \text{ with } F_i: \mathbb{C} \rightarrow \mathbb{C}$$

after realization by a circuit with non-ideal elements.
Generally no analytical expression is available for this mapping. Knowledge about F_i can be gathered by means of subsequent simulation runs.
In the ideal case F_i maps q_i onto itself, but due to the non-idealities q_i' will be somewhat shifted with respect to q_i. The problem is to find the position of q_i^* that is mapped on the 'target' position $q_i^{*'}$.

In the beginning it is assumed that the mapping F_i is such, that $q_i = q_i'$. The initial guess for q_i^* will then be:

$$q_i^{(0)} = q_i^{*'} . \qquad (5.19a)$$

However, $F_i(q_i^{(0)}) = q_i^{(0)'}$ is generally not equal to the target position $q_i^{*'}$. Therefore the model is updated, such that it is assumed that $q_i^{(1)} = q_i^{(0)} + q_i^{*'} - q_i^{(0)'}$. The optimal choice for q_i^* will then be:

$$q_i^{(1)} = q_i^{(0)} + q_i^{*'} - q_i^{(0)'} \qquad (5.19b)$$

Again $F_i(q_i^{(1)}) = q^{(1)'}$ will generally not be equal to the target position $q_i^{*'}$.

The model can be updated as: $q_i = q_i^{(1)} + (q_i' - q_i^{(1)}) \dfrac{q_i^{(1)} - q_i^{(0)}}{q_i^{(1)'} - q_i^{(0)'}}$.

The optimal guess for q_i^* is now

$$q_i^{(2)} = q_i^{(1)} + (q_i^{*'} - q_i^{(1)}) \frac{q_i^{(1)} - q_i^{(0)}}{q_i^{(1)'} - q_i^{(0)'}} .$$

As $F_i(q_i^{(2)}) = q_i^{(2)'}$ instead of $q_i^{*'}$ the model can be updated further, etc.

In the k-th iteration cycle the optimal guess will be:

$$q_i^{(k)} = \sum_{i=0}^{k-1} \left\{ q_i^{(1)} \prod_{\substack{j=0 \\ j \neq i}}^{k-1} \frac{q_i^{*'} - q_i^{(j)'}}{q_i^{(1)'} - q_i^{(j)'}} \right\} \quad , \quad k = 2,3,4,\ldots \qquad (5.19c)$$

Note that this is in fact a Lagrange polynomial expansion of the inverse mapping F_i^{-1}.

Although convergence to the optimal pre-distorted transfer function is not assured, up to now practical applications of this method resulted always in useful pre-distorted transfer functions in only a few iteration cycles, as long as the non-idealities of the circuit elements were moderate.

Often, due to the good sensitivity properties of the SDG synthesis method, the 'target' transfer function was already approximated close

enough with the initial guess, so in these cases pre-distortion could be omitted.
If, on the other hand, the transfer would be seriously affected by the non-idealities, pre-distortion is not advisable. It should be realized that these non-idealities often are non-fixed and dependant on temperature, supply voltage, etc. In fact, pre-distortion is a 'feed-forward' approach. In this case possible further steps could be to improve the applied components (for example by re-designing the amplifiers), to use compensation circuits as outlined before or to apply a less sensitive filter strategy.

It should be mentioned here that the order of the realized transfer functions with non-ideal circuit-elements generally exceeds the order n of the 'target' transfer function. Nevertheless, for sufficiently small non-idealities again, the actual transfer can in general closely be approximated by an n-th order transfer function, obtained by a least squares fit.
As a further remark it can be stated that theoretically the pre-distortion of the several poles and transmission zeros can not be considered completely 'decoupled'. In none of the cases for which this pre-distortion method was applied, this 'coupling' seriously affected its convergence.

Although it sometimes seems to be a challenge to find the real optimal pre-distorted transfer function (at a price of several simulation runs), this is not really meaningful. One should always be aware of the fact that the magnitude of the non-idealities of the circuit-elements never are exactly known, and can even vary, as stated before.

As an example of this method the transfer function of eq.(5.6) will be approximated by a filter with amplifiers with an open-loop DC gain of only 100 and a unity-gain bandwidth of 5 times the switching frequency.

The 'target' transfer function is in this case:

$$H^{*'}(z) = \frac{-1.529 + 0.984z^{-1} - 1.641z^{-2} + 0.749z^{-3}}{-2.618 + 0.853z^{-1} - 0.678z^{-3} + z^{-3}}$$

with zeros:

$$n_{1,2}^{*'} = n_{1,2}^{(0)} = 0.999\ e^{\pm j2\pi*0.238} \qquad n_3^{*'} = n_3^{(0)} = 0.491$$

poles:

$$p_{1,2}^{*'} = p_{1,2}^{(0)} = 0.732\ e^{\pm j2\pi*0.293} \qquad p_3^{*'} = p_3^{(0)} = 0.714$$

and DC gain:

$$H^{*'}(z)\Big|_{z=1} = H^{(0)}(z)\Big|_{z=1} = 0.996$$

The capacitances are dimensioned for a filter (fig.5.12) with ideal circuit elements:

$C_0^{(0)} = 2.000$ $C_1^{(0)} = 1.000$ $C_2^{(0)} = 1.000$ $C_3^{(0)} = 1.000$ $C_S^{(0)} = 2.160$

$C_{12}^{(0)} = 3.909$ $C_{21}^{(0)} = 2.008$ $C_{A1}^{(0)} = 4.246$ $C_{A2}^{(0)} = 2.075$ $C_{A3}^{(0)} = 1.335$

A 'SWITCAP' analysis for the circuit with non-ideal amplifiers shows a transfer that can closely be approximated with a least squares fit by

$$H^{(0)'}(z) = \frac{-1.494 + 1.061z^{-1} - 1.645z^{-2} + 0.728z^{-3}}{-2.645 + 1.099z^{-1} - 0.850z^{-3} + z^{-3}}$$

with zeros:

$$n_{1,2}^{(0)'} = 0.997\ e^{\pm j2\pi*0.232} \qquad n_3^{(0)'} = 0.490$$

poles:

$$p_{1,2}^{(0)'} = 0.729\ e^{\pm j2\pi*0.282} \qquad p_3^{(0)'} = 0.711$$

and DC gain:

$$H^{(0)'}(z)\Big|_{z=1} = 0.967$$

The corresponding amplitude diagram is depicted in fig.5.23.
For the first iteration cycle the pre-distorted transfer function is calculated as:

$$H^{(1)}(z) = \frac{-1.552 + 0.899z^{-1} - 1.628z^{-2} + 0.767z^{-3}}{-2.570 + 0.612z^{-1} - 0.517z^{-3} + z^{-3}}$$

with zeros:

$$n_{1,2}^{(1)} = 1.003\ e^{\pm j2\pi*0.243} \qquad n_3^{(1)} = 0.491$$

poles:

$$p_{1,2}^{(1)} = 0.737\ e^{\pm j2\pi*0.303} \qquad p_3^{(1)} = 0.716$$

and DC gain:

$$H^{(1)}(z)\Big|_{z=1} = 1.028$$

The corresponding values for the capacitances are:

$$C_0^{(1)} = 2.052 \quad C_1^{(1)} = 1.000 \quad C_2^{(1)} = 1.000 \quad C_3^{(1)} = 1.000 \quad C_S^{(1)} = 2.047$$

$$C_{12}^{(1)} = 3.964 \quad C_{21}^{(1)} = 2.000 \quad C_{A1}^{(1)} = 4.220 \quad C_{A2}^{(1)} = 1.999 \quad C_{A3}^{(1)} = 1.304$$

Again a 'SWITCAP' analysis for the circuit with non-ideal amplifiers is made. This yields a transfer that can closely be approximated by

$$H^{(1)'}(z) = \frac{-1.512 + 0.983z^{-1} - 1.632z^{-2} + 0.743z^{-3}}{-2.593 + 0.872z^{-1} - 0.703z^{-3} + z^{-3}}$$

with zeros:

$$n_{1,2}^{(1)'} = 1.001\ e^{\pm j2\pi*0.237} \qquad n_3^{(1)'} = 0.491$$

poles:

$$p_{1,2}^{(1)'} = 0.735\ e^{\pm j2\pi*0.291} \qquad p_3^{(1)'} = 0.714$$

and DC gain:

$$H^{(1)'}(z)\Big|_{z=1} = 0.996$$

The corresponding amplitude diagram is depicted in fig.5.23.

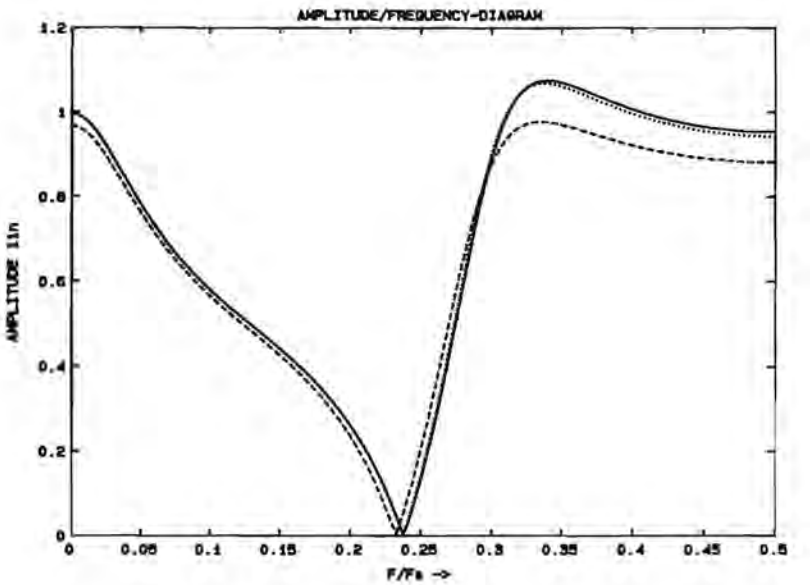


fig.5.23: Amplitude diagram

———— : for the ideal filter $|H^{*\prime}(e^{j2\pi f/f_s})|$

-------- : for the filter with non-ideal amplifiers without pre-distortion $|H^{(0)\prime}(e^{j2\pi f/f_s})|$

.... : for the filter with non-ideal amplifiers with pre-distortion $|H^{(1)\prime}(e^{j2\pi f/f_s})|$

As shown in fig.5.23 one iteration cycle is already sufficient in this case.

One should beware of the danger of exaggeration of pre-distortion. In cases where the non-idealities are fairly over-estimated, the situation with pre-distortion may be even worse than without.

6. COMPARISON WITH OTHER EXISTING SC FILTER SYNTHESIS METHODS.

In order to valuate the SDG approach, a comparison with a number of other synthesis methods will be made here.
First SC leapfrog synthesis, based on LC ladder simulation is considered in section 6.1.
Next, in section 6.2, synthesis based on the application of 2^{nd} order filter units ('biquads') will be regarded.
In section 6.3 the SDG method will be compared with a number of other SFG based methods.

6.1 SC FILTER SYNTHESIS BASED ON LEAPFROG LC LADDER SIMULATION.

The most popular class of synthesis methods for SC filters is based on the simulation of resistively terminated LC ladder filters. The main reason for this is the fact that these continuous-time ladder filters have inherently lower sensitivity in the passband to component variations than most other filter topologies [33]. The intention is to preserve this excellent sensitivity property by careful translation into a SC configuration.
Because of the popularity of this class of filters it seems useful to make a comparison between them and filters designed by the SDG method, proposed in chapter 5.

The most commonly adopted procedure for the ladder synthesis of SC filters is to start with a conventional LC ladder filter which satisfies the given specifications. This filter can be obtained from available filter tables, or be computed by special filter design packages. Then the well-known leapfrog technique is applied, resulting in a SFG, representing the relations between node-voltages and branch-currents of the reactive elements by vertices with transfer 1/s (ideal continuous-time integration). As a final step this SFG is transformed into an SC realization by the application of SC (discrete-time) integrators, most often the so called LDI-integrator of fig.6.1.

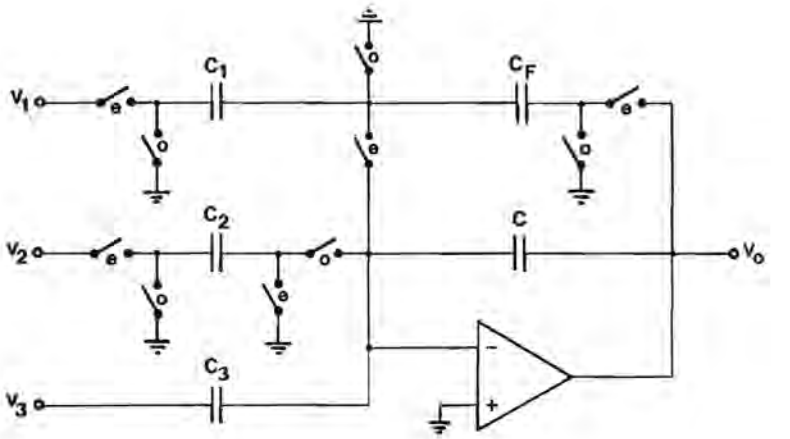


fig.6.1: LDI-integrator as a general building block for SC ladder filters.

The output voltage V_o^o of this circuit can be expressed in V_1^e, V_2^e and V_3^o and yields

$$V_o^o = \frac{- C_1 z^{1/2} V_1^e + C_2 z^{-1/2} V_2^e - 2\gamma C_3 V_3^o}{\gamma(2C + C_F) + \mu C_F} \qquad (6.1)$$

with $\gamma = (z^{1/2}-z^{-1/2})/2$, being the LDI (Lossless Discrete Integration) transformed Laplace operator s, and $\mu = (z^{1/2}+z^{-1/2})/2$ representing $\cos(\Omega/2)$ for $z = e^{j\Omega}$.

Note that because μ is frequency dependant, the damping of this integrator (necessary for the realization of the resistive terminations of the ladder filter) is frequency dependant too. This means that in fact the terminations r of the realized LC ladder filter will have a frequency dependant character r/μ, which affects the filter transfer, especially for signal frequencies in the neighborhood of the Nyquist rate.

When this is unacceptable an exact synthesis based on the application of the bilinear transform $\lambda = (z-1)/(z+1)$ is possible. By scaling all impedances of the reference filter in this λ-domain with a factor of $1/\mu$ and using the relations $\lambda = \gamma/\mu$ and $\mu^2 = 1+\gamma^2$ a filter is obtained with 'inductors' with impedance $\gamma\ell$, 'capacitors' with

admittance γc and 'resistors' with impedance r/μ. This is a bilinear λ-domain transformed filter, implemented as an LDI γ-domain filter, now with realizable frequency dependant terminating resistances r/μ.

As an example of this synthesis method a bilinear transformed Cauer filter will be derived.
As a reference the third-order lowpass ladder filter of fig.6.2 will be used.

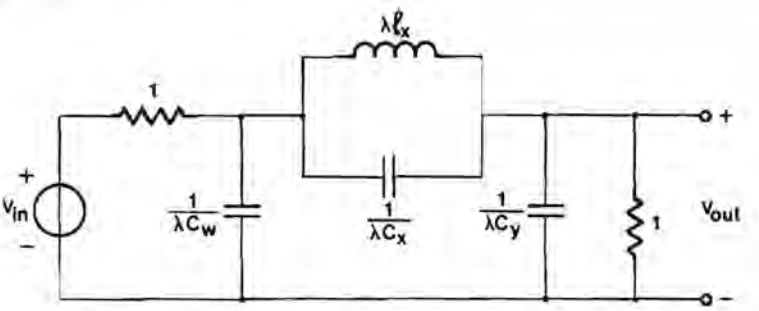


fig.6.2: Reference third-order lowpass ladder filter.

First all impedances are scaled by a factor of $1/\mu$, resulting in fig.6.3, with $c'_x = c_x + 1/\ell_x$.

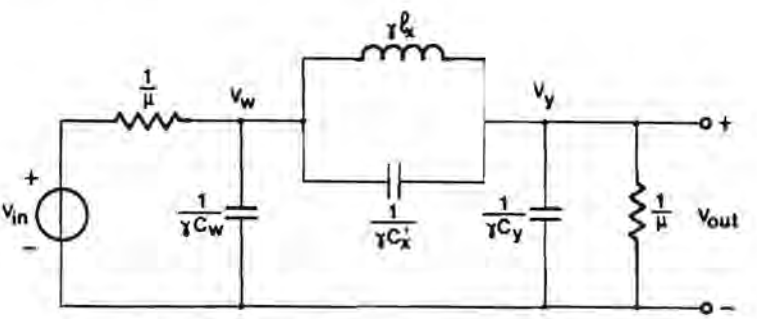


fig.6.3: Filter of fig.6.2 after scaling.

In order to make the leapfrog technique applicable c'_x has to be removed. This can be done by transforming the circuit of fig.6.3 into the equivalent form of fig.6.4, with $c'_w = c_w + c'_x$, $c'_y = c_y + c'_x$,

$\alpha_{yw} = c'_x/c'_w$, $\alpha_{wy} = c'_x/c'_y$.

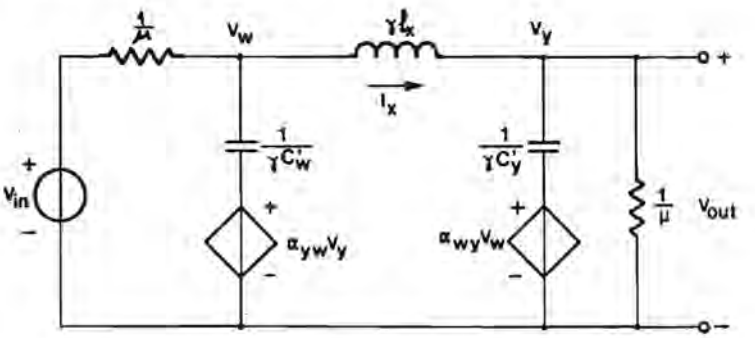


fig.6.4: Equivalent form for the filter of fig.6.2.

For this circuit the following relations between the node-voltages and branch-currents can be obtained:

$$V_w = \frac{-I_x + \alpha_{yw} c'_w \gamma V_y + \mu V_{IN}}{\gamma c'_w + \mu} \qquad (6.2a)$$

$$I_x = \frac{V_w - V_y}{\gamma \ell_x} \qquad (6.2b)$$

$$V_y = \frac{I_x + \alpha_{wy} c'_y \gamma V_w}{\gamma c'_y + \mu} \qquad (6.2c)$$

These relations can be rewritten as:

$$V_w = \frac{z^{-1/2}(-z^{1/2} I_x) + \mu V_{IN}}{\gamma c'_w + \mu} \qquad (6.3a)$$

$$(-z^{1/2} I_x) = \frac{z^{1/2} V_w - z^{1/2}(-V_y)}{\gamma \ell_x} \qquad (6.3b)$$

$$(-V_y) = \frac{z^{-1/2}(-z^{1/2}I_x)}{\gamma c'_y + \mu} \qquad (6.3c)$$

These relations are commonly represented by a SFG as depicted in fig.6.5, with $V_1 = V_w$, $V_2 = -z^{1/2}I_x$ and $V_3 = -V_y$.

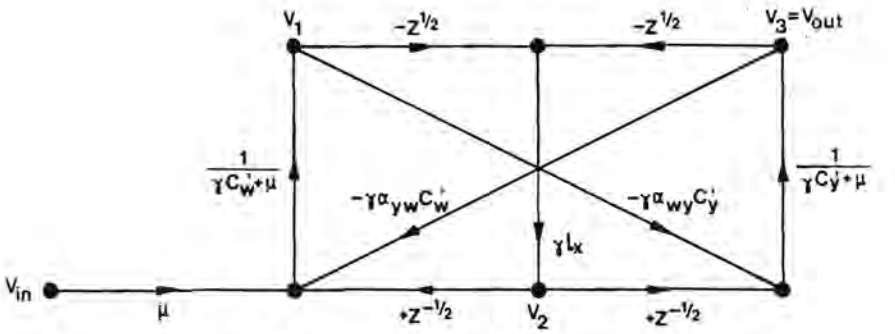


fig.6.5: A 'leapfrog' SFG representation for eq.(6.2a,b,c).

As can be seen, all three expressions (6.3a,b,c) can directly be realized by application of the circuit of fig.6.1, except for the μV_{IN} term in (6.3a). This μ branch represents in fact a transmission zero at z = -1, which is a result of the application of the bilinear transform for a continuous-time network having one transmission zero less than it has poles. This transmission zero can for example be realized with the strays-insensitive circuit of fig.6.6. [34], where it is assumed that $V^o_{IN} = z^{-1/2}V^e_{IN}$.

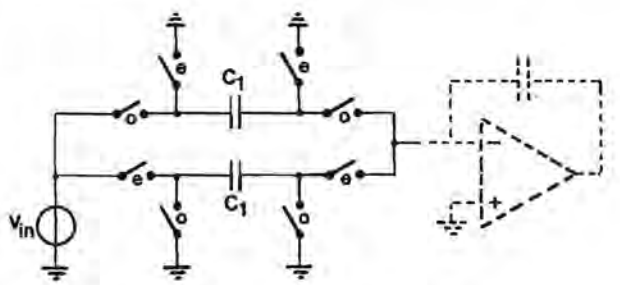


fig.6.6: Realization of a transmission zero at z = -1.

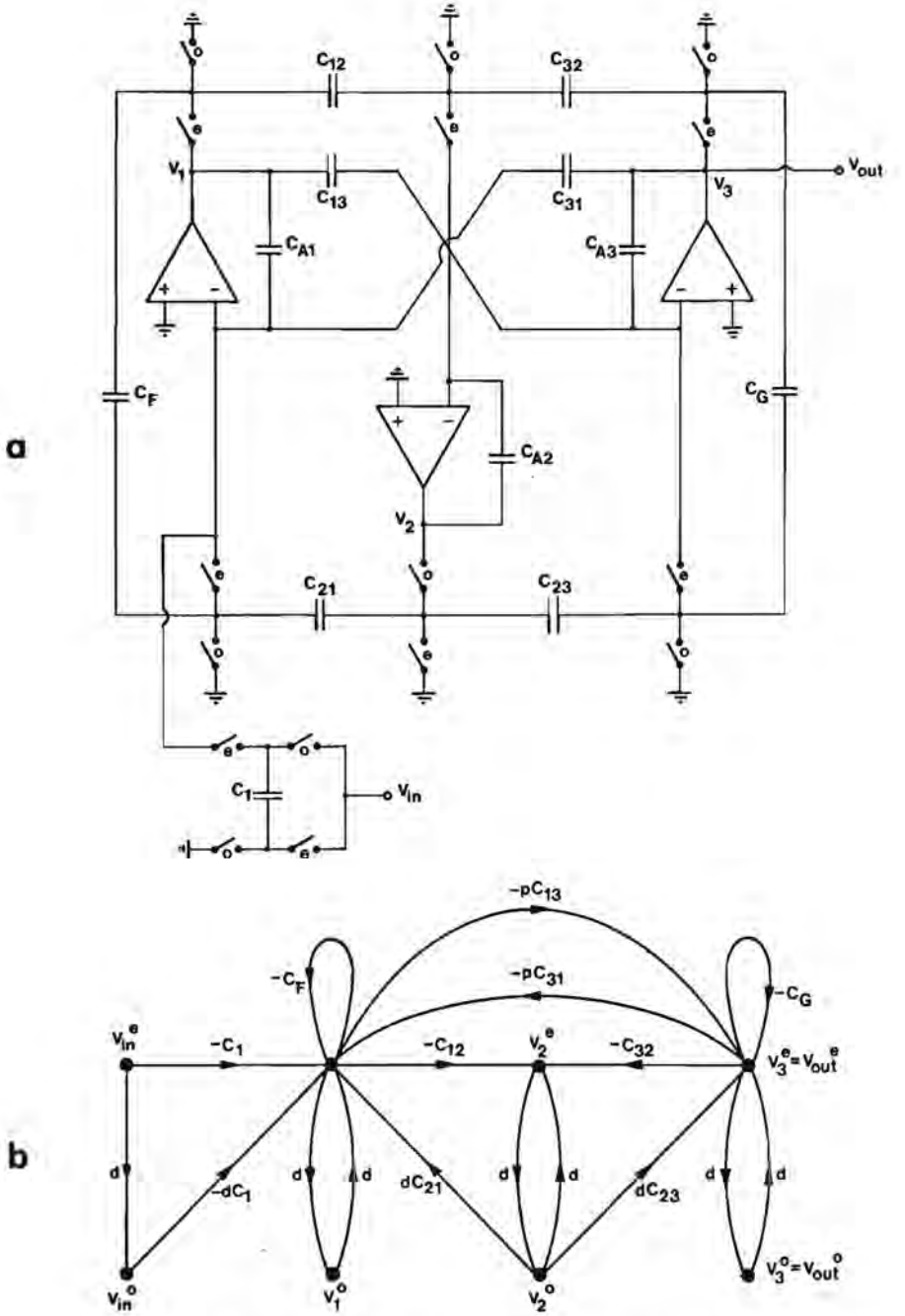


fig.6.7a: Bilinear transformed C 03 15 16 lowpass filter, cutoff angle $\omega_c T = \pi/5$, after [35].

b: Corresponding SFG.

In [35] a bilinear transformed Cauer lowpass filter (C 03 15 16, cutoff angle $\omega_c T = \pi/5$) has been designed, using the same approach as outlined above. The resulting circuit of fig.6.7 consists of three coupled LDI-integrators as depicted in fig.6.1.

After optimization of the dynamic range and minimization of the total capacitance the values for the capacitors for this circuit are:

$C_1 = 4.32$ $C_{12} = 1.47$ $C_{13} = 1.00$ $C_{21} = 6.98$ $C_{23} = 4.77$
$C_{31} = 1.00$ $C_{32} = 1.00$ $C_F = 6.36$ $C_G = 2.95$ $C_{A1} = 7.97$
$C_{A2} = 2.70$ $C_{A3} = 3.70$

Note that another realization of the transmission zero at $z = -1$ is applied here by means of the configuration around C_1. This realization has the advantage of not being based on the matching of two capacitors like the circuit of fig.6.6, therefore resulting in a good sensitivity for variations of this one capacitor. However, the disadvantage that this configuration is not strays-insensitive makes it of poor quality.

The transfer function of this circuit

$$H(d) = \frac{-0.1520 - 0.2416d^2 - 0.2416d^4 - 0.1520d^6}{-3.3092 + 5.3677d^2 - 3.8456d^4 + d^6}$$

can also be realized with the SDG approach, resulting in the SFG and circuit as drawn in fig.6.8.

After optimization of the dynamic range and minimization of the total capacitance the following values for the capacitors are obtained:

$C_0 = 2.303$ $C_1 = 1.000$ $C_2 = 1.000$ $C_3 = 1.000$ $C_a = 15.190$
$C_{12} = 4.999$ $C_{21} = 2.454$ $C_{23} = 16.182$ $C_{32} = 3.693$ $C_{A1} = 4.448$
$C_{A2} = 8.091$ $C_{A3} = 6.578$

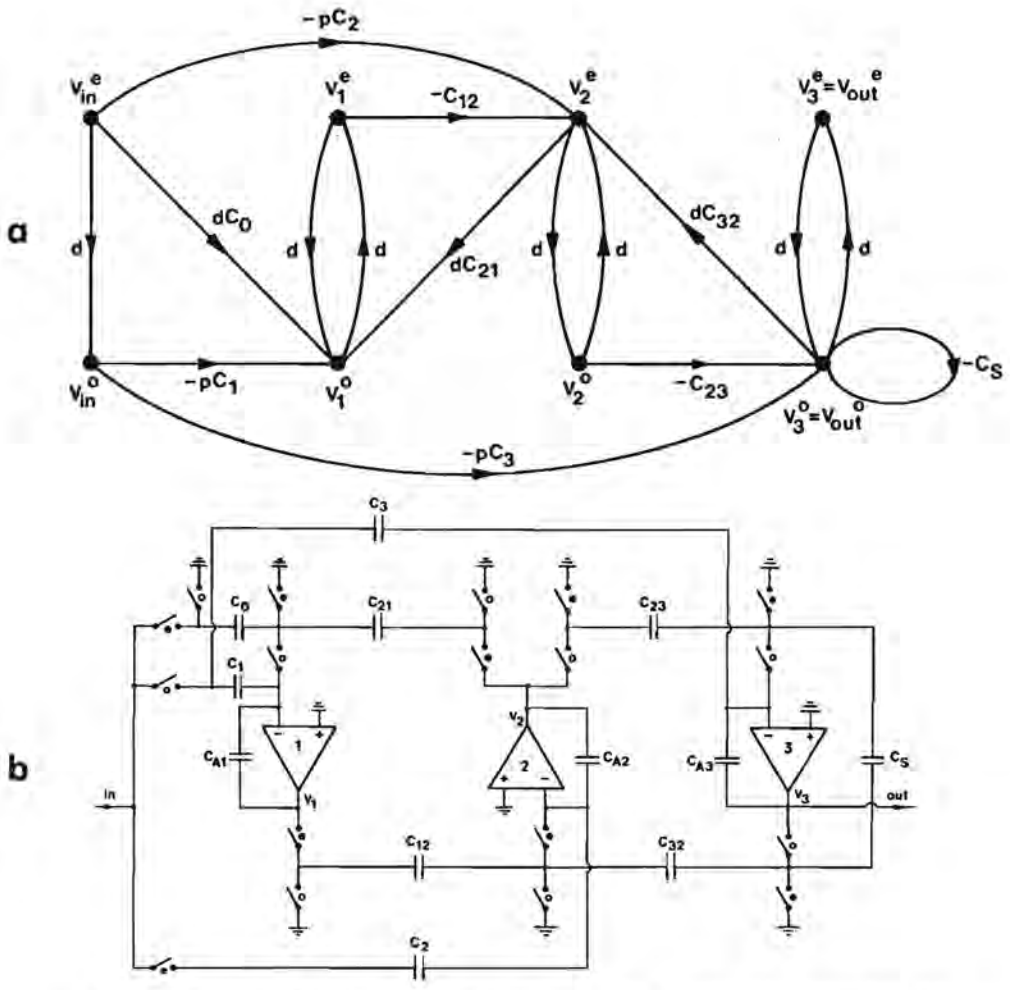


fig.6.8: Alternative realization of the same transfer function as for the circuit of fig.6.7 using SDG synthesis

a: SFG

b: corresponding realization.

Note that in this example the ladder implementation requires 33% less capacitance than the circuit obtained by SDG synthesis, but examples showing just the other way around could also be given.

A comparison of the sensitivities of both circuits to variations of

the capacitors values results in the diagrams of fig.6.9.

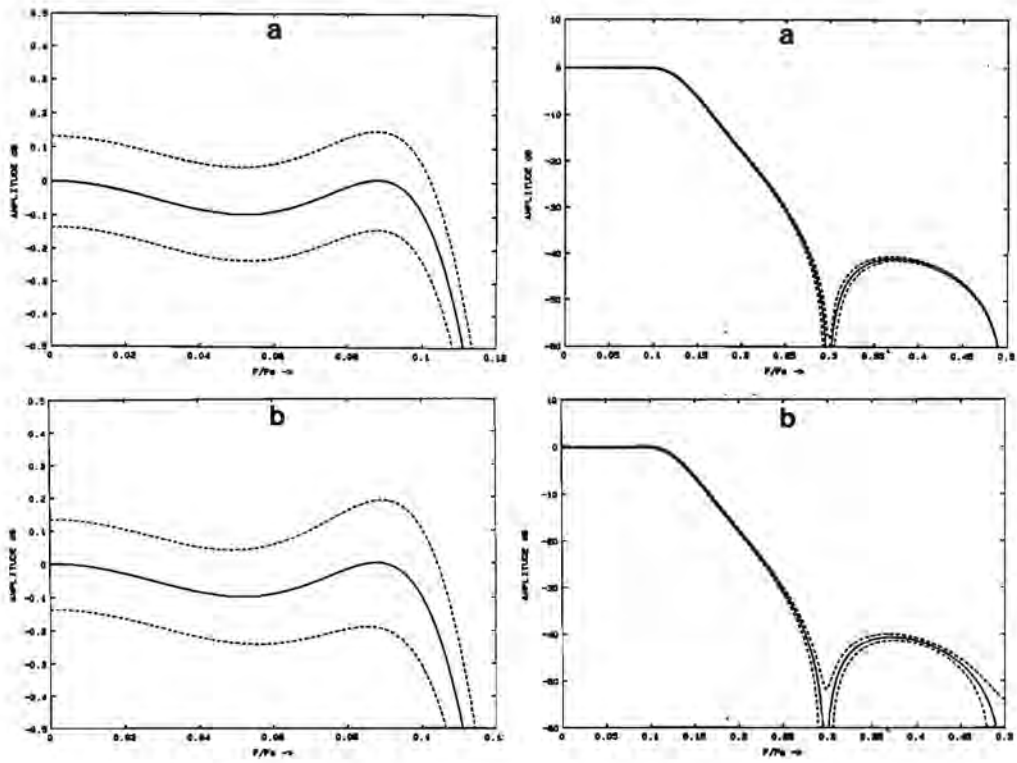


fig.6.9: Monte Carlo simulation results for uncorrelated normal distributed errors with σ = 1% for each capacitor

———— : mean value

---------- : mean value $\pm \sigma$

a: for the bilinear ladder circuit of fig.6.7

b: for the circuit of fig.6.8 based on the SDG approach.

Both circuits show good sensitivity properties.

In the vicinity of the transmission zeros the bilinear ladder filter shows a better sensitivity than the SDG circuit, but the minimum stopband losses are barely affected by this.

We should keep in mind that the transmission zero for $f = 0.5\ f_s$ in the bilinear ladder filter has been obtained using a strays-sensitive realization. When strays are considered the accuracy of the realization of this transmission zero is worse than for the SDG based

circuit. In case the strays-insensitive realization of fig.6.6 would have been applied, then the position of this transmission zero would no longer be fixed, but also be sensitive for capacitor variations.
The transmission zero for $f \approx 0.3\ f_s$ of the bilinear ladder filter has been derived from the parallel resonator branch in the LC ladder filter of fig.6.2, forcing it to be an 'infinite zero'. For the leapfrog realization of this branch we needed two VCVS'es in the equivalent circuit of fig.6.4, resulting in the loop, formed by C_{13}, C_{A3} with corresponding amplifier, C_{31} and C_{A1} with corresponding amplifier.
Note that in this way a delay free loop containing two amplifiers was created.
Such a loop on its own can be regarded as an active-C filter and its transfer and stability depends on the frequency responses of the amplifiers [36].
Even for the theoretical situation of ideal amplifiers these loops may lead to unstable circuits. For the circuit of fig.6.7 Eriksson [35] has shown that for cutoff angles $\omega_c T \geq 89.408^\circ$ the gain of this delay free loop exceeds 1. In practical situations, already at lower cutoff angles, these loops may cause unacceptable 'ringing' of the signal. Solutions for this phenomenon are given, but these are not strays-insensitive or increase the complexity of the circuit because of the need of additional sample-and-hold circuits.

Another interesting aspect is the sensitivity of the circuits for the amplifier gains.
Both circuits show practically the same small sensitivities for finite DC gains of the amplifiers.
When the sensitivity for finite gain-bandwidth products of the amplifiers are considered, both circuits show about the same small deviations at low signal frequencies, but at higher frequencies our circuit shows a better behavior than the bilinear ladder filter. An explanation can be found in a comparison of the SFG structures of both circuits. The bilinear ladder filter shows far more 'coupling', as described in chapter 5, than the SDG circuit. For highpass filters, but also for lowpass filters with higher cutoff angles this may be an important advantage of the SDG circuit.

A further advantage is the fact that the design is completely done in the discrete-time domain which is less cumbersome than a design that is partly done in the continuous-time domain. In the case of a design based on a continuous-time LC ladder reference filter, the desired specifications first have to be transformed to the continuous-time domain using the inverse transformation as applied for the transform of the filter back to the discrete-time domain. Then an appropriate LC ladder filter has to be found. When the designer has a filter design package at his disposal he may use it, if not, he will choose one out of several types (Butterworth, Chebychev, inverse Chebychev, Cauer, etc.) tabulated in a designer's handbook. Perhaps none of these standard filters meet the specifications. Furthermore if the designer makes use of filter tables, he will face the problem that a great majority of the standard filter tables are only given for lowpass filters, so in cases where another type of filter is needed he has to do a frequency transformation. When he finally has found an appropriate LC ladder filter he has to compose a corresponding leapfrog SFG which then can be transformed into a SC filter in the discrete-time domain.
In the case of SDG design, which is completely performed in the z-domain, a simple optimization program will do the job.

The classical design of analog allpass networks involves realizations having symmetrical lattice structures [37]. These can be transformed into ladder structures by using Bartlett's bisection theorem. However, as shown in [37], a first order allpass ladder filter has the same structure as the third order lowpass filter of fig.6.2, so its realization as a corresponding SC filter will need three amplifiers. A second order allpass ladder filter derived from a symmetrical allpass lattice network has the same structure as that of a bandpass filter of order six, as depicted in fig.6.10.

The complexity of the resulting SC structure makes this approach unattractive in comparison with the SDG based method.

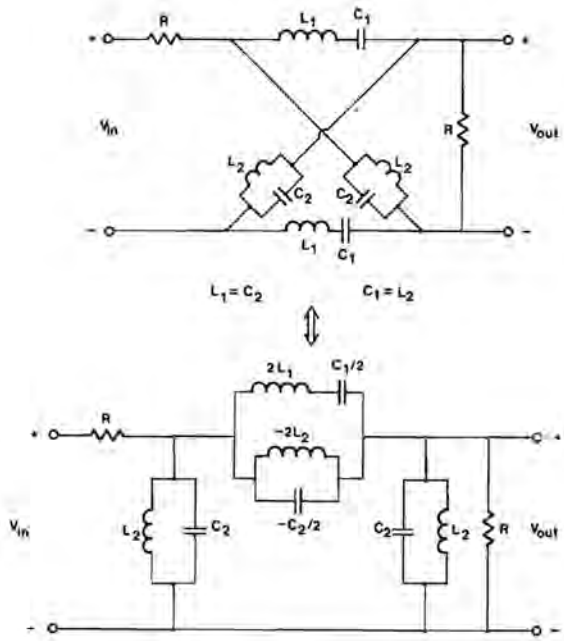


fig.6.10: Second order allpass ladder filter, derived from a symmetrical allpass lattice network [37].

6.2 SC FILTER SYNTHESIS BASED ON A BIQUADRATIC BUILDING-BLOCK APPROACH

This second existing design methodology that will be considered here is in fact a whole 'family' of synthesis methods.
The mostly known member of this family is of course the biquad cascade (extended with a first order building block or a triquad if the transfer function that has to be realized is of odd order). Furthermore multiple-loop feedback [46] (and feedforward) structures with biquadratic cells, such as '(generalized) follow-the-leader feedback' [38, 39], 'primary-resonator block', 'shifted companion' [40], '(modified) leapfrog' [41 - 45], 'inverse follow-the-leader feedback' and 'minimum sensitivity feedback' can be mentioned here. Some of these are very closely related to each other and all are well-known from active-RC filter synthesis. A detailed discussion of these structures is not in the scope of this thesis.

In fact these biquad-based design methodologies are not considered as competitors for the SDG synthesis method, but more as a class of filters to which we can contribute in adding new biquadratic cells that can serve as building blocks.

Because of the importance of this group of filter structures, much effort has been invested by a great number of people in finding new biquadratic cells [29,36,47-54]. A very extensive search has been made by Bermudez and Bhattacharyya [55] for parasitic insensitive SC biquads. This search was however not exhaustive because it was based on the assumption that the input-signal was fixed over a full clock period. This is also the case for the output of those biquads, so these structures are 'self-compatible'. Furthermore as a starting point for their work the unextended Hasler constraints were used, so the application of the important 'floating' nodes, as in this thesis, has been omitted. A contribution in this field could be made by using the method that was already suggested in chapter 4, generating a SFG with two 'type 4' d*d loops and all 32 input network branches ('type 1, 2 and 3'), calculating the input to output transfer of the graph and removing all possible combinations of superfluous branches again. This has not yet been carried out. Nevertheless we can add new biquadratic cells to the library of [55], by using the SDG approach, as depicted in fig.6.11.
The SFG of fig.6.11a results in transfer functions:

$$H^{ee} = \frac{V^e_{out}}{V^e_{in}} = -\frac{C_2 - d^2(2C_2+K_0K_{12}-C_1K_{12}) + d^4(C_2-C_1K_{12})}{(1+C_s) - d^2(2+C_s+K_{12}K_{21}) + d^4} \qquad (6.4a)$$

$$H^{oo} = \frac{V^o_{out}}{V^e_{in}} = dH^{ee}, \quad H^{oe} = \frac{V^e_{out}}{V^o_{in}} = d^{-1}H^{ee} \quad \text{and} \quad H^{oo} = \frac{V^o_{out}}{V^o_{in}} = H^{ee}$$

with $K_0 = \pm C_0$, $K_{12} = \pm C_{12}$ and $K_{21} = \pm C_{21}$,

and the SFG of fig.6.11b in

$$H^{ee} = \frac{V^e_{out}}{V^e_{in}} = -\frac{(C_0+C_2) - d^2(2C_0+C_2-C_1K_{12}) + d^4C_0}{(1+C_s) - d^2(2+C_s+K_{12}K_{21}) + d^4} \qquad (6.4b)$$

$$H^{eo} = \frac{V^o_{out}}{V^e_{in}} = dH^{ee}$$

with $K_{12} = \pm C_{12}$ and $K_{21} = \pm C_{21}$.

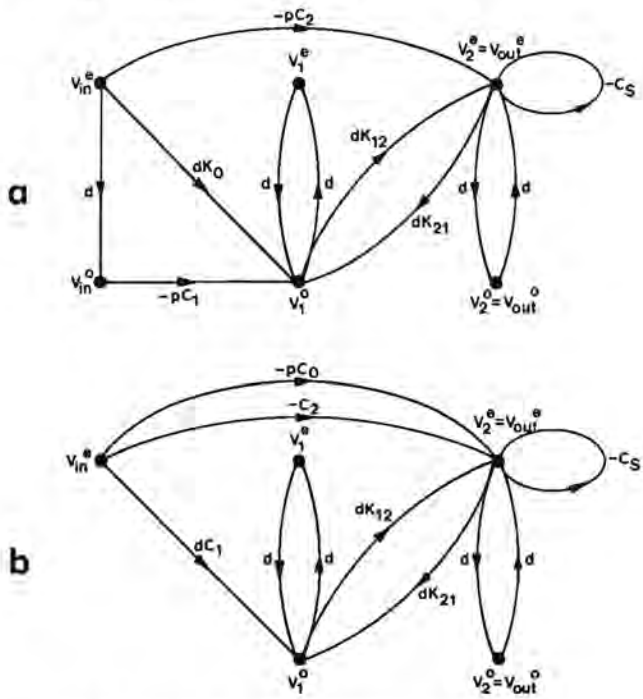


fig.6.11: SFG's for biquadratic cells
a: obtained by the application of SDG1,
b: obtained by the application of SDG2.

In order to realize complex pole-pairs, the product $K_{12}K_{21}$ has to be negative for both graphs. This results in two possible configurations for each of them. Furthermore for the cases where $K_{12} = +C_{12}$, there is no input network branch starting on the V_1^e node. Therefore other input

branches are allowed to end on it, without conflicting with the application of the sign inverting structure. With all possible input branch combinations, this results in 12 different circuits. When furthermore all possibilities for 'capacitor-sharing' are taken into account this results in another 24 circuits.

For $C_s>0$ the complex pole-pair is always situated within the unit circle in the z-plane, resulting in inherently stable biquads, with good sensitivity properties for their denominator coefficients.

In many applications, for instance for leapfrog coupled biquads, poles that are located on the unit-circle are needed. This is automatically obtained by taking $C_s = 0$.

Also transmission zeros that are located on the unit-circle are often needed. These can be realized by omitting C_1 for all biquads derived from the SFG of fig.6.11a or by leaving C_2 out for the biquads obtained from the SFG of fig.6.11b. This is done without the need of (sensitive) cancellation by means of matching of capacitances.

When both transfer functions 6.4a and 6.4b are transformed to the s-domain using the bilinear transformation, this results in:

$$H(s) = A \frac{s^2 + \frac{s\omega_n}{Q_n} + \omega_n^2}{s^2 + \frac{s\omega_p}{Q_p} + \omega_p^2}$$

This yields the following good relative sensitivities for variations in the capacitances.

A. For both denominators of eq.6.4a and b:

$$S^{\omega_p T}_{C_{12}} = S^{\omega_p T}_{C_{21}} = \frac{1}{2}\left[1 + (\omega_p T/2)^2\right]$$

$$S^{\omega_p T}_{C_s} = -\frac{1}{2}\frac{\omega_p T/2}{Q_p}$$

$$S^{Q_p}_{C_{12}} = S^{Q_p}_{C_{21}} = \frac{1}{2}\left[1 - (\omega_p T/2)^2\right]$$

$$S^{Q_p}_{C_s} = -1 + \frac{1}{2}\frac{\omega_p T/2}{Q_p}$$

B. For the numerator of eq.(6.4a):

$$S^{\omega_n T}_{C_0} = \mp \frac{1}{2}\left[1 + (\omega_n T/2)^2\right] \qquad \text{for } K_0 = \pm C_0$$

$$S^{\omega_n T}_{C_1} = \frac{1}{2}\frac{\omega_n T/2}{Q_n}$$

$$S^{\omega_n T}_{C_2} = \frac{1}{2}\left[1 + (\omega_n T/2)^2 - \frac{\omega_n T/2}{Q_n}\right]$$

$$S^{\omega_n T}_{C_{12}} = \mp \frac{1}{2}\left[1 + (\omega_n T/2)^2 - \frac{\omega_n T/2}{Q_n}\right] \qquad \text{for } K_{12} = \pm C_{12}$$

$$S^{Q_n}_{C_0} = \pm \frac{1}{2}\left[1 - (\omega_n T/2)^2\right] \qquad \text{for } K_0 = \pm C_0$$

$$S^{Q_n}_{C_1} = -1 + \frac{1}{2}\frac{\omega_n T/2}{Q_n}$$

$$S^{Q_n}_{C_2} = \frac{1}{2}\left[1 + (\omega_n T/2)^2 - \frac{\omega_n T/2}{Q_n}\right]$$

$$S^{Q_n}_{C_{12}} = \mp \frac{1}{2}\left[1 + (\omega_n T/2)^2 - \frac{\omega_n T/2}{Q_n}\right] \qquad \text{for } K_{12} = \pm C_{12}$$

C. For the numerator of eq.(6.4b):

$$S^{\omega_n T}_{C_0} = -\frac{1}{2}\left[1 + (\omega_n T/2)^2 - \frac{\omega_n T/2}{Q_n}\right]$$

$$S^{\omega_n T}_{C_1} = \frac{1}{2}\left[1 + (\omega_n T/2)^2\right]$$

$$S^{\omega_n T}_{C_2} = -\frac{1}{2}\frac{\omega_n T/2}{Q_n}$$

$$S^{\omega_n T}_{C_{12}} = \pm \frac{1}{2}\left[1 + (\omega_n T/2)^2\right] \qquad \text{for } K_{12} = \pm C_{12}$$

$$S^{Q_n}_{C_0} = \frac{1}{2}\left[1 + (\omega_n T/2)^2 - \frac{\omega_n T/2}{Q_n}\right]$$

$$S^{Q_n}_{C_1} = \frac{1}{2}\left[1 - (\omega_n T/2)^2\right]$$

$$S^{Q_n}_{C_2} = -1 + \frac{1}{2}\frac{\omega_n T/2}{Q_n}$$

$$S^{Q_n}_{C_{12}} = \pm \frac{1}{2}\left[1 - (\omega_n T/2)^2\right] \qquad \text{for } K_{12} = \pm C_{12}$$

Furthermore all biquad circuits obtained in this way have output voltages that are fixed over a full clock-period, making them

output-to-input compatible with other biquadratic cells. Moreover, the circuits derived from fig.6.11b don't need an input voltage that is fixed over a full clock-period, making them also input-to-output compatible with other circuits.

6.3 OTHER EXISTING SIGNAL FLOW GRAPH BASED SC SYNTHESIS METHODS.

Signal Flow Graphs can be considered as versatile tools for (SC) filter synthesis (and analysis) and are therefore frequently applied in many design methods, including LC ladder based leapfrog synthesis and multiple-loop feedback and feedforward synthesis with biquadratic cells.
In this paragraph however, we will restrict ourselves to existing methods, which directly synthesize the desired transfer function in the z-domain (or equivalently expressed in z^{-1} or $d=z^{-1/2}$).

As stated before, one of the reasons that complicates the SFG synthesis of SC filters with respect to, for example digital filter synthesis, is the fact that we have to deal with clock-phases. This forces us to work in certain specific graph structures.

One approach is to use a Discrete Signal Flow Graph description as applied for digital filter synthesis and implement the multiplications, summations and delays with SC structures.
A possible SC structure that can be used for this purpose [56] is given in fig.6.12.

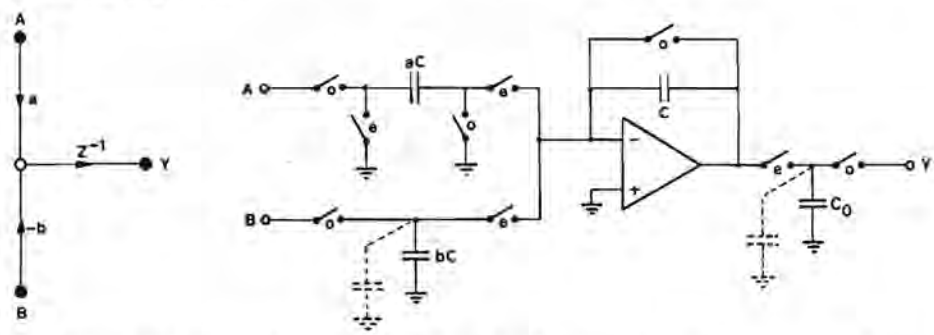


fig.6.12: Part of a Discrete Signal Flow Graph and a corresponding SC implementation (important strays drawn dashed).

As can be seen, this method uses strays-sensitive structures to solve the sign problem. Furthermore, as each summation is realized by a virtual ground node, this approach is rather amplifier consuming. In addition, the opamp networks realize in fact the 'type 5' structures (see chapter 4), having a deteriorated sensitivity for the finite bandwidth and slew-rate of the amplifiers, as stated before. The introduction of these 'type 5' structures can be seen as a way of reducing (flattening) the SFG: all voltage nodes in the graph corresponding with amplifier outputs at clock-phase 'o' are simply made redundant.

Another, more elegant way of such a reduction in 'flattening' the SFG can be found in [57], where the amplifiers are applied in such a way, that for every voltage node (including the input) V_j the expression $V_j^o = dV_j^e$ holds. Here the problem of the two clock-phases has been evaded by 'freezing' all amplifier-outputs at clock-phase 'o'.
The standard building-block for this approach is depicted in fig.6.13.

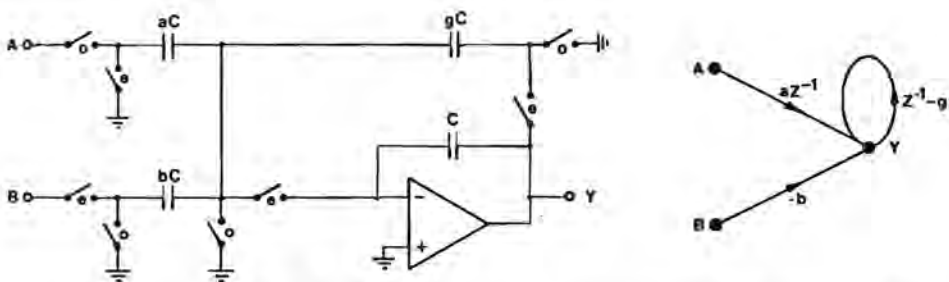


fig.6.13: Standard building-block and corresponding subgraph for the method proposed in [57].

A realization for a biquadratic transfer function given in [57], using this building block, can be shown to have a very poor sensitivity of its numerator for capacitor variations. Furthermore for every stage where aC and/or gC is being used there is 'coupling', resulting in a deteriorated sensitivity for the amplifier gain-bandwidth products, as was cleared up in chapter 5.

In a recent paper [23] this same 'flattening' method of freezing all voltage nodes in clock-phase 'o' was used. In order to solve the problem with the signs, again a strays-sensitive structure was introduced. Two examples of this method are given in the same paper. In the first example the SFG of a biquadratic transfer function is realized, using strays-sensitive structures and two amplifiers in a delay free loop. The other example is a strays-free realization of a biquadratic transfer function, but here 3 amplifiers were needed, one of them without any feedback in one of the clock-phases. This may drive this amplifier into saturation, slowing down the maximum allowable clock-frequency.

A more important competitive approach is given in [58]. However, a closer look to this method shows that, in order to solve the signs-problem, the input signal needs to be held over a full clock-period. On the other hand the output voltage itself changes in every clock-phase. This will for example complicate the application of biquadratic building blocks, generated with this method, in cascaded or multiple-loop designs. The gain-bandwidth sensitivity for the SDG method is expected to be better, because of the small 'coupling' between the amplifiers. Although the sensitivity for capacitance variations in biquads are comparable to the ones obtained by the SDG method, these sensitivities for higher order filters however, turn out to be significantly worse than the sensitivities in the SDG method.

7. A SWITCHED CAPACITOR EQUIVALENT IMMITTANCE CONVERTER

In this chapter another contribution to SC filter synthesis, employing a special circuit, will be considered. This circuit, that will be called an Equivalent Immittance Converter (EIC), has proved to be a useful building-block for practical filter design. As will be shown, the behavior of an EIC in SC filters is comparable with that of a Generalized Immittance Converters (GIC) in continuous-time filters. Therefor we will first briefly discuss these GIC's in section 7.1. Next the SC realization of an EIC circuit will be introduced, and its similarity with a GIC will be shown.

This concept is applied in an (n+1)-th order filter, using n EIC circuits, as cleared up in section 7.2.

In section 7.3, as an example, a 4-th order all-pole filter will be designed. This circuit has actually been built as an NMOS integrated circuit. The transfer of this realized filter will be compared with the ideal behavior.

Furthermore, in section 7.4, we will discuss a compensation method for stray-capacitances in EIC filters.

Finally in section 7.5, the influence of the finite gain of the amplifier of an EIC is considered.

7.1 IMMITTANCE CONVERTERS

The input admittance Y_i at port 1 of a continuous-time GIC is related to the load admittance Y_l at port 2 by

$$Y_i = h(s)Y_l \tag{7.1}$$

as depicted in fig.7.1.

The ports of the GIC can be mutually interchanged. In that case a load admittance Y_l will be converted into an input admittance $Y_i = Y_l/h(s)$. In general $h(s)$ is called the 'admittance conversion function' of the device. Depending on this admittance conversion function, a conductive load G_l can for example be converted into an inductive input admittance $\frac{1}{sL_i}$ for $h(s) = \frac{1}{sG_lL_i}$, or a capacitive load sC_l

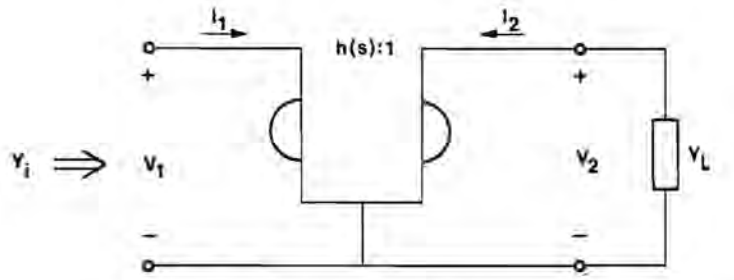


fig.7.1: Immittance converter, transforming a load admittance Y_L into an input admittance Y_i.

into a 'frequency dependant negative resistor' with admittance s^2F_1 for $h(s) = s\frac{F_1}{C_1}$ etc.

Generally two specific types of GIC's are distinguished:

- the Current-converting Generalized Immittance Converter (CGIC), characterized by its chain-matrix description:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & h(s) \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \qquad (7.2)$$

- the Voltage-converting Generalized Immittance Converter (VGIC), described by:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} \frac{1}{h(s)} & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \qquad (7.3)$$

A well-known continuous-time realization of a CGIC is the circuit of Antoniou [59] with two operational amplifiers and four admittances. Another interesting circuit is given by Holt and Carey [60], where only one operational amplifier and four admittances are used for the realization of a GIC with an inherent parallel loading element. Although not mentioned by Holt, this operational amplifier may be replaced by a unity-gain buffer. In this case the circuit still realizes a GIC, but now with an inherent series, instead of a parallel, loading element.

The switched capacitor EIC that will be considered here is realized by the circuit of fig.7.2, using only one operational amplifier and two capacitors with additional switches [61].

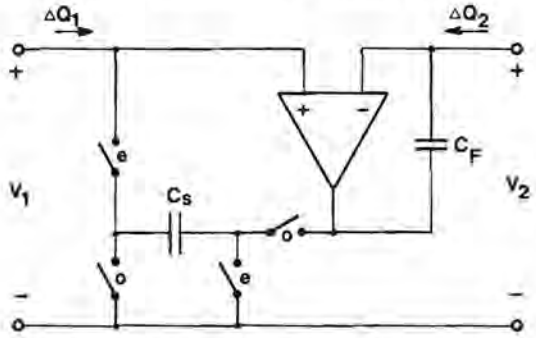


fig.7.2: SC equivalent immittance converter.

The circuit can be described by a chain-matrix K , relating the port voltages and charge-increments for both clock-phases:

$$\begin{pmatrix} V_1^e \\ V_1^o \\ \Delta Q_1^e \\ \Delta Q_1^o \end{pmatrix} = K \begin{pmatrix} V_2^e \\ V_2^o \\ -\Delta Q_2^e \\ -\Delta Q_2^o \end{pmatrix}$$

with

$$K = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ C_s & z^{-1/2}C_s & \frac{C_s/C_F}{z-1} & z^{1/2}\frac{C_s/C_F}{z-1} \\ 0 & 0 & 0 & 0 \end{pmatrix} \qquad (7.4)$$

In order to obtain a 2×2 chain-matrix, that can be compared with a continuous-time description, we define

$$\left.\begin{aligned} \Delta Q_k &= \Delta Q_k^o + z^{-1/2}\Delta Q_k^e \\ V_k &= V_k^o \end{aligned}\right\} \; k \in (1,2). \qquad (7.5)$$

We will consider two cases here:

a: the case for which $V_k^e = z^{-1/2}V_k^o = z^{-1/2}V_k$

b: the case for which $V_k^e = z^{+1/2}V_k^o = z^{+1/2}V_k$

with $k \in (1,2)$.

In fact case a will only be discussed for the sake of completeness. The applications of the EIC that are described in this thesis all use this building-block in mode b.

For both cases the following chain-matrix description is obtained:

$$\begin{bmatrix} V_1 \\ \Delta Q_1 \end{bmatrix} = K' \begin{bmatrix} V_2 \\ -\Delta Q_2 \end{bmatrix} \tag{7.6}$$

with

$$K' = \begin{bmatrix} 1 & 0 \\ \alpha C_S & \dfrac{C_S/C_F}{z-1} \end{bmatrix} \tag{7.7}$$

where $\alpha = 2z^{-1}$ for case a , or $\alpha = (1+z^{-1})$ for case b.

Matrix K' can be factorized as follows:

$$K' = K_1 \cdot K_2 = \begin{bmatrix} 1 & 0 \\ \alpha C_S & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ 0 & \dfrac{C_S/C_F}{z-1} \end{bmatrix} \tag{7.8}$$

This represents in fact an EIC with conversion function $h(z) = \dfrac{C_S/C_F}{z-1}$ with a parallel equivalent admittance $Y_1^*(z) = \alpha C_S$ at port 1, or alternatively $Y_2^*(z) = \alpha(z-1)C_F$ at port 2.

For case a: $Y_1^*(z) = Y_{1a}^*(z) = 2z^{-1}C_S$ or $Y_2^*(z) = Y_{2a}^* = 2(1-z^{-1})C_F$,

For case b: $Y_1^*(z) = Y_{1b}^*(z) = (1+z^{-1})C_S$ or $Y_2^*(z) = Y_{2a}^* = (z-z^{-1})C_F$,

as depicted in fig.7.3.

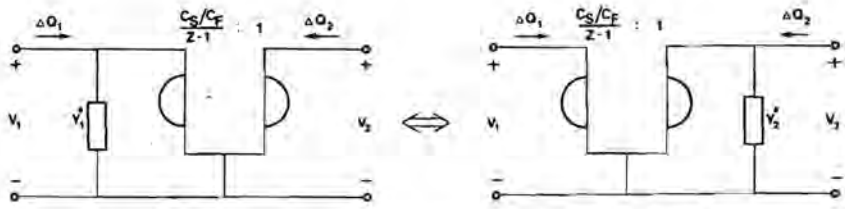


fig.7.3: Equivalent circuits for fig.7.2

$$Y_1^* = Y_{1a}^* = 2z^{-1}C_S \quad \text{or} \quad Y_2^* = Y_{2a}^* = 2(1-z^{-1})C_F \quad \text{(case a)}$$

$$Y_1^* = Y_{1b}^* = (1+z^{-1})C \quad \text{or} \quad Y_2^* = Y_{2a}^* = (z-z^{-1})C_F \quad \text{(case b)}$$

This EIC can be used for the conversion of an equivalent load admittance $Y_l(z)$ at port 2 into an equivalent input admittance $Y_i(z) = h(z)Y_l(z)$ at port 1. When the two ports are mutually exchanged, an equivalent load admittance $Y_l(z)$ will be converted into an equivalent input admittance $Y_i(z) = Y_l(z)/h(z)$.
The inherently obtained equivalent load admittance Y^* will be used as a circuit element for our filter.

In fact the behavior of an EIC in terms of port voltages, charge increments and equivalent admittances is comparable with that of a GIC, expressed in terms of port voltages, currents and admittances. For signals with a low frequency with respect to the sampling frequency $f_s=1/T$ we can use the approximations $(1+z^{-1}) \approx 2z^{-1} \approx 2$ and $z-1 \approx sT$. In this case the circuit of fig.7.3 can be considered as a discrete-time equivalent of a continuous-time CGIC with a conversion function of

$$h(s) \approx \frac{C_S/C_F}{sT} \tag{7.9}$$

and a parallel conductance

$$G^* \approx \frac{2C_S}{T} \qquad \text{at port 1,} \tag{7.10a}$$

or equivalently a parallel capacitor

$$C^* \approx 2C_F \qquad \text{at port 2.} \tag{7.10b}$$

This GIC can actually be realized with the continuous-time circuit of

fig.7.4.

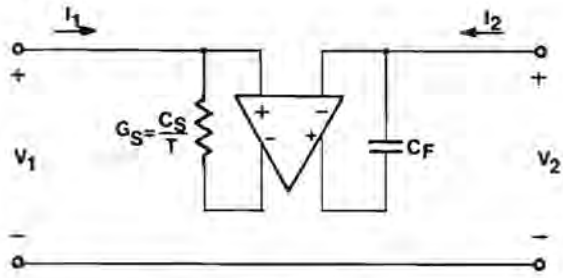


fig.7.4: Continuous-time GIC.

This circuit has a chain-matrix:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = K_c \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \qquad (7.11)$$

with

$$K_c = \begin{bmatrix} 1 & 0 \\ \frac{2C_S}{T} & \frac{C_S/C_F}{sT} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{2C_S}{T} & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ 0 & \frac{C_S/C_F}{sT} \end{bmatrix} \qquad (7.12)$$

Note that for this continuous-time realization a differential output operational amplifier is needed. For the SC circuit however, a normal single-output operational amplifier suffices. This means that in case of an SC realization one has no problems with asymmetry, like unequal gains of the two outputs of a differential output amplifier, or a non-ideal discrimination factor.

7.2 APPLICATION OF GIC's AND EIC's IN FILTER SYNTHESIS

We are able to realize an (n+1)-th order continuous-time filter, as depicted in fig.7.5a, using n GIC's of fig.7.4 as building blocks. An equivalent circuit is drawn in fig.7.5b. Seen from the output using the conversion functions of these GIC's, this circuit can be converted into the circuit of fig.7.5c.

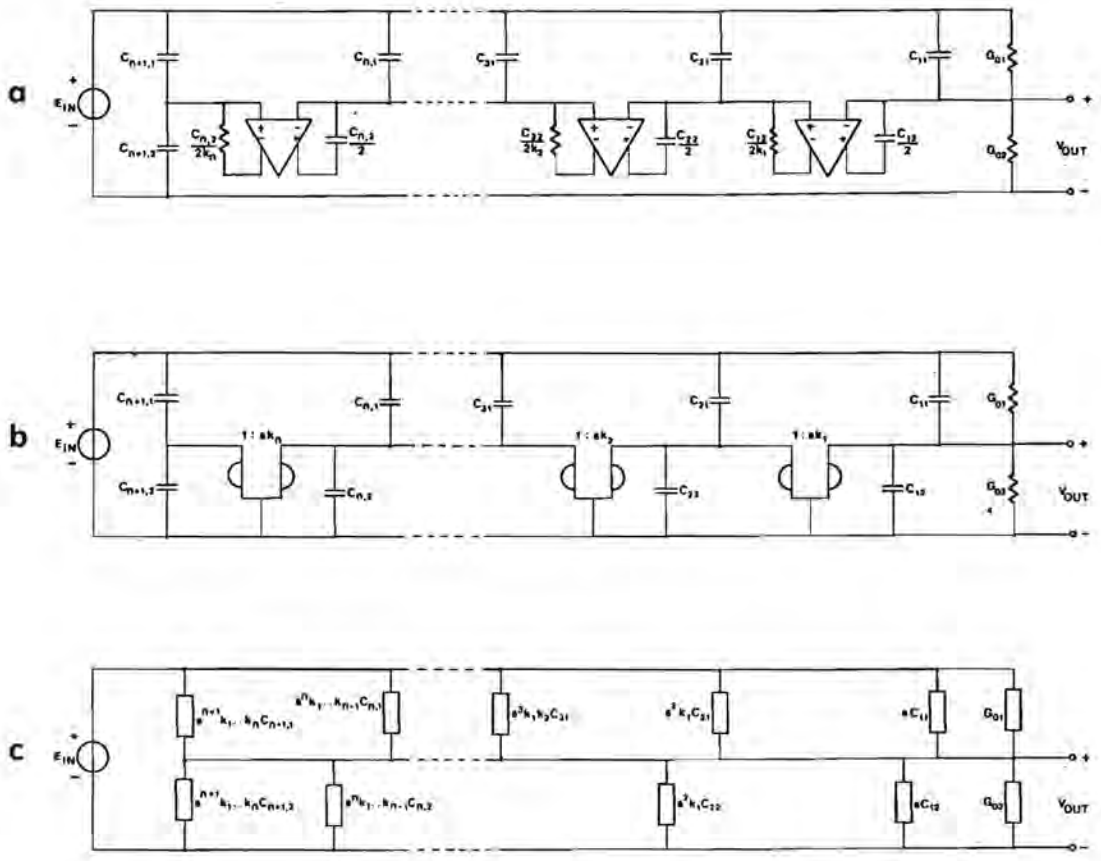


fig.7.5a: (n+1)-th Order continuous-time filter using n times the circuit of fig.7.4,

b: equivalent circuit,

c: converted circuit, as 'seen' from the output side.

From fig.7.5c, the filter can easily be seen to have a transfer function

$$H(s) = \frac{V_{out}(s)}{E_{in}(s)} = \frac{N(s)}{D(s)}$$

with

$$N(s) = G_{01} + sC_{11} + s^2k_1C_{21} + \ldots + s^nk_1k_2..k_{n-1}C_{n,1} + s^{n+1}k_1k_2..k_nC_{n+1,1} \qquad (7.13a)$$

and

$$D(s) = (G_{01}+G_{02})+s(C_{11}+C_{12})+s^2k_1(C_{21}+C_{22})+\ldots.$$
$$\ldots.+s^nk_1k_2\ldots k_{n-1}(C_{n,1}+C_{n,2})+s^{n+1}k_1k_2\ldots k_n(C_{n+1,1}+C_{n+1,2}) \qquad (7.13b)$$

The circuit of fig.7.5a can be transformed into a discrete-time equivalent circuit as given in fig.7.6a, applying n EIC's of fig.7.2. Using equivalent admittances, this circuit can be redrawn as depicted in fig.7.6b, assuming $E^e_{in} = z^{1/2}E^o_{in}$. In this situation all EIC's in the circuit are functioning according to case b. Using the conversion functions of these EIC's, this circuit can be converted into the circuit of fig.7.6c.

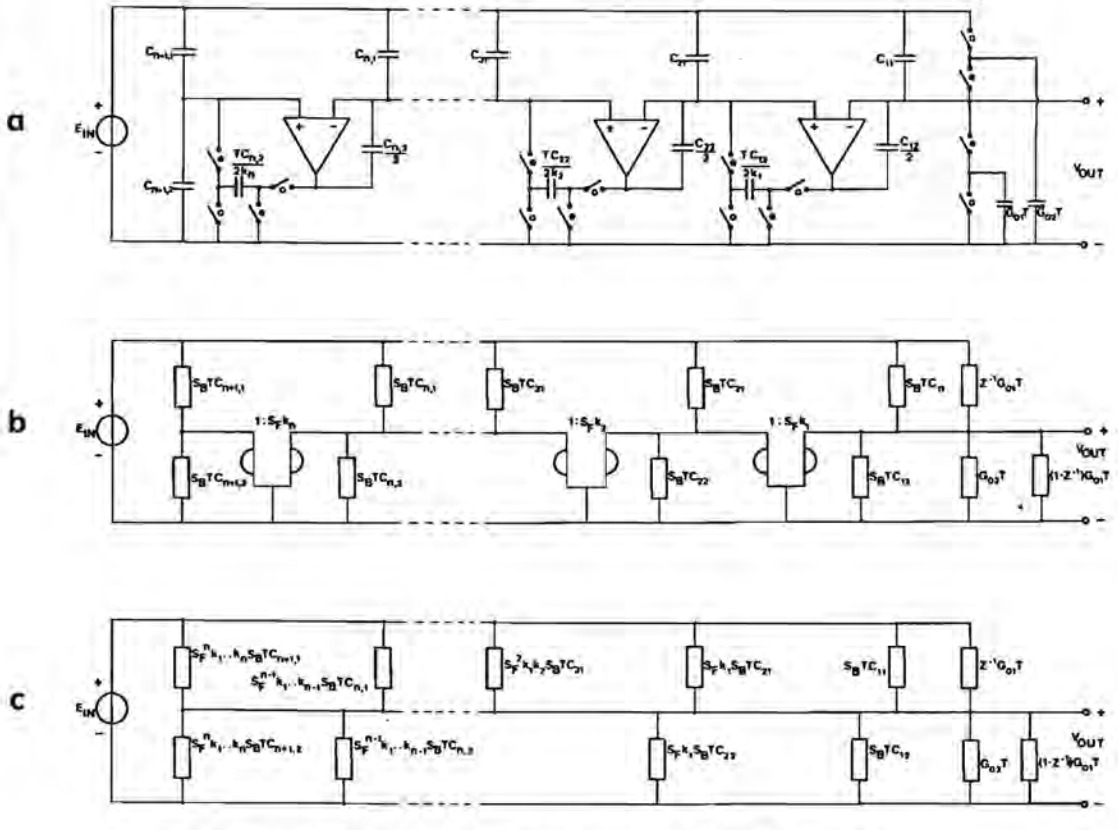


fig.7.6a: (n+1)-th order SC filter using n EIC's of fig.7.2,
b: equivalent circuit, using equivalent admittances,
c: converted circuit, as 'seen' from the output side.

Analysis of this circuit yields a transfer function

$$H^{oo}(z) = \frac{V^{o}_{out}(z)}{E^{o}_{in}(z)} = \frac{N'(z)}{D'(z)}$$

with

$$N'(z) = z^{-1}G_{01}+s_B C_{11}+s_F k_1 s_B C_{21}+.....+s_F^{n-1}k_1 k_2..k_{n-1}s_B C_{n,1}+$$

$$s_F^{n}k_1 k_2..k_n s_B C_{n+1,1} \qquad (7.14a)$$

and

$$D'(z) = (G_{01}+G_{02})+(s_B C_{11}+s_L C_{12})+s_F k_1(s_B C_{21}+s_L C_{22})+....$$

$$....+s_F^{n-1}k_1 k_2..k_{n-1}(s_B C_{n,1}+s_L C_{n,2})+s_F^{n}k_1 k_2..k_n(s_B C_{n+1,1}+s_L C_{n+1,2}) \qquad (7.14b)$$

where

$$s_F = \frac{z-1}{T} \quad , \quad s_B = \frac{z-1}{zT} \quad \text{and} \quad s_L = \frac{z^2-1}{2zT}$$

have been used as abbreviations.
Noting that

$$s_F \approx s_B \approx s_L \approx s \quad \text{and} \quad z^{-1} \approx 1$$

for signal frequencies that are relative low in comparison with the sampling-frequency $f_s = 1/T$, the similarity between the continuous-time transfer function of eq.(7.13) and the discrete-time transfer-function of eq.(7.14) is obvious.

7.3 NMOS REALIZATION OF AN EIC-BASED FILTER.

In [61] a 2-nd order SC bandpass filter with one operational amplifier, based on this approach was presented. Measurements on an SC circuit were compared with a continuous-time realization.

Especially the realization of all-pole filters with our EIC results in very simple structures. In this case capacitors C_{i1} , $i \in (1,2,..,n+1)$

and $G_{02}T$ of fig.7.6 can be omitted, resulting in an n-th order filter realization with only n-1 operational amplifiers, n unswitched and n switched capacitors.

In order to verify the usefulness of this approach in an actually integrated SC filter design, a 4-th order all-pole Butterworth lowpass filter (fig.7.7) was realized in NMOS.
As a starting-point a normalized 4-th order continuous-time Butterworth lowpass transfer function was used:

$$H(s) = \frac{1}{s^4 + 2.613s^3 + 3.414s^2 + 2.613s + 1} \qquad (7.15)$$

This was transformed into a discrete-time transfer function with a cut-off frequency chosen as $0.1f_s$, with f_s being the sampling frequency. As a transformation method, the matched-z transform was applied, yielding:

$$H(z) = \frac{0.06858}{z^4 - 2.402z^3 + 2.361z^2 - 1.084z + 0.1936} \qquad (7.16)$$

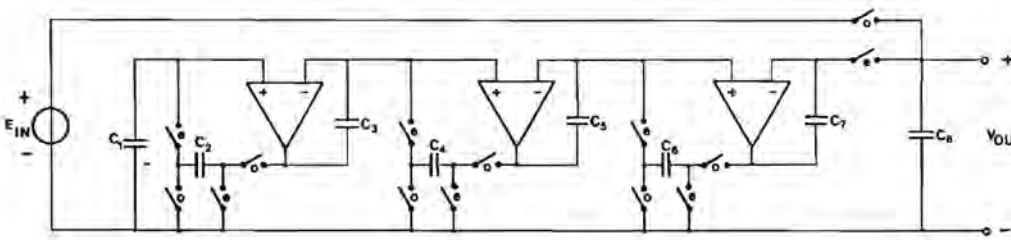


fig.7.7: 4-th Order all-pole filter.

Application of eq.(7.14) and minimization of the total capacitance results in capacitor values:

$C_1 = 1.000$ $C_2 = 1.251$
$C_3 = 1.142$ $C_4 = 1.000$
$C_5 = 2.680$ $C_6 = 1.000$
$C_7 = 2.648$ $C_8 = 1.000$

expressed in unit-capacitances. These values were slightly altered as a compensation for stray-capacitances, as will be explained in section 7.4.

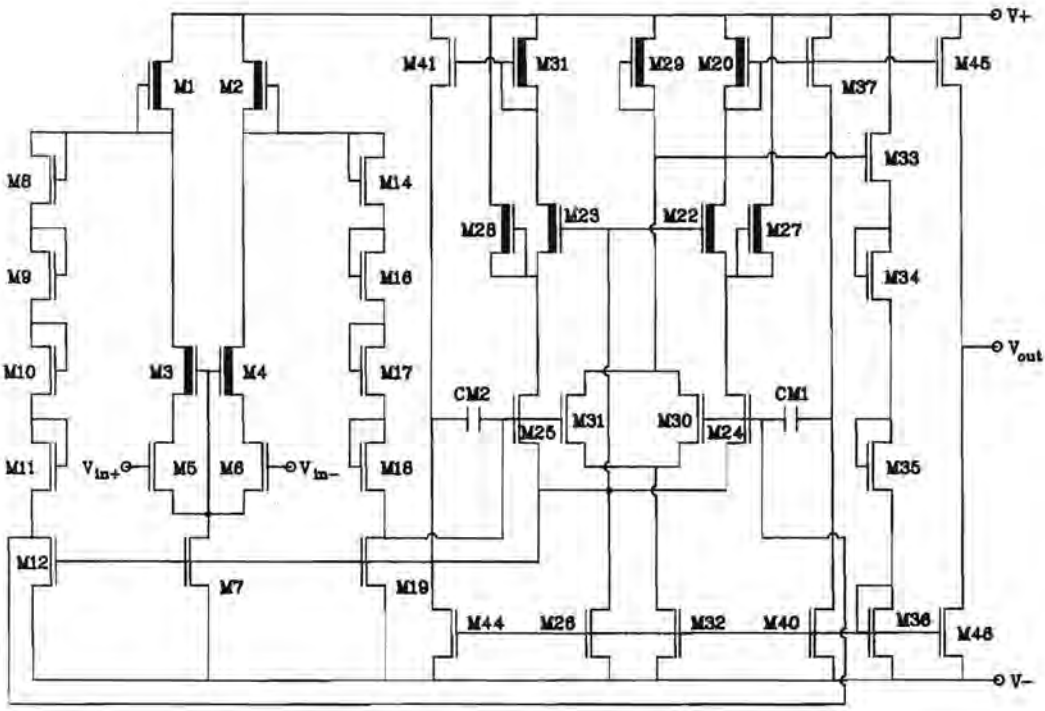


fig.7.8: NMOS amplifier circuit.

In fig. 7.8 the circuit diagram of the applied NMOS amplifiers [62] is given. It consists of a differential input-stage (M_1-M_7), level-shifters (M_8-M_{12}, M_{14}-M_{19}), a gain-stage (M_{20}-M_{26}) with current-injection (M_{27}-M_{28}), common-mode feedback (M_{29}-M_{36}) and Miller compensation (M_{37}-M_{44}, C_{M1}, C_{M2}) and finally an output-stage (M_{45}-M_{46}).

The specifications for this amplifier are:

Supply voltage:	±6 V
DC open loop gain A_0:	63 dB
CMRR:	97 dB
Output voltage swing:	±2 V
Phase-margin (20pF load):	45°
Gain-bandwidth product:	3.5 MHz
Slew rate (20pF load):	1 V/μsec

The capacitors were composed from double-poly type unit-capacitances of 80×80 μm^2 (approx. 4pF). Standard 6×6 μm^2 enhancement NMOS transistors (V_{th} = 0.55 V typ.) were applied for the switches, without additional circuitry for compensation of clock-feedthrough.

A die photo of this filter is given in fig.7.9, showing the amplifiers at the upper half, the capacitors at the lower half. At the lower left edge the clock circuit is situated.
Dimensions of the total filter are approx. 1.5 × 0.7 mm^2.

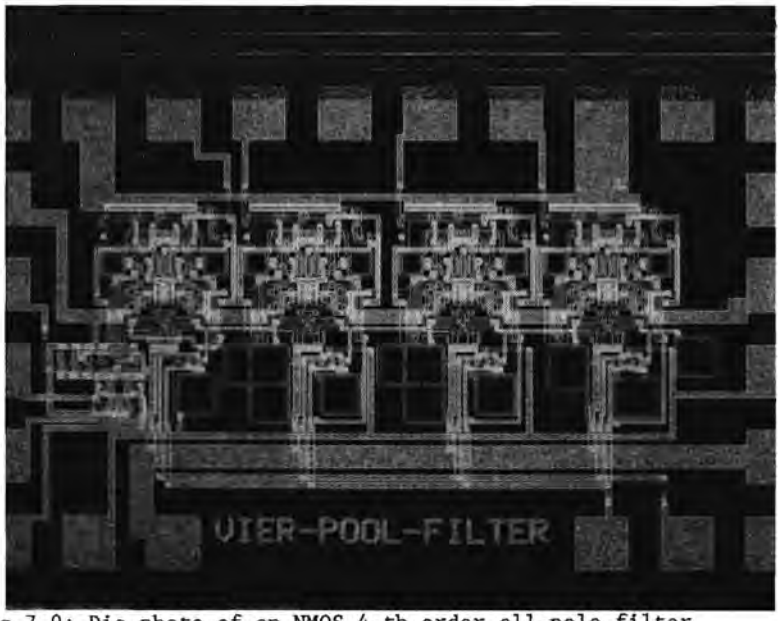


fig.7.9: Die photo of an NMOS 4-th order all-pole filter.

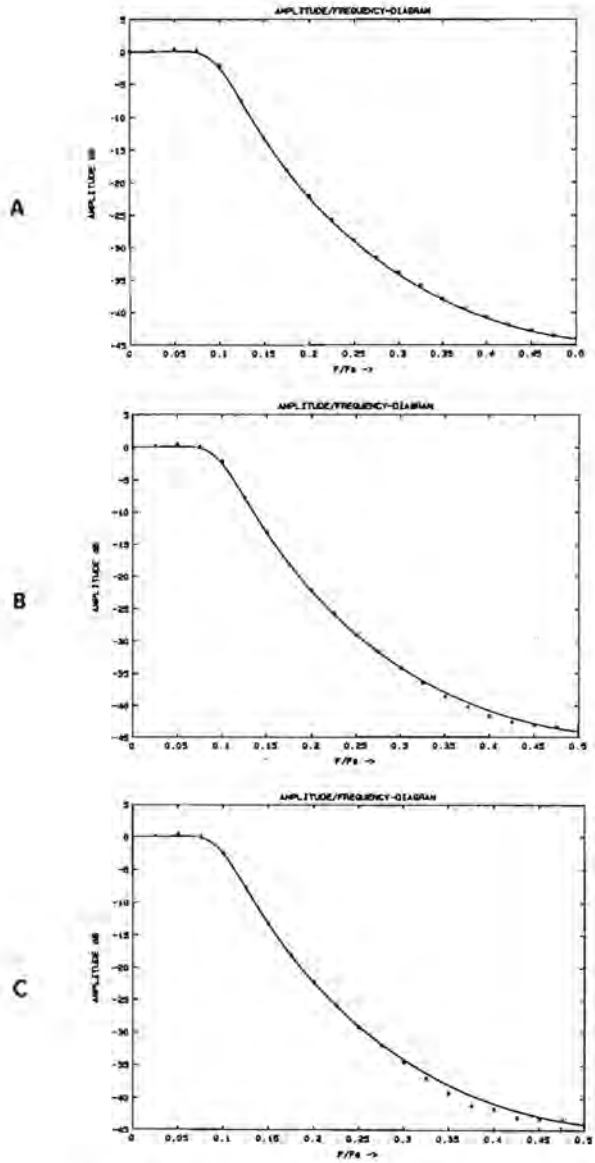


fig.7.10: Amplitude transfer diagrams for several clock-frequencies f_s of the realized circuit of fig.7.7

a: f_s = 500 Hz - 50kHz; b: f_s = 100 kHz; c: f_s = 200 kHz.

———— : ideal curve

x x x x x : experimental data

Measurement of the amplitude transfer for clock-frequencies varying from 500 Hz to 200 kHz were in good accordance with the theoretical curve, as depicted in fig.7.10

Further experimentally obtained data (f_s = 50 kHz, clock-amplitude ±4V):

- Clock-feedthrough: 8 mV (at $f = f_s$)
- DC offset voltage: 5 mV
- Output noise voltage: 7 $\mu V/\sqrt{Hz}$ at $f = 0.1\ f_s$ (maximum in noise-spectrum)
  $<2\ \mu V/\sqrt{Hz}$ for $f > 0.2\ f_s$
- Harmonic distortion: -67 dB (2^{nd} harm.)
  -59 dB (3^{rd} harm.)
  -71 dB (4^{th} harm.)
  } input signal 0.775 V, 400 Hz

7.4 COMPENSATION OF PARASITIC CAPACITANCES

The EIC of fig.7.2 is insensitive to the (relative large) bottom-plate stray capacitances, if capacitors C_S and C_F have their bottom plates at the amplifier-output side of the circuit. Although the circuit is sensitive to the (relative small) top-plate stray capacitances, it will be shown that these strays can be incorporated by predistorting the capacitor values C_S and C_F. Of course this predistortion is only useful for applications where the designer has a reasonable estimation for the actual stray-capacitances. It should be noted that compensation by the application of predistortion is never ideal in practice, because of the non-linearities of the strays.

In fig.7.11 the EIC circuit of fig.7.2 is redrawn, however now with the stray-capacitances taken into consideration.

Here C_{p1} represents the top-plate stray-capacitance of C_S and the strays of the switch-terminals connected with it. C_{p2} represents the top-plate strays of C_F , the stray-capacitance from the inverting amplifier input to ground and all other strays connected with it. C_{p3}

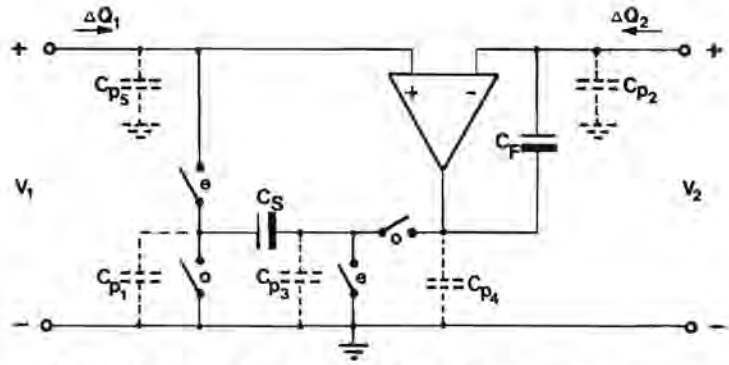


fig.7.11: EIC circuit with stray-capacitances.

stands for the bottom-plate strays of C_S and that of the connected switch terminals. C_{p4} incorporates the bottom-plate strays of C_F, the output capacitance of the operational amplifier and the strays of the connected switch terminal. C_{p5} is needed for the representation of all strays connected with the non-inverting amplifier input, included the connected switch terminal.

In fact C_{p5} can be considered as the 'C_{p2}' of the left neighbor EIC, or if the EIC itself is the leftmost, C_{p5} can be incorporated in the capacitor connected with port 1. If the output-impedance of the amplifier is sufficiently low, C_{p4} will be redundant. The same is true for C_{p3}, if furthermore the on-resistance of the switches may be neglected. Therefore the only parasitic capacitances taken into consideration will be C_{p1} and C_{p2}.

With these two parasitics taken into account, the chain matrix of eq.(7.4) is rewritten as:

$$K = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ C_S+C_{p1} & z^{-1/2}C_S\left[1+\frac{C_{p2}}{C_F}\right] & \frac{C_S/C_F}{z-1} & z^{1/2}\frac{C_S/C_F}{z-1} \\ 0 & 0 & 0 & 0 \end{bmatrix} \qquad (7.17)$$

Similar to section 7.1, two cases

a: $(V_k^a = z^{-1/2}V_k^o = z^{-1/2}V_k)$ and

b: $(V_k^a = z^{-1/2}V_k^o = z^{-1/2}V_k)$

are considered.

Again the 4×4 chain matrix can be reduced to dimensions 2×2:

$$\begin{pmatrix} V_1 \\ \Delta Q_1 \end{pmatrix} = K' \begin{pmatrix} V_2 \\ -\Delta Q_2 \end{pmatrix}$$

with

$$K' = \begin{bmatrix} 1 & 0 \\ Y^* & \dfrac{C_S/C_F}{z-1} \end{bmatrix} \qquad (7.18)$$

where $Y^* = Y_a^* = 2z^{-1}C_S + z^{-1}\left(C_{p1} + \dfrac{C_S}{C_F} C_{p2}\right)$ for case a (7.19a)

and $Y^* = Y_b^* = (1+z^{-1})C_S + \left(C_{p1} + z^{-1}\dfrac{C_S}{C_F} C_{p2}\right)$ for case b (7.19b)

It can be seen that the parasitic capacitances affect only the inherent loading admittance Y^*. The equivalent admittance conversion function $h(z) = \dfrac{C_S/C_F}{z-1}$ turns out to be strays-insensitive for both cases.

For case a the parasitics can be completely compensated for, by replacing C_S by C_S' and C_F by C_F' according to

$$C_S' = C_S - \frac{1}{2}\left(C_{p1} + \frac{C_S}{C_F} C_{p2}\right) \qquad C_F' = C_F \frac{C_S'}{C_S} \qquad (7.20a)$$

For case b complete compensation for parasitics can only be derived if $C_{p1} = \dfrac{C_S}{C_F} C_{p2}$ (eventually obtained by increasing the smallest of the two parasitics on purpose) by replacing C_S and C_F by

$$C_S' = C_S - C_{p1} \qquad C_F' = C_F \frac{C_S'}{C_S} \qquad (7.20b)$$

For highly oversampled filters, where only frequencies in the vicinity

of $z = 1$ are of interest, predistortion according to eq.(7.20a) will be sufficiently effective, also for case b.
Note that our 4-th order all-pole circuit of fig.7.7 functions in accordance with case b for $E^e_{in} = z^{1/2}E^o_{in}$. As it furthermore has a relative low cut-off frequency, this latter compensation method was applied for that circuit.

7.5 FINITE GAIN EFFECTS OF THE AMPLIFIERS

Besides parasitic capacitances, effects due to the finite gain of the amplifier in the EIC are another important item that should be considered.

When the amplifier has a finite gain A_0 , this will alter the chain matrix description of the EIC of eq.(7.4) into:

$$K = \begin{bmatrix} 1+\frac{1}{A_0} & 0 & \frac{1}{A_0C_F}\frac{z}{z-1} & \frac{1}{A_0C_F}\frac{z^{-1/2}}{z-1} \\ 0 & 1+\frac{1}{A_0} & \frac{1}{A_0C_F}\frac{z^{-1/2}}{z-1} & \frac{1}{A_0C_F}\frac{z}{z-1} \\ C_s\left(1+\frac{1}{A_0}\right) & z^{-1/2}C_s & \frac{C_s/C_F}{z-1}\left(1+\frac{z}{A_0}\right) & z^{1/2}\frac{C_s/C_F}{z-1}\left(1+\frac{1}{A_0}\right) \\ 0 & 0 & 0 & 0 \end{bmatrix} \qquad (7.21)$$

For case a, for which $V^e_k = z^{-1/2}V^o_k = z^{-1/2}V_k$
and case b, for which $V^e_k = z^{+1/2}V^o_k = z^{+1/2}V_k$
$\Big\}\ k \in (1,2)$

the size of this chain matrix can again be reduced to 2×2 in a similar way as was done in section 7.1:

$$\begin{bmatrix} V_1 \\ \Delta Q_1 \end{bmatrix} = K' \begin{bmatrix} V_2 \\ -\Delta Q_2 \end{bmatrix} \qquad (7.22)$$

For case a:

$$K' = K'_a = \begin{bmatrix} 1+\frac{1}{A_0} & \frac{z}{A_0 C_F (z-1)} \\ \left(2+\frac{1}{A_0}\right) z^{-1} C_S & \frac{C_S/C_F}{z-1}\left(1+\frac{1}{A_0}\right) \end{bmatrix} \tag{7.23}$$

which can be factorized as

$$K'_a = \begin{bmatrix} 1+\frac{1}{A_0} & \frac{z}{A_0 C_S} \\ \left(2+\frac{1}{A_0}\right) z^{-1} C_S & 1+\frac{1}{A_0} \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ 0 & \frac{C_S/C_F}{z-1} \end{bmatrix} \tag{7.24}$$

The only alteration with respect to the ideal case is the addition of an admittance $A_0 z^{-1} C_S$ in the inherently obtained load-circuit, as depicted in fig.7.12. The equivalent admittance conversion function turns out to be insensitive to the finite gain of the amplifier.

For case b the 2×2 chain matrix

$$K' = K'_b = \begin{bmatrix} 1+\frac{1}{A_0} & \frac{z}{A_0 C_F (z-1)} \\ \left(1+z^{-1}+\frac{1}{A_0}\right) C_S & \frac{C_S/C_F}{z-1}\left(1+\frac{z}{A_0}\right) \end{bmatrix} \tag{7.25}$$

can be factorized as

$$K'_b = \begin{bmatrix} 1+\frac{1}{A_0} & \frac{z}{A_0 C_S} \\ \left(1+z^{-1}+\frac{1}{A_0}\right) C_S & 1+\frac{z}{A_0} \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ 0 & \frac{C_S/C_F}{z-1} \end{bmatrix} \tag{7.26}$$

Also for case b the finite gain of the amplifier is fully incorporated and turns up in the added equivalent admittance $A_0 z^{-1} C_S$ only, as depicted in fig.7.12.

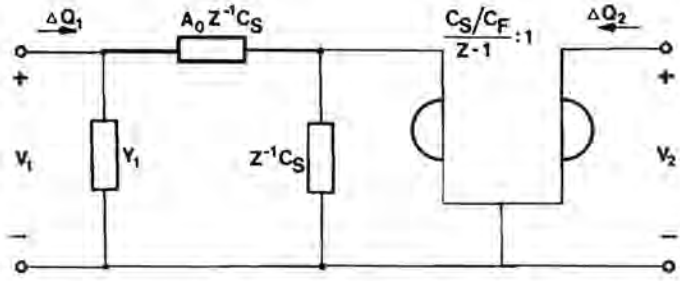


fig.7.12: Equivalent circuit for fig.7.2 with non-ideal amplifier with finite gain A_0
$Y_1 = z^{-1}C_S$ for case a
$Y_1 = C_S$ for case b

It will be clear that the load-circuit can be converted to port 2.

For the continuous-time GIC circuit of fig.7.4 the finite amplifier gain can be modelled in a similar way (fig.7.13). Also for this device, the admittance conversion function turns out to be insensitive to this non-ideal gain. The only effect is the addition of an admittance A_0G_S in the load-circuit.

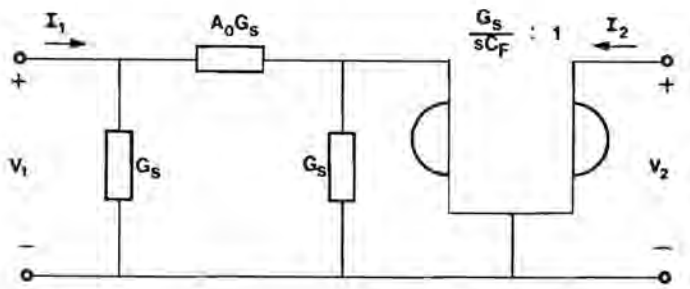


fig.7.13: Equivalent circuit for fig.7.2 with non-ideal amplifier with finite gain A_0

This representation of the finite amplifier gain, expressed in virtual (equivalent) admittances can give us more insight in its effects.

8. CONCLUSIONS.

A number of contributions to switched capacitor filter synthesis were proposed in this thesis.
The aim was to create a methodology for a synthesis, that would generate biphase-clocked SC filters which should inherently have the strays-insensitivity property. For that purpose Hasler's constraints were extended and combined with a simplified Signal Flow Graph approach. This resulted in three methods, one of them, based on a 'Strays-insensitive Design Graph', being very well suited for an algorithmic approach. This method was shown to have a number of additional attractive properties, making it a valuable competitor for other existing synthesis methodologies.
Furthermore an SC 'Equivalent Immittance Converter' was presented. As was shown, its application may result in filters with a reduced number of circuit elements. Its usefulness was demonstrated with a fourth order filter as an integrated circuit, realized in NMOS technology.

Some suggestions can be made for a follow-up of the presented work.

In the first place the algorithmic character of the SDG-based synthesis seems to make it very well suited for an automated SC filter design. In fact at this moment a great deal of the design steps are already implemented in a number of separate computer programs. Integrating these in one main program would be of advantage.

Two forms for an SDG were presented, but very likely more forms, with hopefully comparable, or even better properties can be found.

At this moment the considered synthesis is restricted to biphase-clocked circuits only. An extension to multiphase-clocked circuits could be investigated.

An 'exhaustive search', for strays-insensitive biquads, as was already suggested in section 6.2, using the 'extended Hasler constraints' could be made.

APPENDIX A

EXAMPLE OF THE ANALYSIS BASED ON CHARGE CONSERVATION OF AN SC CIRCUIT WITH FINITE AMPLIFIER DC GAIN AND BANDWIDTH.

Consider the circuit of fig. A.1.

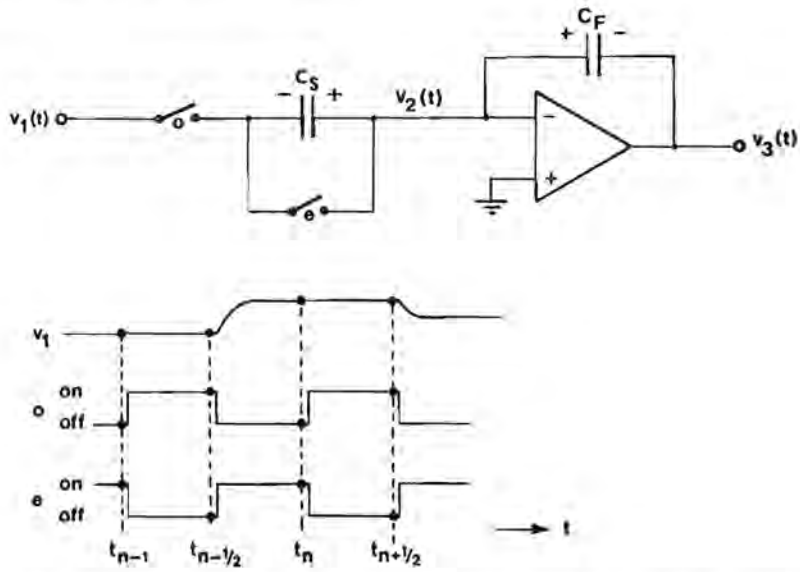


Fig. A.1: example circuit for an analysis method based on charge conservation

All elements in this circuit are assumed ideal, except for the gain of the amplifier, which has a single-pole roll-off frequency dependancy:

$$V_3(s) = - \frac{A_o}{1 + \frac{sA_o}{\omega_u}} V_2(s) \qquad \text{(A.1a)}$$

or expressed in the time domain:

$$\frac{dv_3(t)/dt}{\omega_u} + \frac{v_3(t)}{A_o} = - v_2(t) \qquad \text{(A.1b)}$$

The input voltage $v_1(t)$ changes only during clock-phase 'e'.
As a first step the circuit is redrawn for clock-phases 'e' and 'o' separately.

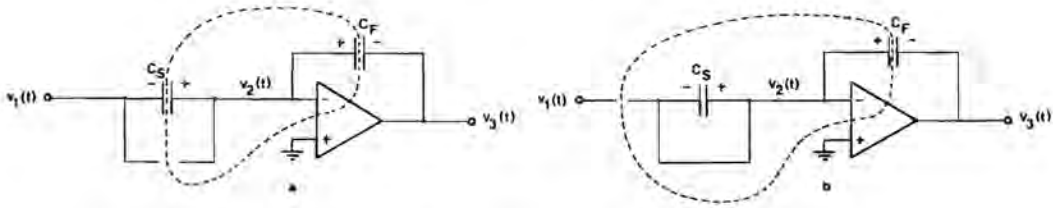


Fig.A.2a: example circuit of fig. A.1 during clock-phase 'o'
b: " " " " " " " " 'e'

The dashed lines in figs.A.2a and b represent the charge conservation contours.
For clock-phase 'o' charge conservation can be expressed as

$$q_S(t) + q_F(t) = q_S(t_{n-1}) + q_F(t_{n-1}), \qquad t_{n-1} \le t \le t_{n-1/2}$$

or, using the fact that $q_S(t_{n-1}) = 0$:

$$q_S(t)+q_F(t)=q_F(t_{n-1}), \qquad t_{n-1} \le t \le t_{n-1/2} \qquad (A.2a)$$

For clock-phase 'e':

$$q_F(t) = q_F(t_{n-1/2}), \qquad t_{n-1/2} \le t \le t_n \qquad (A.2b)$$

with q_i being the charge on the plate marked '+' of capacitor i.
Expressed in node voltages and capacitances:

$$C_s[v_2(t) - v_1(t)] + C_F[v_2(t) - v_3(t)] = C_F[v_2(t_{n-1}) - v_3(t_{n-1})], \qquad t_{n-1} \le t \le t_{n-1/2} \qquad (A.3a)$$

$$C_F[v_2(t) - v_3(t)] = C_F[v_2(t_{n-1/2}) - v_3(t_{n-1/2})], \qquad t_{n-1/2} \le t \le t_n \qquad (A.3b)$$

So for $t = t^+_{n-1}$, the moment immediately after the ending of phase 'e' and the beginning of phase 'o';

$$C_s[v_2^+(t_{n-1}) - v_1(t_{n-1})] + C_F v_2^+(t_{n-1}) = C_F v_2(t_{n-1}) \qquad (A.4a)$$

where the fact has been used that $v_1(t^+_{n-1}) = v_1(t_{n-1})$
and $v_3(t_{n-1}^+) = v_3(t_{n-1})$

For $t=t^+_{n-1/2}$ immediately after the ending of phase 'o' and the beginning of phase 'e', using $v_3(t^+_{n-1/2}) = v_3(t_{n-1/2})$:

$$v_2(t^+_{n-1/2}) = v_2(t_{n-1/2}) \qquad (A.4b)$$

Combining eq. (A.3a) and (A.1b) yields:

$$\frac{dv_3(t)/dt}{\omega_u} + v_3(t)\ (\beta + \frac{1}{A_o}) = \beta\ v_3(t_{n-1}) - v_2(t^+_{n-1}), \qquad (A.5a)$$
$$t_{n-1} < t \leq t_{n-1/2}$$

with $\beta = \dfrac{C_F}{C_s + C_F}$

Eq. (A.3b) and (A.1b) result in:

$$\frac{dv_3(t)/dt}{\omega_u} + v_{3(t)} \left[1 + \frac{1}{A_o}\right] = v_3(t_{n-1/2}) - v_2(t^+_{n-1/2}), \qquad (A.5b)$$
$$t_{n-1/2} < t \leq t_n$$

Note that there are two mechanisms playing an important role:

- the mechanism of charge redistribution
- the mechanism of relaxation of the amplifiers.

In most practical circuits, with not too high output resistances of the amplifiers and on-resistances of the switches, the first mechanism is relative fast. Immediately after the beginning of a new clock-phase charge is redistributed between the capacitors, in acordance with the charge conservation relations .

Now a situation has been created where the amplifiers have departed from steady state. which they try to reach again. This is a mechanism of relaxation, in accordance with the differential equations describing the circuit behaviour during the clock phases [eq. (A.5a) and (A.5b)].

The time constants of this relaxation mechanism highly depend on circuit topology and bandwidth of the amplifiers. In most practical circuits it is a slower mechanism than that of charge redistribution, but its time constants should be short enough in comparison with the duration of the clock-phases, in order to keep the amplifier bandwidth

sensitivities low.

The solution for eq. (A.5a) is:

$$v_3(t) = \frac{\left[v_2(t^+_{n-1}) + \frac{v_3(t_{n-1})}{A_o}\right] e^{-(t-t_{n-1})/\tau_o} + \beta\, v_3(t_{n-1}) - v_2(t^+_{n-1})}{\beta + \frac{1}{A_o}},$$

$$t_{n-1} < t \leq t_{n-1/2}$$

with τ_o being the time-constant in clock-phase 'o': $\tau_o = \frac{1}{\omega_u(\beta + \frac{1}{A_o})}$

It is assumed here that $t_n - t_{n-1/2} = t_{n-1/2} - t_{n-1} = T/2$, so

$$v_3(t_{n-1/2}) = \frac{\left[v_2(t^+_{n-1}) + \frac{v_3(t_{n-1})}{A_o}\right] e^{-T/2\tau_o} + \beta\, v_3(t_{n-1}) - v_2(t^+_{n-1})}{\beta + \frac{1}{A_o}}, \qquad \text{(A.6a)}$$

and for eq.(A.5b):

$$v_3(t) = \frac{\left[v_2(t^+_{n-1/2}) + \frac{v_3(t_{n-1/2})}{A_o}\right] e^{-(t-t_{n-1/2})/\tau_e} + v_3(t_{n-1/2}) - v_2(t^+_{n-1/2})}{1 + \frac{1}{A_o}}$$

$$t_{n-1/2} < t \leq t_n$$

τ_e being the time-constant in clock-phase 'e': $\tau_e = \frac{1}{\omega_u\,(1 + \frac{1}{A_0})}$

so

$$v_3(t_n) = \frac{\left[v_2(t^+_{n-1/2}) + \frac{v_3(t_{n-1/2})}{A_o}\right] e^{-\frac{T}{2\tau_e}} + v_3(t_{n-1/2}) - v_2(t^+_{n-1/2})}{1 + \frac{1}{A_o}} \qquad \text{(A.6b)}$$

Using eq.(A.4a) and (A.4b) yields:

$$v_3(t_{n-1/2}) =$$

$$= \frac{(1-\beta)\left(e^{-\frac{T}{2\tau_o}}-1\right)v_1(t_{n-1}) + \beta\left(e^{-\frac{T}{2\tau_o}}-1\right)v_2(t_{n-1}) + \left(\beta+\frac{e^{-\frac{T}{2\tau_o}}}{A_o}\right)v_3(t_{n-1})}{\beta + \frac{1}{A_o}} \qquad \text{(A.7a)}$$

$$v_3(t_n) = \frac{\left(e^{-\frac{T}{2\tau_e}}-1\right)v_2(t_{n-1/2}) + \left(1+\frac{e^{-\frac{T}{2\tau_e}}}{A_o}\right)v_3(t_{n-1/2})}{1+\frac{1}{A_o}} \qquad \text{(A.7b)}$$

Eq. (A.7a) and (A.7b) can be transformed to the z-domain:

$$V_3^o = \frac{z^{-1/2}}{\beta+\frac{1}{A_o}}\left[(1-\beta)(e^{-\frac{T}{2\tau_o}}-1)V_1^e + \beta(e^{-\frac{T}{2\tau_o}}-1)V_2^e + \left(\beta+\frac{e^{-\frac{T}{2\tau_e}}}{A_o}\right)V_3^e\right] \qquad \text{(A.8a)}$$

$$V_3^e = \frac{z^{-1/2}}{1+\frac{1}{A_o}}\left[\left(e^{-\frac{T}{2\tau_e}}-1\right)V_2^o + \left(1+\frac{e^{-\frac{T}{2\tau_e}}}{A_o}\right)V_3^o\right] \qquad \text{(A.8b)}$$

with

$$V_i^o = V_i^o(z) = \sum_{n=-\infty}^{\infty} v_i(t_{n-1/2})z^{-(n-1/2)} \quad \text{and} \quad V_i^e = V_i^e(z) = \sum_{n=-\infty}^{\infty} v_i(t_n)z^{-n},$$

$$i = 1,2,3.$$

Now taking eq. (A.3a) for $t = t_{n-1/2}$, eq. (A.3b) for $t=t_n$ and transformation to the z-domain yields:

$$V_2^o = \frac{z^{-1/2}(1-\beta)V_1^e + \beta(1-z^{-1})V_3^o}{1-z^{-1}\beta} \qquad \text{(A.9a)}$$

$$V_2^e = \frac{z^{-1}(1-\beta)V_1^e - z^{-1/2}(1-\beta)V_3^o}{1-z^{-1}\beta} + V_3^e \qquad \text{(A.9b)}$$

After some manipulation combining eq. (A.8a), (A.8b), (A.9a) and (A.9b) yields:

$$\frac{V_3^e}{V_1^o} = z^{1/2}\frac{V_3^e}{V_1^e} = \frac{N^e}{D}$$

and $$\frac{V_3^o}{V_1^o} = z^{1/2}\frac{V_3^o}{V_1^e} = \frac{N^o}{D}$$

with

$$D = \left[\left(\beta + \frac{1}{A_o}\right)(1-z^{-1}\beta) + z^{-1}\beta\,(\beta-1)\left(1-e^{-\frac{T}{2\tau_o}}\right)\right]\left(1+\frac{1}{A_o}\right) +$$

$$+ z^{-1}\,e^{-\frac{T}{2\tau_o}}\left(\beta+\frac{1}{A_o}\right)\left[\beta\left(1-e^{-\frac{T}{2\tau_e}}\right)(1-z^{-1}) - (1-z^{-1}\beta)\left(1+\frac{e^{-\frac{T}{2\tau_e}}}{A_o}\right)\right] \qquad \text{(A.10a)}$$

$$N^e = -z^{-1/2}(1-\beta)\left[\left(\beta+\frac{1}{A_o}\right)\left(1-e^{-\frac{T}{2\tau_e}}\right) + \left(1+\frac{e^{-\frac{T}{2\tau_e}}}{A_o}\right)\left(1-e^{-\frac{T}{2\tau_o}}\right) +\right.$$

$$\left. - \left(1-e^{-\frac{T}{2\tau_e}}\right)\left(1-e^{-\frac{T}{2\tau_o}}\right)\beta\right] \qquad \text{(A.10b)}$$

$$N^o = -(1-\beta)\left[\left(1+\frac{1}{A_o}\right)\left(1-e^{-\frac{T}{2\tau_o}}\right) + z^{-1}\left(\beta+\frac{1}{A_o}\right)\left(1-e^{-\frac{T}{2\tau_e}}\right)e^{-\frac{T}{2\tau_o}}\right] \qquad \text{(A.10c)}$$

When $A_o \gg 1$ and $\omega_u T \gg 1$ this can be approximated by

$$D \approx \left[\left(\beta+\frac{1}{A_o}\right)(1-z^{-1}\beta) - z^{-1}\beta\,(1-\beta)\right]\left(1+\frac{1}{A_o}\right) \qquad \text{(A.11a)}$$

$$N^e \approx -z^{-1/2}(1-\beta)\left[1+\frac{1}{A_o} - (1-\beta)\,e^{-\frac{T}{2\tau_o}}\right] \qquad \text{(A.11b)}$$

$$N^{o} \approx -(1-\beta)\left[1+\frac{1}{A_o}-(1-z^{-1}\beta)e^{-\frac{T}{2\tau_o}}\right] \qquad (A.11c)$$

In the ideal case ($A_o \to \infty$, $\omega \to \infty$)

$$H^{oe} = \frac{V_3^e}{V_1^o} = -\frac{z^{-1/2}}{1-z^{-1}} \cdot \frac{1-\beta}{\beta} = -\frac{z^{-1/2}}{1-z^{-1}} \cdot \frac{C_S}{C_F} \qquad (A.12a)$$

being an inverting LDI integrator, and

$$H^{oo} = \frac{V_3^o}{V_1^o} = -\frac{1}{1-z^{-1}}\frac{1-\beta}{\beta} = -\frac{1}{1-z^{-1}}\frac{C_S}{C_F} \qquad (A.12b)$$

which is an inverting Backward Euler integrator.

Compared with this ideal case the pole of the transfer function at z=1 is somewhat shifted in the direction of the origin to $z \approx 1 - \frac{C_S}{A_o C_F}$, so the actual integrator is damped. This effects the amplitude and phase characteristics for very low frequencies only.
Furthermore H^{oo} appears to have a zero in the vicinity of the origin at

$$z \approx -\beta\, e^{-\frac{T}{2\tau_o}} \approx -\frac{C_F}{C_S+C_F}\, e^{-\frac{\omega_u T}{2}\frac{C_F}{(C_S+C_F)}}, \qquad (A.13)$$

which causes a maximum gain deviation by a factor of

$$1+\frac{C_F}{C_S+C_F}\, e^{-\omega_u T \frac{C_F}{2(C_S+C_F)}}. \qquad (A.14)$$

Furthermore there is an almost frequency independent decrease of the gain by a factor of

$$1 - \frac{1 + \frac{C_S}{2C_F}}{A_o} - \frac{C_S}{C_S+C_F} e^{\frac{-\omega_u TC_F}{2(C_S+C_F)}} \qquad \text{(A.15a)}$$

for H^{oe}, and of

$$1 - \frac{1 + \frac{C_S}{2C_F}}{A_o} - \frac{C_S+2C_F}{C_S+C_F} e^{\frac{-\omega_u TC_F}{2(C_S+C_F)}} \qquad \text{(A.15b)}$$

for H^{oo}.

When $A_o >> 1$ and $\omega_u T >> 1$ these non-idealities have little effect. For instance for $A_o = 1000$, $\omega_u T = 2\pi * 5$ and $C_S = C_F = 1$ the pole at z=1 is shifted to 0.999 due to the finite DC gain; the transmission zero for H^{oo} is at z= -0.0002, causing a gain deviation of 0.0017 dB maximum; the overall gain decrease is 0.015 dB for H^{oe} and 0.018 dB for H^{oo}.

APPENDIX B

ELEMENTARY SC CIRCUITS WITH FINITE GAIN AMPLIFIERS

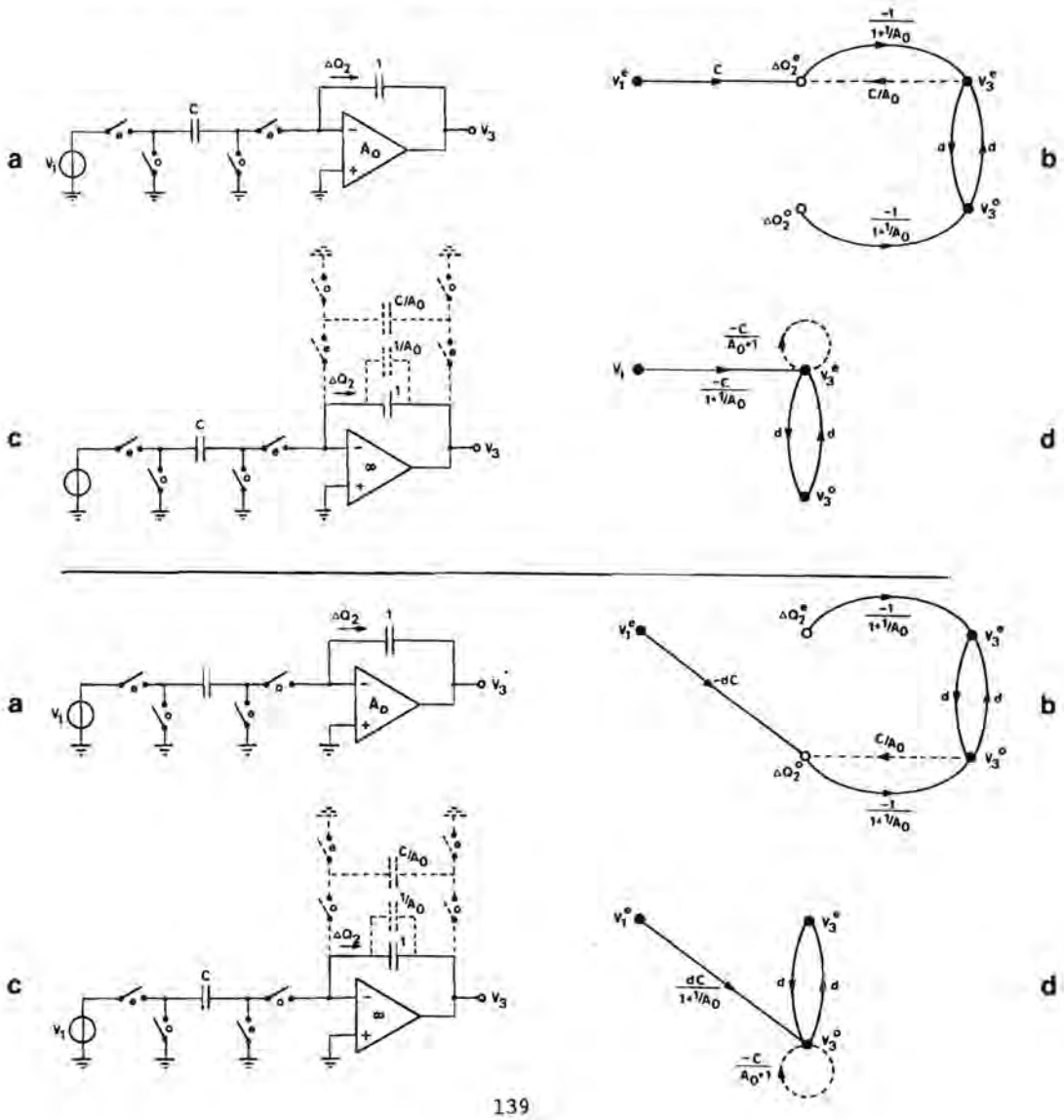
a: elementary SC circuits, comprising finite gain amplifiers

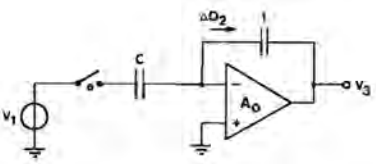
b: corresponding SFG's

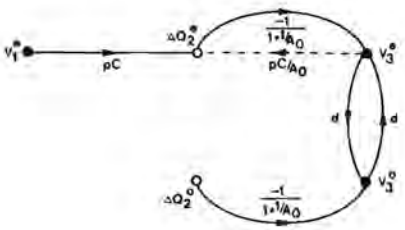
c: representation with virtual capacitors

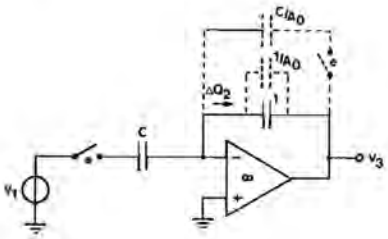
d: SFG's with charge-increment nodes eliminated

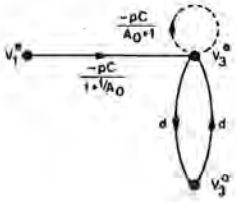
(clock-phases 'e' and 'o' may be mutually interchanged)

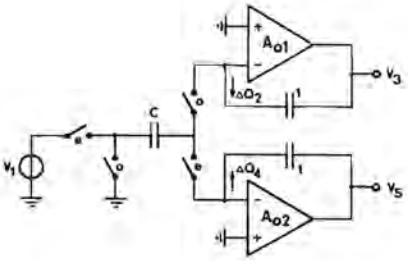


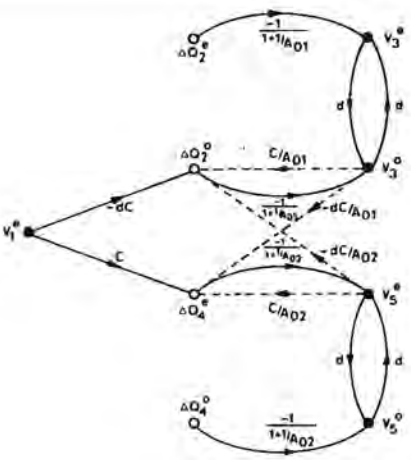

a
C
A_0
V_1
V_3
ΔQ_2
1

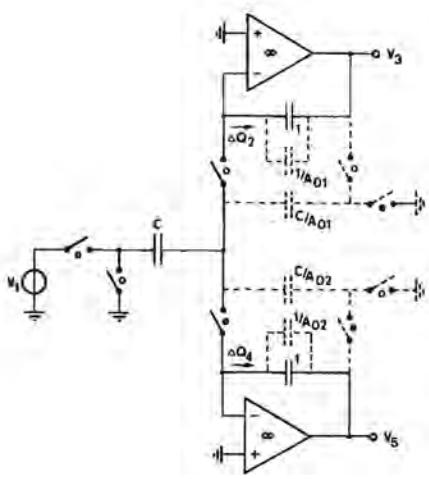

b
V_1^e
ΔQ_2^e
pC
$\frac{-1}{1+1/A_0}$
pC/A_0
V_3^e
d
V_3^o
ΔQ_2^o

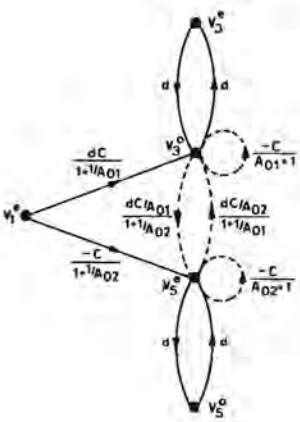

c
C
C/A_0
$1/A_0$
ΔQ_2
V_1
V_3

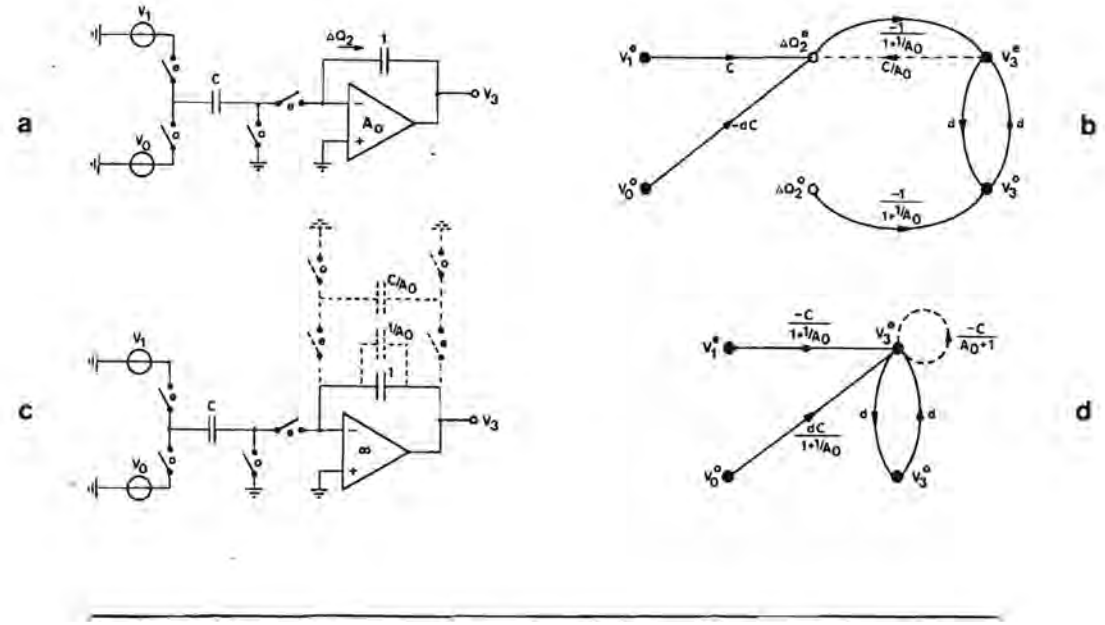

d
V_1^e
$\frac{-pC}{A_0+1}$
$\frac{-pC}{1+1/A_0}$
V_3^e
d
V_3^o

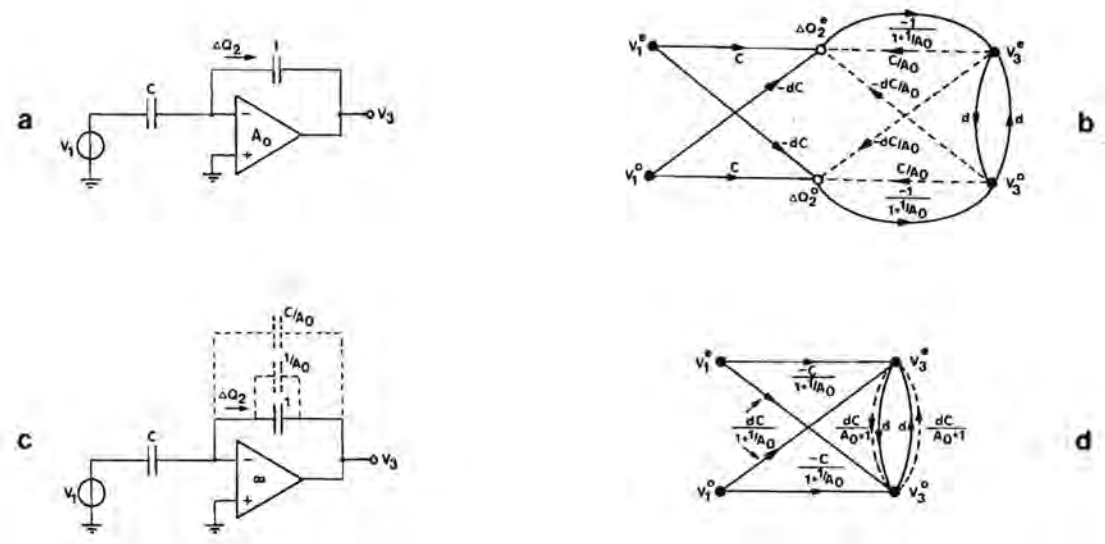

a
C
A_{01}
A_{02}
V_1
V_3
V_5
ΔQ_2
ΔQ_4
1


b
V_1^e
ΔQ_2^e
$\frac{-1}{1+1/A_{01}}$
V_3^e
d
ΔQ_2^o
C/A_{01}
V_3^o
-dC
$-dC/A_{01}$
C
$-dC/A_{02}$
ΔQ_4^e
C/A_{02}
V_5^e
ΔQ_4^o
$\frac{-1}{1+1/A_{02}}$
V_5^o


c
C
V_1
V_3
V_5
ΔQ_2
ΔQ_4
$1/A_{01}$
C/A_{01}
C/A_{02}
$1/A_{02}$
1


d
V_3^e
d
V_3^o
$\frac{dC}{1+1/A_{01}}$
$\frac{-C}{A_{01}+1}$
V_1^e
$\frac{dC/A_{01}}{1+1/A_{02}}$
$\frac{dC/A_{02}}{1+1/A_{01}}$
$\frac{-C}{1+1/A_{02}}$
V_5^e
$\frac{-C}{A_{02}+1}$
V_5^o


a
b
c
d
V_1
V_0
V_3
C
A_0
ΔQ_2
1
C/A_0
$1/A_0$
∞
V_1^e
V_0^e
V_3^e
ΔQ_2^e
V_1^o
V_0^o
V_3^o
ΔQ_2^o
-dC
d
$\frac{-1}{1+1/A_0}$
$\frac{C/A_0}{1+1/A_0}$
$\frac{-C}{1+1/A_0}$
$\frac{-C}{A_0+1}$
$\frac{dC}{1+1/A_0}$


a
b
c
d
V_1
V_3
C
A_0
ΔQ_2
1
C/A_0
$1/A_0$
∞
V_1^e
V_3^e
ΔQ_2^e
V_1^o
V_3^o
ΔQ_2^o
-dC
$-dC/A_0$
d
$\frac{-1}{1+1/A_0}$
$\frac{C/A_0}{1+1/A_0}$
$\frac{dC}{1+1/A_0}$
$\frac{dC}{A_0+1}$
$\frac{-C}{1+1/A_0}$

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SAMENVATTING.

Al sinds de twintiger jaren worden er op industriële schaal audiofrekewente elektrische filters geproduceerd. Aanvankelijk waren dit voornamelijk passieve circuits, opgebouwd uit spoelen, condensatoren en weerstanden. In de zestiger jaren kwamen ook actieve filters in de handel. Deze bevatten geen spoelen meer, die duur, groot en zwaar waren, maar als nieuw (actief) element operationele versterkers. Deze versterkers werden aanvankelijk nog uit discrete componenten opgebouwd, maar sinds het begin van de zeventiger jaren werd er meer en meer gebruik gemaakt van operationele versterkers op één chip. Deze werden gecombineerd met dunne-film weerstanden en condensatoren tot dunne-film hybride geïntegreerde filterschakelingen. O.a. door verbeteringen in de processing werden de afmetingen van deze filters steeds verder gereduceerd, maar het werkelijk op één chip integreren van deze 'actieve RC' filters stuitte op een aantal problemen. Geïntegreerde weerstanden hadden bijvoorbeeld het probleem van een aanzienlijke niet-lineariteit en temperatuurafhankelijkheid. Afgezien van deze effekten was de reproduceerbaarheid van deze weerstanden slecht: gedacht moet worden aan toleranties van tientallen procenten. De niet-lineariteit en temperatuurcoëfficiënt van geïntegreerde condensatoren was aanzienlijk beter, maar hun absolute tolerantie was, net als die van de weerstanden, onacceptabel hoog. Aangezien de karakteristieke frequenties van deze filters bepaald werden door produkten van weerstands- en capaciteitswaarden, waren er grote problemen met het produceren van nauwkeurige filters van dit type. Een van de oplossingen om toch kwalitatief goede filters op één chip te produceren werd gevonden in het toepassen van geschakelde capaciteiten. David Fried toonde in een publikatie in 1972 aan dat door condensatoren te combineren met MOS-transistoren, die m.b.v. een klokgenerator als schakelaars gebruikt werden, filters konden worden gerealiseerd. De geschakelde capaciteiten fungeerden hier, net als weerstanden, als ladings-transporteurs, zij het dat in plaats van een continue ladingsstroom er nu sprake was van discrete ladingspakketjes. De karakteristieke grootheden van deze filters bleken niet bepaald te worden door onnauwkeurige RC-produkten, maar door de frequentie van de klokgenerator en verhoudingen van capaciteiten. Alhoewel de absolute

nauwkeurigheid van geïntegreerde condensatoren slecht was, waren de toleranties in de capaciteitsverhoudingen op één chip orde grootten beter. Wel was er nog het probleem van de parasitaire capaciteiten die op een bepaald niet verwaarloosbare wijze de filterfunctie beïnvloedden. Aan het eind van de zeventiger jaren kwamen er ontwerpen voor filters met geschakelde capaciteiten die ook dit bezwaar omzeilden, door gebruik te maken van strooi-capaciteit-ongevoelige configuraties. Sindsdien hebben deze filters een stormachtige ontwikkeling doorgemaakt en vormen op dit moment een belangrijk industrieel produkt. Redenen voor hun succes zijn o.a. de lage produktiekosten, mede doordat het benodigde chip-oppervlak voor deze filters klein is en zij in een standaard MOS-proces te produceren zijn, hun geringe vermogensdissipatie, hun hoge nauwkeurigheid, de eenvoudige verstembaarheid door wijziging van de klokfrequentie en de mogelijkheid om deze filters te combineren met digitale circuits op één en dezelfde chip.

Veel ontwerpen van filters met geschakelde capaciteiten zijn duidelijk afgeleid van tijdcontinue equivalente filters. Gezien de geschetste historische achtergrond hoeft dit niet te verbazen. Filterontwerpers en netwerk theoretici bezaten met betrekking tot tijdcontinue filters al een grote hoeveelheid kennis en ervaring, die ook benut werd bij de synthese van filters met geschakelde capaciteiten.

In dit proefschrift wordt gepoogd om als uitgangspunt voor de synthese van filters met geschakelde capaciteiten niet reeds bestaande tijdcontinue concepten te gebruiken, maar van de mogelijkheden en onmogelijkheden van geschakelde capaciteiten zelf uit te gaan.

Alvorens dit verder uit te werken, worden in hoofdstuk 2 in het kort enige elementaire transformatiemethoden beschreven, waar in de overige hoofdstukken weer gebruik van wordt gemaakt. Bovendien wordt een beschrijving gegeven van de opbouw van 'dubbel-poly' condensatoren, zoals deze door de Eindhovense Fabricage Faciliteit voor IC's (EFFIC) worden geproduceerd.
In hoofdstuk 3 komen een aantal analysemethoden aan bod. Enerzijds worden de lezer hiermee methoden aangereikt om de schakelingen, zoals

gebruikt in dit proefschrift, te analyseren. Anderzijds kan analyse opgevat worden als de inverse van synthese: door analysemethoden te bestuderen kan inzicht verkregen worden over synthese. Een van de beschreven analysemethoden zal dan ook een belangrijk hulpmiddel blijken voor de ontwikkelde synthesemethoden.
Gestreefd is naar synthesemethoden die inherent zouden moeten leiden tot filterstructuren, die ongevoelig zijn voor strooi-capaciteiten. Om de complexiteit van dit synthese probleem te beperken, is uitgegaan van schakelingen met twee-fasen klokcircuits. Deze beperking is niet in strijd met de interesse van de industrie: een overgrote meerderheid van de industrieel geproduceerde filters is gebaseerd op een dergelijk eenvoudig klokcircuit. Vanzelfsprekend bestaat er altijd de mogelijkheid om te onderzoeken in hoeverre deze aanpak is uit te breiden tot circuits met meer klokfasen.
In hoofdstuk 4 worden als uitgangspunt voor deze synthese de voldoende voorwaarden van Hasler voor strooi-capaciteit ongevoelige schakelingen gebruikt. Het blijkt echter dat naast de klasse van knooppunten, welke voldoen aan deze voorwaarden, onder bepaalde omstandigheden ook 'zwevende' knooppunten mogen worden toegestaan, zonder dat de schakeling zijn ongevoeligheid voor strooi-capaciteiten verliest. Daarom wordt gebruik gemaakt van wat hier 'uitgebreide Hasler voorwaarden' genoemd worden. Door van basiscircuits te eisen dat zij aan deze voorwaarden voldoen en verder overbodige bouwstenen te vermijden, blijkt de verzameling van toegestane elementaire schakelingen bijzonder klein te zijn.
De uitgebreide Hasler voorwaarden blijken zeer fraai aan te sluiten op de voorwaarden waaronder de eenvoudigste van de in hoofdstuk 3 behandelde analysemethoden, welke gebruik maakt van 'Signal Flow Graphs' mag worden toegepast. Daarom wordt nader gekeken naar deze methode, waarbij blijkt dat deze nog verder vereenvoudigd kan worden en daarmee uitstekend geschikt is gemaakt voor synthese doeleinden.
In dit stadium is het synthese probleem van filters met geschakelde capaciteiten met strooi-capaciteit ongevoeligheid en twee-fasen klok gereduceerd tot het probleem van het samenstellen van een geschikte graaf uit takken, afkomstig uit een zeer beperkte verzameling.
Hoofdstuk 4 wordt afgesloten met de beschrijving van twee hierop gebaseerde synthesemethoden.

In hoofdstuk 5 wordt de derde en meest belangrijke methode beschreven, waarin gebruik gemaakt wordt van wat hier 'strooi-capaciteit ongevoelige ontwerp grafen' ('Strays-insensitive Design Graphs' of SDG's) genoemd worden. Ontwerp-voorbeelden worden gegeven, gekeken wordt naar gevoeligheids eigenschappen van deze filters en methoden worden beschreven voor synthese met versterkers met een matige versterking. De beschouwde synthesemethode is algoritmiseerbaar en daardoor zeer geschikt voor geautomatiseerd filter ontwerp. Een ander voordeel is het feit dat geen tijdcontinu prototype filter ontworpen hoeft te worden. De gegenereerde schakelingen bezitten precies genoeg vrijheidsgraden om de uitstuurbaarheid te optimaliseren en de totale benodigde capaciteit te minimaliseren. Met uitzondering van een kleine klasse van overdrachtsfuncties is de beschreven methode canoniek in het aantal benodigde versterkers. Voor een meerderheid aan overdrachtsfuncties is het niet nodig de beschikking te hebben over een ingangssignaal dat 'bevroren' is gedurende een hele klokperiode. Dit in tegenstelling tot een groot aantal andere filterontwerpen. Anderzijds bezit het uitgangssignaal wel deze eigenschap, hetgeen het cascaderen van filterschakelingen vereenvoudigt. De verkregen filterstructuren bezitten geen vertragingsvrije lussen waarin meer dan één versterker is opgenomen, hetgeen ten goede komt aan de stabiliteit van deze schakelingen. Bovendien blijken de gegenereerde filters goede gevoeligheids eigenschappen voor capaciteitsafwijkingen, eindige versterking en eindige bandbreedte van de toegepaste opamps te bezitten.
In hoofdstuk 6 wordt de SDG methode vergeleken met een aantal algemeen aanvaarde synthesemethodieken.

Hoofdstuk 7 vormt een afzonderlijk deel van dit proefschrift, waarin een 'Equivalente Immittantie Converter' (EIC) beschreven wordt. Deze bouwsteen voor filters met geschakelde capaciteiten is vergelijkbaar met een 'Gegeneraliseerde Immittantie Converter' (GIC), bekend uit de tijdcontinue filtersynthese. Deze EIC is zeer eenvoudig van structuur en leidt tot filters die kunnen worden opgebouwd uit slechts een gering aantal componenten. Als voorbeeld wordt een 4e orde Butterworth laagdoorlaat filter beschreven, dat daadwerkelijk als NMOS geïntegreerd circuit is gerealiseerd. De EIC schakeling is ongevoelig

voor de belangrijkste strooi-capaciteiten: de zgn. bodemplaat parasieten. Voor een aantal andere strooi-capaciteiten is er wel nog sprake van gevoeligheid, maar zoals wordt aangetoond kunnen deze gecompenseerd worden. Een interessante eigenschap van deze bouwsteen is het feit, dat het eindig zijn van de versterking van de gebruikte opamp volledig kan worden gerepresenteerd door een uitwendig, passief circuit.

Als afsluiting worden in hoofdstuk 8 een aantal conclusies getrokken en suggesties gedaan voor een voortzetting van het beschreven werk.

Alhoewel de kaft van dit proefschrift maar één naam vermeldt, hebben meerdere mensen een bijdrage geleverd aan de totstandkoming hiervan. Met name wil ik daarom mijn promotor prof. Wim van Bokhoven bedanken, ondermeer voor het feit dat ik nooit tevergeefs een beroep op hem heb hoeven doen. Verder mijn tweede promotor, prof. J.A.G. Jess en de andere leden van de promotiecommissie voor de discussies over de inhoud van dit proefschrift en de bruikbare aanwijzingen. Frans Bakker en Wim Verhoeven wil ik heel hartelijk danken voor het geduld en de nauwgezetheid waarmee zij de tekeningen verzorgd hebben, Linda Balvers voor de morele steun en alle kollega's van mijn vakgroep voor de uitstekende sfeer en de wijze waarop ik tijdens de laatste maanden van mijn promotiewerk door hen ben ontzien. Ook de kollega's van de vakgroep Elektronische Bouwstenen en de medewerkers van de EFFIC wil ik bedanken voor de plezierige samenwerking. En bovenal mijn vrouw Marti en onze kinderen Stan en Ledje, die voor mij de drijfveer zijn geweest.

Curriculum Vitae

De schrijver van dit proefschrift werd geboren op 30 juni 1952 te Amsterdam. Juni 1974 behaalde hij het diploma Elektrotechniek aan de Hogere Technische School te 's Hertogenbosch. Na zijn dienstplicht te hebben vervuld begon hij zijn studie aan de afdeling Elektrotechniek van de Technische Hogeschool te Eindhoven. December 1982 behaalde hij aldaar met lof het diploma Elektrotechnisch Ingenieur. Mei 1983 trad hij als Wetenschappelijk Assistent in tijdelijke dienst bij de vakgroep Elektronische Schakelingen van de Technische Hogeschool te Eindhoven. Sinds januari 1987 is hij als Universitair Docent aan deze vakgroep verbonden.

STELLINGEN BIJ HET PROEFSCHRIFT VAN

J.A. HEGT

28 juni 1988

VIII

Bij het doceren is de overdracht van interesse minstens zo belangrijk als de overdracht van kennis.

IX

De feitelijke kopieerbeveiliging van veel software bestaat eruit dat niet alleen de diskettes, maar ook de bijbehorende handleidingen gekopieerd moeten worden.

X

Het direct na een tentamen laten invullen van een vragenlijst t.b.v. onderwijsevaluatie door studenten gaat ten koste van de objectiviteit van de antwoorden.

XI

De mens onderscheidt zich van het dier door onder andere de graad van mechanisatie van zijn beestachtigheden.