A 14bit 200 MS/s DAC with SFDR>78 dBc, IM3

A 14 bit 200 MS/s DAC With SFDR $>$78 dBc, IM3 <-83 dBc and NSD <-163 dBm/Hz Across the Whole Nyquist Band Enabled by Dynamic-Mismatch Mapping

Yongjian Tang, Joost Briaire, Kostas Doris, Robert van Veldhoven, Pieter C. W. van Beek, Hans Johannes A. Hegt, *Senior Member, IEEE*, and Arthur H. M. van Roermund, *Senior Member, IEEE*

***Abstract*—This paper presents a 14 bit 200 MS/s current-steering DAC with a novel digital calibration technique called dynamic-mismatch mapping (DMM). By optimizing the switching sequence of current cells to reduce the dynamic integral nonlinearity in an I–Q domain, the DMM technique digitally calibrates all mismatch errors so that both the DAC static and dynamic performance can be significantly improved in a wide frequency range. Compared to traditional current source calibration techniques and static-mismatch mapping, DMM can reduce the distortion caused by both amplitude and timing mismatch errors. Compared to dynamic element matching, DMM does not increase the noise floor since the distortion is reduced, not randomized. The DMM DAC was implemented in a 0.14 μm CMOS technology and achieves a state-of-the-art performance of SFDR $>$ 78 dBc, IM3 <-83 dBc and NSD <-163 dBm/Hz in the whole 100 MHz Nyquist band.**

***Index Terms*—Calibration, digital-to-analog converter (DAC), dynamic-mismatch mapping (DMM), error measurement, mapping, mismatch, mismatch sensor, switching sequence, timing error.**

I. Introduction

EMERGING wireless and wireline communication standards exploiting wideband and multicarrier modulation, e.g., in base stations, demand lower signal distortion and noise to improve signal quality and system capacity. Since a digital-to-analog converter (DAC) acts as an interface between digital baseband and RF front-end, it is the first analog signal generator in a transceiver transmitting path and determines the maximal performance achievable in the whole system. Moreover, in those applications, dynamic performance of the DAC, such as SFDR, IM3 and NSD, are more important and concerned than its static performance.

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Y. Tang was with the Department of Electrical Engineering, Eindhoven University of Technology, 5600MB Eindhoven, The Netherlands. He is now with NXP Semiconductors, 5656AG Eindhoven, The Netherlands (e-mail: jimmy.tong@gmail.com).

J. Briaire, K. Doris, R. van Veldhoven, and P. C. W. van Beek are with NXP Semiconductors, 5656AG Eindhoven, The Netherlands.

H. J. A. Hegt and A. H. M. van Roermund are with the Department of Electrical Engineering, Eindhoven University of Technology, 5600MB Eindhoven, The Netherlands.

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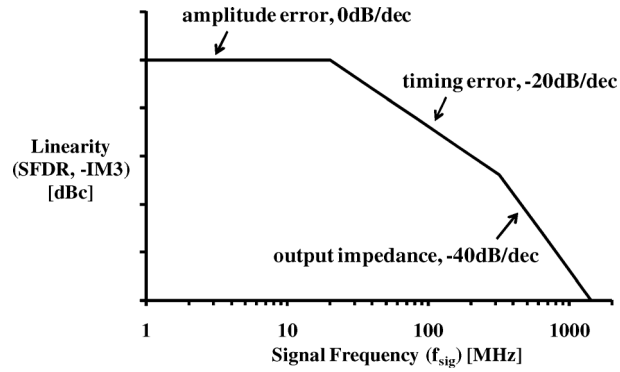

Fig. 1. Typical DAC linearity versus signal frequencies ($f_{\rm sig}$).

Current-steering is a suitable architecture for high-speed high-performance DACs because of its intrinsic high speed and driving capability for a typical 50 Ω load. It consists of a certain number of binary- and thermometer-weighted switched-current cells that are controlled by the input digital word. Though the architecture is simple, the performance is limited by many error sources [1]–[4]. Fig. 1 shows how the DAC linearity is typically affected by various errors when the signal frequency $f_{\rm sig}$ changes. At very low $f_{\rm sig}$ or sampling frequency $f_{\rm s}$, the linearity is determined by current amplitude mismatch errors of current cells. Since the amplitude error is a static error, its effect does not scale with frequency as shown in Fig. 1. However, the effect of timing mismatch error during cell switching does scale with frequency. With frequency increasing, the timing error becomes more visible and starts to dominate the linearity above tens of MHz, showing a -20 dB/decade roll-off with $f_{\rm sig}$ when keeping the same ratio of $f_{\rm sig}/f_{\rm s}$ [1]. With increasing $f_{\rm sig}$ even to hundreds of MHz, the effect of the finite output impedance of current cells will dominate the linearity with a -40 dB/decade roll-off [4]. In most applications, the signal frequency $f_{\rm sig}$ is from DC to hundreds of MHz where mismatch errors typically dominate the linearity. In order to achieve a good performance within a wide signal bandwidth, both amplitude and timing mismatch errors have to be reduced.

Mismatch error is a result of process local variations, layout asymmetry and IR imbalance in current sources, switches, latches, supplies, clock distribution, etc. [1]–[3]. For a certain technology node, there is a limit to how much mismatch errors can be reduced by intrinsic DAC design with reasonable chip

area and power consumption [1]. For instance, the area of current sources has to be 4x larger for one additional bit in static matching accuracy, while a fast switching transition is required to reduce timing errors, which translates to increased power consumption. Calibration techniques have been developed to overcome these limitations. Traditional calibration techniques, such as current source calibration [3], [5]–[9] and static-mismatch mapping (SMM) [10]–[13], only address the reduction of amplitude errors. However, as frequencies increase, the effect of timing errors will dominate that of amplitude errors. Thus, the improvement on the DAC dynamic performance will become negligible if only amplitude errors are addressed. Moreover, unlike amplitude errors, timing errors are far more difficult to be reduced by intrinsic circuit design, even with high power consumption in latches and symmetrical layout [1]. Dynamic element matching (DEM) is a well-known technique that randomizes signal-dependent distortion caused by both amplitude and timing errors such that the linearity is improved, but at the cost of a significantly increased noise floor [14].

In this work, a novel digital calibration technique called dynamic-mismatch mapping (DMM) is presented. With DMM, the effect of both amplitude and timing errors can be calibrated so that both DAC static and dynamic performance can be significantly improved without increasing the noise floor. The DMM technique is validated on a 14 bit 200 MS/s Nyquist current-steering DAC.

This paper is organized as follows. In Section II, the relationship between the matching of switched-current cells and the DAC dynamic nonlinearity is evaluated by introducing two new parameters, dynamic-INL and dynamic-DNL. In Section III, the DMM technique is introduced. The chip implementation and measurement results as well as a comparison with previously published work are discussed in Sections IV and V. Finally, conclusions are given in Section VI.

II. Dynamic Differential and Integral Nonlinearity

A. Dynamic Mismatch of Current Cells

In current-steering DACs, static-mismatch errors are known as DC amplitude errors of current cells. However, in applications with high signal and sampling frequencies, the current cell is used as a switched-current cell rather than a static current source. At high frequencies, the DAC dynamic performance, such as SFDR and IM3, is dominated by the dynamic switching behavior of current cells instead of by their static behavior. The mismatch between the dynamic switching behaviors of current cells, including both amplitude and timing errors, is called dynamic-mismatch error, as shown in Fig. 2(a). Obviously, compared to static mismatch, dynamic mismatch represents the matching of switched-current cells more completely and accurately.

Static-mismatch errors can be easily measured in the time domain using a current comparator or an ADC [3], [5]–[8], [10], while dynamic-mismatch errors can be measured more efficiently in the frequency domain. By digitally switching a current cell as square-wave output at modulation frequency $f_{\rm m}$, its dynamic-mismatch error appears as vector errors ($\rm E_{fm}$, $\rm E_{2fm}$, etc.) at all harmonic frequencies, as shown in the frequency and I-Q domain in Fig. 2(b)–(c). Due to the property of a square wave, mismatch errors ($\rm E_{fm}$, $\rm E_{2fm}$) at fundamental and second harmonic frequencies are the two most dominant errors that already include all amplitude and timing error information: $\rm E_{fm}$ is mainly determined by amplitude and timing delay errors, while $\rm E_{2fm}$ is mainly determined by amplitude and timing duty-cycle errors. In general, dynamic-mismatch errors are not limited to amplitude and timing errors. Since they are measured as a combined mismatch effect in the frequency domain, all mismatch errors, including impedance mismatch, are included.

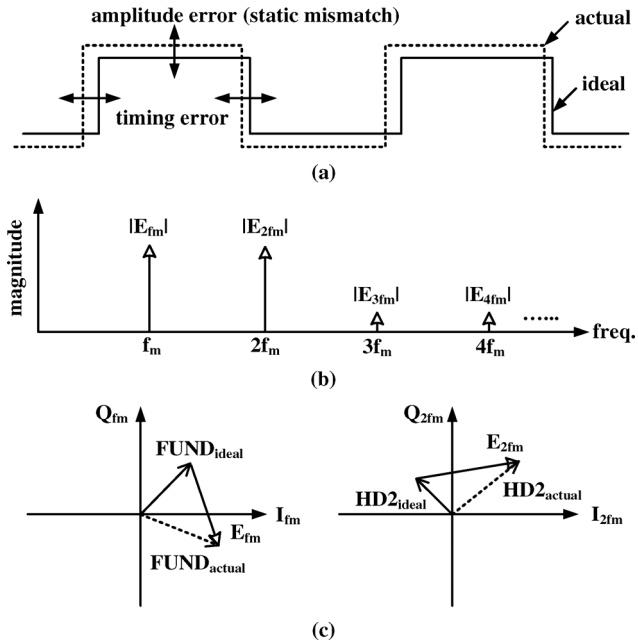

Fig. 2. Dynamic-mismatch error in the time, frequency and I-Q domain. (a) Dynamic-mismatch error in the time domain. (b) Dynamic-mismatch error in the frequency domain. (c) Dynamic-mismatch error in the I-Q plane.

B. Dynamic-INL and Dynamic-DNL

Traditional differential nonlinearity (DNL) and integral nonlinearity (INL) are based on the static transfer function of the DAC, and are the parameters to evaluate its static performance. However, since both amplitude and timing errors together contribute to the dynamic-mismatch error, just INL and DNL are not enough to evaluate the matching performance of current cells. Dynamic performance parameters, such as SFDR and IM3, only show a consequence of mismatch errors, but do not show the fundamental relationship between the DAC linearity and mismatch errors. In this section, two new parameters, called dynamic integral nonlinearity (dynamic-INL) and dynamic differential nonlinearity (dynamic-DNL), are introduced to evaluate the dynamic matching of current cells and the DAC linearity.

Dynamic-INL/DNL can be derived from a DAC transfer function that is based on dynamic-mismatch errors versus the digital input code. This transfer function is called dynamic transfer function. As the digital input is increased from zero to full-scale, instead of evaluating the static transfer function by sequentially turning on unit current cells as DC-current outputs, for evaluating the dynamic transfer function, all unit current cells are sequentially turned-on and modulated as

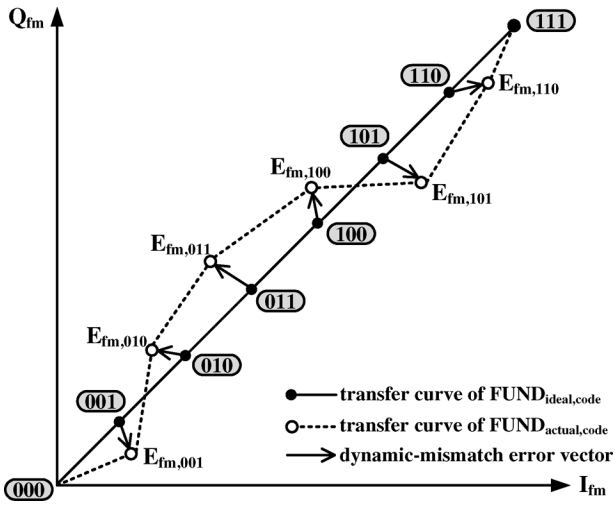

Fig. 3. Two-dimensional dynamic transfer curve of the fundamental component of a 3-bit modulated DAC output.

square-wave outputs at modulation frequency $f_{\rm m}$. In other words: for the static transfer function, the DAC output is a summed DC current of current cells, while for the dynamic transfer function, the DAC output is a sum of the modulated square-wave output of current cells. Fig. 3 shows its ideal and actual dynamic transfer functions of the fundamental component of the modulated DAC output in the I-Q plane taking a 3-bit thermometer-coded DAC as an example. As shown, in the ideal case, when the input code is increased from 000 to 111, the fundamental component ($\mathrm{FUND_{ideal,code}}$) of the DAC output linearly increases in magnitude, but keeps the same phase. However, in the actual case, due to amplitude and timing errors, the fundamental component ($\mathrm{FUND_{actual,code}}$) has a nonlinear increase in magnitude and has also a varying phase. $\mathrm{E_{fm,code}}$ is the integral dynamic-mismatch error of the fundamental component at a given code input, and it equals the sum of $\mathrm{E_{fm}}$ of all turned-on current cells at that code input, given as

$$\begin{aligned}\mathrm{E_{fm,code}} &= \mathrm{FUND_{actual,code}} - \mathrm{FUND_{ideal,code}} \\ &= \sum_{\mathrm{i}=1}^{\mathrm{code}} \mathrm{E_{fm,i}} \qquad (\mathrm{code} = 0 \ldots \text{full-scale}) \end{aligned} \tag{1}$$

where $\mathrm{E_{fm,i}}$ is the dynamic-mismatch error $\mathrm{E_{fm}}$ of the ith current cell as defined in Section II-A. The same definition can be used for the integral dynamic-mismatch error $\mathrm{E_{2fm,code}}$ of the second harmonic component. As mentioned before, $\mathrm{E_{fm}}$ and $\mathrm{E_{2fm}}$ already include all mismatch information and are the most dominant two errors. Therefore, similar to the traditional INL, the dynamic-INL is defined as the maximum RMS value of the summed power of $\mathrm{E_{fm,code}}$ and $\mathrm{E_{2fm,code}}$ over the power of the fundamental component of the modulated square-wave output of one ideal LSB cell, as shown below:

$$\text{dynamic-INL} = \max\left(\sqrt{\frac{|\mathrm{E_{fm,code}}|^2 + |\mathrm{E_{2fm,code}}|^2}{|\mathrm{FUND_{ideal,1LSB}}|^2}}\right) \mathrm{LSB}, \quad \mathrm{code} = 0 \ldots \text{full-scale}. \tag{2}$$

Similar to the dynamic-INL, the dynamic-DNL is defined as shown in (3) at the bottom of the page.

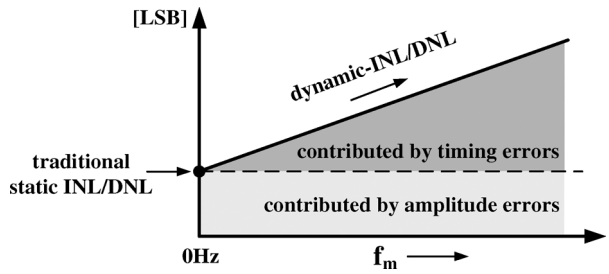

Fig. 4. Dynamic-INL/DNL versus modulation frequency ($f_{\rm m}$).

C. Dynamic-INL/DNL Versus Traditional Static INL/DNL

Compared to the traditional static INL/DNL used to evaluate the static matching of current cells, the dynamic-INL/DNL includes all mismatch errors to evaluate the dynamic matching of current cells. Both static and dynamic switching behaviors are evaluated by these two parameters. Thus, the dynamic-INL/DNL describes the matching of switched-current cells more completely than the INL/DNL. By minimizing the dynamic-INL/DNL, the impact of both amplitude and timing error are reduced so that both DAC static and dynamic performance can be improved.

By definition, the dynamic-INL/DNL are parameters not only related to mismatch errors, but also modulation-frequency-dependent. Fig. 4 shows an example of a dynamic-INL/DNL as $f_{\rm m}$ increases. As seen, when $f_{\rm m}$ is zero, the dynamic-INL/DNL are equal to the INL/DNL, respectively. This is obvious because at $f_{\rm m} = 0$ Hz, the dynamic-INL/DNL are determined only by amplitude errors, and the modulated square-wave used to measure the dynamic-INL/DNL becomes a "DC" signal which is the same situation in measuring the static INL/DNL. As $f_{\rm m}$ increases, timing errors become more and more dominant in the dynamic-INL/DNL. In summary, when $f_{\rm m}$ changes, the weight between amplitude and timing errors in dynamic-mismatch errors changes, resulting in a frequency-dependent dynamic-INL/DNL. How to improve the DAC performance by reducing the dynamic-INL/DNL will be discussed in Section III.

$$\text{dynamic DNL} = \max\left(\sqrt{\frac{|\mathrm{E_{fm,code}} - \mathrm{E_{fm,code-1}}|^2 + |\mathrm{E_{2fm,code}} - \mathrm{E_{2fm,code-1}}|^2}{|\mathrm{FUND_{ideal,1LSB}}|^2}}\right) \mathrm{LSB} \tag{3}$$

III. Dynamic-Mismatch Mapping

A. Traditional Mapping

For a thermometer or segmented DAC, the switching sequence of thermometer current cells has a significant impact on the linearity since the performance is typically dominated by the thermometer part [1], [4]. The principle of mapping calibration techniques is digitally optimizing the switching sequence so that the integral nonlinear error is minimized. Existing mapping techniques, such as static-mismatch mapping (SMM) [10]–[13] and timing error mapping [15], [16] can only optimize the switching sequence based on single kind of error, either amplitude or timing. However, the DAC linearity is determined by both amplitude and timing errors, especially at high frequencies. Just mapping amplitude or timing error is not enough to guarantee a good performance over a wide frequency range. In this paper, a novel mapping technique called dynamic-mismatch mapping (DMM) is developed to calibrate all mismatch errors.

B. Dynamic-Mismatch Mapping (DMM)

Instead of the traditional SMM optimizing the switching sequence by reducing the integral static-mismatch error (i.e., INL) which is only based on amplitude errors [10]–[13], the proposed DMM technique improves the performance by reducing the integral dynamic-mismatch error (i.e., dynamic-INL) so that the impact of both amplitude and timing errors can be reduced. The advantage of DMM over SMM is that DMM can improve the DAC performance even at high frequencies, where a significantly less improvement can often be seen in SMM DACs [10]–[13].

DMM reduces the dynamic-INL according to certain criteria. A simple criterion is used in this work as an example: DMM changes the switching sequence of thermometer current cells, such that the dynamic-mismatch error of each cell can be maximally canceled by that of the following cell. More complex criteria may reduce the dynamic-INL even more. However, this simple sorting logic combines an easy hardware implementation with substantial performance improvement. Clearly, if dynamic-mismatch errors ($\mathrm{E_{fm}}$, $\mathrm{E_{2fm}}$) of two cells have to cancel each other, since $\mathrm{E_{fm}}$ and $\mathrm{E_{2fm}}$ are vector signals, they should be canceled in the I-Q plane, respectively. As an example shown in Fig. 5 (for simplicity, only $\mathrm{E_{fm}}$ is shown), the $(\mathrm{i}+1)$th cell following the i-th cell in the switching sequence is found by minimizing the total power of the summed $\mathrm{E_{fm}}$ and $\mathrm{E_{2fm}}$ of these two cells, i.e., find a cell from still unsorted cells such that

$$\begin{aligned}&|\mathrm{E_{fm,i}}+\mathrm{E_{fm,i+1}}|^2+|\mathrm{E_{2fm,i}}+\mathrm{E_{2fm,i+1}}|^2\\&\quad=(\mathrm{I_{fm,i}}+\mathrm{I_{fm,i+1}})^2+(\mathrm{Q_{fm,i}}+\mathrm{Q_{fm,i+1}})^2\\&\qquad+(\mathrm{I_{2fm,i}}+\mathrm{I_{2fm,i+1}})^2+(\mathrm{Q_{2fm,i}}+\mathrm{Q_{2fm,i+1}})^2\end{aligned}\quad(4)$$

is minimal; the $(\mathrm{i}+2)$th, $(\mathrm{i}+3)$th current cells in the switching sequence and so on are found one-by-one from the unsorted current cells by the same principle. The room for optimization reduces during mapping since the number of the unsorted cells become less and less. Therefore, the current cell with the largest error is compensated firstly. By sorting all current cells in this way, the dynamic-INL can be reduced. Moreover, DMM finds the optimized switching sequence based on the relative dynamic-mismatch errors of current cells in the I-Q plane. The absolute values of dynamic-mismatch errors have no effect on finding an optimal switching sequence. Only the relative position of dynamic-mismatch errors in the I-Q plane is the deterministic factor in this calibration technique. Therefore, the circuit requirements for measuring dynamic-mismatch errors, such as offset and reference accuracy, are significantly relaxed.

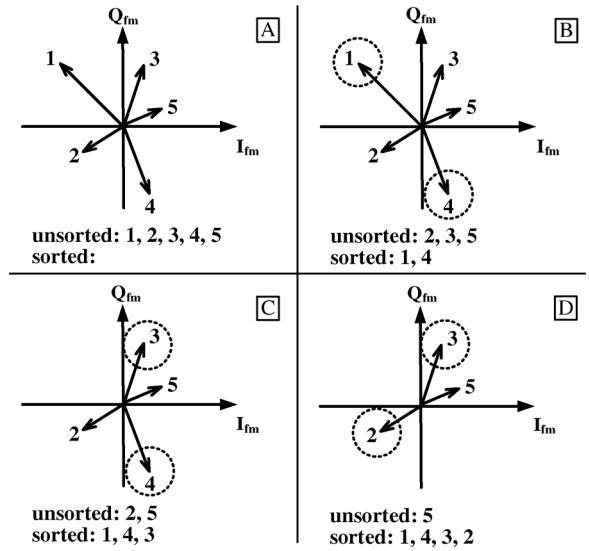

Fig. 5. Dynamic-mismatch mapping, five-cell example.

C. Monte-Carlo Simulations

Monte-Carlo simulations are performed to evaluate the performance improvement by the DMM technique. A 14 bit 200 MS/s 6T-8B segmented DAC is chosen as an example. The amplitude and timing errors of thermometer current cells are assumed to be zero-mean Gaussian distributed with standard deviations of 0.15% (relative to the ideal full-scale output of a current cell) and 5 ps, respectively. As shown in Fig. 4, the dynamic-INL is a curve evaluated with the modulation frequency f_{m} sweeping from DC to high frequency. For practical and simple use of DMM, the mismatch errors and the dynamic-INL are only measured and optimized at a selected f_{m}, called measurement frequency f_{meas}. Obviously, how the wideband DAC performance is improved by DMM depends on how large the mismatch errors are and which f_{meas} is chosen. Figs. 6–8 give the simulated dynamic-INL/DNL and SFDR with 99.7% yield, with or without DMM. Different f_{meas} (chosen as 0 Hz, 5 MHz, 40 MHz, 100 MHz) is chosen in DMM to find the best f_{meas}. Several important phenomena can be observed. As shown in Fig. 6, without mapping, the dynamic-INL at 0 Hz f_{m}, which is equal to the static INL, is 4.9 LSB with 99.7% yield. This is in line with a theoretical model in [17]: the INL with 3σ yield is 4.9 LSB for the total 14-bit accuracy. As f_{m} increases, the dynamic-INL increases showing that the DAC performance will decrease with sampling and signal frequencies.

If the switching sequence is optimized by DMM with $f_{\mathrm{meas}}=0$ Hz, the calibration is only based on amplitude errors and DMM becomes identical to traditional SMM, resulting in an optimized dynamic-INL of 1.9 LSB as shown in Fig. 6.

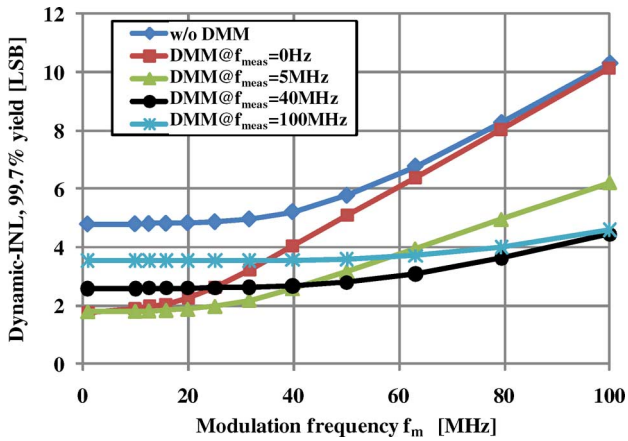

Fig. 6. Dynamic-INL with DMM optimized at different f_{meas}.

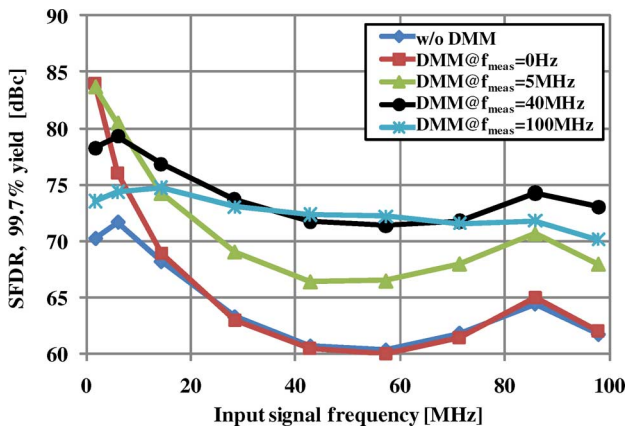

Fig. 7. SFDR with DMM optimized at different f_{meas}.

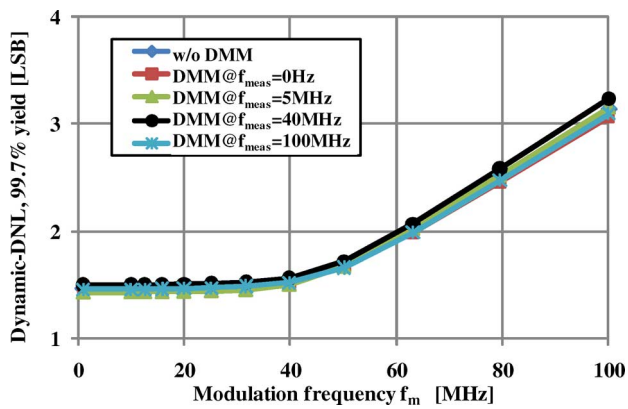

Fig. 8. Dynamic-DNL with DMM optimized at different f_{meas}.

The reduction factor is 2.6, i.e., roughly 1.4 bit benefit, which is a typical value in SMM DACs [10]–[13]. However, this improvement on the dynamic-INL decreases quickly with f_{m} since timing errors are not calibrated. For the SFDR shown in Fig. 7, the 1.4 bit dynamic-INL improvement results in a 14 dB SFDR improvement at very low signal frequencies. While at high signal frequencies where the switching rate of current cells is high, there is no improvement anymore. This limitation is also often seen in SMM DACs [10], [13], which further highlights the necessity of correcting both amplitude and timing errors.

With increasing f_{meas}, the weight of timing errors in the dynamic-mismatch errors increases and the weight of amplitude errors decreases. Thus, the switching sequence optimized by DMM tends to correct more on timing errors and less on amplitude errors. This means that the benefit from correcting amplitude errors is traded with the benefit from correcting timing errors. As shown in Fig. 6, with f_{meas} being increased from 0 to 40 MHz, a little loss in the dynamic-INL improvement at low f_{m} returns a significantly larger improvement at high f_{m}. For example, for DMM@$f_{\mathrm{meas}} = 40$ MHz, the optimized dynamic-INL is 2.5 LSB at low f_{m}, which is 0.6 LSB less improvement than DMM@$f_{\mathrm{meas}} = 0$ Hz and the reduction factor is 1.96 compared to w/o DMM. However, its optimized dynamic-INL is 4.4 LSB at 100 MHz f_{m}, which is 5.8 LSB more improvement than DMM@$f_{\mathrm{meas}} = 0$ Hz and the reduction factor is 2.3 compared to w/o DMM. Therefore, in this example, the DMM with 40 MHz f_{meas} is able to provide one bit performance improvement in a wide frequency range. This is verified by the SFDR results shown in Fig. 7, as f_{meas} increases from 0 to 40 MHz, the optimized SFDR is comparable at very low signal frequencies, but a significantly larger improvement can be achieved at high signal frequencies. Compared to traditional SMM that only improves the SFDR at very low frequencies, the SFDR optimized by DMM@$f_{\mathrm{meas}} = 40$ MHz is increased by around 10 dB across the whole Nyquist band. This advantage will be more attractive at high sampling-rate DACs where the timing error is more dominant.

Further increasing f_{meas} does not help anymore because it continuously decreases the weight on correcting amplitude errors. As shown in Fig. 6, with DMM@$f_{\mathrm{meas}} = 100$ MHz, the improvement on the dynamic-INL is even lower at low f_{m} because amplitude errors are not corrected enough. However, the optimized dynamic-INL shows similar improvements as DMM@$f_{\mathrm{meas}} = 40$ MHz at high f_{m} since timing errors are well corrected. The same situation is valid for the SFDR. The SFDR with DMM@$f_{\mathrm{meas}} = 100$ MHz is worse than with DMM@$f_{\mathrm{meas}} = 40$ MHz. As a result, there is a best weight balance between calibrating amplitude and timing errors, which determines the best f_{meas} used in DMM, e.g., f_{meas} around 40 MHz is a good balance point in this example.

Therefore, for a certain application (i.e., how high the sampling and signal frequencies are) and a certain DAC (i.e., how large its amplitude and timing errors are), f_{meas} has to be properly chosen to maximize the benefit of DMM. Actually, this opens a door to optimize the DAC performance for different applications. For example, more weight on calibrating timing errors for high frequency applications, and more weight on calibrating amplitude errors for low frequency applications. It can also be concluded that there exists no universal best switching sequence, but only the most suitable switching sequence for a defined DAC and application.

Since DMM changes only the switching sequence of current cells, it only reduces the impact of mismatch errors, but not actual mismatch errors. Therefore, the dynamic-DNL stays the same with or without DMM, as shown in Fig. 8. This is also the case for SMM, i.e., just changing the switching sequence will

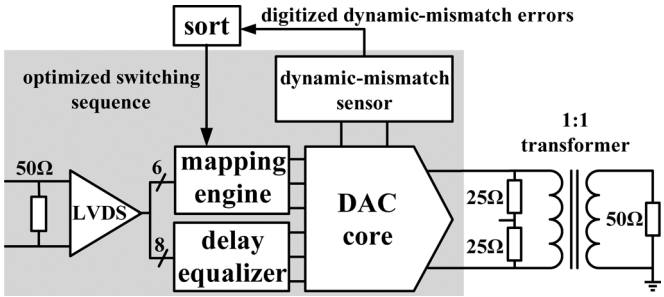

Fig. 9. Architecture of the DMM DAC.

not improve the DNL, as confirmed by SMM DACs in [10], [12], [13].

D. Comparison to Other Calibration Techniques

DMM is a digital calibration technique. It measures analog errors and corrects them in the digital domain. Compared to analog calibration techniques for mismatch errors, such as current source calibration [3], [7], [23], it keeps the analog core clean and compact which is preferred for high speed design. DMM also has fundamental advantages over existing digital calibration techniques, such as SMM [10]–[13] and DEM [14], [18]. Compared to SMM that only improves the performance at very low frequencies, DMM can provide a constant and significant improvement (around 10 dB in theory with a simple sorting algorithm) across the whole Nyquist band even at high sampling frequencies, as long as the mismatch errors are dominant. Compared to DEM, DMM does not increase the noise floor because the mismatch impact is reduced instead of randomized. Moreover, DMM can be on top of many other calibration techniques, such as current source calibration [3], [7], [23], so that the performance can be improved even further.

IV. Chip Implementation

A. Architecture

The strategy for the test chip is starting with a good intrinsic DAC design, and then applying DMM to push the performance even further. Fig. 9 shows the architecture of the 14 bit 200 MS/s DMM DAC. It has a segmented architecture: the six MSBs are implemented as thermometer current cells and the rest are binary cells. This partition is a trade-off between performance, area and power [1], also the calibration complexity. The dynamic-mismatch errors are measured and digitized by an on-chip dynamic-mismatch sensor. An optimized switching sequence of thermometer current cells is achieved with DMM by sorting measured dynamic-mismatch errors. For flexibility, this sorting logic is implemented off-chip in this prototype, but it is simple and easy to be integrated on-chip since it only needs to calculate and compare the values of (4). The computation time for the calibration is typically less than 1 ms. A memory-based mapping engine is used to allow full freedom in programming the switching sequence. The DAC is implemented in a 1.8 V 0.14 μm CMOS baseline technology, and the die photo is shown in Fig. 10. The full-scale current output is 20 mA. Since no thick-oxide transistors were used, the AC voltage output

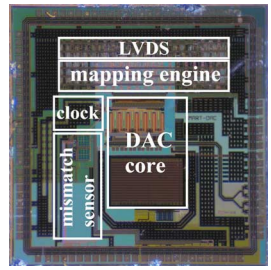

Fig. 10. Die micrograph.

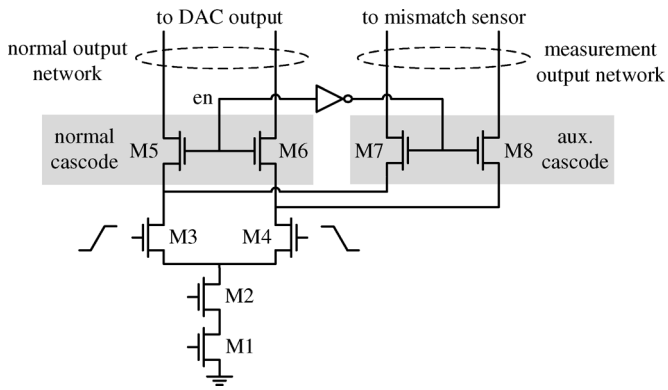

Fig. 11. DAC current cell.

swing is 0.5 V_{ppd} which is limited by 1.8 V transistors, and the maximum power delivered to the 50 Ω transformer load is −2 dBm. Moreover, since the DAC output is current, the linearity is independent of the output voltage swing, as long as the output loading performs a linear I-V conversion and the finite output impedance is not a dominant error source. Solutions to alleviate the limitation of finite output impedance were addressed in [4], [19], and is out of the scope of this work.

B. DAC Core

The current cell in the DAC core is depicted in Fig. 11. It has the same current source array as [20]. Since the output is current, the DAC is often terminated by a low impedance loading, e.g., the ac-equivalent differential 25 Ω in Fig. 9. Therefore, the power of the mismatch error will be weak if it is directly measured at the normal output of the current cell. In order to increase the power of the mismatch error, an auxiliary cascode pair (M7, M8) and a second output network are added to every current cell, so that a higher impedance loading can be connected. This additional output network is called measurement output network, with respect to the normal output network which is low-impedance terminated. This measurement output network is laid out side-by-side with the normal output network in order to have the same delay.

C. Dynamic-Mismatch Sensor

Fig. 12 shows the circuit diagram of the on-chip dynamic-mismatch sensor based on a zero-IF receiver. All current cells are measured one-by-one relative to a reference cell which is an arbitrary chosen cell. The cell to be measured ($cell_i$) and the reference cell ($cell_{ref}$) are switched as square waves with opposite phases that can be shifted digitally by 90° to measure I or

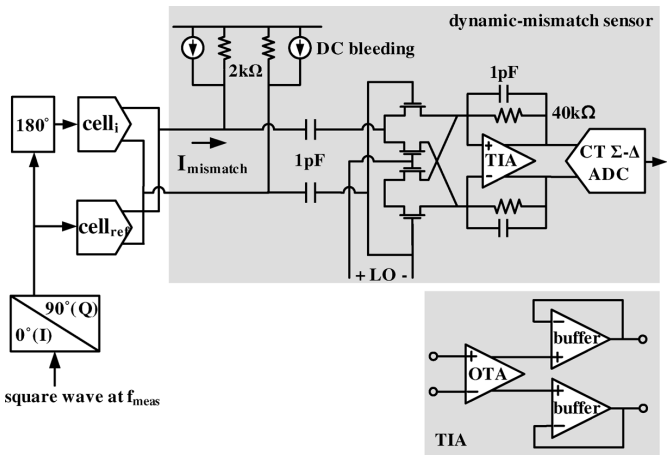

Fig. 12. Dynamic-mismatch sensor.

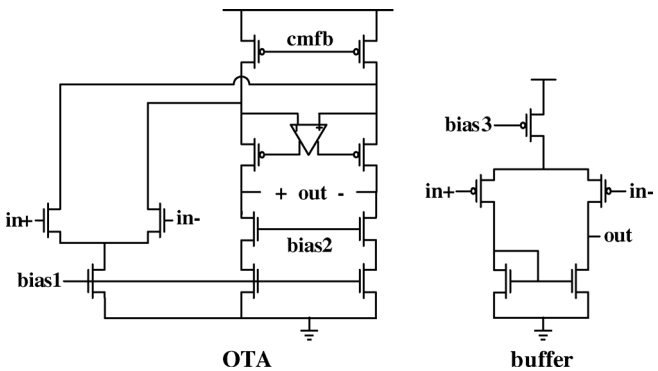

Fig. 13. OTA and buffer.

Q, such that the AC signal at the summation node only comprises mismatch errors and the dynamic range required for the sensor is significantly reduced. A current-bleeding source takes half of the DC current so that a larger loading resistor (2 kΩ) can be connected to increase the signal gain. Then the signal is ac-coupled and down-converted to dc by a passive mixer. Since the signal is directly down-converted to dc, low frequency noise has to be minimized. A passive mixer has low $1/f$ noise since no DC current flows, as compared to an active Gilbert mixer [21]. A low-noise transimpedance amplifier (TIA) with RC low-pass filtering converts and amplifies the down-converted current to a voltage. As shown in Fig. 13, the TIA includes a folded gain-boosting operational transimpedance amplifier (OTA) with 80 dB DC gain as main gain stage, and a buffer stage. The input transistor of the OTA has a large size to minimize the $1/f$ noise since it is the most dominant noise source. Finally, a 5th-order CT ΣΔ ADC based on[22] is used to digitize the output of the TIA. The measurement frequency ($f_{\rm meas}$) is chosen to be 45 MHz. The LO frequency can be $f_{\rm meas}$ or $2f_{\rm meas}$ to measure $\rm E_{fm}$ or $\rm E_{2fm}$. Simulation results show that with a measurement bandwidth of [10 Hz, 200 kHz], the sensor has a resolution of 22.4 nA for amplitude errors and 171 fs for timing errors, respectively.

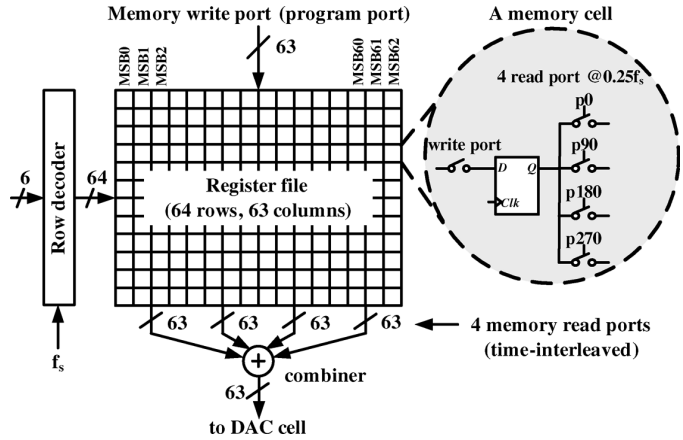

Fig. 14. Mapping engine.

D. Mapping Engine

The mapping engine integrates the function of the standard binary-to-thermometer decoder and the programming of the switching sequence of thermometer current cells. It is based on a $64 * 63$ register file as shown in Fig. 14. According to the DAC input word, the row decoder selects a row as the decoded output. The switching sequence of 63 thermometer current cells is programmed and preset via the write port, so that each row presents the output state of the corresponding input. To increase the speed, four time-interleaved read ports operating at a quarter of the DAC sampling frequency ($0.25f_{\rm s} = 50$ MHz) are used for output. A stream combiner combines these four 63-bit outputs at 50 MHz into one 63-bit output stream at 200 MHz.

V. Measurement Results

A. Static Performance

The static performance is dominated by the thermometer current cells. Fig. 15 shows the measured INL and DNL for the thermometer cells. As shown, with the same sorting algorithm, the INL is improved from 3.2 LSB to 1.7 LSB with traditional SMM and to 1.8 LSB with DMM, on a 14-bit level. The INL reduction factor is 1.78 with DMM, i.e., about 1-bit improvement. Compared to SMM, DMM has almost the same improvement on the static performance, but as shown later, it offers significantly larger improvement on the dynamic performance. As explained in Section III-C, mapping techniques do not improve the DNL. The DNL with and without mapping are both around 2 LSB.

B. Dynamic Performance

Fig. 16 shows the measured IM3 versus signal frequency. As shown, benefiting from a good intrinsic design, the original IM3 already show a rather good performance of < -77 dBc in the whole Nyquist band. With traditional SMM to correct amplitude errors, the IM3 is improved but the improvement reduces with increasing signal frequency, which means the benefit from only correcting amplitude errors decreases and is almost negligible above 80 MHz. DMM provides an additional benefit on the IM3 by also correcting timing errors, especially at high frequencies, resulting in a total improvement of 10 dB up to 70 MHz

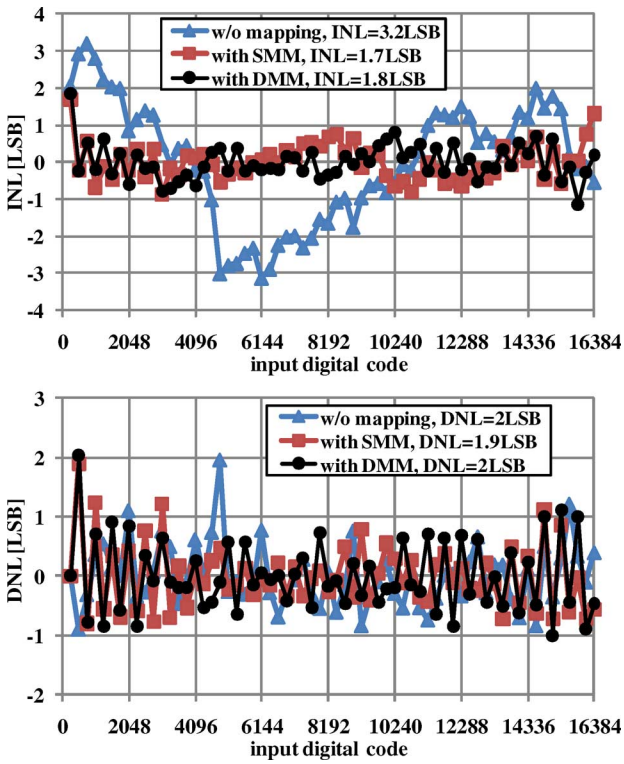

Fig. 15. Measured INL and DNL.

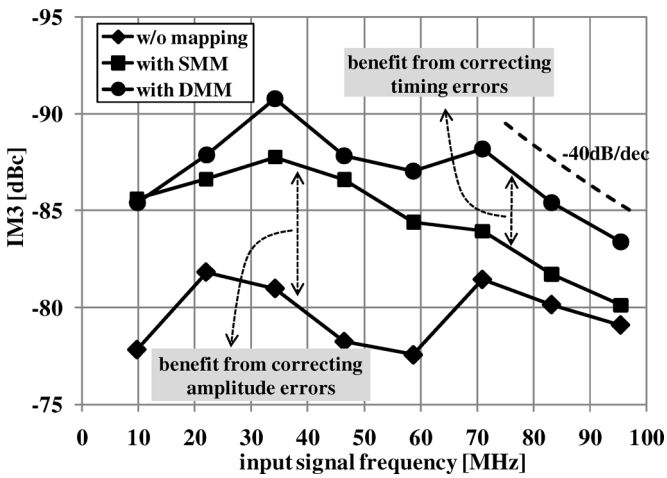

Fig. 16. Measured IM3 versus signal frequency at 200 MS/s, 0 dB FS.

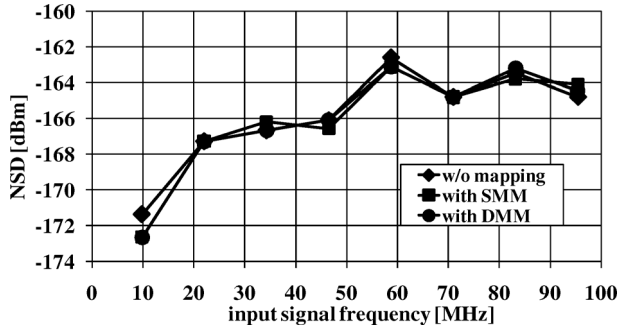

Fig. 17. Measured NSD versus signal frequency at 200 MS/s, 0 dB FS.

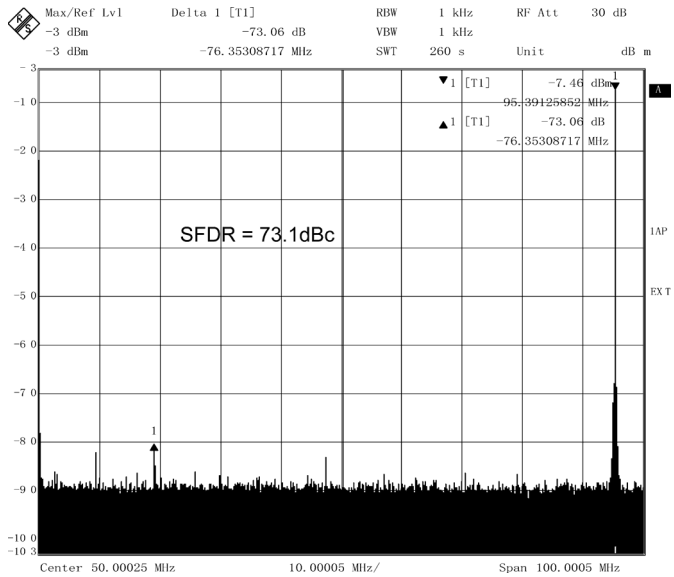

Fig. 18. DAC output spectrum with single-tone at 95.9 MHz, w/o DMM.

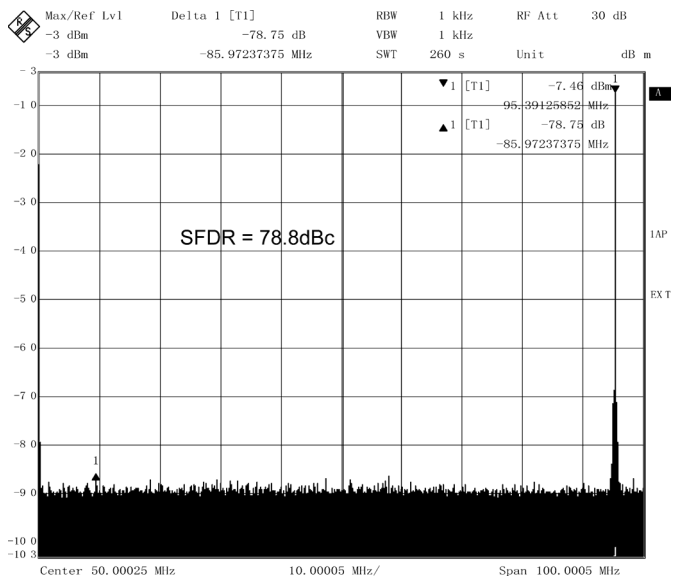

Fig. 19. DAC output spectrum with single-tone at 95.9 MHz, with DMM.

and still 5 dB up to 100 MHz where traditional SMM shows no improvement. At signal frequencies above 70 MHz, the improvement by DMM is limited by the finite output impedance of current cells, which is a non-mismatch error and is confirmed by the -40 dB/decade roll-off. Unlike DEM, DMM does not increase the noise floor since the mismatch impact is reduced instead of randomized. The noise power spectral density (NSD) remains < -163 dBm/Hz independent of mapping, as shown in Fig. 17.

The SFDR is also significantly improved in the whole Nyquist band. Figs. 18 and 19 show the DAC output spectrum with a single output tone at 95.4 MHz. As seen, the original SFDR is 73 dB, while with DMM the SFDR is improved by 6 dB to 79 dB. The measured SFDR versus signal frequency f_{sig} is shown in Fig. 20, together with a comparison with state-of-the-art DACs at similar sampling rate. Without DMM, the original SFDR of this work already achieves a good

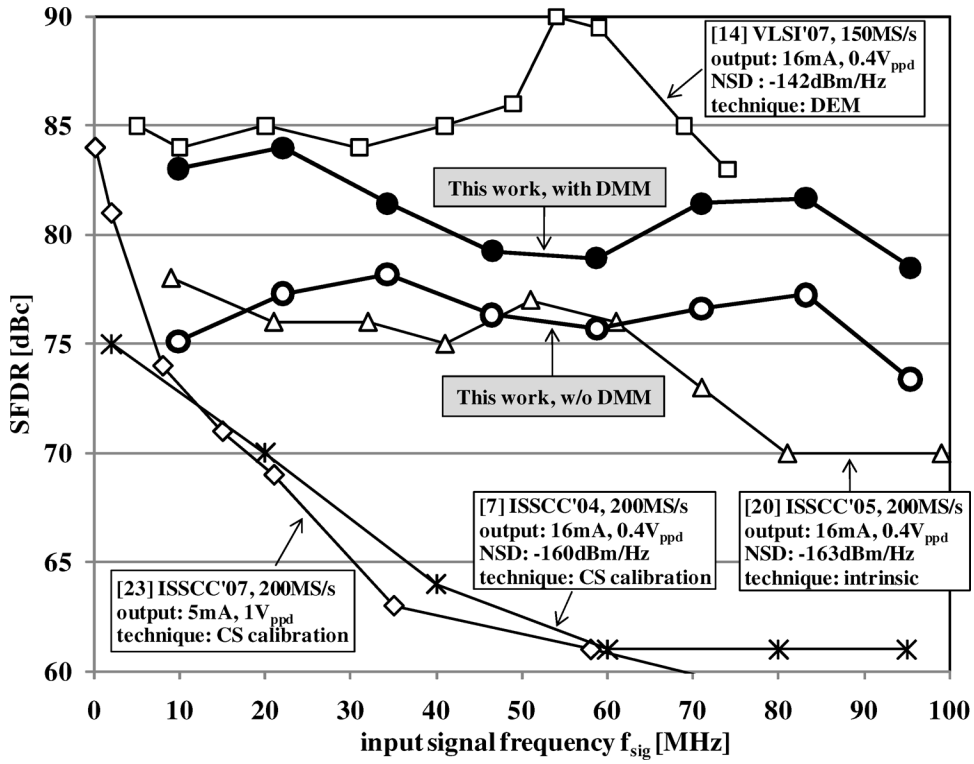

Fig. 20. SFDR performance and comparison with literature.

TABLE I
PERFORMANCE OVERVIEW

Technology	0.14 μm CMOS	
Resolution	14 bit	
Sampling rate	200 MHz	
Full-scale output	20 mA	
Power	270 mW @ 1 / 1.8 V digital / analog supply	
Area	total 2.4 mm^2 (0.27 mm^2 for dynamic-mismatch sensor and 1 mm^2 for mapping engine)	
	w/o DMM	with DMM
INL/DNL	3.2 LSB / 2 LSB	1.8 LSB / 2 LSB
IM3	<-77 dBc	<-84 dBc
SFDR	>73 dBc	>78 dBc
NSD	<-163 dBm/Hz, independent of mapping	

SFDR of $>$73 dB across the whole 100 MHz Nyquist band. With DMM, the SFDR is improved by as much as 8 dB and maintains above 78 dB. The improvement around 50 MHz is limited by the interferences coupled from the time-interleaved mapping engine operating at 1/4 $f_s = 50$ MHz, e.g., substrate coupling. The strength of these interferences increases with f_{sig}, but they will be modulated outside the Nyquist band when f_{sig} is above 50 MHz. This side effect can be attenuated by better shielding. Compared to those DACs with current source calibration [7], [23], this work achieves much better SFDR by calibrating both amplitude and timing errors. Compared to a DEM DAC [14], this work has 21 dB better NSD, higher bandwidth and comparable SFDR. This work also has 5$\sim$10 dB better SFDR as compared to [3], [4] in the 100 MHz f_{sig} range. The performance of the DMM DAC is summarized in Table I.

VI. CONCLUSION

In this paper, a 14 bit 200 MS/s DAC is presented that features a novel digital calibration technique called dynamic-mismatch mapping (DMM). The DMM technique has the advantages of significant improvement on the DAC linearity in a wide frequency range and a low noise floor. Compared to traditional current source calibration and SMM, DMM calibrates both amplitude and timing errors so that both the DAC static and dynamic performance can be significantly improved. Compared to DEM, DMM does not increase the noise floor since the mismatch effect is reduced, not randomized. Moreover, since DMM calibrates all mismatch errors in the digital domain, it adds minimal overhead in the DAC analog core which is preferred in high speed design. It is more attractive on top of a good intrinsic design to efficiently push the performance further and is in favor with advanced CMOS processes, benefiting from the scaling of the area, power, and speed of digital circuits. This DMM DAC achieves a state-of-the-art performance of SFDR $>$78 dB, IM3 <-83 dBc and NSD <-163 dBm/Hz across the whole 100 MHz Nyquist band.

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Yongjian Tang was born in 1981 in Jiangsu, China. He received the B.Sc. and M.Sc. degrees (with honors) from Zhejiang University, Hangzhou, China, in 2002 and 2005, respectively. In 2010, he received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, The Netherlands.

From 2005 to 2009, he was with NXP Semiconductors, Research, Eindhoven, in the Mixed-Signal Circuits and Systems group. From 2009 to 2011, he was a senior research scientist in NXP Semiconductors, Research, Eindhoven. In 2011, he joined MaxLinear, Inc., California, USA, as a member of technical staff. His research interests include analog/RF circuit design, especially high-speed high-performance ADCs and DACs.

Joost Briaire received the M.Sc. degree in 1996 and the Ph.D. degree in 2000 in electrical engineering from Eindhoven University of Technology, The Netherlands.

From 2000 to 2006 he was with Philips Research Laboratories in Eindhoven in the Mixed-Signal Circuits and Systems Department as a senior designer working on high-performance digital-to-analog converters. In 2006 he transferred to the Research Department of NXP Semiconductors while maintaining the same position. In 2010 he moved within NXP to the product line High Speed Converters where he is the principal architect for high-performance digital-to-analog converters.

Kostas Doris received the M.Sc. degree in physics and radio-electronics from Aristotle University of Thessaloniki, Greece, in 1996 and 1998, respectively, and the Ph.D. degree from the Technical University of Eindhoven, Eindhoven, The Netherlands, in 2004.

He joined Philips Research in 2003, and later in 2006 joined NXP Semiconductors, Eindhoven. He is currently a Senior Scientist in the Central Research and Development Department leading activities on high-speed data converters for highly digitized receivers. He is the author or coauthor of many papers and patents in the field of data converters, and the author of the book *Wide-Bandwidth High Dynamic Range D/A Converters* (Springer, 2006).

Robert van Veldhoven was born in Eindhoven, The Netherlands, in 1972. After finishing his pre-education (HAVO) at Het Hertog-Jan College in Valkenswaard, he started to study hands-on electronics at the MTS Leonardo Da Vinci College in Eindhoven. After two years at the MTS, he started studying electrical engineering at the polytechnical college Fontys Hogescholen in Eindhoven. In 1996 he joined the Mixed-Signal Circuits and Systems group at Philips Research after successfully finishing his graduation project on a low-power Sigma-Delta modulator for multi-meter applications. After working for three years at Philips he started to pursue a Master degree in electronics at the Technical University of Eindhoven, which he successfully finished in 2003. After working for 10 years at Philips Research, he joined the Mixed-Signal Circuits and Systems group at NXP Semiconductor Research in Eindhoven in 2006, where he is an expert in the field of high-resolution A/D and D/A converters, and integrated circuits for instrumentation-, sensor-, audio-, and radio-systems. In 2007 he started pursuing a Ph.D. degree in electronics by writing a thesis, in which the results of his work on Sigma-Delta modulators was summarized. His Ph.D. was also published as a book.

Dr. Van Veldhoven holds several U.S. patents and has published various papers at leading conferences and journals, and is a reviewer for several professional journals and conferences. In 2004 and 2010, he was invited to give a forum presentation at the IEEE ISSCC about Sigma-Delta modulators for wireless and cellular receivers.

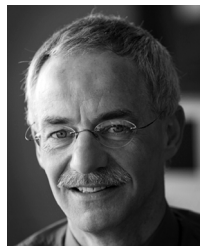
Pieter C. W. van Beek was born in Waalwijk, The Netherlands, in 1978. He received the Bachelor in electrical engineering degree with honors in 2000 from Hogeschool Rens & Rens, Hilversum, The Netherlands. He received the M.S. degree from the Eindhoven University of Technology, where he graduated with honors in 2003. Since 2003 he has been working towards the Ph.D. degree in the field of digital-to-analog converters.

In 2007 he joined NXP Research in Eindhoven in the Mixed-Signal Circuits and Systems Department as a designer working on high-performance DACs. In 2010 he moved within

NXP to the product line High Speed Converters where he is currently working on high-performance DACs.

Johannes A. (Hans) Hegt (M'97–SM'01) was born on June 30, 1952 in Amsterdam, The Netherlands. He studied electrical engineering at the Eindhoven University of Technology (TU/e), The Netherlands, where he graduated with honors in 1982.

From 1983 until 1986 he was an assistant at the TU/e. Since 1987, he has been a Lecturer at this University, where he gives courses in the areas of switched-capacitor filter engineering, switched current filters, digital electronics, microprocessors, digital signal processing, neural networks, nonlinear systems and mixed-signal systems. In 1988 he received the Ph.D. degree on synthesis of switched-capacitor filters. Since 1994 he has been an Associate Professor on mixed analog/digital circuit design. He is currently especially involved in the hardware realization of ADCs and DACs.



Arthur H. M. van Roermund (SM'95) was born in Delft, The Netherlands, in 1951. He received the M.Sc. degree in electrical engineering in 1975 from the Delft University of Technology and the Ph.D. degree in applied sciences from the K.U. Leuven, Belgium, in 1987.

From 1975 to 1992 he was with Philips Research Laboratories in Eindhoven. From 1992 to 1999 he has been a full Professor at the Electrical Engineering Department of Delft University of Technology, where he was chairman of the Electronics Research Group and member of the management team of DIMES. From 1992 to 1999 he has been chairman of a two-years post-graduate school for "chartered designer". From 1992 to 1997 he has been consultant for Philips. In October 1999 he joined Eindhoven University of Technology as a full professor, chairing the Mixed-signal Microelectronics Group. Since September 2002 he has been also director of research of the Department of Electrical Engineering. Until 2009 he was a member of the supervisory board of the NRC Photonics research centre. He is chairman of the board of ProRISC, the microelectronics platform in the Netherlands, and vice chair of the ICT-research platform for The Netherlands (IPN). He has authored or coauthored 470 articles and 29 books.

Since 2001, Dr. van Roermund has been one of the three organizers of the yearly workshop on Advanced Analog Circuit Design (AACD). In 2004 he received the Simon Stevin Meester award, for his scientific and technological achievements. In 2007 he was a member of an international assessment panel for the Department of Electronics and Information of Politecnico di Milano, and in 2009 for Electronics and Electrical Engineering for the merged Aalto University Finland.