Novel operation and control modes for series-resonant converters

Novel Operation and Control Modes for Series-Resonant Converters

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Abstract—**A series-resonant converter (s.r.-converter) able to generate an output voltage either lower or higher than the source voltage is described. Moreover, a novel control scheme is presented which renders two degrees of freedom for control and which guarantees symmetrical steady-state waveforms in all operation modes. Both the average resonant current as well as the peak voltage of the resonant capacitor can be controlled independently. Special attention is given to an operation mode which facilitates converter operation when the output voltages approximately equal the source voltage ($q \simeq 1$). Test results are presented of both controller and converter.**

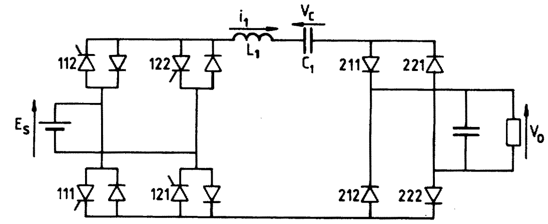

Fig. 1. Basic full-bridge s.r. dc–dc power circuit

I. INTRODUCTION

THE significance of series-resonant converters (s.r.-converters) has grown during the last decade. Initially the s.r.-converter was mainly used for dc-power conversion in aerospace and electronic systems because of its favorable properties (efficiency, weight, and reliability) [1]-[3]. Recently a trend can be perceived towards the development of s.r.-power converters for high-power processing. This includes four-quadrant dc-dc machine driving [4], polyphase ac-dc conversion with a high-power factor in the polyphase supply line [5], and dc-ac power conversion with sinusoidal output waveforms [9]. Apart from weight, efficiency, and reliability, these converters can provide a high-speed response and an accurate generation of ac waveforms with low harmonic distortion.

All the s.r.-converters described up to now have in common that the average output current is controlled by means of controlling the so-called firing angle ψ_r. For dc–dc conversion there are both historical and theoretical reasons to do this. Simulations and experiments [9] showed that this method of control cannot be applied to an important class of multiphase s.r.-converters. In this paper the basic problem will be pointed out. Subsequently, a new way of controlling s.r.-converters is presented which guarantees stable and uninterrupted operation of s.r.-converters. This control mode affects the resonant current and provides an extra degree of freedom for control purposes.

The new control mode of the s.r.-converter, which involves zero current intervals, is illustrated in conjunction with a special type of dc–dc converter. In this converter all switches in the input bridge, including diodes, are implemented as thyristors. Although this large number of thyristors is not strictly required in dc–dc converters, one should bear in mind that it is required for ac-converters. This setup is considered as an intermediate step to multiphase power generation. The structure of the input bridge facilitates several operation modes of the s.r.-converter. The converter is able to supply power to an output voltage that is smaller than the source voltage ("$q < 1$") as well as to an output voltage that is greater than the source voltage ("$q > 1$"). These two operation modes will be shown in combination with the new control method. In this paper the presentation is restricted to first and third quadrant operations, unless noted otherwise.

A. Some Properties of S.R.-Converters

The principles and applications of the s.r.-converter or Schwarz-converter have been treated in literature [1]-[3]. The basic schematic of a s.r. dc–dc converter commonly in use is depicted in Fig. 1. The switches in the input bridge are implemented as a thyristor with antiparallel diodes although any other type of controllable switch can be used such as MOSFET's. The input switching matrix, consisting of switches 111, 112, 121, and 122, connects a power source with voltage E_s to an s.r. circuit of high quality. By means of the input matrix a square-wave voltage is generated across the LC-circuit, thus inducing a resonant current in the circuit. The high-frequency alternating current is rectified by the output matrix (switches 211, 212, 221 and 222) and subsequently supplied to a filter-load system.

The only "input" where one can intervene from outside in the power part of the converter is the time of ignition $\beta_k + \psi_r(k)$ of the thyristors. Once a thyristor has been fired, a resonant sinusoidal current pulse follows, and immediately thereafter a diode current pulse (Fig. 2). This occurs in both the continuous and discontinuous operation mode. The way of operation as described above will be referred to as the "normal control mode". The resonant waveform is not necessarily periodical in a strict sense and depends on initial conditions, the value of $\psi_r(k)$ and the terminal voltages.

1) Definitions: To obtain a compact notation the time is normalized with respect to the natural frequency ω_1 of the

Manuscript received September 20, 1984.
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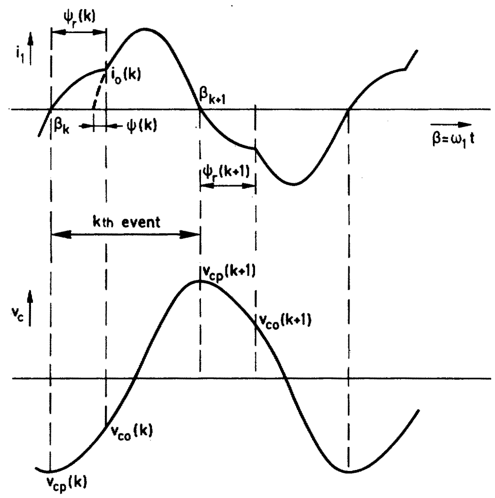

Fig. 2. Resonant current and capacitor voltage waveform for the normal operation mode.

resonant circuit

$$\beta = \omega_1 t. \tag{1}$$

The interval (β_k, β_{k+1}) between two current zero crossings is designated as the kth converter cycle. Both the diode interval $(\beta_k, \beta_k + \psi_r(k))$, as well as the thyristor interval $(\beta_k + \psi_r(k), \beta_{k+1})$ will be designated as converter subcycles. For steady-state conditions the index k will be omitted. For nonsteady-state conditions, all variables within the kth converter cycle (β_k, β_{k+1}) are denoted by index k (Fig. 2).

Define:

$$v_{cp}(k) = v_c(\beta_k) \tag{2}$$

$$v_{co}(k) = v_c(\beta_k + \psi_r(k)) \tag{3}$$

$$i_{io}(k) = i_1(\beta_k + \psi_r(k)). \tag{4}$$

If in the kth cycle the converter is connected to source #i of a multiphase source $e_{si}(i = 1, \cdots, M)$, then the input voltage $E_s(k)$, or shortly E_s, is defined as

$$E_s = e_{si}(\beta_k). \tag{5}$$

It is supposed that the input capacitor and the output capacitors are sufficiently large to justify the assumption of a constant source and load voltage within the kth converter cycle.

The diode current can dispose of excessive energy and serves the turnoff process of thyristors by generating a reverse-bias voltage of approximately 1 V. Insufficient turnoff conditions may lead to a short-circuit in the input bridge. For that reason a diode current should occur for a sufficiently long time. Inspection of Fig. 1 reveals that the thyristors 112 and 121, which have been conducting in the interval $(\beta_k + \psi_r(k), \beta_{k+1})$, might be forward-biased in the interval following β_{k+1} if $v_{cp}(k + 1) < E_s + V_o$. The proof follows from an application of Kirchhoff's law at time β_k on a "worst-case" maze, including source and load. If $v_{cp} > E_s + V_o$ at time β_k, a diode current will start to flow and the inductor will absorb excessive volts. Consequently, a reverse-bias voltage of approximately 1 V is guaranteed for the thyristors 112 and 121.

From the well-known s.r.-converter theory [2], [3] it follows that for given values of E_s and V_o the following steady-state relationship exists between v_{cp} and ψ_r:

$$v_{cp} = E_s \left\{ \frac{(1+q)(1-q\cos\psi_r)}{(q-\cos\psi_r)} \right\}. \tag{6}$$

Moreover, the following formula can be written for $|i_1|_{av}$:

$$|i_1|_{av} = \frac{E_s}{Z_1} \left\{ \frac{2(1+q)(1-\cos\psi_r)}{(\psi_r + \pi - \psi)(q - \cos\psi_r)} \right\} \tag{7}$$

where

$$Z_1 = \sqrt{L_1/C_1}$$

and

$$\psi = \pi/2 + \arctan \left\{ \frac{2q - (1+q^2)\cos\psi_r}{(1-q^2)\sin\psi_r} \right\}.$$

Two important conclusions can be extracted from (6) and (7).

1) v_{cp} and $|i_1|_{av}$ cannot be controlled independently for the method of converter operation described.

2) For all combinations of q and ψ_r the capacitor peak voltage will be greater than or equal to $2E_s$.

$$v_{cp} \geqslant 2E_s \tag{8}$$

where the equal sign applies to the discontinuous conduction mode. The condition $v_{cp} > E_s + V_o$ does not seem relevant when (8) is considered. However, (6) and (8) are based on steady-state symmetrical resonant currents, i.e., the shape of a positive resonant-current pulse is a replica of the shape of a negative one. It can be shown [6] that asymmetrical steady-state operation modes exist where

$$v_{cp}(k) \neq v_{cp}(k+1)$$

and

$$v_{cp}(k) = v_{cp}(k+2). \tag{9}$$

In this operation mode it is feasible that $v_{cp}(k) < 2E_s$, while $v_{cp}(k + 1) > 2E_s$. In comparison to the symmetrical operation mode this mode imposes extra stress on the components, so that the controller should serve to reject asymmetries.

Summarizing, the following areas for the capacitor peak voltage can be distinguished:

1) when $v_{cp}(k) < E_s + V_o$: converter might be damaged (10)

2) when $E_s + V_o < v_{cp}(k) < 2E_s$: converter will operate in an asymmetrical mode (11)

3) when $v_{cp}(k) > 2E_s$: symmetrical converter operation is feasible. (12)

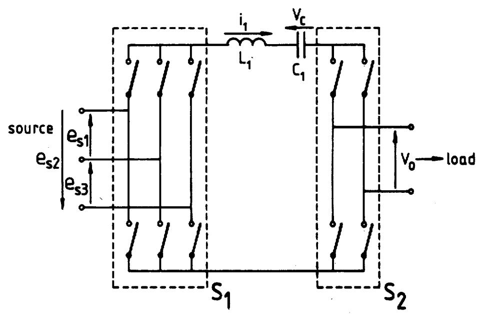

Fig. 3. Typical power circuit of a s.r.-converter with a multiphase source. S_1 and S_2 are switch matrices.

To increase the reliability of s.r.-converters, usually [7] the occurrence of condition (10) is monitored in some way (reverse-bias detection) and used to interrupt converter operation in case of pending turnoff failure. In the following section it will be shown that these interruptions may frequently occur in normally operated multiphase s.r.-converters, due to the absence of condition (10). Moreover, it will be shown that a control method exists which guarantees the occurrence of condition (12) for successive cycles.

B. Abruptly Changing Terminal Voltages

A multiphase s.r.-converter consists of a s.r.-circuit which is connected via two switch matrices S_1 and S_2 to a multiphase source (and/or load) (Fig. 3). From the point of view of the resonant network the multiphase s.r.-converter is basically a dc–dc converter which is connected to a certain source $e_{si}(i = 1, 2, \cdots, M)$ for the duration of one or more converter subcycles. The multiphase source (or load) voltage is supposed to vary slowly with respect to the duration of a converter subcycle, so within a converter subcycle the selected source voltage e_{si} can considered to be constant. At the beginning of the next converter subcycle, the converter may switch to a different source, so that the apparent source (or load) voltage of the resonant circuit may be discontinuous at times β_k.

Based on the conclusions from the preceding section, it is expected that if the resonant circuit switches from a relatively low-source voltage e_{s1} to a large source voltage e_{s2}, the converter operation might be interrupted due to insufficient thyristor turnoff conditions. This particularly occurs when a lightly loaded converter—thus $v_{cp} \cong 2e_{s1}$—switches from a small source e_{s1} to a large source e_{s2}, where

$$2e_{s1} < e_{s2} + V_o. \tag{13}$$

The example above illustrates that the normally controlled s.r.-converter exhibits a drawback which obstructs the application of the s.r.-converter in those classes of multiphase networks where switching between voltages of different magnitudes is required. The multiphase converters presented up to now [5], [7], [8] switch from one source to another at the time the voltages of the respective sources are approximately equal. In those converters the problem described is avoided by sacrificing the potential ability to switch between voltages at arbitrary times. To guarantee uninterrupted converter operation it is

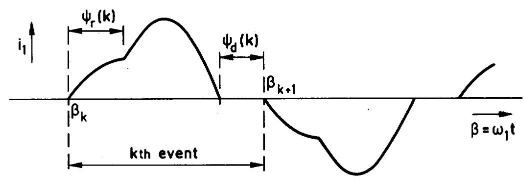

Fig. 4. Resonant current waveform in a s.r.-converter where capacitor peak voltage and average current are controlled independently.

in fact necessary to control the capacitor peak voltage independently from the average current and maintain it at a sufficiently high value.

The problem stated above can be solved by taking advantage of the specific structure of multiphase s.r.-converters. In these converters all semiconductors, including diodes, are implemented as thyristors, so the "diode" current can be retarded, thus generating a resonant current as indicated in Fig. 4. Note that although the multiphase network does not contain diodes, the term "diode current" is still used to designate the first current interval following a current zero crossing. The retardation angle, also referred to as the interpulse time t_d, provides an extra degree of freedom for control. The firing angle ψ_r is used to control the peak capacitor voltage, while the retardation angle ψ_d is used to control the average current $|i_1|_{av}$ independently from v_{cp}. If the average current is controlled by means of a pulse integral controller, then ψ_d follows from

$$\int_{\beta_k}^{B_{x+1}} (|i_1|_{av} - i_{\text{ref}})\, d\beta = 0. \tag{14}$$

The peak capacitor voltage should be controlled in such a way that a thyristor reverse bias is guaranteed for all possible combinations of input and output voltages. From the discussion in relation to (5), (6), and (7), it will be clear that a reverse bias is guaranteed when

$$v_{cp}(k) > 2 \max \{E_{si}(k), V_{oj}(k)\}. \tag{15}$$

Possibly a less stringent condition might be formulated; however, the analysis under nonsteady-state conditions will be cumbersome and an alternative formulation will probably lead to asymmetrical currents. It will be shown that if (15) holds, one can find $\psi_r(k)$ such that the following equation also holds:

$$|v_{cp}(k+1)| = |v_{cp}(k)|. \tag{16}$$

Equation (16) implies that 1) the reverse bias can be guaranteed for all succeeding converter cycles; 2) the converter is operating in a symmetrical mode with respect to the peak capacitor voltage.

Proof: If it is assumed that within the kth thyristor cycle the converter is connected to a source voltage $E_s(k)$ and an output voltage $V_o(k)$, then the following energy balance can be written

$$\frac{1}{2}C_1 v_c^2(t_1) + \frac{1}{2}L_1 i_1^2(t_1) + \int_{t_1}^{t_2} \{E_s(k) - V_o(k)\} i_1(t)\, dt$$

$$= \frac{1}{2}C_1 v_c^2(t_2) + \frac{1}{2}L_1 i_1^2(t_2) \tag{17}$$

where t_1 and t_2 are arbitrary times within the kth thyristor cycle. The last term on the left-hand side of the equation can be reformulated as

$$\int_{t_1}^{t_2} (E_s - V_o) i_l \, dt = (E_s - V_o) C_1 \{v_c(t_2) - v_c(t_1)\}. \quad (18)$$

For notational convenience the index k is omitted at V_o and E_s.

By eliminating the integral from (17) and (18) the following useful equation can be deduced:

$$\{v_c(t_1) - E_s + V_o\}^2 + Z_1^2 i_1^2(t_1) = \{v_c(t_2) - E_s + V_o\}^2 + Z_1^2 i_1^2(t_2) \quad (19)$$

where

$$Z_1^2 = L_1/C_1.$$

Let

$$\omega_1 t_1 \equiv \beta_k + \psi_r(k)$$

and

$$\omega t_2 \equiv \beta_{k+1}$$

then (see Fig. 2):

$$v_c(t_1) \equiv v_{co}(k) \qquad v_c(t_2) \equiv v_{cp}(k+1)$$
$$i_1(t_1) \equiv i_{1o}(k) \qquad i_1(t_2) \equiv 0$$

so that

$$v_{cp}(k+1) = E_s - V_o + \{(v_{co}(k) - E_s + V_o)^2 + Z_1^2 i_{10}^2(k)\}^{1/2}. \quad (20)$$

The value of $v_{co}(k)$ can be expressed in $v_{cp}(k)$ and $\psi_r(k)$. (See Figs. (1) and (2).)

$$v_{co}(k) = v_{cp}(k) + Z_1 \int_0^{\psi_r(k)} i_1(\beta^1) \, d\beta^1 \quad (21)$$

where

$$i_1(\beta^1) = \frac{-1}{Z_1} \{v_{cp}(k) + E_s + V_o)\} \sin \beta^1 \quad (22)$$

so

$$i_{10}(k) = \frac{-1}{Z_1} \{v_{cp}(k) + E_s + V_o\} \sin \psi_r(k). \quad (23)$$

Evaluation of (21) yields

$$v_{co}(k) = -E_s - V_o + (v_{cp}(k) + E_s + V_o) \cos \psi_r(k). \quad (24)$$

Elimination of $v_{co}(k)$ and $i_{1o}(k)$ from (20) be substitution of (23) and (24) renders the following expression [6]:

$$v_{cp}(k+1) = E_s - V_o + \{(v_{cp}(k) + E_s + V_o)^2 + 4E_s(-v_{cp}(k) - E_s - V_o) \cdot \cos \psi_r(k) + 4E_s^2\}^{1/2}. \quad (25)$$

Because $v_{cp}(k) < 0$, (25) can be written as

$$v_{cp}(k+1) = E_s - V_o + \{(-|v_{cp}(k)| + E_s + V_o)^2 + 4E_s(|v_{cp}(k)| - E_s - V_o) \cdot \cos \psi_r(k) + 4E_s^2\}^{1/2}. \quad (26)$$

This equation will be used to show that if

$$v_{cp}(k) < -2 \max \{E_s, V_o\} \quad (15)$$

one can find a $\psi_r(k)$ such that $|v_{cp}(k+1)| = |v_{cp}(k)|$. For $\psi_r(k) = 0$ (26) reduces to

$$v_{cp}(k+1) = E_s - V_o + \{[(-|V_{cp}(k)| + E_s + V_o) - 2E_s^2]\}^{1/2}. \quad (27)$$

Because the expression within square brackets is negative, it follows that

$$v_{cp}(k+1) > 2(E_s - V_o) + |v_{cp}(k)|. \quad (28)$$

Because $E_s > V_o$, it follows that $|v_{cp}(k+1)| > |v_{cp}(k)|$ for $\psi_r = 0$. For $\psi_r(k) = \pi$, (26) reduces to

$$v_{cp}(k+1) = -|v_{cp}(k)| + 4E_s. \quad (29)$$

Because $v_{cp}(k) < -2E_s$, it follows that

$$v_{cp}(k+1) < 2E_s.$$

Thus from (28) and (29), respectively, it follows that

1) If $|v_{cp}(k)| > 2E_s(k)$ then $|v_{cp}(k+1)| > |v_{cp}(k)|$ for $\psi_r = 0$,

2) if $|v_{cp}(k)| > 2E_s(k)$ then $|v_{cp}(k+1)| < |v_{cp}(k)|$ for $\psi_r = \pi$.

Because (25) is a continuous function of ψ_r, it follows that there is at least one ψ_r such that $|v_{cp}(k)| = |v_{cp}(k+1)|$.

Note that analysis will reveal that (25) is a monotonous function of ψ_r, so that there is only one solution. The validity of (11) follows from (28) and (29) as well. If $|v_{cp}(k)| < 2E_s$ then for both $\psi_r = 0$ and $\psi_r = \pi$, the value of $|v_{cp}(k+1)|$ will be greater than $2E_s$. Because v_{cp} is a monotonous function of ψ_r, we cannot find a ψ_r such that $|v_{cp}(k)| = |v_{cp}(k+1)|$.

Instead of solving $\psi_r(k)$ from (25), the capacitor peak voltage is maintained at a constant value by application of a network (Fig. 5) which gives a real-time prediction of $v_{cp}(k+1)$ based on $i_1(t)$, $v_c(t)$, $E_s(k)$ and $V_o(k)$. Whenever the predicted

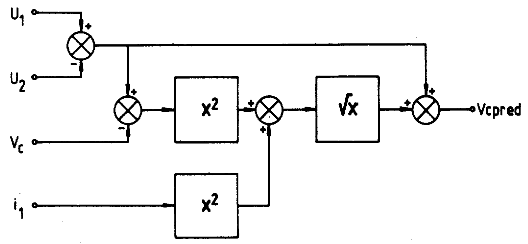

Fig. 5. Capacitor peak voltage prediction network.

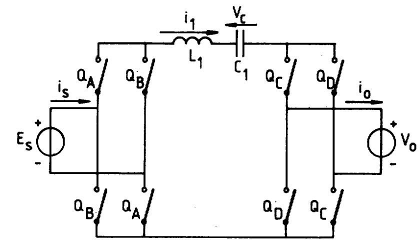

Fig. 6. Basic full-bridge s.r.-converter that is capable of operating at $q > 1$.

value of $v_{cp}(k + 1)$ equals the v_{cp} reference, v_{cpref}, a "thyristor" pulse is generated. Note that in Fig. 5, U_1 and U_2 correspond to either $+E_s$ or $-E_s$ and $+V_o$ or $-V_o$, respectively. To enable better insight, the prediction network is depicted with three multipliers, although a slight reformulation of the problem will reveal that two multipliers will suffice.

Note that for this new control mode (6) is still valid for the stationary state; however, (7) should be multiplied by a kind of duty factor

$$\delta = 1 - \psi_d/(\psi_r + \pi - \psi_o + \psi_d) \tag{30}$$

to obtain the average resonant current. In the new operation mode the current distortion factor is slightly increased by a factor of $\sqrt{\delta}$ in comparison with the normal operation mode.

II. SWITCHING MODE WITH $q > 1$

Based on a reconsideration of the basic switching modes of the s.r.-converter it will now be shown that the converter as depicted in Fig. 6 is, in combination with the previously described control mode, capable of generating output voltages $V_o > E_s$ as well as $V_o < E_s$. The converter from Fig. 6 is considered as a part of the multiphase s.r.-converter from Fig. 3. All switches are implemented as antiparallel thyristors. For the ease of argument it is assumed throughout the following discussion that both E_s and i_o are positive, although this restriction is not essential. In this case the input bridge from Fig. 6 may be identical to the input bridge from Fig. 1 and may contain diodes. If it is supposed that

$$|v_{cp}(k)| = |v_{cp}(k+1)| \tag{31}$$

then the energy content of the converter will be the same at times β_k and β_{k+1}. N.B.: $i_1(\beta_k) = 0$.

Bearing in mind that the energy transferred by a voltage source V within a certain interval is equal to the product of voltage V and the transferred charge Q within that interval, it follows from an energy balance that

$$\frac{Q_D(k)}{Q_T(k)} = \frac{E(k) - V_o(k)}{E(k) + V_o(k)} \tag{32}$$

where $Q_D(k)$ and $Q_T(k)$, respectively, represent the charge transferred by i_o in the diode and thyristor interval considered. In the normal operation mode from Fig. 2 both Q_D and Q_T are positive, so it follows from (32) that

$$|V_o| < E_s \text{ or } |q| < 1. \tag{33}$$

It is well known [4] that the network from Fig. 6 can operate at negative values of V_o in the normal operation mode (4th quadrant). Fig. 7(a) and (b) show waveforms of i_s, i_1, and i_o for both $q > 0$ and $q < 0$ where $|q| < 1$. Note that it follows from (32) that

$$Q_D(k) > Q_T(k)$$

if

$$V_o(k) < 0. \tag{34}$$

Converter operation at a negative value of q does in fact signify that power is transferred from a low voltage V_o to a high voltage E_s. Because of the perfect structural symmetry of the converter in Fig. 6 with respect to the input and output, the converter should be able to transfer power from E_s to V_o where $V_o > E_s$. Fig. 7(c) and (d) show the associated current waveforms where $q > 1$.

Note that essentially only two different switching modes exist because mode a is equivalent to mode d, and mode b is equivalent to mode c. We distinguish a transfer of power from a high to a lower voltage and the reverse.

Although Figs. 7(a)-(d) are drawn for positive values of E_s and i_o, it will be clear that diagrams for negative values of E_s and/or i_o can be obtained easily. From (38) and Fig. 7 it follows that for all converter switching modes the current waveforms have some properties in common:

- The diode current is opposed by the highest absolute terminal voltage,
- the direction of the thyristor current on the high voltage side is opposite to the direction of the diode current on that side,
- the direction of both the thyristor and the diode current on the low voltage side is such that they transfer power in the desired direction,
- when net energy is transferred to the highest absolute voltage voltage the following relation holds: $Q_D(k) > Q_T(k)$,
- the average current on the low voltage side of the converter is equal to $|i_1|_{av}$, while that on the high voltage side is equal to $|i_1|_{av}/q$.

This last remark implies that for converters which operate in the $q > 1$ mode, the average current $|i_1|_{av}$ cannot be used to control the average output current.

As mentioned earlier (6) and (7) also apply to negative values of q. In Fig. 8 normalized curves of v_{cp}, $|i_1|_{av}$, and i_p

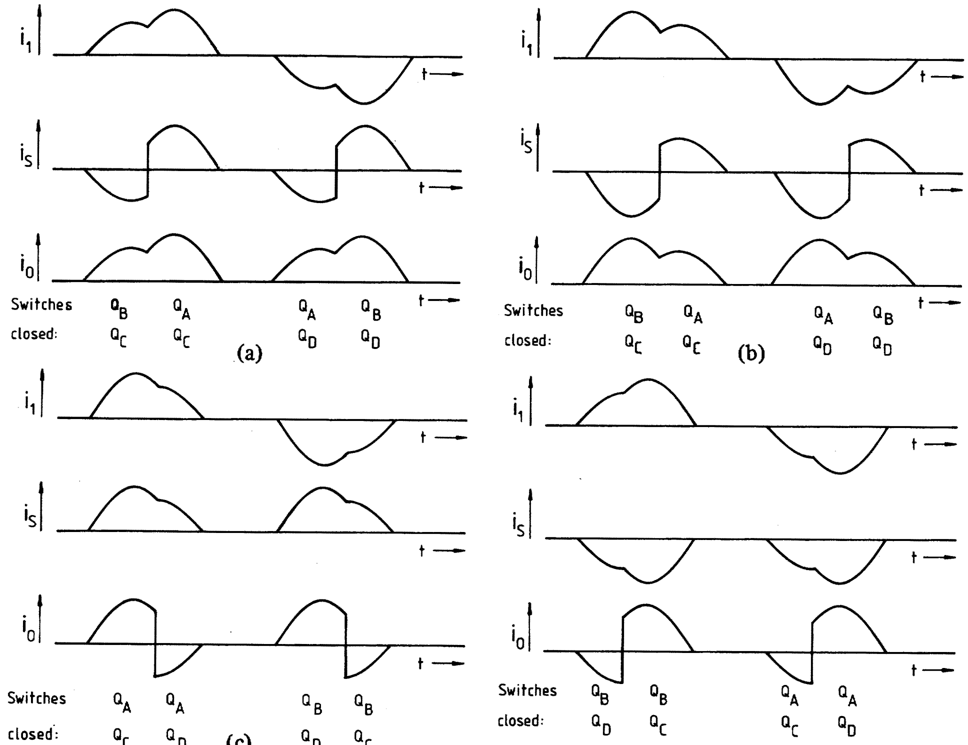

Fig. 7. Basic switching modes of a s.r.-converter fully equipped with thyristors (N.B. $E_s > 0$); $I_o > 0$). (a) $0 < q < 1$. (b) $-1 < q < 0$. (c) $q > 1$. (d) $q < -1$.

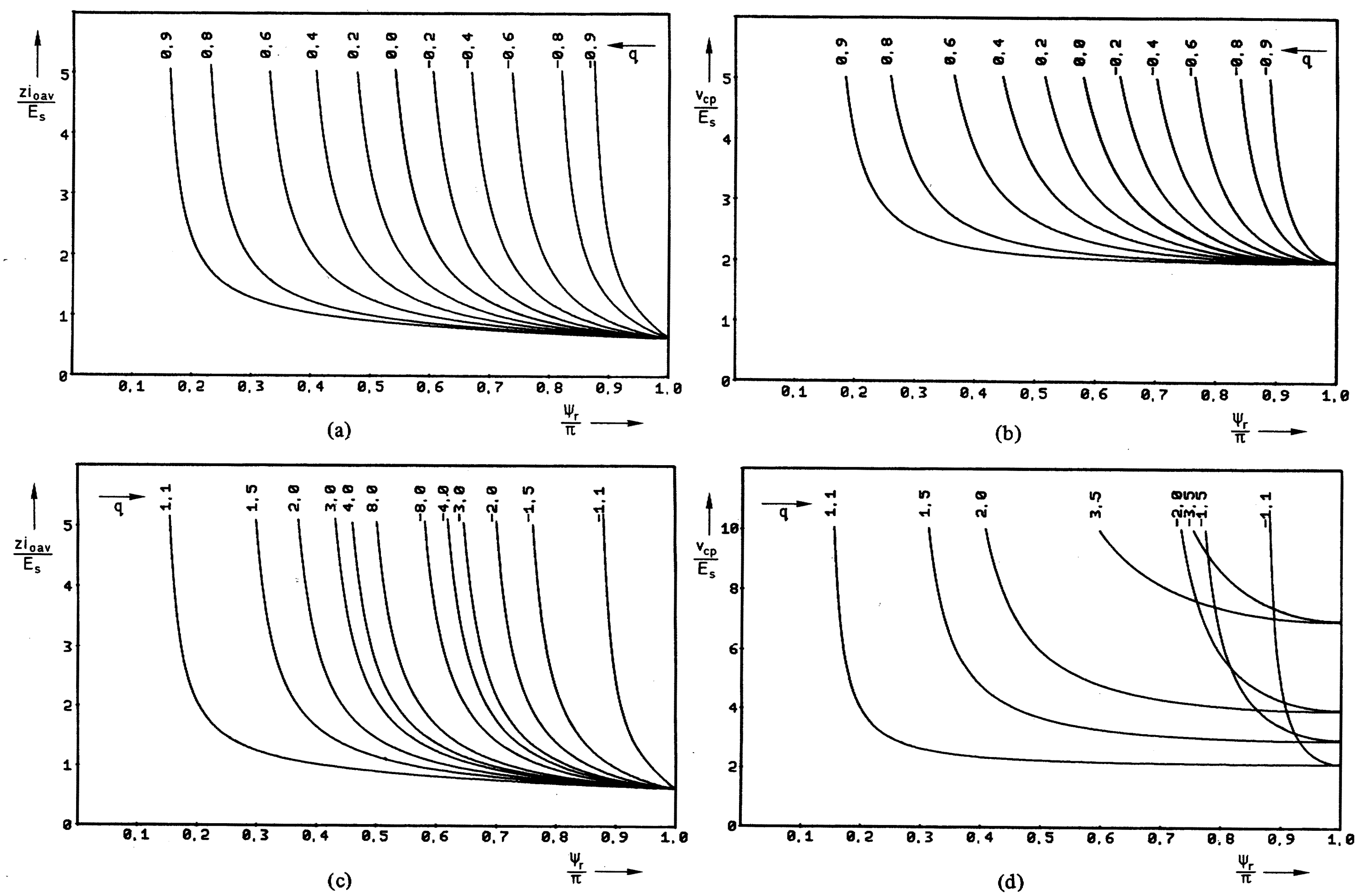

Fig. 8. Normalized average output current i_{oav} and normalized capacitor peak voltage v_{cp} as a function of ψ_r for both $|q| < 1$ and $|q| > 1$.

are plotted as a function of ψ_r for both $q < 0$ and $q > 0$. Formulas for $|q| > 1$ can be constructed from formulas for $|q| < 1$ by properly redefining of the input and output (replacing q by $1/q$, and E by qE). This redefinition process leads to the following formulas for v_{cp} and $|i_1|_{av}$. For convenience the results are plotted in Fig. (8)

$-1 < q < 1: |i_o|_{av} = |i_1|_{av}$ see (7)

v_{cp} see (8)

$$|q| > 1: v_{cp} = qE_s \left\{ \frac{(q+1)(1-\cos\psi_r)}{(1-q\cos\psi_r)} \right\} \tag{35}$$

and

$$|i_o|_{av} = |i_1|_{av}/q = \frac{E_s}{Z_1} \left\{ \frac{2(q+1)(1-\cos\psi_r)}{(\psi_r + \pi - \psi)(1 - q\cos\psi_r)} \right\} \delta \tag{36}$$

with

$$\psi = \pi/2 + \arctan \left\{ \frac{2q - (1+q^2)\cos\psi_r}{(q^2-1)\sin\psi_r} \right\} \tag{37}$$

and δ according to (30).

Note that in the $q > 1$ switching mode, the minimum delay angle ψ_d should correspond to the turnoff time t_q of the output-bridge thyristors. This statement holds for the first and third quadrant operations only.

III. VERIFICATION

In order to evaluate the previously described switching modes a and c, and the new v_c-control mode, a converter is required that is equipped with thyristors and antiparallel diodes in both input and output bridge. The test converter had the following specifications:

source voltage	E_s	=	100 V
maximum inverter frequency	f_1	=	10 kHz
peak capacitor voltage	v_{cp}	=	350 V
resonant capacitor	C_1	=	1.11 μF
resonant inductor	L_1	=	146 μH
input filter capacitor	C_s	=	50 μF.
output filter capacitors	C_o	=	50 μF.

To generate an output voltage in excess of the source voltage, the converter will have to turn over from switching mode a to switching mode c. This turnover process needs some elucidation. In both switching modes a and c (Fig. 7), the capacitor peak voltage is maintained at a predescribed reference level ($v_{cpref} \cong 3E_s$).

From Fig. 8 it follows that in the steady state ψ_r has to decrease when q approaches 1. When $q = 1$, the capacitor peak voltage cannot be maintained at the predescribed level, and will theoretically decay to $2E_s$. Without special measures the converter will stop due to the absence of a thyristor reverse-bias. To overcome this problem an additional operation mode is added to the converter. Whenever a decay of v_{cp} is detected below a certain value, for instance 2.3 E_s, the next diode pulse is omitted. After the thyristors have turned off, an extra thyristor pulse is generated which flows through the source and through a short-circuited output bridge via thyristors 211 and 212. This extra converter cycle does increase the capacitor peak voltage by approximately 2 E_s to 4.3 E_s, thus enabling the converter to operate for a few cycles in the $q = 1$ region. For a 90-percent efficient s.r.-converter this "cycle stealing" process will have to be carried out for values of q in between approximately 0.9 and 1.0, provided the converter turns over from switching mode a to switching mode c at $q = 1$. Fig. 9 shows the cycle stealing process when $q = 0.9$. Note the decay of v_{cp} and further that a current pulse in i_1 is missing in i_o. The particular pulse is marked by the lower trace signal. Fig. 10 shows the turnover process from mode a to mode c and the changed appearance of i_1 and i_o.

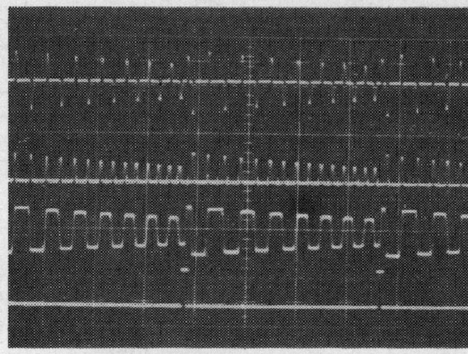

Fig. 9. Converter operation near $q = 0.9$ to show the cycle stealing process. Upper trace: i_1, 50 A/div; second trace: i_0, 50 A/div; and third trace: v_c, 700 V/div, 500 μs/div.

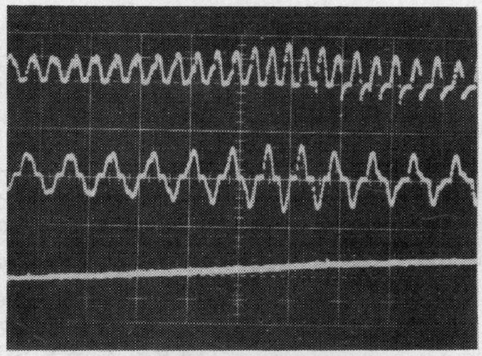

Fig. 10. Resonant current and capacitor peak voltage at the moment of turnover from switching mode a to switching mode c. Upper trace i_0, 50 A/div; middle trace i_1, 50 A/div; and lower trace: V_o; 200 μs/div.

The importance of the $q > 1$ feature is evident when one considers converter efficiency η. It is well known [2], [4], [5], [7] that losses in s.r.-converters are approximately proportional to $|i_1|_{av}$, and independent of q. So η rapidly decreases with decreasing q.

$$V_{\text{loss}} = (1 - \eta)E_s. \tag{38}$$

The decreasing η is due to the fact that a decreasing q is accompanied by an increasing diode current which does not contribute to the power extracted from the source, although it does contribute to the losses. From this statement it can be concluded that for all applications where a variable input-output voltage ratio is required, for instance, dc-ac conversion, it may be of advantage to allow for the $q > 1$ switching mode, and choose transformers, if present, such that the "average" q value of the converter is close to 1. Here q is defined according to $q = V_{xa}/E_s$ where V_{xa} is the reflected output voltage on the primary side of the transformer.

IV. CONCLUSION

The control mode described in this paper facilitates independent control of average resonant current and capacitor peak voltage. Proper control of v_{cp} will guarantee uninterrupted and symmetrical operation of a class of multiphase s.r.-converters. For dc-dc converters the benefits of this control mode are less significant and probably do not counterbalance the handicaps of a slight increase of current distortion, as well as having to replace diodes by controllable switches in the input or output bridge. Single and multiphase ac-converters do not require any modification of the power network to implement the new control mode. For a converter which does contain controllable switches in the output bridge (Fig. 6), the new switching mode is demonstrated and associated current waveforms are shown for the new and related basic switching modes. The new switching mode facilitates the operation of s.r.-converters at both $q < 1$, and well as $q > 1$, without the application of a transformer. The added feature provides a tool for optimizing the performance of s.r.-ac converters.

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