High capacity photonic integrated switching circuits

High Capacity Photonic Integrated Switching Circuits

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"Science is the belief in the ignorance of the experts"
Richard P. Feynman

"Stay hungry, stay foolish"
Steward Brand and the whole earth catalog team

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SUMMARY

High Capacity Photonic Integrated Switching Circuits

As the demand for high-capacity data transfer keeps increasing in high performance computing and in a broader range of system area networking environments; reconfiguring the strained networks at ever faster speeds with larger volumes of traffic has become a huge challenge. Formidable bottlenecks appear at the physical layer of these switched interconnects due to its energy consumption and footprint. The energy consumption of the highly sophisticated but increasingly unwieldy electronic switching systems is growing rapidly with line rate, and their designs are already being constrained by heat and power management issues. The routing of multi-Terabit/second data using optical techniques has been targeted by leading international industrial and academic research labs. So far the work has relied largely on discrete components which are bulky and incur considerable networking complexity. The integration of the most promising architectures is required in a way which fully leverages the advantages of photonic technologies.

Photonic integration technologies offer the promise of low power consumption and reduced footprint. In particular, photonic integrated semiconductor optical amplifier (SOA) gate-based circuits have received much attention as a potential solution. SOA gates exhibit multi-terahertz bandwidths and can be switched from a high-gain state to a high-loss state within a nanosecond using low-voltage electronics. In addition, in contrast to the electronic switching systems, their energy consumption does not rise with line rate.

This dissertation will discuss, through the use of different kind of materials systems and integration technologies, that photonic integrated SOA-based optoelectronic switches can be scalable in either connectivity or data capacity and are poised to become a key technology for very high-speed applications. In Chapter 2, the optical switching background with the drawbacks of optical switches using electronic cores is discussed. The current optical technologies for switching are reviewed with special attention given to the SOA-based switches. Chapter 3 discusses the first demonstrations using quantum dot (QD) material to develop scalable and compact switching matrices operating in the 1.55μm telecommunication window. In Chapter 4, the capacity limitations of

scalable quantum well (QW) SOA-based multistage switches is assessed through experimental studies for the first time. In Chapter 5 theoretical analysis on the dependence of data integrity as ultrahigh line-rate and number of monolithically integrated SOA-stages increases is discussed. Chapter 6 presents some designs for the next generation of large scale photonic integrated interconnects. A 16x16 switch architecture is described from its blocking properties to the new miniaturized elements proposed. Finally, Chapter 7 presents several recommendations for future work, along with some concluding remarks.

Contents

Chapter

1 Introduction

This chapter introduces and highlights the increasing need for greater interconnection bandwidth and dynamic re-configurability in future core, metropolitan, wide and short area (MAN, WAN, SAN) networks.

1.1 Data Deluge

The preservation and dissemination of data has revealed an exponential growth with data volumes doubling every 18-months [1]. This means that, if we extrapolate this growth-rate, by 2015 it may reach the staggering amount of few zetabytes, 1 trillion gigabytes of information, see figure 1. The internet itself has been predicted to carry over a zetabyte of annual traffic by 2015 and may become even more pronounced as new technologies get connected to it [2].

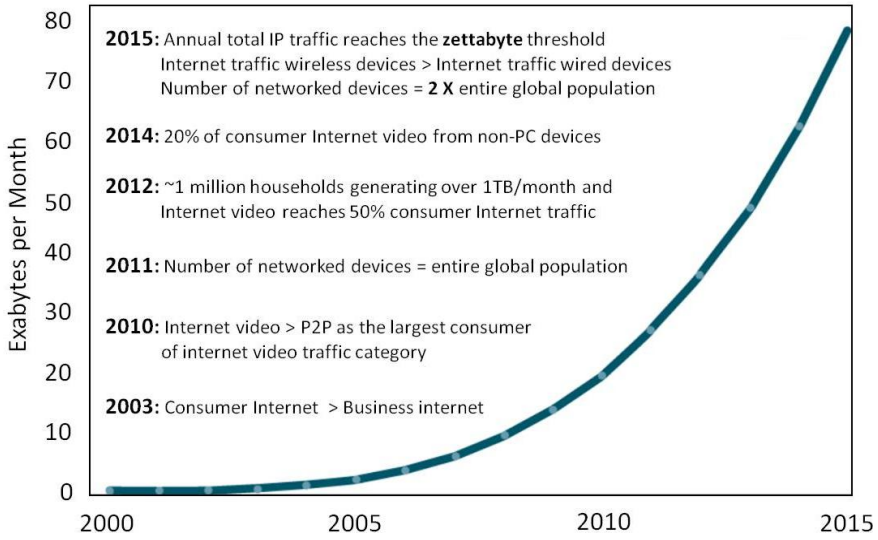


Figure 1.1: Overall traffic growth forecasts and milestones.

The 2011 CISCO study, Figure 1.1, forecasts that the volume of traffic will continue to grow, generated largely by video. Internet video will be half of the total volume of traffic that will be generated next year, 2012. The device repertoire is becoming increasingly portable, and traffic originating from Wi-Fi devices is predicted to surpass traffic from wired devices in 2015. Globally, the IP traffic will reach 245 Tbps in 2015 which is the equivalent of 204,100,000 people streaming Internet high-definition video simultaneously, all day, every day [2].

Most of these data, nowadays, flows across the Internet using different wavelengths (different colours of light), pulsing through interconnected silica or polymer fibers to form global fiber optic networks. Setting optical communication technologies at the core of the ongoing information technology era.

This data explosion has been driven by two main factors: a reduction in the cost of communications technologies and a dramatic increase in system capacity. The transmission system capacity[1] has increased from tens of Gigabits per second, in the mid 80's to tens of terabits per second today, 2011 [3]. This represents an increase in data rate of more than 4 orders of magnitude.

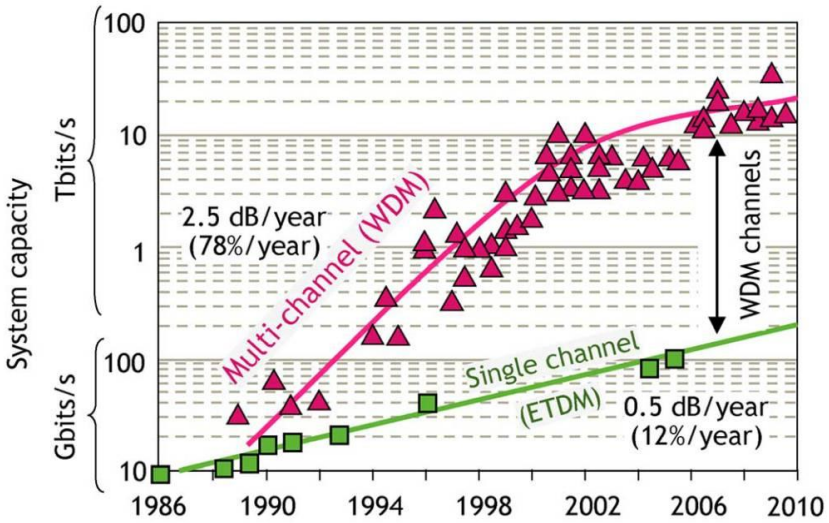


Figure 1.2: Historical evolution of record capacity. [3]

[1] The capacity of a system measures the amount of data that can be transmitted over the communication medium

The capacity evolution since the mid 80's is plotted in Figure 1.2. The lower curve in the plot indicates the transmission data rate obtained on a single optical wavelength (single colour) using electronically time-division multiplexed (ETDM) transmitters. The experienced growth rate is about 12% per year, which would have been insufficient to facilitate the bandwidth demand of modern data services that grows at about 60% per year [2].

Multi-channel technologies were developed in the early 90's and allowed parallel transmission using many optical wavelengths (many colours) on the same fiber. This enabled a growth rate in total fiber capacity of about 78% per year for over 10 years, as shown in the top plot in figure 2.

In early 2000, the capacity growth began to slow down due to both the optical amplifiers intrinsic bandwidth limitations and the dot-com bubble burst. The system capacity still is growing, about 12% per year, and this is mainly due to an increase in spectral-efficiency[2] brought by advanced modulation formats that have been replacing the existing ON-OFF Keying (OOK) modulated systems in the long-haul transport networks [3].

In addition to the long-haul communication bandwidth growth, the sustained improvements in electronic technologies (computing processing) and optoelectronic device technologies (transceivers) have opened new system services with high-capacity interconnection requirements. Such services demand communication networks operating with low latency, low power consumption and with low cost. Examples of these systems include local and storage networks, data centers, blade servers and high performance computing [4].

1.2 Optical Interconnection

The aforementioned capacity trends, highlight the increasing need for greater interconnection bandwidth and dynamic re-configurability in core, metropolitan, wide and short area (MAN, WAN, SAN) networks. These interconnection demands can be addressed, currently, using electrical switch fabrics for both electrical and optical interconnects in the current high-capacity systems [5]. However the ever increasing requirement for processing, storage and communications capacity within these systems is stressing the current electrical switches and routers.

Today's state-of-the-art core routers consume over 10kW [6] and utilize

[2] The data rate that can be transmitted over a given bandwidth in a specific communication system.

multi-rack designs in order to spread the system power over multiple racks, reducing the power density and pushing aggregate capacities to 100's of Tbps. However these systems require as many as six power-hungry optoelectronic (O-E) conversions per input/output (I/O), and multi-rack configurations which are dominated by power-hungry interface cards [7]. Thus the power consumption/dissipation and footprint increase as the number of ports and bit rate per port increase.

In state-of-the-art data centers, each rack of approximately 40 blade-servers consumes over 20kW [7] and it is connected via a Gigabit-Ethernet[3] (GbE) switch, which uplinks via a 10GbE link to a cluster switch of much higher capacity [8]. The capacity scaling of these systems translates in an increase in energy consumption, as more GbE switches are required, thereby increasing the power consumption density. As a result the thermal issues of these systems are becoming significantly more troublesome.

Architecting electronic core routers and data center switches with higher capacities continues to burden all aspects of the system design and the intrinsic technologies; including switch fabric capacity and packet processing, such as forwarding, queuing, and buffering [5]. Scaling the system capacity using electrical interconnection systems is constrained mainly by the resulting size/cost increment, stringent synchronization issues, extra de/serialisation circuits and energy consumption.

Therefore, researchers have investigated the use of optics in interconnection networks [9], [10]. Switching in the optical domain brings tremendous advantages to the network. It extends the reach of the immense optical bandwidth from the transmission systems to the switching nodes, increasing the information capacity of the network to levels beyond electronic switching capabilities. The migration of switching to the optical domain has the potential to enhance network agility, flexibility and reliability, and can make the network more cost effective [5]. This is because of the inherent advantage that optical transmission systems and switches, being effectively bit-rate agnostic, have to switch very high data-rate signals at the packet/burst level, rather than at the bit level as in the purely electronically switching systems of today [6].

Optical Packet Switching (OPS) has been proposed as a technology for better exploiting the network resources [5]. It is expected to provide greater

[3] 10GbE signaling is used to connect distributed clusters, as sending Infiniband signals across a WAN is challenging. Infiniband is more suitable inside the cluster.

bandwidth efficiency and flexibility to both long and short reach networks [10], [11]. Table 1.1 compares a number of demonstrated technology prototypes used for optical packet switching fabrics purely in terms of the optical performance. This table indicates that the inherent signal regeneration properties of electronic switch fabrics are highly attractive when moderate transmission rates are used. It also shows that static wavelength tuning switches facilitates routing by means of advanced electronic control through a passive wavelength router and, therefore, does not suffer significant optical impairments. Both systems are, however, narrowband systems with a single wavelength per port. The remaining active optical switching technologies outlined in Table 1.1 are broadband and can also incur additional optical power penalties, due to crosstalk, noise, loss, or signal impairments.

When comparing the implementation of switching technologies for broadband optical interconnects, the electronic and static wavelength routing solutions reveal significant disadvantages. Requiring additional transceivers for each wavelength imposing an undesirable power consumption and large footprint. The active switching schemes, offer the potential for low-complexity broadband routing with much more compact solutions. In particular Semiconductor Optical Amplifiers (SOA) gates offer the broadest spectral performance, without the restrictions imposed by channel blockers, directional couplers and interferometers.

Optical packet switching networks require large scale switches (16 I/O ports or bigger) with broadband and high-speed re-configurations capabilities [12] with low power consumption. The technologies shown is table 1.1 fulfil some of the requirements but not all of them. Some of them like the electronic core technology, can achieve very high connectivity but with high energy consumption (10's nJ per bit) and limited bandwidth. The active switching elements like SOAs offer broadband and high-speed reconfiguration capabilities with relatively low energy consumption (10's pJ per bit) but its scalability in port count is still under active research.

Table 1.1: Key Technologies Available for WDM Optical Packet Switch Fabrics.

Switch Technology	**Electronic Cores** [5]	**Optical Cores**				
		Static Wavelength tuning [13]	**** Reconfigurable Wavelength tuning** [12]	**Phase Modulation** [14], [15]	**Loss Modulation** [16]	**Gain Modulation** [17], [18]
Implementation	WDM Optical Circuit Switching	Fast Tunables with passive wavelength routers	MEMs-based WSS	Mach-Zehnder Directional Couplers	Channel Blockers with passive wavelength routers	SOA gates
Electrical Characteristics	× Added TX/RX	× Additional laser control	✓Low Switch Voltage	× High Switch Voltage	✓Low Switch Voltage	✓ Low Switch Voltage
Optical Characteristics	✓Signal regeneration ✓Error correction ✓Performance monitoring ✓Sub-wavelength routing	✓Low loss ✓Low Crosstalk ✓No added Noise ✓No added distortion	✓Low crosstalk ✓Low loss ✓No added Noise ✓No added distortion	× Moderate Loss × Moderate Crosstalk ✓ No added Noise ✓ No added distortion	× High loss ✓Low Crosstalk ✓Low Noise ✓Low distortion	✓ **Lossless** ✓ Low Crosstalk × 7dB Noise Figure × Distortion prone
Channel Granularity	× Narrowband fixed λ/port ✓Broadcast possible	× Narrowband fixed λ/port × No Broadcast	✓Broadband ✓Broadcast possible	× Moderate bandwidth ✓ Broadcast possible	× Moderate bandwidth ✓Broadcast possible	✓ **Broadband** ✓ Broadcast possible
Footprint	× Added TX/RX × Added de/mux	× Large footprint	× Moderate footprint	× Large footprint	✓Compact	✓Compact
Switching time	Nanosecond region	10's to 100's nanosecond	× Microsecond	10's to 100's nanosecond	Nanosecond region	**Nanosecond** to **picosecond** region
Scalability	✓Very high port count	× Small size	✓Large size	✓Large size	✓Large size	× Moderate size
Energy Consumption [19]	10's nJ per bit	1nJ per bit	10pJ per bit	1nJ per bit	10pJ per bit	80pJ per bit

SOA = Semiconductor Optical Amplifier, WSS = Wavelength Selective Switch, ** = Not for packet/burst switching

This thesis focuses on one of the key building blocks for realizing high capacity, low latency optical networking, namely a high capacity and highly scalable optical switch. Although several technologies are available for implementing such devices, the focus is mainly on Semiconductor Optical Amplifier (SOA) based switches, in particular SOA-based space switches. These switches are superior on a number of key points, as they are extremely versatile with respect to system applications (from long range networks to short range networks), have a large optical bandwidth, and can be integrated. Still some challenges remain to be investigated such as scalability integrity, data capacity limits and energy efficiency.

The work combines a physical layer perspective with a system level perspective on SOA-based optical switches, where experimental demonstrations are supported by a physical modelling to face some of the challenges mentioned. The numerical description provides valuable insight into the performance, and possible optimization of ultra high capacity SOA-based switches. In the next section, the main contributions of this research work are presented.

1.3 Novel Contributions

- Demonstration of a novel 2x2 switching structure optimized to serve as a building block for high port-count switches using multiple stages of this element. This novel switch structure minimizes the number of electrodes, reducing the control complexity of the switch. This was demonstrated, for the first time ever, in an all-active photonic integrated 2x2 SOA-based switch using quantum dots (QD) emitting in the 1550nm telecommunications window.
- Demonstration of the first all-active photonic integrated multistage 4x4 QDSOA-based switch in the 1550nm emission region. Operation characteristics and results experimentally observed in such devices make them highly promising for larger scale monolithic photonic circuits.
- Demonstration of the first active-passive monolithically integrated multistage quantum well (QW) 4x4 SOA-based switch working at serial line rates of 160 and 320Gbit/s. This represents a highly promising route to large scale monolithic optoelectronic interconnection circuits operating at ultrahigh line rates with energy efficient signal processing.
- The capacity limitations of scalable SOA-based multistage switches are theoretically studied for the first time. Experimental findings are used to calibrate and compare the numerical models. 640Gbp/s transmission is

predicted.

- A new 16x16 switch architecture has been proposed, for SOA-based switches, optimised for a non-blocking operation with a low number of SOA switching elements. This switch uses a low number of switch cascades and a new set of miniaturised building block to make it compact.

1.4 Thesis Outline

In this dissertation work, I combine physics knowledge of materials and quantum dots with engineering and device design skills to fabricate and assess state of the art photonic integrated switching circuits. I link the knowledge acquired from these devices with deep understanding of the implications and concepts of ultrafast optical communications networks to design and experimentally assess monolithic interconnects operating at ultrahigh line rates up to 320Gbps (for a total potential data capacity of 1280Gbps). The implemented Multi-Quantum Well (MQW) multistage device represent one of the most complex multistage InP photonically integrated circuits ever reported; with up to four SOA stages. To provide further insight into the scaling of line rate and connectivity for larger scale integrated switching circuits, simulation studies are performed.

This dissertation will discuss through the use of different materials and integration technologies that photonic integrated SOA-based optoelectronic switches can be scalable in either connectivity or data capacity and are poised to become a key technology for very high-speed applications. In Chapter 2, the optical switching background with the drawbacks of optical switches with electronic cores is discussed. The current optical technologies for switching are reviewed with special attention given to the SOA switches. Chapter 3 discusses the first demonstrations using quantum dot (QD) material to develop scalable and compact switching matrices operating in the 1.55μm telecommunication window. In Chapter 4, the capacity limitations of scalable quantum well (QW) SOA-based multistage switches are assessed through experimental studies for the first time. In Chapter 5 theoretical analysis on the dependence of data integrity as ultrahigh line-rate and number of monolithically integrated SOA-stages increases is discussed. Chapter 6 presents some designs for the next generation of large scale photonic integrated interconnects. A 16x16 switch architecture is described from its blocking properties to the new miniaturized elements proposed. Finally, Chapter 7 presents several recommendations for future work, along with some concluding remarks.

Chapter

2 Optical Switching

This chapter introduces optical switching and discusses its technologies advantages and disadvantages. This chapter also discusses the promises that photonic integration technologies and the use of new materials bring.

2.1 Introduction

The current technologies in the interconnection network start to limit the possible "universal access" for Internet and data communications [20]. The available, several hundred gigabits/second, capacity in optical fibers, is limited by the electronic low speed "intelligence" or processing at the interconnection network.

To overcome this limitation, optical high-speed transmission streams are broken into several lower-speed electronic data streams operating in parallel. Such optoelectronic conversion and the use of more and more electronic signal-processing in parallel to scale the system, consume considerable energy and increase the system footprint as the bit rate and the number of I/O ports increases [21]. This has increased the system power demands and pushed aggregate capacities; creating an "energy-footprint" bottleneck in the interconnection network [22]. Therefore, it is increasingly desirable to introduce highly functional, low power and large scale optical interconnection technologies with the potential to enable high capacity-bandwidth systems to scale in a different manner than today's systems.

2.2 Optical Switching

It is clear that the increasing demands in interconnection bandwidth can be met by using higher data rates and/or more data links. The use of multi-channel schemes, i.e. Wavelength Division Multiplexing (WDM), to exploit today's system bandwidth [23], [24], created the challenge of switching the large number of wavelength channels that it enables. Each wavelength channel can

transmit bit rates of 2.5, 10 and 40Gbps that are now available and soon bit rates of about 100Gbps will be available commercially [25]. Since switching in these networks still is performed by electronics, optical to electrical to optical (O-E-O) conversions are essential at switching centres and cross-connect nodes. These electronic switches dot not work at high rates, so incoming signals have to be not only converted from optical to electrical form but also have to be demultiplexed to lower bit rates. In conclusion, the use of electronic cores for switching lacks scalability and suffers from serious performance bottlenecks rising power consumption and cost. To omit these power-hungry, expensive signal conversions and demultiplexing inconvenients, switching systems based on optical technology have been implemented in research laboratories and industry [9], [26].

Optical switching, enables optical signals to be switched directly from inputs to outputs without conversion to electronic form. Switching in the optical domain brings tremendous advantages to the network. It extends the reach of the immense optical bandwidth from transmission systems to the switching nodes, increasing the information capacity of the network to levels that are beyond reach with electronic switching. The migration of switching to the optical domain has the potential to enhance network agility, flexibility and reliability, and can make the network more cost effective. An additional benefit of the use of optical switching technologies is thought to be a significant energy efficiency improvement within data centers and telecommunication routers. This is the reason behind this work, to assess the possible energy efficiency improvement while pushing the technology limits.

Different technologies are being used to construct optical switching elements. These elements exploit various optical effects in various materials. In general, these technologies can be grouped into two main categories [5]: light-guided based switches and free-space switches. Each category can be further divided into different classes, depending on the physical phenomena used to switch the light between inputs and outputs.

It must be noted that regardless of the physical effect responsible for the switching process, which is used as platform for this categorization, external control of the switching device is electrical in the vast majority of cases. Electrical control is used to trigger electro-optic effects, to generate acoustic surface waves, to supply heating energy, to actuate switching systems and to control SOA gates. These five categories summarizes most of the optical switching technologies which have received considerable attention from both academy and industry. Other technologies which do not perfectly fit within this classification may also exist in the literature, but its characteristic are not

reviewed in this thesis due to technological difference such as very different packaging approaches, e.g. bubble jet switch [27], non linear directional coupler [28], moving fiber [29], moving beam[30], thermo-capillary switch [31]and holographic switches [32].

We can distinguish: electro-optic switches, acousto-optic switches, thermo-optic switches, opto-mechanical, SOA-based switches. Detailed description of different technologies and examples of optical switching elements can be found in Table 2.1.From this table it is possible to conclude that although the opto-mechanical technology offers the best scalability and signal integrity its main limitation relies in its reconfiguration time which is in the order of microseconds. This limitation becomes important when routing high bit rates. On the other hand Optical Amplifier-based technologies offer one of the fastest reconfiguration times, lossless operation. Although this technology has very important characteristics there are still challenges to solve such as cost, scalability and footprint.

Table 2.1:WDM Optical Packet Switching Fabrics, Optical Mechanisms and Performance Comparison.

Technology	Material	Mechanism	Switching time	Scalability	Signal Integrity
Electo-optic	Lithium-Niobate [33-35]	Refractive Index Modulation	Nano-second region	✓ Low power consumption × Moderate footprint ✓ Large port switch size	✓ Low PDL × Moderate crosstalk × High insertion loss
	Liquid Crystal [36-38]	Birefringence + Polarization Control	Micro-second region	✓ Low power consumption × Large footprint ✓ Large port switch size	✓ Low PDL × Moderate crosstalk × Moderate insertion loss
Acousto-optic	Lithium-Niobate [39], [40] III-V SCs [41]	Refractive Index Modulation + Polarization Control	10's to 100's of nanoseconds	× Moderate power consumption × Moderate footprint (III-V SCs) × Small port switch size	× Low PDL × High crosstalk × High insertion loss
Thermo-optic	Silica [42], [43] Polymer [43], [44]	Refractive Index Modulation	Millisecond region	× High power consumption × Large footprint × Moderate port switch size	× Low PDL × Low crosstalk × Moderate insertion loss
Opto-mechanical	MEMS [45-49]	Actuator to change the mirror reflection angle	Millisecond [50-52] Microsecond [53]	✓ Low power consumption × Compact but moving parts limits reliability ✓ Very large port switch size	✓ Low PDL ✓ Low crosstalk ✓ Low insertion loss
Optical Amplifier-based	III-V Semiconductor Optical Amplifiers [54]	Refractive Index Modulation + Gain Modulation	**Sub/Nano-second region**	× Moderate power consumption ✓ **Compact footprint** × Moderate port switch size × Scalability limited by noise	✓ Low PDL demonstrated ✓ Low Crosstalk × 7dB Noise Figure × Distortion prone ✓ **Lossless**

SCs = Semiconductors, PDL = Polarization Dependent Loss

2.3 Optical Switching and Contention

The nodes increasingly deployed in telecommunication are Optical Add/Drop Multiplexers (OADMs) and Optical Cross-Connects (OXCs). Different architectures of OADMs and OXCs were proposed in the literature and implemented in practice [55]. Some of them use optical switching fabrics to switch fibres or wavelengths. Most of the implemented optical fabrics use MEMS switches because they are relatively cheap and mature [51]. But MEMs have the drawback that their switching time is rather slow, and cannot be used in Optical Packet Switches (OPS). Much faster switching elements are needed in OPS. However, fast optical switches are at the moment very expensive and not mature.

The compromise between the circuit switching and packet switching is the Optical Burst Switching (OBS). OBS is packet based, which makes it potentially more bandwidth efficient than OCS. The technological requirements to implement OBS are relaxed in comparison to those of OPS. In an OBS network, packets are assembled into larger data bursts (DB) than in pure OPS. In packet (burst) switching, one of the important functions of the switch it to solve the output contention problem.

This contention appears when two or more packets are to be directed to the same output at the same time. The output contention can be solved in the space, wavelength, or time domains. In the space domain, one packet is directed to the desired output, while other competing packets are directed to other outputs. When wavelength multiplexing is used in the output ports, contention may be solved in the wavelength domain by sending contention packets to the same output but on a different wavelength. This requires wavelength conversion capability in the switching node. Finally, when one of the competing packets is sent to its original output, other congested packets are directed to the memory and delayed for some time. This is call buffering and it is an important functionality in optical burst-switched networks. It allows the temporal storing of data bursts or packets to resolve contention for the switch outputs. These contention challenges have to be addressed in the design of such optical packed switched networks. Nowadays these challenges are assumed to be solved in the electrical domain at the edge of the optical switch.

2.4 Optical Switching Technologies with SOAs

Most of the proposed approaches to create highly functional, low power and large scale optical switching technologies implement semiconductor optical

amplifier (SOA) as gates [54]. The operation principle of SOA gates is the optical gain manipulation when an electrical current is injected into the SOA active region.

Using optical gain for switching enables the use of the "broadcast-and-select" method, which is the method used "at the heart" of the proposed circuits in this thesis. In this method, the input signal power is divided into two or more paths, i.e."broadcast", and SOA gates are used to "select" any of the paths. The optical signal in the path with the SOA turned ON will be amplified, and thus selected, while the optical signal in the path with SOA turned OFF will be attenuated. These SOA-based optical switches offer the potential for a broadband, fast reconfigurable and loss-less routing [56] with electrical energy consumption nearly independent to the line-rate or data format [6] thus breaking the electronics' vicious link of rising line-rate and increasing energy consumption.

Extensive research into optical switching has been carried for various network applications. The SOA has been identified as a useful switching technology for packet switched long reach and short reach interconnection networks. The key projects using SOAs for WDM packet and wavelength routing switches are listed in the Table 2.2. To achieve higher capacity-bandwidth systems, recent SOA-based test-bed studies have focussed on the routing of tens of wavelength multiplexed 40 Gbps data signals over single and multiple stage networks of discrete switching elements [17], [57-61] and by using nonlinearities in discrete SOAs (e.g. cross gain and/or cross phase modulation) higher line rates, ultrafast routing and ultrahigh speed optical demultiplexing has been achieved [62-64]. Remarkable challenges still remain in terms of cost, connectivity, and footprint, but photonic integration of these interconnection technologies [65], [66] is now striving to deliver in many of these areas [67].

Table 2.2: Key projects using SOAs for WDM optical packet switching.

Long Reach Networks (Backbone, WAN and MAN)	
Key to Optical Packet Switching (**KEOPS**), 1998, European [68]	All-optical transport and switching platform for high capacity applications Wavelength routing switch + 3R optical regeneration and packet header rewriting capabilities
Wavelength Switched Packet Network (**WASPNET**), 1999, UK [69]	Wavelength routing and network control + Contention resolution through wavelength conversion + Optical Buffering with FDL in a switch with recirculation configuration
Hybrid Optoelectronic Ring Network (**HORNET**), 2003, USA [70]	WDM optical packet transmission over a ring MAN network Fast tunable TXs + wavelength routing switches + media access control to avoid packet collision
Data and Voice Integrated over DWDM (**DAVID**), 2003, European [9]	Highlights the potential of optical packet switching for high capacity MAN and WAN networks A non-blocking 16x16 SOA based switch optical crossconnect for space and wavelength selection A 32-gate SOA switch module for high speed packet switching
Short Reach Networks	
Smoothed Optical Asynchronous Time Division Packet Switching (**SOAPS**), 2005, UK, Intel [71]	High capacity transparent optical packet switch with low latency and low cost using commercially available optical and electrical components. 3x3 SOA-based switch fabric + gigaEthernet cards + media access control + edge electrical buffering for contention resolution
Data Vortex, 2007, USA, Columbia University [72]	Architecture uses deflection routing to eliminate optical buffering. 12x12 switch with 2x2 SOA-based nodes arranged in a hierarchical switching structure
Scalable Photonic Integrated Network (**SPINet**), 2007, USA, Columbia University [58]	Architecture for optical packet switched interconnection networks for LAN, SAN and HPC systems 4x4 3-stage optical packet switch with: optical address encoding/decoding + contention resolution + physical layer acknowledgement transmission and path distribution.
Optical Shared Memory Supercomputer (**OSMOSIS**), 2007 USA Corning and Europe IBM [10]	64-node wavelength switched network for high performance computing applications. 2048 port optical switch using a fat-tree connected 64-node switch architecture +OEO conversion and electrical buffering between the switch stages.

2.5 Photonic Integration: A viable solution

Integrating multiple photonic functions on a single chip requires miniaturized optical circuits that consists of passive components (e.g. waveguides) as well as active ones (e.g. light sources, amplifiers, detectors). These components must be manufactured on the surface of a thin substrate of semiconductor material that has been optimized for generating and transporting laser light. The integration of optical devices on semiconductor material promise advantages such as: less power consumption, speed, robustness, potentially cheaper and in some cases compatible with electronic integration technologies [20]. Characteristics that can make photonic integration a cornerstone in the future of optical communications.

2.5.1 Integration technologies

The photonic integrated circuits (PICs) have been fabricated in a variety of material systems, including elemental semiconductors (Si- and Ge-related), compound semiconductors (InP and gallium arsenide (GaAs)-based), dielectrics (SiO_2 and SiN_x -related), polymers and nonlinear crystal materials (e.g. $LiNbO_3$) [73]. Each of them exhibit desirable but discrete functionalities. For example, InP and GaAs are good materials for light sources, while silica- and Si-based waveguides exhibit at least an order of magnitude lower propagation loss than their group III –V counterparts. The reality is that both, InP and Si, offer advantages and disadvantages when creating the desired highly functional, low cost, low power and large scale photonic integrated interconnection technology. Three major platforms have been exploited and developed.

The Si-platform has shown promise for large-scale integrated circuits mainly due to its claimed potential compatibility with the standard complementary metal-oxide semiconductor (CMOS) integration process, holding the promise to enable both optical and electronic integration. The relative maturity and ease of manufacture of this technology has led to the increasing use of silicon-based planar lightwave circuits (PLCs) for integrating functions such as reconfigurable optical add/drop multiplexers (ROADMs) [74]. However, the practical difficulties associated with implementing high-performance active optoelectronic functions such as lasing and modulation, generally limits its usefulness to the integration of mainly passive optical devices.

The immature, but promising, III-V/Si heteroepitaxy platform, nowadays is being developed to tackle the problem of low intrinsic optical gain in silicon. This is done through the coupling of the high single-pass direct-bandgap gain of III-V materials with the CMOS compatibility of high-index-contrast silicon

waveguides [75-77].

The InP-platform supports light generation, amplification, modulation and detection. It enables all the key high-value optoelectronic functions required to be integrated on a single substrate maximizing potential cost reduction. It has demonstrated the ability to reliably integrate both active and passive optical devices operating in the 1310nm or 1550nm telecom windows with the capability of mass production using standard high-yield, batch semiconductor manufacturing processes [74].

2.5.2 Quantum confined materials

The exploration of novel structures at the nano-scale, such as quantum well (QW) and dots (QD), and how to make them useful for optical telecommunications is especially exciting as it is believed that these materials will open the way for smallest, most complex, least power-consuming and fastest photonic integrated devices. Bringing us closer to the goal of a vastly superior network performance [20]. Researchers studying semiconductor laser and amplifiers have improved the performance of these devices by altering the density of states through higher dimensional carrier confinement. From bulk, QW to QD.

In a regular bulk material, no carrier confinement is present and the density of states increases smoothly as the square root of the energy. A bulk SOA device requires high bias current levels because the amount of carriers needed to reach gain is only achieved after first filling the lower energy levels [78].

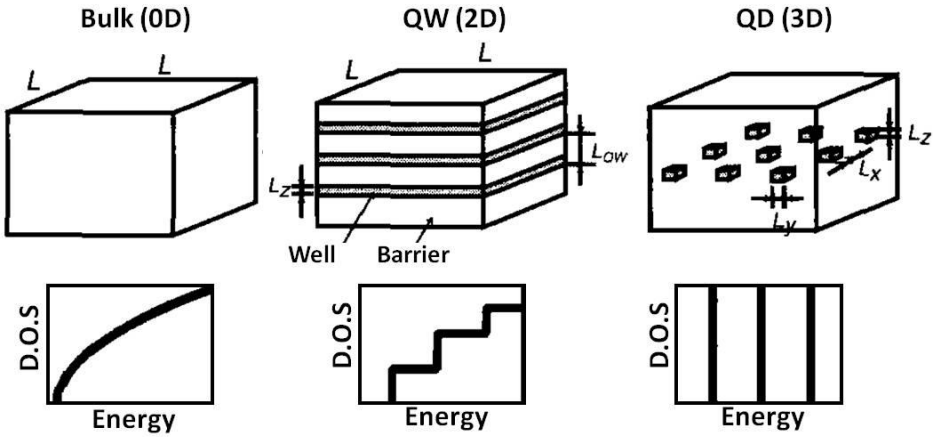


Figure 2.1: The density of states for bulk, QW and QD structures. Carrier Confinement Bulk (0D), QW(2D) and QD(3D) [79].

In a QW material, the carriers are confined in two dimensions (2D) and the density of states is described by a Heaviside step function of the energy. A lower operation bias current, in comparison to bulk materials, is achieved in QWs because they provide gain from the first energy level at the bottom of the band. This 2D carrier confinement enables a superior performance at higher temperatures and a higher modulation bandwidth [78]

In a QD material, the carriers are confined in three dimensions (3D) and the density of states is described by an ensemble of delta energy response [79]. Recent development in QD-SOAs have shown exciting attributes that are desirable for optical switches and are enabling new opportunities for large scale photonic interconnection networks. These attributes include a fast reconfiguration response [80], low distorsion [81], low noise figure (<5 dB [81]), high output saturation power (23dBm) and potential for uncooled operation [82-84] highlighting the potential of the QD SOA materials for enhanced performance in high capacity and high port count data routing applications.

2.5.3 Towards High Capacity SOA-Based Switches

Challenges in new materials, optical device designs and overall system architectures are being faced to produce the desirable impact in future high capacity telecommunication systems.

Photonic integration of SOA-based switches improves their routed signal integrity and energy efficiency. The photonic integration of these devices reduces optical losses by minimising the number of on-off-chip connections. This additionally improves noise performance and reduces operating gain for the SOA gates. This is important as the bias current used for amplification, non-radiative and spontaneous recombination ultimately determines the energy consumption. The use of energy-hungry temperature controllers in SOA integrated circuits is importantly reduced through epitaxial designs that enable an enhanced electronic confinement and therefore excellent electronic injection efficiency at high temperature [85], [86].

The race for high capacity, high connectivity switching circuits using SOA-based devices has demonstrated integrated InP SOA-based interconnection sub-systems, in which 40 Gbps transmission has been achieved for multi-wavelength transmitters [87], tuneable wavelength convertors [88], and two-input two-output switch matrices [89]. However, data routing integrity has mainly been studied for single stage circuits, and multi-stage networks of switches are required to scale the network connectivity. A recently reported 3-stage monolithically integrated 16x16 Clos network routing 10 Gbps data [90]

represents the most complex circuits reported to date. Here data rates were limited by signal degradation from noise accumulation and gain saturation due to the all-active integration approach followed in the fabrication of the device

2.6 Summary

The increasing capacity requirement in interconnection networks creates a problem in the switches with electronic cores. Optical switching without electrical conversion has number of advantages such as capacity bandwidth with good scalability in power and costs. Among the optical switch technologies, the SOA with its broad bandwidth, moderate power consumption and nanosecond switching speed has the highest potential to meet the requirements of future interconnection networks.

Optical switching with SOAs, however, suffers from signal distortion, specially at low data rates, and amplified noise that degrades the data integrity. The use of QD materials together with photonic integration technology promises interconnection technologies with exciting attributes. These attributes include high gain [81] and output power saturation power, high switching speeds [91], low penalty performance [92] and enhanced temperature stability [93]. Their high output saturation power relaxes the power budget in multistage switches improving their cascadability performance. The uncooled operation will improve their hardware and energy efficiencies, leading to cost savings. In the next chapter, the first experimental studies of monolithic quantum dot SOA-based multistage switches operating at 1550nm are presented for the first time.

Chapter

3 Monolithic QDSOA Based Switches

This chapter is based on the publications [94-98] made about this topic during this Ph.D project. This chapter describes the impact that monolithic cascaded quantum dot SOA-based switching devices could have when scaling such devices to higher number of connections.

3.1 Introduction

Photonic integrated switches using SOAs as gates have been demonstrated using broadcast-select [99] and cross-point architectures [100]. However, such approaches are complex to scale, with numbers of waveguide crossings and multiple control signals increasing rapidly with connectivity. The epitaxial design for the mentioned SOA-based switches has commonly impaired saturation properties and compromised performance at high data rates.

Research into quantum dot (QD) semiconductor optical amplifiers (SOAs) has shown exciting possibilities for their use in optical switching applications. Characteristics such as, multi-Terahertz bandwidth, low distortion, low noise figure [81], fast gain recovery [80] and potential for uncooled operation [84] make them a promising building block for future hardware-efficient photonic switching networks. In this chapter, the developed monolithic 1.55μm QD-SOA switches will be described. The space switch design and fabrication process will be described before its static and data routing characterisation is presented.

3.2 QD SOA Amplifiers and Switches

The mentioned quantum dot characteristics (e.g. massive bandwidth, low distortion) and good cascaded performance [101] make the QD-SOAs extremely interesting candidates for the advanced optical switch fabrics

required in the next generation low-latency, high-bandwidth interconnection networks. To this end, some research groups have done some pioneering research. The first monolithic QDSOA-based 2x2 switch operating in the 1300nm spectral window has been demonstrated by the University of Cambridge together with NL Nanosemiconductor GmbH[4] and it has shown negligible data degradation, 0.1dB power penalty, for 10Gbits/s data routing [92].

In this chapter, the first demonstrations of QDSOA-based switches operating in the 1550nm telecommunications window will be presented, showing negligible signal degradation with excellent power penalties of the order 0.2dB and 0.4-0.6dB for 2x2 and 4x4 switching circuits, respectively [94], [98]. In this section the all-active layer stack is described together with the fabrication process. Then the switch designs and characterisation details will be presented.

3.2.1 QD Fabrication Technology

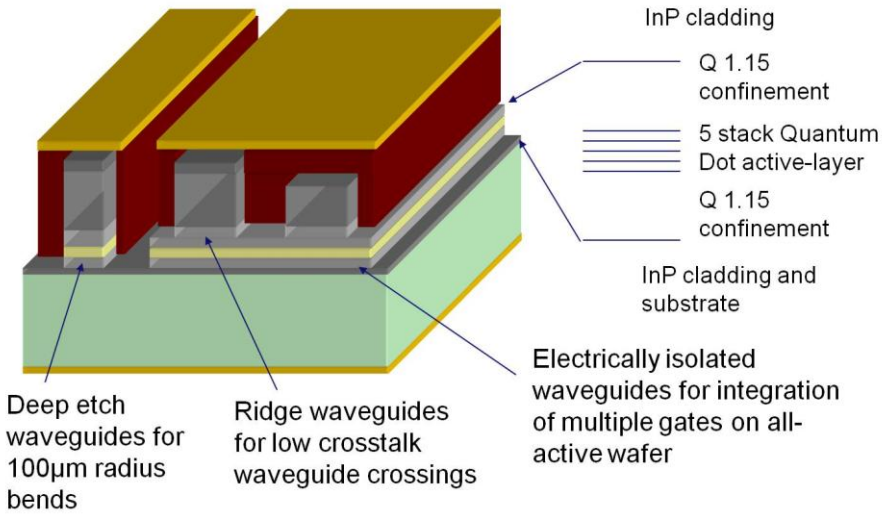


Figure 3.1: All active fabrication technology with QD material.

The fabrication of a semiconductor integrated optical device consists of two main steps: the semiconductor wafer growth with a specific layer stack and the fabrication of the optical devices on the grown wafer. The fabricated circuits have been devised and prototyped on five stacked InAs QD active layers

[4] In 2007 the company name changed to INNOLUME

embedded in a *Q*1.15 InGaAsP separate confinement heterostructure with an ultrathin GaAs interlayer underneath each QD layer to control the emitted wavelength. A single step all-active epitaxy is used. The width, height and surface density of the QDs are: 30-60nm, 4-7nm and ~$3x10^{10}$ cm^{-2}, respectively [102], [103]. Bottom and top claddings are 500nm *n*-InP buffer and 1.5µm *p*-InP, completed by a 75nm *p*-InGaAsP contact layer.

The fabrication process follows a three step etching with tailored photolithographic masks enabling the deployment of shallow, deep and isolation waveguides throughout the circuit. This facilitates: low divergence waveguide crossings for low crosstalk crossovers, tight waveguide bends of down to 100 microns for ultra-compact circuit layouts and electronically isolated regions with isolation exceeding 10kΩ; all within the same circuits. The planarization has been performed prior to gold evaporation and plating, see Figure 3.1. The devices have been mounted as-cleaved, epoxy bonded to patterned ceramic tiles and wire bonded for assessment.

3.2.2 Single-stage- 2x2 QD-Switch

The first 1.55µm highly scalable two-input, two-output quantum dot optical amplifier crossbar switch has been proposed, fabricated and demonstrated exhibiting negligible power penalty when routing 10Gbit/s data, providing an important building block for larger switch matrices.

3.2.2.1 Design

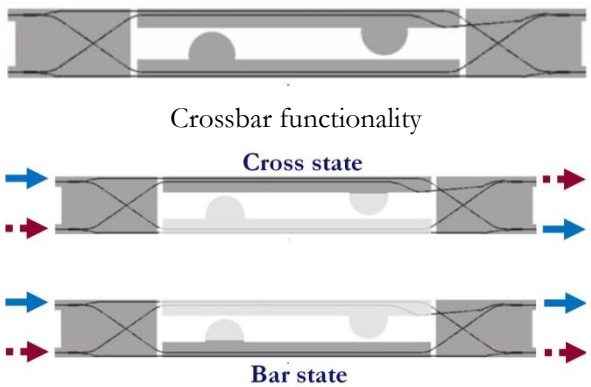


Figure 3.2: Top Schematic design. Bottom Crossbar functionality

The implemented device is a 2x2 broadcast and select tree-architecture implemented into a cross bar circuit. In a crossbar switch the optical paths

between input and output are made by enabling either the cross or the bar state. The bar state directly maps the input ports to the output ports. In the cross state the inputs are not mapped directly to the outputs, they are interchanged. For clarity, Figure 3.2, coloured arrows are used to distinguish between input ports. In the bar state the upper input port is mapped directly to the upper output port and in the cross state the upper input signal is mapped to the lower output port.

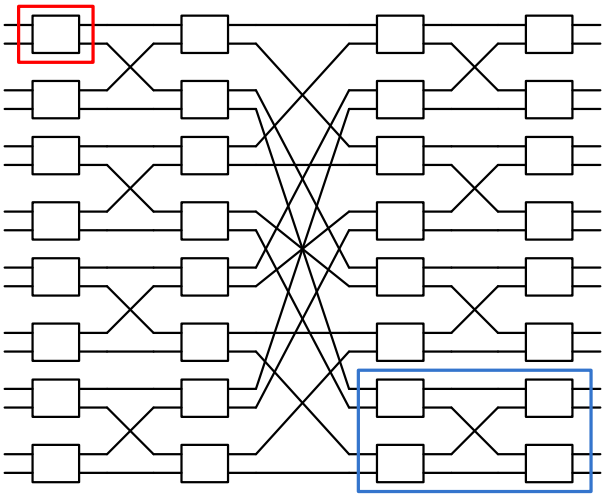


Figure 3.3:Multistage architecture for larger port count switches. 16 port butterfly network using the presented switching block.

The 2x2 crossbar circuit schematic, shown in Figure 3.2, incorporates a novel electrode geometry that is specified to address common waveguides, simplifying control and minimising the number of electrical connections and size. This is extremely important since these circuits might be implemented as building blocks of larger multistage matrices, as shown in Figure 3.3. In this figure a 16-input 16-output switch is implemented using 2x2 switching elements. Thus to create hardware and energy efficient switching devices it is important to reduce the electrode count to reduce control complexity and energy consumption.

The top view scanning electron micrograph of the fabricated device is shown in Figure 3.4. The optical paths are implemented with a combination of multimode interference splitters (MMI) and combiners located within the input and output regions. The fabricated two-input, two-output crossbar is 3.2mm in length with gate length of 1.4mm.

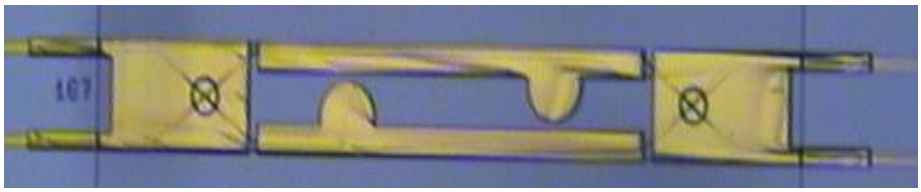


Figure 3.4: Monolithically integrated crossbar switch.

The input and output waveguides are placed on a 0.25mm pitch for ease of fibre access. A crossing is implemented within output electrodes using tight bend radius 100μm curves in combination with shallow-etched orthogonal crossings. This allows the area required for crossings to be significantly reduced.

3.2.2.2 Characterisation

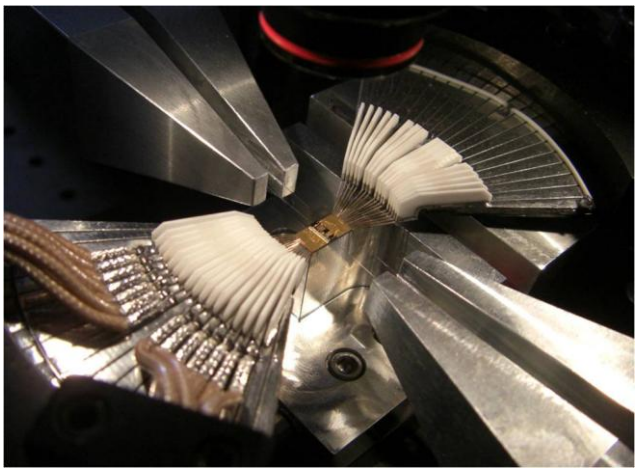


Figure 3.5: Characterisation set-up.

In the experimental characterisation setup, Figure 3.5, multi-pin probes are used in combination with a reconfigurable electronic multiplexer to connect the current sources. The circuit was assessed on a temperature controlled stage at 17°C and four lensed fibres were used to characterise all the switching paths.

The mean fibre coupling loss between fibre and chip is estimated from photocurrent measurements to be 8dB per facet, including an estimated 1.5dB loss through the cleaved facet. To estimate the off-state loss, direct power measurements of output signals with respect to an input signal with in-fiber power of 0dBm at 1550nm were performed. This procedure gave a typical 30dB off-state fibre-coupled loss. The expected off-state fibre-coupled loss was

calculated to be 25dB (8dB coupling loss/facet + 3.5dB/MMI + 6.5dB/cm waveguide loss). The QD devices shown a high polarisation dependant loss making them transparent in the TM state of polarisation. In following sections this excess loss is discussed together with the low QD gain achieved within these devices

3.2.2.3 Data Routing

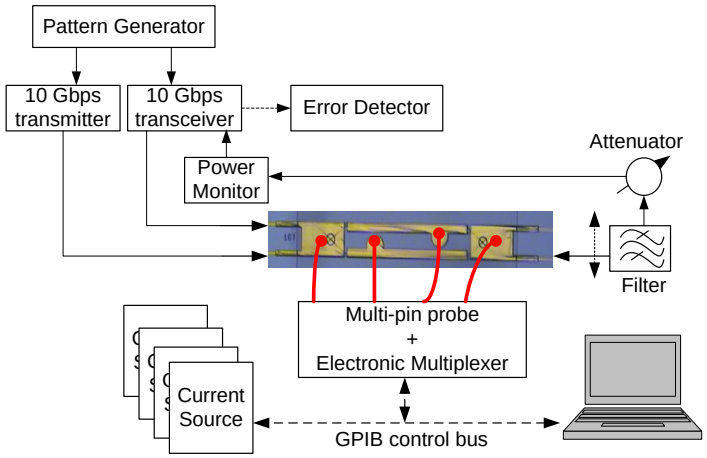


Figure 3.6: Switch experimental arrangement. Polarisation controllers not shown

The experimental arrangement to assess the integrity of routed data is shown in Figure 3.6. Power penalty measurement was performed using a XFP-Finisar transceiver to measure a 10 Gbps data rate signal with a 2^{31}-1 pseudorandom bit sequence. The polarisation is carefully aligned and additional fibre amplification is provided to overcome fibre chip coupling losses and on-chip losses from splitters and combiners. In-fibre input powers of 10dBm at 1550nm are used. Input and output sections in Figure 3.4 are biased at 160mA.

Off-state and On-state gate currents are set to 0mA and 120mA, respectively, enabling switching extinction ratios within 23.8 and 24.5dB for the switch paths. The output signal from the switch circuit is optically filtered for broadband noise rejection to assess the data routing performance.

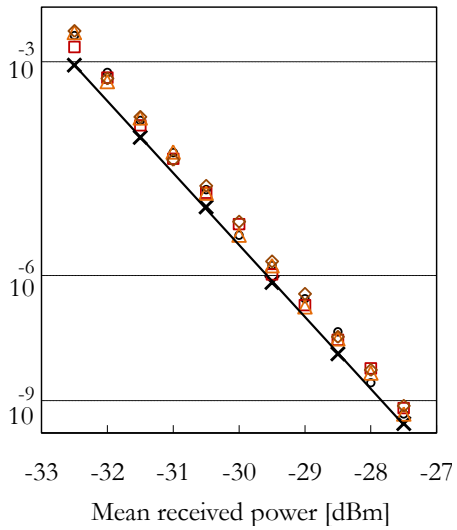


Figure 3.7: Bit Error Rate for each switched path

Power penalty performance is assessed from the bit error rate dependence on received power shown in Figure 3.7 where the trend-line is given for back to back data to assist the eye. Symbols describe the results obtained when data is input into both top (squares and circles) and bottom (triangles and diamonds) waveguides when routed though a bar or cross state, respectively. Path dependent power penalties of 0.15 to 0.25dB are observed with no evidence of distortion.

3.2.3 Multistage 4x4 Switch Matrix

Many of the single stage SOA architectures proposed have scaled poorly. Mainly because their insertion loss increases rapidly as the number of switching elements increases. Multistage switching networks are known to enable considerable increases in interconnectivity, but there is little work into the feasibility of monolithically cascaded meshed amplifier circuits. As the number of ports increases, in SOA-based photonic integrated switch, limitations as noise, distortion and crosstalk become more important and need to be studied to implement solutions. To date, crosstalk studies have been restricted to discrete components [104], steady state integrated circuits [105], and simulation [106]. Therefore it is important to study the technology limits while assessing highly scalable and high capacity photonic integrated switches.

In this section, a study on 10Gbit/s data routing and meshed interconnection crosstalk is addressed, for the first time for QD circuits, to assess the impact of monolithic cascaded switching circuits.

3.2.3.1 Design and Fabrication

The 4x4 multistage switch was implemented using the same five stack quantum dot active layer and fabrication process described in previous sections. Electrically-isolated deep and shallow amplifying waveguides were implemented in the required interconnection topology. Multimode interference (MMI) couplers are employed as splitters and combiners with separately contacted gate waveguides enabling the reconfigurable routing. Deep etched curved waveguides with minimum bend radii of 0.1mm provide compact interconnection.

The switch architecture is conceived to simplify both electronic and photonic interconnection with an electrode geometry, again, specified to address common waveguides, thus simplifying control and minimising the number of electrical connections. A modified version of the novel architecture and highly scalable 2x2 switch proposed in the previous section is used as a building block in the designed of the first 1.55μm multistage 4x4 switch matrix.

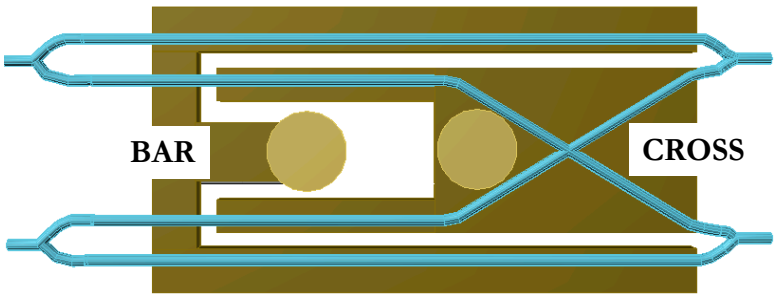


Figure 3.8: 2x2 crossbar electrode connections

The electrode connections that allow two operational states for each 2×2 crossbar switch element: *cross* and *bar* are shown in Figure 3.8. One plated electrode is implemented for each pair of gates enabling a considerable reduction in electrical complexity. Only two circular bond pads are therefore provided for each crossbar element.

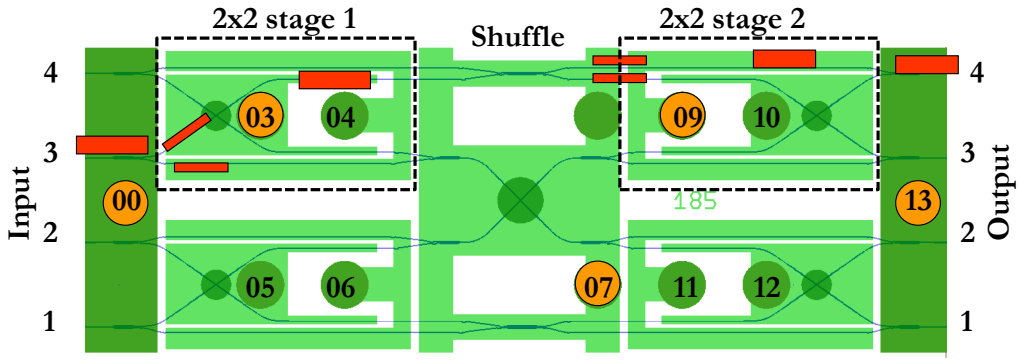


Figure 3.9:Dual stage 4x4 design circuit.

The dual-stage four-input four-output (4×4) circuit, shown in Figure 3.9, is 3.2mm in length with gate length of 0.8mm. The input and output waveguides are placed on a 0.25mm pitch for ease of fibre access. The paths are implemented with a combination of multimode interference splitters (MMI) and combiners located within the input, shuffle and output regions (pads 00, 07 and 13). These are interconnected by two stages of cascaded SOA gates (pads 03-06 and 09-12) which are electronically configured. To fully operate the switch matrix, only five pads need to be in the on-state at any given time.

A reduced shuffle network is implemented at the centre of the switch to interconnect four crossbar switch elements. Allowing any optical input to be directed to any optical output by means of electronic addressing, although not necessarily simultaneously. This blocking behaviour might be addressed with an efficient packet time-scale media access protocol. The 4×4 routing map enables non-blocking operation as part of a larger scale network such as the butterfly in Figure 3.3 and provides the basis for studies into cascaded switches in this work. The connections for the switch matrix including three of the mask layers is shown in Figure 3.9. This 4x4 all-active switch schematic includes the SOA waveguide layer in dark green, *p*-metallisation denoted by the light shading (green), and regions with shallow SOA waveguides denoted by the dark shading (green). The mask layer for the electrical isolation is not shown, the InGaAs capping layer is removed between the metal areas for this purpose.

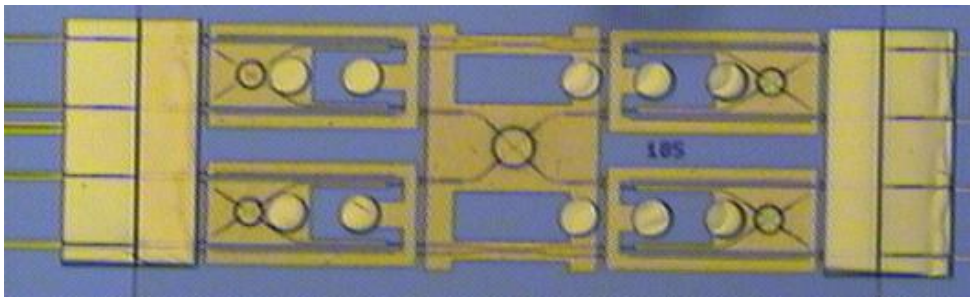


Figure 3.10: Photograph of fabricated device.

The physical implementation photograph of the switch topology is shown in Figure 3.10. This top view highlights the narrow dark waveguides, the lighter shaded gold electrodes and the dark background of exposed InP.

3.2.3.2 Characterisation

The switch is assessed using the same setup in Figure 3.5 where a multi-probe to the ceramic tile in combination with a reconfigurable electronic multiplexer are implemented. Forward series resistance values between 4-6Ω are measured depending on the addressed waveguides with one electrical fail at pad 5. Electrical isolation is measured to be in excess of 100kΩ for all electrode combinations. Initial characterisation is performed without electrical bias as the quantum dot epitaxy enables such characterisation and this is expected to provide clearer insight into on-chip component performance. The circuit is mounted on a temperature controlled stage at 17°C. Lens ended fibres were used for the measurements.

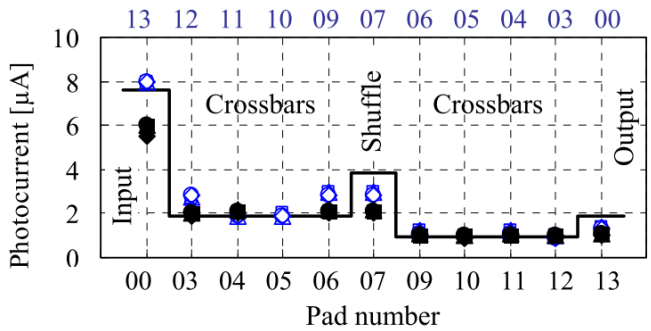


Figure 3.11: Measured photocurrent generated at each pad or electrode when light is independently input on both sides of the circuit. The solid line shows the predicted values. There is no electrode powered or biased and the photocurrent at each electrode pad generated by the input light

Photocurrent measurements were performed for each circuit element with a continuous wave optical input of -13.7dBm in-fibre. Relative uniform optical performance throughout the circuit was achieved as shown in Figure 3.11. This figure shows the photocurrent generated at each electrical connection with the remaining connections left open circuit. Both forward and reverse directions through the circuit are overlaid with separate axes to show responses to all eight optical inputs and outputs.

The data indicate a relatively uniform optical performance throughout the circuit. Predicted photocurrent values are also shown for the circuit with a solid line assuming the designed de/multiplexing gain[5] (for the large electrodes with pad numbers 00, 07 and 13 in Figure 3.9) and 4dB combiner losses.

A mean photocurrent reduction of 9dB is observed from the input electrode pin to the output electrode pin. The mean fibre coupling loss between fibre and the chip is estimated from photocurrent measurements to be 8dB per facet, including an estimated 1.5dB loss through the cleaved facet. A predicted fibre to fibre loss of 31dB (8dB/facet + 9dB photocurrent reduction + 6dB demultiplexing photocurrent gain) for the unbiased circuit. This may be compared with direct power measurements at the input and output fibres where best case fibre coupled measurements give a 36dB off-state loss. Typical off-state loss values of around 40dB were measured.

DC currents are applied to combinations of five electrodes to form the switch paths. The input, output and shuffle pins are each operated at 200mA. The crossbar electrodes are selected according to the required state and are biased at 100mA. When one crossbar element is switched from "on" to "off' state, a switching extinction ratio of over 15dB is typically observed. The chip gain in the was lower than expected as no lossless operation was achieved.

3.2.3.3 Gain analysis of QD SOAs

To study the reasons behind this low gain in the switching devices, an experimental gain analysis of QDSOAs devices was performed.

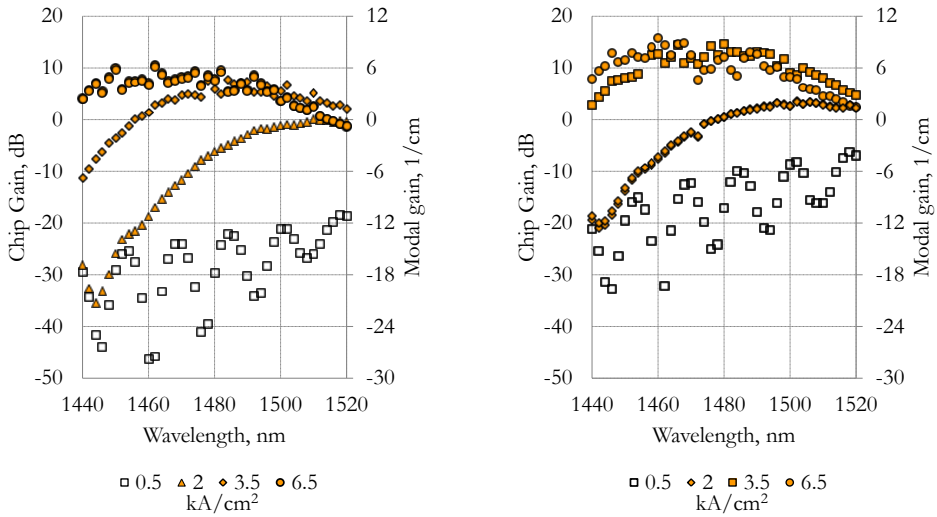
A possible way to improve the possible achievable gain in QD devices is to increase the density of QDs in the device by increasing the number of stacked QD layers [107]. For this reason, two QD-SOAs were assessed, one with 5 layers (QD5)[6] and the other one with 9 QD-layers (QD9)[7], both of them within

[5] Large electrodes cover more than one waveguide. If there is light in more than one of them the photocurrent generated comes from both. i.e. photocurrent multiplexing

[6] MO891 (Internal reference)

the same design of Q1.25 confinement layer. The SOAs have dimensions, for both cases, of 4mm in length and 2μm in width. The fabrication followed a 3-step reactive ion etching (RIE) process for waveguide definition.

For the gain assessment, a tuneable laser with a calibrated in-fiber input power at each tested wavelength of -10dBm is used. The polarisation state is optimised, at the input facet of the 10°C temperature controlled integrated device, for maximum gain. The current injection to the device is varied between 0 and 6.5kA/cm^2 for both operation conditions, continuous bias (DC) and pulsed current operation. For the pulsed current operation, a 5% duty cycle signal with 10μs period was used to bias the device. The bias current levels were selected by optimizing the peak level of the pulse in order to achieve the same gain levels as in the relatively low DC current density regime of 2kA/cm^2. This was done to avoid any misleading calibration due to impairments coming form the device heating. The gain calculations were done taking into account the fiber to chip coupling losses of 9dB/facet, obtained from photocurrent measurements.



DC operation

Pulsed operation 10μs and 5% Duty cycle

Figure 3.12: Gain Spectra for a QDSOA with 5 layers.

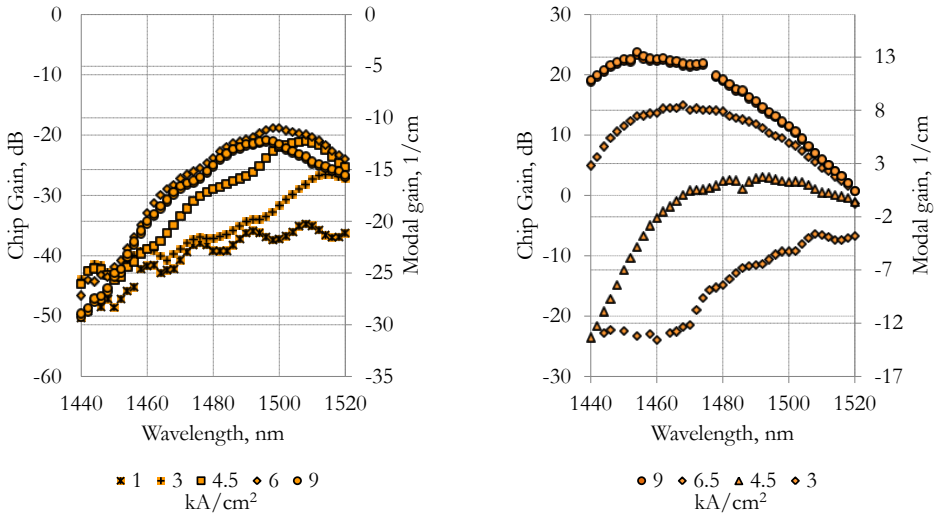
The gain characteristics for the 5-layer QDSOA is shown in Figure 3.12. In the left hand side plot, the chip (facet-facet) and modal gain obtained under DC

[7] MO892 (Internal reference)

operation are shown. It can be seen that, as expected, the gain increases with the current injection. Reaching a saturation point around 6.5kA/cm^2. The maximum chip gain and modal gain at 1460nm was 10dB and 6cm^{-1} respectively. Material gain saturation in quantum dot devices has been shown at a low gain in the literature [108] . This apparent saturation of the QD gain is temperature dependent and can be improved if the QD device works at lower temperature conditions . It is thought that at low temperature conditions, the rate at which carriers escape from the dots to the wetting layer is significantly reduced, and this effectively decouples the dots from both the wetting layer and each other. Concentrating the carriers in the dots and not in the wetting layer which does not provide gain.

In the right hand side of Figure 3.12, the chip and modal gain obtained under pulsed operation are plotted. It can be seen that, at the same wavelength and current density (6.5kA/cm^2) as in DC case; i.e. 1460nm, a maximum chip gain and modal gain of 15dB and 9cm^{-1} is observed, respectively. The modal gain obtained in this operation regime is 3dB higher with respect to the DC operation regime. This was the first indication that the QDSOAs were getting hot as a higher gain is achieved under pulsed operation.

For both operation current regimes, periodical features are observed at low current levels with a periodicity of ~15nm. The cause of these features was not further investigated because it was out of the scope of this thesis. However, the ~15nm periodicity could indicate that a cavity of ~23μm was created somewhere in the measurement setup or along the QDSOA due to imperfect facets or a damaged waveguide. On the other hand one could speculate that the periodical features are a manifestation of the contribution to the gain from ensemble of quantum dots with similar sizes i.e. homogeneous gain broadening [109]. The full-width half maximum (FWHM) of each of these features is ~5meV or ~10nm and ~9meV or ~16nm for the QD5 and QD9, respectively. These values compare well with the 10meV obtained at room temperature in [110]. This fact doesn't make valid this speculation as more rigorous studies have to be done in order to get into a conclusion. In the literature a similar behaviour has been theoretically observed on multi-quantum well media for various current densities and it is called optical absorption resonance [111]



CW case Pulsed operation 10μs and 5% Duty cycle

Figure 3.13: Gain Spectra for a QDSOA with 9 layers.

The gain characteristics for the 9-layer QDSOA are shown in Figure 3.13. The gain measurement under DC operation (left hand side plot) was disappointing. It was expected a higher gain but instead negative gain values were obtained. The gain evolution increases with the bias current, reaching saturation around 6kA/cm^2. A higher bias density of 9kA/cm^2 showed that the QDSOA gain was already saturated. The maximum chip gain and modal gain were -19dB and -13cm^{-1}, at 1500nm.

The gain evolution under pulsed mode is completely different from that of the DC case as shown in the right hand side plot in Figure 3.13. Maximum chip and modal gain of 23dB and 13cm^{-1}, respectively was observed for a wavelength of 1460nm and 9kA/cm^2 current density. The gain difference between the pulsed and CW operation in the QD9 confirms that considerably heating is compromising the achievable gain in our QD devices.

To continue with the quantum dot gain characterisation. Optical gain saturation properties have also been studied. The 10°C temperature controlled QDSOA chosen for this test was the one with 5 layers. This is because its behaviour is much better under DC current biasing. The device operation current was 400mA. A high power Raman laser operating at 1445nm was used as the input optical signal. The polarization is optimized with a polarization controller to achieve the highest gain.

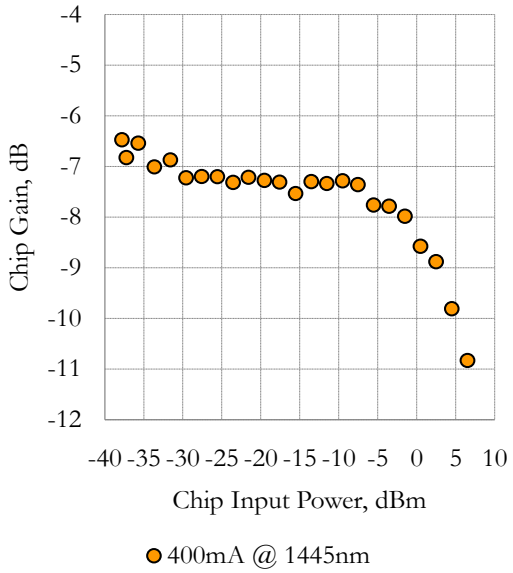


Figure 3.14: Gain saturation. Input Power vs Gain

The dependence of the gain on device input power is proven to be negligible up to -5dBm with a input saturation power of +5dBm as shown in Figure 3.14. It is important to mention that the 400mA or 5kA/cm^2 DC bias current or current density, used for the gain saturation characterisation, is almost two times higher that the operation current used for the switching devices. For this reason I don't expect any significant signal impairments coming from saturation effects in the SOA gates as the gain keeps almost constant over a wide input power dynamic range of more than 40dB in these quantum dots.

In the next section an experimental demonstration of data routing and crosstalk assessment for the 4x4 multistage QDSOA switch is presented.

3.2.3.4 Data Routing

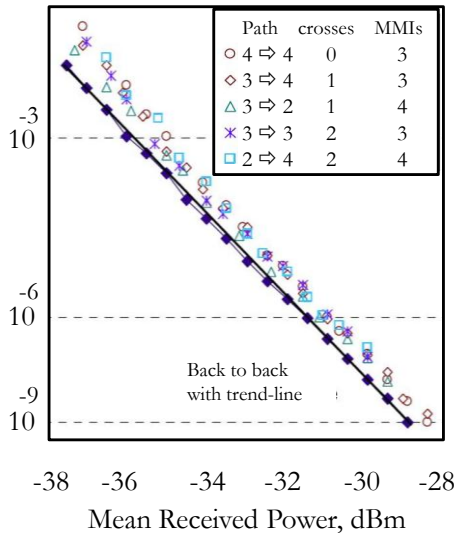


Figure 3.15: Bit error rate measurements for representative paths.

To assess the integrity of routed data, bit error rate measurements were performed at a data rate of 10Gbit/s with a pattern length of 2^{31}-1. The same experimental arrangement shown is Figure 3.6 is implemented for the data routing characterisation of the 4x4 QDSOA switch. Fibre-coupled input powers, to the switch matrix, of +10dBm are used at a wavelength of 1550nm.

The device operating conditions are the same as for the static performance assessment, 100mA per SOA gate and 200mA for the shuffle network. Because the switch matrix is polarisation sensitive the injected state is optimised for minimum path loss. The output signal from the QD switch matrix is passed through a 0.7nm optical band-pass filter. This signal is pre-amplified by an Erbium fibre amplifier and input to a 10Gbit/s receiver and error detector.

Power penalty performance is assessed from the bit error rate curves shown in Figure 3.15 for representative paths. The number of waveguide crossings and multimode interference (MMI) couplers and splitters are path dependent as reflected in the inset caption. Measured data show no indication of an error floor or distortion within the switch matrix itself. Power penalty varies only slightly with values between 0.4 to 0.6dB for the range of paths indicating a weak power penalty dependence on selected path.

3.2.3.5 Crosstalk Analysis

Larger scale mesh interconnection of multiple SOA-based circuit elements places a particular constraint on the crosstalk performance [104], [105]. In this subsection, an experimental study on the incoherent crosstalk robustness of the 4x4 switching network is presented.

For this purpose, time de-correlated data is used for the two input channels on closely spaced wavelengths of 1549.3nm and 1549.6nm. Both wavelength channels pass efficiently through the same receiver filter and therefore represent the in-band interference which may be present in such multipoint-to-multipoint circuits. The role of the interferer channel is explored by deliberately co-biasing the appropriate second path, resulting in two contending channels at the measured output. The intended path gate electrode is biased at 100mA while the interferer channel path current is varied between 0mA and 100mA. The crosstalk is measured directly at the switch output as the ratio of peak powers. A minimum crosstalk value of 22dB is achieved.

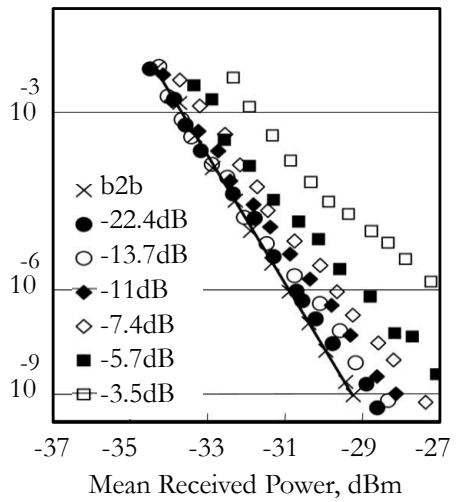


Figure 3.16:Bit error rate performance in an incoherent crosstalk study.

The crosstalk dependent power penalty is assessed through bit error rate measurements shown in Figure 3.16. The inset indicated the amount of incoherent crosstalk as the unwanted path biasing increases. Figure 3.17 depict the power penalty evolution as the Incoherent crosstalk increases. A picture of the assessed device is presented to indicate the inputs and output assessed.

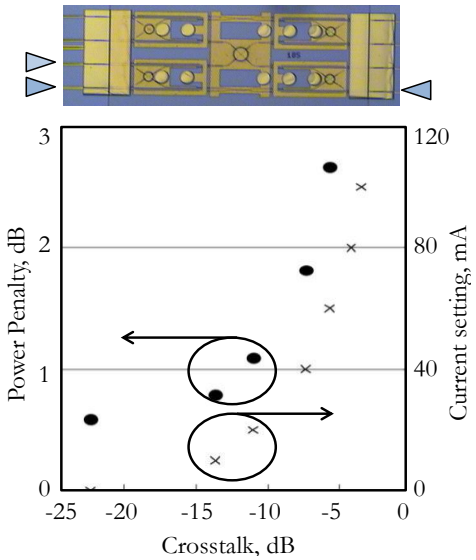


Figure 3.17: Incoherent Crostalk penalty.

A 0.6dB crosstalk power penalty when the unwanted path current is set to zero is indicated in Figure 3.17. Increasing the unwanted signal to -10dB incurs over 1dB penalty. The modest gate length of only 0.8 mm allows for even further reductions in crosstalk if larger crossbar gate elements are used in next generation switches.

3.3 Discussion

As the number of integrated stages increases, a very modest degradation in penalty occurs, varying from 0.2±0.05dB to 0.5±0.1dB for the single stage and the multistage, respectively. This is attributable to the modest level of amplified spontaneous emission and the high optical saturation threshold (low distortion) (~5dBm in-chip) which was observed during the static characterisation of the devices.

Although the assessed devices achieved an excellent performance, it is important to mention some key aspects in which there is room to improve. The extinction ratio of 22dB per switching gate in the 4x4 multistage device proved to be sufficient to obtain negligible same-wavelength path-dependent crosstalk. This extinction ratio is highly dependant in the polarization state of light due to the high polarization sensitivity of the used QD gain material [107]. An extinction ratio as high of 35dB was achieved for a single SOA 4mm long in which no bends or multi-contact elements were present to change the state of

polarization inside the chip.

As mentioned, the devices displayed properties previously reported for the quantum dot gain medium such as high optical saturation threshold. But they where not able to compensate completely their losses in order to achieve net fibre-to-fibre gain. A way to improve the possible achievable gain is to increase the density of QDs in the device by increasing the number of QD layers. With this in mind a gain study for two QD-SOAs was assessed, one with 5 (QD5) and the other one with 9 QD-layers (QD9), both of them with a Q1.25 confinement layer. The experimental study proved that the low gain in the circuits is, in part, due to a wavelength operation misalignment and a thermal rollover caused by a non-proper heat dissipation by the patterned ceramic tiles where the devices are fixed. Thus, the low gain operation value may be attributable to several causes which may be improved by using the right epitaxy (right wavelength), number of QD layers and proper heat dissipation techniques.

The low gain, due to heating, in the QD devices imposed a limitation in the sophistication of the experiments. For this reason I chose to move to a high gain MQW system in order to continue with the scaling to higher connectivity switches.

In this work, the author acknowledges the contribution of Dr. Kevin Williams, Dr S. Anantathanasarn, Mr T. de Vries and Mr E. Smalbrugge. Dr. Anantathanasarn from the physics (PSN) group in TU/e university developed and grew the QDs emitting at 1550nm. Dr Kevin Williams from the electro-optical communications (ECO) group was involved in the development and implementation of the switches. Mr. T. de Vries and Mr E. Smalbrugge from the Optoelectronic Devices (OED) group provided technical support. Their contributions and stimulating discussion are very much appreciated.

3.4 Summary

A highly promising approach to enabling dynamic routing in highly scalable optoelectronic circuits has been presented. Very low power penalties of order 0.2dB/stage has been observed in monolithic quantum dot circuits showing considerable promise for more complex monolithic interconnection networks. The impact of monolithic cascaded quantum dot semiconductor optical amplifier switch elements has been studied for the first time. The proposed architectures lead to a marked reduction in electrical connections and control complexity compared to previously published SOA based switch arrays. The scaling of such circuits to higher numbers of connections is predicated on the

levels of signal degradation at each stage, and the possibility to provide the required interconnection between stages with low crosstalk and good power efficiency. Even though excellent results were obtained with the QDSOA based switches, still their full potential was not achieved due to the heating problems and their extremely high polarisation sensitivity. If these issues are improved the QD-based devices are extremely appealing because of their low noise figure (NF) which impacts directly the energy consumption of large scale high capacity switches as it will be discuss in following chapters.

In the next chapter the proposed solutions to improve the transmission properties in multistage circuits are implemented. First I turned to a high gain Multi-Quantum Well (MQW) system. Second, through the use of active passive integration any light polarisation issues and bandwidth limitations are minimised. With this changes I designed a MQW SOA-based active-passive monolithic integrated multistage switch which operates at ultrahigh speed line rates per optical path.

Chapter

4 Ultrahigh Capacity Monolithic Multistage Switch

This chapter is based on the publications [112-117] made about this topic during this Ph.D project. In this chapter the highest line-rate serial transmission (320Gbit/s) is reported for a multistage photonic integrated switching network. This represents a step change in the operating speeds for multi-stage integrated photonics in general, and optoelectronic switching networks in particular.

4.1 Introduction

Optoelectronic switching circuits are able to route massively broadband optical signals with bandwidth independent energy consumption and nanosecond time-scale re-configurability [56], [67]. Such circuits may play an increasingly important role in service provisioning in optical data networks and high speed optoelectronic signal processing. Many of the envisaged applications for these circuits require massive bandwidth and high levels of circuit connectivity. Increasingly high line rates have been demonstrated using wavelength multiplexing in networks of discrete photonics switches [26], [118], [119]. While dense wavelength division multiplexing readily exploits the multi-Terahertz bandwidths of photonics, it can also lead to stringent management overheads and increased transceiver complexity. Robust wavelength registration throughout the optical network becomes mandatory and thus unattractive in cost- and energy-sensitive short reach data networking. Serially multiplexed, wavelength-insensitive data formats, as Optical Time Division Multiplexing, on non-critical wavelength grids may offer reduced inventory and management simplification.

Photonic integrated circuits offer a route-map to larger connectivity and sub-systems miniaturisation. A broad range of semiconductor optical amplifier switching circuits have been proposed [17], [67], [120-125] and increasingly sophisticated circuits are being demonstrated. Eight input, eight output

switching sub-systems have been configured from combinations of integrated 1 x 8 switches [60]. Sixteen input and sixteen output (16 x 16) switching fabrics have been implemented in a three stage Clos-Tree hybrid network [90] to allow 10Gbps data routing through monolithic circuits. Higher line rate studies have been performed by exploiting non-linear processes to realize all-optical logic, sophisticated de-multiplexing functions and wavelength conversion [126-128]. Nonlinear operation typically requires auxiliary optoelectronic circuitry which is less well-suited to larger scale integration.

There has been little research into the scalability of monolithic multistage switching circuits operating at very high line rate. In this chapter, I study the performance of a monolithically integrated multistage interconnection circuit operating at serial line-rates of 160 and 320Gbps.

The circuit is realised using up to four cascades of crossbar semiconductor optical amplifier switches. The chosen architecture continues with the idea of reaching higher port count circuits by using multistage circuits with smaller building block as discussed in the previous chapter. The study of data integrity routed through four crossbar-stages gives us a perspective of the feasibility of larger switch matrices such a 16x16 switching matrix. In this chapter, Section II introduces the switch fabric architecture, describing the crossbar switch element used in the circuit. The fabrication approach is outlined in Section III. The physical layer characterisation for the designed and realised circuit is presented in Section IV. High speed data routing and fast reconfigurable circuit operation is described in Section V. A discussion on the findings of this work is presented in Section VI. A summary is presented in Section VII .

4.2 Architecture

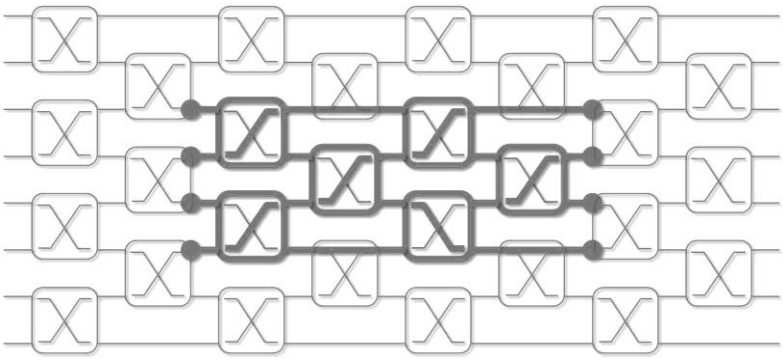


Figure 4.1: N-stage architecture considered in this chapter.

The four-input, four-output multistage optoelectronic switching circuit is implemented using six interconnected two input two output (2 x 2) crossbar elements. This is representative of a broad class of multistage interconnection network architectures based on the concatenation of crossbar elements. Examples of such networks include Spinet, omega, Banyan, butterfly and baseline [58], [129-134]. In this work I integrate the example of the N-stage planar architecture from Spanke and Benes [129], as shown in Figure 4.1, and study physical layer performance for the cascaded SOA crossbar switch elements. In Figure 4.1 The dark grey four input, four output (4 x 4) layout is superimposed on the larger light grey network to show architecture scalability.

4.2.1 Monolithic multistage photonic switching circuit

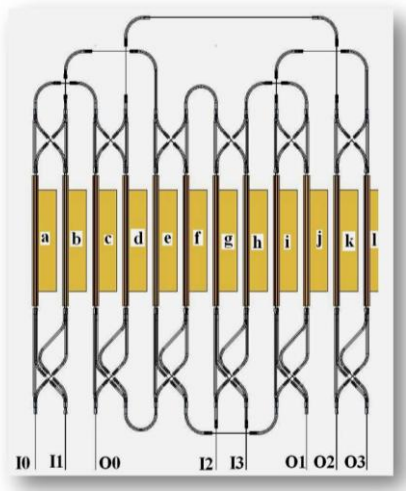


Figure 4.2: Schematic waveguide layout of implemented 4x4 circuit

The implemented paths within the photonic circuit have varying numbers of stages, allowing insight into the role of the number of successive switch elements on signal degradation. The dark grey four input, four output (4 x 4) layout is superimposed on the larger light grey network to highlight the intrinsic scalability of the architecture. For a photonic implementation, the boxes represent optoelectronic crossbar switch elements and the connecting lines in between represent waveguides. Routing of signals through the circuit is defined by the electronic states at each crossbar switch. There are sufficient numbers of crossbar stages in the architecture to enable rearrangeably non-blocking operation. Figure **4.1** shows a minimised number of crossings, and while this is desirable, it is not a fundamental constraint. In the implementation described within this paper, crossings have been required.

The circuit is realized in a multi-project wafer with pre-positioned active switching elements in one row and therefore some additional waveguide bends and crossings have been inserted. The functional circuit layout in Figure 4.1 is folded to give the layout used for the photonic integrated circuit in Figure 4.2. During this manipulation, two connections were inadvertently exchanged. As highlighted in Section 4.2.3, twenty valid paths are nonetheless established through the circuit, including the longest and shortest paths. Four inputs and four outputs are defined on the front facing side at the bottom of Figure 4.2. Using just one facet for the fiber access is expected to simplify fiber array-pig-tailing. The inputs are labelled *I0* through to *I3* and the outputs are labelled *O0* through to *O3*. The inputs and outputs connect directly to the row of crossbar elements. Each crossbar switch element includes two electrodes for the cross and bar states respectively and these are labelled *a* through to *l*. The cross-bar switch elements are interconnected by means of deep etch curved waveguides with minimum bend radii of 0.1 mm. Waveguide crossings are implemented orthogonally in shallow etched straight waveguides for minimum crosstalk and loss.

4.2.2 Crossbar switch element

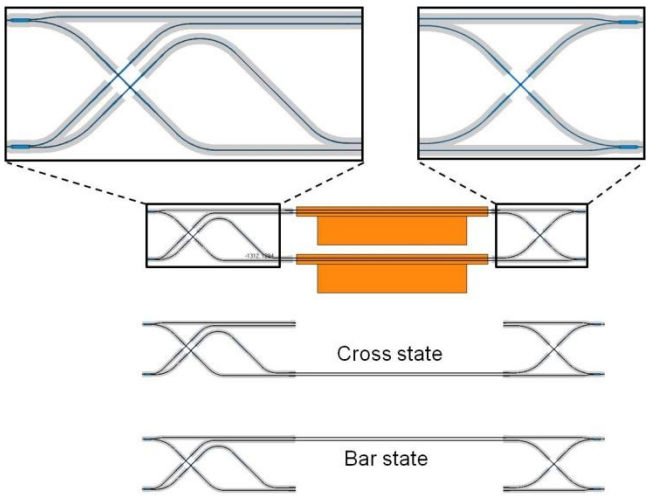


Figure 4.3: Crossbar Switch functionality

The crossbar switch elements are designed with an innovative waveguide and electrode design for miniaturisation and control plane simplifications. The design, first outlined for quantum dot waveguide switches [98] in chapter 3, is now implemented for an active-passive re-grown epitaxy. The active-passive regrown epitaxy is used to further reduce noise and distortion in the circuit.

Only two active islands are required in this new active-passive arrangement as two SOA gates are implemented in each active island. The mode of operation is shown in Figure 4.3 using annotated drawings of the waveguide and electrode mask layers. The optical waveguide arrangement uses a broadcast and select switch. In Figure 4.3, blue lines denote waveguides. When surrounded by a greyed area, the waveguides are deep etched to allow tight bend radii. The orange areas denote the p-electrodes for the active elements. Each input on the left of Figure 4.3 (top) is split into two replica signals. One signal is routed to a lower cross-state gate electrode, while the second replica is routed to the upper bar-state gate electrode. The waveguides are twisted such that the two cross state gates and the two bar state gates are collocated. This enables the use of a common electrode and only two active islands to allow size reductions. The coupled electrode arrangement facilitates the crossbar electronic interface. At any given time, either the cross state is high, or the bar state is high for the tested crossbar switch elements. Only one bit of electrical information is therefore required for the electronic driver for each crossbar, simplifying control logic. The bar and cross states for the switch are shown explicitly in Figure 4.3 (bottom) by removing the off-state waveguides

4.2.3 Optical Paths

The optical paths comprise a high number of passive elements as well as the active semiconductor optical amplifier gates within the crossbar elements themselves. Mode filters are implemented using 1 x 1 multimode interference (MMI) waveguides at the inputs and outputs to promote single mode propagation through the circuit. The splitting operation is performed using symmetric 1 x 2 multimode interference couplers and combiners. Waveguide crossings are shown in detail in the top of left and right insets for Figure 4.3. These are implemented within shallow etched waveguides to allow low-divergence optical guided modes at the intersections to reduce path dependent crosstalk. The waveguides intersect orthogonally for this same purpose. Mode transformers comprising adiabatic tapers are implemented at each transition from a deep to a shallow waveguide.

The numbers of these elements appearing in each path is quantified in Table 4.1. The first column defines the viable optical paths, and the second column highlights the on-state electrode combinations which facilitate these paths. Component numbers are then listed for each path. Between two and four SOAs are used in each path. The multistage network enables more than one path through the circuit for certain combinations of inputs and outputs. This reduces blocking probabilities when routing arbitrary combinations of inputs to

outputs. A subset of inputs can be connected to the same outputs using more than one path. Table 4.1 highlights all the possibilities, separating multiple paths by commas.

Table 4.1: COMPONENTS IN VIABLE OPTICAL PATHS

Optical path	On state electrodes	MMIs	Mode transformer	SOAs
I0 → O0	*ac*	6	6	2
I1 → O0	*bc*	6	10	2
I2 → O1	*hi*	6	12	2
I3 → O1	*gi*	6	14	2
I0 → O2	*bcek, bfil*	10	24, 26	4
I1 → O2	*acek, afil*	10	26, 28	4
I2 → O2	*cfgk, egil*	10	20, 18	4
I3 → O2	*cfhk, ehil*	10	24, 22	4
I0 → O3	*bcel, bfik*	10	28, 28	4
I1 → O3	*acel, afik*	10	30, 30	4
I2 → O3	*cfgl, egik*	10	24, 22	4
I3 → O3	*cfhl, ehik*	10	28, 26	4

4.3 Fabrication

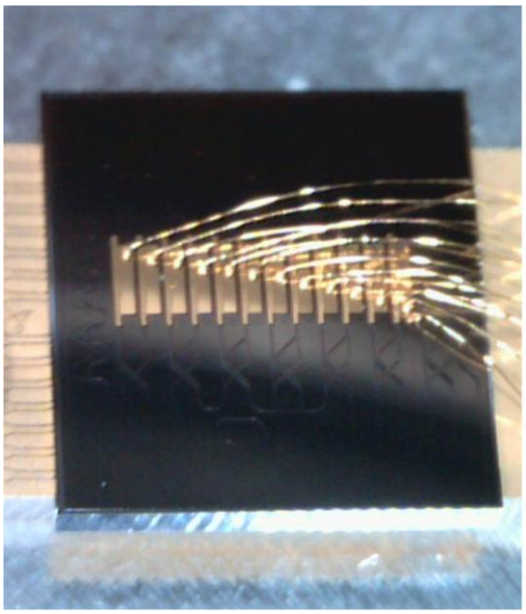


Figure 4.4: Monolithic optoelectronic multistage interconnection network

The circuit is fabricated on a multi-project wafer [135]. The InGaAsP/InP layers used for the semiconductor optical amplifiers are implemented for a 1550nm circuit gain peak. The active epitaxy includes four quantum wells (QW) within a separate confinement heterostructure. A photo-lithographically defined etch creates amplifier islands periodically across the wafer with a 0.25mm pitch. Low loss passive heterostructures are re-grown across the remaining area. The circuits are processed with a two step reactive ion etch to define both shallow low-loss waveguides and deeply etched waveguides for selected optical components and functions. Planarization, gold evaporation and gold plating complete the processing. Circuits are subsequently cleaved to die. No facet coating has been applied to the circuit prior to this study and therefore the facet reflectivity is expected to be 34%. The circuit area is 15mm^2. Figure 4.4 shows a microscope photograph of the completed circuit in the same orientation as used in Figure 4.2. The cleaved facet, including all the input and output waveguides is visible at the lower edge of the circuit. The features visible at the front facet are a reflection of the underlying surface. Some of the passive waveguides are discernable in the region between the metal electrodes and the front facet. The waveguide arrangements are explicitly shown in Figure 4.2 and Figure 4.3. The active SOA waveguide elements are positioned underneath the

twelve electrodes in the centre of the circuit. The circuit is bonded to an Aluminium Nitride carrier with a patterned gold surface for ease of wire bonding and subsequent electronic connection.

4.4 Device characterisation

Detailed measurements are performed at both the component level and circuit level to verify the mode of operation, connectivity and performance. Initially, component level assessment is performed using test structures fabricated simultaneously on the same wafer. The author acknowledges Dr. Martijn J. R. Heck for the test structures characterisation when he was within the opto-electronic devices group of this University.

Input to output circuit level assessment is performed. A cross-comparison between performance anticipated from test structure operation and measured circuit level performance is subsequently presented.

4.4.1 Component characterisation

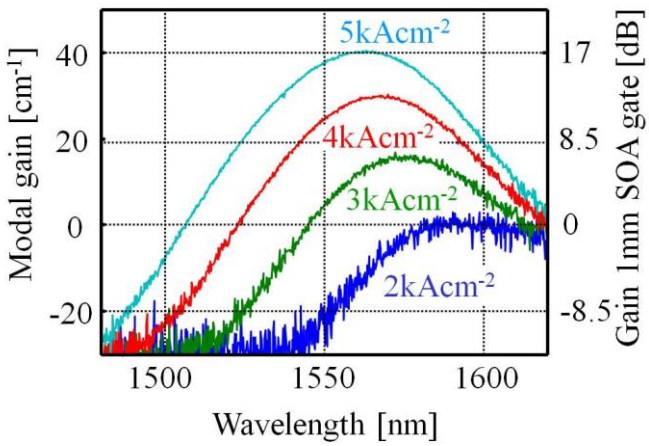


Figure 4.5: Optical gain spectra from test structures. The current density ranges from 2 kAcm^{-2} to 5 kAcm^{-2}, corresponding to a total current range of 44mA to 110mA.

The mask set used in fabrication includes a number of custom test structures to enable process performance monitoring and explicit component level evaluation. Fabry–Perot cavity measurements were performed for deep etched 1.5μm wide waveguides and shallow etched 2μm wide passive waveguides to estimate waveguide losses. Propagation losses for the mode transformers between shallow and deep waveguides were also characterised. Waveguides

with two up to sixteen deep to shallow waveguide mode transformers were fabricated and measured. A linear fitting gives a loss of 0.16dB per mode transformer. Gain spectra are measured using a technique based on the variable stripe length method [136]. High loss spiral waveguides at the rear and 7 off-normal waveguides at the measured front facet minimise the reflections. Comparing two amplifiers with different lengths subsequently allows the estimation of modal gain per unit length of amplifier [136]. This data is in turn used to give the estimated gain for the 1000μm long SOA gates used within the presented circuit Figure 4.5. Values are given in the right y-axis. The gain spectra indicate a 3dB spectral bandwidth of 38.6nm at 5kAcm^{-2}.

Table 4.2: TEST STRUCTURES CHARACTERISTICS AT 1550nm

Optical element		Gain	Units
1 × 1 multimode interference mode filter		- 0.5	dB
1 × 2 multimode interference splitter		- 3.5	dB
Mode transformer		- 0.2	dB
Shallow waveguide		- 5.5	dB/cm
Deep etched waveguide		- 8.0	dB/cm
Semiconductor optical amplifier gain for total crossbar currents[1]	44mA	- 17.0	dB
	66mA	+ 3.7	dB
	88mA	+ 11.8	dB
	110mA	+ 16.7	dB

Data from all the test structure assessments are summarized in Table 4.2.These data are later used for the prediction of circuit level characteristics in Table 4.3.

4.4.2 Circuit characterisation

Electrical measurements are performed for each of the twelve electrodes. One short circuit between electrode *d* and the *n*-type substrate is observed. A second short circuit between electrodes *b* and *c* results from an imperfect gold lift-off. The interconnection of these two electrodes limits the effective operating current and therefore available gain for paths requiring *b* or *c* to be in the on-state. Low leakage diode characteristics are measured for the remaining

electrodes, with turn-on[8] voltages of 0.49–0.53V at 1mA, and series resistances within the range 4–6Ω.

Table 4.3: STEADY-STATE CITCUIT PERFORMANCE AT 1550nm

Optical path	Passive losses[1,2]	Circuit gain[2]	Mean gain per stage[3]	Units
I0 → O0	- 20.8	- 4.2	+ 8.3	dB
I1 → O0	- 21.3	- 10.7	+ 5.3	dB
I2→ O1	- 21.6	- 1.5	+ 10.1	dB
I3 → O1	- 21.9	- 2.5	+ 9.7	dB
I0 → O2	- 42.6	- 3.9	+ 9.7	dB
I1 → O2	- 42.9	- 17.0	+ 6.5	dB
I2 → O2	- 41.7	- 18.0	+ 5.9	dB
I3 → O2	- 42.2	- 20.4	+ 5.5	dB
I0 → O3	- 43.4	- 5.3	+ 9.5	dB
I1 → O3	- 43.4	- 17.0	+ 6.6	dB
I2 → O3	- 42.2	- 16.4	+ 6.5	dB
I3→ O3	- 42.8	- 17.0	+ 6.4	dB

[1] Passive losses estimated from test structure data
[2] Fiber chip coupling losses not included
[3] Passive losses subtracted from circuit gain, scaled for amplifier stages

To understand the operating characteristics for the full circuit, estimates are made for the total passive losses due to non-amplifying components in each path. These are given in Table 4.3.

Measured on-chip circuit gain is recorded experimentally for biased amplifiers within the integrated switch circuit. Performance is quoted for operating currents of 115mA per crossbar, with the exception of the low loss paths to output *O1*. In this case electrodes *g* and *h* are biased at the lower value of 80mA to avoid signal impairments resulting from noise accumulation and oscillations. Laser oscillation between the input and output facets is observed for currents of 122mA at electrode *i* and 95mA at either electrode *g* or *h* for these low loss paths. This is because residual facet reflexions. Comparing the full range of paths, it is evident that there is variation in the path gain. Estimates

[8] A diode needs to be biased with the right voltage in order to conduct or non conduct current i.e. to turn diode on or turn diode off.

are made for the performance of the individual SOA gates. The difference between the passive losses and the circuit gain is divided by the number of amplifiers (Table 4.1) in each path to give an estimate of operating gain for the amplifiers in each stage. Values in Table 4.3 are observed to vary between 5.3 dB and 10.1 dB, lower than might otherwise have been expected from the test data in Table 4.2. This is considered further in next chapter. Nonetheless the mean gain per stage values do indicate a good degree of uniformity for the components used in the paths.

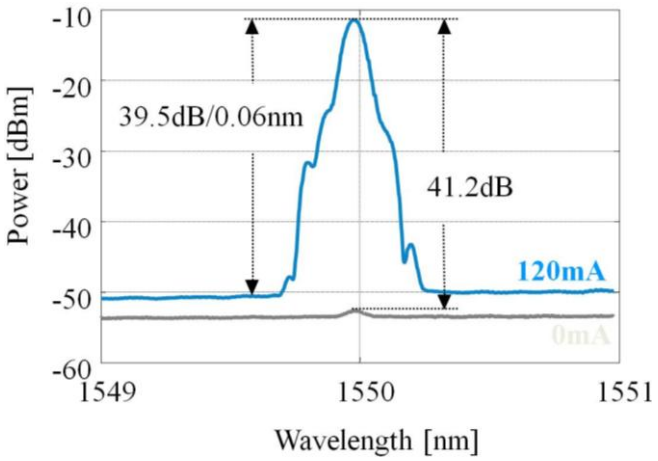


Figure 4.6: Optical signal to noise ratio for path I3 to I1. Crosstalk suppression at OFF-state.

Optical signal to noise ratio has been studied for the range of connections, and values correlate closely with optical losses. The worst case value of 23.0dB/0.06nm is measured for *I1* → *O2* where the circuit gain is somewhat lower than anticipated. The best case measurements are shown in Figure 4.6 for path *I3* → *O1*, showing an optical signal to noise ratio of 39.5dB/0.06nm. Optical signal to noise ratios exceeding 37dB/0.06 nm are measured for five of the paths, including a number of the four stage paths. Spectral features originate from the tuneable laser used in the measurement. Extinction ratio performance is additionally shown in Figure 4.6 where the performance is compared for an on-state for path operating current of 120mA per crossbar and the off-state operating current of 0mA. These settings gave an extinction ratio of 41.2dB. Such a high value is promising for simultaneous operation with all paths routing data.

4.5 Ultrahigh line-rate data routing

Data routing performance is evaluated with several serial-line-rate optical inputs (40, 160 and 320Gbit/s). The experimental arrangement is firstly presented. Some details specific to OTDD/OTDM testbed development are included in Appendix A. The path dependent operation is then discussed, where the role of the number of crossbar stages on signal degradation is identified. Then the dynamically reconfigured electronic control is quantified for 160Gbit/s prior to the measurement of its optical dynamic range.

4.5.1 Experimental Arrangement

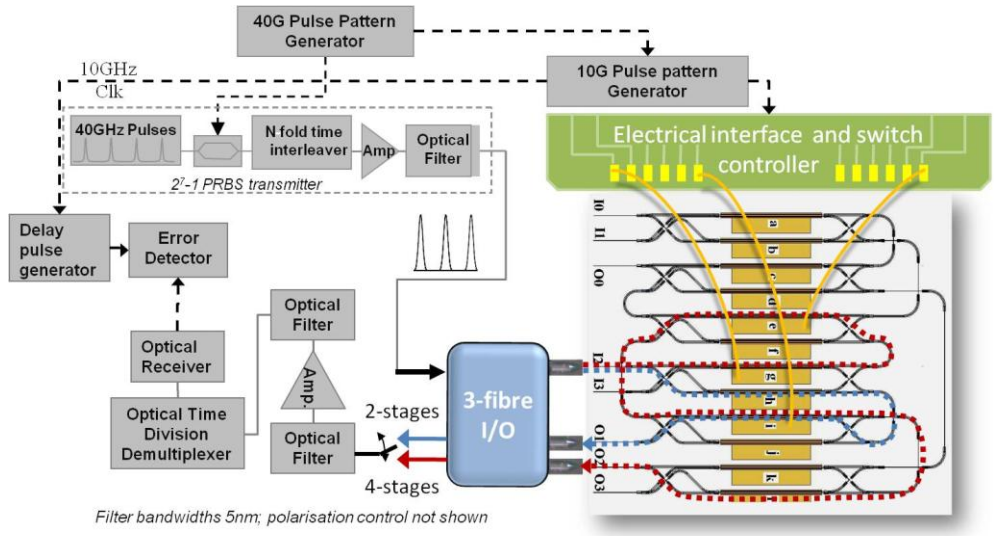


Figure 4.7: Experimental arrangement.

The chip-sub-mount assembly is fixed by vacuum clamp to a temperature stabilized positioning system. The circuit is operated at a fixed temperature of 22°C. Up to three lens ended fibers on individual manipulator stages are used at the same facet. Fiber to chip coupling loss is estimated to be ~6.5dB from photocurrent measurements. Loss values are estimated by accounting for predicted on-chip losses between the facet and SOAs using data in Table 4.2. Operating currents have been varied up to 120mA per switch gate pair, at which point facet reflections lead to oscillations on a number of low loss paths. There is no evidence of reflections within the circuit.

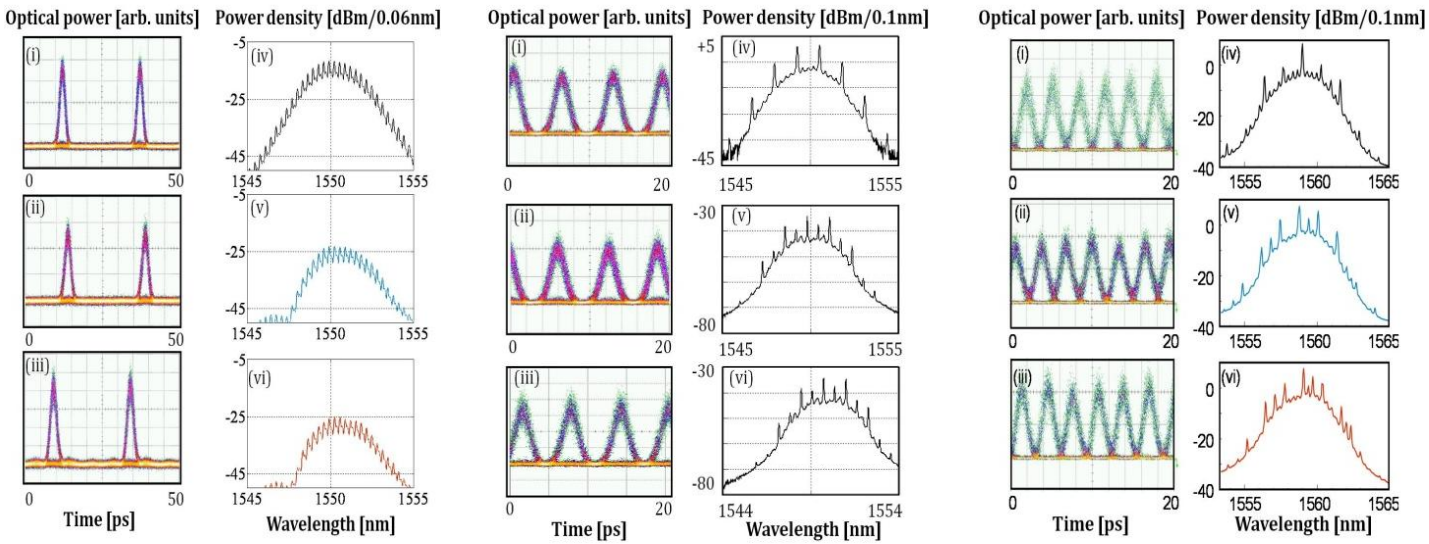
The OTDM data source and receiver is presented in Figure 4.7. A mode-locked fiber laser is used as a 40 GHz optical impulse source. On-off keyed

40Gbps data is generated with a Mach–Zehnder modulator. A pulse interleaver replicates copies of the optical data to generate the time division multiplexed 160 and 320Gbps serial data with a pseudo-random 2^7-1 bit sequence [113]. The optical time division multiplexed data is amplified and filtered with a 5nm bandwidth filter. The polarization state is aligned for maximum gain and extinction ratio through the circuit. The return path to the error test equipment includes a filtered Erbium pre-amplifier and an optical demultiplexer. Fiber dispersion in the experimental assessment is not explicitly studied. It is however minimised through the use of dispersion compensating fiber in both back to back and circuit level bit error rate measurements. The high-speed data experimental setup and the switch experimental setup are in different laboratories separated by two 50m lengths of standard dispersion single mode fiber and 8m of dispersion compensated fiber. It is important to mention that the author was involved in the development of the demultiplexers at 160 and 320Gbps, in a collaborative work with the group of high speed optical signal processing within the electro-optical communications group [116]

4.5.2 Path dependant routing for 40, 160 and 320Gbps OTDM Signals

Paths with two and four crossbar stages are compared for steady-state electronic bias conditions. Fibers are aligned for input *I0* and outputs *O0* and *O2* for the 40 and 160Gbit/s transmission and for the 320Gbit/s transmission the fibers aligned are for input *I2* and outputs *01* and *03* . The change in optical paths for the 320Gbit/s experiment was due to a reduce complexity assessing the electrode pins used to fix the paths.

Figure 4.8 shows the input and output time traces from the circuit as captured on an Agilent 86119A ultra-wideband optical sampling unit in combination with a high speed sampling oscilloscope. Clear eye opening is observed at the input and for both outputs for each data rate.



40Gbit/s 160Gbit/s 320Gbit/s

Figure 4.8:input and output eye diagrams from the circuit (i)-(iii) and the optical spectra (iv)-(vi). The line rate are 40, 160 and 320Gbit/s for two,(ii) and (v), and four, (iii) and (vi), crossbar switch stages.

The optical spectra for the switch input and outputs are also recorded as shown in Figure 4.8(iv–vi). Spectral features in the 40Gbit/s experiment come from a misaligned filtering at the output of the pre-amplifier connected to the receiver. The spectral features for 160 and 320Gbit/s show small fluctuations in the half-frequency harmonic power which has been previously observed and attributed to temperature-induced phase instability in the optical interleaver [137]. The similarity between the optical spectra indicates minimal levels of nonlinear interaction, for both two and four stages of monolithically concatenated stages of optical amplifier switch stages. An optical attenuator with path-matched loss is used in place of the circuit when performing back to back measurements to ensure comparable noise performance in the receiver amplifier.

The data integrity is verified through bit error rate measurements for each of the three data rates. For the multiplexed OTDM signals (160 and 320Gbit/s) this is done by individually selecting and characterising lower line-rate time multiplexed tributaries at the receiver, 40 and 10Gbit/s for 160 and 320Gbit/s, respectively. These are selected either by gating an electro-absorption modulator at 40GHz or by optically mixing the data signal with a 10GHz phase-locked pulse train in a periodically poled Lithium Niobate crystal [116].

Figure 4.9 plots the error rates as a function of received optical power for each data rate. Error rates below 10^{-9} are readily achieved on the tested paths. Measurements performed without the switch in the test path are labelled as the input measurements. These serve as a reference for power penalty measurements.

Data points, for all cases, of the switch circuit output measurements in Figure 4.9 also show a discernable deviation from the anticipated logarithmic sensitivity response of the receiver. The deviation from the back to back response increases with the number of stages. This degradation may be attributable to a build up of amplified spontaneous emission and signal distortion. All traces indicate error rates to below 10^{-9} with evidence of error floors only at the very high serial line rate of 320Gbit/s.

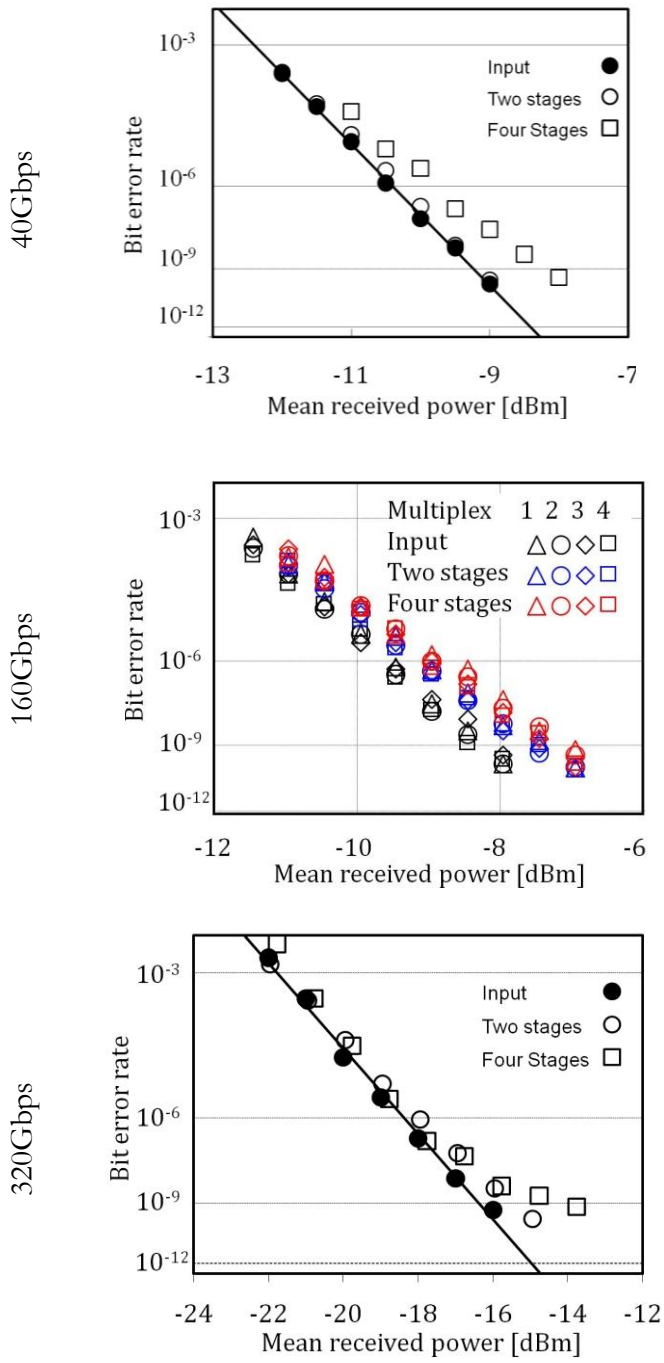


Figure 4.9: Data integrity assessed through bit error rate measurements.

For the 40Gbit/s data routing experiments, the electrode current settings are 120mA for each electrode *a* and *c*. Negligible power penalty is observed for two switch stages with near-complete overlap between the input signal and two stages path error rate dependence on receiver power. A small deviation in slope is evident for the four stage analysis leading to a power penalty of order 1dB.

For the 160 and 320Gbit/s OTDM data routing experiments, all tributary channels are assessed independently to study the routed data integrity through error rate performance and power penalty. In the 160Gbit/s assessment, the power penalty for the two stages of SOA crossbar switch elements is measured to be of the order of 0.6dB for switch operating currents for electrodes *a* and *c* of 115mA and an in-fibre input power of +7 dBm. This power penalty increases to 1.2dB for the four stage path operating at bias currents are 95, 100, 115, 120mA for the four electrode combination, *bcek*.

For the 320Gbit/s data routing, the two stage path requires the on-state operation for the bar electrodes *h* and *i*. These are both biased at 85mA. The four stage routing is enabled by biasing electrodes *k, i, e* and *g* with currents 75mA, 82mA, 93mA and 100mA respectively. The power penalty at the error rate of 10^{-9} is observed to increase from 0.8dB for two stages up to 2.2dB for four stages.

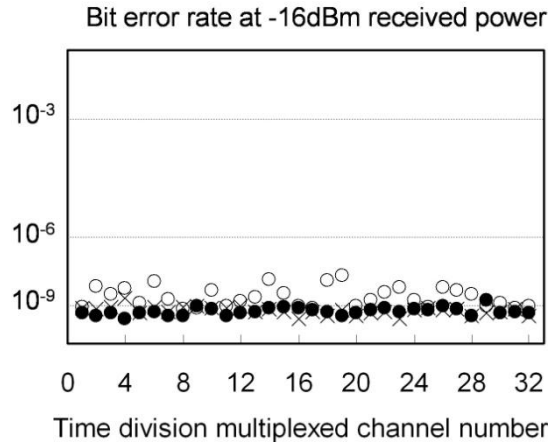


Figure 4.10: Error rate performance for all channels. For 2-stages (filled symbols) and 4-stages (open symbols).

To ensure clarity, and verify successful 320Gbit/s data transmission for the remaining channels, BER is presented for all the channels. At -16dBm received power, all channels operate with error rates below 10^{-7} as shown in Figure 4.10.

4.5.3 160Gbps line-rate data routing in a periodic dynamic environments

The photonic integrated switch circuit is dynamically reconfigured using a bespoke Avtech complementary-output pulse generator with sub-nanosecond transition times. Optical transition times of 1.2 ns (20%-80%) are observed for a current step from 0mA to 115mA under steady state optical input. The pulse generator is clocked from the 10Gbit/s pulse pattern generator as shown in the testbed schematic in Figure 4.7. The periodic electronic control signals have a high-level On-state duration of 409.6ns followed by the same duration off-state signal. Restrictions imposed by the available gated bit error rate test equipment required that the optical data was demultiplexed by a factor of 16:1 to a line-rate of 10Gbps by using two cascaded Electro-Absorption Modulators.

The pulse pattern sequence is programmed and generated at the 40Gbit/s transmitter, and the 10Gbit/s error detector is synchronised and directly programmed to enable bit level comparisons and thus bit error rate measurements for the tributary channels. The in-fiber optical input power is set at +7dBm and injected to both inputs *I2* and *I3*. The output is monitored at *O1*. The centre wavelength was set at 1557nm.

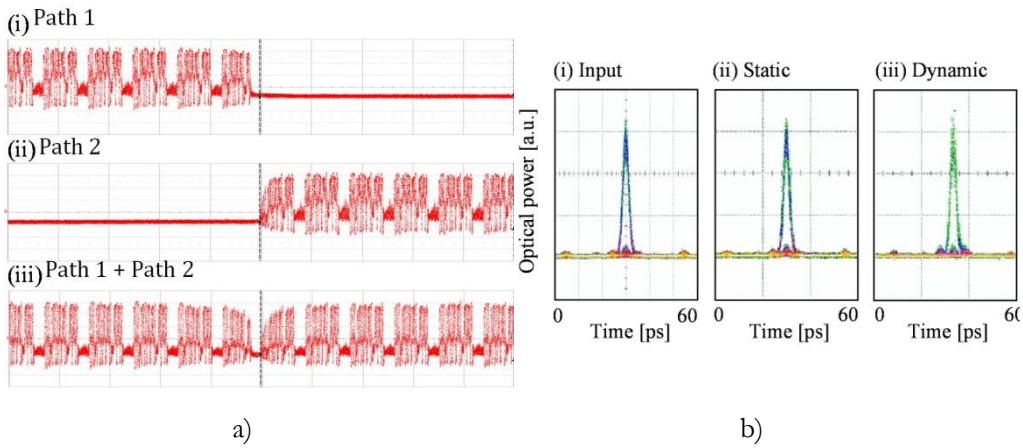
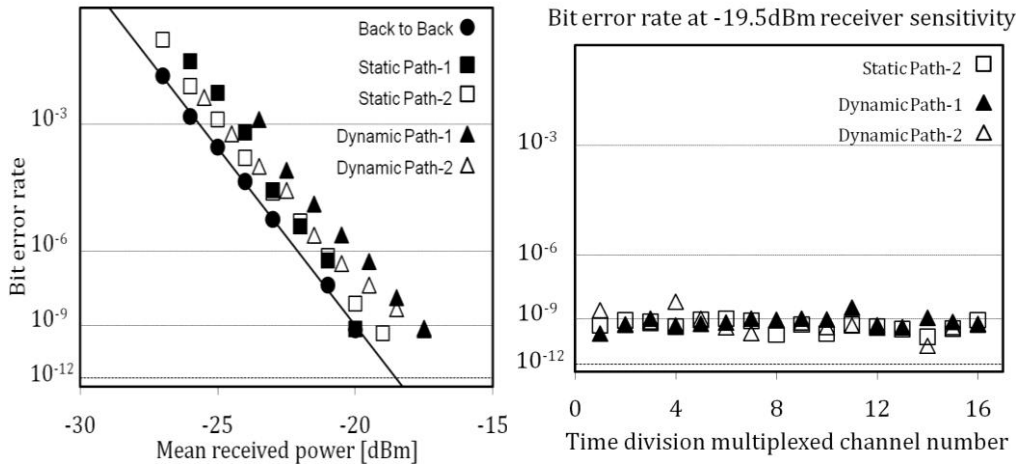


Figure 4.11: a) Time traces (span 73ns) showing dynamic packet routing. b) Eye diagrams for representative demultiplexed 10Git/s tributary channel.

Figure 4.11 shows both the time traces for the dynamically reconfigured switch and the eye diagrams evaluated for the time demultiplexed 10Gbps tributary representative channel. The input, output and dynamically routed signals are each presented for channel 1 showing good eye opening and limited crosstalk.

Bit error rate measurements are performed for both the static conditions, whereby the crossbar switch elements are operating with an invariant current and also for the dynamic condition, whereby the pulse generator periodically reconfigures the switch.



a) b)

Figure 4.12: a) Bit error rate comparison of static control and dynamic routing, b) Error rate at receiver sensitivity for each of the sixteen 10Gbit/s demultiplexed tributaries.

Bit error rate data for static electronic control are presented using squares in Figure 4.12a to reveal a power penalty of 0.8dB for the first tributary channel. Dynamic measurements for the switched signal are shown with triangles, indicating power penalties between 2.0dB and 2.2 dB. The input back to back signal is also shown to indicate the baseline for the power penalty measurements. Error measurement for the dynamically switched configuration is performed for both paths with a window of 384ns within the period of 819.2ns. Performance is measured for each of the time demultiplexed tributaries. For clarity and rigour, data for the remaining fifteen tributaries are presented in terms of error rates at a fixed receiver power. Sensitivity values at the bit error rate of 10^{-9} are recorded at the receiver power level of -19.5dBm in Figure 4.12b and are observed to vary between 10^{-8} and 10^{-10} across all the channels.

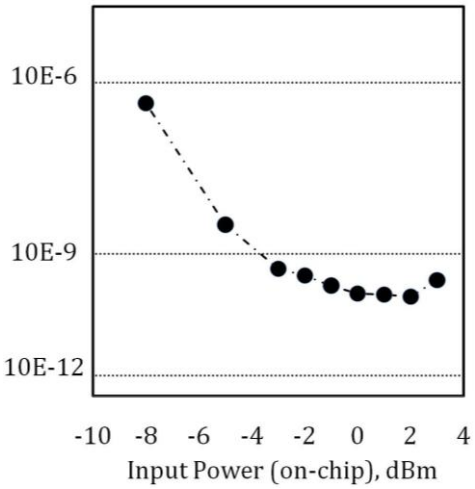


Figure 4.13: : Input Power Dynamic range for path (I3-›O1) operating at 160Gbit/s line rate. Receiver input power of -19 dBm.

The dynamic range for the circuit is studied in terms of bit error rate degradation for static operation. Here the input power into the switch, and signal degradation is monitored in terms of the degradation in bit error rate for a range of circuit input powers. Only a modest sensitivity of error rate to input power is observed over a power range from – 4dBm to + 3dBm as shown in Figure 4.13.

4.6 Discussion

The design, implementation and the demonstration of the first four stage monolithic photonic switching circuit is presented. The low-penalty transmission at record serial 160 and 320Gbit/s line rate represents an important advance towards high-speed photonic signal processing. This is an important finding as further performance enhancement may be anticipated with an optimised power map within the circuit. Increasing the splitting losses between each stage might allow the amplifiers to operate in a lower noise figure regime and enable a rapid increase in connectivity. This enables a more rapid scaling of connectivity with the number of stages, providing a promising route to tens of connections.

Dynamic characterisation of the circuit has been performed with bit error rate testing to verify fast re-configurability. The periodic nature of the measurement scheme does however lead to a fixed on-state time period, and in this work, a fixed 50% duty cycle for the crossbar states. The aperiodic mode

of operation which might be anticipated in networking environments is not therefore studied due to technical difficulties to realize it. While thermal crosstalk is not observed in this study, this may be expected to play an increasingly important role under such a mode of operation.

The circuit real estate in this circuit has been predominantly defined by the constraints in active-passive re-growth mask. The single column of active islands in this work is a restriction imposed only by the use of a predefined pattern for the active regions. Future design can therefore remove considerable numbers of bends and crossings through customised active island placement for improvements in signal to noise performance. The operating gain which can be accessed within the circuit has been modest due to 34% reflections at both the input and output facets. This leads the circuit to oscillate at relatively low currents and has constrained the amount of gain which can be used at each SOA. Anti-reflection coatings can be readily applied to reduce reflections and access the higher on-chip gain.

Benchmarking with alternative technologies may be most readily considered in terms of the energy consumption per switched bit. In the 160Gbit/s transmission case, for an operating current of 115mA for each crossbar switch element, a series resistance of 6Ω and a diode voltage at 1550nm wavelength of 0.8V the power consumption per crossbar is estimated to be 0.2W. This may be extrapolated to 1.2W for a fully operational circuit. For an N-stage planar circuit with four inputs operating with 160Gbps per path, and six crossbars, an energy efficiency of order 1.6pJ/bit may be estimated. For the 320Gbit/s transmission this value reduces to 0.93 picojoule per bit optoelectronic energy consumption. Which is almost two orders of magnitude smaller than the value predicted by R. Tucker of 80pJ per bit in [19]. The selection of the proper epitaxy (enough gain) and the right operation power map (OSNR management) of the device produced the excellent results obtained in terms of capacity and number of cascaded SOAs.

Until now I have presented the performance of photonic integrated switching circuits which were fabricated using different material systems (QD and MQW) and different integration approaches (all-active and active-passive). A valid question would be how do these devices compare?. The answer to this question relies on the functionality that these devices do, i.e. switching and how well they realize it. From the experimental data the comparisons I can draw are the following. Both presented switching speeds in a nanosecond timescale. Switches need to have excellent extinction ratio to be able to scale to a large port count, i.e. larger switches, and, of course to minimize crosstalk related impairments. The MQW devices exceeded the QD devices performance almost

by a factor of 4 when both were routing data through 2 SOA-stages. It is important to mention that these results were obtained operating the QD devices not in the proper conditions as I have shown in a previous chapter. I think this extinction ratio limitation will not be a problem in future QD switches with improved epitaxy designs.

When scaling into large port count switches it is important to use multistage architectures. The possible drawback of SOA-based switching stages is the possible signal impairments due to noise accumulation and gain saturation. For this reason it would be helpful to have SOAs with low noise figure and high saturation input power. The QDs showed a large saturation input power ~5dBm and when data integrity was assessed for the multi-stage device, the signal degradation due to noise was negligible, only 0.5dB penalty, even when the device was fabricated in an all active integration approach. In the case of the MQW device the signal impairment due to noise was ~0.8dB. This was obtained for the 4-stage case and as for the gain saturation very little can be discuss as no experimental data indicates any impairment related to this.

The use of active passive integration reduces the overall power consumption of the switching devices as there is no need to bias the shuffle networks interconnecting the SOAs. Another important advantage is the removal of unnecessary spontaneous emission noise accumulation along the switches. This helps to avoid spectral narrowing which may limit the operational bandwidth. The energy consumption comparison between QDs and MQW shows a 40 percent higher current density per gate in the case of QDs with respect to the MQW gates. This is because of the low gain levels in QDs at low current levels. In conclusion both material systems had excellent performances. In order to make an objective comparison it is necessary to assess the devices under the same circumstances and technological maturity. But the obtained results show an exciting future for active-passive photonic integrated switches either with MQW or QDs. In the next section the reasons behind the low signal degradation in multistage SOA-based switches will be discuss all of this under an ultrafast line rate transmission framework.

4.7 Summary

The highest line-rate serial transmission (320Gbit/s) is reported for a multistage photonic integrated switching network. A route to energy efficient signal processing through increasingly sophisticated, high speed, photonic integrated circuits is identified. This represents a step change in the operating speeds for multi-stage integrated photonics in general, and optoelectronic switching networks in particular.

Chapter

5 Capacity limits in Monolithic Multistage Switches

This chapter make use of three different models: VPIsystems, distortion model and a noise model to help in the understanding of the role that distortion and noise accumulation has in multistage circuits operating at high OTDM speeds.

5.1 Introduction

Most of the proposed approaches to create highly functional, low power and large scale photonic interconnection technologies implement semiconductor optical amplifier (SOA) as gates. These SOA-based photonic interconnects offer the potential for a broadband, fast reconfigurable and loss-less routing [56] with electrical energy consumption nearly independent to the line-rate or data format [6] thus breaking the electronics' vicious link between rising line-rate and increasing energy consumption.

To achieve higher capacity-bandwidth systems, recent SOA-based test-bed studies have focussed on the routing of tens of wavelength multiplexed 40Gbps data signals over single and multiple stage networks of discrete switching elements [17], [57-61]. By using nonlinearities in discrete SOAs (e.g. cross gain and/or cross phase modulation) higher line rates, ultrafast routing and ultrahigh speed optical demultiplexing has been achieved [62-64]. Remarkable challenges still remain in terms of cost, connectivity, and footprint, but photonic integration of these interconnection technologies [65], [66] is now striving to deliver in many of these areas [67].

Integrated SOA-based interconnection sub-systems, 40Gbps transmission has been demonstrated for multi-wavelength transmitters [87], tuneable wavelength convertors [88], and two-input two-output switch matrices [89]. However, data integrity has mainly been studied for single stage circuits, and

multi-stage networks of switches are required for highly scalable network connectivity. A 3-stage monolithically integrated 16x16 Clos network routing 10Gbps data [90] and a monolithically integrated SOA-based network, with up to 4-stages, routing 320Gbps line-rate data represent the most complex circuits reported to date [114]. In this chapter, simulation studies are presented to continue analyzing the dependence of data integrity as both, the line-rate and the number of SOA-stages, increases. Thus, providing insight into the scaling of line rate and connectivity for larger scale integrated switching circuits.

5.2 Multistage switch model and calibration

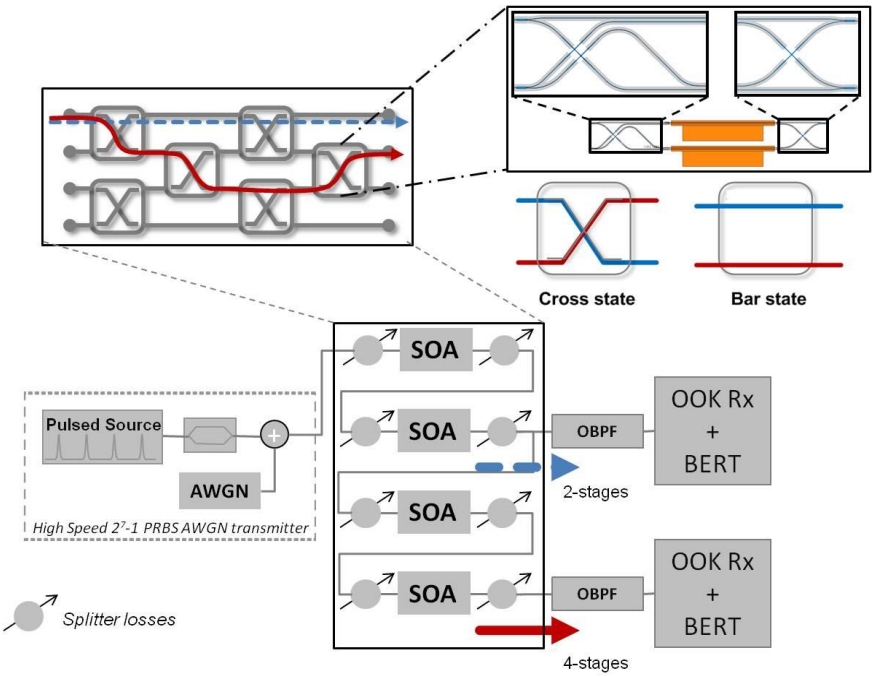


Figure 5.1: Schematic for ultrahigh bit-rate transmission simulation over SOA Switch Networks

The multistage switching network under study is based on six monolithically interconnected 2x2 crossbar switch elements. Four inputs connect to four outputs by means of electronically programmable SOA gates. While this is representative of a broad class of switches, the N-stage planar architecture has recently been considered in our experiments [112], [114]. The optical paths comprise a high number of passive elements as well as active semiconductor optical amplifier gates within the 2x2 crossbar elements themselves [98]. The

paths include long (4-SOA-stages) and short (2-SOA stages) paths through the circuit, and therefore allow a study into the scalability of massively broadband photonic integrated switching circuits. Figure 5.1 shows the high line-rate simulation arrangement for the multistage circuit with the short and the long paths indicated. To understand the scalability of massively broadband photonic integrated switching circuits, the evolution of distortion and noise through the interconnection network was described through the implementation of a photonic transmission-line MQWs SOA numerical model (TLM) using the VPItransmissionMaker software.

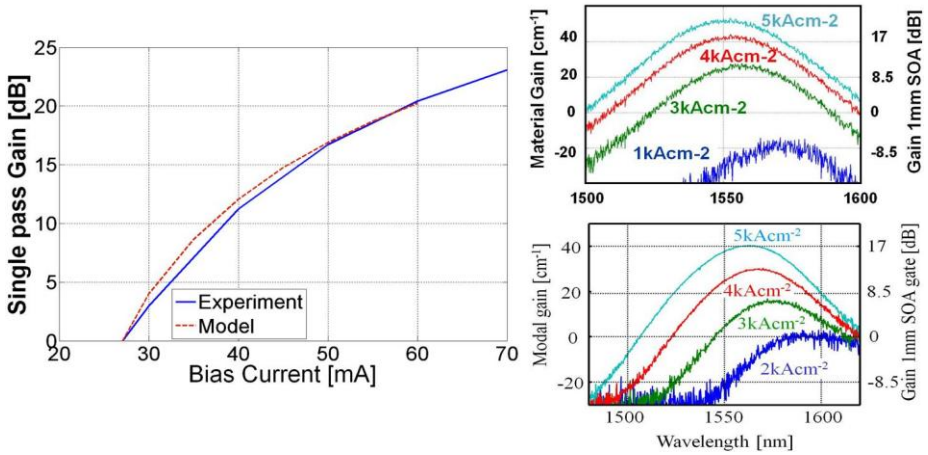


Figure 5.2: Static theoretical validation for the SOA switching element. Simulation and experiment.

Experimental data for individual components are used to configure the simulations. Passive components such as multimode interference (MMI) waveguides are implemented as a discrete loss (3.5dB/MMI) to replicate the inter-stage switch loss. Active elements such as the SOAs are described in terms of the current resolved gain spectrum which were calibrated using the experimental results [114]. The simulated wavelength dependent modal gain was assumed to be parabolic, as shown in Figure 5.2 with the model parameters detailed in Table 5.1. Figure 5.2 shows the modal gain spectra for different bias current levels for the experimental and theoretical characterisation of a 1mm long SOA. SOAs' model parameters as: internal loss, current injection efficiency, carrier dynamics and the logarithmic gain coefficient were obtained through detail analysis of the data obtained through the experimental characterisation of a set of fabricated lasers with different cavity length. The laser characterisation was made by Dr. Martijn Heck from the OED group.

Table 5.1: SOA TLM Model

Parameter	Value	Unit
Device Structure		
Active region type	MQW	
Device section length	1000e-6	m
Active region width	2e-6	m
Active region thickness MQW	30e-9	m
Active region thickness SCH	210e-9	m
Current injection efficiency	0.6	
Optical Parameters		
Nominal wavelength	1.5525e-6	m
Group Effective Index	3.7	
Internal loss	10e2	1/m
Confinement Factor MQW	0.07	
Confinement Factor SCH	0.56	
Facet Reflectivity	1e-6	
Carrier Dynamics		
Linear Recombination	1e9	1/s
Bimolecular Recombination	1.6e-16	m^3/s
Auger Recombination	8.5e-41	m^6/s
Carrier capture time constant	70e-12	s
Carrier escape time constant	140e-12	s
Initial carrier density	1e23	1/m^3
Gain Parameters		
Gain Model	Logarithmic	
Gain coefficient logarithmic	880e2	1/m
Carrier Density Transparency	9e23	1/m^3
Gain shape model	Parabolic	
Gain bandwidth	22e23	Hz
Spontaneous Emission		
Noise Model	Inversion Parameter	
Inversion Parameter	1.5	
Noise Bandwidth	22e23	Hz

5.3 Dynamic Range

Using the calibrated SOA TLM model, further simulation was performed to investigate the power penalty performance of multistage networks at ultrahigh line-rate transmission. A pseudo random bit sequence (PRBS) with pattern length 2^7-1 was imprinted on the return to zero (RZ) optical pulse train at 1552.5nm wavelength with added white Gaussian noise (AWGN). This was injected into the circuit under test and the time-resolved output field from one SOA-stage is input to the next stage to model the accumulation of noise and distortion. The device output signal degradation is monitored over a broad range of operating conditions using a thermal-noise-limited receiver.

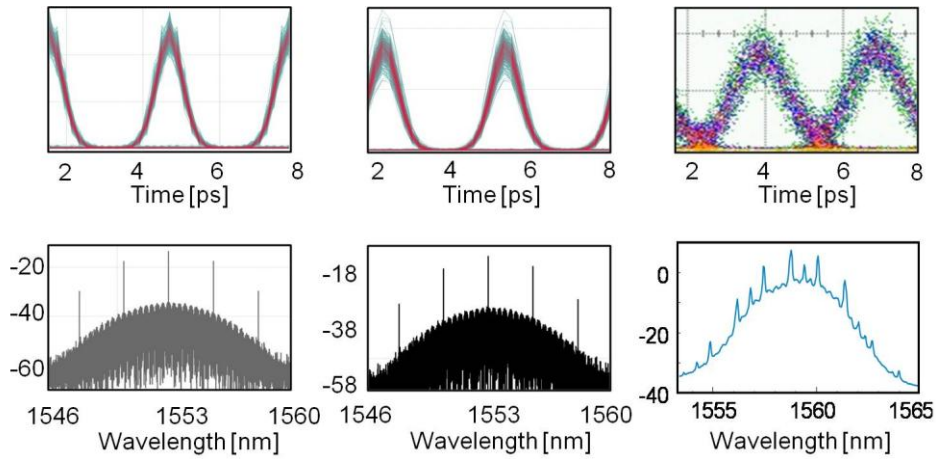


Figure 5.3: Transmitted and routed signal after a 2-stage path. left) Simulation input, middle) Simulation output, right) Experimental results. All the eye patterns are normalized to their respective average signal powers.

Figure 5.3 shows the eye diagrams and spectra for a 320Gbps line rate signal for both the experimental [114] and simulated 2-stage routing case. Power penalty analysis after routing ultrahigh line-rates through a multistage network was carried out to assess the data integrity. The receiver sensitivity power penalty was defined as the required increase in the receiver input power to maintain the same BER at 10^{-9}.

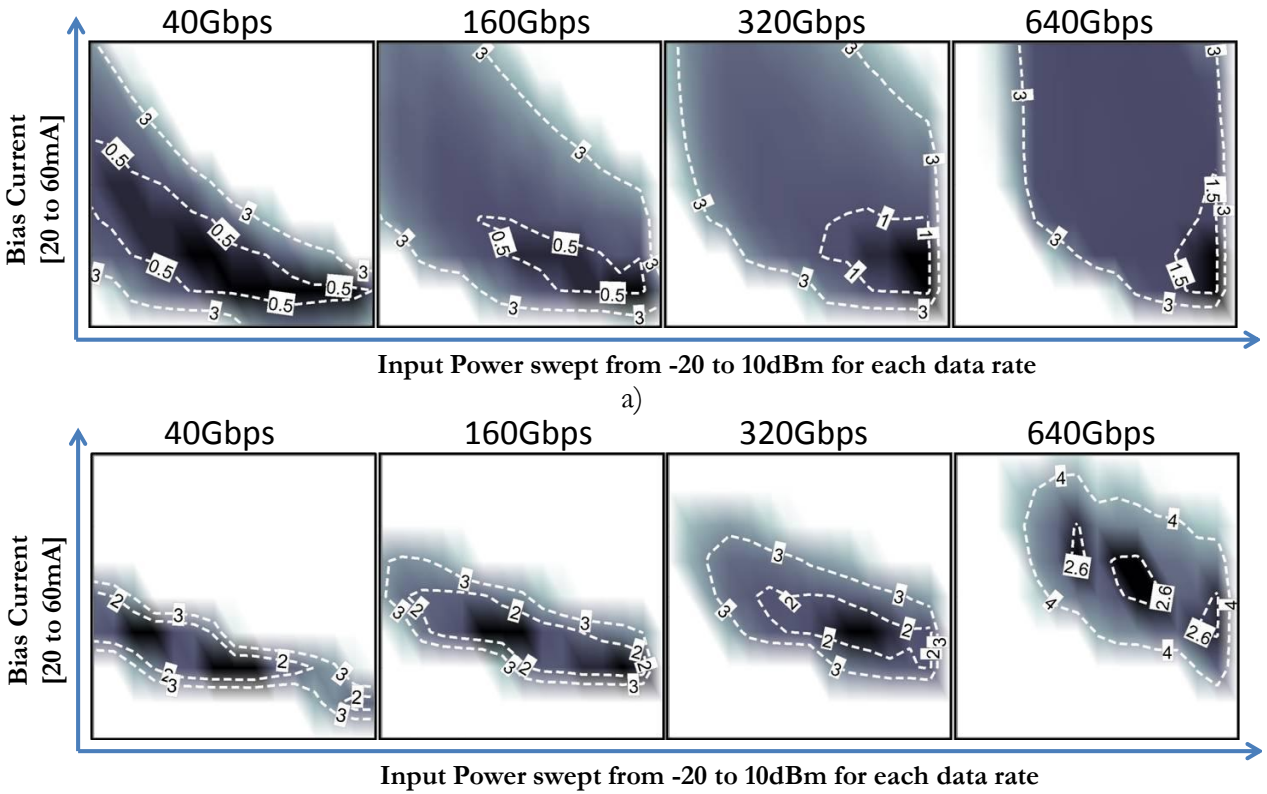


Figure 5.4: Power Penalty maps for a) 2-stages and b) 4-stages. These maps indicate how the power penalty changes as the bias current and input optical power changes. The contour lines delimit the area where the power penalty is lower than the value indicated by the contour line. They were obtained as the number of cascaded SOAs increases and for different line rates 40Gbps, 160Gbps, 320Gbps, 640Gbps.

To monitor the power penalty, a receiver using the Gaussian approximation as the BER estimation method was implemented. Fourth-order Bessel band-pass optical and low-pass electrical filters were implemented with bandwidths of 2.4 and 1.3 times the line-rate, respectively [138]. The filter values depend on the modulation format. For NRZ-OOK the value is 0.75 times the line rate and 1.3 times the line rate for RZ-OOK.

The power penalty maps are obtained and plotted in figure 5.4. These maps indicate how the power penalty changes as the bias current and input optical power changes. The bias current was swept from 20mA to 60mA and the input power from -20 to 10dBm. The contour lines delimit the area where the power penalty is lower than the value indicated by the contour line. In Figure 5.4 the power penalty maps were obtained as the number of cascaded SOAs increases from 2 (5.4a) to 4 (5.4b) and for different line rates (left to right in figure 5.4) 40Gbps, 160Gbps, 320Gbps, 640Gbps.

The power penalty map evolution, as the number of stages increases, shows that the power penalty floor narrows i.e. input bias dynamic range (IBDR)[9] narrows. This behaviour is observed for all the transmitted line-rates and is related to the noise accumulation as the stage number increases.

Furthermore, as the transmitted line-rate increases, the input power dynamic range (IPDR)[10] narrows but the power penalty floor (IBDR) broadens. Figure 5.4a shows that the achievable power penalty minima, in the 2-stage case, appear in a region between 25 and 35mA which corresponds to a single pass gain per SOA between 0 and 6dB. In figure 5.4b, for the 4-stage scenario, the optimum operation point moves towards higher current and input power levels as the line-rate increases.

[9] Useful operating bias current range

[10] Useful operating input signal power range

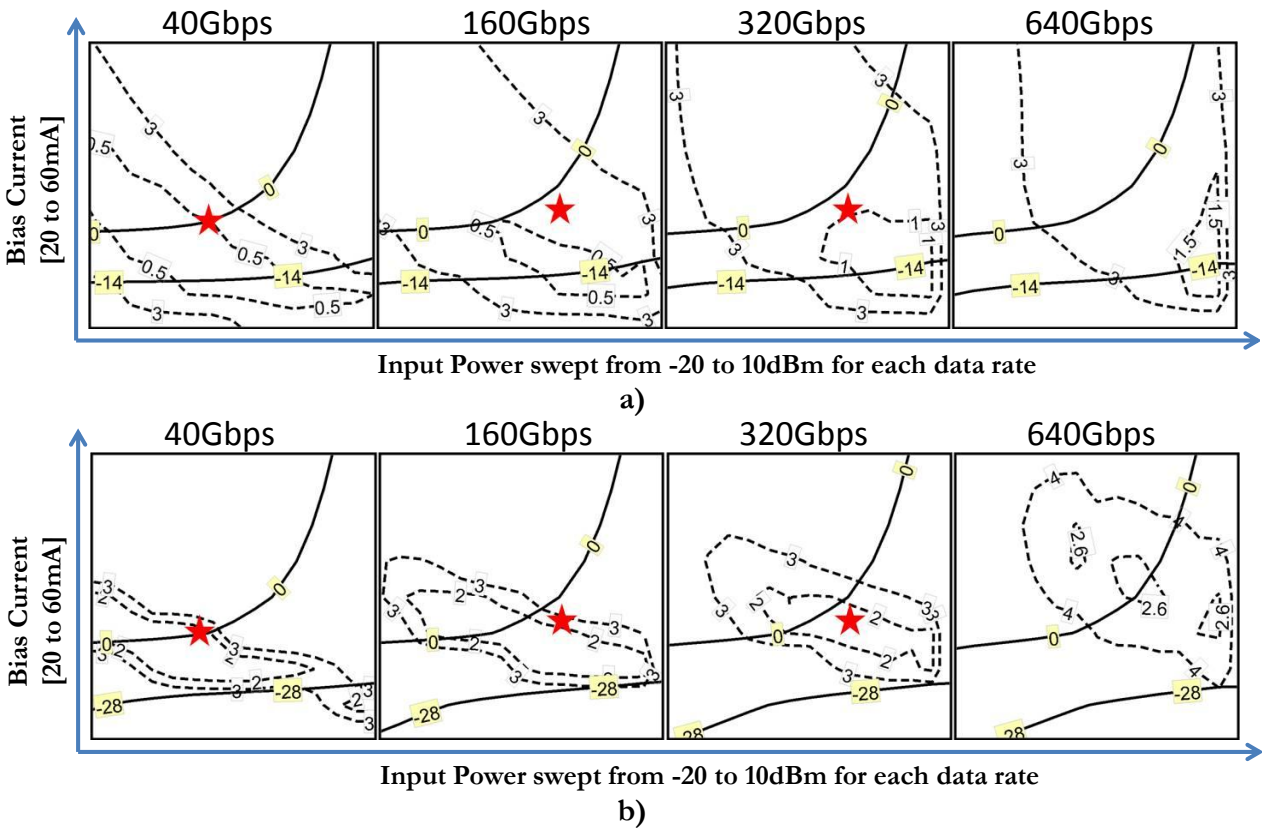
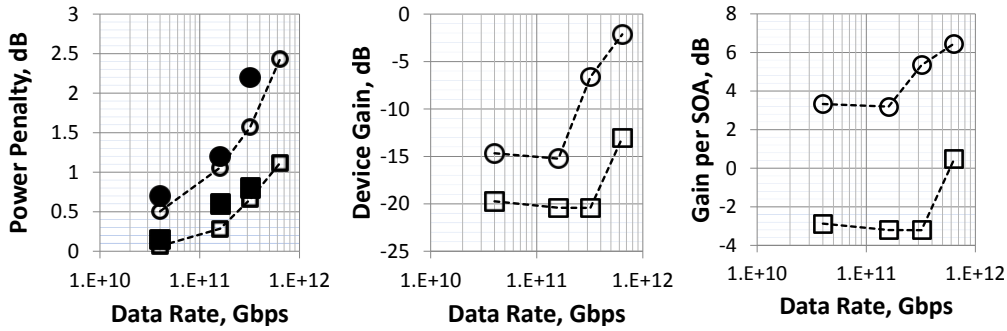


Figure 5.5: Power penalty tolerance. Solid lines indicate circuit gain contour level evolution. Broken lines indicate power penalty contour levels. a) and b) 2 and 4 stages, respectively. The star indicates the input power and average bias current settings used in the experimental characterisation.

5.4 Experimental Comparison

A study on the tolerance for the operation conditions was carried out to better understand the device limitations. For this purpose, the device gain and power penalty contour lines are plot together and shown in Figure 5.5. The solid contour lines indicate the circuit gain-evolution when both the bias current and the input optical power change. In each plot, the lower solid line marked for -14dB (2-stages figure 5.5a) and -28dB (4-stages figure 5.5b) shows the splitter losses contour level. This therefore indicates that the gain per SOA is at 0dB (transparency). The upper solid contour line shows lossless circuit operation indicating that the splitter losses have been compensated. As the input power increases, the biasing has to increase in order to compensate the path losses due to gain saturation in the SOAs, explaining the upper contour line evolution. The broken contour lines show the power penalty. The stars indicate the input power and average bias current settings used in the experimental characterisation. For all the transmitted line-rates and stage numbers, the optimum operation point can be found in between the solid contour lines, indicating that the device does not need to operate under high gain conditions. In Figure 5.5, as the stage number increases the power penalty floor reduces due to noise accumulation and when the line-rate increases, the optimum operation point moves towards circuit transparency due to the more stringent OSNR requirements. In Figure 5.5a and Figure 5.5b, the highest simulated line-rate (640Gbps) requires relatively higher optical power levels (~6dBm) to achieve the optimum operation point. This is due to the SOA noise reduction at high input powers.

To explore the scope for ultrahigh-data-rate transmission in monolithic multistage networks, the experimental trend and the optimum/minimum simulated power penalty trend for different number of stages are presented in Figure 5.6a for the optimum operation conditions. The simulation showed good agreement with the experimental results indicating that the power penalty at the error rate of 10^{-9} increases with the number of stages and data rate. These results show that 10^{-9} error rate transmission of ultrafast signals, extrapolating to 640Gbps is possible through photonic integrated multistage SOA-based circuits. However the power penalty degrades to 1.2dB and 2.6dB for the 2 and 4 stages, respectively.



a) b) c)

Figure 5.6: a) Experimental (fill symbols) and simulation (open symbols) trends for power penalty degradation. Square and circular symbols represent 2 and 4 SOA stages, respectively. b) and c) gain trends.

The optimum power penalty gain evolution for both the short and long paths is shown in Figure 5.6b and Figure 5.6c. Figure 5.6c shows the gain evolution that each SOA provides. All the line-rates operate with low SOA gain levels ranging between -4 and 6dB for both the short and long paths. Due to the low noise accumulation and therefore better OSNR when a small number of cascaded SOAs are used, the required gain for the short path is lower than the one required for the long path. For both paths, the required gain per SOA to achieve the optimum power penalty increases as the line-rate increases. This is explained by the less demanding OSNR requirements at lower line-rates. For the 4-stages case the gain per SOA trend saturates as the line rate increases.

The power penalty maps, shown in Figure 5.4 and Figure 5.5, point out that the input power dynamic range (IPDR) and power penalty floor (IBDR) evolve as a function of the stage number and transmission line-rate.

To study this behaviour the IPDR and the IBDR for the simulated optimum power penalty were plotted in Figure 5.7. The IPDR evolution remains almost constant after the minimum optical power reaches the proper OSNR level at the receiver is achieved. This is observed for the short and long paths as the data line-rate increases. The IPDR magnitude decreases as the line-rate increases. As the stage number increases the best-case power penalty for each line rate also increases 1 ± 0.5dB due to noise accumulation.

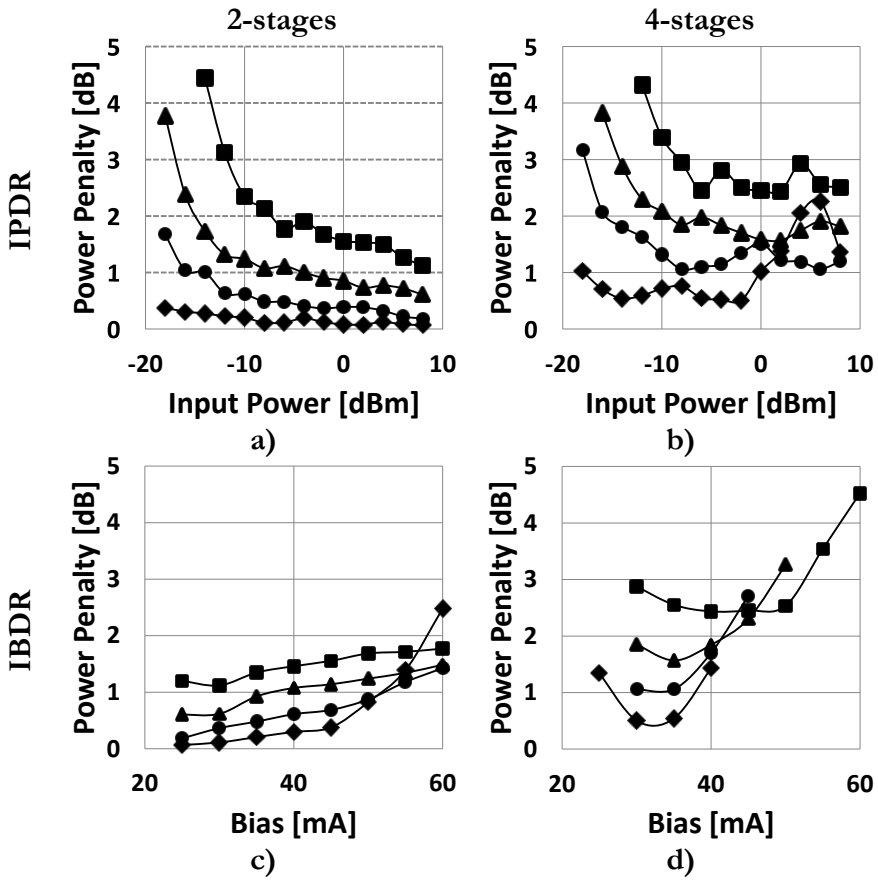


Figure 5.7: Input Power Dynamic Range (IPDR) and Input Bias Dynamic Range (IBDR) power penalty degradation for best-case operation point. Rhombus (40Gbps), circles (160Gbps), triangles (320Gbps), squares (640Gbps) represent different line rates.

Figures 5.7c and 5.7d show the IBDR evolution. For the short path case, the power penalty increases linearly as the input bias increases. This is due, mainly, to the higher ASE noise accumulation levels as the current increases. This becomes important as the stage number increases, causing the IBDR to narrow for all the transmitted line-rates due to the more stringent OSNR operation requirements.

For the 4-stage scenario and as the line rate increases, a broadening in the IBDR is observed from 15mA to up to 30mA. The larger broadening is due to the signal distortion immunity at ultrahigh data rates due to the SOA high-pass frequency response [139] and is explored in the next section.

5.5 Distortion

To characterise the SOA's single-pass gain frequency response a large-signal analysis using the implemented VPI 4QW-SOA model was performed. The simulation used a single frequency radio frequency (RF) tone, frequency-swept and amplitude modulated with an optical input power of 0dBm and 100% modulation depth. The SOA's output signal was assessed through the heterodyne detection of the instantaneous optical power and frequency of the swept sinusoidal optical signal. The heterodyne detection calculates the average phase and magnitude of an electrical signal by mixing the input waveform with the in-phase and quadrature component of a local oscillator and then calculates the mean of the mixer outputs of the in-phase and quadrature signals. With this technique the harmonic distortion is assessed in isolation. The obtained single frequency response is normalized to the maximum gain in order to better distinguish its frequency response.

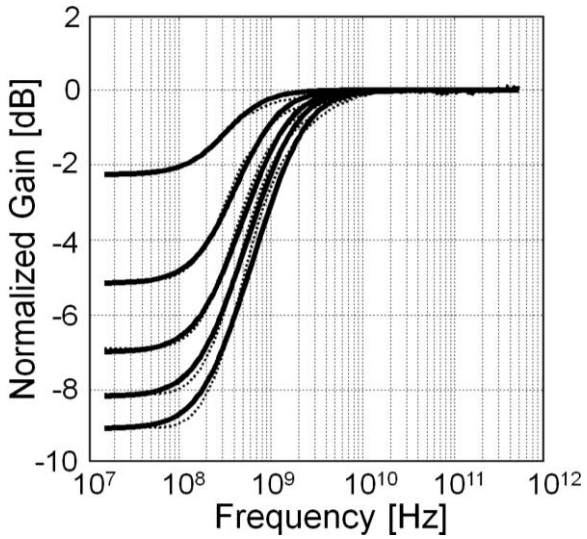


Figure 5.8: Normalized single tone frequency response for a single SOA in "large" signal regime. The solid line corresponds to the fitted SOA large signal response

From Figure 5.8, several interesting characteristics of the SOA gain frequency response can be observed. The quasi-highpass[11] magnitude response becomes steeper as the bias current increases. At low modulation frequencies the single-pass gain gets compressed due to the stimulated emission process, i.e. reduction of optical gain as a result of carrier depletion by the amplification

[11] In a highpass response the zero frequency is infinitely small.

process [140]. This gain compression disappears at high modulation frequencies because the carrier population cannot follow the signal amplitude changes anymore. The normalized single frequency response was approximated by the function,

$$H(i\,\Omega) = 1 - \frac{h_{eff}}{i\,\Omega\,\tau_{eff} + 1} \tag{1}$$

Where the fitting parameters h_{eff} and τ_{eff} represent the normalized gain-compression factor and the effective carrier life time, respectively. Figure 5.8 depicts the approximated function in excellent agreement with the simulated results, clearly showing that the normalize gain-compression increases as the current increases.

Table 5.2: Parameters from the fitting function

I, [mA]	$\boldsymbol{h_{eff}}$	$\boldsymbol{\tau_{eff}[ps]}$
28	0.227	380
36	0.445	270
44	0.550	210
52	0.610	180
60	0.650	150

The fitting parameters, shown in Table 5.2, reveal that h_{eff} increases and τ_{eff} decreases as the bias current increases. As mentioned, the underlying cause for the gain compression is the limited rate at which the amount of carriers is replenished while being depleted by stimulated emission. Two important factors delimit the gain-compression magnitude, namely the rates from: the carrier lifetime and the stimulated emission rate, ${\tau_{sp}}^{-1}$ and ${\tau_{sat}}^{-1}$ respectively, as shown in eqs 2-4.

$$h_{eff} \approx \frac{g_0}{g_{CW}} \frac{\tau_{eff}}{\tau_{sp} + \tau_{sat}} \tag{2}$$

$$\tau_{eff} = \frac{1}{{\tau_{sp}}^{-1} + {\tau_{sat}}^{-1}} \tag{3}$$

$${\tau_{sat}}^{-1} = \frac{\bar{P}}{E_{sat}} \tag{4}$$

Equations 2 - 4 were obtained from the frequency analysis of the SOA's rate equations that is presented in appendix B. These equations express how the fitting parameters h_{eff} and τ_{eff} relate to the mentioned factors ${\tau_{sp}}^{-1}$ and

$\tau_{sat}{}^{-1}$. The unsaturated gain, CW gain, average power and saturation energy are denoted by g_0, g_{CW}, $\bar{P}$, E_{sat}, respectively.

The SOA's single frequency response shows that the frequency components of the transmitted modulated signal will amplify differently resulting in a distorted output signal. Bit error rate measurements were performed to evaluate the data integrity through the power penalty analysis of a purely amplitude distorted signal. This was assessed using a thermal-noise-limited receiver to detect the point-wise product between the normalized SOA frequency-response and the 2^7-1 long-PRBS input RZ-data signal. The input signal with a fixed pattern length of 128bit was convolved with the transfer function with the form shown in Equation 1 for a range of operating currents.

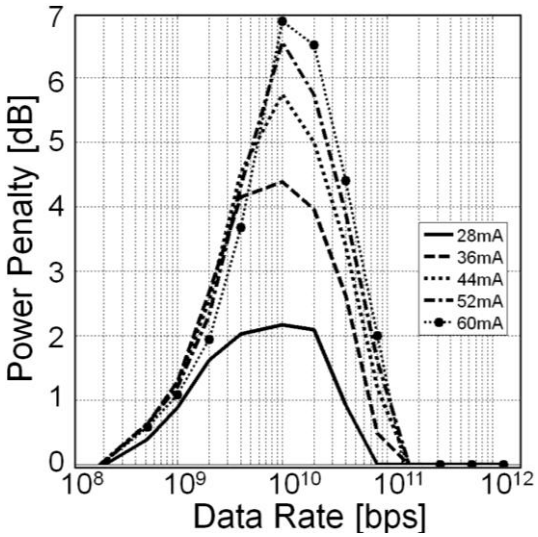


Figure 5.9: Power penalty vs. data rate evolution

In Figure 5.9, the power penalty as a function of data rate is depicted. As the bias current increases the signal degradation increases showing a maximum power penalty level at 10Gbps. There is a data rate band form 0.2Gbps to 100Gbps where the power penalty increases achieving a maximum and then decreasing. The mentioned behaviour help to explain the ultrafast data rate transmission capability that SOA-based monolithic switches have due to the low distortion at higher data rates. This effect is analogous to the low distortion one observed in fibre amplifiers with millisecond carrier lifetimes. For these reason, the information content is shifted above the filter edge as data rate increases.

5.6 Noise

The noise accumulation is the main contributor to data degradation in monolithically cascaded SOA circuits [141]. To better understand how the noise accumulation impacts the data integrity, the power penalty frequency evolution was assessed through the implementation of a travelling wave amplifier noise model [142].

Table 5.3: Noise model set of equations.

Signal terms	Units	Noise terms	Units
		$P_{sp} = \eta_{sp}(G-1)h\,f\,B_o$	W
$I_{s1} = \frac{q}{h\,f}\,\frac{r}{D\,(r+1)}\,P_{in}$	A	$I_{sp} = \frac{q}{h\,f}\,P_{sp}$	A
		$N_{shot} = 2\,B_e\,q\,(G\,I_{s1,0}\,\eta_i + I_{sp})\,\eta_o\,L$	A^2
		$N_{s-sp} = 4\,\frac{B_e}{B_o}\,(G\,I_{s1,0}\,\eta_i \times I_{sp})\,(\eta_o\,L)^2$	A^2
$I_{s0} = \frac{q}{h\,f}\,\frac{1}{D\,(r+1)}\,P_{in}$	A		
		$N_{sp-sp} = \frac{B_e}{{B_o}^2}\,(2\,B_o - B_e)\,I_{sp}^2\,(\eta_o\,L)^2$	A^2
		$N_{th} = i_{th}^2\,B_e$	A^2
$S_{1,0} = (G\,\eta_i\,\eta_o\,L\,I_{s1,0})^2$	A^2	$N_T = N_{shot} + N_{s-sp} + N_{sp-sp} + N_{th}$	A^2
$Q = \frac{\sqrt{S_1} - \sqrt{S_0}}{\sqrt{N_{T,1}} + \sqrt{N_{T,0}}}$			

The set of equations than govern the noise model are shown in Table 5.3.The cumulative effect of the amplifier noise, in a system with multiple inline amplifiers, was studied assuming two things: all the amplifiers have equal noise figure and that the amplifier gain equals the loss in between two amplifiers, GL=1. This led to the substitution of the spontaneous emission factor, η_{sp} with the product $k\,\eta_{sp}$ where k is the number of cascaded amplifiers[142], in the spontaneous emission equation, P_{sp} in Table 5.3.

The power receiver sensitivity at 10^{-9} (Q=6) was calculated as a function of data rate and number of cascaded SOAs, using $\eta_{sp} = 1.5$ or an equivalent noise figure of 6.5dB for each SOA. The noise figure is the same obtained from the SOA calibration using the VPI model. The filters' data-rate-dependent

bandwidths were $B_o = 2.4\ R_{bit}$ and $B_e = 1.3\ R_{bit}$ for the optical and electrical filters, respectively [138]. The RZ input data signal had a 25% duty cycle, D, with an extinction ratio, r, of 20:1. For this study the coupling losses were neglected $\eta_i = \eta_o = 1$ and the losses, L, were set to 7dB.

As it is well known [142], direct detection causes beating of signal with ASE (N_{s-sp} after electrical filtering) and ASE with itself (N_{sp-sp}). Due to the large gain of the optical SOA-based switch, the beat noise terms were the dominating noise sources in the receiver. Shot noise as a consequence of the quantum nature of the optoelectronic conversion process (N_{shot}) and thermal noise originating from the detection electronics (N_{th}, with noise power density $i_{th} = 10\ \frac{pA}{\sqrt{Hz}}$ contributed only to a negligible extent to the total noise. It is important to mention that the used parameters in this analysis were the same parameters used for the results obtained during the simulations using the VPI software.

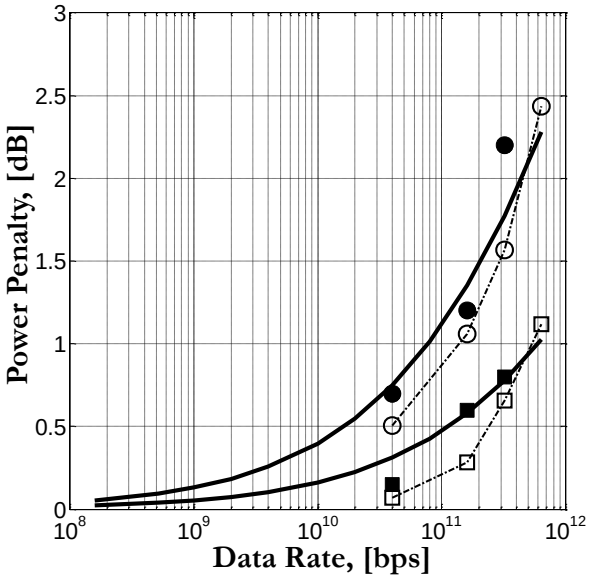


Figure 5.10: Receiver noise simulation results (solid line). Analytical results (solid lines) comparison with the optimum experimental values (solid symbols) and the VPI simulation results (open symbols).

In Figure 5.10, the power penalty trend follows a nonlinear increase with increasing data rate and accumulated noise or number of stages. With higher noise accumulation the power penalty grows faster as the data-rate increases. This behaviour is comparable to the results obtained in previous sections for

the experimental and the VPI simulation data.

Figure 5.10 shows that the experimental power penalty trend can be largely described by the pure noise analysis trend for the optimum modes of operation. In comparison to the VPI results, at relatively low data rates, the pure noise analysis overestimates the power penalty. This is due to the fact that the VPI results were obtained at lower gain regimes, less noise, and not at device transparency GT=1 as in the pure noise analysis case. As the data rate increases the overestimation reduces and both trends become almost equal. This is explained by the fact that, as the data line-rate increases, the operating device gain regime increases close to transparency GT=1, (see Figure 5.6).

5.7 Discussion

Ultrahigh capacity operation is confirmed theoretically up to 320Gbps in monolithic multistage SOA-based switching circuits. Extrapolations to 640Gbps indicate that carrier recombination dependent distortion plays a limited role, but spontaneous noise leads to rapid penalty degradation. The VPI simulation tool neglects a number of important nonlinearities which may also contribute to signal quality degradation as the pulses shorten and powers are enhanced. At Terabit line rates for example, the pulse duration will approach the carrier-carrier scattering time scale. The parabolic gain approximation may also need to be re-evaluated as the signal spectrum approaches the amplifier bandwidth. None the less the model results are in good agreement with the experimental findings when ultrafast line rates are transmitted. The use of three different models (VPI, distortion model and noise model) helped to clarify unknowns about the role of distortion and noise in multistage circuits operating at such high OTDM speeds. The use of other modulation formats might allow higher capacity (>Tbps).

It has been shown through experimental assessments and theoretical analysis that photonic integrated SOA based switches are suitable to scale in capacity and connectivity through the use of multistage schemes. In the next section a 16x16 photonic integrated switch is presented and fabricated.

Chapter

6 Large Scale Photonic Integrated Switching Circuit

In this chapter the development of a large scale photonic integrated SOA based switch is described.

6.1 Introduction

Along this PhD thesis, the characteristics that make SOAs suitable for the future optical interconnect networks have been described. Its nanosecond switching speed makes them suitable for low latency packet routing and its integration capability is a promising feature towards the realisation of large scale compact complex photonic switches [67], [143]. However, high capacity large photonic SOA-based switches have not been implemented yet. Only switches with low energy efficiency but fast switching response (lithium niobate) or switches with slow switching response but with excellent energy consumption (MEMS) have been fabricated into large port counts (128x128[12] for lithium niobate [34] and 1024x1024 for the MEMs [50]).

It is important to mention that a very impressive re-arrangeable Non-blocking 16x16 switch has been already fabricated and assessed in the University of Cambridge, U.K. It uses semiconductor optical amplifiers to form the switching fabric. It has been integrated on a 6.3mm×6.5mm indium phosphide chip using all-active integration. It operates with a power penalty of between 1.8 dB and 5.5 dB (for the longest path) at a BER of 10^{-9} for 10Gbps signals. The power consumption of the switch is 16W [144] which is one of the limitations of this approach together with the low operational bit-rate due to spectral narrowing due to ASE noise accumulation.

In this chapter the development of a large scale photonic integrated SOA

[12] Not fully integrated

based switch is presented. The new switch is thought to be able to route data from 16-inputs to 16-outputs with only three cascaded SOA-stages with an improved power consumption with respect to the Cambridge device as an active passive integration approach has been followed.

6.2 Multistage switches and blocking characteristics

Until now I have been describing the building blocks to develop multistage switches but it is equally important to consider blocking properties of these large port count switches.

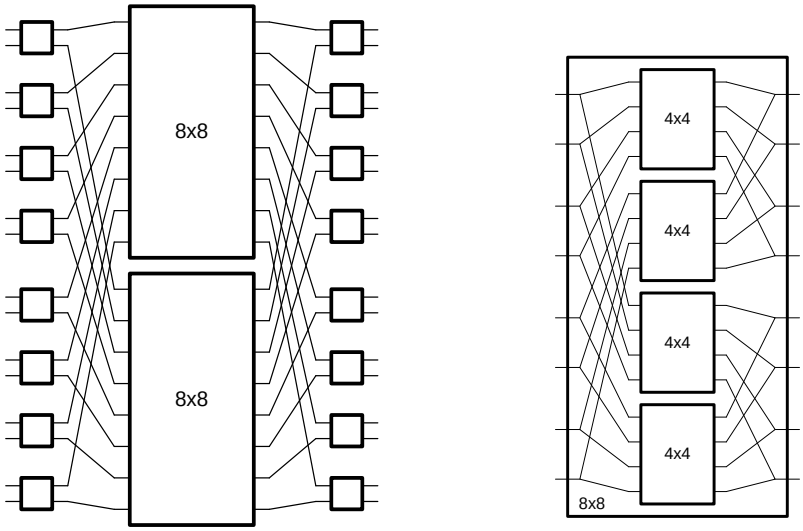
Multistage switch architectures offer efficient switching element scalability for switch architectures with sizes of 16x16 and larger [145]. Switch architectures can be classified by their blocking probabilities. A switch is called non-blocking if it is able to route any available input to any available output at any given time.

There are different categories of non-blocking capabilities:

- Re-arrangeable Non-Blocking (RNB), if any existing connection has to be reconfigured to make the new connection,
- Wide-sense Non-Blocking (WSNB), if a predetermined connection algorithm is required to setup new paths. Do not need to perform any reconfiguration to the existing connection to make new connections.
- Strict-sense Non-Blocking (SNB), if a predetermined connection algorithm is not required to setup new paths. Do not need to perform any reconfiguration to the existing connection to make new connections.

Non-blocking multistage architectures have been proposed in the literature, e.g. Clos [146], Benes [147], Spanke-Benes [129](N-stage) and Banyan [134]. These multistage non-blocking architectures demand a high number of cascaded switching elements (SOAs) and therefore the routing/control algorithms become complex. Besides the control complexity, the optical switch element count has a direct impact on the cost, power consumption and footprint of the switch. In this thesis an optimized optical re-arrangeable non-blocking (RNB) switch architecture using SOAs is proposed to overcome these drawbacks.

6.3 Architecture for the Large Scale SOA based Switch



a) b)

Figure 6.1: Proposed 16x16 switch architecture design. a) 16x16 Benes, b) the 8x8 tree switch which forms the middle stage in a).

The proposed architecture is based on a hybrid approach combining the Benes and Tree architectures to reduce the switching elements. The Benes architecture offer the best scalability in terms of switching element count [145] and the Tree architecture ensures a minimum of cascaded switching elements.

An $N \times N$ Benes switch consists of one input column of 2x2 switching elements, two $N/2 \times N/2$ middle stages constructed using the Benes architecture and one output of 2x2 switching elements as shown in Figure 6.1a. The substitution of the Benes middle stages with the single-stage tree architecture switch, Figure 6.1b, reduces the number of cascaded SOAs to just three and the total number of switching elements remains comparable to the Benes architecture.

The optimized RNB 16x16 multistage switch architecture shown in Figure 6.1a has a total number 192 SOAs with 176 splitters/combiners and 276 crossings. The total number of mode converters is 968, and the total area is 52.8mm^2 (13.2mm x 4mm).

6.3.1 Miniaturisation

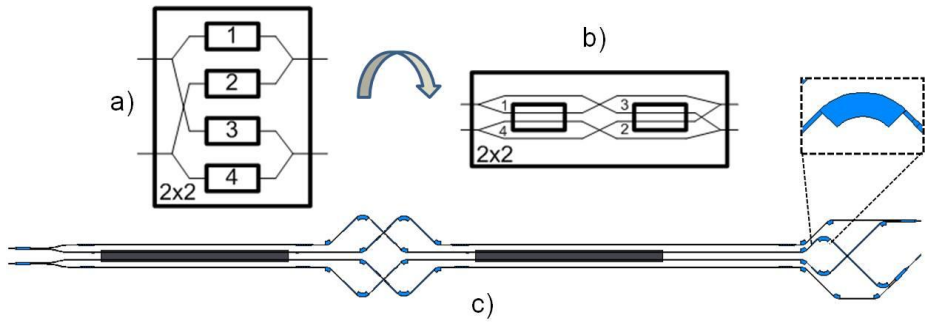


Figure 6.2: 2x2 design and mask layout

To reduce the 16x16 switch dimensions, a compact 2x2 switching element of 0.6mm^2 (2.4mm x 0.25mm) was designed. This 2x2 switching element comes from a tree- broadcast and select architecture, shown in Figure 6.2a. The miniaturization process starts by placing in the same row the four SOA gates, see Figure 6.2b. Only two active regions are used to implement the four SOA gates. This is done by placing in the same active region two different SOA waveguides separated from each other by a distance of 20μm. It is important to mention that the 2x2 circuit remains single stage; this means that only one switching element is needed to enable an optical path. The mask layout of the fabricated 2x2 is shown in Figure 6.2c. To enable further size reduction micro-bend waveguides were designed. These micro-bends exploiting whispering gallery propagation promise a high fabrication tolerance, low polarization conversion below -25dB/90° for sidewall tilts of less than 2° and losses of order 0.2dB/180° [148].

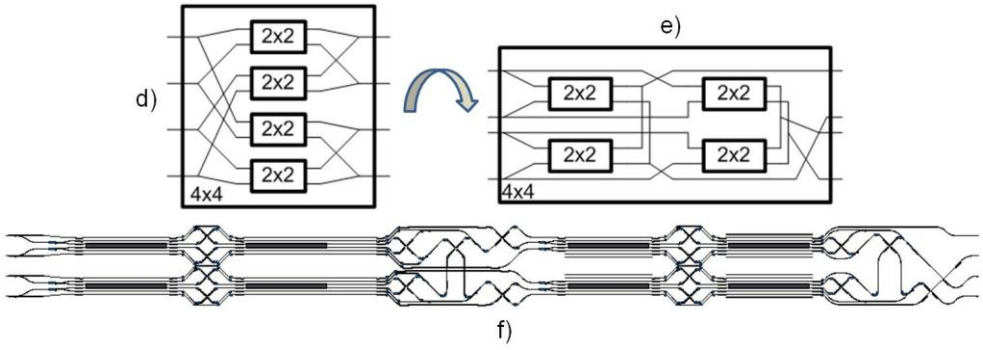


Figure 6.3: 4x4 design and mask layout

The miniaturized 2x2 switches were used as building blocks when designing the 4x4 switches. The total area for the miniaturized 4x4 switch is 2.65mm^2 (5.3mm x 0.5mm). A similar approach is followed to miniaturize this 4x4 switch. The miniaturized architecture is a broadcast and select (BS) 4x4 tree architecture as shown in Figure 6.3e. The 2x2 switching elements in the BS architecture are arranged in two rows and two columns taking care not to create excessive crossings in the interconnection network. These 4x4 switches form the 8x8 tree architecture switch, shown in Figure 6.1b These 8x8 are interconnected to form the 16x16 hybrid Benes switch.

The complete 16x16 fabricated circuit photograph is shown in Figure 6.4. The mask for the fabricated device is shown on the bottom of Figure 6.4. The switch was fabricated by Dr. Patty Stabile in the Clean Room of the Eindhoven University of Technology (TU/e) using an active-passive integration technology very similar to the one presented in Chapter 4.

6.3.2 Switch loss analysis

A limiting factor to the implementation of large scale integrated switch architectures are the losses coming from the splitter and combiners. A conservative value of 3.5dB is estimated for the splitter and combiner loss. The required estimated gain per SOA stage is around 12 dB which seems affordable when using QWs as I already did in previous chapters. This analysis however does not include the gain and signal degradation owing to ASE and distortion. But as it was already shown in previous chapters these impairments can be assessed by operating the device at relative low gain regimes together with new phase modulation formats.

Table 6.1: Splitting/combining loss at each stage for the proposed 16x16 switch.

Switch size	**Number of splitters/combiners per path**	**Splitting/Combining loss per stage, dB**			**Gain Required per SOA stage, dB**
		1st	**2nd**	**3rd**	
16x16	10	7	21	7	35/3 ~ 12dB

The photograph and the connection layout of the complete device are shown in Figure 6.4. The device has been wire bonded and placed in a water cooled mount. The test bed setup is being modified to enable testing of large scale photonic integrated devices.

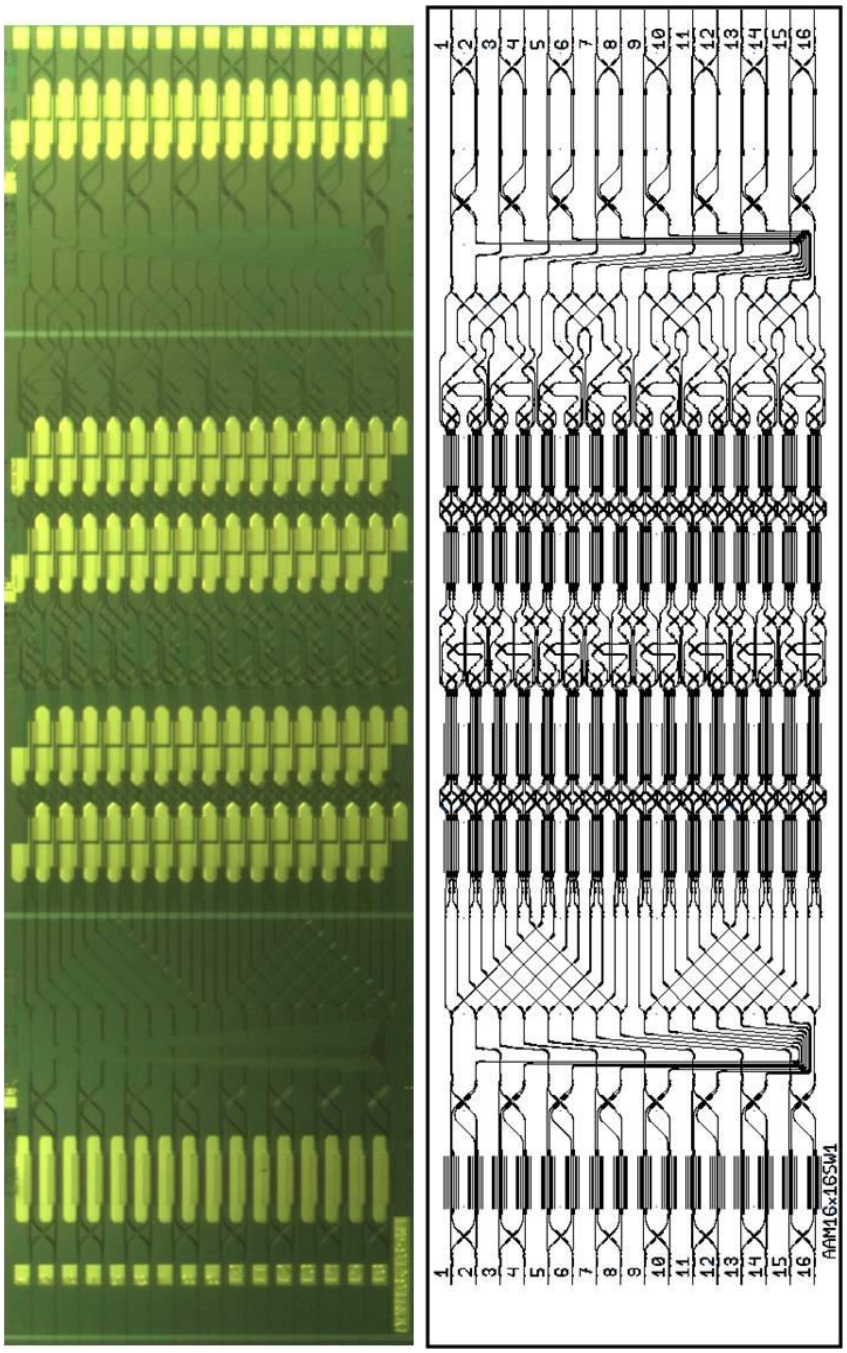


Figure 6.4:16x16 complete circuit. Top) Picture of the fabricated device, bottom) Mask layout

7 Summary of this dissertation and Outlook

In this dissertation, I exploited advanced materials, quantum wells and quantum dots with innovative designs to fabricate and assess state-of-the-art photonic integrated SOA-based switching circuits. The knowledge acquired from these devices was linked with good understanding and concepts of ultrafast optical communications networks to design and experimentally assess a monolithic interconnect operating at ultrahigh line rates up to 320Gbps, for a total potential and predicted data capacity of 1280Gbps. The tested device represents one of the most complex multistage InP PICs reported with up to four SOA-stages. This dissertation proved that photonic integrated SOA-based optoelectronic switches can be scalable in either connectivity or data capacity and are poised to become a key technology for very high-capacity applications.

The first demonstrations using quantum dot (QD)-like material to develop scalable and compact switching matrices operating in the 1.55μm telecommunication window were achieved. Minimal path dependent signal degradation, high switching extinction ratio, negligible same-wavelength path-dependent crosstalk and reduced control complexity were characteristics observed in such devices making them highly promising for larger scale active monolithic photonic circuits.

The impact of all-active monolithic cascaded quantum dot semiconductor optical amplifier switching elements has been studied for the first time. The proposed architectures led to a marked reduction in electrical connections and control complexity compared to previously published SOA-based switch arrays. The scaling of such circuits to higher numbers of connections is predicated on the levels of signal degradation at each stage, and the possibility to provide the required interconnection between stages with low crosstalk and good power efficiency. Although the assessed QD devices achieved an excellent performance, it is important to mention some key aspects in which there are room to improve. The devices displayed properties predicted for quantum dot gain media such as high optical saturation threshold. But they where not able to compensate completely their insertion losses in order to achieve net fibre-to-fibre gain. The low gain value may be attributable to several causes which may

be improved by using the proper epitaxy and improved heat dissipation techniques. But the main improvement can be done either by using a different integration (active-passive) approach instead of the all-active one, by using polarization insensitive QDs or by using a mix of the previous options. This is because; in the all-active photonic integrated devices the polarization state is highly prone to strongly rotate even in waveguides that are not electrically biased. And if this feature is added to the fact that the QD material gain is highly sensitive to the polarization state, this results in a low amplification efficiency provided by the SOAs. These improvements were taken into account in the next generation of monolithic switching circuits. They used an active-passive integration approach to avoid signal impairments and losses caused either by a misaligned polarization state of light or excess heating.

For the first time, the bandwidth limitations of scalable SOA-based multistage switches were assessed through experimental studies. The first active-passive monolithically integrated multistage 4x4 SOA-based switch working at record serial line rates of 160 and 320Gbit/s was demonstrated, representing a step change in the operating speeds for multistage integrated photonics in general, and optoelectronic switching networks in particular. Modest levels of signal degradation per path and dynamic operation with nanosecond timescale re-configurability indicate considerable promise for emerging applications in ultra-broad bandwidth signal routing with energy efficient signal processing. This represents an important milestone in high-bandwidth monolithic circuit integration and offers a highly promising route to large scale monolithic optoelectronic interconnection circuits operating at ultrahigh line rates.

Simulation studies to verify and predict the dependence of data integrity as ultrahigh line-rate and number of stages increases were performed for the first time. Providing insight into the scaling of line rate and connectivity for larger scale integrated switching circuits. An excellent agreement with the experimental data was achieved. This study helped to understand the role of distortion and noise when routing ultrahigh line-rates. Predicted ultrahigh capacity operation up to 640Gbps make monolithic multistage SOA-based switching circuits very promising for high capacity interconnection networks. Other modulation formats might even allow higher scalability and line rate transmission above 640Gbps.

To achieve a higher port count a large scale photonic integrated switching circuit connecting 16 inputs to 16 outputs has been designed and fabricated. All the mentioned achievements were result of the efforts made to push the technology state-of-the-art to achieve hardware efficient and high-capacity

optical interconnects.

7.1 Outlook

The PhD project objectives were:

1. Exploit the state of the art in epitaxial technology and processing techniques to realize high performance space switches for high capacity signal routing.
2. Low signal degradation, even at aggregate throughputs up to Terabit/second.
3. Loss-less operation to ensure applications in a broad range of environments.

The first two objectives were successfully completed, as state of the art quantum dots and mature processing techniques as the one present in Jeppix platform were used to demonstrate world record devices. The first multistage quantum dot switch and the first ultrahigh capacity multistage switch were demonstrated and 640Gbps per path predicted and/or expected.

The last objective of the PhD. Project has still to be completed. But the know-how acquired in this thesis promises this can be assess in next generation chips. For example, the test bed data obtained throughout this PhD work has contributed, to give possible solutions to the main unknowns when building a lossless multistage switching device e.g. the use of active passive integration to reduce interconnection waveguide losses. To achieve a lossless performance it is recommended to implement SOA-based switches with interconnection waveguides with low loss. By doing this the energy consumption goes down because the SOA doesn't need high gain levels to compensate the overall losses. This together with the use of QD material gain with low values of noise figure will improve the necessary power map in this chips and a better performance at low current levels. It would be interesting to test the next generation chip (16x16) and draw further conclusions on capacity, scaling and lossless operation.

7.1.1 Roadmap toward high capacity large scale integrated SOA switches

There is much further work to be done before the realisation of a practical size commercial SOA-based switch. The short term goal to achieve is to implement and optimize 16x16 switches e.g. the one presented in chapter 6 of this thesis. The long term, obviously, is the implementation of integrated switches of larger port count than a 16x16 for example a 64x64. To do this

extensive research has to be done in new switch architectures that will help reducing the number of switching elements and cascades. The development of photonic integrated elements with reduced loss and able to maintain the light polarization state are also needed. Finally the electronic control and electronic processing (regeneration, retiming, buffering, etc) has to be developed further for these large scale photonic integrated switches. For example in these architectures is important to monitor the switch status and provide just the necessary bias to avoid signal degradation caused by noise or gain saturation.

7.1.2 Concluding Remarks

The results of this research therefore opened a route towards the implementation of ultrahigh capacity and energy efficient devices using scalable monolithic SOA based switches. Such scalable, power efficient and broadband switching technology is expected to be of high relevance in reducing the capacity-energy bottleneck in future interconnection applications.

A. OTD-Multiplexing and Demultiplexing

This appendix explains the Optical Time Division Multiplexing work performed for chapter 4.

An important method for transmitting and receiving ultra-high-speed signals (regardless of the modulation format) is seen in the OTDM (Optical Time Division Multiplexing) technique. The OTDM technique performs time-domain multiplexing and demultiplexing of two or more optical data sequences that have the same wavelength. In principle this method does not depend on the processing speeds of electronic devices and can generate ultra-high-speed signals at a single wavelength, the speed depending on the extent of the multiplexing.

Important elemental techniques for OTDM signal generation include ultra-short optical pulse generation, which prevents interference between multiplexed optical data; and optical time division multiplexing, which bit-interleaves individually data-modulated optical signals. For signal reception, OTDM also requires a clock synchronized to the OTDM signal; and optical demultiplexing which extracts multiplexed channels without crosstalk

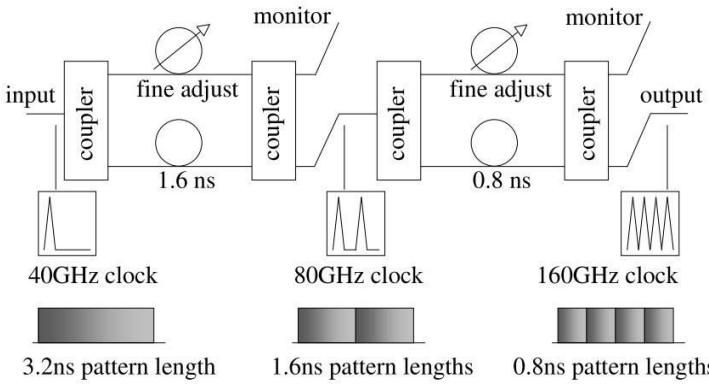
Generating true pseudorandom sequences at ultrahigh bit time rates using bit interleaved sequences of the same sequence is facilitated by the correct choice of delays when combining the sequences. In this work, an electrical binary sequence length of 2^7-1 is generated at 40Gbps with a pulse pattern generator.

The clock rate is quadrupled to 160Gbps using two serial Mach-Zehnder fiber interferometers -a commercially supplied optical clock multiplier from Pritel. In one arm of each Mach-Zehnder interferometer there is a fine adjust delay for bit synchronisation and power equalisation. The second arm includes a half pattern length delay line. This careful choice of delay results in the generation of 2^7-1 patterns at twice the repetition frequency. The operation is repeated to transform the 80Gbps 2^7-1 PRBS to a sequence at 160Gbps with the appropriate delay in the second Mach Zehnder interferometer stage. For the bit at time interval *t*, the pseudo-random bit sequence at the doubled line rate may be derived as follows:

$$PRBS_{80Gb/s}\left({}^{1}/_{2}\ t\right) = PRBS_{40Gb/s}(t_{odd}) + PRBS_{40Gb/s}\left(t_{even} + {}^{1}/_{2}\ 2^{7}\right)$$

The operation is repeated to transform the 80Gbps 2^7-1 PRBS to a sequence at 160Gbps with half the delay in the second Mach Zehnder interferometer stage.

The specific experimental arrangement used is shown in the figure below. Polarisation maintaining components are used throughout the interleaver.



Electroabsorpion demultiplexing: The data clock is applied in electrical form to the modulator to optically gate the desired channel. The phase delay between the received optical input and the applied electrical input determines which demultiplexed tributary is selected for subsequent error rate analysis.

PPLN demultiplexing: Exploiting the sum-frequency generation non- linear process of both coupled signals (clock and OTDM data) into the PPLN and by tuning an optical delay in the clock signal path, a particular channel is selected [116].

B. SOA "Microwave" Frequency Response

These following appendixes address the Microwave response of semiconductor optical amplifiers. The result of this study is used in chapter 5 to propose a fitting function to the frequency response obtain with VPI TLM model.

When an optical signal is launched into the SOA, its amplitude and phase change because of the gain provided by the SOA and the associated changes in the refractive index. To describe this amplification process, I adopt the model developed by Agrawal et al. and write the signal's electric field in the form:

$$E(r,t) = Re\left[\hat{x}\, F(x,y)\, A(z,t)\, e^{i(\beta_0 z - \omega_0 t)}\right] \quad (1)$$

Where $\hat{x}$ is the polarization unit vector, $F(x,y)$ is the mode distribution, $A(z,t)$ is the complex amplitude of the signal, ω_0 is its carrier frequency and $\beta_0 = \bar{n}\omega_0/c$ is the propagation constant of the optical mode with the effective index $\bar{n}$.

The signal amplitude evolves inside the SOA as:

$$\frac{\partial A}{\partial z} + \frac{1}{v_g}\frac{\partial A}{\partial t} = \frac{g}{2}\,(1 - i\,\alpha)\,A \quad (2)$$

Where v_g is the group velocity and α is the linewidth enhancement factor responsible for changes in the mode index with changes in the carrier density N_d that satisfies a rate equation of the form, the three equations represent the same evolution but they are written for clarity in the relations.

$$\frac{\partial N_d}{\partial t} = \frac{I}{q\,V} - \frac{N_d}{\tau_{sp}} - \frac{\Gamma\, a\,(N_d - N_{tr})}{\hbar\,\omega_0}\,|A|^2 \quad (3a)$$

$$\frac{\partial N_d}{\partial t} = \frac{I}{q\,V} - \frac{N_d}{\tau_{sp}} - (N_d - N_{tr})\,\frac{P_d}{E_{sat}} \quad (3b)$$

$$\frac{\partial N_d}{\partial t} = \frac{I}{q\,V} - \frac{N_d}{\tau_{sp}} - a\,v_g\,(N_d - N_{tr})\,S_d \quad (3c)$$

Where V is the active volume; S_d, P_d are the photon density and instantaneous power, respectively; $E_{sat} = \frac{Area\,\hbar\,\omega_0}{a\,\Gamma}$ is the saturation energy and τ_{sp} is the carrier lifetime. It is important to remember that τ_{sp} depends on N_d. If I include both the radiative and Nonradiative recombination processes, this dependence takes the form

$$\frac{1}{\tau_{sp}} = \left(A_{nr} + B_{sp}\, N_d + C_a\, N_d^2\right) \tag{4}$$

Where A_{nr} is the intrinsic nonradiative recombination rate, B_{sp} is the spontaneous recombination coefficient and C_a represents the Auger recombination coefficient.

The equation for the propagation of the photon density $S_d = S[z,t]$ and the propagation of optical power $P_d = P[z,t]$ is:

$$\frac{\partial S_d}{\partial z} = (\Gamma\, a\, (N_d - N_{tr}) - \alpha_i)\, S_d \tag{5a}$$

$$\frac{\partial P_d}{\partial z} = (\Gamma\, a\, (N_d - N_{tr}) - \alpha_i)\, P_d \tag{5b}$$

Here, z is the spatial coordinate along the amplifier and *t* is the local time, measured in a coordinate system moving with the group velocity v_g. Furthermore a is the differential gain, Γ is the confinement factor, N_{tr} is the carrier density at transparency, I is the injected current, V is the active region volume, τ_{sp} is the carrier lifetime and α_i is the total internal loss, which is mainly due to waveguide scattering and free-carrier absorption. The photon density S is related to the instantaneous power P via

$$P = \frac{h\, c\, v_g\, Area}{\lambda\, \Gamma}\, S \tag{6}$$

Where $Area$ is the waveguide geometric area and λ is the signal wavelength. The modal gain in the equations above is represented by the linear approximation for the dependence of the gain on the carrier density N_d.

$$g = g[z,t] = \Gamma\, a\, (N_d - N_{tr}) \tag{7}$$

Assumptions:

These equations neglect ultrafast gain nonlinearities like carrier heating and spectral hole burning for frequencies above Terahertz. The inclusion of these effects leads to quantitative changes but they do not modify the qualitative conclusion of this study.

The influence of spontaneous emission (SE) on the saturation of the gain has been also neglected. For long amplifiers with large gain, the level of SE can be high enough to saturate the amplifier, but this case is not treated here.

The implicit assumption is therefore that the injected power is large enough to dominate the saturation behaviour.

B.1 SMALL SIGNAL ANALYSIS FOR THE SOA FREQUENCY RESPONSE

This study is dedicated to analyze the SOA gain response to a frequency modulation Ω. The situation considered is illustrated in Fig. 1: a modulated laser beam is input to an SOA and modulates the carrier density which translates into a modulation of the amplifier gain.

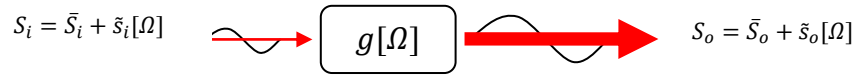


Fig.1 Schematic diagram of configuration for small signal analysis to analyze the SOA gain response to a frequency modulation Ω.

Considering the case where there is a large saturating power in the laser beam and a small modulation superimposed on it. I write the sinusoidal photon density modulation as

$$S_d[z,t] = \bar{S}[z] + \tilde{s}[z]e^{i\Omega t} + \tilde{s}^*[z]e^{-i\Omega t} \tag{8}$$

with $\bar{S}$ and $\tilde{s}[z]$ being the steady-state photon density and the photon density modulation perturbation, respectively. Considering this small-signal modulation, Eq. 8, N takes the form

$$N_d[z,t] = \bar{N}[z] + \tilde{n}[z]e^{i\Omega t} + \tilde{n}^*[z]e^{-i\Omega t} \tag{9}$$

with $\bar{N}[z]$ and $\tilde{n}[z]$ being the steady-state carrier density and the small-signal carrier density modulation perturbation.

For the carrier density steady-state $\bar{N}[z]$ I set the carrier density rate equation (Eq. 3c) time derivative to zero and neglect the time dependent terms resulting after the insertion of the sinusoidal photon density modulation.

$$\bar{N}[z] = \frac{N_{tr}\frac{\bar{S}[z]}{S_{sat}} + \frac{I\,\tau_{sp}}{q\,V}}{\frac{\bar{S}[z]}{S_{sat}} + 1} \tag{10}$$

$$\bar{N}[z] = \frac{\frac{\bar{P}[z]}{E_{sat}}N_{tr} + \frac{I}{q\,V}}{\frac{1}{\tau_{sp}} + \frac{\bar{P}[z]}{E_{sat}}} \tag{10a}$$

Where $\frac{1}{S_{sat}} = a\,v_g\,\tau_{sp}$ is used as the saturation photon density. To get the steady-state $\bar{S}[z]$ and the small signal photon density perturbation along the SOA $\tilde{s}[z]$, the small signal carrier density $\tilde{n}[z]$ is obtained from the carrier density rate equation by neglecting terms but of first order in $\tilde{n}[z]$ and using $P =$

$\frac{h\,c\,v_g\,Area}{\lambda\,\Gamma}\,S$; $E_{sat} = \frac{h\,c\,Area}{a\,\lambda\,\Gamma}$ where the contribution to the lifetime of the stimulated emission by the laser beam is given by: $\frac{1}{\tau_{sat}} = a \cdot v_g \cdot \bar{S}[z] = \frac{\bar{P}[z]}{E_{sat}}$

$$\tilde{n}[z] = -\frac{(\bar{N}[z]-N_{tr})\frac{\tilde{p}[z]}{E_{sat}}}{\frac{1}{\tau_{eff}}+i\Omega} \qquad (11)$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{sp}} + \frac{1}{\tau_{sat}} \qquad (11a)$$

Substituting in Eq. 9 the proposed solutions for $\bar{N}[z]$ and $\tilde{n}[z]$ and inserting this equation in Eq. 5a., the equation for the average photon density along the SOA, $\bar{S}[z]$, and for the small signal photon density perturbation along the SOA, $\tilde{s}[z]$, are obtained after collecting the time independent terms and the time dependent terms, respectively. The behaviour of the steady-state optical power and the small signal propagation is given by

$$\frac{\partial \bar{s}}{\partial z} = (g_{sat} - \alpha_i)\,\bar{S}[z] \qquad (12)$$

$$\frac{\partial \tilde{s}}{\partial z} = (g_{sat} - \alpha_i)\,\tilde{s}[z] - \left(\frac{g_{sat}\,\tilde{s}[z]}{\left(1+i\,\Omega\,\tau_{sp}+\frac{\bar{S}[z]}{S_{sat}}\right)}\,\frac{\bar{S}[z]}{S_{sat}}\right) \qquad (13)$$

Where $g_{sat} = \frac{g_0}{1+\frac{\bar{S}[z]}{S_{sat}}}$; $g_0 = a\,\Gamma\left(\frac{I}{q\,V}\tau_{sp} - N_{tr}\right)$ are the saturated gain and the small signal unsaturated modal gain, respectively.

For a given position in the amplifier, the solutions of the steady state (10 or 10a) and (12) give values for the carrier concentration and local photon density, and hence the CW material gain. The magnitude of the perturbation to the carrier population is governed by (11), which describes the response of the carriers due to the amplification of the modulated laser, and shows that the response at this position has a high frequency roll- off with a 3-dB angular frequency governed by the local effective lifetime τ_{eff}

$$\Omega_{3-dB} = \frac{\sqrt{3}}{\tau_{eff}} \qquad (14)$$

It might therefore appear that this frequency modulation roll-off would also apply to the gain frequency evolution. However, consideration of (13) shows that the last term, which represents coupling of light from the CW component into the time varying component, acts to compress the gain at low frequencies. At higher frequencies the carrier population cannot follow the light variation and the

compression is removed. This effect tends to extend the bandwidth beyond that determined by the denominator of (11). This high-pass response is explained by getting the magnitude of the perturbation to the material gain which is described by (15) after using $g[\bar{S}] = \frac{\partial \bar{s}}{\partial z}\,\frac{1}{\bar{s}[z]}$; $g[\tilde{s}] = \frac{\partial \tilde{s}}{\partial z}\,\frac{1}{\tilde{s}[z]}$ in (13) and the same relationships used to get (11).

$$g[\tilde{s}] = g[\bar{S}] - \left(\frac{g_{sat}}{\tau_{sat}} \frac{1}{\left(\frac{1}{\tau_{eff}} + i\,\Omega \right)} \right) \tag{15}$$

Evaluating the magnitude of the perturbation to the material gain (16) in the frequency limits (17-18) a high-pass response can be observed as the gain values for higher frequencies are higher than the gain values evaluated at lower frequencies.

$$|g[\tilde{s},\Omega]| = g[\bar{S}] \sqrt{\left(\frac{g_{sat}}{\frac{g[\bar{S}]\,\tau_{sat}}{\Omega}\left(\frac{1}{\tau_{eff}^2} + \Omega^2 \right)} \right)^2 + \left(1 - \frac{g_{sat}}{g[\bar{S}]\,\tau_{eff}\,\tau_{sat}\left(\frac{1}{\tau_{eff}^2} + \Omega^2 \right)} \right)^2} \tag{16}$$

$$|g[\tilde{s},\Omega \to 0]| = g[\bar{S}] - \frac{g_{sat}}{\tau_{sat}\left(\frac{1}{\tau_{eff}} \right)} = g[\bar{S}] - \frac{a\,\Gamma\left(\frac{I}{q\,V}\tau_{sp} - N_{tr} \right)}{\left(1 + \frac{\bar{S}}{S_{sat}} \right)^2} \frac{\bar{S}}{S_{sat}} \tag{17}$$

$$|g[\tilde{s},\Omega \to \infty]| = g[\bar{S}] \tag{18}$$

The low frequency gain-compression magnitude (compressed CW material gain) is governed mainly by the gain saturation. In the high frequency regime the gain magnitude is a fix value which corresponds to the CW material gain. This confirms that the carrier population cannot follow the light variation and the low frequency compression is removed.

The cut-off frequency for this high-pass response (16) is governed by the saturated gain, g_{sat}, which is directly related to the injected bias current. In (19) g_{sat} sets where the low frequency roll-off will appear.

$$\Omega_{3-\mathrm{dB}} = \frac{g_{sat}}{\sqrt{3}\,g[\bar{S}]\,\tau_{sat}\,\tau_{eff}} \sqrt{\frac{8\,g[\bar{S}]\,\tau_{sat}\,\tau_{eff}}{g_{sat}} - 3\left(\frac{g[\bar{S}]\,\tau_{sat}}{g_{sat}} \right)^2 - 4\left(\tau_{eff} \right)^2} \tag{19}$$

The gain difference between a certain higher frequency and a certain lower frequency increases with the bias current. A more extreme difference is expressed as

$$|g[\tilde{s},\Omega \to \infty]| - |g[\tilde{s},\Omega \to 0]| = \frac{a\,\Gamma\left(\frac{I}{q\,V}\tau_{sp} - N_{tr} \right)}{\left(1 + \frac{\bar{S}}{S_{sat}} \right)^2} \frac{\bar{S}}{S_{sat}} \tag{20}$$

It is evident that as the injected bias current increases the numerator will increase and this will lead to a more steep frequency response of the SOA.

A simple analytic expression has been derived for the small-signal-modulated gain evolution in a travelling wave SOA. The expression derived describes the physical effects in operation and their relative contributions to gain frequency response. It is found that the modulation bandwidth of the carrier population in the amplifier does not solely determine the bandwidth of the SOA frequency response. This is due to the frequency dependence of the longitudinal propagation of the signal.

The normalized frequency response presented in Equation 1 in chapter 5 was derived from Equation 15 in this appendix.

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List of Publications

Most Significant paper:

Title: *160 Gbit/s line-rate data routing through monolithic multi-stage optical switch circuit.*

Authors: Albores-Mejia, A.; Gomez-Agis, F.; Zhang, S.; Dorren, H.J.S.; Leijtens, X.J.M.; de Vries, T.; Oei, Y.S.; Heck, M.J.R.; Notzel, R.; Robbins, D.J.; Smit, M.K.; Williams, K.A.

Publication: *Electronics Letters* , vol.46, no.17, pp.1209 -1211, August 19, 2010.

In this work, a photonic integrated multistage optical switch network operating at ultra-high line rates is presented for the first time. The step change in line rate to 160Gbps showed that scalable integrated optoelectronic circuits can indeed operate at speeds inaccessible to electronics. Before this paper it was unknown whether multistage photonic integrated circuits using SOA gates could be scalable either in data capacity or connectivity within very high speed applications.

Journals

1. Albores-Mejia, A.; Williams, K.A.; de Vries, T.; Smalbrugge, E.; Oei, Y.S.; Smit, M.K.; Notzel, R., *"Integrated 2 X 2 quantum dot optical crossbar switch in 1.55 μm wavelength range,"* Electronics Letters , vol.45, no.6, pp.313-314, March 12 2009.

2. Albores-Mejia, A.; Williams, K.A.; Gomez-Agis, F.; Zhang, S.; Dorren, H.J.S.; Leijtens, X.J.M.; de Vries, T.; Oei, Y.S.; Heck, M.J.R.; Augustin, L.M.; Notzel, R.; Robbins, D.J.; Smit, M.K.; , *"160Gb/s Serial Line Rates in a Monolithic Optoelectronic Multistage Interconnection Network,"* High Performance Interconnects, 2009. HOTI 2009. 17th IEEE Symposium on , vol., no., pp.157-162, 25-27 Aug. 2009

3. Albores-Mejia, A.; Gomez-Agis, F.; Zhang, S.; Dorren, H.J.S.; Leijtens, X.J.M.; de Vries, T.; Oei, Y.S.; Heck, M.J.R.; Notzel, R.; Robbins, D.J.; Smit, M.K.; Williams, K.A.; , *"160 Gbit/s line-rate data routing through monolithic multi-stage optical switch circuit,"* Electronics Letters , vol.46, no.17, pp.1209 -1211, August 19, 2010. (**Featured Article**)

4. Albores-Mejia, A.; Gomez-Agis, F.; Dorren, H.J.S.; Leijtens, X.J.M.; de Vries, T.; Yok-Siang Oei; Heck, M.J.R.; Notzel, R.; Robbins, D.J.; Smit, M.K.; Williams, K.A.; , *"Monolithic Multistage Optoelectronic Switch Circuit Routing 160Gb/s Line-Rate Data,"* Lightwave Technology, Journal of , vol.28, no.20, pp.2984-2992, Oct.15, 2010.

5. Gomez Agis, F., Calabretta, N., Albores-Meija, A., Dorren, H.J.S. *"Clock-distribution with instantaneous synchronisation for 160 Gbit/s optical time-domain multiplexed packet transmission"*. Optics Letters, 35(19), 3255-3257, 2010.

6. Gomez Agis, F., Okonkwo, C.M., Albores-Mejia, A., Tangdiongga, E., Dorren, H.J.S. (2010). *"320-to-10 Gbit/s all-optical demultiplexing using sum-frequency generation in PPLN waveguide"*. Electronics Letters, 46(14), 1008-1009, 2010.

7. Calabretta, N.; Stabile, R.; Albores-Mejia, A.; Williams, K.A.; Dorren H.J.S.;, *"Scalable InP integrated wavelength selector based on binary search"*. Optics Letters, July, 2011

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Conferences

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2. Albores-Mejia, A.; Williams, K.A.; de Vries, T.; Smalbrugge, E.; Oei, Y.S.; Smit, M.K.; Anantathanasarn, S.; Notzel, R.; , *"Scalable quantum dot*

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4. Albores-Mejia, A.; Williams, K.A.; Gomez-Agis, F.; Zhang, S.; Dorren, H.J.S.; Leijtens, X.J.M.; de Vries, T.; Oei, Y.S.; Heck, M.J.R.; Augustin, L.M.; Notzel, R.; Robbins, D.J.; Smit, M.K.; , *"Monolithic multistage optical switch operating at 160 Gb/s line rate,"* Lasers and Electro-Optics 2009 and the European Quantum Electronics Conference. CLEO Europe - EQEC 2009. European Conference on , vol., no., pp.1-1, 14-19 June 2009. **(post-deadline)**

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Aarón

Curriculum Vitae

Aarón Albores-Mejía was born in Puebla, Puebla, Mexico, in 1980. He received the B.Sc. degree (with honours) in Electronics and Telecommunications Engineering from Universidad de las Americas-Puebla (UDLA-P), Puebla, Mexico, in 2003, and the M.Sc. degree in Electronics and Telecommunications from the Ensenada Center for Scientific Research and Higher Education (CICESE), Baja California, Mexico, in 2007. Since 2007 he has been a Ph.D. researcher in the Electro-optical Communications group at the department of Electrical Engineering at Eindhoven University of Technology/COBRA Research Institute in the Netherlands. His research interests include the design, realisation and demonstration of high speed integrated photonic switching circuits for on- and off-chip communications systems. He has been two times recipient of the Mexican National Science and Technology Council Scholarship.

During his Ph.D. studies, he has authored and co-authored more than 20 publications in international journals and conferences. He is also a peer reviewer for IEEE Journal of Lightwave Technology (JLT) and IEEE Transactions on Parallel and Distributed Systems (TPDS).

His work has been used in invited presentations by others researchers at high-impact conferences including the America's premiere Optical Fiber Communication Conference, OFC. The quality of his research has been recognised by an invited paper at Europe's premiere Optical Communication Conference ECOC'2010 and the featured interview of one of his Electronics Letters.