Design methods for 60GHz beamformers in CMOS

Design Methods for 60GHz Beamformers in CMOS

Yikun Yu

Cover designed by Nancy

Front cover:
”Beam forming”

Back cover:
Summary and Biography

Design Methods for 60GHz Beamformers in CMOS

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Eindhoven, op gezag van de
Rector Magnificus, prof.dr.ir. C.J. van Duijn, voor een
commissie aangewezen door het College voor
Promoties in het openbaar te verdedigen
op maandag 22 november 2010 om 16.00 uur

door

Yikun Yu

geboren te Fujian, China

Dit proefschrift is goedgekeurd door de promotoren:

prof.dr.ir. P.G.M. Baltus
en
prof.dr.ir. A.H.M. van Roermund

Yikun Yu

Design Methods for 60GHz Beamformers in CMOS
Proefschrift Eindhoven University of Technology, 2010
A catalogue record is available from the Eindhoven University of Technology Library
ISBN: 978-90-386-2367-2
NUR 959
Key words: 60GHz / mm-wave / phased array / receiver / transmitter / beam forming / RF phase shifting / phase shifter / CMOS

To my parents, and
my wife Nancy

Samenstelling promotiecommissie:

prof.dr.ir. A.C.P.M. Backx	TU Eindhoven
prof.dr.ir. A.H.M. van Roermund	TU Eindhoven
prof.dr.ir. P.G.M. Baltus	TU Eindhoven
prof.dr.ir. B. Nauta	Univ. of Twente
prof.dr. J.R. Long	TU Delft
prof.dr.ir. J.W.M. Bergmans	TU Eindhoven
prof.dr.ir. A.B. Smolders	TU Eindhoven
dr.ir. P.F.M. Smulders	TU Eindhoven

Contents

1

Introduction

1.1 Background

There are a lot of wireless systems in the world, such as GSM, UMTS W-CDMA, LTE, WiMax (802.16), WiFi (802.11a/b/g/n), Zigbee, Bluetooth and Ultra-wide Band (UWB). These wireless systems are widely used in Wide Area Networks (WAN), Metropolitan Area Networks (MAN), Local Area Networks (LAN) and Personal Area Networks (PAN). As shown in Figure 1.1 [1], their data rates vary from about tens of kbps (e.g. GSM GPRS, ZigBee) to hundreds of Mbps (e.g. WiFi 802.11.n and UWB); their communication distances range from a few meters (e.g. Bluetooth and UWB) to several kilometers (e.g. GSM, UMTS W-CDMA and WiMax).

Recently there are plenty of multimedia applications calling for wireless transmission at several Gbps over short distances. Examples are wireless Giga-bit Ethernet (1.25Gbps), synchronization and high-speed download (as fast as possible), and wireless streaming of high definition video (2-20Gbps). These will require transferring large amounts of data (e.g. high quality video signals) between high-definition (HD) video cameras, game consoles (e.g. Wii, PS3), HD set-top boxes, smart phones (e.g. iphone), blue-ray high-definition (BD/HD) DVD players, personal com-

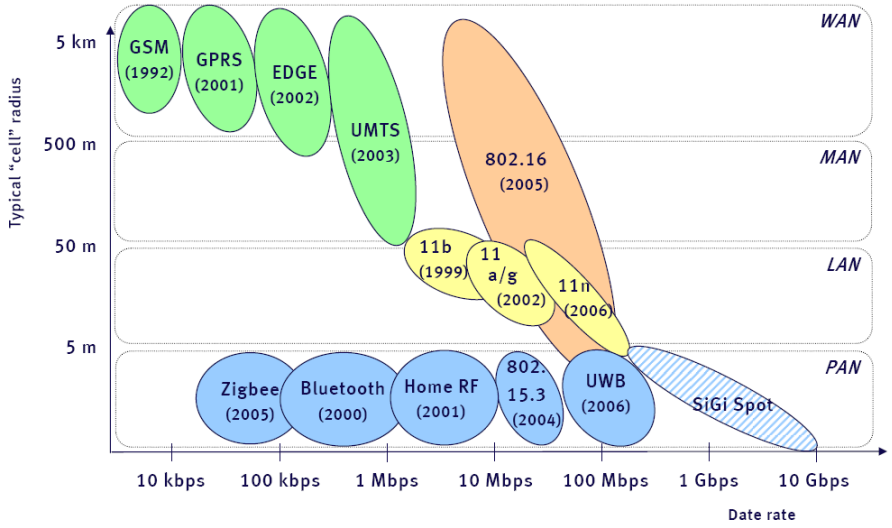


Figure 1.1: Overviews of existing wireless systems and the motivation of this work (SiGi-Spot) [1]

Figure 1.2: Emerging multi-Gbps communication for multimedia applications.

puters, digital video recorders, high-definition televisions (HDTV) and so forth (Fig. 1.2).

These multi-Gbps data rates cannot be accommodated in the traditional frequency bands below, let us say, 10GHz, without significant service degradation. For example, Bluetooth only offers data rates of 1-3Mbps over 100 meters [2]; WiFi provides 11-300Mbps and is optimized for a large distance of 30-50 meters [3]. UWB may be a potential candidate for the short-range high-speed wireless communication, providing data rates of approximately 200Mbps over 10 meters [2], thanks to the large signal bandwidth of at least 500MHz. However, a UWB system has several disadvantages. First, UWB uses the frequency band from 3.1GHz to 10.6GHz and suffers strong interferences from WiFi. Second, UWB has only a limited transmit power of -41.3dBm/MHz, which severely limits the signal-to-noise ratio (SNR) at the input of the receiver.

Fortunately, sufficient spectral space can be found at millimeter-wave frequencies, e.g. around 60GHz where around 5GHz of spectral space has been allocated worldwide for unlicensed use. The transmitted output power can be up to 40dBm and compensate the free-space path loss. The 60GHz band offers exciting opportunities for applications such as high-speed short-range wireless personal area network (WPAN) and real time video streaming at rates of several Gbps [4].

1.2 State of the Art

Traditionally mm-wave radio frequency (RF) technology has been the domain of expensive chip technologies based on III-V compound materials such as GaAs and InP [5]. Recently considerable RF performance at mm-wave frequencies has been achieved using low-cost silicon-based SiGe [6] and CMOS [7–10] technologies.

A major issue in designing a high data rate 60GHz radio is the limited link budget over indoor distances, especially for the non-line-of-sight (NLOS) situations, due to the high path loss during radio propagation, high noise figure of the receiver and low output power of the transmitter [11,12]. On the other hand, thanks to the relatively small size of 60GHz antennas, the phased array technique (Fig. 1.3) is an attractive solution to com-

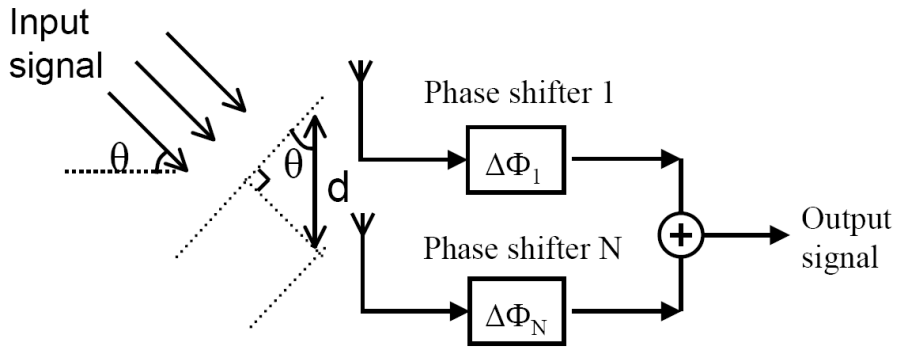


Figure 1.3: Principle of a phased array receiver.

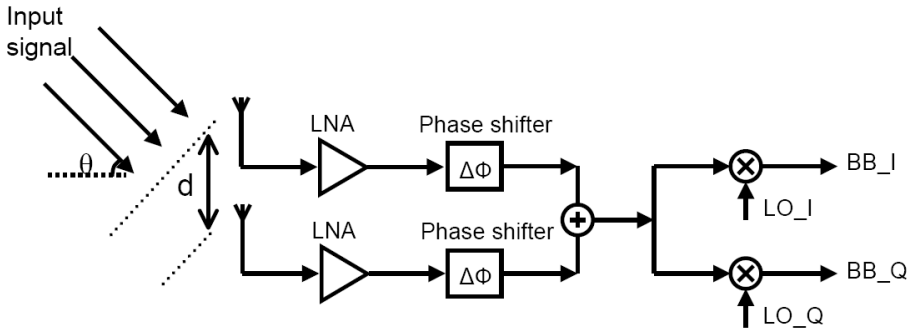


Figure 1.4: A phased array receiver using RF phase shifting.

pensate the path loss and alleviate the requirements of the RF transceiver front-ends. In addition to providing electronically controlled beam forming, phased arrays offer a larger effective isotropic radiated power (EIRP) in the transmitter, a higher signal-to-noise ratio (SNR) in the receiver, as well as interference suppression [13–18]. This leads to higher system capacity and larger range, which is highly beneficial to a 60GHz wireless system.

Phase shifters are essential components in a phased array for adjusting the phase of each antenna path and steering the beam [19, 20]. Phase shifting can be implemented in different parts of a transceiver, such as at RF, IF, LO or digital baseband.

- Placing the phase shifters in the LO- [21–23] or IF-path [24–27] requires separate frequency converters for each of the antennas, while each frequency converter consists of separate mixers, LO buffers and LO distribution. The LO- or IF-path phase shifting allows for easier and less critical implementation of phase shifters, but requires multiplication of many other circuit blocks.

- By placing the phase shifters in the RF path of a receiver/transmitter, the signals from/to each of the antennas are combined/split at RF, which shares the frequency converter among the multiple antennas and results in simple system architecture (Fig. 1.4) [28–31]. However, programmable phase shifters at mm-wave frequencies (60GHz) typically have significant losses; and it is difficult to implement a low-noise amplifier (LNA) or power amplifier (PA) with very high gain in order to compensate the losses of RF phase shifters.

1.3 Aim of the Thesis

The primary goal of this thesis is to investigate new concepts and design techniques that can be used for integrated 60GHz phased-array systems. The implementation of low-loss high-resolution RF phase shifters for an low-cost low-power RF phase shifting architecture is of particularly interest. In both the receiver and transmitter, the following aspects are taken into account:

- Analysis of 60GHz system specifications, and the requirements upon phased arrays and phase shifters.

- Selection among various phased-array architectures for low-cost and low-power considerations.

- Evaluation of the prior-art RF phase shifters and their limitations.

- Design and implementation of new concepts in RF phase shifters in order to improve their performance (e.g. operating frequency, phase accuracy, insertion loss, chip area and power consumption).

- Integration of the RF phase shifters with other key building blocks in the transceiver (e.g. low noise amplifier and power amplifier), in order to evaluate RF beamforming.
- Investigation of the integration of an RF IC and an antenna e.g. in a printed circuit-board (PCB) technology, as an important step towards a full 60GHz system e.g. in a package (SiP).

1.4 Scope of the Thesis

Some limitations on the scope of the thesis are explained below:

- 60GHz. Integrated circuits at 60GHz are implemented. This is because of the worldwide interest in high-speed short-range WPAN and real-time video streaming at rates of several Gbps. It is worth pointing out that the concepts can also be applied to other mm-wave frequencies (e.g. 24, 77, or 94GHz).
- Phased-array techniques with focus on RF phase shifters. This work focuses on phased-array techniques, especially the design of RF phase shifters. This is because phased-array techniques can compensate the path loss and alleviate the requirements of 60GHz RF transceivers; phase shifters are essential components in a phased array for adjusting the phase of each antenna path and steering the beam. The RF phase shifters are further integrated with other key building blocks (i.e. LNA and PA) for evaluation purposes.
- CMOS technology. CMOS technology is selected because it is the lowest-cost option in volume production, and offers high level of integration with RF, analog and digital circuits. In this work, a 65nm CMOS technology is used, whereas the concepts and design techniques can be implemented in other technologies as well.
- General purpose. This work does not aim for a specific target application (e.g. WPAN or Wireless HD). Therefore, the proposed concepts and designs are general purpose, and are not optimized for e.g. a specific signal bandwidth or a specific modulation scheme.

1.5 Original Contributions

The contributions of the thesis are listed below:

- At system level, analyze various applications at mm-wave frequencies e.g. multi-Gbps data communication at 60GHz; analyze the system requirements including digital modulation scheme (e.g. FSK or QPSK), multiple-access scheme (e.g. TDMA) and phased array techniques; analyze the link budget of a 60GHz WPAN; compare different phase array architectures that use e.g. RF-, LO- or IF-path phase shifting.

- At circuit level, analyze the circuit requirements of the receiver and transmitter such as gain, bandwidth, linearity, noise figure of the receiver and output power of the transmitter; derive the step-size requirements (e.g. 22.5^{o}) of a phase shifter from phased-array system simulation of the constellation spreadings of the output signal, as well as of the radiation patterns of a phased array; analyze several types of conventional RF phase shifters and their limitations.

- Design and implementation of a 60GHz digitally-controlled *passive* phase shifter. It consists of a differential transmission loaded with a differential MOS varactor at each side. It achieves low cost, simple design, low insertion loss, a phase-shift step of 22.5^{o} and a phase shift range of 360^{o} at 60GHz.

- Design and implementation of a 60GHz digitally-controlled *active* phase shifter. As compared to *passive* phase shifters, the *active* phase shifter has lower insertion loss (or even gain) and lower variation in loss.

- Design of a 60GHz two-path *receiver* in which each path consists of a low-noise amplifier (LNA), an *active* phase shifter and part of a combiner; design of a 60GHz one-path *transmitter* that consists of an *active* phase shifter and a power amplifier (PA). It is straightforward to scale these designs to more antenna paths. They demonstrate that RF phase shifting is an appealing technique for low-cost low-power 60GHz phased array systems.

- Investigation of the integration of a 60GHz amplifier and an antenna in a printed circuit-board (PCB) package. It demonstrate that an 60GHz amplifier can be integrated with an antenna with good performance.

1.6 Outline of the Thesis

The outline of this thesis is briefly explained below:

Chapter 2 presents an overview of various applications at mm-wave frequencies. System considerations of mm-wave receivers and transmitters are also discussed, followed by the selection of semiconductor technology.

Chapter 3 discusses the motivation for phased array technique, and give an introduction to the operation principles and benefits of phased arrays. The system requirements of phase shifters are discussed. Different phased array architectures are compared.

In Chapter 4, several types of conventional RF phase shifters and their limitations are reviewed.

In Chapter 5, a 60GHz 4-bit *passive* phase shifter is designed in a 65nm CMOS technology, and the measurement results are presented.

Chapter 6 presents the design and measurement results of a 60GHz 4-bit *active* phase shifter and its integration with a low noise amplifier and a combiner for a phased array receiver.

Chapter 7 presents the design and measurement results of a 60GHz 4-bit *active* phase shifter integrated with a power amplifier for a phased array transmitter.

In Chapter 8, the integration of a 60GHz CMOS amplifier and an antenna in a printed circuit-board (PCB) package is investigated.

Finally, conclusions and recommendations for future research are presented in Chapter 9.

2

Millimeter-Wave Wireless Communication

Millimeter-wave frequencies often refer to the frequency range from 30GHz to 300GHz, the wavelength of which is between 10mm to 1mm. There are several motivations for wanting to use mm-wave frequencies in radio links:

- The radio spectrum at mm-wave frequencies is still rather undeveloped, and more bandwidth is available at these frequencies.
- Because of higher attenuation in free space and through walls at mm frequencies, the same frequency can be reused at shorter distances distances.
- The inherent security and privacy is better at mm-wave frequencies because of the limited range and the relatively narrow beam widths that can be achieved.
- The spatial resolution is better at mm-wave frequencies since the small wavelength allows modest size antennas to have a small beam width.
- The physical size of antennas at mm-wave frequencies becomes so small that it becomes practical to build complex antenna arrays and/or further integrate them on chip or PCB.

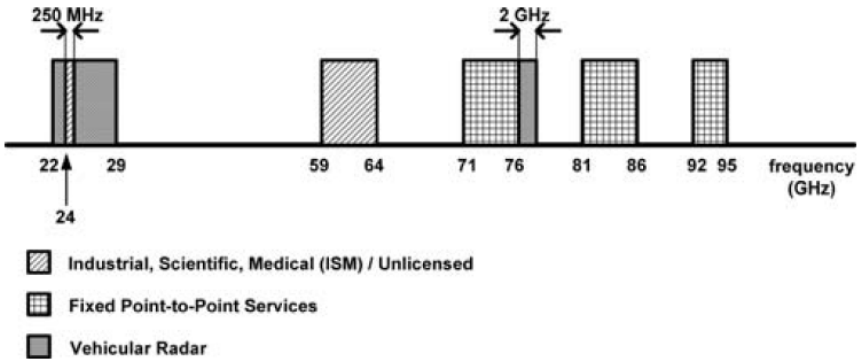


Figure 2.1: Millimeter-wave band allocation in the United States [11].

Figure 2.1 shows the mm-wave band allocation in the United States [11]. There is 5GHz bandwidth available at the 60GHz band (59-64GHz) for Industrial, Scientific and Medical (ISM) unlicensed applications. The 24GHz band (22-29GHz) band and 77GHz band (76-77GHz) are currently assigned to automotive radar. Fixed point-to-point communication links can use 71-76GHz, 81-86GHz and 92-96GHz that need a license in the USA from The Federal Communications Commission (FCC). The mm-wave frequenciy bands offer many new products and services, for example:

- The large bandwidth at 60GHz can provide unlicensed short-range high-speed links for WPAN (802.15.3c) and wireless high definition video streaming (Wireless HD). Data rates can be several Gbps.
- The 77GHz band is suitable for automotive long-range (100m) autonomous cruise-control (ACC) radar. The high carrier frequency allows modest-size antennas to have a small beam width and therefore a better angular resolution.
- The 24GHz band can be used in automotive short-range radar, since the large bandwidth at 24GHz offers sufficient small distance resolution (5cm).
- The large bandwidth at 71-76GHz, 81-86GHz and 92-96GHz can provide licensed high-speed links with data throughput up to 10Gbps.

- The natural thermal emission of objects in the 35GHz and 94GHz bands allows passive imaging to construct an image.

This chapter is organized as follows. The unique mm-wave applications are discussed in Section 2.1. Section 2.2 presents system considerations of mm-wave receiver and transmitter front-ends. The technology choices to implement mm-wave systems are discussed in Section 2.3. Part of this chapter is published in [12].

2.1 Millimeter-Wave Communication

2.1.1 Multi-Gbps Data Communication

In principle, a high data rate can be achieved by a combination of signal bandwidth and dynamic range. The limit for the data rate over a single-input and single-output (SISO) link is set by the capacity (C) of the link and is a function of the bandwidth (BW) and the signal-to-noise ratio (SNR) [32]:

$$C = BW \times log_2(1 + SNR) \tag{2.1}$$

Therefore, a high data rate can be achieved with a low bandwidth if the SNR is high. However, a high SNR requires either a short distance between transmitter and receiver, or a high transmit power, or high gain antennas. This is described in the Friis Transmission equation:

$$P_{sig} = P_t \times G_r \times G_t \times (\frac{\lambda}{4\pi \times d})^{\alpha} \tag{2.2}$$

In this equation, P_{sig} is the received signal power, P_t is the transmitted signal power, G_r is the gain of the receiver antenna, G_t is the gain of the transmitter antenna, λ is the wavelength, and d is the distance between the transmit and receive antennas. The original Friis transmission equation is valid for free space environments with a value of 2 for the parameter α. It is also used to approximate the average received power in multi-path environments inside buildings, in which case the parameter a varies from 1.8 to 5.2 and is higher for higher frequencies because of reduced transmission through typical walls [33].

On the other hand, the input-referred integrated noise power of the receiver can be expressed as [34]:

$$N_{in} = k \times T \times NF \times BW \tag{2.3}$$

In this equation, k is the Boltzmaan constant and is equal to $1.38 \times 10^{-23} J/K$, T is the absolute temperature. NF is the noise factor of the receiver ($NF >= 1$).

By combining Equation 2.1, 2.2 and 2.3, the achievable data rate of a system can be expressed as function of bandwidth and frequency:

$$C = BW \times log_2(1 + \frac{P_t \times G_r \times G_t (\frac{\lambda}{4\pi \times d})^{\alpha}}{k \times T \times BW \times NF}) \tag{2.4}$$

The impact of frequency and bandwidth on the achievable data rate is shown in Figure 2.2 for a system with $d = 10$m, $P_t = 1$W. We assume half-wavelength dipole antennas at in free space (α=2) under line-of-sight situations, and the antenna size decreases at higher frequencies. This figure shows the achievable data rate as a function of frequency and bandwidth. The figure shows that data rates in excess of 10Gbps can be achieved for high bandwidths (1GHz) at low frequencies (1GHz).

The shape of the graph is caused by the different influences of bandwidth and *SNR* (and therefore indirectly frequency) on the channel capacity. Increasing bandwidth seem like an obvious way to improve the channel capacity, but it also increases the noise in the channel and therefore reduces the signal-to-noise ratio at a fixed signal level. Therefore, increasing bandwidth makes sense only if the *SNR* is sufficiently high. Since in in-house environments α is a function of frequency, the optimum at low frequencies will be even more pronounced than shown in Figure 2.2. This, together with the higher transparency of walls at lower frequencies and the simpler and cheaper electronics, explains the popularity of relatively low frequencies for radio communication.

However, this inherently leads to a conflict: if all high data rate applications prefer to use a lot of bandwidth at low frequencies, then the radio spectrum at low frequencies will quickly fill up, which it indeed does. This results in a drive towards higher frequencies, since there will be more bandwidth available than at lower frequencies. In addition, the decrease in data rate when increasing the frequencies as shown in Figure 2.2 is somewhat

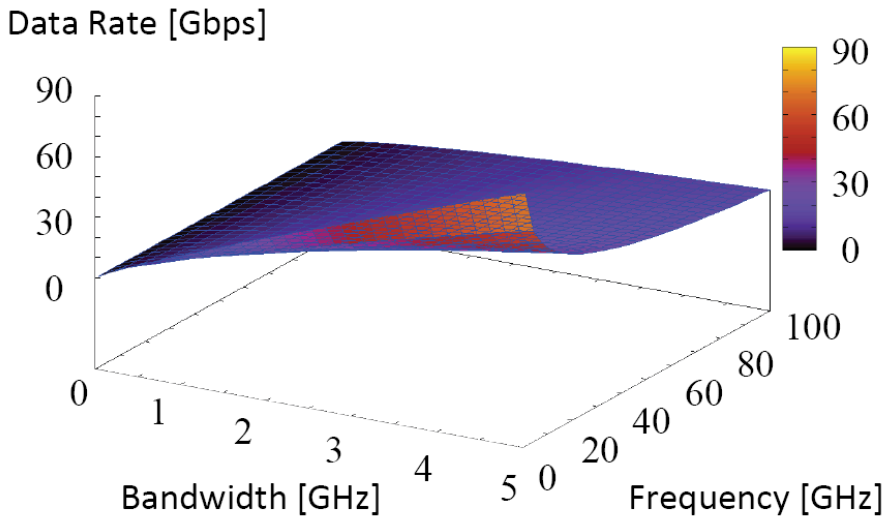


Figure 2.2: Achievable data rate versus frequency and bandwidth with half wavelength dipole antennas.

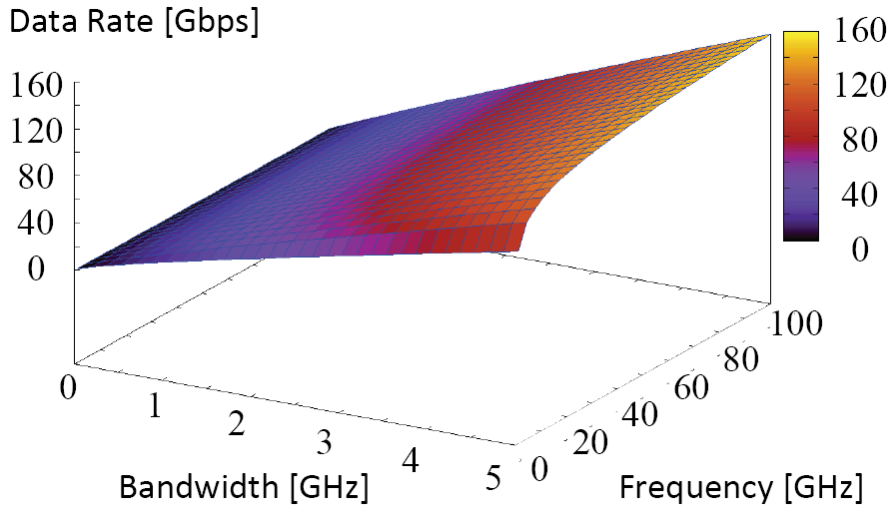


Figure 2.3: Achievable data rate versus frequency and bandwidth with antenna size fixed to a 900MHz dipole antenna.

deceptive, in that it is caused by the decrease in antenna size at higher frequencies. If we keep the physical antenna size the same as a 900MHz dipole antenna (by setting λ to a constant λ_0 in Equation 2.4), the achievable data rate of a system can be expressed as:

$$C = BW \times log_2(1 + \frac{P_t \times G_r \times G_t(\frac{\lambda_0}{4\pi \times d})^\alpha}{k \times T \times BW \times NF}) \tag{2.5}$$

According to Equation 2.5, there is no decrease in data rate with higher frequencies, and the achievable data rate still increases significantly with the bandwidth, as shown in Figure 2.3.

From these two results, high data rate radio links with high bandwidths at high frequencies (60GHz) make sense when electrically large antennas ($\gg \lambda/2$) are used, which provide antenna gain and directivity.

2.1.2 Automotive Radar

The basic principe of radar is that an RF signal is transmitted towards the target of interest, which is reflected from the target and then received by the radar antenna. Information regarding the distance, relative speed and angular position of the target is detected using the reflected signal. For instance, in either a pulse radar or a frequency modulated continuous-wave (FM-CW) radar, the distance of the target can be detected directly or indirectly utilizing the time for the signal to travel to the target and return. Speed can be detected by utilizing the change of distance with respect to time, or utilizing the frequency shift (Doppler Effect) of reflected signals. The angular position of the target can be determined by exploiting the directive gain of the antenna in different directions. When a certain antenna aperture is used, the angular resolution improves with higher RF carrier frequency. Furthermore, in most cases the receiver does not detect the reflected signal while the signal is being transmitted. The minimal detection range in a pulse radar is therefore determined by the pulse length. In order to detect closer targets, a shorter pulse will be used, which requires a larger signal bandwidth. An FM-CW radar also needs larger signal bandwidth to detect closer targets.

Automotive radars, which have been available in high end cars, will be key components of future smart cars. The reason is that car safety is a

serious issue in our lives: auto collisions are the leading cause of injury-related deaths, an estimated total of 1.2 million in 2004, or 25% of the total from all causes [35]. Pre-crash systems with automotive radars can detect an imminent crash and warn the driver and even help the vehicle itself to avoid a collision. As compared to visual and infrared (IR) sensors, the advantage of mm-wave radar is that it can be used not only in day and night conditions, but also in fog and other poor visibility conditions.

The 77GHz band (76-77GHz) can be applied to long-range (100m) autonomous cruise-control (ACC) radar, since the high carrier frequency results in a sufficient angular resolution. ACC radar helps maintain a safe distance to vehicles in front by automatically controlling vehicle speeds [36].

Short-range radars can use e.g. the 24GHz band (22-29GHz), since the large bandwidth offers sufficient small distance resolution (5cm). Short-range car radar has applications such as object detection, pedestrian detection and protection, parking aid, side-impact pre-crash detection and blind spot detection [11].

2.1.3 Millimeter-Wave Imaging

Millimeter-wave frequencies allow a spatial resolution of a few millimeters, which can be used for active and passive imaging [37]. Passive imaging detects natural thermal emissions of objects in the 35GHz and 94GHz bands, and forms the image of objects similar to an optical system. In an active imaging system, mm-wave signals are transmitted in order to “illuminate”objects.

Millimeter-wave imaging can operate not only in day and night conditions, but also in fog and other poor visibility conditions that normally blind visual and infrared (IR) cameras. It can help airport landing, airport operation, harbor surveillance and highway traffic monitoring [37].

Millimeter-wave imaging also has security applications such as concealed-weapon detection [37]. Since the mm-wave signatures of metallic objects are very different from body background, mm-wave imaging offers easy detection and few false alarms.

In addition, mm-wave imaging can be used in medical applications such as tumor detection, temperature measurement, blood flow and wa-

ter/oxygen content measurement [11]. It has the advantage of being harmless to humans: passive imaging only use the natural thermal emission, and active imaging uses radiations with milli-eV energies. In contrast, X-ray based imaging systems require radiations with k-eV energies, and can only be used with limited dosage.

2.2 System Requirements

Although they are in many aspects similar to transceiver architectures at lower frequencies, transceiver architectures at mm-wave frequencies have to meet several different requirements.

As discussed in the previous section, one of the main motivations for implementing radio links at mm-wave frequencies is the availability of empty bands. These bands allow the use of wide bandwidth transmissions to achieve high data rates, as long as a sufficient signal-to-noise ratio can be achieved.

One way to relax the requirements on signal-to-noise ratio is the use of less bandwidth-efficient modulation schemes. Since the performance of RF circuits at mm-wave frequencies is limited, a (relatively) constant envelope modulation scheme such as FSK or QPSK modulation will be attractive. QPSK modulation is used in this work, since it can be extended to other varying-envelop modulation schemes (e.g. high-order PSK with or without OFDM).

A time domain multiple-access (TDMA) scheme fits best with simple modulation schemes. It reduces interference from adjacent and alternate channels that will occur in frequency division multiple access (FDMA) schemes, and easily allows flexible and on-demand allocation of total system capacity across multiple sources.

Because of the high free-space path loss at mm-wave frequencies, phased array technique is an attractive solution to compensate for the path loss and alleviate the requirements of RF transceiver front-ends. This will impact both architectural and circuit level requirements for mm-wave frequency transceivers. Separate receiver/transmitter paths are required for each of the multiple antennas. Special attention has to be paid to phase consistency between the different receiver/transmitter paths. Therefore, a

common VCO/synthesizer with a classical up-conversion transmitter and down-conversion receiver will be both cost-effective and robust, especially for single-chip integration of a phased array transceiver. However, it may be difficult to integrate a large number of receiver/transmitter paths on a single chip, due to the limitation of e.g. chip area, cross-talk, parasitic coupling and power consumption. In that case, it is preferred to have an individually modulated VCO/synthesizer in each chip, and minimize the distribution of high frequency RF or LO signals betweens the multiple chips.

A mm-wave receiver will usually not suffer from very strong interferers. First, walls will attenuate signals from unrelated systems significantly. Second, signals originating in the same room are likely to be part of the same communication system, in which case the higher layers of the communication link can avoid interference by separating such signals in the frequency, spatial and/or time domain. Therefore, only limited channel selectivity will be needed. After the (limited) channel selectivity, the signal can be processed through (strongly) non-linear circuits such as limiters to provide the required gain and automatic gain control.

Circuit requirements for a receiver will typically emphasize gain at mm-wave frequencies, wide bandwidths, and low noise figures, with moderate requirements for linearity. For a zero-IF receiver, because of the limited interference provided by the higher layers, it is usually possible to achieve the desired second-order non-linearity by careful design of the mixers and AC coupling in the IF path.

Requirements on the phase noise of the VCO are likely to be relaxed, since the wide channel bandwidths puts the adjacent channels at a large frequency offset. In addition, if the system is completely TDMA based, and therefore effectively single-channel, requirements on the tuning range for the VCO will be relaxed since only process spread, temperature and power supply variations need to be compensated. It will even be possible to clean up the phase noise of the VCO across the full channel with a wide-band synthesizer loop especially for single-channel systems.

Transmitters for mm-wave systems need to generate wide-band signals. Since in many cases, bandwidth efficiency is not the primary design parameter, and since systems do not have to be dimensioned for minimum interference, requirements on dynamic range and error-vector magnitude

(EVM) are likely to be relaxed. Therefore, the emphasis for most transmitter circuits will be on gain, output power and wide bandwidths.

2.3 Implementation in Silicon & CMOS

Traditionally, mm-wave radio frequency (RF) technology has been the domain of expensive chip technologies based on III-V compound materials such as GaAs and InP [5]. These technologies have low yield and limited integration. They are mainly intended for professional and military applications for which the cost-factor is not of much relevance.

Recently, considerable RF performance at mm-wave frequencies has been achieved using low-cost silicon-based SiGe [6] and CMOS [7–10] technologies. The high frequency capacity of silicon based SiGe and CMOS technologies improves quickly. Their unity-gain frequency f_t and maximum frequency of operation f_{max} have reached hundreds of GHz. Considering that silicon based technologies have replaced GaAs in the low GHz regime except for a few applications (e.g. power amplifiers), they are expected to dominate in the mm-wave frequencies soon.

The advantage of SiGe technology is that as compared to CMOS technology, SiGe has better physical properties, reliable RF models and tools to meet mm-wave requirements. The drawback is that unlike the CMOS technology, SiGe can not cost-effectively integrate the digital baseband on the same chip with RF and analog circuits. Therefore, the radio system needs to be realized in multiple chips instead of a single chip.

CMOS technology has advantages of being the lowest cost option in volume production, and offering high level of integration with RF, analog and digital circuits. Although the RF performance of standard CMOS is worse than that of SiGe, the speed of CMOS transistors increases more rapidly. There are enormous world-wide efforts to scale to lower gate-lengths for the mass market of digital microprocessors, digital computation and memory. As a result, the speed of CMOS circuits increases by roughly one order of magnitude every ten years [38]. High power amplifiers implemented in today's 65 nm RF-CMOS technology can produce an output power level of higher than 10dBm [39, 40], and low noise amplifiers with noise figure of around 6dB can be realized at 60GHz [41, 42].

A fully integrated mm-wave system (RF, analog and digital circuits, or even antennas) in a single chip using a CMOS technology will bring many benefits, for example:

- The single-chip integration will result in a smaller footprint, and reduce the cost of multi-chip packaging and testing.
- With the aid of integrated advanced digital signal processing (DSP), there can be auto-tuning and digital calibration in the RF front-end. The functions may include I/Q matching calibration, filter bandpass tuning, VCO/PLL calibration. In this way, the RF front-end will be robust against process, voltage and temperature (PVT) variations.
- Self-testing of a full transceiver can be carried out in the loop-back mode automatically, which will avoid expensive RF test equipment and cost.

2.4 Conclusion

Millimeter-wave frequencies (30-300GHz) offer many new products and services such as multi-Gbps radio at 60GHz, automotive radar and mm-wave imaging, thanks to the high frequency and large bandwidth available at these frequencies. High data rate radio links with high bandwidths at high frequencies (60GHz) require electrically large antennas ($\gg \lambda/2$) that provide sufficient antenna gain and directivity.

As compared to counterparts at lower frequencies, transceiver architectures at mm-wave frequencies have to meet different requirements. In order to achieve a sufficient signal-to-noise ratio, less bandwidth-efficient modulation schemes (e.g. QPSK) become attractive. A TDMA scheme fits with these simple modulation schemes and can reduce interference to adjacent channels. Phased array techniques are attractive to compensate the path loss and alleviate the requirements of RF transceiver front-ends.

Recently, considerable RF performance at mm-wave has been achieved using low-cost silicon-based technologies. CMOS technology has advantages of being the lowest cost option in volume production, and offering high level of integration with RF, analog and digital circuits. In the next

chapters, we will present the design and implementation of 60GHz integrated circuits in a 65nm CMOS technology.

3

Phased Arrays and Architecture Selection

The 7GHz of unlicensed band around 60GHz offers exciting opportunities for applications such as high-speed short-range wireless personal area network (WPAN) and real time video streaming at rates of several Gbps [4–6].

A major issue in designing such a high data rate 60GHz radio is the limited link budget over indoor distances, especially for non-line-of-sight (NLOS) situations, due to the high path loss during radio propagation, high noise figure of the receiver and low output power of the transmitter [11,12].

Due to the relatively small size of 60GHz antennas, the phased array technique is an attractive solution to compensate for the path loss and alleviate the requirements of the RF transceiver front-ends. In addition to providing electronically controlled beam forming, phased arrays offer larger effective isotropic radiated power (EIRP) in the transmitter and higher signal-to-noise ratio (SNR) in the receiver [13–18]. This leads to higher system capacity and larger range which is highly beneficial to a 60GHz wireless system.

In this chapter, the motivation for phased-array techniques is discussed first in Section 3.1. The operation principles and benefits of phased arrays are discussed in Section 3.2 and Section 3.3 respectively. Section 3.4 compares the phased array technique to other MIMO techniques. Sec-

tion 3.5 discusses the phase-shift step-size requirements in phased arrays. Finally, different phased array architectures are compared in Section 3.6. This chapter is partly published in [12].

3.1 A 60GHz WPAN Link Budget

The target of this work is to provide a data rate of higher than 2Gbps over an indoor distance of 10 meters for general purpose (including WPAN and WirelessHD) applications. This data rate can be achieved by a 60GHz radio with a channel bandwidth of 2GHz using e.g. shaped QPSK modulation. As discussed in Section 2.1.1, a high data rate 60GHz radio requires electrically large antennas with high antenna gain and directivity. This can be analyzed in detail in the link budget calculation.

A high data rate 60GHz radio has a limited link budget over indoor distance, due to the high path loss during radio propagation, high noise figure of the receiver and low output power of the transmitter [11]. The large signal bandwidth required to transmit at a large data rate further increases the noise floor of the receiver. Figure 3.1 shows the link budget calculation. In the calculation, the transmitted output power is +10dBm [23, 31], omnidirectional antennas are used in the transmitter and receiver with antenna gain of 0dBi, and the receiver noise figure is +10dB [8, 43]. According to Friis' equation (Equation 2.2), the received power is $P_{sig} = -78$dBm at a distance of 10 meters. On the other hand, the integrated noise referred to the input of the receiver can be expressed as:

$$N_{tot} = -174 + NF + 10log_{10}(BW) \tag{3.1}$$

in dBm, where NF is the noise figure of the receiver and BW is the signal bandwidth. Given $NF = +10$dB and $BW = 2$GHz, the integrated noise referred to the input of the receiver is $N_{tot} = -71$dBm. The signal-to-noise ratio (SNR) at the output of the receiver can be defined as

$$SNR_{out} = P_{sig} - N_{tot} \tag{3.2}$$

in decibels, which is $-78 + 71 = -7$dB in this case. This SNR is much lower than the required value of 10dB in order to properly demodulate e.g. QPSK signals.

Component	Contribution	Running total
TX power	+10 dBm	+10 dBm signal
TX antenna gain	0 dBi	+10 dBm signal
Path loss over 10m	-88 dB	-78 dBm signal
RX antenna gain	0 dBi	**-78 dBm signal**
Background noise	-174 dBm/Hz	-174 dBm/Hz noise
Noise BW (2GHz)	+93 dB	-81 dBm/Hz noise
Noise figure of RX	+10 dB	**-71 dBm noise**
SNR of RX		**-78 – (-71) = -7 dB**
Required SNR		**10 dB (i.e. for QPSK)**
System margin		**-17 dB**

Figure 3.1: Link budget of a 60GHz WPAN using omni-directional antennas.

An appealing solution to the limited link budget at 60GHz is to use high gain antennas, which can partly compensate for the path loss and alleviate the requirements of the RF transceiver front-ends. Figure 3.2 shows the link budget calculation of a 60GHz radio under line-of-sight (LOS) situations if both the receiver and transmitter using directional antennas with antenna gain of $G_t = G_r = 12$dBi. Then the SNR at the output of the receiver will be increased to 17dB, which meets the demodulation requirement of e.g. QPSK signal with 7dB margin.

The link-budget calculation above leads to the conclusion that for the transmission of higher than 2Gbps over a distance of 10 meters under LOS situations at 60GHz, antennas should have a relatively high gain. It is worth pointing out that the link budget will be further reduced for a higher data rate, a larger distance and especially under non-line-of-sight (NLOS) situations. In this case, although we may increase the transmitter output power and reduce the receiver noise figure (limited by the cost, power and technology), using higher gain antennas seems to be the most practical solution for the link budget.

Fortunately, it is possible to achieve a high antenna gain with a relatively small structure at 60GHz, since the antenna gain (G) for a given effective antenna area (A) can be expressed as:

Component	Contribution	Running total
TX power	+10 dBm	+10 dBm signal
TX antenna gain	12 dBi	+22 dBm signal
Path loss over 10m	-88 dB	-66 dBm signal
RX antenna gain	12 dBi	**-54 dBm signal**
Background noise	-174 dBm/Hz	-174 dBm/Hz noise
Noise BW (2GHz)	+93 dB	-81 dBm/Hz noise
Noise figure of RX	+10 dB	**-71 dBm/Hz noise**
SNR of RX		**-54 – (-71) = 17 dB**
Required SNR		**10 dB (i.e. for QPSK)**
System margin		**7 dB**

Figure 3.2: Link budget of a 60GHz WPAN using high-gain directional antennas.

$$G = 4\pi A/\lambda^2 \tag{3.3}$$

where λ is the signal wavelength, which is 5mm in free space for 60GHz radio. In theory, the effective area of an 60GHz isotropic antenna is $\lambda^2/(4\pi) = 2\text{mm}^2$. An antenna with an effective area of 32mm^2, which is 16 times the effective area of an isotropic antenna, can achieve an antenna gain of 12dBi at 60GHz. This high gain antenna can be physically implemented as a single antenna or an antenna array. For fixed links (e.g. LMDS), we can use a single antenna that is mechanically aligned towards the antenna on the opposite side of the radio link. For mobile links, the alignment of the main lobe needs to be achieved dynamically, usually through phased array antenna structures, which is the research topic of this work.

3.2 Operation Principles of Phased Arrays

The operation principle of the phased array technique (using a receiver as an example) is depicted in Figure 3.3. The phased array receiver consists of N separate signal paths that connect to separate antennas. The

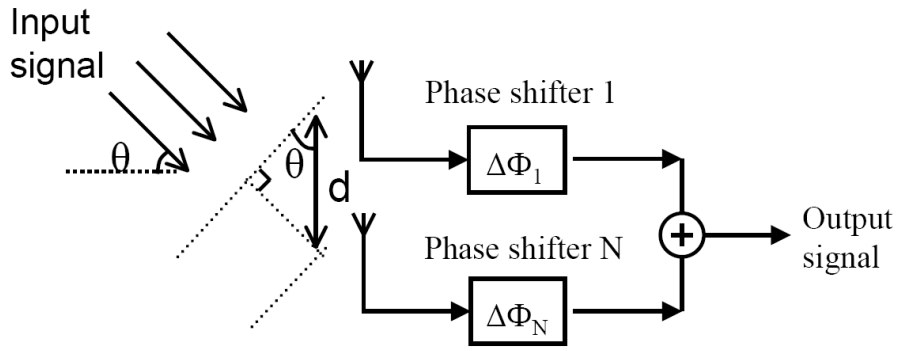


Figure 3.3: Principle of a phased array receiver.

desired signal from certain incident angle(s) (θ) arrives at these antennas with different time delays. In a one-dimensional antenna array receiver, the progressive time delay between two adjacent antennas is

$$\tau = dsin(\theta)/c \tag{3.4}$$

where d is the antenna spacing and c is the light speed. The signal received by the first antenna of a phased array receiver can be represented as

$$S_0(t) = A(t)cos[2\pi ft + \varphi(t)] \tag{3.5}$$

The signal received by the nth antenna is

$$S_i(t) = S_0(t - n\tau) = A(t - n\tau)cos[2\pi ft + \varphi(t - n\tau) - 2\pi nf\tau] \tag{3.6}$$

where $A(t)$ and $\varphi(t)$ are the gain and phase of the signal and f is the carrier frequency.

The time delays among the different signals paths can be compensated in the receiver so that the signals are combined coherently at the output. By this means only signals from certain directions are received, while the interferers from other directions are suppressed. An ideal programmable time-delay compensation for this purpose has to achieve a sufficient delay-resolution and be capable to work with large delay-range [44,45]. The implementation of such a time-delay compensation is challenging due to the loss, nonlinearity and chip area constraints. An alternative is to approximate the required time-delay compensation with a programmable phase

shifter [16, 18]. For a radio system that has a signal bandwidth much less than the carrier frequency, τ is much less than the baseband symbol period. Then we have

$$A(t) \approx A(t - n\tau) \tag{3.7}$$

$$\varphi(t) \approx \varphi(t - n\tau) \tag{3.8}$$

If the phase shift in the nth path is given by

$$\phi_n = n\phi = 2\pi n f \tau \tag{3.9}$$

and supposing that each path of the receiver has a unity gain, then the combined signal at the output can be expressed as

$$\begin{aligned} S_{out}(t) &= \sum_{n=0}^{N-1} A(t - n\tau) cos[2\pi f t + \varphi(t - n\tau) - 2\pi n f \tau + \phi_n] \\ &\approx \sum_{n=0}^{N-1} A(t) cos[2\pi f t + \varphi(t) - 2\pi n f \tau + \phi_n] \\ &= N * S_0(t) \end{aligned} \tag{3.10}$$

This result shows that phase shifters can also compensate the carrier phase shift of each path. In this way, the signals received by the multiple antennas can be approximately added up coherently at the output, which improves the signal gain in comparison to a single-antenna receiver. The approximation of a time-delay compensation with a programmable phase shifter, however, brings errors in the output signal, since the baseband signals (Equation 3.7 and 3.8) are not fully synchronized. These errors will be further analyzed in Section 3.5.

3.3 Benefits of Phased Arrays

Phased arrays bring several advantages to the wireless system.

Firstly, in a phased array receiver, the signals received by the multiple antennas can be added up coherently. On the other hand, as shown in

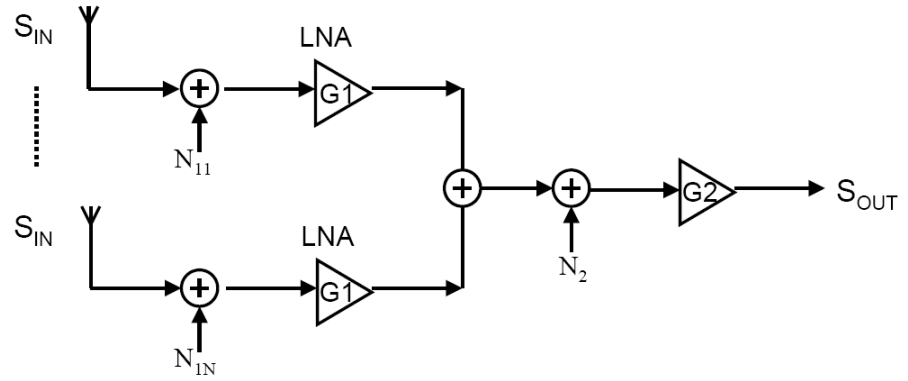


Figure 3.4: SNR improvement in a phased array receiver.

Figure 3.4, the noises of different receiver paths, dominated by the contributions of separate antennas and the low noise amplifiers after the antennas ($N_{11}, N_{12}, ..., N_{1N}$), can be considered to be uncorrelated to each other. As a result, if N antennas are used in the receiver, the output signal-to-noise ratio and therefore the sensitivity of the receiver can be improved by $10log_{10}(N)$dB.

Secondly, in a phased array transmitter (Figure 3.5), the signals transmitted by the multiple antennas can be added up coherently in certain direction(s) in space through spatial power combining. In comparison to a single-antenna transmitter that transmits an output power of P_0, each path of the phased-array transmitter can transmit an output power of P_0/N and keep the sum of the output power equal to P_0. The equivalent isotropic radiated power (EIRP) of the phased-array transmitter will be $P_0 * N$, which is increased by $10log_{10}(N)$dB in comparison to a single-antenna transmitter. Besides, the output power of a phased array transmitter can be controlled by simply turning on or off a certain number of transmitter paths.

Thirdly, a phased array system can place nulls in undesired direction(s), which improves channel multipath profile and reduces interference to/from other systems.

As a result, a phased array leads to higher system capacity, larger range and interference suppression, which is highly beneficial to a mm-wave (60GHz) wireless system.

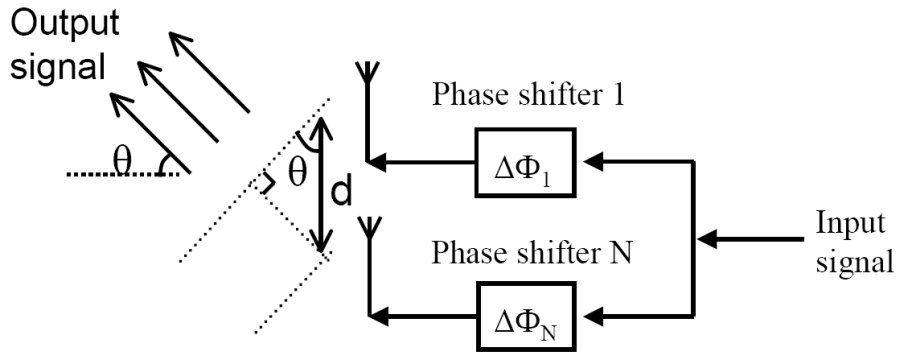


Figure 3.5: Principle of a phased array transmitter.

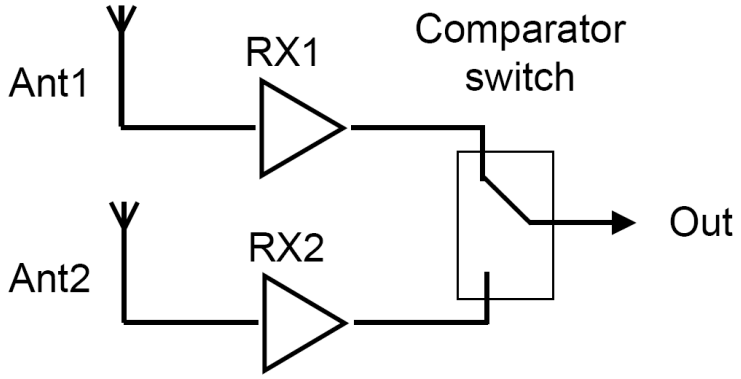


Figure 3.6: Antenna diversity

3.4 Phased Arrays and MIMO

MIMO (multiple-input-multiple-output) often refers to a wireless communication system employing multiple antennas at both a transmitter and a receiver. MIMO can be sub-divided into three main categories, namely phased array beamforming, diversity and spatial multiplexing [46].

Beamforming systems (Fig. 3.3) receive the same signal from each of the antennas with appropriate phase (and sometimes gain) weighting. In this way, the signal power is maximized at the receiver output. The benefits of beamforming are the increase of signal gain from constructive combination of the output signal and the reduction of multipath fading

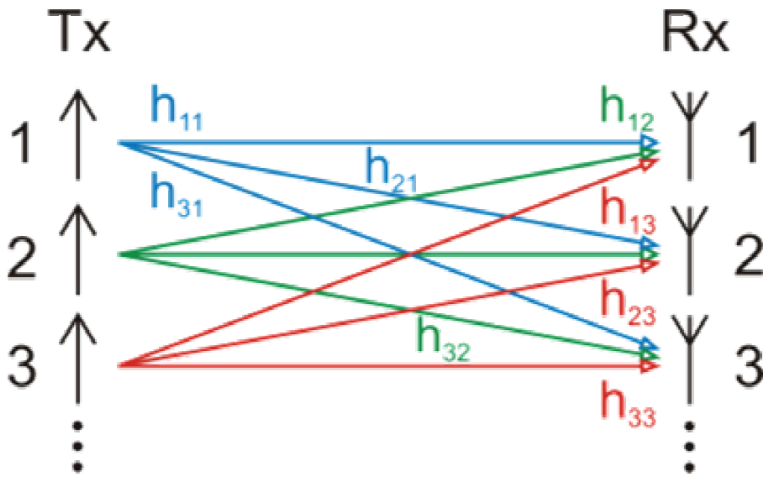


Figure 3.7: Spatial multiplexing [46].

effect.

In diversity systems (using a receiver as an example) as shown in Figure 3.6), multiple and redundant copies of a data stream are received by the receiver. The receiver decides to choose some of the data streams that survive the physical path between transmission and reception in a good enough state. A diversity transmitter works in a similar way.

Using spatial multiplexing methods (Figure 3.7 [46]), different data streams are transmitted by the different transmit antennas. If these steams arrive at the receiver antenna array with sufficiently different spatial signatures, the receiver can separate these streams and create parallel channels. This can increase data rate by using parallel channels.

From the above, in both beamforming and diversity systems, the same signal is received by the multiple antennas, which will increase link reliability. Beamforming has further advantage of increased signal gain and reduced interference through coherent signal combination. Spatial multiplexing methods can increase data throughput with the use of a limited bandwidth, but need independent transmitter, receiver and baseband digital signal processing for each of the multiple data streams.

Instead of using spatial multiplexing or diversity methods, beamform-

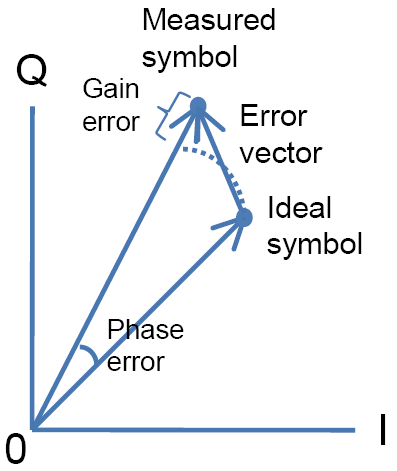


Figure 3.8: The constellation spreading can be quantified as error-vector magnitude (EVM).

ing methods are preferred at mm-wave (60GHz) for short-range high-speed communications. The reason is that, firstly, there are large bandwidths available at these frequencies, and it seems not necessary to use spatial multiplexing in order to further increase data rate. Furthermore, the environment does not provide rich multipath at 60GHz [4].

3.5 Phase-Shift Quantization

A phase shifter can provide a continuously variable phase shift, or a discrete set of phase states. In comparison with a continuously variable phase shifter, a discrete-step phase shifter has phase quantization errors. The advantage of using a discrete-step phase shifter is that it can be fully digitally controlled, which allows for a simple control and better immunity to noise on the control lines. The step-size requirement of a phase shifter (being either continuously variable or in certain discrete steps) depends on the phased array system specifications.

Firstly, the step-size requirement can be derived from the constellation spreading of the output signal in a phased array system (Figure 3.8) [18]. This is because when a continuously variable phase shifter is used instead

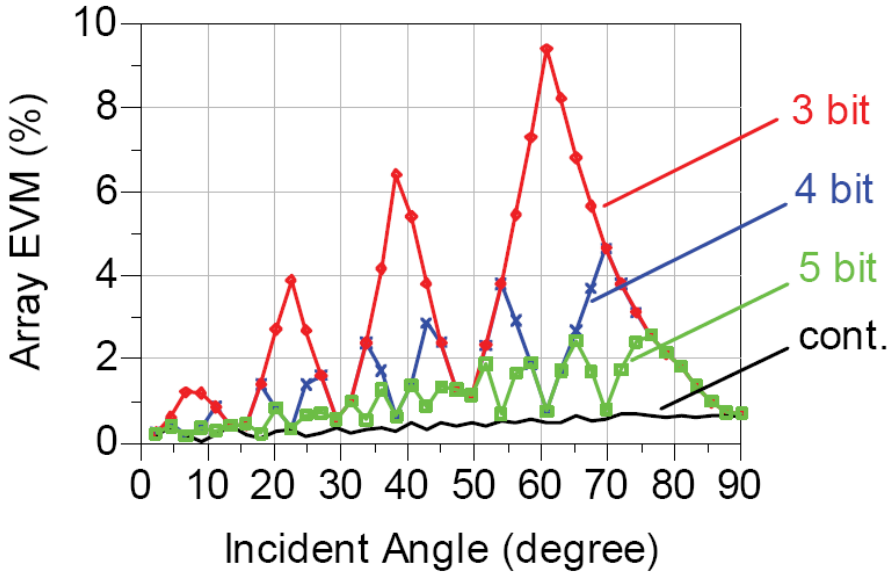


Figure 3.9: Simulated EVM of a 60GHz 8-path phased array receiver (BW=7.5GHz, Data rate=10Gbps using QPSK modulation) with various phase shift steps (continuous, 3-bit, 4-bit or 5-bit respectively).

of a time-delay compensation, the baseband signals are not fully synchronized, which reduces signal integrity. When a discrete-step phase shifter is used, the phase shift can only compensate the carrier phase shift exactly at a few incident angles. For other angles, the signal constellation at each path is rotated by a different (and incorrect) phase shift, thus further reducing signal integrity and increasing the constellation spreading. The difference between ideal symbol constellation (using a time-delay compensation) and actual symbol constellation (using a phase shifter) can be quantified as the error-vector magnitude (EVM) [18]. It is equivalent to the inverse of signal-to-noise-and-distortion ratio ($SNDR$), and in a phased array it can be expressed as [47]

$$EVM_{RMS} = \sqrt{\frac{\sum_{n=0}^{M-1} \mid \frac{S_{out}(t)}{C_0} - S_0(t) \mid^2}{\sum_{n=0}^{M-1} \mid S_0(t) \mid^2}} \tag{3.11}$$

Here M is the total number of symbols. C_0 is a complex constant representing the amplitude and phase offset between S_0 and S_{out}, which includes the phase offset of the carrier.

The EVM depends on, among others, the ratio of the signal bandwidth to the carrier frequencies, the step size of the phase shifters, the incident angle, the number of antennas and the digital modulation scheme. In a simulation, we have assumed a 60GHz 8-path phased array receiver that uses isotropic antennas with an antenna spacing of $\lambda/2$, which provides an antenna gain of 12dBi as discussed in Section 3.1. It has a bandwidth of 7.5GHz and bit rates of 10Gbps by employing shaped QPSK modulation ($\beta = 0.5$). Fig. 3.9 shows the EVM results as a function of various phase-shift step sizes i.e. 0^o (continuous), 11.25^o (5-bit), 22.5^o (4-bit) or 45^o (3-bit), when the incident angle (θ) varies from 0^o to 90^o. When a continuous phase shifter is used, the EVM is 0.7% at incident angle of 90^o. Using a 4-bit phase shifter, the peak EVM is 4.6% at an incident angle of 70^o. This peak EVM is equivalent to a minimum output SNDR of around 27dB (contributed only by the phase shifters), which meets the required SNDR for QPSK signal demodulation (10dB) with sufficient margin. It is worth pointing out that the EVM results can be reduced by using a narrower bandwidth (e.g. 2GHz) and/or OFDM modulation method, where a phase shifter with a larger step size (e.g. 45^o) may be used. On the other hand, if a higher date rate is desired by using a higher-order modulation scheme (e.g. 16QAM or 64QAM), the phase shifter may require a smaller step size (e.g. 11.25^o).

Another requirement of the step size of a phase shifter can be derived from the radiation pattern of the phase array. Using a continuously variable phase shifter, the beam direction of a phased array can be continuously swept to cover all incident angles. When a discrete-step phase shifter is used, the beam direction is swept in discrete steps, which may result in mismatch between the beam direction and the signal incident angles and therefore reduce the array gain. According to Equation 3.10, assuming a phase shifter with $\phi_n = n\phi_0$ is used in the nth path, the signal gain of the phased array receiver for a certain incident angle (θ) can be calculated. This signal gain can be normalized to the signal gain of an ideal N-path phased array, which is often defined as the normalized array factor (AF)

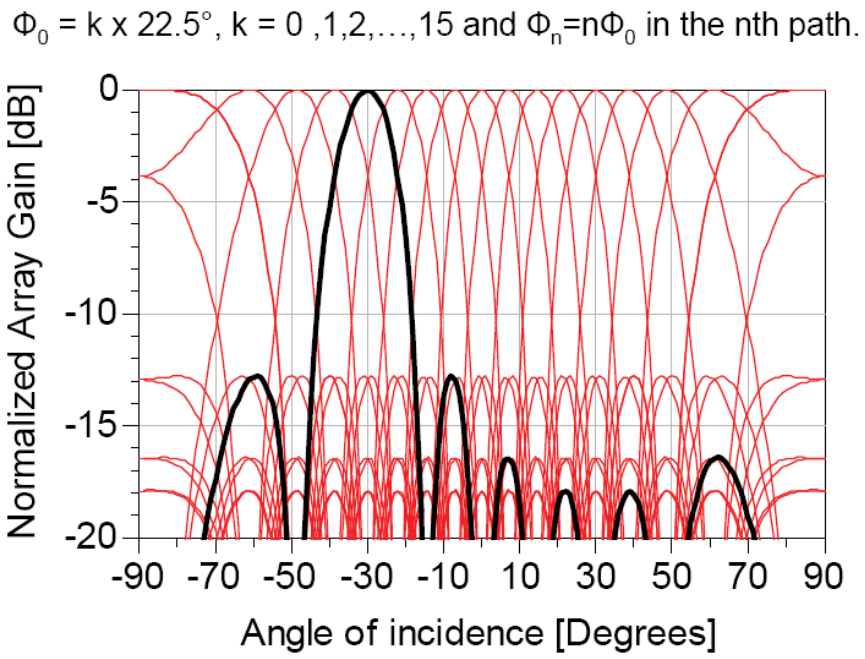


Figure 3.10: Simulated normalized 8-path beam patterns with 4-bit phase shifters. As an example, the beam pattern for an incident angle of -30° is highlighted.

[44] and can be expressed as

$$AF(\theta) = \frac{1}{N}\sqrt{\frac{\sum_{n=0}^{M-1} \mid S_{out}(t) \mid^2}{\sum_{n=0}^{M-1} \mid S_0(t) \mid^2}} \approx \frac{sin(\frac{N}{2}(\frac{2\pi fd}{c}sin(\theta)-\phi_0))}{Nsin(\frac{1}{2}(\frac{2\pi fd}{c}sin(\theta)-\phi_0))} \tag{3.12}$$

For example, the simulated array patterns of an 8-path phased array receiver with a 4-bit phase shifter are shown in Fig. 3.10. By increasing the incremental phase shift ϕ_0 from 0 to 337.5° in a 22.5° step size, the beam direction can be steered from -90° to 90° in 16 patterns. The beam pattern for the incident angle of -30° is highlighted in Fig. 3.10. In this application it can be seen that using a 4-bit phase shifter is sufficient for an 8-path phased array to cover all incident angles. The antenna array is operated close to its peak array gain; in the worst case, the signal loss is still less than 1dB. It can be shown that a smaller array (with e.g. 4

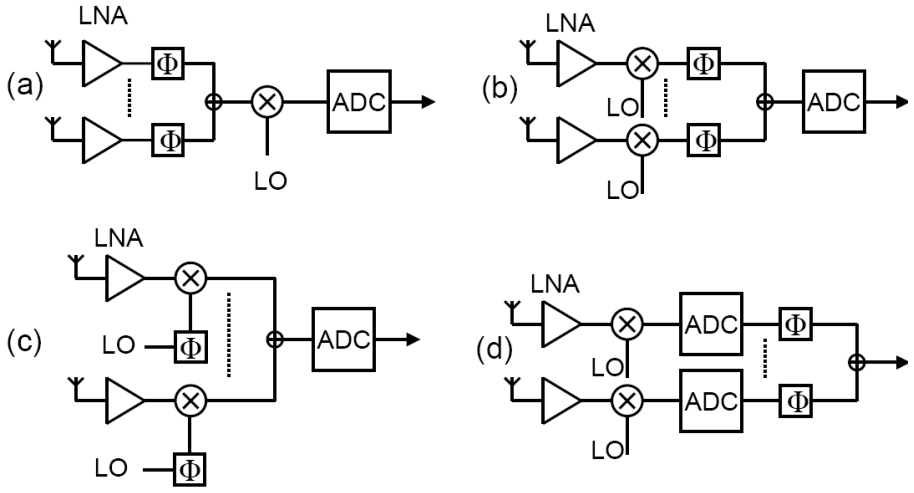


Figure 3.11: Phased array architectures with phase shifting at (a) RF, (b) IF, (c) LO and (d) digital baseband.

antennas) may use a phase shifter with a larger step for the beam direction consideration. However, if it is required to suppress interference by placing nulls in undesired directions, the phase shifter may require a smaller step.

In summary, the step-size requirement of a phase shifter can be derived from the system specifications with respect to e.g. constellation spreading, beam direction and interference suppression. Using a 4-bit phase shifter, which is often the choice of step size, is close to an ideal continuous phase shifter for the 60GHz system. Therefore, 4-bit phase shifters are designed and implemented for 60GHz phased array radio, which can be scaled to e.g. 3-bit or 5-bit according to different system requirements.

3.6 Phased-Array Architectures

Phase shifting can be implemented in different parts of a transceiver, such as at RF, IF, LO or digital baseband, as depicted in Figure 3.11(a)-(d) respectively. For simplicity, only the receive path is shown for a system with just 2 antennas.

Phase shifting in the digital domain shown in Figure 3.11(d) is often used for beam steering transceivers at the low GHz range, because it often

offers several advantages:

- high flexibility;
- high accuracy;
- relatively easy to design;
- robust against process, temperature and supply voltage variations except for mismatch between paths.

However, this architecture has several disadvantages at mm-wave frequencies:

- The IF bandwidth of a mm-wave frequency transceiver is usually much higher than at lower frequencies, making the phase shifting and adding operation non-obvious to design, and potentially power-hungry.
- The RF/LO/IF path, including mixers, local oscillators and data converters, has to be implemented multiple times (once for every antenna), typically increasing cost.
- Interference cancellation only occurs after the adder in the digital domain. Consequently, all circuits before that adder need to provide sufficient dynamic range to process these interferers without degrading the signal. This dynamic range requirement will increase the difficulty of the design of the RF/IF circuits and data converters, as well as increase the power dissipation of these circuits.

Therefore, in most cases it will be attractive to move the signal combining operation to the left towards the antenna. Various architectures can be considered as shown in Figure 3.11(a)-(c).

In Figure 3.11(a), phase shifting and combining of the antenna signals for beam steering is carried out at RF [28–31]. The RF phase shifting and combining can be done immediately after the antennas, but the programmable phase shifters at these frequencies will typically have significant losses and reduce the receiver sensitivity. Therefore, a better compromise is usually to insert the phase shifters between the low noise amplifiers and the mixers. The advantage of RF phase shifting is that the LO/IF

path, including the mixers, filters, variable gain amplifiers, local oscillators and data converters, can be shared among all antennas. Furthermore, interference cancellation occurs at RF, which reduces the dynamic range requirement of the following RF/IF circuits and data converters.

In Figure 3.11(b) an architecture with phase shifting and combining at IF is shown [24–27], which has the advantage that both operations now occur at lower frequencies (although still in the analog domain). This IF phase shifting and combining allows for easier and less critical implementation, but requires a relatively broadband analog phase shifter.

Figure 3.11(c) shows an architecture with phase shifting in the LO path and combining at IF [21–23]. The LO phase shifting requires multiplication of more circuits than RF phase shifting, but has the advantage that combining of signals at IF is easier to implement. Also, the LO phase shifting is not in the signal path, making the total performance less sensitive to the losses of the phase shifters (since they can be compensated for by generating more LO power). Finally, the phase shifter only needs to operate within a relatively narrow bandwidth (compared to the center frequency), making it relatively easy to implement.

Based on this analysis, if we can design RF phase shifters with programmability, low cost and low power, the RF phase shifting architecture offer the best overall performance in cost and power dissipation. An RF phase shifter may require a higher dynamic range as compared to an LO phase shifter. On the other hand, an RF phase shifting approach keeps the floor plan of the LO circuitry simple, i.e., there is only a single mixer (or two in an I/Q scheme) to be driven by the LO signal. This also means that the core circuitry of the receiver and transmitter (up to the mixer) can be reused for different array configurations, without the need to add additional mixers to the circuitry when, for example, increasing the number of antennas. At the end, the number of physical circuit elements is smaller in an RF phase shifting scheme than in an LO phase shifting scheme, leading to a smaller chip area. Therefore, in the next chapters, we will focus on the design of low cost, low power and programmable RF phase shifters at 60GHz.

3.7 Conclusion

A high data rate 60GHz radio has limited link budget over indoor distance, due to the high path loss during radio propagation, high noise figure of the receiver and low output power of the transmitter. Phased arrays help to direct energy from/to desired targets, which are highly beneficial to a 60GHz wireless system.

The step-size requirement of a phase shifter has been derived from the system specifications with respect to e.g. constellation spreading, beam direction and interference suppression. Simulation results show that using a 4-bit phase shifter is close to using an ideal continuous phase shifter for the 60GHz system.

If we can design RF phase shifters with programmability, low cost and low power, the RF phase shifting architecture offer the best overall performance in cost and power dissipation. For this reason, we will work on the design of low cost, low power and programmable RF phase shifters at 60GHz.

4

RF Phase Shifters for Phased Arrays

Phase shifters are essential components in a phased array for adjusting the phase of each antenna path and steering the beam. Ideally a phase shifter change the insertion phase (phase of S21) of a network while keeping the insertion gain (amplitude of S21) constant. The requirements of phase shifters include large phase-control range (360^{o}), small phase-shift step size (e.g. 22.5^{o}), low insertion loss (or even gain) and low variation in loss over all phase states. Furthermore, phase shifters need to achieve low power consumption, occupy a small chip area and be simple to control. The loss and loss-variations of a phase shifter can be (partly) overcome using an extra variable gain amplifier (VGA) stage in front of the phase shifter, but such a VGA not only consumes large chip area and power consumption but also becomes difficult to design at mm-wave frequencies.

There are various types of RF phase shifters, such as switched-line [48], loaded-line [49], reflection [50], switched-filter [51–53], traveling-wave [44, 54] and vector-modulator based [19, 55] phase shifters. These phase shifters are analyzed next in this chapter.

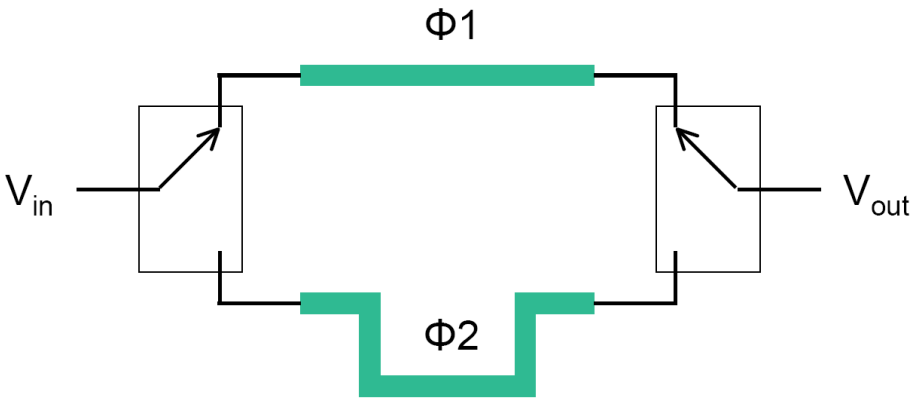


Figure 4.1: A switched-line phase shifter.

4.1 Switched-Line Phase Shifters

As shown in Figure 4.1, a phase shift can be achieved by switching two transmission lines with different electrical lengths [48]. If the insertion phase [phase(S21)] of two lines are ϕ_1 and ϕ_2 respectively and if the switches are ideally on or off, the change in phase shift obtained can be expressed as

$$\Delta\phi = \phi_2 - \phi_1 \tag{4.1}$$

Switched-line phase shifters are often used to achieve large phase-shift steps (e.g. 180^o and 90^o). Different phase shifters such as loaded-line phase shifters can be used for small phase shift steps (e.g. 45^o and 22.5^o).

The main challenge of designing a silicon based switched-line phase shifter at mm-wave frequencies lies in the single-pole double-throw (SPDT) switches. This is because the switches are often realized with MOSFETs, and their performance is limited at mm-wave frequencies. On the one hand, when switches are on, the switches need to have a large W/L value in order to achieve a small on-resistance and therefore a low insertion loss. On the other hand, the switches need to have a high isolation (i.e. 20dB) in the off state, otherwise there will be perturbation in the amplitude and phase response due to leakage of the ”off” path. However, large switches usually have large parasitic capacitance, which results in poor isolation during off. Although the off-state capacitance of the switches can be (partly) tuned

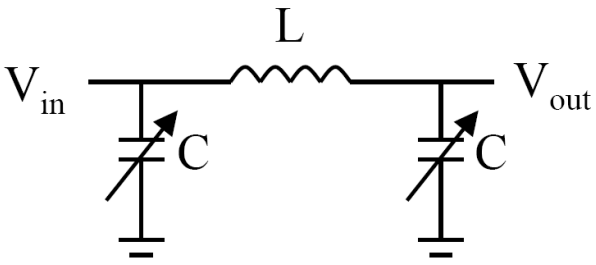


Figure 4.2: A loaded-line phase shifter.

out at desired frequencies by using a shunt inductor, this inductor-tuning solution results in a very narrow-band response and significantly increases chip area.

4.2 Loaded-Line Phase Shifters

A phase shift can also be obtained by tuning a lumped-element equivalent of a transmission line (Figure 4.2) [49]. This is because a transmission line with characteristic impedance Z_0 and insertion phase ϕ is equivalent to a low pass π configuration at carrier frequency f, if the following equations are valid:

$$Z_L = 2\pi f L = Z_0 \sin(\phi) \tag{4.2}$$

$$Y_C = 2\pi f C = \frac{1}{Z_0} \tan(\frac{\phi}{2}) \tag{4.3}$$

Although the inductor values may be varied by using active inductors, active inductors consume high dc power and increase the circuit and control complexity. Therefore, it is often to fix the inductor value by using a lumped inductor or a distributed transmission line.

The capacitance values can be varied by using MOS varactors or switching capacitors. The capacitance values Y_C are varied such that they create a perturbation in the phase of the signal, while the amplitude perturbation needs to be minimized in both states. As shown in Figure 4.3 [49], if the capacitance-control ratio $r_C = Y_{C,max}/Y_{C,min}$ is limited, increasing the center characteristic length ϕ_0 close or equal to 90^o can help to achieve a large

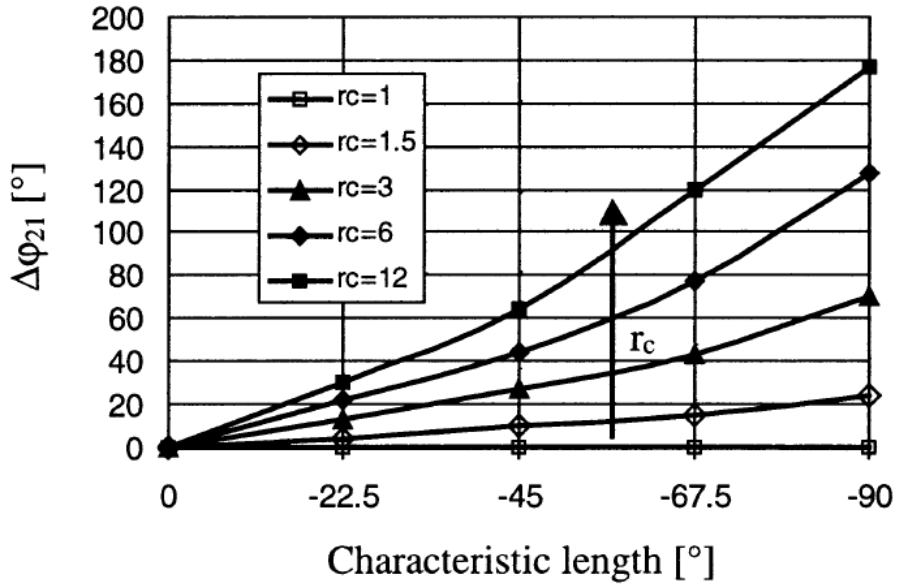


Figure 4.3: Phase-control range $\Delta\phi$ versus capacitance-control ratio r_C and center characteristic length ϕ_0 [49](©IEEE 2003).

phase control range. For example, if $r_C = 1.5$ and $\phi_0 = 90$, the theoretical phase control range is approximately 22^o. Due to the limited capacitance-control ratio (Y_{C2}/Y_{C1}), loaded-line phase shifters are usually only used for 45^o or lower phase-shift steps.

In Chapter 5, we will present a 60GHz 4-bit loaded-line phase shifter in a 65nm CMOS technology.

4.3 Reflection-Type Phase Shifters

Figure 4.4 shows a reflection-type phase shifter [50, 56]. A quadrature coupler divides the input signal into two signals 90^o out of phase. These signals reflect from a pair of reflective loads, and combine in phase at the phase shifter output. The phase of the reflection-type phase shifter can be controlled by varying the impedance of the reflective load Z_l. The reflec-

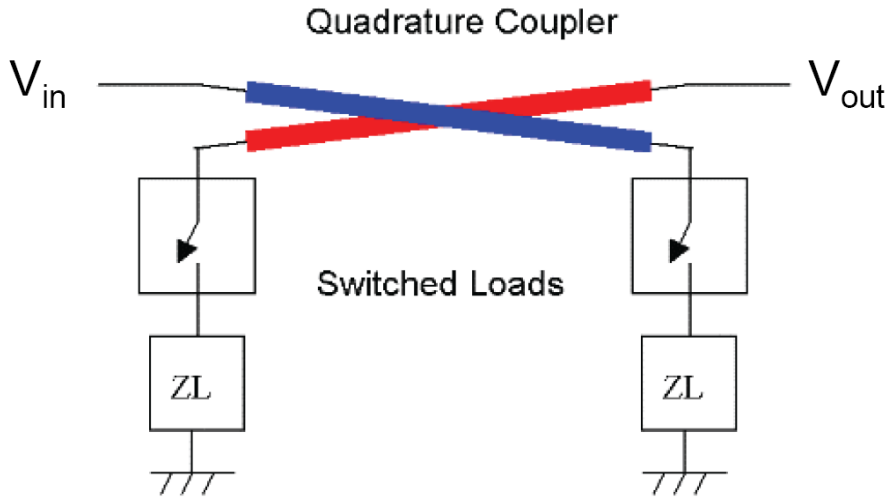


Figure 4.4: A reflection-type phase shifter [56] (used with permission from Microwaves101.com).

tion coefficient can be expressed as

$$\Gamma = \frac{Z_l - Z_0}{Z_l + Z_0} \tag{4.4}$$

If Z_l varies from Z_{min} to Z_{max}, the phase shift achieved is given by

$$\Delta\phi = 2[\arctan(\frac{Z_{max}}{Z_0}) - \arctan(\frac{Z_{min}}{Z_0})] \tag{4.5}$$

Reflection-type phase shifters can be used to provide both large and small phase shifts. For example, if the reflective loads use only varactors with a capacitance-control ratio of 4, the theoretical phase control range is 60^o [50]. If the varactors are used in series resonance with inductors, phase-control ranges of over 360^o can be theoretically reached even with such limited capacitance control ranges [50].

There are two main disadvantages in using reflection-type phase shifters. First, a silicon-based on-chip quadrature coupler often occupies a large chip area and has a high insertion loss at mm-wave frequencies. Second, programming of the reflection coefficient brings variations in both the phase and the amplitude of the reflected signal, which often results in large variations in loss over different phase settings.

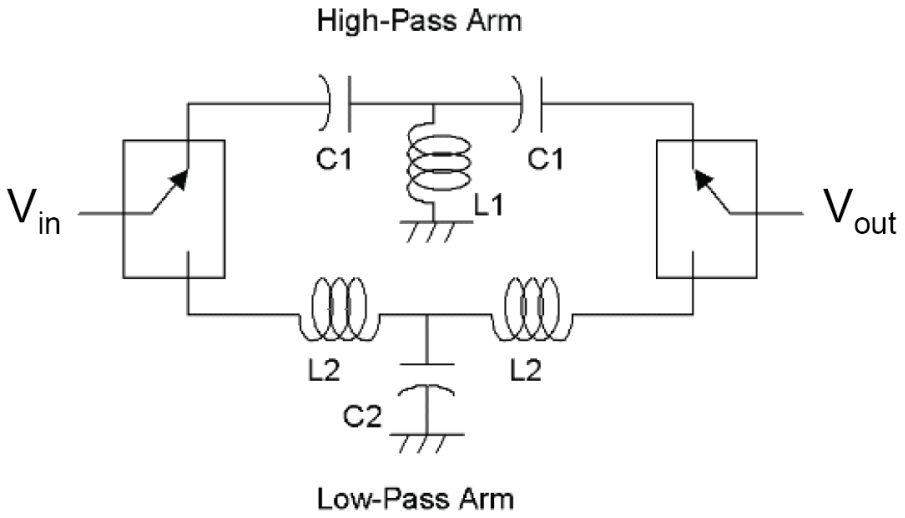


Figure 4.5: A high-pass low-pass phase shifter [56] (used with permission from Microwaves101.com).

4.4 Switched-Filter Phase Shifters

Switched-filter phase shifters can be implemented, for example, either by switching between high-pass/low-pass states which is called a high-pass/low-pass phase shifter [52,56]; or by switching between high-pass/by-pass states which is named a switched high-pass filter phase shifter [51–53].

A high-pass/low-pass phase shifter can achieve a constant phase shift over a large frequency range. As shown in Figure 4.5, the phase shifter switches to one arm as a high-pass filter or the other arm as a low-pass filter. It looks like a switched-line phase shifter that uses lumped elements instead of transmission lines. This phase shifter offers a compact layout at "low frequencies"(i.e. below X-band) where transmission lines are large. Similarly to switched-line phase shifters, it is difficult to design a silicon based high-pass/low-pass phase shifter at mm-wave frequencies, because MOSFET switches have high insertion loss during on and low isolation during off.

In comparison with a high-pass/low-pass phase shifter, a switched high-pass filter phase shifter (Figure 4.6) does not require SPDT switches, which

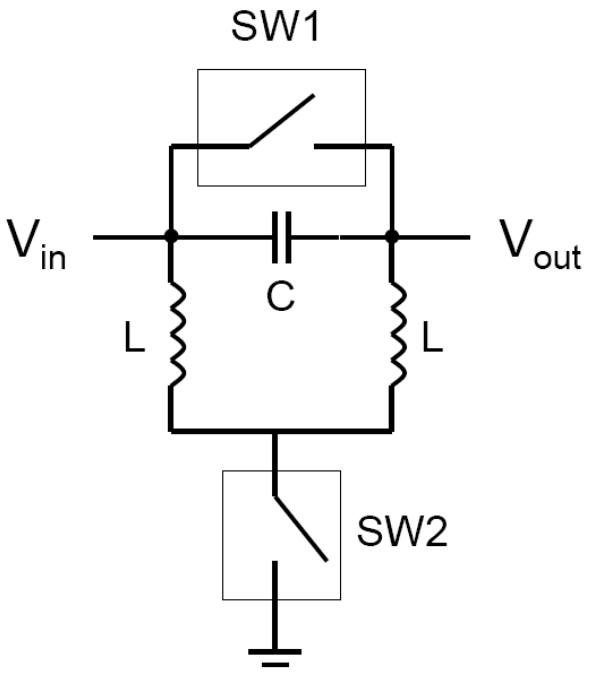


Figure 4.6: A switched high-pass filter phase shifter.

may result in less insertion loss. In the bypass state, SW1 shorts out the series capacitor, SW2 opens and disconnects the shunt inductors L from ground. In this way, the input signal is bypassed to the output. In the high-pass state, SW1 opens and SW2 shorts, and the high-pass π filter is realized. The high-pass filter's values are chosen such that it provides the required transmission phase while it has almost no effect on the amplitude in the high-pass state. However, it is still difficult to implement such a phase shifter at mm-wave frequencies due to the limitations of MOSFET switches.

4.5 Traveling-Wave Phase Shifters

Different phase shifts can also be achieved by interpolating the signal from different locations of a transmission line. Figure 4.7 shows a traveling-wave phase shifter [44, 54], which is also called a distributed phase shifter

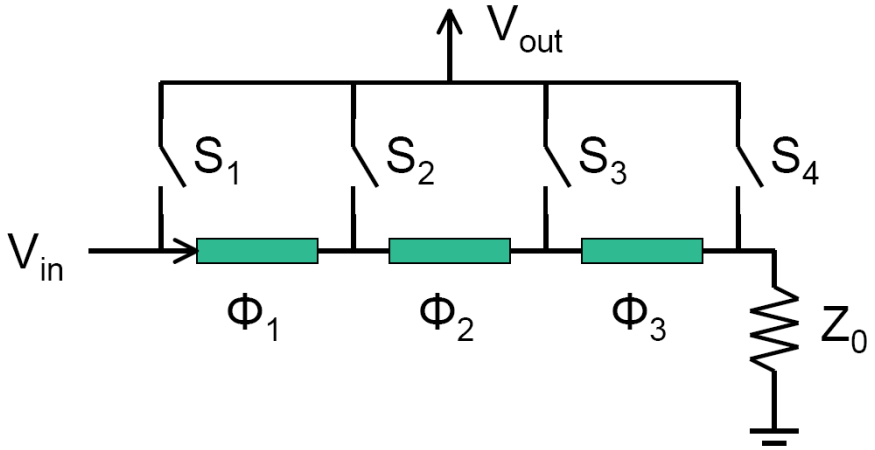


Figure 4.7: Concept of a traveling-wave phase shifter.

since it uses a technique that is also used in a distributed amplifier. It consists of a transmission line with impedance termination Z_0 and several switches. The parasitic capacitance of the switches can be (partly) absorbed into the transmission lines; this relaxes the requirements of the switches. If one of the switches among S_1, S_2, S_3 or S_4 is on and the remaining switches are off, the ideal insertion phase from the input (V_{in}) to output (V_{out}) will be 0, ϕ_1, $\phi_1+\phi_2$ or $\phi_1+\phi_2+\phi_3$ respectively.

There are two main problems to implement a traveling-wave phase shifter at mm-wave frequencies. First, the impedance of switches often changes significantly during on or off, which results in large amplitude variations and phase errors over different phase settings. Second, there is inherent power loss and extra noise contribution, because part of the input power sinks into the impedance termination Z_0 instead of going to the output (V_{out}).

4.6 Vector-Modulator Based Phase Shifters

Fig. 4.8 shows a vector-modulator based phase shifter [19, 55]. It is based on programmable weighted combinations of I/Q signals. The phase shift

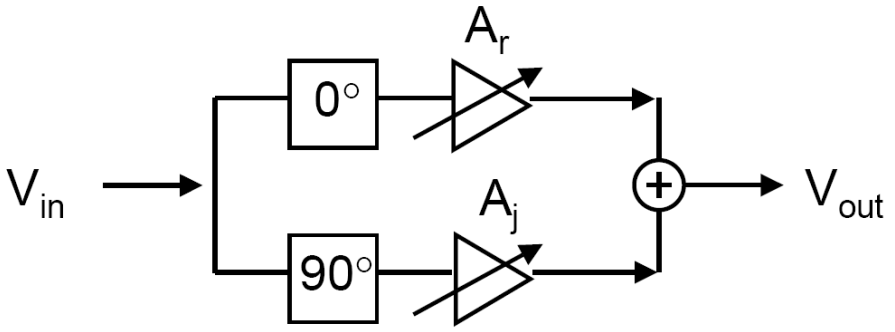


Figure 4.8: A vector-modulator based phase shifter.

achieved is given by

$$\phi = \arctan(A_j/A_r) \tag{4.6}$$

The gain of the phase shifter can be expressed as

$$A = \sqrt{A_r^2 + A_j^2} \tag{4.7}$$

Here A_r and A_j are the voltage gain of the two VGAs in the I/Q paths respectively. By programming the ratio of A_j/A_r in different settings, the phase shift can vary between 0^o to 90^o. By changing the polarity of A_r and A_j, a phase control range of 360^o can be achieved, which can be done by swapping the positive and negative paths in differential circuits. Furthermore, the gain of the phase shifter can be kept near constant over different phase settings.

The accuracy of the phase shift depends on the accuracy of the I/Q signal generation and the gain ratio of the two VGAs. The I/Q signals can be generated using a quadrature coupler [57], an RC poly-phase filter [19], a high-pass/low-pass filter, a quadrature all-pass filter [55] or simply a 90^o transmission line [21, 58]. A VGA can be controlled by e.g. changing the DC bias current of the transistors [55], or the DC bias voltage of a cross-coupled quad [57, 59], or through digitally controlled current steering by turning on or off a certain number of unit transistors in parallel [19, 58].

In contrast to the passive phase shifters, a vector-modulator based phase shifter is promising to achieve high gain and high phase accuracy. The

drawback is that it often has a lower linearity as compared to that of a passive phase shifter. A 60GHz 4-bit vector-modulator based phase shifter and its integration with LNA and PA in a 65nm CMOS technology will be presented in Chapter 6 and Chapter 7.

4.7 Conclusion

Phase shifters are essential components in a phased array for adjusting the phase of each antenna path and steering the beam. The requirements of phase shifters include large phase-control range (360^o), high phase-shift resolution(e.g. 22.5^o), low insertion loss (or even gain), low variations in loss over all phase states, etc.

It is challenging to design RF phase shifters at mm-wave frequencies (60GHz) in a CMOS technology. Some phase shifters, such as switched-line and switched-filter phase shifters, suffer from the limited performance of MOSFET switches. Other phase shifters, such as reflection-type and traveling-wave phase shifters, often have high insertion losses and large variations in losses. In the next Chapters, we will present both a 60GHz passive phase shifter and a 60GHz active phase shifter in a 65nm CMOS technology.

5

A 60GHz Passive Phase Shifter

This chapter presents the design of a 60GHz 4-bit passive phase shifter in a 65nm CMOS technology (Figure 5.1). The phase shifter consists of a differential transmission line loaded with a differential MOS varactor at each side. It achieves a phase-shift step size of 22.5^{o} (4-bit) and a phase control range of 360^{o} at 60GHz.

This chapter is organized as follows. Section 5.1 presents the design of a 60GHz 4-bit passive phase shifter. The measurement results of the phase shifter are presented in Section 5.2. This chapter is published in [60].

5.1 Design of a Passive Phase Shifter

As discussed in Section 4.2, phase shifters can be designed by tuning (part of) the lumped-element equivalent of a transmission line. In this work, a differential varactor-loaded transmission line phase shifter (Figure 5.2) is designed and implemented. The phase shifter consists of a differential transmission line loaded with a differential MOS varactor at each side. The cross-sectional view of a differential MOS varactor is shown in Figure 5.3. The top and bottom plates of the varactor are formed by the poly gates

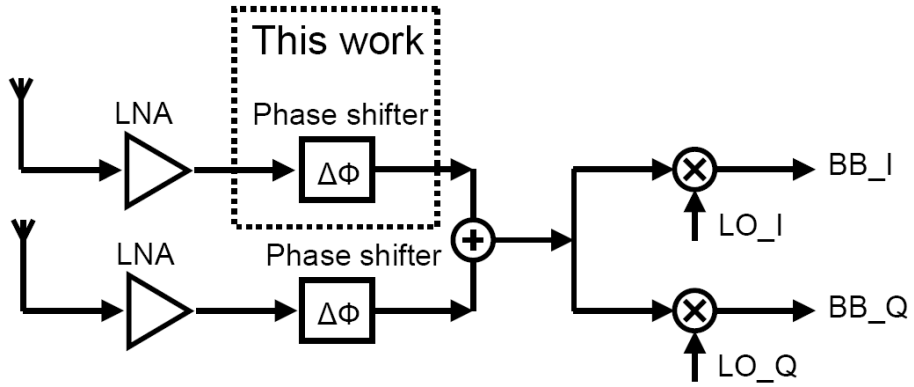


Figure 5.1: An RF phase shifter for 60GHz phased arrays.

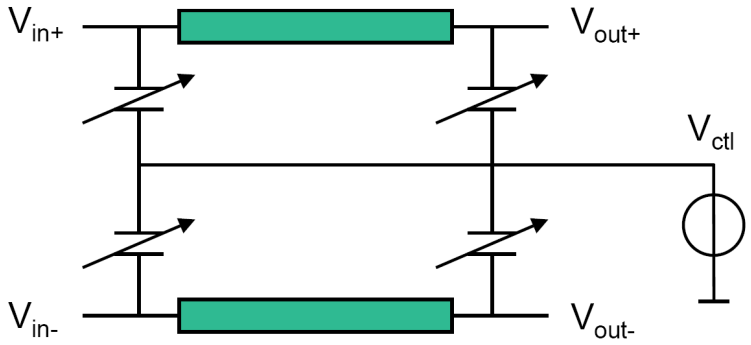


Figure 5.2: Schematic of a differential phase shifter consisting of a differential transmission line loaded with a differential varactor at each side.

and n-well. The differential gate terminals of the varactor are connected to the transmission line and the n-well of the varactor is connected to the DC control voltage. The varactor capacitance can be varied by the DC control voltage.

One advantage of using a differential phase shifter is that the differential paths can be swapped to provide a discrete phase step of 180^o, when e.g. integrated with a differential amplifier. Therefore, a differential phase shifter is only required to achieve a phase control range of another 180^o. Another advantage of using a differential phase shifter is that a differential

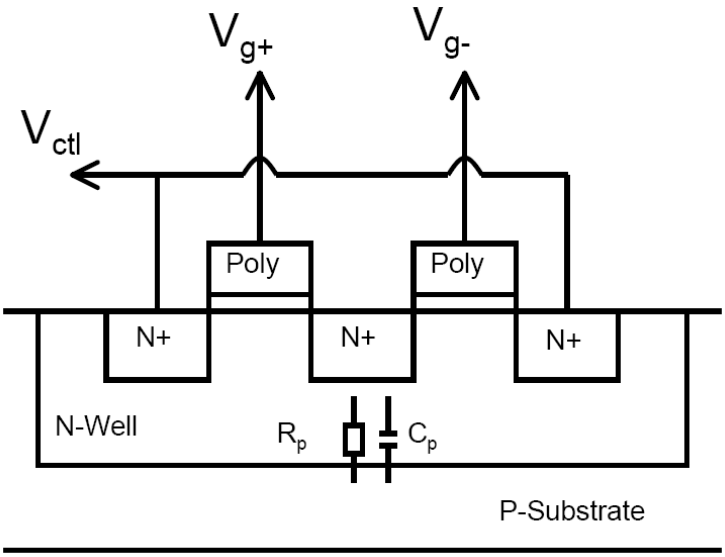


Figure 5.3: A cross-sectional view of a differential poly/n-well MOS varactor.

varactor has better capacitance-control range and better quality factor as compared to a single-ended varactor. This is because operating in a differential mode, the n-well node of a varactor is a virtual ground and less sensitive to parasitics (i.e. R_p and C_p). In contrast, it is difficult to create a low-impedance broadband AC ground at the n-well node of a single-ended varactor especially at 60GHz. As a result, a differential loaded-line phase shifter has better performance as compared to a conventional single-ended loaded-line phase shifter.

Figure 5.4 shows the performance of a differential MOS varactor at 60GHz in simulation. The DC bias voltages of the gates are set to 0.6V and the DC control voltage at the n-well is swept from 0 to 1.2V. The capacitance-voltage (CV) curve is almost flat when the control voltage is around 0 or 1.2V. By setting the control voltage digitally to either 0 or 1.2V, the varactor has a capacitance-control ratio of about 2 and a quality factor of more than 15 at 60GHz. The advantage of using binary voltage control, instead of using analog or multi-bit voltage control between 0 to 1.2V, is that it is less sensitive to the noise on the control voltage.

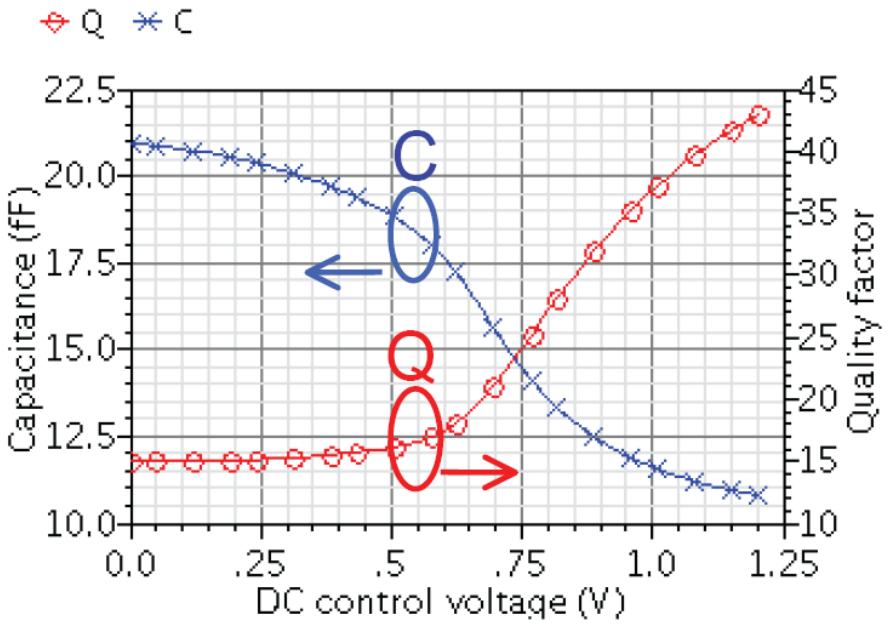


Figure 5.4: The simulated capacitance and quality factor of a differential MOS varactor at 60GHz.

The transmission line in Figure 5.2 might be replaced by distributed low-pass structures consisting of spiral inductors and capacitors [49]. The advantage of using a transmission line instead of a spiral inductor is that a transmission line is easy to model, scalable and has better isolation between the lines. The phase control range of a phase shifter depends on the capacitance-control ratio of the varactor and the length and characteristic impedance of the transmission line. By using a high-impedance transmission line, a large phase control range can be achieved. A high-impedance transmission line, however, usually has a higher loss. As a trade-off between the phase-control range, insertion loss and return loss, the differential impedance of the transmission line is chosen to be equal to the system impedance (100Ω).

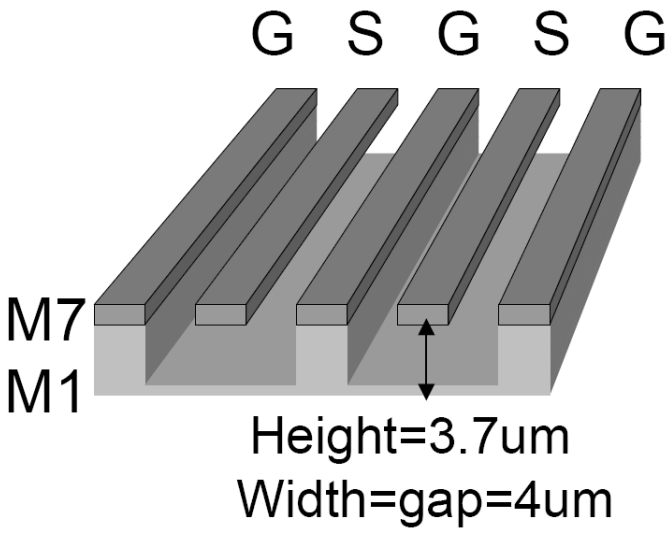
The transmission line used in this work is shown in Figure 5.5a. It is a differential coplanar transmission line in a ground-signal-ground-signal-ground (GSGSG) configuration with a solid ground plane. The signal lines are isolated from each other and also from the lossy silicon substrate.

Therefore, the electromagnetic (EM) modeling of the transmission line is relatively simple, accurate, less frequency dependent, and less process dependent (e.g. to the resistivity and thickness of the substrate), as compared to other transmission line structures without a solid ground plane. Besides, different transmission lines can be closely placed together in the layout to save area. The signal lines are using the top metal layer (metal-7) which achieves the desired characteristic impedance with a low insertion loss for two reasons: firstly, these lines are relatively thick (0.9μm); secondly, these lines are relatively far from the ground plane and can be reasonably wide for the desired characteristic impedance. The ground lines are using the top metal layer (metal-7) that is connected to the bottom metal layer (metal-1) through vias, and form a solid ground plane using the bottom metal layer (metal-1) underneath the signal lines. Based on EM simulation results, the width and spacing of the signal lines and ground lines are all 4μm at the top metal layer (metal-7), which achieves a differential impedance of 100Ω with a relatively low insertion loss and a small chip area.

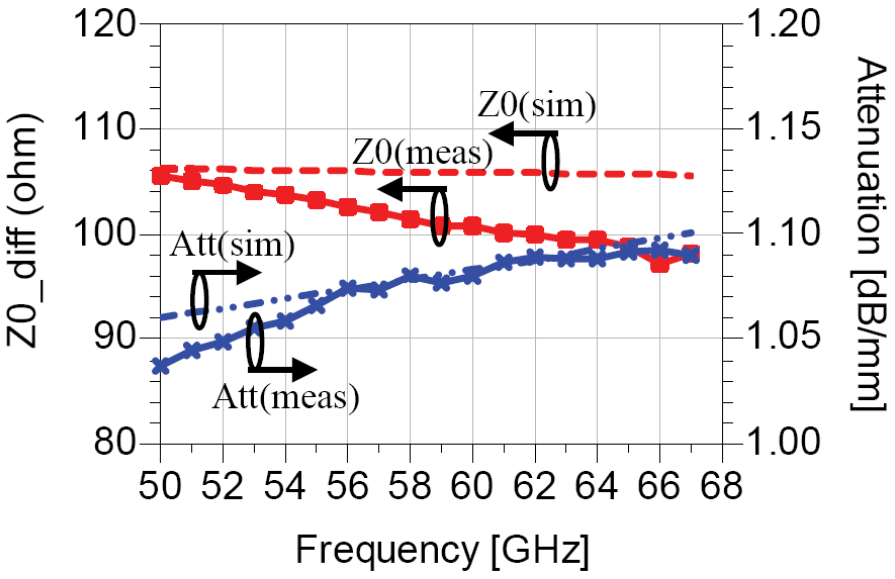
Figure 5.5b shows the measurement results of the transmission line. It has a measured differential impedance $Z_0 = 100\Omega$, a relative dielectric constant (ε_r) of 3.8 and an attenuation of 1.08dB/mm at 60GHz, which matches the EM-simulation results. The difference between simulated and measured Z_0 is probably due to the accuracy of de-embedding, since there are open and short stubs used as test structures, whereas load and through structures are not available.

Due to the limited capacitance-control ratio of a MOS varactor, the phase control range of each phase shifter section is designed to be around 22.5^o at 60GHz. The length of each transmission line is 0.16 wavelengths at 60GHz. The insertion phase of each section is designed to be around either -101^o or -79^o when the control voltage is low or high respectively, the center insertion phase of which is -90^o, in order to keep the impedance relatively constant when switching states.

Seven π-sections are cascaded to achieve a total phase control range of 157.5^o as shown in Figure 5.6, whereas a discrete phase step of 180^o can be provided by swapping the differential paths. The DC bias voltages of the transmission lines are 0.6V. There are 8 different phase states by setting the control voltage of a certain number of π-sections to logic low or high according to 3 digital control bits (V_{N2}, V_{N1} and V_{N0} in Figure 5.6).



(a)



(b)

Figure 5.5: (a) A differential coplanar (GSGSG) transmission line, in which the signal lines use the top metal layer (metal-7) and the solid ground plane uses the bottom metal layer (metal-1) underneath the signal lines, and (b) its measured results.

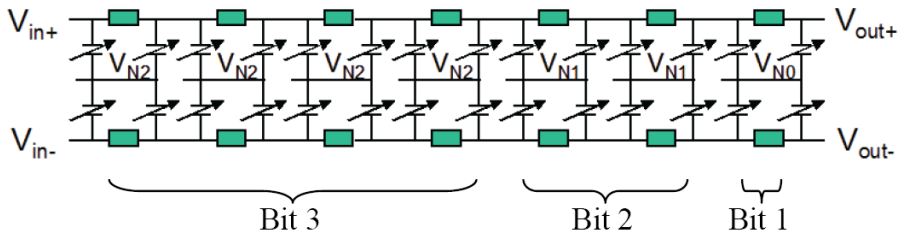


Figure 5.6: A schematic of 60GHz phase shifter, in which seven π sections are cascaded to realize a phase control range of 157.5^{o}.

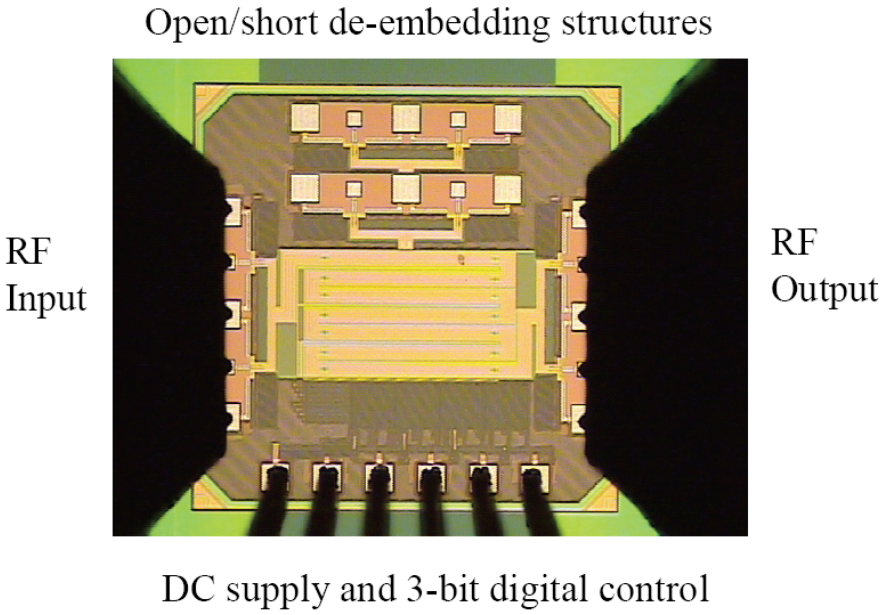


Figure 5.7: Photograph of the 60GHz passive phase shifter including open and short de-embedding structures.

The phase shifter can be extended to e.g. 5-bit by cascading another π-section that provides a phase step of 11.25^{o}.

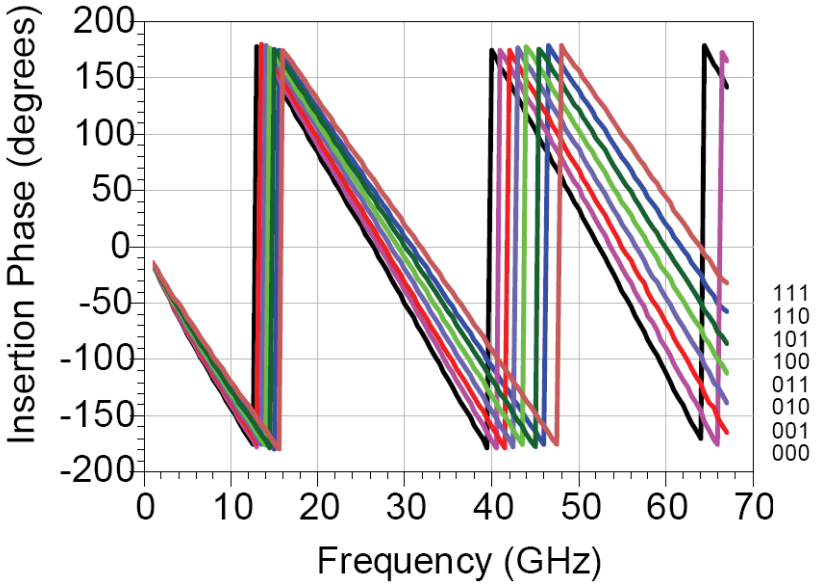


Figure 5.8: The measured insertion phase of 8 different phase states over frequency.

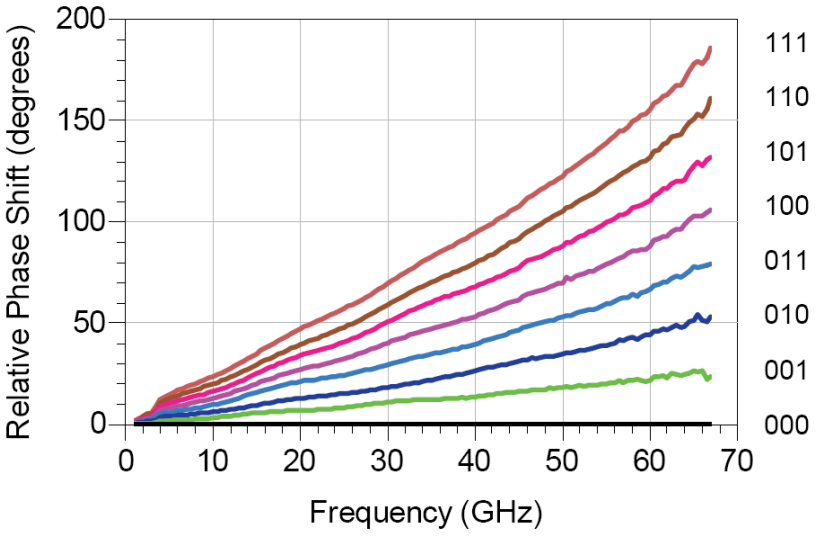


Figure 5.9: The measured relative phase shift of 8 different phase states over frequency.

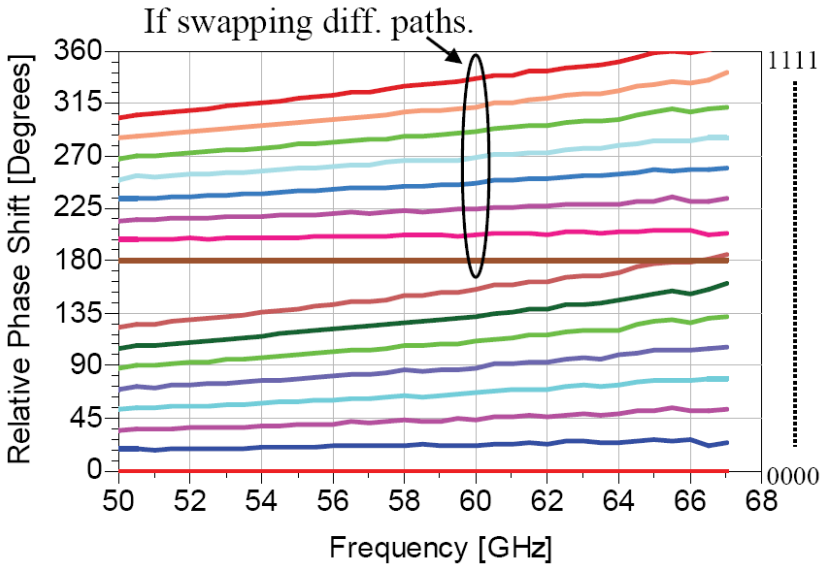


Figure 5.10: The synthesized phase shift of 16 different phase states, with the differential paths swapped to provide a discrete 180^{o} phase shift.

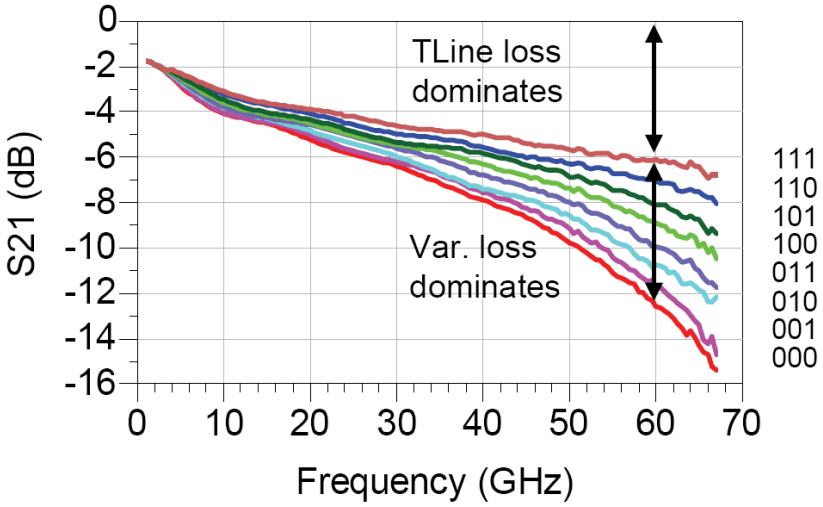


Figure 5.11: The measured insertion loss of 8 different phase states over frequency.

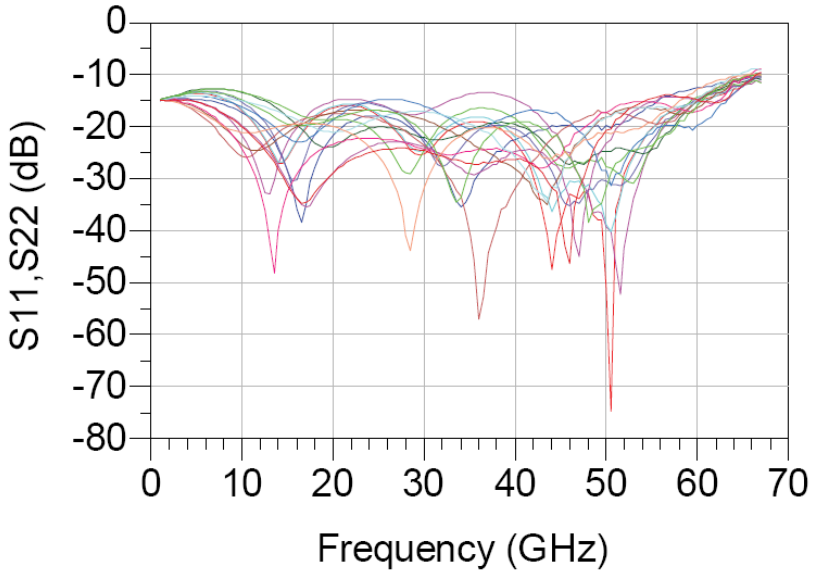


Figure 5.12: The measured return loss of 8 different phase states over frequency.

5.2 Measurement Results

The phase shifter is implemented in a 65nm CMOS technology and occupies an active area of 0.2mm^2. Figure 5.7 shows the photograph of the phase shifter. Open and short de-embedding structures are used to correct for the bondpad and ESD parasitics. The total chip area is 1mm^2.

Figure 5.8 shows the measured insertion phase [phase(S21)] of the 8 different phase states over frequency. At 60GHz the phase resolution is 22^o and the phase control range is 156^o. The RMS phase error of the 8 phase states is less than 9.2^o, as compared to an ideal 4-bit phase shifter, for all the frequencies from 50 to 65GHz.

Figure 5.9 shows the relative phase shift of the 8 different phase states referred to state 000 ($N_2 = N_1 = N_0 = 0$). The phase shifter provides an almost linear phase shift from 1 to 67GHz. With the differential paths swapped to provide another 180^o phase step, we achieve 16 different phase states as shown in Figure 5.10.

Figure 5.11 shows the measured insertion loss [dB(S21)] of the 8 different phase states over frequency. The insertion loss is within 9.4±3.1dB over the 8 phase states at 60GHz. The loss variation is due to the low Q and large capacitance of a varactor when the DC control voltage is low (as shown in Figure 5.4). The average insertion loss is between 8.5dB and 10.3dB from 55 to 65GHz. Variable gain amplifiers can be used in each RF path to equalize the loss variation of the phase shifters and avoid array pattern degradation.

Figure 5.12 shows the measured input and output return loss of the phase shifter, which are better than 10dB from 55 to 65GHz.

In Table 5.1, the key results of this work are summarized and compared with other published passive [48, 49, 52, 57] and active [53–55, 57] phase shifters in compound semiconductors and silicon. The phase shifter presented in this work has a low insertion loss (among passive phase shifters) and a high phase resolution at 60GHz.

Table 5.1: Benchmark of mm-wave phase shifters

Ref.	Freq. [GHz]	Phase range/step [°]	Gain [dB]	DC power [mW]	Tech.
This work	60	180 diff./22.5	-9.4	Passive ~0	65nm CMOS
[49]	5.5	360/analog	-3.9	Passive ~0	0.6μm GaAs MESFET
[52]	12	360/11.25	-14.5	Passive ~0	0.18μm CMOS
[48]	34	360/22.5	-13.1	Passive ~0	0.15μm GaAs HJFET
[54]	12	360/22.5	3.5	Active 26.6	0.18μm CMOS
[55]	26	360/22.5	-3	Active 12	0.13μm CMOS
[53]	34	360/22.5	1	Active 5.4	0.12μm SiGe BiCMOS
[57][1]	60	180/analog (+DAC)	-7	Passive ~0	0.13μm SiGe BiCMOS
[57][1]	60	360/analog (+DAC)	-2	Active 32	0.13μm SiGe BiCMOS

[1] Published later than this work [60].

5.3 Conclusion

A 60GHz 4-bit passive phase shifter has been implemented in a 65nm CMOS technology. It is based on a differential varactor-loaded transmission line architecture, which consists of a differential transmission line loaded with a differential MOS varactor at each side.

The 60GHz passive phase shifter achieves low cost, simple design, low insertion loss and small phase-shift step size (22.5^{o}). The loss (variation) of this passive phase shifter can be overcome using an extra (variable gain) amplifier stage at the cost of chip area and power consumption. On the other hand, an active phase shifter with less insertion loss (or even some gain) and less variations in loss will also be of interest. In the next two chapters, we will present a 60GHz vector-modulator based active phase shifter and its integration with a low-noise amplifier (LNA) and a power amplifier (PA) for 60GHz phased arrays.

6

A 60GHz Active Phase Shifter Integrated with LNA

This chapter presents a 4-bit active RF phase shifter that is based on programmable weighted combinations of I/Q paths with digitally controlled variable gain amplifiers (VGAs). Compared to the passive designs [53, 57, 60, 62, 63], this phase shifter achieves high gain, small area, large phase shift range (360^o) and small phase-shift step size (22.5^o). Instead of using an all-pass polyphase filter [55, 59] or quadrature coupler [57], the I/Q signals are generated using a 90^o transmission line that enables low loss and sufficient I/Q accuracy. The gain settings of the VGAs are achieved through digitally controlled current steering by turning on or off a certain number of unit transistors in parallel. The fully digitally controlled phase shifter allows for a simple control and better immunity to the noise in the control lines.

With the use of the 4-bit active RF phase shifter, this chapter describes the design of a 60GHz two-path receiver (Fig. 6.1) in which each path consists of an LNA, a phase shifter and part of a combiner, in a 65nm CMOS technology.

This chapter is organized as follows. The principle of the active RF phase shifter is discussed in Section 6.1. The design and implementation

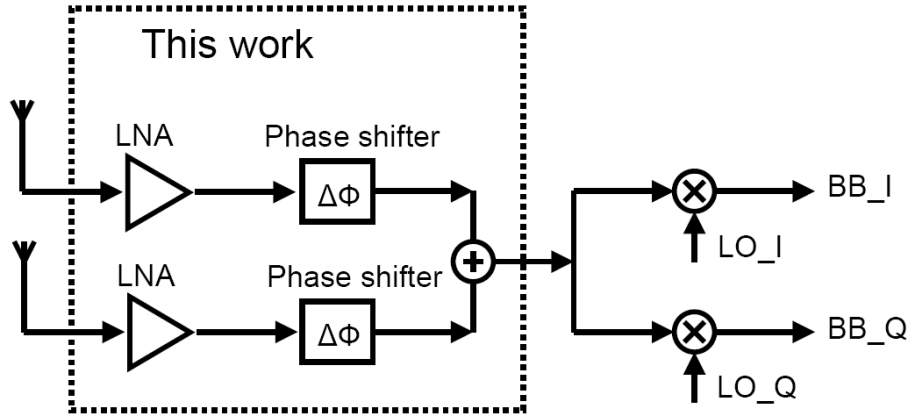


Figure 6.1: A 60GHz phased array receiver front-end using RF-path phase shifting.

of the RF phase shifter is presented in 6.2. Section 6.3 discusses the design of a 60GHz LNA and a 60GHz combiner. The measurement results of this receiver path are presented and discussed in Section 6.4. This chapter is published in [58, 61].

6.1 Principle of an Active RF Phase Shifter

The active RF phase shifter has a phase resolution of 22.5^{o} (4-bit resolution) and a phase control range of 360^{o}. The propagation time delay in a phased array system is approximated to a constant phase shift over the signal bandwidth, which may lead to distortion in a system that uses a broadband high order modulation scheme or uses an instantaneously wide bandwidth [44, 45]. System simulation shows that the use of a 4-bit constant phase shifter meets the requirements including error vector magnitude (EVM) and array patterns of a 60GHz 8-path phased array transceiver, which employs shaped QPSK modulation ($\beta = 0.5$) and has bit rates of 10Gbps (Section 3.5).

The active RF phase shifter has low insertion loss (or even gain) and low variation in loss. In this way, it is not required to implement an LNA or PA with very high gain, programmable gain settings, and large power

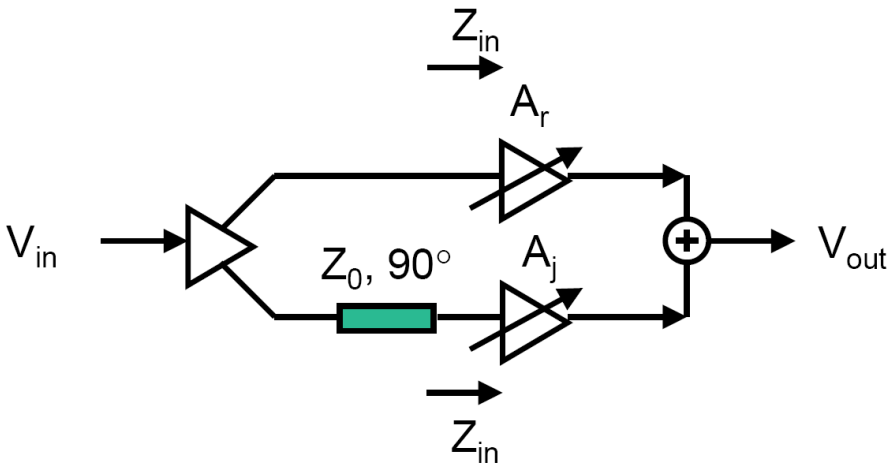


Figure 6.2: Block diagram of the active phase shifter.

dissipation in order to compensate the loss and loss variations. The phase shifter also requires sufficient linearity, because in the receiver path, the LNA and phase shifter may need to process the desired signals along with strong interferers, whereas beamforming and possible "nulling"of jammer are achieved after signal combining. In the transmitter path the phase shifter should not limit the linearity and output power of the transmitter.

Fig. 6.2 shows the block diagram of the active RF phase shifter. The input signal (V_{in}) is fed through two paths with or without a 90^o phase shift respectively, which generates I/Q signals. These I/Q signals are weighed by separate VGAs (A_r and A_j) and combined at the output (V_{out}). If the input impedance of each VGA (Z_{in}) is equal to the characteristic impedance (Z_0) of the transmission line, and if there are no gain and phase errors in the I/Q signals, the output signal of the phase shifter can be expressed as

$$V_{out} = (A_r + jA_j)V_{in} \tag{6.1}$$

The phase shift achieved is given by

$$\phi = \arctan(A_j/A_r) \tag{6.2}$$

The gain of the phase shifter can be expressed as

$$A = \sqrt{A_r^2 + A_j^2} \tag{6.3}$$

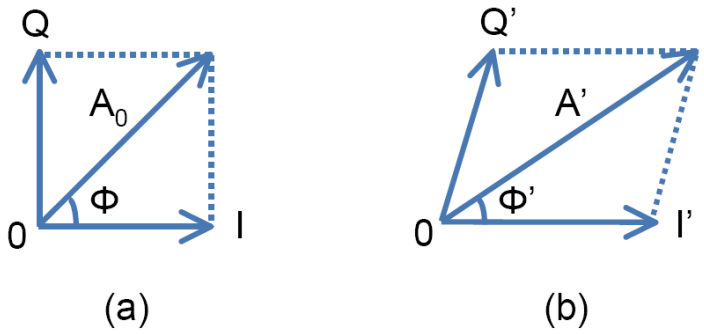


Figure 6.3: Phase shift achieved with (a) ideally weighted I/Q signals; and (b) gain and phase errors in the weighted I/Q signals.

Here A_r and A_j are the gains of the two VGAs in the I/Q paths respectively, which are given by

$$A_r = A_0 \cos(\phi) \tag{6.4}$$
$$A_j = A_0 \sin(\phi) \tag{6.5}$$

in which ϕ is the desired phase shift, and A_0 is a constant representing the gain of the phase shifter. In this way, the phase shifter achieves a phase shift of ϕ with a constant gain of A_0, as shown in Fig. 6.3(a).

However, there are often gain and phase errors in the weighted I/Q signals before signal combination, which result in gain and phase error in the desired phase shift [Fig. 6.3(b)]. This is because, firstly, the 90^o transmission line itself has gain and phase errors. Secondly, there can be impedance mismatch (and therefore reflection) between the input impedance of each VGA (Z_{in}) and the transmission line (Z_0). In the 60GHz broadband system this impedance mismatch is often more severe, as compared to that at lower frequencies, due to the variation of impedance (Z_{in} and Z_0) within the broad band of interest. Thirdly, gain and phase errors can also be contributed by the weighting of the two VGAs. If we model the overall gain errors and phase errors in the weighted I/Q signals as ε and θ respectively,

the output signal (V_{out}) of the phase shifter can be expressed as

$$\begin{aligned} V_{out} &= [A_r + A_j(1-\varepsilon)e^{j(\frac{\pi}{2}-\theta)}]V_{in} \\ &\approx [(A_r + \theta A_j) + jA_j(1-\varepsilon)]V_{in} \\ &= [\cos(\phi) + \theta\sin(\phi) + j\sin(\phi)(1-\varepsilon)]A_0 V_{in} \end{aligned} \tag{6.6}$$

The phase shift achieved due to the gain and phase errors in the weighted I/Q signals is given by

$$\phi' = \arctan\frac{\sin(\phi)(1-\varepsilon)}{\cos(\phi) + \theta\sin(\phi)} \tag{6.7}$$

As compared to the ideal phase shift in Equation (6.2), the phase error of the phase shifter due to the gain and phase errors in the weighted I/Q signals can be written as

$$\begin{aligned} \Delta\phi &= \phi' - \phi \\ &= \arctan[\frac{-\frac{\theta}{2} - \frac{\varepsilon}{2}\sin(2\phi) + \frac{\theta}{2}\cos(2\phi)}{1 - \frac{\varepsilon}{2} + \frac{\theta}{2}\sin(2\phi) + \frac{\varepsilon}{2}\cos(2\phi)}] \\ &\approx -\frac{\theta}{2} - \frac{\varepsilon}{2}\sin(2\phi) + \frac{\theta}{2}\cos(2\phi) \end{aligned} \tag{6.8}$$

The RMS phase errors (in radians) of the phase shifter [29], as compared to an ideal phase shifter, can be expressed as

$$\begin{aligned} \Delta\phi_{RMS} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(\phi' - \phi)^2 d\phi} \\ &\approx \sqrt{\frac{3}{8}\theta^2 + \frac{1}{8}\varepsilon^2} \end{aligned} \tag{6.9}$$

The gain of the phase shifter with the gain and phase errors in the weighted I/Q signals is given by

$$\begin{aligned} A' &= A_0\sqrt{(\cos(\phi) + \theta\sin(\phi))^2 + \sin^2(\phi)(1-\varepsilon)^2} \\ &\approx A_0\sqrt{1 - \varepsilon + \theta\sin(2\phi) + \varepsilon\cos(2\phi)} \end{aligned} \tag{6.10}$$

As compared to an ideal phase shifter, the RMS gain errors (in dBs) [29] of the phase shifter can be expressed as

$$\begin{aligned}\Delta A_{RMS,dB} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(A'_{dB}-A_{0,dB})^2 d\phi} \\ &\approx 8.7\sqrt{\frac{1}{8}\theta^2+\frac{3}{8}\varepsilon^2}\end{aligned} \tag{6.11}$$

From Equation (6.9) and (6.11), for example, in order to design a 4-bit phase shifter with RMS gain and phase errors of less than 1.7dB and 11.25^o respectively, we should have $\varepsilon \leqslant 0.28$ and $\theta \leqslant 0.28$. In other words, in comparison to an ideal phase shifter with perfect I/Q signal generation and weighting, the gain and phase errors in the weighted I/Q signals before signal combination should be less than 2.8dB and 16^o respectively. It is worth pointing out that a 90^o transmission line contributes less than 9^o phase error within 20% bandwidth at 60GHz. Therefore, it is used to generate the broadband I/Q signals at the 60GHz band. The transmission line structure and its measurement results are presented in Fig. 5.5a and Fig. 5.5b. A 90^o transmission line has a width of 36um, a total length of 650μm and an measured insertion loss of 0.7dB at 60GHz.

In order to generate 4-bit phase shifts (Fig. 6.4), the gain ratio of the two VGAs in the I/Q paths (A_j/A_r) is programmed in certain discrete settings such as $0/3$, $1/3$, $2/2$, $3/1$ or $3/0$, in this way the phase shift can vary between 0^o to 90^o in a step of approximately 22.5^o. By changing the polarity of A_r and A_j independently, a phase control range of 360^o can be achieved, which can be done by swapping the positive and negative paths in the differential circuits of the two VGAs. Note that the gain ratio settings of A_j/A_r are set to $1/3$ or $3/1$ in order to achieve phase shift of 22.5^o or 67.5^o, since these ratio settings are simpler to be implemented than the exact gain ratios of $1/2.4$ or $2.4/1$ for these phase shifts. The resulting gain and phase errors in the phase shifter due to these simplified gain ratio settings are well acceptable for this application (as it needs antenna gain but no interferer nulling). As compared to an ideal 4-bit phase shifter, this phase shifter achieves a peak gain error of less than ±0.5dB and a peak phase error of less than 4^o for the different phase settings in simulation, when used in combination with ideal I/Q signals. The phase shifter can

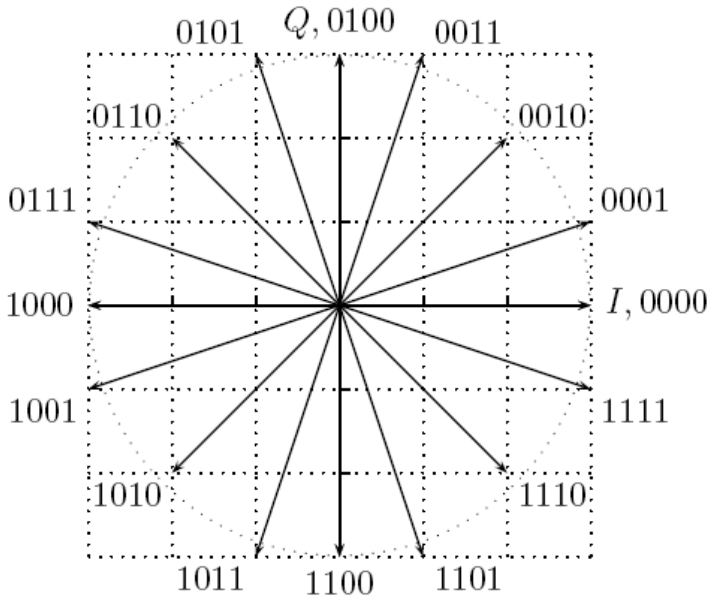


Figure 6.4: Generating the 360° phase shifts in 22.5° steps by programmable weighted combinations of I and Q signals in discrete settings.

be extended to achieve higher phase resolution, for example, 5-bit, by programming A_j/A_r in more discrete settings.

6.2 Design of an Active RF Phase Shifter

Fig. 6.5 shows the schematic of the active RF phase shifter for a receiver. The input transconductance stage, 90° line and two digitally controlled VGAs are merged in a common-source cascode configuration for low power, high gain and stability considerations. The input transconductance stage (M1-M4) converts the signal (V_{in+} and V_{in-}) into separate currents. I/Q signals are generated by feeding these currents through two paths with and without a 90° transmission line respectively. Two digitally controlled VGAs weigh these I/Q signals separately and generate the required phase at the combined output (V_{out+} and V_{out-}). The shunt transmission

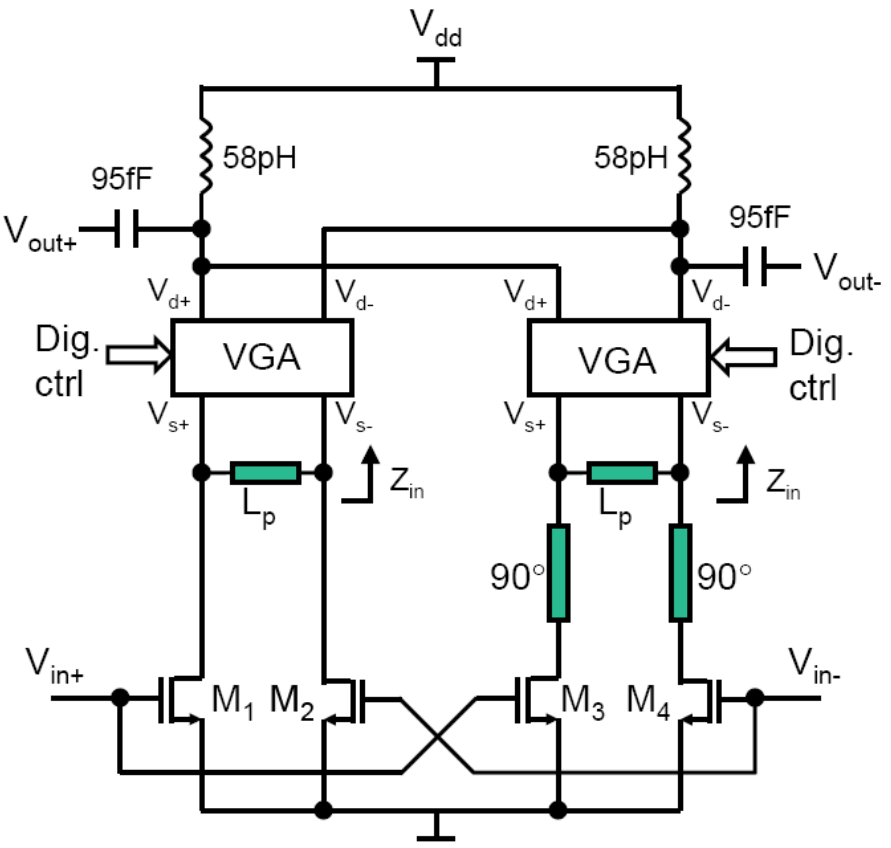


Figure 6.5: Schematic of a 60GHz 4-bit phase shifter in the receiver.

line (L_p) cancels the impedance contributed by the input capacitance of the VGA at 60GHz. The real part of the input impedance of each VGA (Z_{in}) is chosen to be equal to the characteristic impedance of the 90^o transmission line (Z_0).

The VGAs in the phase shifter are implemented using a common-gate configuration as shown in Fig. 6.6. The gain is programmed by switching on or off a certain number of unit transistors, which are connected to V_{out+} ,V_{out-} or V_{dd} respectively. The connections of these transistors are based on the digital control at their gates. In this way, the desired portion of the input currents of each VGA is diverted to the output, while the remaining portion is fed into the supply. For example, if $1/4$ of the input current of the

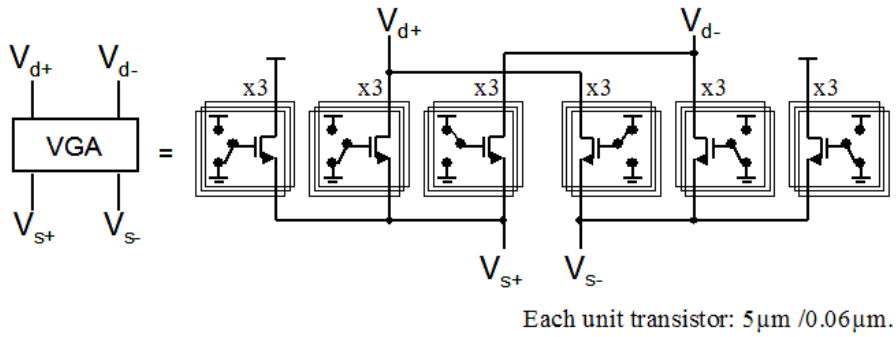


Figure 6.6: Schematic of a VGA in the phase shifter of the receiver.

I-path VGA and $3/4$ of the input current of the Q-path VGA are diverted to the output, the gain ratio of the two VGAs (A_j/A_r) is $3/1$; therefore, the phase shift achieved is approximately 67.5^o. By programming A_j/A_r to $0/3$, $1/3$, $2/2$, $3/1$ or $3/0$ as well as changing the polarity of A_r and A_j, the phase shifter achieves a phase control range of 360^o in steps of approximately 22.5^o. This current steering approach provides a phase shift that is in the first order insensitive to the variations in technology, supply voltage and temperature (PVT), since the phase shift is set by the gain ratio and therefore the number of unit transistors that connects to the output of the two VGAs. Moreover, by using the dummy transistors that connect to V_{dd}, the total number of unit transistors switched on is constant. In this way, the variations of the VGA input impedance are minimized, which provides the broadband load impedance required at the output of the 90^o transmission line.

In simulation, the active RF phase shifter in the receiver (Fig. 6.5) has an average insertion gain of 0dB, an output P_{1dB} of -9dBm at 60GHz and consumes 19.5mW.

6.3 Design of an LNA and a Combiner

Thanks to the active RF phase shifter with low loss, the requirements of the LNA are low noise figure, reasonable gain and low power consumption. The two-stage differential LNA is shown in Fig. 6.7. The common-

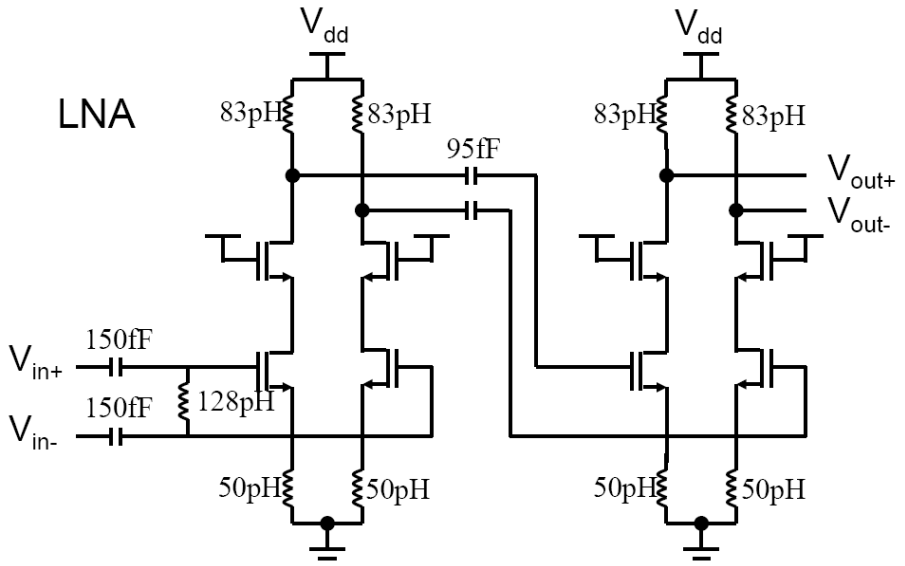


Figure 6.7: Schematic of a 60GHz LNA.

source cascode configuration offers low noise, high gain and stability. The input of the LNA is matched to 100Ω differential antennas [64]. There is inductive degeneration at the source of the input transistors to provide broadband power and noise matching. Measured results (Fig. 6.8) show that a stand-alone LNA has a measured minimum noise figure of 5.5dB and a power gain of 8.4dB at 61GHz. The 3dB-bandwidth is 10.4GHz. The LNA consumes 39mW.

The combiner that follows the phase shifters is shown in Fig. 6.9. The RF signals from two antenna paths are fed into two common-source cascode amplifiers. Subsequently, the signals are combined at the outputs of these amplifiers. The output of the combiner is matched to 100Ω differentially for measurement purposes. The common-source cascode configuration provides isolation between two antenna paths. It achieves a simulated insertion gain of 4dB (from V_{in1} or V_{in2} to V_{out}) at 60GHz and consumes 19.5mW. This implementation of power combiner has a higher gain than a passive power combiner (such as a Wilkinson power combiner [29]). It is worth pointing out that by connecting more amplifiers in parallel, this combining method can be scaled to more paths (Fig. 6.10a). However,

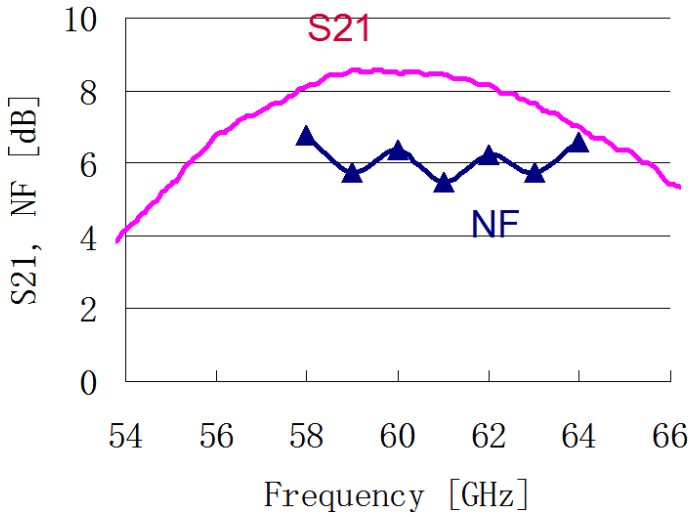


Figure 6.8: Measured performance of a stand-alone LNA.

for a large number of paths, the output impedance of the combiner may be reduced significantly. Therefore, it becomes difficult to drive the load impedance of the combiner (i.e. the input impedance of the mixer). The loading problem can be solved by using multiple combiner stages in a tree-structure to combine a large number of paths while maintaining sufficient output impedance (Fig. 6.10b) [27].

The spiral inductors in this work use the top-two metal layers (metal-7 and metal-6) as signal paths, the bottom metal layer (metal-1) as a patterned ground shield, and are implemented using single-turn differential inductors with center tap. Simulations using the LSIM 3.1 tool [65] show that the quality factors of the inductors are higher than 20 at 60GHz, thanks to the thickness of metal-7 and metal-6 (0.9μm each). The capacitors are implemented using the intermediate metal layers stacking from metal-2 to 5, with minimum-spacing interdigitated fingers fringe capacitor configuration. Metal-1 is not used due to the significant parasitics to the substrate, whereas metal-6 and metal-7 are not used because of the larger spacing required in these two layers. In the simulation, the capacitors have quality

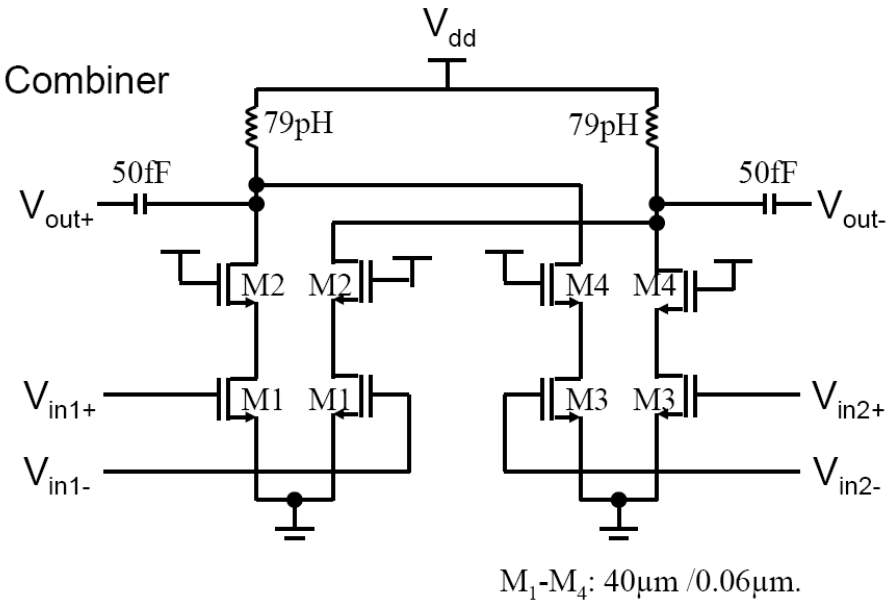


Figure 6.9: Schematic of a 60GHz combiner.

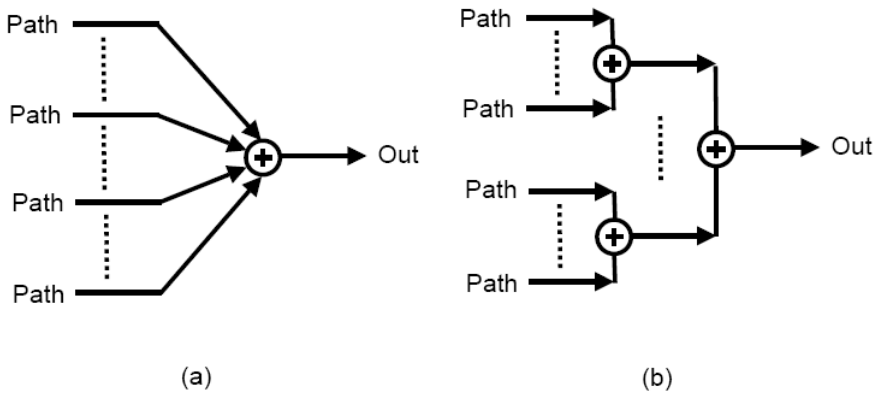


Figure 6.10: Signal combining method by using (a) parallel combination; and (b) tree-structure combination

factors of around 10 at 60GHz.

To achieve optimal noise figure and power gain, the finger width of the MOS transistors is chosen to be 1μm and the DC current density is approximately 0.15mA per μm-gate-width. Wideband matching networks are adopted in order to provide broadband performance with low sensitivity to modeling inaccuracies and process variations. Extensive parasitic extractions have been performed on the layouts and taken into account during the circuit simulation. Long on-chip interconnect lines are implemented as transmission lines. The supply voltage in the receiver path is 1.5V in order to provide voltage headroom in the cascode topologies. Since the gates of the cascode transistors are all connected to 1.5V, within the 1dB compression point the voltage swings at the inductive loads are less than the threshold voltage (V_{TH}) of the transistors. The cascode structures help to reduce the voltage stress on each transistor well below the specified breakdown voltage, although special attention is needed when the product is powered down.

6.4 Measurement Results

As shown in Fig. 6.1, a two-path 60GHz receiver is implemented in a 65nm CMOS technology, in which each path consists of an LNA, a 4-bit RF phase shifter and part of a combiner (a common-source cascode amplifier). Each phase shifter is controlled independently using digital inputs that are loaded to the phase shifter by a serial peripheral interface (SPI). Fig. 6.11 shows the die photo. The die area is 1.6mm^2 and the active circuit occupies 0.9 mm^2. The layout is symmetrical between the two receiver paths.

Each receiver path consumes 52mA from a 1.5V supply, in which the LNA, phase shifter and part of a combiner consume 26mA, 13mA and 13mA respectively.

Fig. 6.12 shows the measured noise figure of one receiver path for 16 digitally controlled phase settings. The noise figure is between 6.7 to 7.2dB across all phase settings at 61GHz, which is mainly contributed by the LNA with a measured noise figure of 5.5dB.

The measured insertion phase [phase(S21)] of one receiver path for 16

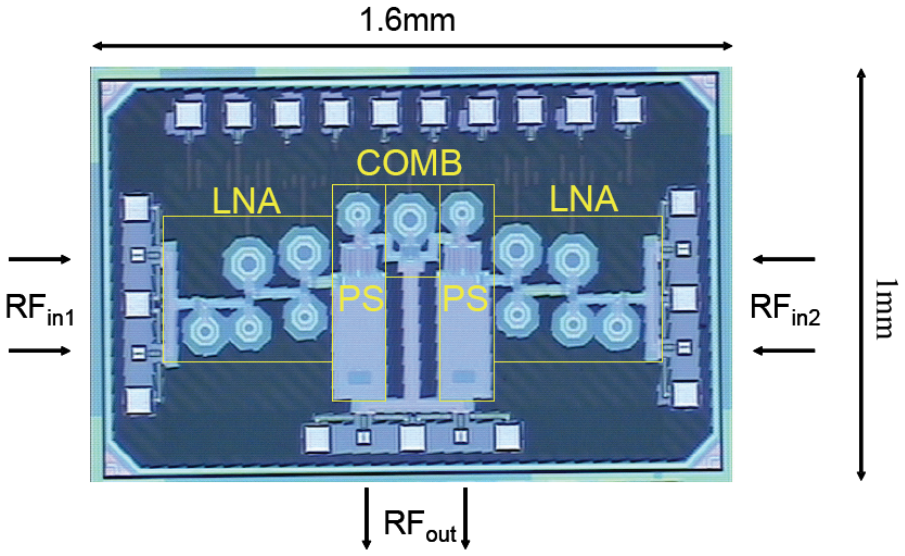


Figure 6.11: Chip photo of a two-path 60GHz receiver in which each path consists of an LNA, a phase shifter and part of a combiner.

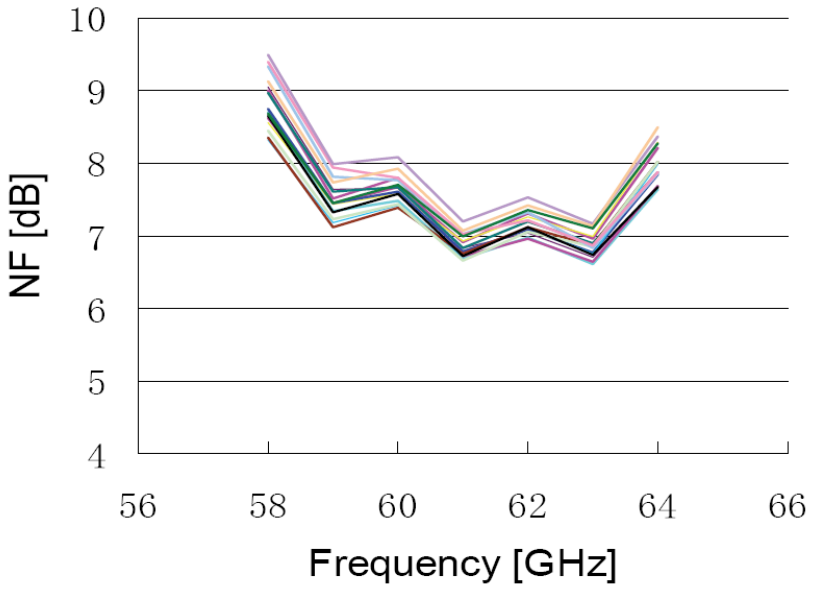


Figure 6.12: Measured noise figure of one receiver path for 16 phase settings.

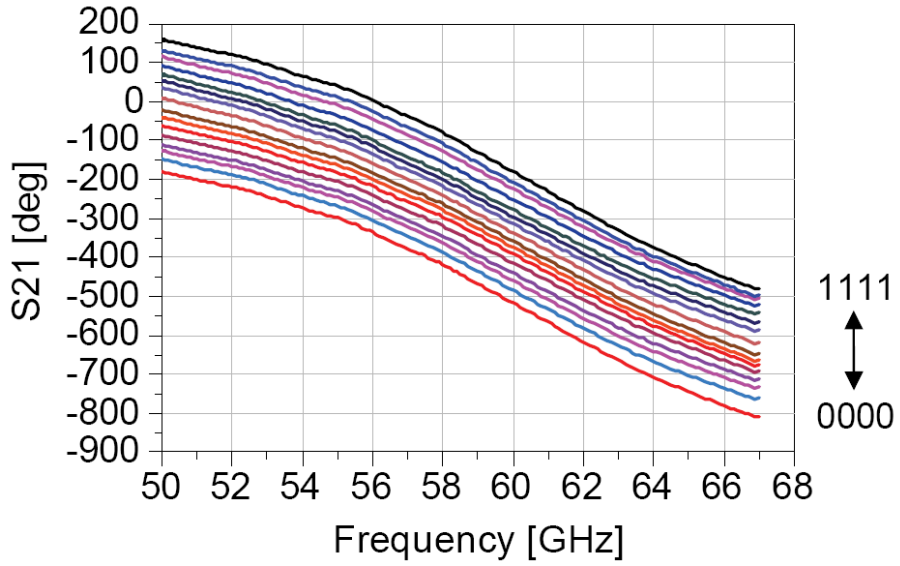


Figure 6.13: Measured insertion phase of one receiver path for 16 phase settings.

phase settings is depicted in Fig. 6.13. The phase step is approximately 22.5^{o} (4-bit resolution) and the phase control range is 360^{o} in the 60GHz band.

Fig. 6.14 highlights the relative phase shifts of one receiver path for 16 phase settings by setting the phase state 0000 as a reference. This shows that the 4-bit phase shifts achieved are relatively constant over a wide frequency range, which is due to the broadband I/Q signal generation and the frequency insensitive gain ratio of the two VGAs that weigh these I/Q signals.

Fig. 6.15 presents the measured insertion gain [dB(S21)], input and output return loss [dB(S11) and dB(S22)] of one receiver path for 16 phase settings. At the center frequency of 61GHz, the average insertion gain is 12dB, and the peak-to-peak gain variation is 3.4dB across all phase settings. The 3dB bandwidth is 5.5GHz. This insertion gain is contributed separately by the LNA that has measured gain of 8.6dB, the part of the combiner that has a simulated gain of 4dB, and the phase shifter that has a simulated average gain of 0dB. The measured S11 and S22 of one receiver

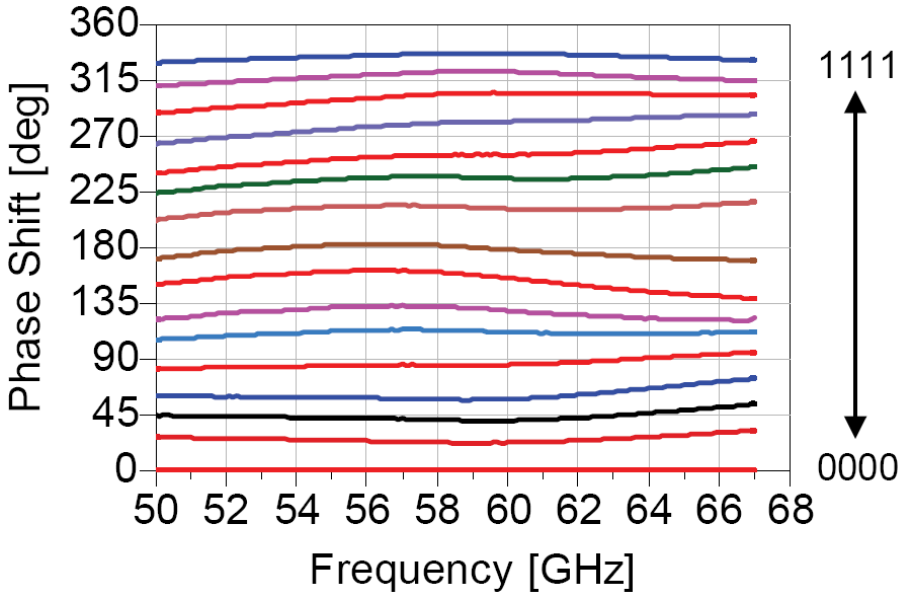


Figure 6.14: Measured relative phase shift of one receiver path for 16 phase settings.

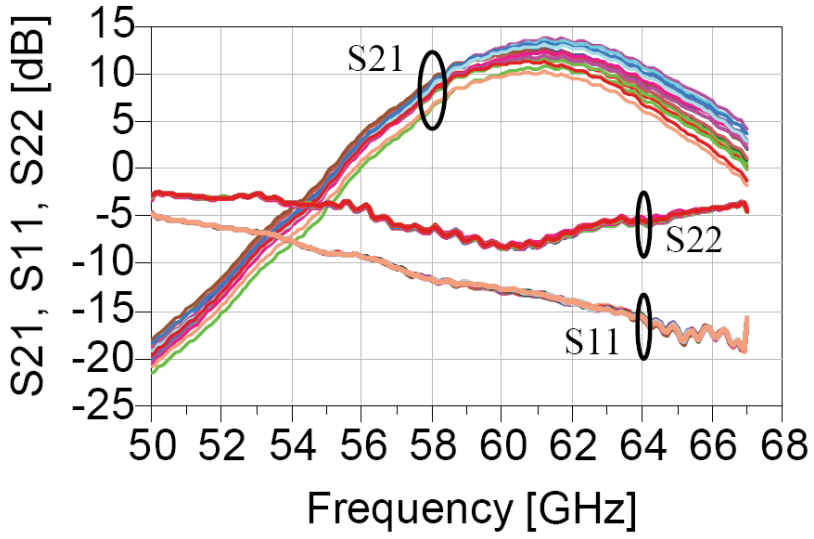
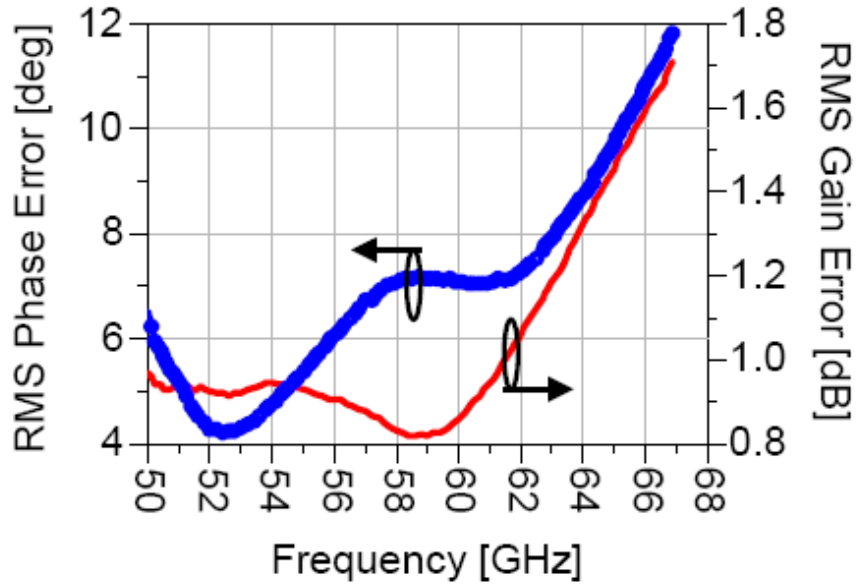
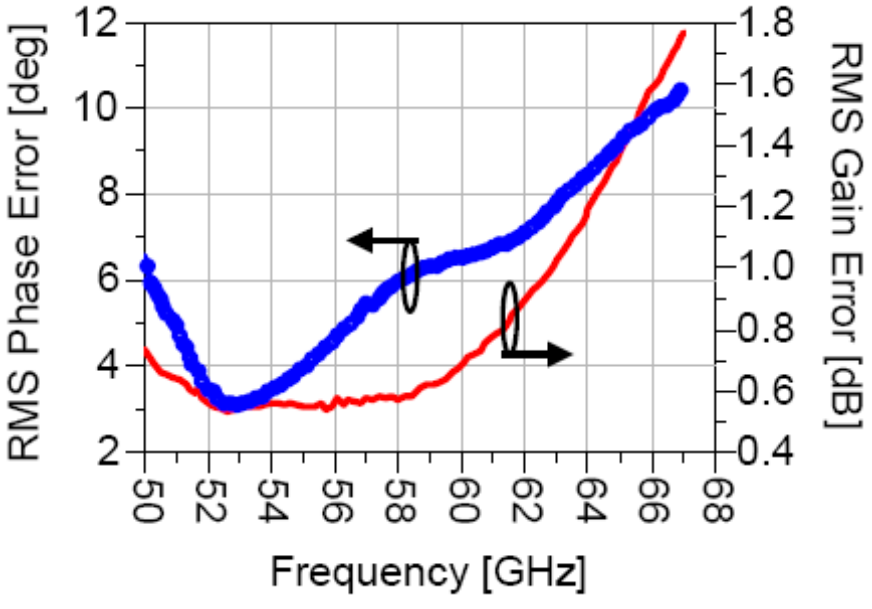


Figure 6.15: Measured insertion gain, input and output matching of one receiver path for 16 phase settings.



(a)



(b)

Figure 6.16: Measured RMS gain and phase errors: (a) of the 16 phase states; (b) of the I and Q signals as compared to an ideal 4-bit phase shifter

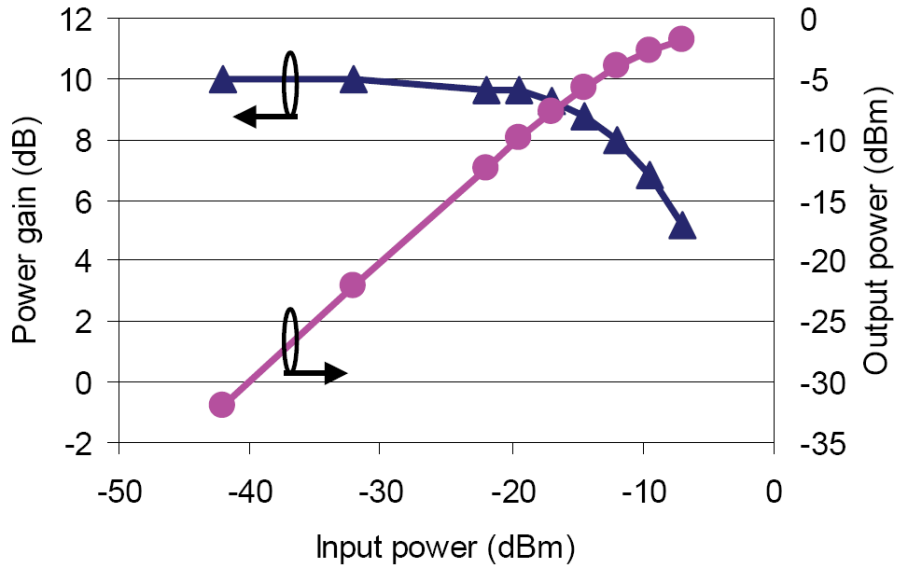


Figure 6.17: Measured power gain and output power of one receiver path at 61GHz versus the RF input power.

path for 16 phase settings are -13dB and -8dB respectively at 61GHz, which are determined by the input matching of the LNA and the output matching of the combiner separately and do not change for different phase settings.

Derived from the measured insertion gain and phase shifts, Fig. 6.16a shows the RMS gain and phase errors of the 16 phase states. They are 0.9dB and 7° at 61GHz respectively, as compared to an ideal 4-bit phase shifter with a uniform gain. As highlighted in Fig. 6.16b, the RMS gain and phase errors of the I/Q signals, which are measured indirectly using phase state 0°, 90°, 180° and 270°, are 0.8dB and 6.8° respectively at 61GHz. These frequency dependent gain and phase errors are contributed by the 90° transmission line, the impedance mismatch between the input of each VGA (Z_{in}) and the transmission line (Z_0), as well as the layout mismatch in the pseudo-differential paths.

Fig. 6.17 shows the measured non-linearity of one receiver path. The power gain and output power are plotted as a function of the RF input power at 61GHz. The measured input referred P_{1dB} of one receiver path

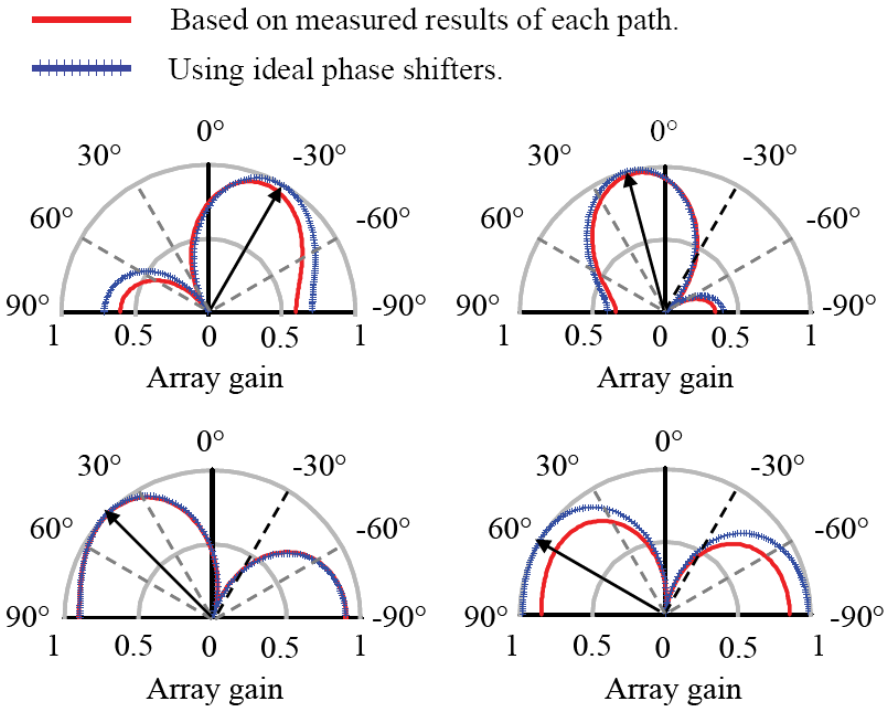


Figure 6.18: Simulated normalized 2-path beam patterns of the receiver (e.g. for an angle of arrival of -60^o, -30^o, 0^o or 45^o) constructed from the measured performance of each path.

is observed to be -16dBm at 61GHz. This P_{1dB} is limited by the input transconductance stages of the phase shifter and can be improved by e.g. source degeneration, at the cost of reduced gain and/or increased power consumption.

The measured isolation between the two input ports of the receiver is -43dB, thanks to the pseudo-differential cascode topologies with differential inductors used in the LNA, phase shifter and combiner.

The mismatches of the two receiver paths are measured through two-port S-parameter measurements in either of the two paths over different phase settings. By comparing the S-parameters of the two paths for the same phase settings, the insertion gain and phase mismatches of the two paths are quantified as RMS gain mismatch and RMS phase mismatch [29]. The measured RMS gain and phase mismatch of the two paths are 0.4dB and 2.1^{o} respectively at 61GHz. Since the layout of the two receiver paths are symmetrical to each other, these mismatch results can be contributed by the measurement inaccuracies (brought by probe placement and cable stability when measuring one of the two paths at a time), as well as process mismatch, temperature variation, etc.

Fig. 6.18 shows the simulated normalized 2-path beam patterns e.g. for angle of arrival (θ) of -30^{o}, 15^{o}, 45^{o} or 60^{o} at 60GHz. These patterns are constructed in ADS from the measured insertion gain and phase shift of each receiver path for various phase settings. The simulation assumes that a linear array of isotropic antennas are used without mutual coupling, that the antenna spacing is $\lambda/2$ at 61GHz, and that the lengths of the interconnects from the antennas to each path are equal [28, 29]. In the ideal case, each receiver path is assumed to have a uniform gain of 12dB (the measured average power gain of each path) and infinite phase resolution, and the first and second path use a phase shift of 0 and $180^{o}\times\sin(\theta)$ respectively. In the measurement cases, the phase required in each path is digitized to the nearest measured 4-bit phase states, and the corresponding insertion gain and phase shift are used. The beam patterns constructed from measured results are very close to the ideal patterns: the beam directions are almost the same, and the peak array gain has less than 1.2dB difference in the worst case. This is due to the very low RMS gain and phase errors in the 16 phase settings. The RMS gain and phase errors rather than the peak-to-peak errors of each path are more relevant in the beam patterns

especially when using a large number of antennas, since there are typically different phase settings in the different antenna paths. Therefore, the gain and phase errors of the different antenna paths average out.

Table 6.1 summarizes the measured performance of the receiver path in comparison with reported mm-wave RF-path phase shifting receivers.

Table 6.1: Benchmark of mm-wave RF-path phase shifting receivers

Spec.	[59]	[57]	[28]	[66][1]	This work
Frequency (GHz)	77	60	60	60	61
Phase shifting @	RF	RF	RF	RF	RF
Number of paths	1	1	4	16	2
Key building blocks	LNA, phase shifter	phase shifter	LNA, phase shifter, combiner	LNA, phase shifter, combiner, mixer, frequency synthesizer, etc.	LNA, phase shifter, combiner
Power Gain of each path (dB)	≤ 17	-2	≥ 8	72 (max @baseband)	12 (average)
Phase shift step (^{o})	Analog (+DAC)	Analog (+DAC)	Analog	Digital, 11	Digital, 22.5
NF of each path (dB)	4 (LNA only)	17	≤ 6.9	7.4	≤ 7.2
Input P_{1dB} of each path (dBm)	-	-7	-33.5	-16 (@min gain)	-16
Power consumption (mW)	128 (1 path)	32 (1 path)	265 (4 paths)	1800 (16 paths)	156 (2 paths)
Technology	0.13µm SiGe Bi-CMOS	0.13µm SiGe Bi-CMOS	0.12µm SiGe Bi-CMOS	0.12µm SiGe Bi-CMOS	65nm CMOS
Chip area (mm^2)	0.46	1.48	4.6	38	1.6

[1] Published later than this work [58].

6.5 Conclusion

This chapter presents the design of a 60GHz 4-bit active phase shifter and its integration with an LNA for phased array receivers. The operation of the active phase shifter is based on programmable weighted combinations of I/Q paths with digitally controlled variable gain amplifiers. The 60GHz 4-bit active phase shifter can be extended to operate in other mm-wave frequencies and/or achieve a different phase-shift step size.

With the use of the 4-bit active phase shifter, a 60GHz two-path receiver has been implemented. Each receiver path consists of an LNA, a phase shifter and part of a combiner. Expansion of two paths to more antenna paths is straightforward. Measurement results show that each receiver path achieves 7.2dB noise figure, a phase control range of 360^{o} in steps of approximately 22.5^{o}, an average insertion gain of 12dB at 61GHz, a 3dB-bandwidth of 5.5GHz and a power dissipation of 78mW. The 2-path beam patterns constructed from measured results are very close to the ideal patterns thanks to the low RMS gain and phase errors in the 16 phase settings.

7

A 60GHz Active Phase Shifter Integrated with PA

Power amplifiers (PA) are typically the most power hungry building blocks in RF transmitters. Achieving high output power and high efficiency is challenging at 60GHz due to the low gain and low breakdown voltage of the CMOS transistors and the loss of on-chip passive components. Thanks to the phased-array architecture that can increase the transmitter's effective isotropic radiated power (EIRP) through spatial power combining, the output power of an individual power amplifier is less critical.

This chapter presents the design of a 60GHz active phase shifter integrated with a PA in a 65nm CMOS technology for phased array transmitters. The one-path transmitter can be extended to multiple antenna paths.

This chapter is organized as follows. The design of a 60GHz active phase shifter for a transmitter is presented in Section 7.1. Section 7.2 discusses the design of a 60GHz power amplifier. The measurement results of the transmitter path are presented and discussed in Section 7.3. This chapter is published in [61].

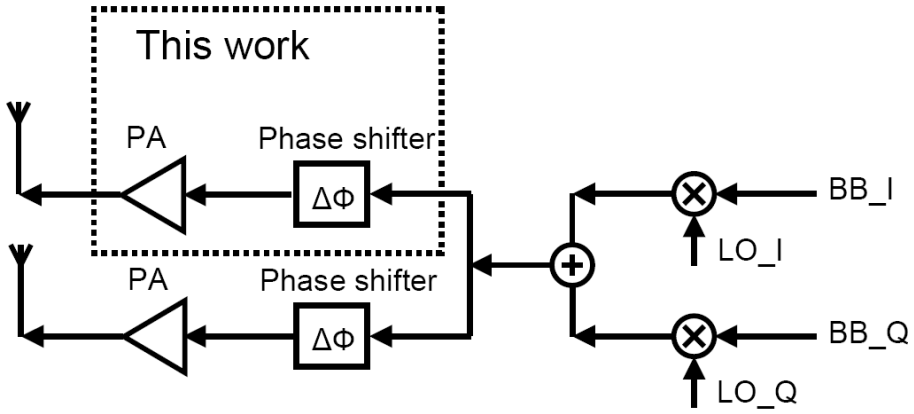


Figure 7.1: A 60GHz phased array transmitter front-end using RF-path phase shifting.

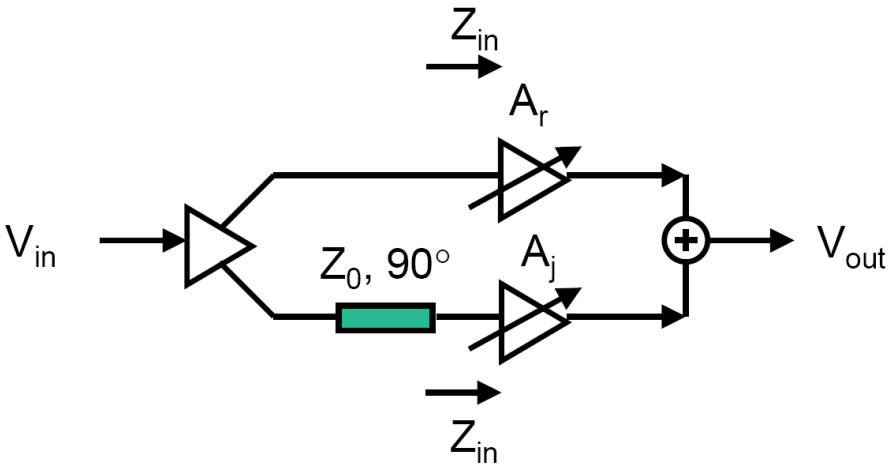


Figure 7.2: Block diagram of an active RF phase shifter.

7.1 Design of an Active RF Phase Shifter

The phase shifter in the transmitter has a high linearity requirement, so that it is the output stage of the power amplifier rather than the phase shifter that saturates first, otherwise the overall efficiency of the transmitter would be decreased.

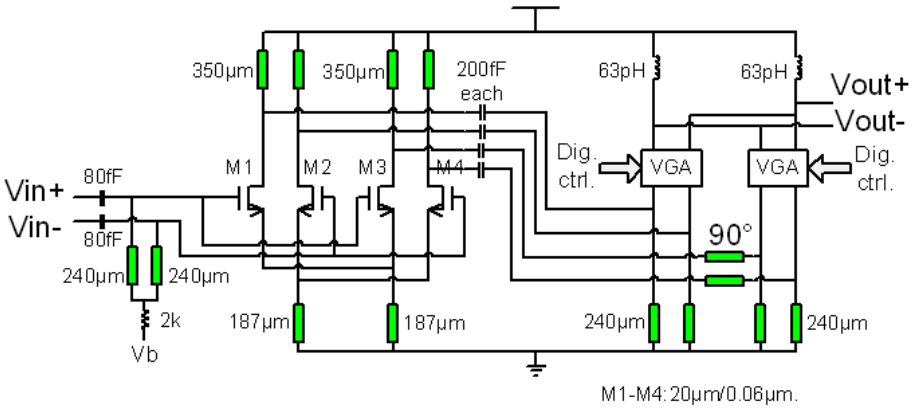


Figure 7.3: Schematic of a 60GHz 4-bit phase shifter in the transmitter.

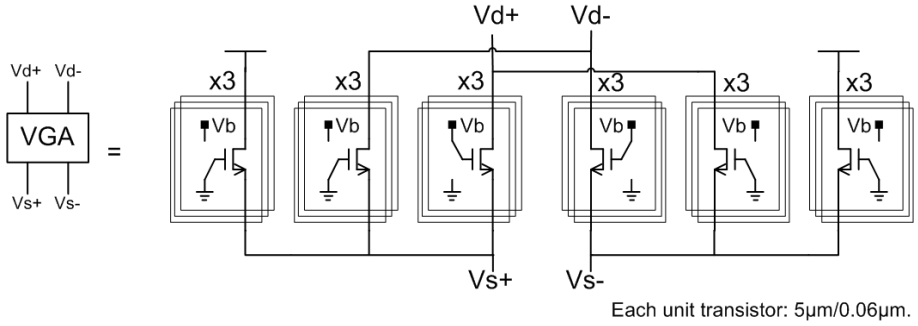


Figure 7.4: Schematic of a VGA in the phase shifter of the transmitter.

The phase shifter in the transmitter is based on programmable weighted combinations of I/Q paths with digitally controlled VGAs (Fig. 7.2). The schematic of the phase shifter is depicted in Fig. 7.3. Its operating principle is similar to that in the receiver (Fig. 6.5). The RF signal (V_{in+} and V_{in-}) is converted into separate currents by a transconductance stage (M1-M4). I and Q signals are generated by feeding these currents through two paths with or without a 90^o line, and weighted by the digitally controlled VGAs separately. The required phase is generated at the combined output (V_{out+} and V_{out-}).

As compared to the implementation in the receiver that merges the transconductance stage and the VGAs in a common-source cascode configuration, the phase shifter in the transmitter cascades the transconductance stage and the VGAs in two separate stages, in order to achieve a larger voltage swing and higher output P_{1dB}. Furthermore, there is inductive degeneration at the source of the input transconductance stage in order to provide input impedance matching (100Ω differentially) for measurement purposes.

The VGAs that are used in the phase shifter are shown in Fig. 7.4. They are similar to those in the receiver (Fig. 6.6) that program the gain by switching on or off a certain number of unit transistors. The only difference between the VGAs in the receiver and in the transmitter lies in the DC bias voltage at the gate of the transistors in order to work properly: in Fig. 7.4 the gate bias of each transistor is either V_b (DC bias voltage, which is 0.7V) or 0, instead of being either V_{dd} or 0 in Fig. 6.6.

In simulation, the active RF phase shifter (Fig. 7.3) in the transmitter achieves an average insertion gain of -6dB, an output P_{1dB} of -2dBm at 60GHz and a power consumption of 25mA from a 1.2V supply. It features a higher output P_{1dB} than that in the receiver. In this way, the power amplifier instead of the phase shifter limits the linearity of the transmitter. The insertion gain of the phase shifter is lower than that in the receiver, mainly because of its inductive source degeneration that achieves input matching for measurement purposes.

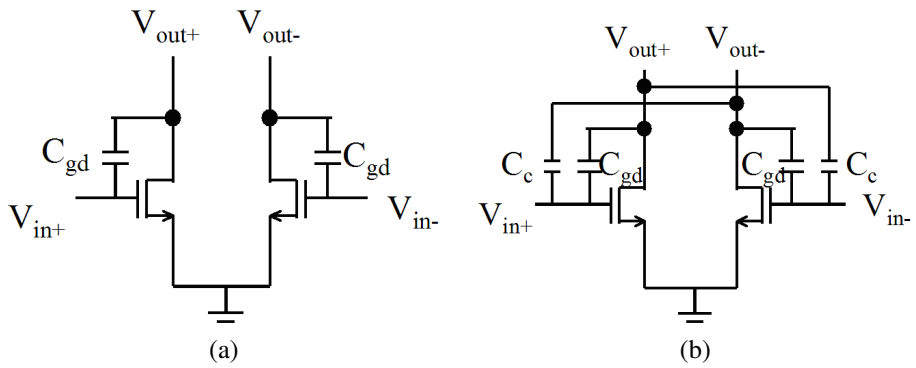


Figure 7.5: (a) A common-source amplifier with Miller capacitance and (b) compensating the Miller capacitance using cross-connected neutralization capacitors C_c.

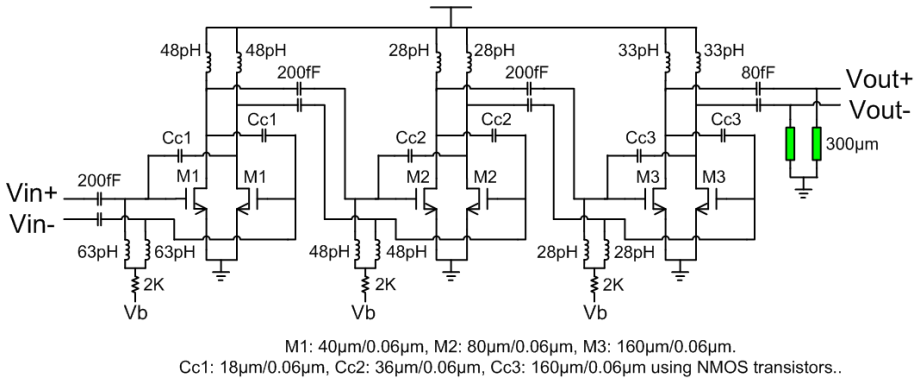


Figure 7.6: Schematic of a 60GHz 3-stage power amplifier.

7.2 Design of a Power Amplifier

Thanks to the phased array system that can increase the effective isotropic radiated power (EIRP) of a transmitter by spatial power combining, the output power of an individual power amplifier is less critical. On the other hand, if each individual power amplifier has a very low output power, a large number of antennas are required in order to achieve the desire EIRP. As a trade-off, the output power of each individual power amplifier is designed to be around +10dBm, as discussed in Section 3.1.

A power amplifier is often designed using a common-source or common-source cascode configuration. In a common-source configuration (Fig. 7.5a), the Miller capacitance (C_{gd}) reduces the gain, reverse isolation and stability. As a result, the common-source topology is conditionally stable, which is prone to instability because of the limited accuracy in the transistor model and in the matching network at this high frequency. A common-source cascode structure improves the devices stability but has the disadvantage of reduced voltage headroom and drain efficiency.

In this work, the Miller capacitance of a common-source configuration is compensated using neutralization capacitors (C_c) cross-connected between the drains and gates of the pseudo-differential transistors (Fig. 7.5b). As compared to a common-source cascode configuration, this common-source configuration provides a large output swing. The neutralization capacitors in this work use MOS transistors with the gate as one capacitor terminal and the drain and source connected together as the other capacitor terminal. By properly sizing the MOS transistors, these MOS-transistor based neutralization capacitors match the Miller capacitors of the common-source amplifiers and are less sensitive to the variations in PVT. In this way, the Miller effect is compensated and stability is ensured. This is an advantage compared to neutralization by the use of fixed parallel-plate metal capacitors as in [67].

Fig. 7.6 shows the schematic of a 60GHz three-stage power amplifier. The output of the power amplifier connects to 100Ω differential antennas [64], and the output matching network of the power amplifier is designed through a large-signal load-pull simulation to achieve a large output power and high power efficiency. The inductors at the drains and gates of the transistors connect to the supply voltage (V_{dd}) and bias voltage V_b respectively. These inductors, together with the series fringe capacitors and the shunt transmission line (300μm at the output), form the input, output and inter-stage matching networks. The total gate width of the transistors in each stage of the power amplifier doubles progressively, which ensures that the output stage saturates first if each stage has at least 3dB power gain. To achieve an optimal power gain performance, the gate finger width of the MOS transistors is chosen to be 1μm with gate contacts at both sides and the DC current density is approximately 0.2mA per μm-gate-width. In simulation, the power amplifier achieves an insertion gain of 15dB and a

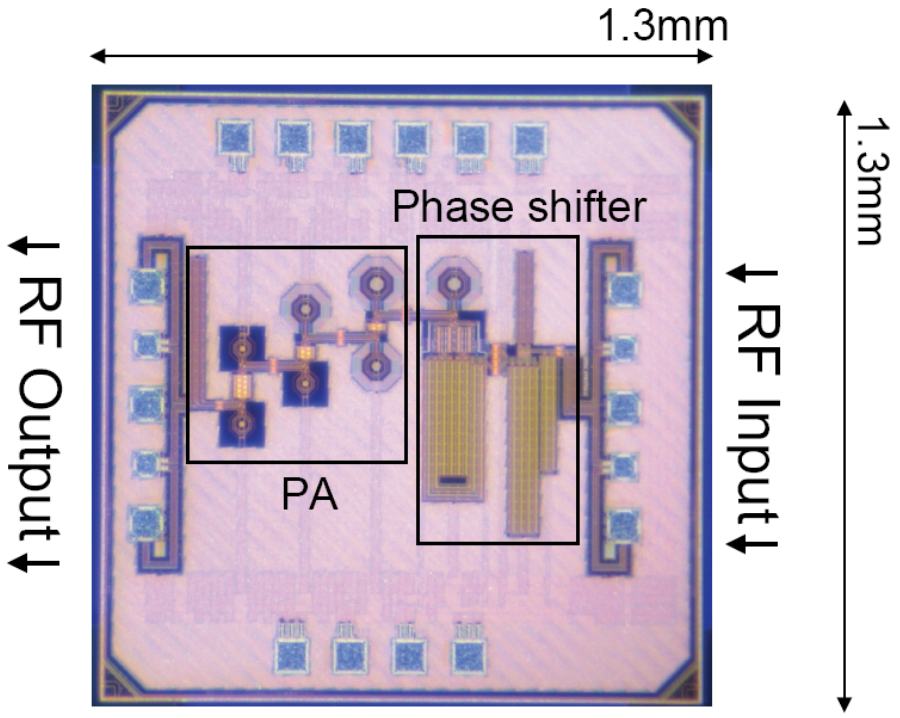


Figure 7.7: Chip photo of a 60GHz transmitter path that consists of a phase shifter and a PA.

maximum output power (P_{max}) of +11dBm at 60GHz.

7.3 Measurement Results

Consisting of a 4-bit active RF phase shifter and a power amplifier, a 60GHz transmitter path is implemented in a 65nm CMOS technology (Fig. 7.1). Expansion of one path to multiple antenna paths can be straightforward: the RF signal from a shared frequency up-converter is split, phase shifted, amplified and fed into the multiple antennas. Fig. 7.7 shows the chip photo. The chip area is 1.3mm*1.3mm and the active area is only 0.8mm*0.4mm. The transmitter path draws 140mA from a 1.2V supply, in which the phase shifter and PA draws 25mA and 115mA respectively.

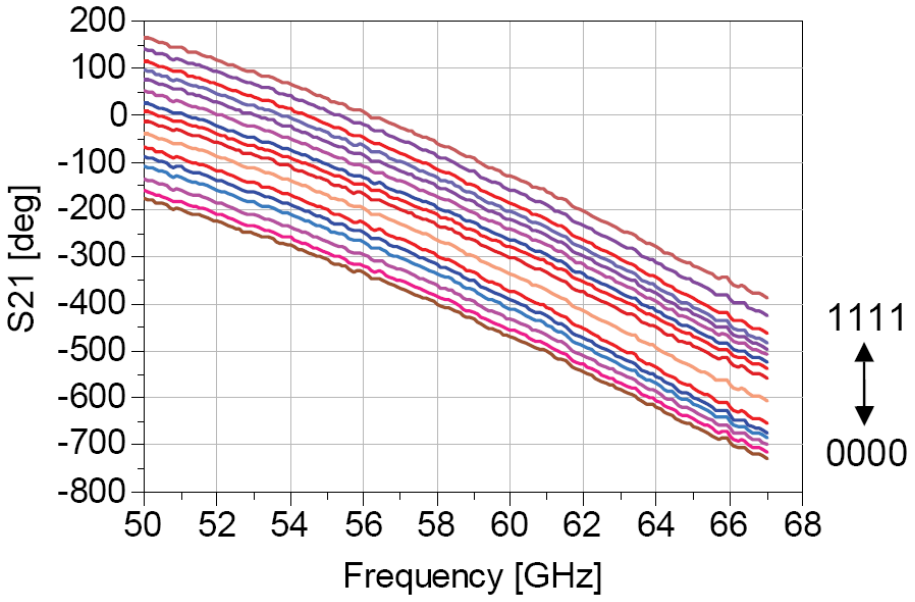


Figure 7.8: Measured insertion phase of one transmitter path for 16 phase settings.

The measured insertion phase [phase(S21)] of one transmitter path for 16 digitally controlled phase settings is depicted in Fig. 7.8. It achieves a phase step of approximately 22.5^{o} and a phase control range of 360^{o} in the 60GHz band.

Fig. 7.9 shows the measured insertion gain [dB(S21)], input and output reflection coefficients [dB(S11) and dB(S22)] of one transmitter path for 16 phase settings. It has an average insertion gain of 7.7dB at 62GHz and a 3dB-bandwidth of 6.5GHz, which matches the simulated S21 of phase state 0000. This insertion gain is contributed separately by the phase shifter that has a simulated insertion gain of -6dB, and the power amplifier that has a simulated gain of 15dB. The measured S11 and S22 are all better than -8dB at 62GHz; they are determined by the input matching of the phase shifter and the output matching of the power amplifier respectively and do not change for different phase settings. Besides, the measured reversed isolation (S12) of the transmitter path is -44dB.

Based on the measured insertion gain and phase shifts, the RMS gain

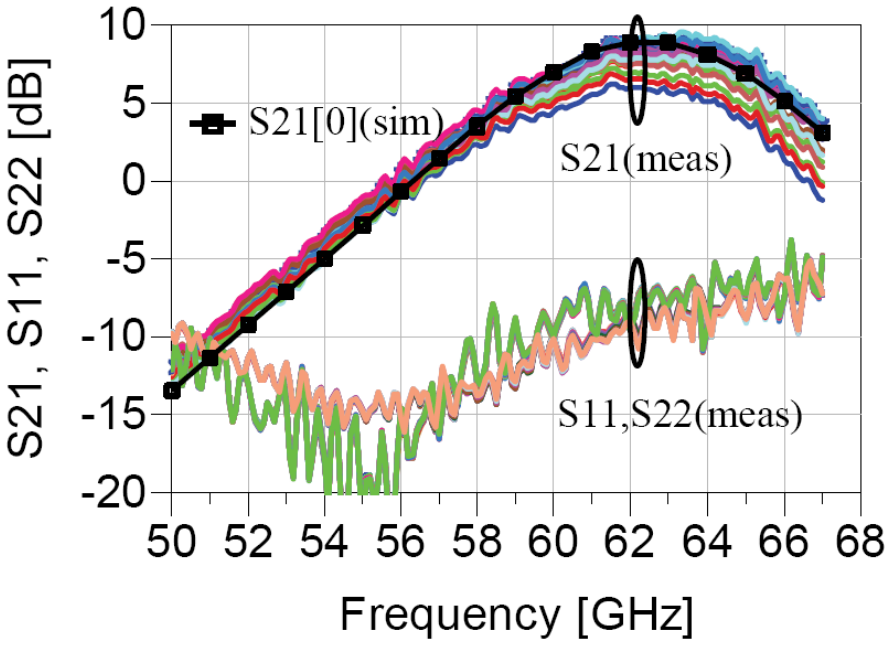


Figure 7.9: Measured insertion gain, input and output matching of one transmitter path for 16 phase settings.

and phase errors of one transmitter path are plotted in Fig. 7.10. They are 1.2dB and 9.2° at 62GHz respectively, as compared to an ideal 4-bit phase shifter with a uniform gain. The phase accuracy meets the 4-bit requirement.

Fig. 7.11 presents the measured non-linearity of one transmitter path and compares it to the simulated result. The measured output P_{1dB} is +4dBm at 62GHz. The measured maximum output power (P_{max}) of one transmitter path is observed to be higher than +8.3dBm (limited by the test equipment) with a corresponding power-added efficiency (PAE) of 2.4%. Considering that the phase shifter has a simulated loss of 6dB and consumes 30mW, the power amplifier has a corresponding gain of approximately 10dB and a PAE of 4.4% when transmitting the maximum output power. The power gain, output power and efficiency of the power amplifier can be further improved using a transformer coupled input, interstage and output matching network [40, 67], as the insertion loss of the match-

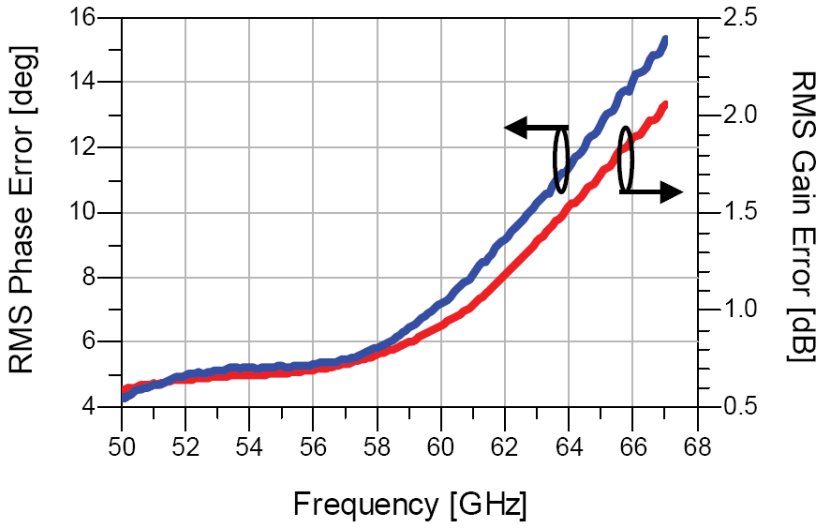


Figure 7.10: Measured RMS gain and phase errors of the 16 phase states as compared to an ideal 4-bit phase shifter

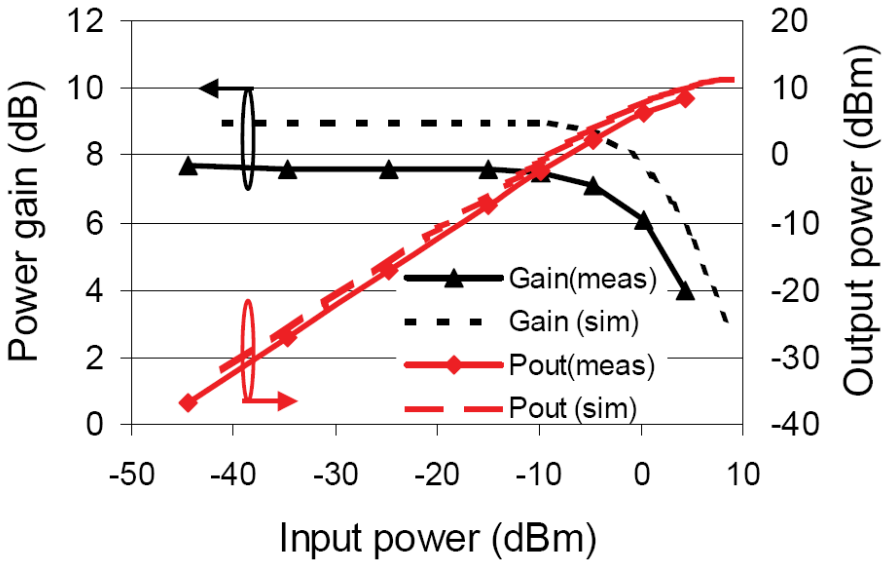


Figure 7.11: Measured power gain and output power of one transmitter path at 62GHz versus the RF input power.

ing network can be reduced without the use of lossy passive components including spiral inductors, fringe capacitors and long interstage interconnects.

Table 7.1 summarizes the measured performance of the transmitter path in comparison with published mm-wave phased-array transmitters. Although the comparison is not totally fair in the sense that we describe a single path, it is still useful.

Table 7.1: Benchmark of mm-wave phased array transmitters

Spec.	[21]	[30]	[31]	[23]	This work
Frequency (GHz)	77	42.5	60	60	62
Phase shifting @	LO	RF	RF	LO	RF
Number of paths	4	16	16	4	1
Key building blocks	PA, mixer, VCO, phase shifter, frequency divider, etc.	PA, phase shifter, signal divider, etc.	PA, phase shifter, mixer, RF power distribution, frequency synthesizer, etc.	PA, mixer, phase shifter, LO tripler, etc.	PA, phase shifter
Power Gain of each path (dB)	40.6 (@baseband)	12.5	35 (max @baseband)	20 (@baseband)	7.7 (average)
Max. output power of each path (dBm)	+12.5	-2.5	+9 (P_{out1dB})	+11	$\geq +8.3$
Phase shift step (^{o})	Analog	Digital, 22.5	Digital, 11.25	Analog	Digital, 22.5
Supply voltage (V)	2.5&1.5	5&3.3	2.6	1	1.2
Power consumption (mW)	1828 (4 paths)	3600 (16 paths)	3800 (16 paths)	590 (4 paths)	168 (1 path)
Technology	0.12μm SiGe Bi-CMOS	0.18μm SiGe Bi-CMOS	0.12μm SiGe Bi-CMOS	65nm CMOS	65nm CMOS
Chip area (mm^2)	17	8.3	43.9	4.1	1.7

7.4 Conclusion

In this chapter, we have presented a 60GHz 4-bit active phase shifter integrated with a power amplifier (PA) for phased array transmitters. The RF phase shifter in the transmitter has high linearity requirement, so that it is the output stage of the power amplifier rather than the phase shifter that saturates first. The one-path transmitter can be extended to multiple antenna paths.

Consisting of an active RF phase shifter and a PA, one transmit path achieves 360^o phase shift range in approximately 22.5^o steps, a maximum output power of higher than +8.3dBm and an average insertion gain of 7.7dB at 62GHz, a 3dB-bandwidth of 6.5GHz and a power dissipation of 165mW in the measurement.

This transmitter path, together with the receiver path presented in the previous chapter, have demonstrated that RF phase shifting is an appealing technique for 60GHz phased arrays: it achieves sufficient phase-shift resolution (22.5^o), large phase range (360^o), full integration in CMOS, low supply voltage, low power consumption, consumes small chip area, and possesses further scalability towards larger phased arrays without modification of the existing frequency converter and LO distribution network. In the next chapter, we will investigate the integration of a 60GHz IC and an antenna in a printed circuit-board (PCB) technology.

8

Flip-Chip Integration

As presented in the previous chapters, advances in silicon technology allow the realization of low-cost RF front-ends at 60GHz. However, to utilize the potential of this frequency band, low-cost transceiver designs are needed in which antennas, RF frontend and baseband processing are fully integrated.

In this chapter, the integration of a 60GHz amplifier and an antenna in a printed circuit-board (PCB) technology is investigated, as shown in Fig. 8.1[1]. Both the amplifier and the antenna have a differential design to provide a reliable interconnect that is low-loss. The amplifier is realized in a 65nm CMOS technology and achieves a gain of approximately 5dB and a 3dB gain bandwidth that ranges from 54 to 66GHz[2]. The antenna is a balanced-fed aperture-coupled patch (BFACP) antenna that is optimized for bandwidth and radiation efficiency [68]. The realized bandwidth is 10-15% and the accompanying radiation efficiency is larger than 75%.

This chapter is organized as follows. Section 8.1 discusses the materials that are used for the realization of the PCB package. The implemen-

[1] The design of the antenna and the PCB are mainly contributed by J.A.G. Akkermans and M.I. Kazim.

[2] This amplifier was implemented earlier than and different from those amplifiers presented in Chapter 6 and 7.

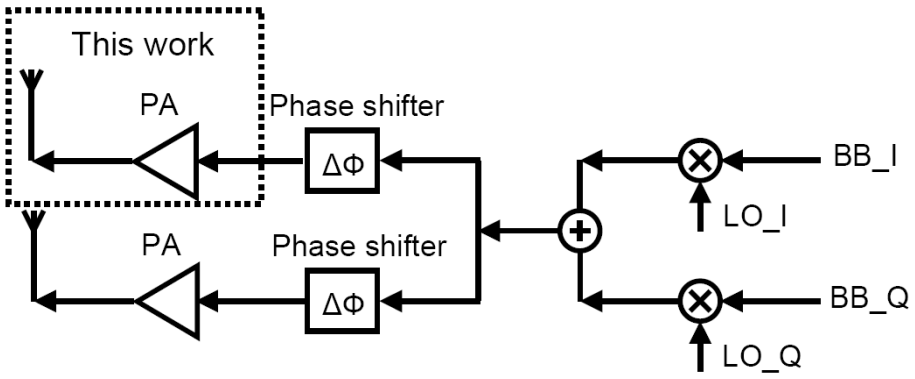


Figure 8.1: The integration of an amplifier and an antenna.

tation of flip-chip interconnection between the amplifier and the PCB is presented in Section 8.2. The measurement results of the flip-chip integration are presented and discussed in Section 8.3. This chapter is published in [64].

8.1 Package Materials

The integration of an amplifier and an antenna has to be realized in a single PCB package. For this purpose, the BFACP antenna is very well suited. In the prototypes of the BFACP antennas, the dielectric layers have been realized from teflon-based materials (NY9217, $\varepsilon_r = 2.17$). The low dielectric constant of this material and the inherent surface-wave suppression of the antenna element provides a high radiation efficiency.

Although teflon-based materials have good RF performance, they cannot be employed to create a complete package. The disadvantages of teflon-based materials are that they are not very rigid and that they have a large thermal expansion coefficient. Therefore, this material cannot be used for the realization of a rigid package, and the implementation of vias can be difficult because of the relatively large thermal expansion. An improved PCB stack that can function as a package is shown in Fig. 8.2. The upper layer of this package is realized from teflon-based material to ensure good RF performance. The lower layers are realized from a glass-reinforced hydrocarbon/ceramic material (Ro4350B). This material

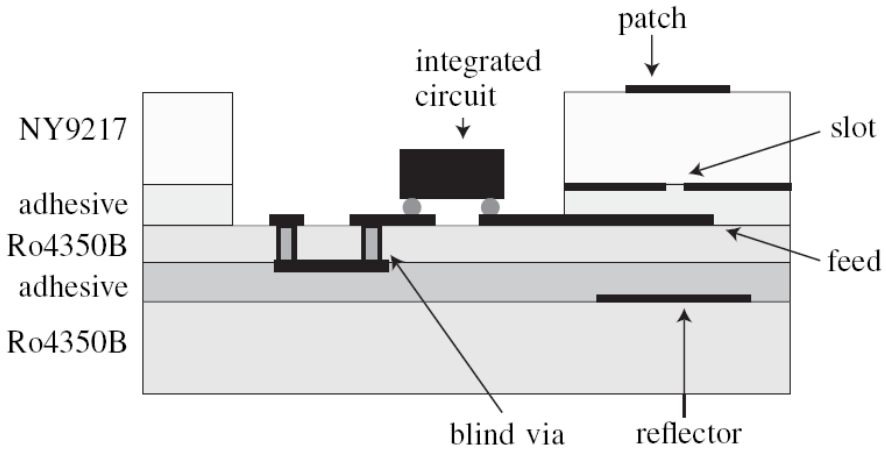


Figure 8.2: Schematic layout of PCB package with an amplifier and an antenna.

is much more rigid compared to teflon-based materials and has low dissipative losses as well. The dielectric constant of this material is specified to be 3.66 at 10GHz. The lowest dielectric layer of the package is used to provide the package with its mechanical rigidity. The middle layer is a thin layer that is used to create a well-defined RF feed. This layer also allows the realization of vias, such that the routing of control signals can be simplified. The dielectric layers are laminated together with adhesive layers in between that are tailored for adhesion with these materials.

8.2 Package Prototype

A prototype has been built, which embeds a 60GHz amplifier and a BFACP antenna into one package. A schematic layout of the package is shown in Fig. 8.2. The frequency band of the optimized antenna ranges from 56 to 65GHz and the simulated radiation efficiency in this band is larger than 75 % (see Fig. 8.3). The amplifier, which is different from that presented in Chapter 6 and 7, is realized in a 65nm CMOS technology and is initially characterized with RF probes that connect directly to the chip. The measured maximum gain of the amplifier is about 5dB and the 3dB gain

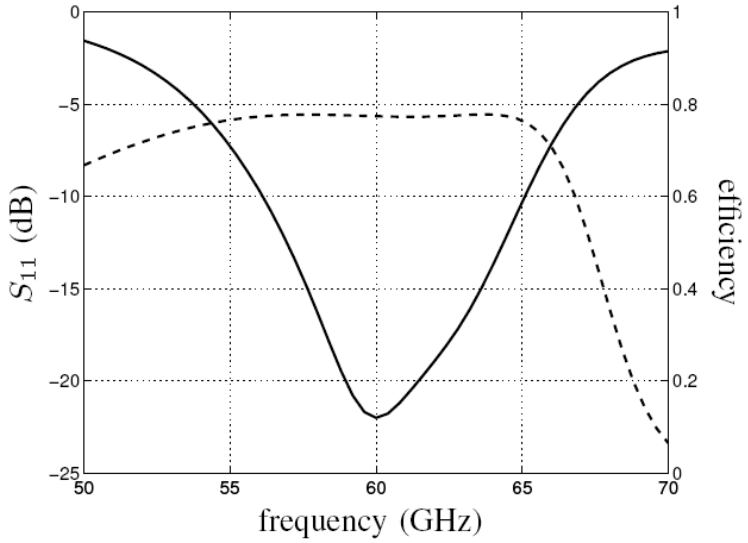


Figure 8.3: Simulated reflection coefficient (solid) and radiation efficiency (dashed) of the optimised antenna.

bandwidth ranges from 54 to 66GHz.

8.2.1 Flip-chip Interconnect

To integrate the amplifier with the antenna, a reliable interconnection needs to be realized. Traditionally, the interconnection between an amplifier and a PCB is realized through wire-bonding, but the performance of this type of interconnect decreases rapidly for higher frequencies, because of the large wire inductance (1nH/mm) that is associated with the wire-bonding. Alternatively, flip-chip technologies can be employed to provide a better interconnection, since flip-chip interconnections have lower and more predictable parasitic inductances [69]. In flip-chip technology, the metallic pads on the amplifier are connected to a corresponding set of pads on the PCB using an array of balls or bumps. These balls or bumps can be realized from solder or metal like gold and copper [70]. In this demonstrator, gold stud bumps have been used in combination with an anisotropic conductive adhesive. First, the gold bumps are placed on the pads of the amplifier. Second, the amplifier is flipped and pushed onto the PCB. In between the

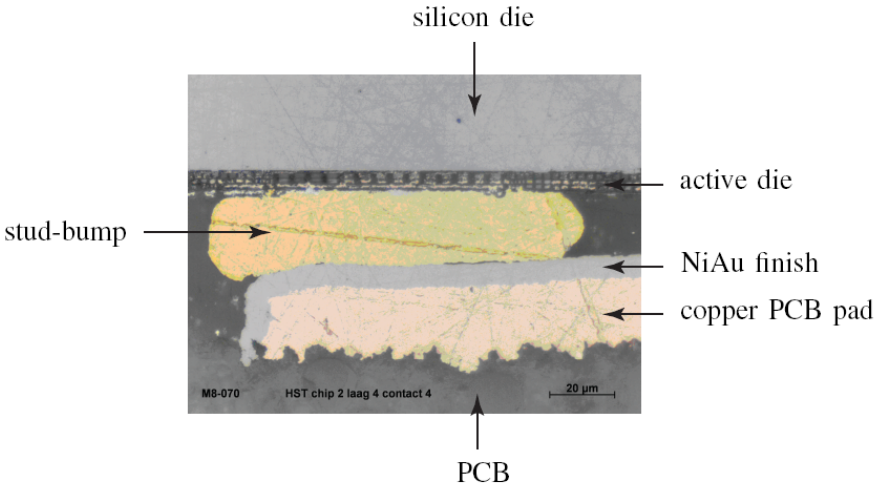


Figure 8.4: Microscopic photograph of the cross-section of a flip-chip interconnection.

amplifier and the PCB, an adhesive is placed that contains silver particles. Because of the applied pressure, these particles form a conducting path in between the stud bumps and the PCB pads. A microscopic photograph of the cross-section of such a flip-chip interconnection is shown in Fig. 8.4.

8.2.2 Chip Mount

The layout of the chip mount is shown in Fig. 8.5. This chip mount has been designed such that the pads on the PCB correspond with the pads of the amplifier. The input signal of the amplifier can be provided through the ground-signal-signal-ground (GSSG) connection on the PCB. Vias have been used to connect all the grounds to a large metal plane underneath the chip mount. The DC supply and bias voltages can be applied to the amplifier from the PCB as well. RF stubs have been employed to suppress the RF signals on the DC supplies. The output of the amplifier connects directly to the differential feed of the antenna.

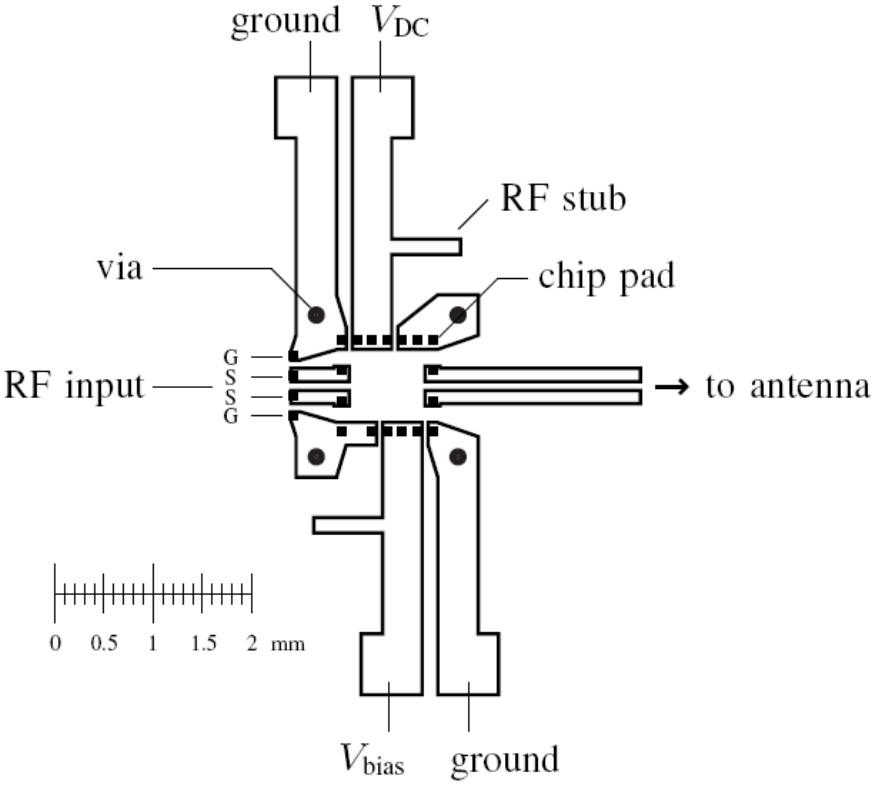


Figure 8.5: Layout of amplifier chip mount.

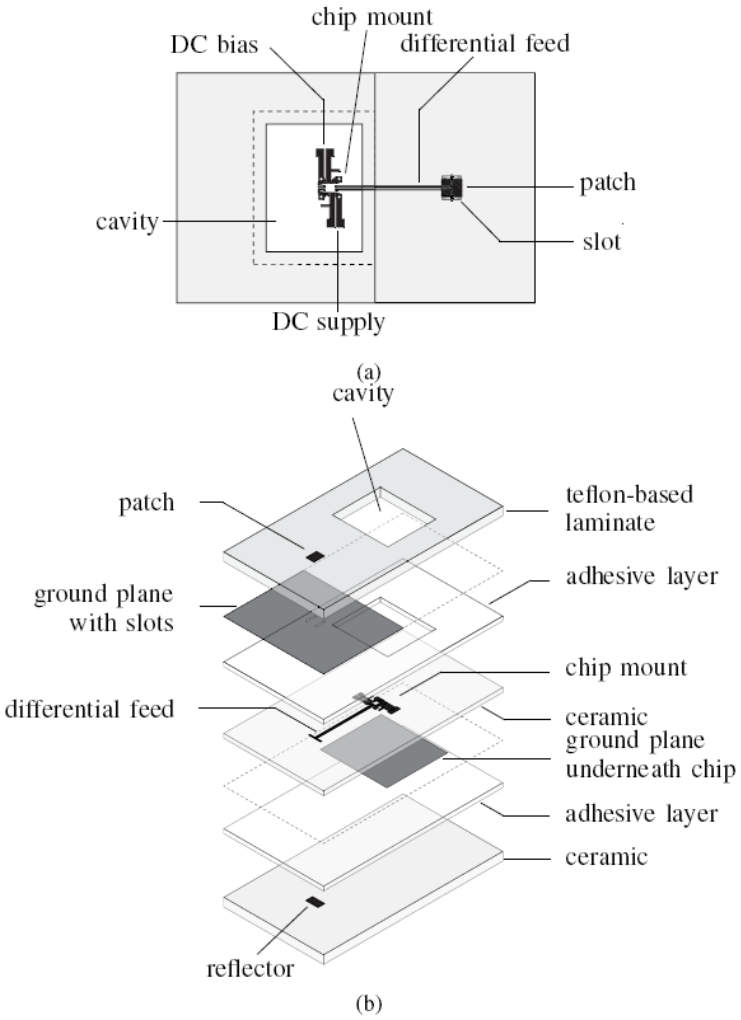


Figure 8.6: Layout of package. (a) Top view. (b) Explored view.

8.2.3 Package

The complete package is depicted in Fig. 8.6. Here, the layout of each layer can be easily identified. The width and length of the package is 18×28mm, whereas the total thickness is 0.82mm. The coplanar microstrip feed connecting the amplifier and the antenna is constructed such that it has a ground plane underneath it near the amplifier and above it near the

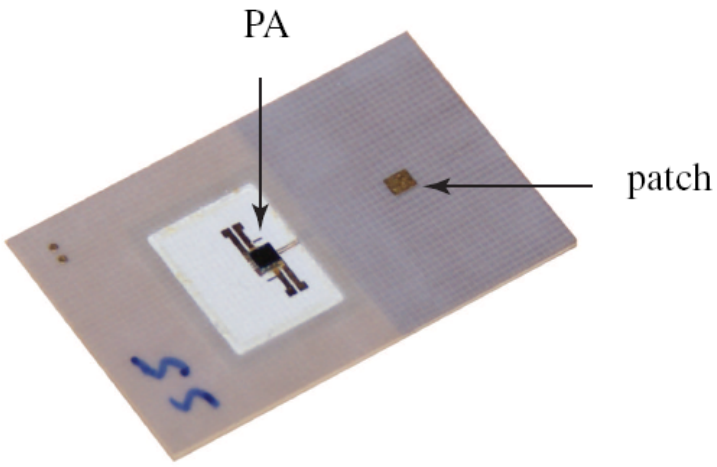


Figure 8.7: Photograph of integrated amplifier and BFACP antenna.

antenna. In this way, the characteristic impedance of the differential feed is close to 100Ω everywhere.

8.3 Measurement Results

To characterize the performance of the packaged amplifier and antenna (Fig. 8.7), the performance of the antenna is evaluated first. Since the antenna has a differential feed, GSSG RF probes have been used in combination with an external balun to provide the balanced input signal. The RF probe has been calibrated with a one-port load-reflect-match (LRM) calibration. The measured and simulated reflection coefficients are shown in Fig. 8.8. It is observed that the impedance matching of the antenna is below -10dB in the frequency range from 57.7 to 65.0GHz. This corresponds well with the gain bandwidth of the amplifier that ranges from 54 to 66GHz.

The performance of the packaged amplifier and antenna has been investigated as well. The operation of this package has been tested on a probe station first (see Fig. 8.9). A GSSG RF probe has been used to connect the RF input signal to the amplifier. The DC supply and bias voltages

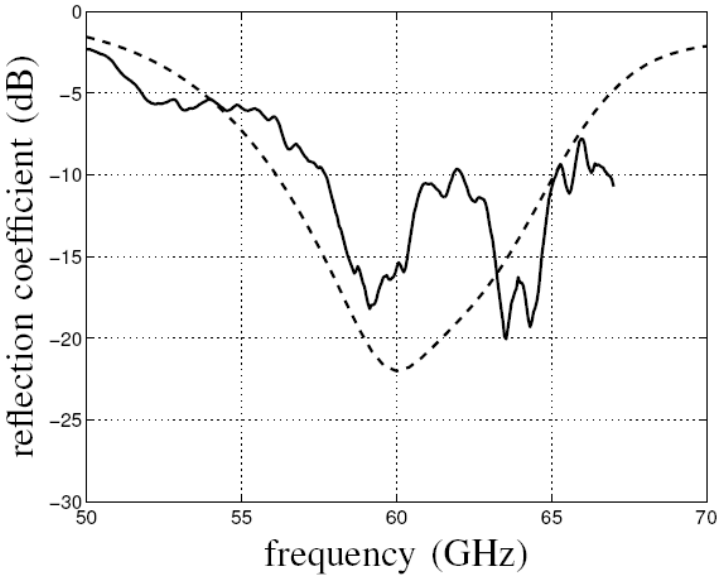


Figure 8.8: Reflection coefficient of the packaged BFACP antenna. Measurement (solid), simulation [Spark] (dashed).

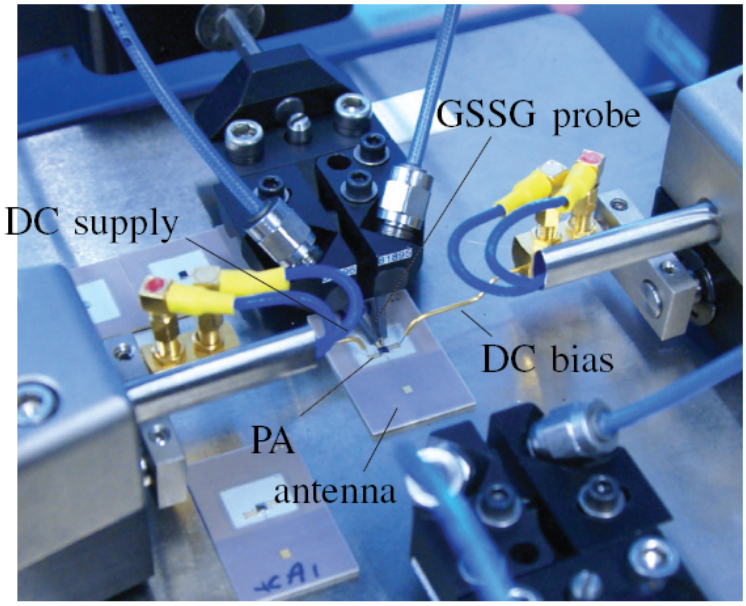


Figure 8.9: Measurement setup of antenna package on probe station.

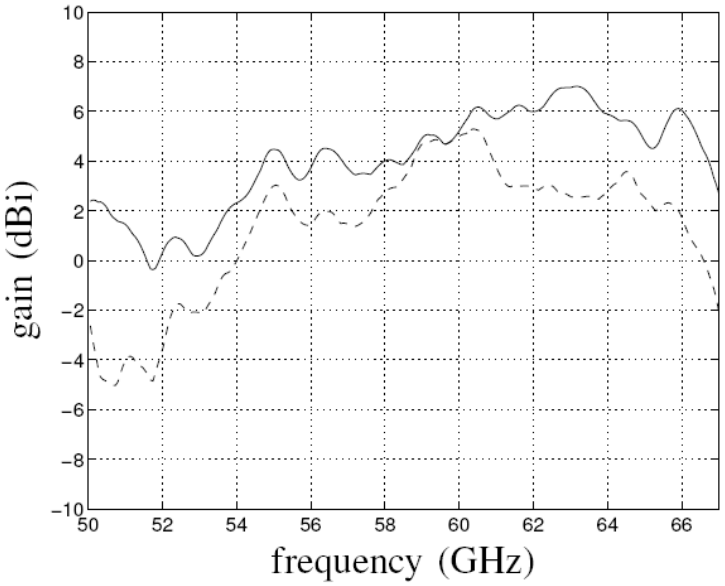


Figure 8.10: Measured maximum gain of the packaged BFACP antenna with amplifier (dashed) and without amplifier (solid).

have been applied with DC probes. We compared the gain of the combined amplifier and antenna with the gain of the antenna alone (i.e., without amplifier). To characterize the radiation pattern of the combined amplifier and antenna, wires have been soldered to the DC bias and supply connections of the package, and the radiation patterns are measured on the far-field radiation pattern measurement setup.

The gain of the antenna alone and the amplifier-antenna combination is compared in Fig. 8.10. It is observed that the gain of the amplifier is 0-4dB lower than the gain of the antenna alone in the operating range of the antenna (57.7 - 65.0GHz). This implies that the insertion losses due to the input and output flip-chip interconnection are equal or larger than the gain of the packaged amplifier (5dB). The causes for these losses are:

- ○ Resistive loss. The flip-chip interconnection has been realized with gold stud-bumps in combination with an anisotropic conductive adhesive (see Fig. 8.4). This interconnect introduces some dissipative losses due to the finite conductivity of the transition.

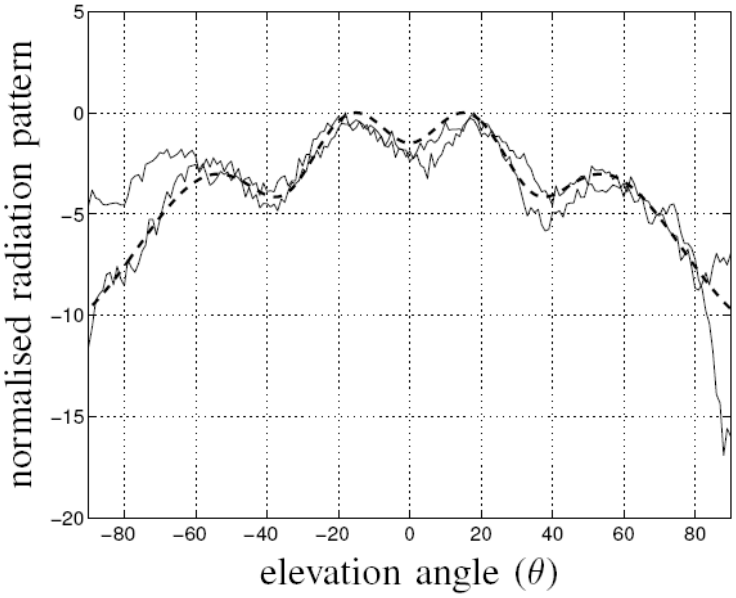


Figure 8.11: Measured normalized radiation pattern of packaged antenna and amplifier. E-plane, frequency $f = 60$GHz. Measurements of antenna pattern with and without amplifier (solid), simulated radiation pattern [CST Microwave Studio] (dashed).

- ○ Impedance mismatch. Both the amplifier and the antenna have been designed for an input and output impedance of 100Ω; the presence of the flip-chip interconnect distorts the matching between the RF probe and the input of the amplifier, as well as the matching between the output of the amplifier and the input of the antenna.

- ○ Amplifier de-tuning. The amplifier has been characterized with on-wafer tests. The input and output of the amplifier are de-tuned in frequency when it is flip-chipped onto the PCB.

These losses can be analyzed by fully characterizing the flip-chip interconnection using on-chip short-open-load-thru (SOLT) test structures in future research. When the model of the flip-chip interconnection is included in the co-design of amplifier and antenna, the insertion loss due to impedance mismatch and amplifier de-tuning can be minimized. The re-

sistive loss can be reduced e.g. by improving the anisotropic conductive adhesive.

The normalized radiation patterns are compared in Fig. 8.11. It is observed that both measured radiation patterns are very similar. This indicates that the power is radiated by the antenna alone and no significant amount of power is radiated by the RF probe, the amplifier or the flip-chip transitions. Moreover, it is observed from Fig. 8.11 that the radiated patterns are in good agreement with simulated results.

8.4 Conclusion

The integration of a 60GHz amplifier and an antenna in a PCB technology has been investigated. The implementation of flip-chip integration and the measurement results are presented and discussed in detail. It has been shown that the antenna can be integrated with an amplifier, although the gain of the amplifier-antenna combination is lower then expected. Possible causes for this gain reduction have been discussed and can be improved in future research.

9

Conclusions and Recommendations

9.1 Conclusions

Here are the conclusions of the thesis:

- ○ It is feasible to implement an low-cost high data-rate 60GHz wireless system using phased array techniques in a CMOS technology. The RF phase shifting architecture shows low cost and low power. The *passive* and *active* RF phase shifters, and the integration with other other key building blocks (i.e. LNA and PA), achieve high performance.

- ○ The loaded-line based *passive* phase shifter achieves linear phase shifts over a large frequency range and functions as a true time-delay compensation; in contrast, the vector-modulator based *active* phase shifter shows relatively constant phase shifts over frequencies.

- ○ The step-size requirement (e.g. 22.5^{o}) of a phase shifter has been derived from the phased-array system specifications of e.g. constellation spreading, beam direction and interference suppression.

- The 60GHz 4-bit *passive* phase shifter shows high operating frequency (60GHz), small phase-shift step (22.5^{o}) and low insertion loss.

- The 60GHz 4-bit *active* phase shifter shows low insertion loss (or even gain) and low variation in loss, as compared to passive phase shifters. In this way, it is not required to implement an low-noise amplifier (LNA) or power amplifier (PA) with very high gain, programmable gain settings and large power dissipation in order to compensate the loss and loss variations.

- The integration of the 60GHz *active* phase shifter with other key building blocks (i.e. LNA and PA) has demonstrated that RF phase shifting is an appealing technique for 60GHz phased arrays: it achieves sufficient phase resolution (4-bit), large phase range (360^{o}), full integration in CMOS, low supply voltage, low power consumption, consumes small chip area, and possesses further scalability towards larger phased arrays without modification of the existing frequency converter and LO distribution network.

- A 60GHz CMOS amplifier and an antenna have been integrated in a printed circuit-board (PCB) package. It demonstrates that a 60GHz amplifier can be integrated with an antenna with good performance.

9.2 Recommendations for Future Research

In future, these research topics can be interesting:

- Investigate phased array techniques at higher operating frequencies (100GHz and beyond). At these higher frequencies, the performance (e.g. noise figure, gain and output power) of a transceiver will be even worse. Thanks to the smaller antenna sizes, phased array techniques will significantly contribute to a sufficient link budget for a wireless system.

- Investigate phased arrays techniques for a larger number of antennas and also for interference nulling. These will increase the perfor-

mance (e.g. antenna gain and directionality) of the wireless system, but often require a higher phase-shift accuracy.

- ○ Besides one-dimension antenna arrays, investigate two- or three-dimensional antenna arrays and their requirements upon phase shifters. These will achieve beamforming and beam steering in full space.

- ○ Integrate an antenna array with a phased array transceiver e.g. in a printed circuit-board (PCB) package. This requires a full characterization of the flip-chip interconnection, as well as the mismatch and coupling between different antenna paths.

List of Symbols and Abbreviations

ACC	Autonomous Cruise Control
ADC	Analog-to-digital Converter
BFACP	Balanced-fed Aperture-coupled Patch
BW	Bandwidth
CMOS	Complementary Metaloxidesemiconductor
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
EIRP	Effective Isotropic Radiated Power
EM	Electromagnetic
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FDMA	Frequency Domain Multiple Access
FM	Frequency Modulated
FSK	Frequency-shift Keying
GPRS	General Packet Radio Service
GSGSG	Ground-signal-ground-signal-ground
GSM	Global System for Mobile Communications
GSSG	Ground-signal-signal-ground
HDTV	High Definition Television
IC	Integrated Circuit
IF	Intermediate Frequency
IR	Infrared Radiation
ISM	Industrial, Scientific and Medical
LAN	Local Area Network

LMDS	Local Multipoint Distribution Service
LNA	Low Noise Amplifier
LTE	Long Term Evolution
LO	Local Oscillator
LOS	Line-of-sight
LRM	Load-reflect-match
MAN	Metropolitan Area Network
MOSFET	Metaloxidesemiconductor Field-effect Transistor
MIMO	Multiple-input and Multiple-output
NLOS	Non-line-of-signt
NF	Noise Figure
OFDM	Orthogonal frequency-division multiplexing
P_{1dB}	1dB Compression Point
PA	Power Amplifier
PAE	Power-added Efficiency
PAN	Personal Area Network
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase-locked Loop
P_{max}	Maximum Power
PVT	Process, Voltage and Temperature
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
SIP	System in Package
SISO	Single-input and single-output
SNR	Signal-to-noise Ratio
SOLT	Short-open-load-through
SPDT	Single Pole Double Throw
TDMA	Time Domain Multiple Access
UMTS	Universal Mobile Telecommunications System
UWB	Ultra-wideband
VCO	Voltage Controlled Oscillator
VGA	Variable-gain Amplifier
WAN	Wide Area Network
WCDMA	Wideband Code Division Multiple Access
WPAN	Wireless Personal Area Network

References

[1] "SiGi-Spot basic design considerations," Presentation of Dr. P. Smulders, 2006, Eindhoven University of Technology.

[2] *Technical Comparison*, www.bluetooth.com, 2010.

[3] *Comparison of wireless data standards*, www.wikipedia.org, 2010.

[4] P. Smulders *et al.*, "Exploiting the 60 GHz Band for Local Wireless Multimedia Access," *IEEE Communications Magazines*, vol. 2, no. 1, pp. 140–147, Jan. 2002.

[5] S. E. Gunnarsson *et al.*, "60 GHz Single-Chip Front-End MMICs and Systems for Multi-Gb/s Wireless Communication," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1143–1157, May 2007.

[6] B. Floyd *et al.*, "SiGe Bipolar Transceiver Circuits Operating at 60 GHz," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 156–167, Jan. 2005.

[7] C. H. Doan *et al.*, "Millimeter Wave CMOS Design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[8] B. Razavi, "A 60-GHz CMOS Receiver Front-End," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.

[9] C. Marcu *et al.*, "A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2009.

[10] J. Borremans *et al.*, "A Digitally Controlled Compact 57-to-66GHz Front-End in 45nm Digital CMOS," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2009.

[11] A. M. Niknejad *et al.*, *mm-Wave Silicon Technology: 60 GHz and Beyond*, Springer, New York, 2008.

[12] P. Baltus *et al.*, *Systems and Architechtures for very High Frequency Radio Links*, Analog Circuit Design, Springer, 2008.

[13] G.E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[14] D. Parker *et al.*, "Phased Arrays - Part I: Theory and Architectures," *IEEE Transaction on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 678–687, Mar. 2002.

[15] D. Parker *et al.*, "Phased-arrays C part II: implementations, applications, and future trends," *IEEE Transaction on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 688–698, Mar. 2002.

[16] X. Guan *et al.*, "A Fully Integrated 24-GHz Eight-Element Phased-Array Receiver in Silicon," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[17] A. Natarajan *et al.*, "A Fully Integrated 24-GHz Phased-Array Transmitter in CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2502–2514, Dec. 2005.

[18] H. Hashemi *et al.*, "A 24-GHz SiGe Phased-Array Receiver - LO Phase-Shifting Approach," *IEEE Transaction on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 614–625, Feb. 2005.

[19] A. Afsahi *et al.*, "A Low-Power Single-Weight-Combiner 802.11abg SoC in 0.13μm CMOS for Embedded Applications Utilizing An Area

and Power Efficient Cartesian Phase Shifter and Mixer Circuit," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1101–1118, May 2008.

[20] J. Paramesh *et al.*, "A Four-Antenna Receiver in 90-nm CMOS for Beamforming and Spatial Diversity," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2515–2524, Dec. 2002.

[21] A. Natarajan *et al.*, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 2807–2819, Dec. 2006.

[22] K. Scheir *et al.*, "A 52GHz Phased-Array Receiver Front-end in 90nm Digital CMOS," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2008.

[23] Wei L. Chan *et al.*, "A 60GHz-Band 2×2 Phased-Array Transmitter in 65nm CMOS," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 42–43.

[24] P. Baltus *et al.*, "A 3.5mW 2.5GHz diversity receiver in Silicon-On-Anything," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2074–2079, Dec. 1998.

[25] P. Baltus *et al.*, "Optimizing RF Front Ends for Low Power," *Proceedings of the IEEE*, Dec. 2000.

[26] S. Kishimoto *et al.*, "A 60-GHz Band CMOS Phased Array Transmitter utilizing Compact Baseband Phase Shifters," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2009.

[27] K. Raczkowski *et al.*, "A Wideband Beamformer for a Phased-Array 60GHz Receiver in 40nm Digital CMOS," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 40–41.

[28] A. Natarajan *et al.*, "A Bidirectional RF-Combining 60GHz Phased-Array Front-End," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2007, pp. 202–203.

[29] K. Koh *et al.*, "An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18μm SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, June 2008.

[30] K. Koh *et al.*, "A Millimeter-Wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18-μm SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[31] A. Valdes-Garcia *et al.*, "A SiGe BiCMOS 16-Element Phased-Array Transmitter for 60GHz Communications," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 218–219.

[32] C. Shannon, "A Mathematical Theory of Communication," *The Bell System Technical Journal*, vol. 27, pp. 379–423, 623–656, July-October 1948.

[33] H. Hashemi, "The Indoor Radio Propagation Channel," *Proceedings of the IEEE*, vol. 81, no. 7, July 1993.

[34] B. Razavi, *RF Microelectronics*, Prentice Hall, 1998.

[35] *Automobile safety*, www.wikipedia.org, 2010.

[36] IMS 2002 Workshop, www.mtt.org, *Automotive Radar and Prospective Circuit/Antenna Technologies - From Car Collision Avoidance to Autonomous Driving*.

[37] L.Yujiri, "Passvie mm-Wave Imaging," *IEEE Microwave Magazines*, vol. 4, no. 3, pp. 39–50, Sept. 2003.

[38] *International Technology Roadmap for Semiconductors (ITRS) 2006*, http://www.itrs.net/.

[39] Jie-Wei Lai *et al.*, "A 1V 17.9dBm 60GHz Power Amplifier in Standard 65nm CMOS," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 424–425.

[40] B. Martineau *et al.*, "A 53-to-68GHz 18dBm Power Amplifier with an 8-Way Combiner in Standard 65nm CMOS," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 428–429.

[41] M. Varonen *et al.*, "Millimeter-Wave Integrated Circuits in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 1991–2002, Sept. 2008.

[42] A. Tomkins *et al.*, "A Zero-IF 60 GHz 65 nm CMOS Transceiver With Direct BPSK Modulation Demonstrating up to 6 Gb/s Data Rates Over a 2 m Wireless Link," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 8, pp. 2085–2099, Aug. 2009.

[43] T. Mitomo *et al.*, "A 60-GHz CMOS Receiver Front-End With Frequency Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, Apr. 2008.

[44] J. Roderick *et al.*, "Silicon-Based Ultra-Wideband Beam-Forming," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1726–1739, Aug. 2006.

[45] Ta-Shun Chu *et al.*, "A True Time-Delay-Based Bandpass Multi-Beam Array at mm-Waves Supporting Instantaneously Wide Bandwidths," in *IEEE International Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 38–39.

[46] *MIMO*, www.wikipedia.org, 2010.

[47] Advanced Design System 2009, *Product Documentation*.

[48] K. Maruhashi *et al.*, "Design and Performance of a Ka-band Monolithic Phase Shifter Utilizing Nonresonant FET Switches," *IEEE Transaction on Microwave Theory and Techniques*, Aug. 2000.

[49] F. Ellinger *et al.*, "Varactor-Loaded Transmission-Line Phase Shifter at C-Band Using Lumped Elements," *IEEE Transaction on Microwave Theory and Techniques*, Apr. 2003.

[50] F. Ellinger *et al.*, "Ultracompact Reflective-Type Phase Shifter MMIC at C-Band With 360^{o} Phase-Control Range for Smart Antenna Combining," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 481–486, Apr. 2002.

[51] C. F. Campbell *et al.*, "A Compact 5-Bit Phase-Shifter MMIC for K-Band Satellite Communication Systems," *IEEE Transaction on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2652–2656, Dec. 2000.

[52] D. Kang *et al.*, "Ku-band MMIC Phase Shifter Using a Parallel Resonator with 0.18-μm CMOS Technology," *IEEE Transaction on Microwave Theory and Techniques*, Jan. 2006.

[53] B. Min *et al.*, "Single-Ended and Differential Ka-Band BiCMOS Phased Array Front-Ends," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.

[54] D. Kang *et al.*, "A 4-bit CMOS Phase Shifter Using Distributed Active Switches," *IEEE Transaction on Microwave Theory and Techniques*, July 2007.

[55] K. Koh *et al.*, "A 0.13-μm CMOS Phase Shifters for X-, Ku-, and K- band Phased Arrays," *IEEE Journal of Solid-State Circuits*, Nov. 2007.

[56] Microwave Encyclopedia, www.mocrowaves101.com, 2010, *Phase Shifters*.

[57] M. Tsai *et al.*, "60GHz Passive and Active RF-path Phase Shifters in Silicon," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2009.

[58] Y. Yu *et al.*, "A 60GHz Digitally Controlled RF-Beamforming Receiver Front-end in 65nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2009.

[59] I. Sarkas *et al.*, "W-band 65-nm CMOS and SiGe BiCMOS Transmitter and Receiver with Lumped I-Q Phase Shifters," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2009.

[60] Y. Yu *et al.*, "A 60GHz Digitally Controlled Phase Shifter in CMOS," in *European Solid-State Circuits Conf. (ESSCIRC)*, 2008, pp. 250–253.

[61] Yikun Yu *et al.*, "A 60GHz Phase Shifter Integrated with LNA and PA in 65nm CMOS for Phased Array Systems," *IEEE Journal of Solid-State Circuits*, 2010.

[62] S. Alalus *et al.*, "A 60GHz Phased Array in CMOS," in *IEEE Custom Integrated Circuits Conf. (CICC)*, 2006, pp. 393–396.

[63] E. Cohen *et al.*, "A bidirectional TX/RX four element phased-array at 60GHz with RF-IF conversion block in 90nm CMOS process," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2009.

[64] J.A.G. Akkermans *et al.*, "Flip-chip integration of differential CMOS power amplifier and antenna in PCB technology for the 60-GHz frequency band," in *European Conference on Antennas and Propagation (EuCAP)*, 2009.

[65] L. Tiemeijer *et al.*, "Predictive Spiral Inductor Compact Model For Frequency and Time Domain," in *International Electron Devices Meeting (IEDM)*, 2003, pp. 36.4.1– 36.4.4.

[66] S. K. Reynolds *et al.*, "A 16-Element Phased-Array Receiver IC for 60GHz Communications in SiGe BiCMOS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2010.

[67] W. L. Chan *et al.*, "A 58-65 GHz Neutralized CMOS Power Amplifier With PAE Above 10% at 1-V Supply," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.

[68] J. Akkermans *et al.*, "Design of a millimeterwave balanced-fed aperture-coupled patch antenna," in *European Conference on Antennas and Propagation (EuCAP)*, 2006, pp. 1–6.

[69] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Transaction on Microwave Theory and Techniques*, vol. 49, no. 5, pp. 871–878, May 2001.

[70] R. K. Ulrich and W. D. Brown, *Advanced electronic packaging, 2nd ed.*, Wiley, New York, 2006.

List of Publications

Journal Article

[1] Yikun Yu, P.G.M. Baltus, A. de Graauw, E. van der Heijden, C.S. Vaucher and A.H.M. van Roermund, "A 60GHz Phase Shifter Integrated with LNA and PA in 65nm CMOS for Phased Array Systems," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1697-1709, Sept. 2010.

Book Chapter

[1] P.G.M. Baltus, P. Smulders and Yikun Yu, "Systems and Architechtures for very High Frequency Radio Links," *Analog Circuit Design*, Springer 2008.

Conference Proceeding

[1] Yikun Yu, P.G.M. Baltus, A. de Graauw, E. van der Heijden, M. Collados and A.H.M. van Roermund, "A 60GHz Digitally Controlled RF-Beamforming Receiver Front-end in 65nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)* 2009.

[2] Yikun Yu, P.G.M. Baltus, A. de Graauw, D. Jeurissen, E. van der Heijden, R. Pijper and A.H.M. van Roermund, "A 60GHz Digitally Controlled Phase Shifter in CMOS," *Proc. European Solid-State Circuits Conference (ESSCIRC)*, pp. 250-253, Sept. 2008.

[3] J.A.G. Akkermans, M.I. Kazim, Yikun Yu, M.H.A.J. Herben, P.G.M. Baltus, P.F.M. Smulders, "Flip-chip integration of differential CMOS power amplifier and antenna in PCB technology for the 60-GHz frequency band," *European Conference on Antennas and Propagation (EuCAP)* 2009.

[4] Yikun Yu, S. Butselaar and K.A.A. Makinwa, "A 2nd-order Sigma-Delta ADC as an Interface Circuit for SOI Accelerometer Sensors," *Proc. Program for Research on Integrated Systems and Circuits (ProRISC)*, pp. 316-319, Nov. 2005.

Summary

The 60GHz band is promising for applications such as high-speed short-range wireless personal area network (WPAN), real time video streaming at rates of several Gbps, automotive radar, and mm-Wave imaging, since it provides a large amount of bandwidth that can freely (i.e. without a license) be used worldwide. However, transceivers at 60GHz pose several additional challenges over microwave transceivers. In addition to the circuit design challenges of implementing high performance 60GHz RF circuits in mainstream CMOS technology, the path loss at 60GHz is significantly higher than at microwave frequencies because of the smaller size of isotropic antennas. This can be overcome by using phased array technology. This thesis studies the new concepts and design techniques that can be used for 60GHz phased array systems.

It starts with an overview of various applications at mm-wave frequencies, such as multi-Gpbs radio at 60GHz, automotive radar and millimeter-wave imaging. System considerations of mm-wave receivers and transmitters are discussed, followed by the selection of a CMOS technology to implement millimeter-wave (60GHz) systems.

The link budget of a 60GHz WPAN is analyzed, which leads to the introduction of phased array techniques to improve system performance. Different phased array architectures are studied and compared. The system requirements of phase shifters are discussed. Several types of conventional

RF phase shifters are reviewed.

A 60GHz 4-bit *passive* phase shifter is designed and implemented in a 65nm CMOS technology. Measurement results are presented and compared to published prior art.

A 60GHz 4-bit *active* phase shifter is designed and integrated with a low-noise amplifier (LNA) and combiner for a phased array receiver. This is implemented in a 65nm CMOS technology and the measurement results are presented.

The design of a 60GHz 4-bit *active* phase shifter and its integration with a power amplifier (PA) is also presented for a phased array transmitter. This is implemented in a 65nm CMOS technology. The measurement results are also presented and compared to reported prior art.

The integration of a 60GHz CMOS amplifier and an antenna in a printed circuit-board (PCB) package is investigated. Experimental results are presented and discussed.

Samenvatting

De 60GHz-band is een veelbelovend frequentiegebied voor applicaties zoals high-speed shortrange wireless personal area networks (WPAN), real time video streaming met data-rates van enkele Gbps, automotive radar en mm-golf imaging, omdat een grote bandbreedte beschikbaar is die bovendien wereldwijd licentievrij gebruikt kan worden. Transceivers voor 60GHz brengen echter een aantal extra uitdagingen met zich mee ten opzichte van microgolf transceivers. Naast de uitdaging van het implementeren van goed presterende 60GHz RF circuits in standaard CMOS technologie, is bovendien het signaalverlies op 60GHz significant hoger ten opzichte van microgolf frequenties vanwege de kleinere afmetingen van isotropische antennes. Dit probleem kan opgelost worden door gebruik te maken van phased array technologie. Deze thesis bestudeert nieuwe concepten en ontwerptechnieken die gebruikt kunnen worden voor 60GHz phased array systemen.

Eerst wordt een overzicht van diverse applicaties voor mm-golf frequenties gegeven, zoals multi-Gpbs radio op 60GHz, automotive radar en mm-golf imaging. Systeemaspecten van mm-golf ontvangers en zenders worden besproken, gevolgd door de selectie van een CMOS technologie voor de implementatie van mm-golf (60GHz) systemen.

Het link budget van een 60GHz WPAN wordt geanalyseerd, wat leidt tot de introductie van phased array technieken om de systeemprestaties te

verbeteren. Verschillende phased array architecturen worden bestudeerd en vergeleken. De systeemeisen van de phase shifters worden besproken, en verschillende conventionele RF phase shifters worden bekeken.

Een 60GHz 4-bit passive phase shifter is ontworpen en geimplementeerd in een 65nm CMOS technologie. Meetresultaten worden gepresenteerd en vergeleken met eerder gepubliceerd werk.

Een 60GHz 4-bit active phase shifter is ontworpen en geintegreerd met een low-noise amplifier (LNA) en combiner voor een phased array ontvanger. Dit geheel is geimplementeerd in een 65nm CMOS technologie, en de meetresultaten worden gepresenteerd.

Het ontwerp van een 60GHz 4-bit active phase shifter wordt ook gepresenteerd, alsmede de integratie met een power amplifier (PA) voor een phased array zender. Dit geheel is geimplementeerd in een 65nm CMOS technologie. Ook hiervan worden meetresultaten gepresenteerd en vergeleken met eerder gepubliceerd werk.

De integratie van een 60GHz CMOS versterker en een antenne op een PCB wordt onderzocht. Experimentele resultaten worden gepresenteerd en besproken.

Acknowledgement

This work could not have been realized without the help and advice of many people. Here I would like to express my deep and sincere gratitude.

First of all, I would like to thank my promotors Prof. Peter Baltus and Prof. Arthur van Roermund. Thank you for offering me an exciting research project, providing me insightful guidance, always believing in me, and always supporting me throughout these years.

I am grateful to the members of my promotion committee Prof. Ton Backx, Prof. John Long, Prof. Bram Nauta, Prof. Jan Bergmans, Prof. Bart Smolders and Dr. Peter Smulders, for their time and insightful suggestions to improve the thesis.

I would like to express my gratitude to Prof. Johan Huijsing and Prof. Kofi Makinwa, for teaching me analog integrated-circuit design during my MSc study, and encouraging me to solve technical problems analytically and creatively. Thank Prof. John long again for teaching me RF integrated-circuit design. I also thank Prof. Larry Larson for offering me a great opportunity as being a visiting scholar in San Diego, California, USA.

My appreciation also goes to the people in NXP Research, for the profound knowledge and professional experience that contribute significantly to the thesis. I am especially grateful to Raf Roovers, Domine Leenaerts, Cicero Vaucher, Edwin van der Heijden, Anton de Graauw, Dennis Jeurissen, Gerard van der Weide, Manel Collados, Ralf Pijper, Mark van der

Heijden, Mustafa Acar, Juan Osorio and Xin He.

I would like to thank all the members of the Mixed-signal Microelectronics group, for the pleasant environment, support and friendship. Special gratitude goes to Hans Hegt, Eugenio Cantatore, Reza Mahmoudi, Piet Klesssens, Margot van den Heuvel, Yu Lin, Wei Deng, Yongjian Tang, Pieter Harpe, Emanuele Lopelli, Dusan Milosevic, Georgi Radulov, Xia Li, Hao Gao, Erwin Janssen, Pooyan Sakian Dezfuli, Maarten Lont, Hammad Cheema, Maja Vidojkovic and Xiaopeng Yu.

I would like to thank SenterNovem for funding the project. Also thanks to my colleagues Iwan Akkermans, Imran Kazim, Xueli An and Dries Neirynck, for the fruitful cooperation in the different research areas of the project.

I sincerely thank Bert Gyselinckx, Harmke de Groot, Kathleen Philips, Guido Dolmans and Margot Nijkamp-Diesfeldt, for offering me a position as a research scientist in IMEC, Eindhoven.

I am also deeply indebted to all other colleagues and friends for lots of happy times.

Last, but certainly not least, I would like to thank my parents, and my wife Nancy, for their unconditional love, support and encouragement.

Biography

Yikun Yu was born in Fujian, China on November 16, 1981. He received the B.Sc. degree in electrical engineering from Tsinghua University, Beijing, China, in 2002, and the M.Sc degree (with honors) in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2005. In September 2005, he started working towards the Ph.D degree at Eindhoven University of Technology, Eindhoven, The Netherlands.

During 2004-2005, he was with Automotive Business Line, Philips Semiconductors, Nijmegen, The Netherlands. During 2007-2009, he was with NXP Semiconductors, Research, Eindhoven, The Netherlands. In 2009, he visited the Department of Electrical and Computer Engineering, University of California at San Diego, California, USA. He joined IMEC, Eindhoven, The Netherlands, in 2009, as a research scientist. His research interests include analog, RF and millimeter-wave integrated circuit design.